IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

TECHNOLOGY PROPERTIES LTD. and PATRIOT SCIENTIFIC CORP., Plaintiffs,	§	
vs.	§	CIVIL ACTION NO. 2:05-CV-494 (TJW)
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD., ET AL., Defendants.	§	

MEMORANDUM OPINION AND ORDER

After considering the submissions and the arguments of counsel, the Court issues the following order concerning the claim construction issues:

I. Introduction

Plaintiffs Technology Properties Limited ("TPL") and Patriot Scientific Corp. accuse multiple defendants of infringing United States Patent Nos. 5,809,336 ("the '336 patent") entitled "High Performance Microprocessor Having Variable Speed System Clock," 6,598,148 ("the '148 patent") entitled "High Performance Microprocessor Having Variable Speed System Clock," and 5,784,584 ("the '584 patent") entitled "High Performance Microprocessor Using Instructions that Operate within Instruction Groups." This opinion resolves the parties' various claim construction disputes.

II. Background of the Technology

The '336 patent discloses a mechanism to improve the speed of microprocessor operations. First, a variable speed clock circuit is fabricated on the same chip as the microprocessor. By placing

the clock circuitry on the microprocessor, the clock will be subject to the same variations in operating conditions as the microprocessor. Second, the slower input/output clock is separated from the system clock.

The '148 patent also discloses a mechanism to improve the speed of the microprocessor. In addition to the on-chip clock described in the '336 patent, the microprocessor of the '148 patent includes memory on a majority of the microprocessor substrate.

The '584 patent addresses a bottleneck problem where the computing speed of the microprocessor depends on how quickly instructions can be loaded from memory into the instruction register of the microprocessor. Microprocessors can only process instructions as fast as the instructions can be loaded from the memory. The '584 patent discloses improvements on how to fetch and decode instructions. This is accomplished by arranging certain instructions into a group and fetching the entire group of instructions into the instruction register. As a result, the microprocessor no longer needs to wait for those instructions to be loaded from memory into the instruction register.

III. General Principles Governing Claim Construction

"A claim in a patent provides the metes and bounds of the right which the patent confers on the patentee to exclude others from making, using or selling the protected invention." *Burke, Inc. v. Bruno Indep. Living Aids, Inc.*, 183 F.3d 1334, 1340 (Fed. Cir. 1999). Claim construction is an issue of law for the court to decide. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 970-71 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996).

To ascertain the meaning of claims, the court looks to three primary sources: the claims, the specification, and the prosecution history. *Markman*, 52 F.3d at 979. Under the patent law, the

specification must contain a written description of the invention that enables one of ordinary skill in the art to make and use the invention. A patent's claims must be read in view of the specification, of which they are a part. *Id*. For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims. *Id*. "One purpose for examining the specification is to determine if the patentee has limited the scope of the claims." *Watts v. XL Sys., Inc.*, 232 F.3d 877, 882 (Fed. Cir. 2000).

Nonetheless, it is the function of the claims, not the specification, to set forth the limits of the patentee's claims. Otherwise, there would be no need for claims. *SRI Int'l v. Matsushita Elec. Corp*., 775 F.2d 1107, 1121 (Fed. Cir. 1985) (en banc). The patentee is free to be his own lexicographer, but any special definition given to a word must be clearly set forth in the specification. *Intellicall, Inc. v. Phonometrics*, 952 F.2d 1384, 1388 (Fed. Cir. 1992). And, although the specification may indicate that certain embodiments are preferred, particular embodiments appearing in the specification will not be read into the claims when the claim language is broader than the embodiments. *Electro Med. Sys., S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 1054 (Fed. Cir. 1994).

This Court's claim construction decision must be informed by the Federal Circuit's decision in *Phillips v. AWH Corporation*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). In *Phillips*, the court set forth several guideposts that courts should follow when construing claims. In particular, the court reiterated that "the *claims* of a patent define the invention to which the patentee is entitled the right to exclude." 415 F.3d at 1312 (emphasis added) (*quoting Innova/Pure Water, Inc. v. Safari Water Filtration Systems, Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). To that end, the words used in a claim are generally given their ordinary and customary meaning. *Id*. The ordinary and customary

meaning of a claim term "is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id*. at 1313. This principle of patent law flows naturally from the recognition that inventors are usually persons who are skilled in the field of the invention. The patent is addressed to and intended to be read by others skilled in the particular art. *Id*.

The primacy of claim terms notwithstanding, *Phillips* made clear that "the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id*. Although the claims themselves may provide guidance as to the meaning of particular terms, those terms are part of "a fully integrated written instrument." *Id*. at 1315 (*quoting Markman*, 52 F.3d at 978). Thus, the *Phillips* court emphasized the specification as being the primary basis for construing the claims. *Id*. at 1314-17. As the Supreme Court stated long ago, "in case of doubt or ambiguity it is proper in all cases to refer back to the descriptive portions of the specification to aid in solving the doubt or in ascertaining the true intent and meaning of the language employed in the claims." *Bates v. Coe*, 98 U.S. 31, 38 (1878). In addressing the role of the specification, the *Phillips* court quoted with approval its earlier observations from *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998):

> Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim. The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction.

Consequently, *Phillips* emphasized the important role the specification plays in the claim construction process.

The prosecution history also continues to play an important role in claim interpretation. The prosecution history helps to demonstrate how the inventor and the PTO understood the patent. *Phillips*, 415 F.3d at 1317. Because the file history, however, "represents an ongoing negotiation between the PTO and the applicant," it may lack the clarity of the specification and thus be less useful in claim construction proceedings. *Id*. Nevertheless, the prosecution history is intrinsic evidence. That evidence is relevant to the determination of how the inventor understood the invention and whether the inventor limited the invention during prosecution by narrowing the scope of the claims.

Phillips rejected any claim construction approach that sacrificed the intrinsic record in favor of extrinsic evidence, such as dictionary definitions or expert testimony. The *en banc* court condemned the suggestion made by *Texas Digital Systems, Inc. v. Telegenix, Inc.*, 308 F.3d 1193 (Fed. Cir. 2002), that a court should discern the ordinary meaning of the claim terms (through dictionaries or otherwise) before resorting to the specification for certain limited purposes. *Id*. at 1319-24. The approach suggested by *Texas Digital*–the assignment of a limited role to the specification–was rejected as inconsistent with decisions holding the specification to be the best guide to the meaning of a disputed term. *Id*. at 1320-21. According to *Phillips*, reliance on dictionary definitions at the expense of the specification had the effect of "focus[ing] the inquiry on the abstract meaning of words rather than on the meaning of the claim terms within the context of the patent." *Id*. at 1321. *Phillips* emphasized that the patent system is based on the proposition that the claims cover only the invented subject matter. *Id.* What is described in the claims flows from the statutory requirement imposed on the patentee to describe and particularly claim what he or she has invented. *Id*. The definitions found in dictionaries, however, often flow from the editors'

objective of assembling all of the possible definitions for a word. *Id*. at 1321-22.

Phillips does not preclude all uses of dictionaries in claim construction proceedings. Instead, the court assigned dictionaries a role subordinate to the intrinsic record. In doing so, the court emphasized that claim construction issues are not resolved by any magic formula. The court did not impose any particular sequence of steps for a court to follow when it considers disputed claim language. *Id*. at 1323-25. Rather, *Phillips* held that a court must attach the appropriate weight to the intrinsic sources offered in support of a proposed claim construction, bearing in mind the general rule that the claims measure the scope of the patent grant. The court now turns to a discussion of the relevant claim terms.

IV. Discussion

Claim 1 of the '336 patent, Claim 1 of the '148 patent, and Claim 29 of the '584 patent are representative of how the terms in dispute are used in the asserted claims. Claim 1 of the '336 patent is an independent apparatus claim. It provides:

> A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.

Claim 1 of the '148 patent is an independent apparatus claim. It provides:

> A microprocessor integrated circuit comprising:
>
> a program-controlled processing unit operative in accordance with a sequence of program

instructions;

a memory coupled to said processing unit and capable of storing information provided by said processing unit;

a plurality of column latches coupled to the processing unit and the memory, wherein, during a read operation, a row of bits are read from the memory and stored in the column latch; and

a variable speed system clock having an output coupled to said processing unit;

said processing unit, said variable speed system clock, said plurality of column latches, and said memory fabricated on a single substrate, said memory using a greater area of said single substrate than said processing unit, said memory further using a majority of a total area of said single substrate.

Claim 29 of the '584 patent is a method claim. It provides:

In a microprocessor system including a central processing unit, memory, and an instruction register, a method for providing instructions and operands from said memory to said central processing unit comprising the steps of:

providing instruction groups to said instruction register from said memory wherein certain of said instruction groups include at least one instruction that, when executed, causes an access to an operand or an instruction or both, said operand or instruction being located at a predetermined position from a boundary of said instruction groups;

decoding said at least one instruction to determine said predetermined position;

locating said predetermined position; and

supplying, from said instruction groups, using the predetermined location, said operand or instruction or both to said central processing unit.

A. Agreed Construction

The parties have agreed to the construction of the following terms.

1. '336 Patent

"Oscillator" means "a circuit capable of maintaining an alternating output."

"On-chip input/output interface" means "a circuit having logic for input/output

communications, where that circuit is located on the same semiconductor substrate as the CPU (claims 1-2, 6-10) or the microprocessor (claims 3-5)."

"Integrated circuit" means "a miniature circuit on a single semiconductor substrate."

"External memory bus" means "a group of conductors coupled between the I/O interface and an external storage device."

2. '148 Patent

"Integrated circuit substrate" means "a single supporting material upon or within which is formed a miniature circuit."

3. '584 Patent

"Instruction" means "a command to a processor that tells the processor what operation to perform."

"Boundary of said instruction groups" means "beginning or end of an instruction group."

"Supplying, from said instruction groups, using the predetermined location, said operand or instruction or both to said central processing unit" means "using the results of the locating step in the step of transferring the bits from the accessed operand or instruction to the central processing unit."

"Instruction register" means "a hardware element that receives and holds an instruction group as it is extracted from memory; the register either contains or is connected to circuits that interpret the instructions in the group."

B. Disputed Constructions

1. '336 Patent

a. "central processing unit"

The first term for construction is "central processing unit." The plaintiffs propose "an electronic circuit that controls the interpretation and execution of programmed instructions." The defendants propose "the central electronic circuit in a computer that controls the interpretation and execution of programmed instructions." There are two main disputes - 1) whether the circuit needs to be in a computer and 2) whether the circuit needs to be the "central electronic circuit."

In support of their construction, the plaintiffs argue that the specification teaches that the microprocessor can be used in applications other than a computer (e.g., HDTV and automobiles). '336 patent, 9:61-10:12. The plaintiffs also observe that the specification states that the microprocessor can be part of a multiprocessor system and, therefore, no one CPU is the "central electronic circuit" for the computer. *See* '336 patent, 11:64-12:4. The defendants, on the other hand, argue that they did not intend to limit the use of the CPU to a computer. They assert, however, that a CPU must be part of a computer chip.

The parties appear to agree that one of ordinary skill in the art would understand that a computer chip or other integrated circuit can be used in various devices, such as automobiles or televisions. The Court construes the term to mean "an electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions."

b. "microprocessor"

The plaintiffs propose "an electronic circuit that executes programmed instructions and is capable of interfacing with input/output circuitry and/or memory circuitry." The defendants propose

"an electronic circuit that uses a central processing unit to interpret and execute programmed instructions." The main disputes are whether the microprocessor must be capable of interfacing with input/output circuitry and/or memory circuitry, and whether the microprocessor needs to use a central processing unit.

The plaintiffs argue that the patent discloses a microprocessor that communicates with memory circuitry. '336 patent, 8:56-58, 11:49-54. The plaintiffs also argue that the claim language does not support the fact that a microprocessor is required to use a central processing unit because claim 3 does not recite the use of a central processing unit whereas all other independent claims require the use of a central processing unit.

The defendants argue that one of ordinary skill in the art would understand that microprocessors include a central processing unit. In addition, the defendants contend that not all microprocessors need to interface with input/output circuitry because some microprocessors communicate solely with external memory. The defendants also contend that microprocessors do not need to connect to external memory because some microprocessors rely solely on on-chip memory.

The Court is not persuaded that the additional limitations proposed by the plaintiffs or the defendants are appropriate. The input/output interface and the central processing unit limitations are included in other portions of the claims and, therefore, adding those limitations to the construction would be superfluous. *See, e.g.,* '336 patent, 32:12-13, 25-26. The Court construes "microprocessor" to mean "an electronic circuit that interprets and executes programmed instructions."

c. "ring oscillator"

The next term is "ring oscillator." The plaintiffs contend that this term means "an oscillator having a multiple, odd number of inversions arranged in a loop." The defendants propose "an [oscillator] having an odd number of inverting logic stages connected in a loop." The main dispute is whether a ring oscillator is required to have multiple inverters or whether it can have just one.

The plaintiffs argue that a single inverter would not be appropriate because it could not maintain an oscillating output. The defendants, on the other hand, rely on extrinsic evidence to support their proposed construction. Specifically, the defendants cite to a semiconductor textbook depicting a ring oscillator with only one inverter.

The plaintiffs have the better argument. The extrinsic evidence cited by the defendants also supports the plaintiffs' construction. It states that timers are built as "chains of inverters," not just one inverter. Defendants' Claim Construction Brief, Ex. U, MEAD & CONWAY, INTRODUCTION TO VLSI SYSTEMS (1980), at 234. Accordingly, the Court adopts the plaintiffs' proposed construction.

d. "an entire ring oscillator variable speed system clock in said integrated circuit"

The plaintiffs argue that this term means "a ring oscillator that generates the signal(s) used for timing the operation of the CPU, capable of operating at speeds that can change, where the ring oscillator is located entirely on the same semiconductor substrate as the CPU." The defendants' proposed construction is "a [ring oscillator variable speed system clock] that is completely on-chip and does not rely on a control signal or an external crystal/clock generator." The dispute is whether the ring oscillator may rely on a control signal or an external crystal/clock generator.

In support of their construction, the defendants argue that the applicant disclaimed use of a

control signal and a external crystal/clock generator in order to distinguish over prior art. The plaintiffs contend that it did not disclaim all types of control signals, such as voltage and current controlled oscillators; there was only a disclaimer of the more narrow "command input." In addition, the plaintiffs argue that, although an external crystal is not directly used to generate a system clock signal, the external crystal can be used as a reference signal to account for delay across certain circuit elements.

The Court agrees with the defendants that the applicant disclaimed the use of an input control signal and an external crystal/clock generator to generate a clock signal. *See* Response to Office Action, April 11, 1996, at 8; Response to Office Action, January 13, 1997, at 4; Response to Office Action, July 7, 1997, at 3-4. Accordingly, the Court construes the term to mean "a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not directly rely on a command input control signal or an external crystal/clock generator to generate a clock signal."

e. "variable speed"

The next term is "variable speed." The plaintiffs' proposed construction is "capable of operating at speeds that can change." The defendants argue that the term means "a speed (frequency) that is not tightly controlled and varies more than minimally."

The plaintiffs contend that the specification discloses a ring oscillator that is capable of operating at various speeds based on variations in operating conditions. '336 patent, 16:59-63. The plaintiffs also argue that the defendants' proposed construction is too restrictive. The defendants, on the other hand, point to the prosecution where the applicant describes fixed-frequency as a speed that is "tightly controlled" and "var[ies] minimally." Amendment, July 7, 1997, at 3-4. According

to the defendants, "variable speed" is the opposite of fixed-frequency.

Notwithstanding the defendants' arguments, one of ordinary skill in the art would understand "variable speed" to describe a component capable of operating at different speeds. Accordingly, the Court construes the term to mean "capable of operating at different speeds."

f. "system clock" and "variable speed clock"[1]

The plaintiffs propose "a circuit that generates the signal(s) used for timing the operation of the CPU." The defendants contend that the term means "a circuit that is itself responsible for determining the frequency of the signal(s) used for timing the operation of the CPU." The dispute is whether the circuit alone is responsible for determining the frequency of the signal.

A system clock does not generate the signal alone because the timing can be derived from the ring oscillator. '336 patent, 16:63-67. Accordingly, the Court adopts the plaintiffs' proposed construction.

g. "oscillator . . . clocking"

The plaintiffs contend that no construction is necessary, but if a construction is required, they propose "the oscillator generates the signal(s) used for timing the operation of the CPU." The defendants propose "an oscillator that is itself determining the frequency of the signal(s) used for timing."

The Court agrees that the term requires construction. The Court construes the term to mean "an oscillator that generates the signal(s) used for timing the operation of the CPU."

h. "processing frequency"

The plaintiffs propose "the speed at which the CPU operates." The defendants propose

[1] The parties appear to agree that these two terms should have the same construction.

"fastest safe operating speed." The issue is whether the term refers to the "fastest safe operating speed."

The plaintiffs contend that the specification uses the language "maximum possible frequency" with regard to one embodiment of the CPU. The plaintiffs also point out that "fastest safe operating speed" was mentioned in response to an office action. Response to Office Action, January 8, 1997, at 4. The response to the office action states that the present invention provides

> a variable speed clock for the microprocessor, with the clock speed varying in the same way as variations in the operating characteristics of the electronic devices making up the microprocessor. This allows the microprocessor to operate at its fastest safe operating speed, given its manufacturing process or changes in its operating temperature or voltage. *Id*. at 3-4.

According to the plaintiffs, this does not mean that the CPU must operate at the fastest safe operating speed, but that it is capable of operating at its fastest safe operating speed.

In support of their proposed construction, the defendants point to the specification which states that the "CPU will always execute at the maximum frequency possible, but never too fast." '336 patent, 17:1-2. The defendants also point to a portion of the prosecution history which states that

> these claims further state that the plurality of transistors included within the ring oscillator clock have operating characteristics which vary similarly to operating characteristics of transistors included within the microprocessor, thereby enabling the processing frequency of the microprocessor to track the speed of the ring oscillator clock: '...CPU clock 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process. Response to Office Action, April 11, 1996, at 8-9.

Frequency is not limited to the fastest safe operating speed. The portion of the prosecution history cited by the defendants refers to varying the processing frequency based on operating

conditions. In the Court's view, the applicants did not clearly define or limit the term "processing frequency." Accordingly, the Court adopts the plaintiffs' proposed construction.

i. "processing frequency capability"

The plaintiffs propose "the range of speeds at which the CPU can operate." The defendants propose "fastest safe operating speed at which the CPU can operate."

As discussed in the previous section, "processing frequency" is not limited to the "fastest safe operating speed." In addition, "capability" is not limited to a range or to the fastest speed. Accordingly, the Court construes the term to mean "the speeds at which the CPU can operate."

j. "varying together"[2]

The next term is "varying together." The plaintiffs contend that the term means "both increase or both decrease." The defendants' proposed construction is "increasing and decreasing by the same amount." The dispute is whether this term is limited to "the same amount."

The defendants claim that the only way for the invention to work is to match the clock speed to the CPU's processing speed capability. According to the defendants, if the frequency capability increased from 50 MHz to 100 MHZ but the clock rate only increased from 25 MHz to 150 MHZ, then the CPU would not be operable. In addition, the defendants argue that there are numerous statements in the prosecution history stating that the processing frequency should "track" or "vary correspondingly with" the clock rate. *See* Response to Office Action, April 11, 1996, at 6, 8; Response to Office Action, January 8, 1997, at 4.

There is no limitation in the intrinsic evidence requiring the variation between the frequency

[2] This construction would also include the terms "vary together," "varying . . . in the same way," and "varying in the same way."

capability and the clock to match exactly. The Court construes the term to mean "increasing and decreasing proportionally."

k. "second clock"

The plaintiffs' proposed construction is "a clock not derived from the first clock." The defendants contend that no construction is necessary, but if construction is necessary, then they propose "another clock."

The plaintiffs argue that the claims state that the second clock is independent of the first clock. According to the plaintiffs, a second clock derived from the first clock would not be independent as required by the claims.

The defendants appear to agree that the first clock is independent of the second clock. In any event, the independence of the second clock is required by the claim language. Accordingly, the Court declines to construe this term.

l. "external clock"

The plaintiffs propose "a clock not derived from the first clock, and which is not originated on the same semiconductor substrate upon which the entire variable speed clock is located." The defendants contend that no construction is necessary, but if a construction is necessary, then they propose "a clock not on the integrated circuit substrate."

As discussed previously, the defendants appear to agree that, like the second clock, the external clock is independent of the first clock. The plaintiffs' proposed construction includes limitations already in the claims. The Court construes "external clock" to mean "a clock not on the integrated circuit substrate."

m. "second clock independent of said ring oscillator . . . system clock" and "second clock independent of the ring oscillator system clock"

The plaintiffs propose "a change in the frequency of the ring oscillator does not affect the frequency of the second clock." The defendants propose "a second clock wherein a change in the frequency of one of the second clock or the ring oscillator system clock does not affect the frequency of the other." The dispute is whether the term "independent" means "one-way independence" or "two-way independence."

The plaintiffs argue that the specification only refers to one-way independence because it describes the situation where the I/O clock has a fixed speed while the CPU clock has a variable speed. According to the plaintiffs, there is no discussion about the situation where the I/O clock speed can be modified without affecting the CPU clock speed; the specification only states that varying the CPU clock speed would not affect the I/O clock speed.

The defendants argue that the plaintiffs' construction would conflict with the purpose of the invention of having a first clock function independently from the second clock. According to the defendants, the specification describes the first and second clock as functioning independently from one another.

The defendants have the better argument. One of ordinary skill in the art would understand the term "independence" to mean "two-way independence." Accordingly, the Court construes the term to mean "a second clock wherein a change in the frequency of either the second clock or ring oscillator system clock does not affect the frequency of the other."

n. "external clock is operative at a frequency independent of a clock frequency of said oscillator"

The plaintiffs propose "a change in the frequency of the oscillator (claims 6-9) or the variable

speed clock (claim 10) does not affect the frequency of the external clock." The defendants propose "an external clock wherein a change in the frequency of one of the external clock or oscillator does not affect the frequency of the other (claim 6)."

The Court construes the term to mean "an external clock wherein a change in the frequency of either the external clock or oscillator does not affect the frequency of the other."

o. "fixed frequency"

The plaintiffs contend that no construction is necessary, but if the court determines that a construction is needed, then they propose "a non-variable frequency." The defendants propose "having a speed that is tightly controlled and varies minimally." This term is not a technical term and can be understood according to its plain and ordinary meaning. Accordingly, the Court declines to construe this term.

2. '148 Patent

a. "processing unit"

The plaintiffs propose "an electronic circuit that controls the interpretation and execution of programmed instructions." The defendants do not appear to dispute the plaintiffs' proposal. Accordingly, the Court adopts the plaintiffs' proposed construction.

b. "memory" and "a memory"

The plaintiffs propose "all of the storage elements on the substrate and the control circuitry configured to access the storage elements." The defendants claim that this term is indefinite, but if construction is possible, they propose "an information storing array that does not include registers,

cache or column latches."[3] The main dispute appears to be whether or not memory can include registers, cache, or column latches.

The defendants contend that "memory" and "column latches" must have different meanings because when two claim terms are used, they are presumed to mean different things. *See* '148 patent, claim 1. The defendants, therefore, argue that "memory" cannot include "column latches." The defendants also point out that the specification recognizes that latches, registers and cache can exist within the CPU which is separate from the memory. *See* '148 patent, 4:5-10, 4:14-19, 5:58-60.

The plaintiffs contend that the specification describes DRAM to include registers and column latches. '148 patent, 8:65-9:4. The defendants, moreover, agree that registers, cache, and column latches may be considered part of the memory when they are included in the storage array. Defendants' Responsive Claim Construction Brief, at 34.

In the Court's view, the plaintiffs' proposal is too broad because it would include storage elements that are within the CPU. On the other hand, the defendants' proposed construction is too limiting because it would exclude registers and cache that one of ordinary skill in the art would consider to be types of memory. The claim language, however, does indicate that "memory" does not include "column latches." "Memory" and "column latches" are two distinct elements in Claim 1 of the '148 patent. The claim also states, in relevant part, that "a plurality of column latches [is] coupled to . . . the memory . . . ." '148 patent, 31:11-12. If "memory" included "column latches," then the claim would not need to specify that "column latches" are coupled to the "memory." Accordingly, the Court construes "memory" to mean "storage elements other than column latches."

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[3] The defendants do not present their arguments for indefiniteness in their claim construction briefing.

c. "total area of said single substrate" or "total area of said substrate"

The plaintiffs propose "the total surface of the supporting material upon or within which is formed an interconnected array of circuit elements." The defendants propose "area enclosed by the outermost edges of the substrate." This term is used in the context of memory which is claimed to occupy "a majority" of the "total area" of the substrate. The issue is what constitutes the "area."

The plaintiffs argue that the defendants' proposal would include areas of the substrate that are not being actively used (e.g., the sides and back of the substrate). According to the plaintiffs, the proper approach is to refer to the portion of the substrate that has active circuitry as depicted in Figure 9 of the '148 patent.

The area of the substrate refers to the top portion of the substrate, and not the sides or back. *See* '148 patent, Fig. 9. The Court construes the term to mean "the total top surface area of the substrate."

d. "area of said single substrate" or "area of said substrate"

The Court construes this term to mean "the top surface area of the substrate."

e. "variable"

This is not a technical term that requires construction and may be understood according to its plain and ordinary meaning. The Court declines to construe this term.

f. "system clock"

The Court adopts its previous construction of this term in the '336 patent. *See* Section IV(B)(1)(f).

g. "ring oscillator"

The Court adopts its previous construction of this term in the '336 patent. *See* Section IV(B)(1)(c).

h. "a ring oscillator having a variable output frequency"

The Court adopts its previous construction of "ring oscillator" in the '336 patent. *See* Section IV(B)(1)(c). No further construction of this term is necessary.

i. "the [ring oscillator] disposed on said integrated circuit substrate"

The Court adopts its previous construction of "ring oscillator" in the '336 patent. *See* Section IV(B)(1)(c). No further construction of this term is necessary.

j. "interface ports for interprocessor communication"

The plaintiffs contend that no construction is necessary. Alternatively, if a construction is needed, then the plaintiffs propose "channels through which data can be transferred between two separate processing units." The defendants propose "channels through which data is transferred between two separate processing units." The dispute is whether the interface ports may be used for purposes other than to transfer data.

The defendants argue that the plaintiffs' construction would allow the interface ports to be used for any purpose and render the words "for interprocessor communication" meaningless. The plaintiffs contend that the specification describes interface ports for use other than interprocessor communication. *See* '148 patent, 9:64-10:12.

One of ordinary skill in the art would understand that interface ports are not limited solely to the transfer of data. The Court construes the term to mean "channels through which data is allowed to be transferred between two separate processing units."

3. '584 Patent

a. "microprocessor"

The Court adopts its previous construction of this term in the '336 patent. *See* Section IV(B)(1)(b).

b. "central processing unit"

The Court adopts its previous construction of this term in the '336 patent. *See* Section IV(B)(1)(a).

c. "instruction groups"

The next term is "instruction groups." The plaintiffs' proposed construction is "sets of from 1 to a maximum number of sequential instructions, each set being provided to the instruction register as a unit and having a boundary." The defendants propose "sets of from 1 to a maximum number of sequential instructions, in which the execution of the instruction depends on each set being provided to the instruction register as a unit and in which any operand that is present must be right justified and which cannot encompass a single 32-bit traditional conventional instruction." The dispute is whether an operand that is present in the instruction group must be right justified and whether the instruction group may encompass a single 32-bit traditional conventional instruction.

The plaintiffs contend that right justified operands are a feature of the preferred embodiment. The plaintiffs also argue that the claim language was broadened during prosecution history when the language "selecting, in accordance with position in said instruction register of one of said instructions of one of said instruction groups, an operand from said one of said instruction groups" was removed from the claim. Amendment, June 12, 1997, at 6. In addition, the plaintiffs point out that the specification includes 32-bit instructions. *See* '584 patent, 20:41-42.

The defendants argue that the specification states that "operands must be right justified in the instruction register." '584 patent, 16:15-16. In addition, the defendants argue that the applicants limited operands in this manner to overcome prior art rejections. *See* Amendment, June 17, 1997, at 13; Amendment, February 5, 1998, at 7. The defendants also contend that although the specification includes 32-bit instructions, the specification never identifies a *single* 32-bit instruction as instruction *groups*. According to the defendants, the specification defines "instruction group" as "being 8-bit and 16 or 24-bit instructions." '584 patent, 23:4-7.

The specification and prosecution history refer to the fact that operands in the instruction register must be right justified. The applicants, however, did not exclude a single 32-bit instruction as an instruction group. In a preferred embodiment, a microprocessor fetches instructions "in 32-bit chunks called 4-byte instruction groups" where an "instruction group may contain from one to four instructions." '584 patent, 23:4-5, 19:18-19. If a 4-byte (or 32-bit) instruction group contains one instruction, then the instruction group may contain a single 32-bit instruction. The Court construes "instruction groups" to mean "sets of from 1 to a maximum number of sequential instructions, each set being provided to the instruction register as a unit and having a boundary, and in which any operand that is present must be right justified."

d. "operand"

The plaintiffs argue that the term means "an input to an operation specified by an instruction that is encoded as part of the instruction." The defendants propose "an input to a single operation specified by an instruction that is encoded as part of the instruction where the size of the input can vary depending on the value of the input."

The plaintiffs argue that the defendants' proposed construction would exclude a preferred

embodiment which includes fixed length operands. *See* '584 patent, 29:62-27:7. However, the plaintiffs appear to agree that the size of the input can vary.

The intrinsic evidence does not show a clear limitation where the size of the input needs to vary depending on the value of the input. The Court construes the term to mean "an input to a single operation specified by an instruction that is encoded as part of the instruction where the size of the input can vary."

e. "said instruction groups include at least one instruction that, when executed, causes an access to an operand or instruction or both"

The plaintiffs propose "the instruction being executed causes the CPU to use an immediate operand or execute a second instruction which is not the next sequential instruction." The defendants' proposed construction is "the instruction being executed causes the CPU to use data or execute a second instruction." The main dispute is whether the second instruction can be the next sequential instruction.

The plaintiffs argue that one of ordinary skill in the art would regard the normal program flow of going from one instruction to the next sequential instruction as "causing an access to an instruction." The defendants contend that the specification describes a SKIP instruction where the second instruction accessed is the next sequential instruction. '584 patent, 23:12-14. In reply, the plaintiffs contend that claim 29 refers to control flow instructions, not ordinary instructions.

The intrinsic evidence does not support the limitation proposed by the plaintiffs. Accordingly, the Court construes the term to mean "the instruction being executed causes the CPU to use an operand or execute a second instruction."

f. "said operand or instruction being located at a predetermined position from a boundary of said instruction groups"

The plaintiffs propose "the immediate operand or the instruction that is accessed has a position, relative to the beginning or end of the instruction group that includes the operand or instruction being accessed, that is determined based on a portion of an accessing instruction that identifies an operation to be performed and without reference to operand or address bits in the accessing instruction." The defendants propose "the bits forming the accessed operand or instruction either begin or end at a position defined in relation to the boundaries of the instruction group in the instruction register rather than the currently executing instruction." The principal dispute is whether the instruction group refers to the group in which the currently executing instruction is located or whether it refers to the group in which the instruction or operand being accessed is located.

The plaintiffs argue that, during prosecution, the applicants referred to the predetermined position of the *accessed* operand or instruction. *See* Supplemental Amendment, February 5, 1998, at 6-8. The plaintiffs also argue that instruction location is determined based on the particular place for instructions of that type. In addition, the plaintiffs contend that the target address specified by the instruction has no effect on the decision to begin executing at the beginning boundary of a target group.

The defendants argue that the Abstract explains the meaning of this phrase. It states

> A high-performance microprocessor system using instruction that access operands and instructions located relative to the current instruction group rather than located relative to the current instructions, as is the convention, is disclosed herein. '584 patent, Abstract.

The defendants also contend that the plaintiffs add limitations that are not supported by the intrinsic evidence.

In reply, the plaintiffs contend that the term "current" in the Abstract refers to the target group, not the accessing group. For example, one of ordinary skill in the art would, in the case of a BRANCH instruction, determine the target instruction relative to the boundary of the target group, not the accessing group.

A "predetermined position" refers to a position based on the instruction group being accessed. *See* '584 patent, 2:29-35. The Court construes the term to mean "the operand or instruction is accessed at a position defined in relation to the boundaries of the instruction group that includes the operand or instruction being accessed."

g. "decoding said at least one instruction to determine said predetermined position"

The plaintiffs contend that the term means "interpreting an instruction, in particular the portion thereof that signifies the operation to be performed, in order to identify a position relative to the beginning or end of the instruction group that includes the operand or instruction being accessed, without reference to the operand or address bits in the instruction being interpreted." The defendants propose "interpreting an instruction, in particular the portion thereof that signifies the operation to be performed, in order to identify a position relative to the beginning or end of the current instruction group."

The Court construes the term to mean "interpreting an instruction, in particular the portion therefor that signifies the operation to be performed, in order to identify a position relative to the beginning or end of the instruction group that includes the operand or instruction being accessed."

h. "locating said predetermined position"

The next term is "locating said predetermined position." The plaintiffs argue that this term

means "establishing operand or instruction supply within the instruction group that includes the operand or instruction being accessed at the predetermined position." The defendants argue that the term means "using the results of the decoding step to ascertain the address of the accessed operand or instruction by referencing the current instruction group address rather than the current executing instruction address without adding or subtracting an operand with the current Program Counter." The parties make similar arguments with regards to "predetermined position" as discussed in the previous section.

The plaintiffs oppose the additional limitation in the defendants' proposed construction of "without adding or subtracting an operand with the current Program Counter." According to the plaintiffs, this would exclude a preferred embodiment from the specification stating that the processor "treats the three operands similarly by adding or subtracting them to the current program counter." '584 patent, 11:13-15. In support of this additional limitation, the defendants argue that additions and subtractions are done only at assembly/linking and not at run time. *See* '584 patent, 20:43-50.

The defendants' construction improperly incorporates a limitation from the preferred embodiment. The Court construes the term to mean "locating the operand or instruction within the instruction group that includes the operand or instruction being accessed at the predetermined position."

V. Conclusion

The Court adopts the constructions set forth in this opinion for the disputed terms of the '336 patent, the '148 patent, and the '584 patent. The parties are ordered that they may not refer, directly or indirectly, to each other's claim construction positions in the presence of the jury. Likewise, the parties are ordered to refrain from mentioning any portion of this opinion, other than the actual

definitions adopted by the Court, in the presence of the jury. Any reference to claim construction proceedings is limited to informing the jury of the definitions adopted by the Court.

SIGNED this 15th day of June, 2007.

T. JOHN WARD
UNITED STATES DISTRICT JUDGE