Volume I of II, Pages A1 to A7288

Nos. 2014-1076, -1317

United States Court of Appeals for the Federal Circuit

HTC CORPORATION and HTC AMERICA, INC.,

Plaintiffs-Cross-Appellants,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED,

Defendants-Appellants.

Appeals from the United States District Court for the Northern District of California in Case No. 5:08-cv-00882-PSG,
United States Magistrate Judge Paul S. Grewal

CORRECTED NON-CONFIDENTIAL JOINT APPENDIX

James C. Otteson
Thomas T. Carmack
Philip W. Marsh
AGILITY IP LAW, LLP
149 Commonwealth Dr.
Menlo Park, CA 94025
(650) 227-4800

Attorneys for Defendants-Appellants Technology Properties Limited, Patriot Scientific Corporation and Alliacense Limited

Heidi L. Keefe
Mark R. Weinstein
Kyle D. Chen
COOLEY LLP
3175 Hanover Street
Palo Alto, CA 94306-2155
(650) 843-5000

Stephen R. Smith
COOLEY LLP
One Freedom Square
Reston Town Center
11951 Freedom Drive
Reston, VA 20190-5656
(703) 456-8000

Attorneys for Plaintiffs-Cross-Appellants HTC Corporation and HTC America, Inc.

October 8, 2014

TABLE OF CONTENTS

CONFIDENTIAL MATERIAL OMITTED

Pages A7125, A7152, A7161-A7163, and A7199-A7200 have been omitted from this non-confidential version of the Joint Appendix. The material on those pages was designated by HTC as confidential under the protective order dated April 21, 2010. They contain the damages expert's opinion based on confidential financial information.

Pages A9041, and A9054 have been omitted from this non-confidential version of the Joint Appendix. The material on those pages was designated by HTC as confidential under the protective order dated April 21, 2010. They contain HTC's confidential technical information.

Pages A9043-A9045, A9050-A9052, A9065-A9066, A9072-A9073, and A9316-A9317 have been omitted from this non-confidential version of the Joint Appendix. The material on those pages was designated by Qualcomm as confidential under the protective orders dated April 21, 2010 and May 17, 2011. They contain Qualcomm's confidential technical information.

Pages A9056-A9058, and A9068-A9069 have been omitted from this non-confidential version of the Joint Appendix. The material on those pages was designated by Texas Instruments as confidential under the protective order dated April 21, 2010. They contain Texas Instruments' confidential technical information.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, et al.,

Defendants.

Case No.: 5:08-cv-00882-PSG

ORDER RE: HTC'S MOTIONS FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT AND NO WILLFULNESS

(Re: Docket Nos. 457, 458)

Before the court in this patent case are two motions for summary judgment brought by Plaintiffs HTC Corporation and HTC America, (collectively "HTC"). HTC first moves for "full" summary judgment of non-infringement and no willful infringement of U.S. Patent No. 5,809,336 ("the '336 patent"). HTC separately moves for partial summary judgment of non-infringement of the '336 patent and U.S. Patent No. 5,530,890 ("the '890 patent") and no willful infringement of the '890 patent. On August 13, 2013, the parties appeared for a hearing. Having considered the papers and arguments of counsel:

The court DENIES HTC's motion for summary judgment of "full" non-infringement of the '336 patent.

The court DENIES HTC's motion for partial summary judgment of non-infringement of the '336 patent.

The court DENIES HTC's motion for summary judgment of no willful infringement of the '336 patent.

The court GRANTS HTC's motion for partial summary judgment of non-infringement of the '890 patent.

The court GRANTS-IN-PART HTC's motion for partial summary judgment of no willful infringement of the '890 patent.

The court sets forth its reasoning below.

I. BACKGROUND

HTC Corporation is a Taiwan corporation with its principal place of business in Taoyuan, Taiwan, R.O.C. HTC's subsidiary, HTC America, is a Texas corporation with its principal place of business in Bellevue, Washington. Defendants Technology Properties Limited and Alliacense, Limited ("Alliacense") are California corporations with their principal place of business in Cupertino, California; Patriot Scientific Corporation ("Patriot") is a Delaware corporation with its principal place of business in Carlsbad, California. These defendants – Technology Properties Limited, Alliacense, and Patriot (collectively "TPL") – claim ownership of a family of related microprocessor patents. TPL refers to those patents as the Moore Microprocessor Portfolio patents ("MMP patents"), in recognition of co-inventor Charles Moore's contributions. HTC filed this suit on February 8, 2008, seeking a judicial declaration that four of the MMP patents – U.S. Patent Nos. 5,809,336 ("the '336 patent"), 5,784,584 ("the '584 patent"), 5,440,749 ("the '749 patent"), and 6,598,148 ("the '148 patent") – are invalid and/or not infringed.[1] TPL counterclaimed for

[1] *See* Docket No. 1.

infringement of the '336, '749, '148, and '890 patents on November 21, 2008.[2] On April 25, 2008, TPL filed two complaints in the Eastern District of Texas against HTC alleging infringement of the four patents at issue in the pending declaratory judgment action.[3] On June 4, 2008, TPL filed additional patent infringement actions against HTC in the Eastern District of Texas asserting U.S. Patent No. 5,530,890 ("the '890 patent").[4] On July 10, 2008, HTC amended its complaint before this court, adding claims for declaratory relief with respect to the '890 patent.[5] On February 23, 2009 the parallel Texas litigation was dismissed without prejudice following Judge Fogel's decision to deny TPL's Motion to Dismiss, or in the Alternative, to Transfer Venue in the California action.[6] On March 25, 2010, the court accepted the parties' stipulation to dismiss the '584 patent from this litigation.[7] On August 24, 2012, Technology Properties Limited, Patriot, and Phoenix Digital Solutions initiated an International Trade Commission ("ITC") investigation regarding HTC's alleged infringement of the '336 patent.[8] On July 17, 2013, the court accepted the parties' stipulation to dismiss the '148 and '749 patents from this litigation.[9]

The bottom line is that only the '336 and '890 patents remain at issue for the purposes of this litigation.

A. The '336 Patent

---

[2] *See* Docket No. 60 at 6-8.

[3] *See* Docket No. 16 at 3.

[4] *See* Docket No. 35 at 5.

[5] *See* Docket No. 34.

[6] See Docket Nos. 49 (denying motion to dismiss, to transfer venue, and to stay) and 88 (granting motion for leave to file motion for reconsideration and denying motion for reconsideration).

[7] *See* Docket No. 152.

[8] *See* Docket No. 561-1. Claims 1, 6, 7, 9-11, and 13-16 were asserted in the investigation. On September 6, 2013, Administrative Law Judge James Gildea issued an Initial Determination from in the ITC proceeding holding that HTC did not violate Section 337 of the Tariff Act of 1930. *See id.*

[9] *See* Docket No. 462.

The '336 patent issued on September 15, 1998 and describes a microprocessor with an internal variable speed clock, or oscillator, that drives the processor's central processing unit ("CPU"). Traditional microprocessors use external, fixed speed crystals to clock the CPU. A CPU's maximum possible processing capacity depends on process, voltage, and temperature ("PVT parameters"). An external clock must therefore set the timing of the CPU to suboptimal PVT conditions, resulting in waste of the CPU's processing speed under optimal conditions. The internal, variable clock described in the '336 patent claims real-time adjustment of the timing of the CPU by placing the clock on the chip itself. Thus, the CPU can perform optimally under any set of parameters. The microprocessor nevertheless requires a second external clock because devices other than the CPU do not operate at variable speed.

TPL claims that HTC's accused products infringe the '336 patent by their internal, variable speed oscillator on their microprocessors. At issue are claims 1, 6, 10, 11, 13, and 16.[10]

Claim 1 provides:

> A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.

Claim 6 provides:

> A microprocessor system comprising:

[10] Docket No. 494 at 7.

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices; an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.

Claim 10 provides:

In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of: providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency; providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors; clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate; connecting an [on chip] on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock and wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock.

Claim 11 provides:

A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator

variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperatureof said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein said central processing unit operates asynchronously to said input/output interface.

Claim 13 provides:

A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices; an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and further wherein said central processing unit operates asynchronously to said input/output interface.

Claim 16 provides:

In a microprocessor system including a central processing unit, a method for locking said central processing unit comprising the steps of providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency; providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors; clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate; connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus,

and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock, wherein said central processing unit operates asynchronously to said input/output interface.

B. The '890 Patent

The '890 patent first issued on June 25, 1996 and originally included ten claims, nine of which depended from the sole independent claim, claim 1.[11] On January 19, 2009, the '890 patent was subjected to ex parte reexamination.[12] An amended version of the patent emerged on March 1, 2011.[13] The reexamination proceeding resulted in the cancellation of claims 1-4, confirmation of the patentability of claims 5-10, and addition of claims 11-20. At issue in this suit are claims 11, 12, 13, 17, and 19.[14]

Claim 11, the amended independent claim on which all of the other claims depend, describes:

> A microprocessor, which comprises a main central processing unit and a separate direct memory access central processing unit in a single integrated circuit comprising said microprocessor, said main central processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus, said internal data bus being bidirectionally connected to a loop counter, said loop counter being connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register, said stack pointer pointing into said first push down stack, said internal data bus being connected to a memory controller, to a Y register of a return push down stack, an X register and a program counter, said Y register, X register and program counter providing outputs to an internal address bus, said internal address bus providing inputs to said memory controller and to an incrementer, said incrementer being connected to said internal data bus, said direct memory access central processing

[11] *See* Docket No. 458 at 2.

[12] *See id.*

[13] *See id.*

[14] *See id.*

unit providing inputs to said memory controller, said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory.

During reexamination, the patentee added the phrase "said stack pointer pointing into said first push down stack," which did not appear in claim 1.

II. SUMMARY JUDGMENT STANDARDS

Summary judgment is appropriate only if there is "no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law."[15] The moving party bears the initial burden of production by identifying those portions of the pleadings, discovery, and affidavits which demonstrate the absence of a triable issue of material fact.[16] The standard for summary judgment differs depending on whether the moving party bears the burden of persuasion at trial.[17] If the moving party bears the burden of persuasion at trial, that party must present "credible evidence" showing that he is entitled to a directed verdict.[18] The burden of production then shifts to the non-moving party to produce evidence raising a genuine issue of material fact.[19] On the other hand, if the moving party does not bear the burden of persuasion at trial, he can prevail on a motion for summary judgment in two ways: by proffering "affirmative evidence negating an element of the non-moving party's claim," or by showing the non-moving party has insufficient evidence to establish an "essential element of the non-moving party's claim."[20] If met by the moving party, the burden of production then shifts to the non-moving party, who must then provide

[15] Fed. R. Civ. P. 56(a).

[16] *See* Fed. R. Civ. P. 56(c)(1); *Celotex Corp. v. Catrett*, 477 U.S. 317, 323 (1986).

[17] *See Celotex Corp.*, 477 U.S. at 331.

[18] *Id.*

[19] *See id.*

[20] *Id.*

specific facts showing a genuine issue of material fact for trial.[21] In both instances, the ultimate burden of persuasion remains on the moving party.[22] In reviewing the record, the court must construe the evidence and the inferences to be drawn from the underlying evidence in the light most favorable to the non-moving party.[23]

III. DISCUSSION

A. HTC's Motion for Summary Judgment of Non-Infringement and No Willful Infringement of the '336 Patent

1. Non-Infringement of the '336 Patent

The court first considers HTC's motion for summary judgment of "full" non-infringement of the '336 patent. HTC argues that summary judgment is warranted because when the independent claims of the '336 patent are properly construed, HTC's products do not perform the claimed invention. HTC specifically points to three terms that each appear in two claims: (1) "entire ring oscillator variable speed system clock" (claims 1 and 11), (2) "entire oscillator" (claims 6 and 13), and (3) "an entire variable speed system clock" (claims 10 and 16).

HTC argues as follows. The prosecution history of the '336 patent demonstrates the applicants' repeated and express disclaimer that the claimed timing element – the oscillator or variable speed clock – had any connection to or dependence on a reference signal from an external crystal or other fixed timing piece. To further distinguish the '336 patent, the applicants added the "entire" term to explicitly claim only a timing element that wholly and exclusively appeared with the CPU on the chip. HTC's processors, in contrast, rely on an external crystal timing piece (called

[21] *See id.* at 330; *T.W. Elec. Service, Inc. v. Pac. Elec. Contractors Ass'n*, 809 F.2d 630, 630 (9th Cir. 1987).

[22] *See id.*

[23] *See Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 248 (1986); *Matsushita Elec. Indus. Co. v. Zenith Radio Corp.*, 475 U.S. 574, 587 (1986).

a phase-locked loop or "PLL"). Unlike the invention, therefore, the timing elements of HTC's processors do not sit entirely on the chip and do not vary with PVT parameters.

TPL responds that HTC improperly seeks reconsideration of this court's previous claim construction. The court properly construed the "entire variable speed system clock" term and this construction should extend to the other three "entire" terms. HTC's additional limitations are not supported by the specification, which does not speak to whether the oscillator or variable speed system clock also could work with an external crystal. As for any disclaimer, the applicants never disclaimed all reliance or reference to an off-chip crystal. Instead, the disclaimer to avoid the Magar reference was to an off-chip oscillator that generated the on-chip clock. As to the Sheets reference, the applicants distinguished their clock reference by pointing out that it was not an on-chip oscillator but rather an off-chip clock, and that off-chip clock required a command input to change its frequency. The oscillator taught by the '336 patent, in contrast, is self-generating on the chip itself and does not require an outside command to change frequency. As to the variation argument, even by HTC's own admission, the on-chip HTC oscillators vary and the PLLs in fact serve to limit that variation. That the net result may be a minimal change in the frequency of the clock is not enough to take HTC's accused products beyond the claim language.

HTC replies that the on-chip oscillator does not "generate" the CPU clock unless it communicates with the PLL, making the PLL necessary to "generate" the clock – and thereby outside of the claim language (as construed in light of the disclaimers). HTC further replies that frequency control in fact is generation of the clock because the oscillator does not begin to run independently. The PLL controls the oscillator and sets the frequency, which generates the clock. As to the variation issue, HTC argues that a person of ordinary skill in the art would understand the de minimis variation experienced by its products as rendering the timing element essentially fixed.

The court agrees with HTC that the disputed limitations are properly understood to exclude any external clock used to generate a signal.[24] Nevertheless, there remains a factual dispute whether HTC's products contain an on-chip ring oscillator that is self-generating and does not rely on an input control to determine its frequency. While HTC's expert says that the PLLs generate the clock, TPL's expert counters that the ring oscillators generate the clock and the PLLs merely buffer or fix the frequency.[25] This is a classic factual question that requires a trial to answer.

2. Willful Infringement of the '336 Patent

To "establish willful infringement, a patentee must show by clear and convincing evidence that the infringer acted despite an objectively high likelihood that its actions constituted infringement of a valid patent."[26] A patentee therefore must establish two elements. First, the patentee must show the accused infringer acted with "objective recklessness." Objective recklessness remains a question of law "predicated on underlying mixed questions of law and fact."[27] The objective recklessness prong "entails an objective assessment of potential defenses based on the risk presented" by the patent which "may include questions of infringement but also can be expected in almost every case to entail questions of validity that are not necessarily

[24] The patentee's arguments traversing the prior art narrowed the claims. *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722, 740 (2002) ("A patentee's decision to narrow his claims through amendment may be presumed to be a general disclaimer of the territory between the original claim and the amended claim."); *cf. Saeilo Inc. v. Colt's Mfg. Co.*, 26 F. App'x 966, 973 (Fed. Cir. 2002) ("Where an amendment narrows the scope of a claim for a reason related to the statutory requirements for patentability, prosecution history estoppel acts as a complete bar to the application of the doctrine of equivalents to the amended claim element.").

[25] *Compare* Docket No. 457 at 16 ("the oscillators in the accused products indisputably rely on an external crystal or clock generator to clock" the CPU), *with* Docket No. 470 at 14 ("Each HTC product includes a CPU/system clock – a ***ring oscillator*** within a PLL – that ***generates*** a clock signal ***on its own***, as long as it has a power supply.") (emphasis in original).

[26] *In re Seagate Tech., LLC*, 497 F.3d 1360, 1371 (Fed. Cir. 2007) (*en banc*).

[27] *See Bard Peripheral Vascular, Inc. v. W.L. Gore & Assocs., Inc.*, 682 F.3d 1003, 1006-07 (Fed. Cir. 2012) (holding that the objective determination of recklessness, even though predicated on underlying mixed questions of law and fact, is decided by the judge as a question of law subject to de novo review).

dependent on the factual circumstances of the particular party accused of infringement."[28] Second, if the requisite threshold objective recklessness is established, then the patentee must show that the "objectively-defined risk" of infringement determined by the record developed in the infringement proceeding "was either known or so obvious that it should have been known to the accused infringer."[29]

HTC argues that TPL has not presented sufficient evidence to make a prima facie case of willful infringement, in view of its "clear, legitimate, and objectively reasonable defenses" to HTC's claims of infringement.[30] In particular, its proposed constructions have been adopted by other tribunals and the ITC in particular. HTC's non-infringement position at the ITC was "sufficiently compelling and reasonable" that both the ITC staff attorney and Judge Gildea himself agreed with HTC's position.[31]

TPL takes issue with HTC's reference in this case to the ITC litigation. Different theories of infringement and different products are implicated by the two cases. Different claim constructions have issued in the cases. The staff attorney's position and Judge Gildea's conclusions are therefore irrelevant. Separately, TPL's successful licensing of the MMP patent portfolio suggests that HTC could not reasonably or realistically expect its invalidity or

[28] *Id.* at 1006.

[29] *Seagate*, 497 F.3d at 1371.

[30] Looking to Fed. R. Civ. P. 37(c)(1) HTC further points out that TPL failed to substantively respond to its interrogatory about willful infringement. *See* Fed. R. Civ. P. 37(c)(1) ("If a party fails to provide information or identify a witness as required by Rule 26(a) or (e), the party is not allowed to use that information or witness to supply evidence on a motion, at a hearing, or at a trial, unless the failure was substantially justified or is harmless."). But TPL's response raising a host of objections appears substantially justified, even if it is not ultimately persuasive, and in any event HTC does not appear to have taken any steps whatsoever in the intervening four years to compel a more complete response.

[31] Judge Gildea's Initial Determination ("ID") did not issue until September 6, 2013, after the papers for this motion were filed.

non-infringement defenses to succeed in this litigation. Finally, direct pre-suit communication between HTC and TPL establishes that HTC had notice of its allegedly infringing activities.

District courts appear split as to whether current evidence that a party's actions were objectively reasonable is relevant to a willfulness analysis under *Seagate*. In *i4i Ltd. P'ship v. Microsoft Corp.*, Judge Davis held that the correct willfulness analysis "focuses on whether, given the facts and circumstances prior to [the accused infringer's] infringing actions, a reasonable person would have appreciated a high likelihood that acting would infringe a valid patent."[32] The "number of creative defenses that Microsoft is able to muster in an infringement action after years of litigation and substantial discovery is irrelevant to the objective prong of the *Seagate* analysis."[33] Judge Davis then explained that the court should more properly focus on whether defenses would have been objectively reasonable and apparent before Microsoft infringed and was sued.[34] In *Uniloc USA, Inc. v. Microsoft Corp.*, Judge Smith was "not convinced that such a 'before and after' line is so easily drawn, or for that matter appropriate, to measure the objective likelihood (or lack thereof) that a party acted to infringe a valid patent."[35] Judge Smith emphasized that "the inquiry is case-specific" and should focus on an objective view of the record.[36]

The court agrees with HTC that favorable court rulings can support the objective reasonableness of its non-infringement positions. The court cannot help but take note of the analogous issue of the "book of wisdom" when addressing patent damages. The Supreme Court has affirmed that after-arising "[e]xperience . . . is a book of wisdom that courts may not

---

[32] 670 F. Supp. 2d 568, 582 (E.D. Tex. 2009).

[33] *Id.*

[34] *See id.*

[35] 640 F. Supp. 2d 150, 177 n. 33 (D.R.I. 2009).

[36] *Id.*

neglect."[37] Nonetheless, "as the party moving for summary judgment" HTC "must do more than persuade [the court] that its defenses were reasonable."[38] Instead, HTC "must establish that 'there is no genuine dispute as to any material fact' and that [the accused infringer] 'is entitled to judgment as a matter of law'—in other words, that *no reasonable fact-finder* could find willful infringement."[39]

Viewing the evidence in the light most favorable to TPL, the court concludes that a reasonable fact finder could plausibly find facts sufficient to support a conclusion of willful infringement. TPL's burden to show willful infringement by clear and convincing evidence is a steep one. But where factfinding is necessary, trial courts generally reserve willfulness until after a full presentation of the evidence on the record to the jury.[40] The record supports a finding that HTC knew about the patents and TPL's claims of infringement before it began the activities that allegedly infringe and as explained above, here there remains an important issue regarding the role of the external crystal in HTC's products in generating a signal.[41] Under these circumstances summary judgment on the issue of willfulness is not warranted.

B. Partial Summary Judgment of Non-Infringement of the '336 Patent and the '890 Patent and No Willful Infringement of the '890 Patent

HTC next moves for partial summary judgment of non-infringement of the '336 patent and the '890 patent based on the doctrine of absolute intervening rights. By this same motion, HTC also seeks summary judgment of no willful infringement under the '890 patent.

---

[37] *Sinclair Ref. Co. v. Jenkins Petroleum Process Co.*, 289 U.S. 689, 690 (1933).

[38] *Kimberly-Clark Worldwide, Inc. v. First Quality Baby Products, LLC*, Case No. 1:09-cv-1685, 2013 WL 1465403, at *2 (M.D. Pa. Apr. 11, 2013)

[39] *Id.* (citing Fed. R. Civ. P. 56(a)).

[40] *See, e.g. Bard*, 682 F.3d at 1008; *Fujitsu Ltd. v. Belkin Int'l, Inc.*, Case No. 10-cv-03972-LHK, 2012 WL 4497966, at *39 (N.D. Cal. Sept. 28, 2012).

[41] *See* Docket No. 470-1, Ex. A (Nov. 7, 2006 correspondence from Alliacense to HTC); Docket No. 470-1, Ex. B (Nov. 20, 2006 correspondence from Alliacense to HTC).

Under 35 U.S.C § 307(b), a patent owner may not recover for infringement of claims that are invalidated or amended through the reexamination process.[42] The "reexamination statute restricts a patentee's ability to enforce the patent's original claims to those claims that survive reexamination in 'identical' form."[43] "'Identical' does not mean verbatim, but means at most without substantive change."[44] The court must therefore determine whether the scope of the claims are the same, not just whether the same words are used.[45] Section 307 shields "those who deem an adversely held patent to be invalid; if the patentee later cures the infirmity by reissue or reexamination, the making of substantive changes in the claims is treated as an irrebuttable presumption that the original claims were materially flawed."[46] The "statute relieves those who may have infringed the original claims from liability during the period before the claims are validated."[47]

Whether "amendments made to overcome rejections based on prior art are substantive depends on the nature and scope of the amendments, with due consideration to the facts in any given case that justice will be done."[48] "An amendment that clarifies the text of the claim or makes it more definite without affecting its scope is generally viewed as identical."[49] To make its determination under the so-called doctrine of intervening rights, the court must consider "the scope of the original and reexamined claims in light of the specification, with attention to the references

---

[42] *See Fresenius USA, Inc. v. Baxter Intern., Inc.*, 721 F.3d 1330, 1339 (Fed. Cir. 2013).

[43] *Id.* (listing cases).

[44] *Id.*

[45] *See id.*

[46] *Bloom Eng'g Co. v. N. Am. Mfg. Co.*, 129 F.3d 1247, 1249 (Fed. Cir. 1997).

[47] *Id.*

[48] *Id.*

[49] *Id.*

that occasioned the reexamination, as well as the prosecution history and any other relevant information."[50]

1. Non-Infringement of the '336 Patent

As noted earlier the '336 patent issued September 15, 1998, and included ten originally-issued claims.[51] A series of ex parte reexamination requests were filed against the '336 patent between October 2006 and January 2007.[52] When the reexamination proceedings completed, claims 1, 6, and 10 emerged with modified language, and new independent claims 11, 13, and 16 were added. TPL amended claim 1 to further describe the "second clock independent of said ring oscillator" to say that "wherein a clock signal of said clock originates from a source other than said ring oscillator variable speed system clock." Claim 6 was amended to describe the "off-chip external clock" to likewise derive its "clock signal" "from a source other than said oscillator." Claim 10 includes a similar amendment that adds that the "off-chip external clock" has a "clock signal" that "originates form a source other than said variable speed clock." Claims 6 and 10 also added "off-chip" references to the descriptions of the second clocks. Claims 11, 13, and 16 were based on independent claims 1, 6, and 10, but during reexamination TPL added an additional clause to the end of each claim: "wherein said central processing unit operates asynchronously to said input/output interface."

In HTC's view, it should not be held liable for infringement of the '336 patent claims 1, 6, 10, 11, 13, and 16 because those claims were either substantially narrowed or newly-added through reexamination. Any recovery for the '336 patent should be limited to the date of the issuance of the reexamination certificate on December 15, 2009, because the amendments were sufficiently substantive to preclude recovery from before the amendments.

---

[50] *Id.*

[51] *See* Docket No. 458 at 5.

[52] *Id.*

TPL responds that these amendments serve as nothing more than clarification of the claim language and that the scope of the claims have not changed. Several excerpts from the prosecution history of the reexamination demonstrate that the patentee believed the amended claim language only clarified how the second clock was "independent"[53] and that the "external" components were in fact "off-chip"[54].

HTC replies that the original claims differ from the amended claims in scope because the original claims spoke only to the difference in frequency control – and that is what "independence" really references in these claim terms. Because a clock with signal origins from the ring oscillator but with an independent frequency could exist under the original claims but not under the amended claims, the claim is narrower and therefore substantively different. For claims 11, 13, and 16, the "independent" clock signals could have a "readily predictable phase relationship." Because of that possibility, the claims are narrower and thereby substantively different. Further, the court should not credit self-serving testimony from the prosecution history.[55]

On balance, the court finds that the amended claim language added during reexamination did not substantively amend the asserted '336 claims' scope. "Independent" in the disputed claims must be understood to be just that: without dependence of any kind. While HTC offers a more nuanced interpretation that focuses exclusively on frequency control, it cites no intrinsic – or for that matter extrinsic evidence – to support its position. Coupled with the references in the prosecution history indicating that the amendments really were for clarification purposes only, TPL's argument is more persuasive.

---

[53] *See* Docket No. 471-5, Ex. E at 2; Docket No. 471-6, Ex. F at 11, 27; Docket No. 471-7, Ex. G at 8-12, 14.

[54] *See* Docket No. 471-7, Ex. G at 12, 16.

[55] *See Moleculon Research Crop. v. CBS, Inc.*, 793 F.2d 1261, 1270 (Fed. Cir. 1986) (holding that documents submitted by the patentee during prosecution may be considered for claim interpretation purposes, but "might very well contain merely self-serving statements which likely would be accorded no more weight than testimony of an interested witness or argument of counsel. Issues of evidentiary weight are resolved on the circumstances of each case.").

2. Motion for Partial Summary Judgment of Non-Infringement and No Willful Infringement of the '890 Patent

a. Non-Infringement of the '890 Patent

The court next considers HTC's motion for summary judgment of non-infringement of the '890 patent claims 11, 12, 13, 17, and 19. As noted above, claims 12, 13, 17, and 19 all depend on independent claim 11.

HTC again argues the doctrine of absolute intervening rights entitles it to summary judgment of non-infringement. During reexamination, TPL added claim language further defining a stack pointer as "pointing into said first push down stack," after the examiner identified no function for the stack pointer in the original claim language. The examiner noted that the amendment to claim 1 prevented the claim from being anticipated by the prior art under 35 U.S.C. § 102. This change to the '890 patent during reexamination was substantive and that the absolute intervening rights doctrine bars liability arising before the reexamination terminated.

TPL initially responds that HTC's assertion of the absolute intervening rights doctrine is untimely because it did not include the affirmative defense in its answer to TPL's complaint.[56] As to the merits, TPL says that the amendment only clarified the claim scope but did not substantively amend the claim, precluding the absolute intervening rights doctrine. Further, in *Norwood v. Vance* the Ninth Circuit noted that parties may raise affirmative defenses for the first time at summary judgment only if the opposing party is not prejudiced.[57] Allowing HTC to assert the defense – four years into this litigation – would subject it to unfair prejudice.

The court is not persuaded that TPL has established the prejudice necessary to bar HTC's assertion of the absolute intervening rights doctrine at this stage in the litigation. TPL does not, for

[56] The initial declaratory judgment complaint in this case was filed February 8, 2008. *See supra* note 1. The '890 patent did not reissue following reexamination until March 1, 2011. *See supra* note 13.

[57] 591 F.3d 1062, 1075 (9th Cir. 2010).

example, articulate the discovery it might have otherwise taken had HTC promptly moved to amend its answer in 2011.

Turning to the merits, HTC asserts estoppel and argues claim 11 emerged from reexamination substantively different from former claim 1. During reexamination, the examiner found claim 1 invalid. In an August 12, 2010, advisory action the examiner noted that claim 1 failed to provide a function for the "stack pointer" and the claim language only identified the stack pointer as "bidirectionally connected to an internal bus," – an error claim 11 corrected. The examiner also observed that the additional language in claim 11 avoided the May reference, U.S. Patent No. 4,758,948 ("the '948 patent"), that teaches using a push down stack but not expressly a stack pointer performing the function that the amended language defines. Therefore, that the absolute intervening rights doctrine bars infringement liability prior to the issuance of the reexamination certificate.

TPL sees it differently. The change to claim 11 only makes the claim more definite. The examiner's primary concern with claim 1 centered on the discussion in the May patent of an instruction pointer. The instruction pointer identifies the instructions of a process and under the broadest interpretation the stack pointer likewise could be construed to read onto the prior art. No person of ordinary skill in the art would understand a stack pointer could not perform equivalently to an instruction pointer. As described in claim 1, the stack pointer would be understood by a person of ordinary skill in the art to point to only to the first push down stack referenced in claim 1 – and so the additional language only explicitly states what a person of ordinary skill in the art already would understand claim 1 to teach.

HTC replies that TPL's arguments rely on extrinsic evidence and that the intrinsic evidence reveals that absent the added limitation, the stack pointer was impermissibly vague and the amendment substantively narrowed the claim.

The court agrees with HTC. As the examiner's office actions indicated, in the original claim language the stack pointer did nothing except connect to the internal data bus, but TPL's argument that a person of ordinary skill in the art necessarily would color in the ambiguity with an understanding that the stack pointer points only to the first push down stack is not persuasive. As HTC points out, claim 1 (and claim 11) employs the term "comprising," which reveals that the claim is "inclusive or open-ended and does not exclude additional, unrecited elements or method steps."[58] Given that the specification in fact references a second push down stack, the second stack must be presumed to be distinct from the return stack identified in the claim language, other push down stacks potentially could be used and still fall within claim 1. Thus, where the stack pointer points matters. If multiple push down stacks were included in a processor, it is unclear under the language of claim 1 whether the stack pointer points to one of the stacks, all of the stacks, or some multiple in between.

At bottom, the court finds the added language limits the stack pointer to the first push down stack and substantively changes the scope of the claim. Because the added claim language narrows the scope of the claims, any claims of infringement before the date of the issuance of the reexamination certificate must be precluded.

b. Willful Infringement of the '890 Patent

The court finally addresses the issue of willful infringement related to the '890 patent.

HTC asserts that under the objective recklessness prong, the reexamination and amendment of the '890 patent supports HTC's position that it was not objectively reckless. HTC points out that TPL has offered no evidence that it even knew of the '890 patent before the suit. HTC also argues that the failure by TPL to pursue a preliminary injunction suggests that willful infringement is not at issue.

[58] *CollegeNet, Inc. v. ApplyYourself, Inc.*, 418 F.3d 1225, 1235 (Fed. Cir. 2005).

TPL responds that it provided notice to HTC of the patents and of its infringing behavior in 2006. The reexamination process actually cuts against HTC because most of the substance of the patents in fact survived intact with a "second stamp of validity from the PTO."[59] The PTO accepts 92% of reexamination applications, so the PTO's grant of patent reexamination is not enough to undercut willful infringement.[60] A "substantial question of patentability raised by a reexamination request is not dispositive" in a willfulness inquiry.[61]

Although the record at least suggests that HTC was made aware of the patents-in-suit as early as November 2006,[62] as discussed above the reexamined '890 patent bars claims of infringement before the date of the issuance of the certificate because the additional language added to independent claim 11 narrowed the scope of the claim.[63] It follows that because HTC cannot be held liable for infringement before March 1, 2011, willful infringement for this period is precluded.

The court next turns to whether HTC can be found to have willfully infringed the '890 patent following reexamination. Generally, a "patentee who does not attempt to stop an accused infringer's activities [by moving for a preliminary injunction] should not be allowed to accrue

[59] Docket No. 469 at 17.

[60] *See id.* n.11.

[61] *Plumley v. Mockett*, 836 F. Supp. 2d 1053, 1075 (C.D. Cal. 2010); *see also See Lucent Techs., Inc. v. Gateway, Inc.*, Case No. 07–cv–2000–H, 2007 WL 6955272, at *7 (S.D. Cal. Oct. 30, 2007) ("The Court does not assume that a reexamination order will always prevent a plaintiff from meeting their burden on summary judgment regarding willful infringement, but it does consider this as one factor among the totality of the circumstances.").

[62] *See* Docket No. 469-12, Ex. C (correspondence from Alliacense notifying HTC that HTC was infringing the patents contained in the MMP Portfolio, including the '890 patent).

[63] Moreover, at least one district court has noted, albeit in dicta, that "a patentee's willful infringement claim fails as a matter of law where the PTO requires amendments to the patent before issuing a reexamination certificate." *Plumley*, 836 F. Supp. 2d at 1075 (explaining court's opinion in *TGIP, Inc. v. AT & T Corp.*, 527 F. Supp. 2d 561 (E.D. Tex. 2007)).

enhanced damages based solely on the infringer's post-filing conduct."[64] But as TPL happily highlights, HTC conceded in prior litigation "that *Seagate* did not create a *per se* bar to claims for post-filing willful infringement where an injunction was not sought."[65] "Because *Seagate* did not create a *per se* bar, the determination of whether a patentee may pursue a claim for willful infringement based on post-filing conduct without seeking a preliminary injunction 'will depend on the facts of each case.'"[66] Patentees who neither practice the invention nor directly compete with the accused infringer are "excused from *Seagate's* rule that a patentee must seek an injunction to sustain a claim for post-filing willful infringement."[67] There may be circumstances "where an infringer's post-filing conduct was found to be willful" where "some material change that could create an objectively high likelihood of infringing a valid patent, such as a patent surviving a reexamination proceeding without narrowed claims."[68]

Viewing the evidence in the light most favorable to TPL and drawing all reasonable inferences in its favor, especially TPL's successful licensing program related to the patents-in-suit, the court concludes that a reasonable fact finder could plausibly find facts supporting a conclusion of willful infringement following the reexamination of the '890 patent.

---

[64] *Seagate*, 497 F.3d at 1372; *see also Anascape, Ltd. v. Microsoft Corp.*, Case No. 9:06-cv-158, 2008 WL 7182476 (E.D. Tex. Apr. 25, 2008) (patentee who did not move for preliminary injunction was not entitled to benefit from its lack of diligence by obtaining enhanced damages for willfulness during the post-filing period).

[65] *DataQuill Ltd. v. High Tech Computer Corp.*, 887 F. Supp. 2d 999, 1015 (S.D. Cal. 2011).

[66] *Id.* (citing *Seagate* 497 F.3d at 1374).

[67] *Id.*

[68] *LML Holdings, Inc. v. Pac. Coast Distrib. Inc.*, Case No. 11-cv-06173-YGR, 2012 WL 1965878 (N.D. Cal. May 30, 2012) (citing *St. Clair Intellectual Prop. Consultants, Inc. v. Palm, Inc.*, Case No. 04–1436–JJF–LPS, 2009 WL 1649751, at *1 (D. Del. Jun.10, 2009)); *see also Webmap Technologies, LLC v. Google, Inc.*, Case No. 2:09–cv–343–DF–CE, 2010 WL 3768097, at *2-3 (E.D. Tex. Sep. 10, 2010).

IT IS SO ORDERED.

Dated: September 17, 2013

PAUL S. GREWAL
United States Magistrate Judge

IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

Acer, Inc.,

Plaintiff,

v.

Technology Properties Ltd, et al.,

Defendants.
_____/

HTC Corp.,

Plaintiff,

v.

Technology Properties Ltd, et al.,

Defendants.
_____/

Barco NV,

Plaintiff,

v.

Technology Properties Ltd, et al.,

Defendants.
_____/

NO. C 08-00877 JW
NO. C 08-00882 JW
NO. C 08-05398 JW

FIRST CLAIM CONSTRUCTION ORDER

I. INTRODUCTION

Technology Properties Limited, Patriot Scientific Corporation and Alliacense, Ltd. (collectively, "Defendants") own a group of five patents known as the Moore Microprocessor

Portfolio patents.[1] Plaintiffs Acer, Inc.,[2] HTC Corp.[3] and Barco, N.V.[4] each filed lawsuits seeking a judicial declaration that the Patents-in-Suit are either invalid or are not infringed. Defendants filed counterclaims for infringement of the Patents-in-Suit. In due course, the actions were related and consolidated.[5]

On January 27, 2012, the Court conducted a hearing in accordance with Markman v. Westview Instruments, Inc.,[6] to construe language of the asserted claims over which there is a dispute. At the hearing, in addition to the normal intrinsic evidence, the parties relied upon a prior

---

[1] The five Patents-in-Suit are U.S. Patent Nos. 5,809,336 ("the '336 Patent"), 5,784,584 ("the '584 Patent"), 5,440,749 ("the '749 Patent"), 6,598,148 ("the '148 Patent") and 5,530,890 ("the '890 Patent").

[2] The first of these now-consolidated actions was filed on February 8, 2008. Acer filed suit against Defendants seeking a judicial declaration that the '336 Patent, the '584 Patent and the '749 Patent are invalid or are not infringed by Acer. (See Docket Item No. 1 in No. C 08-00877 JW.) On November 21, 2008, Defendants counterclaimed for infringement of the '336 Patent and the '749 Patent. (See Docket Item No. 60 in No. C 08-00877 JW.) On February 9, 2009, Acer amended its complaint to add claims pertaining to the '148 Patent and the '890 Patent. (See Docket Item No. 98 in No. C 08-00877 JW.) On February 24, 2009, Defendants counterclaimed with respect to those two patents. (See Docket Item No. 99 in No. C 08-00877 JW.)

[3] On February 8, 2008, HTC also filed suit seeking a judicial declaration that the '336 Patent, the '584 Patent, the '749 Patent and the '148 Patent are invalid or are not infringed by HTC. (See Docket Item No. 1 in No. C 08-00882 JW.) On July 10, 2008, HTC amended its complaint to add claims pertaining to the '890 Patent. (See Docket Item No. 34 in No. C 08-00882 JW.) On November 21, 2008, Defendants counterclaimed with respect to each of those patents except for the '584 Patent. (See Docket Item No. 60 in No. C 08-00882 JW.)

[4] On December 1, 2008, Barco filed suit seeking a judicial declaration that the '584 Patent, the '749 Patent and the '890 Patent are invalid or are not infringed by Barco. (See Docket Item No. 1 in No. C 08-05398 JW.) On February 17, 2009, Defendants counterclaimed for infringement with respect to the '749 Patent, the '890 Patent and the '336 Patent. (See Docket Item No. 27 in No. C 08-05398 JW.)

[5] Judge Fogel ordered the cases related. (See Docket Item No. 21 in No. C 08-00882 JW; Docket Item No. 21 in No. C 08-05398 JW.) On September 1, 2011, this matter was reassigned from Judge Fogel to Chief Judge Ware. (See Docket Item No. 291 in No. C 08-00877 JW.)

[6] 517 U.S. 370 (1996).

claim construction order by Judge T. John Ward[7] and documentary material from reexamination proceedings.[8]

This Claim Construction Order sets forth the Court's construction of disputed words and phrases tendered to the Court for construction.

II. STANDARDS AND PROCEDURES FOR CLAIM CONSTRUCTION

A. General Principles of Claim Construction

Claim construction is a matter of law, to be decided exclusively by the Court. Markman, 517 U.S. at 387. In accordance with the Patent Local Rules of the Northern District, the parties submit their joint selection of the ten disputed terms that are significant in resolving the case as well as their proposed definitions for construction. See Patent L.R. 4-3. After the Markman hearing and upon consideration of the parties' briefs, the Court issues an order construing the meaning of the disputed terms. The Court's construction becomes the legally operative meaning of the disputed terms that governs further proceedings in the case. See Chimie v. PPG Indus., Inc., 402 F.3d 1371, 1377 (Fed.

---

[7] In 2006, Defendants filed a patent infringement suit based upon three of the Patents-in-Suit in this matter–the '336 Patent, the '148 Patent and the '584 Patent–in the Eastern District of Texas. (See Order Denying Motions to Dismiss, to Transfer Venue, and to Stay at 3, Docket Item No. 47 in No. C 08-00877 JW (discussing the Texas action).) Defendants brought that action against unrelated third parties. (See id.) On June 15, 2007, Judge Ward issued a Claim Construction Order in the Texas action in which he construed some of the words and phrases from the three patents at issue in that case. See Tech. Props. Ltd. v. Matsushita Elec. Indus. Co., Ltd., 514 F. Supp. 2d 916 (E.D. Tex. 2007).

[8] As of April 30, 2009, "a total of eleven reexamination proceedings had been initiated against the [Patents-in-Suit] in the United States Patent and Trademark Office ('USPTO')." (Order Granting in part Motion to Stay at 2-3, Docket Item No. 144 in No. C 08-00877 JW.) On June 17, 2009, the Court granted in part motions to stay this action pending reexamination of several of the Patents-in-Suit. (See id.) On February 22, 2010, the Court lifted the stay. (See Docket Item No. 156 in No. C 08-00877 JW.)

The reexamination certificate for the '749 Patent was issued on June 7, 2011. (See Declaration of James C. Otteson in Support of Defendants' Opening Claim Construction Brief for the "Top Ten" Terms, hereafter, "Otteson Decl.," Ex. BB, Ex Parte Reexamination Certificate, Docket Item No. 310-6.) The reexamination of the '749 Patent resulted in amendments to Claim 1, among others. Claim 1 of the '749 Patent–which includes multiple disputed terms–was amended to include the two "wherein" clauses. (See id.)

The reexamination certificate for the '336 Patent was issued on December 15, 2009. (See Otteson Decl., Ex. DD, Ex Parte Reexamination Certificate, Docket Item No. 310-8.) The reexamination of the '336 Patent resulted in amendments to Claims 1, 6 and 10, and the addition of Claim 11, among others. (Id.)

Cir. 2005). Although greater weight should always be given to the intrinsic evidence,[9] claim construction is a fluid process in which the Court may consider a number of extrinsic sources of evidence, so long as they do not contradict the intrinsic evidence. See Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582-83 (Fed. Cir. 1996).

B. Construction from the Viewpoint of an Ordinarily Skilled Artisan

A patent's claims define the scope of the patent: the invention that the patentee may exclude others from practicing. Phillips, 415 F.3d at 1312. The Court generally gives the patent's claims their ordinary and customary meaning. In construing the ordinary and customary meaning of a patent claim, the Court does so from the viewpoint of a person of ordinary skill in the art at the time of the invention, which is considered to be the effective filing date of the patent application. Thus, the Court seeks to construe the patent claim in accordance with what a person of ordinary skill in the art would have understood the claim to have meant at the time the patent application was filed. This inquiry forms an objective baseline from which the Court begins its claim construction. Id. at 1313.

The Court proceeds from that baseline under the premise that a person of ordinary skill in the art would interpret claim language not only in the context of the particular claim in which the language appears, but also in the context of the entire patent specification of which it is a part. Phillips, 415 F.3d at 1313. Additionally, the Court considers that a person of ordinary skill in the art would consult the rest of the intrinsic record, including any surrounding claims, the drawings and the prosecution history, if it is in evidence. Id.; see also Teleflex, Inc. v. Fisosa N. Am. Corp., 299 F.3d 1313, 1324 (Fed. Cir. 2002). In reading the intrinsic evidence, a person of ordinary skill in the art would give consideration to whether the disputed term is a term commonly used in lay language, a technical term, or a term defined by the patentee.

C. Commonly Used Terms

In some cases, disputed claim language involves a commonly understood term that is readily apparent to the Court. In such a case, the Court considers that a person of ordinary skill in the art

---

[9] Phillips v. AWH Corp., 415 F.3d 1303, 1324 (Fed. Cir. 2005).

would give the term its widely accepted meaning, unless a specialized definition is stated in the patent specification or was stated by the patentee during prosecution of the patent. In articulating the widely accepted meaning of such a term, the Court may consult a general purpose dictionary. Phillips, 415 F.3d at 1314.

D. Technical Terms

If a disputed term is a technical term in the field of the invention, the Court considers that one of skill in the art would give the term its ordinary and customary meaning in that technical field, unless a specialized definition is stated in the specification or during prosecution of the patent. Phillips, 415 F.3d at 1314. In arriving at this definition, the Court may consult a technical art-specific dictionary or invite the parties to present testimony from experts in the field on the ordinary and customary definition of the technical term at the time of the invention. Id.

E. Defined Terms

It is well established that a patentee is free to act as his or her own lexicographer. See, e.g., Process Control Corp. v. HydReclaim Corp., 190 F.3d 1350, 1357 (Fed. Cir. 1999). Acting as such, the patentee may use a term differently than a person of ordinary skill in the art would understand it, without the benefit of the patentee's definition. Vitronics Corp., 90 F.3d at 1582. Thus, the Court examines the claims and the intrinsic evidence to determine if the patentee used a term with a specialized meaning.

The Court regards a specialized definition of a term stated in the specification as highly persuasive of the meaning of the term as it is used in a claim. Phillips, 415 F.3d at 1316-17. However, the definition must be stated in clear words which make it apparent to the Court that the term has been defined. See id.; Vitronics Corp., 90 F.3d at 1582. If the definition is not clearly stated or cannot be reasonably inferred, the Court may decline to construe the term pending further proceedings. Statements made by the patentee in the prosecution of the patent application as to the scope of the invention may be considered when deciding the meaning of the claims. Microsoft Corp. v. Multi-Tech Systems, Inc., 357 F.3d 1340, 1349 (Fed. Cir. 2004). Accordingly, the Court

may also examine the prosecution history of the patent when considering whether to construe the claim term as having a specialized definition.

In construing claims, it is for the Court to determine the terms that require construction and those that do not. See U.S. Surgical Corp. v. Ethicon, Inc., 103 F.3d 1554, 1568 (Fed. Cir. 1997). Moreover, the Court is not required to adopt a construction of a term, even if the parties have stipulated to it. Pfizer, Inc. v. Teva Pharm. USA, Inc., 429 F.3d 1364, 1376 (Fed. Cir. 2005). Instead, the Court may arrive at its own constructions of claim terms, which may differ from the constructions proposed by the parties.

III. DISCUSSION

Pursuant to the Patent Local Rules, the parties have tendered ten terms that they have identified as significant to resolving these cases. The parties have asked the Court to consider the tendered words and phrases in a particular order. However, because the sequence in which the patents were issued might influence how a person of ordinary skill in the art would understand the patents, the Court will discuss the words and phrases in the order in which they appear in the Patents-in-Suit.[10]

A. '749 Patent

The '749 Patent is entitled: "High Performance, Low Cost Microprocessor Architecture."

Claim 1 of the '749 Patent, as allowed after reexamination, provides:[11]

> A microprocessor system, comprising a central processing unit integrated circuit, a memory external of said central processing unit integrated circuit, a bus connecting said central processing unit integrated circuit to said memory, and means connected to said bus for fetching instructions for said central processing unit integrated circuit on said bus from said memory, said means for fetching instructions being configured and connected to fetch **multiple sequential instructions** from said memory in parallel and **supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle**, said bus having a width at least equal to a number of bits in each of the instructions times a number of the

[10] Subject to further proceedings, the Court's construction of any particular term is presumed to apply consistently across all claims in the Patents-in-Suit in which the term appears. See, e.g., Paragon Solutions, LLC v. Timex Corp., 566 F.3d 1075, 1087 (Fed. Cir. 2009).

[11] Unless otherwise indicated, all bold typeface is added by the Court for emphasis.

> instructions fetched in parallel, said central processing unit integrated circuit including an arithmetic logic unit and **a first push down stack connected to said arithmetic logic unit**, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input and means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input, a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack, said arithmetic logic unit having an output connected to said means for storing a top item;
> wherein
> the microprocessor system comprises an **instruction register** configured to store the multiple sequential instructions and from which instructions are accessed and decoded;
> and wherein
> the means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to the central processing unit integrated circuit during a single memory cycle comprises supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched.

Claim 1 recites a microprocessor system. The parties have tendered for construction a number of words and phrases used in Claim 1.

1. "multiple sequential instructions"

Claim 1 recites that the system comprises, among other components, a "means for fetching"[12] that is configured to fetch "multiple sequential instructions." The parties tender for construction the phrase "multiple sequential instructions."

Upon review, the Court finds that this phrase is composed of commonly used words that have a plain and ordinary meaning. There is nothing in the claim or written description that would lead a person of ordinary skill in the art to conclude that the inventors intended to use the phrase with anything other than its plain and ordinary meaning. In particular, the Court finds that the word "multiple" would have been understood, by a person of ordinary skill in the art, to mean "two or more," while the phrase "sequential instructions" would have been understood to mean "computer

[12] For convenience, the Court will refer to this "means" as the "means for fetching limitation."

instruction in a sequential order." Therefore, at this time, the Court declines to use any different words or phrases to construe the phrase "multiple sequential instructions."

2. ". . . configured and connected to . . . supply multiple sequential instructions to central processing unit integrated circuit during a single memory cycle"

Claim 1 recites that the "means for fetching" is configured and connected to supply multiple sequential instructions to the central processing unit "during a single memory cycle." The parties request the Court to decide what, if any, effect the reexamination proceedings had on the meaning of the phrase "during a single memory cycle."[13] Specifically, the issue tendered to the Court is whether the phrase should be defined as requiring a "prefetch buffer."

During reexamination, the inventors, in referring to the phrase "during a single memory cycle," defended allowance of the claim over a prior art reference known as "Edwards" by stating the following:

> Edwards describes the way the Transputer decodes and executes instructions. As described in Edwards, see, e.g., Fig. 8, below, instructions are supplied to a one-instruction-wide instruction buffer, one at a time, and are there decoded. Fetching multiple instructions into a prefetch buffer and then supplying them one at a time is not sufficient to meet the claim limitation–the supplying of "multiple sequential instructions to a CPU during a single memory cycle."[14]

Upon review, the Court does not find that the cited statements constitute a basis for construing the language of Claim 1 to include the presence or configuration of a prefetch buffer.[15]

---

[13] (See, e.g., Plaintiffs' Consolidated Responsive Claim Construction Brief at 26-28, hereafter, "Plaintiffs' Brief," Docket Item No. 315 in No. C 08-00877 JW.)

[14] (See Declaration of Kyle Chen in Support of Plaintiffs' Consolidated Responsive Claim Construction Brief, hereafter, "Chen Decl.," Ex. 16, Amendment in Response to Non Final Office Action in Ex Parte Reexamination Proceedings at 26, Docket Item No. 316-16.)

[15] Plaintiffs cite to three additional statements made by the inventors that purportedly contain similar disavowals. (See Plaintiffs' Brief at 27-28.) However, the Court finds that none of these cited statements refer to a "prefetch buffer." Further, each cited statement expressly distinguishes the alleged invention from the prior art reference on the same basis, namely, that the instructions are supplied to the CPU "during a single memory cycle." (Id.)

Having disposed of the only issue tendered with respect to this phrase, the Court declines to further construe it.[16]

3. "push down stack connected to said arithmetic logic unit"

Claim 1 recites a central processing unit integrated circuit including an arithmetic logic unit and "a first push down stack connected to said arithmetic logic unit." The parties tender for construction the phrase "push down stack connected to said arithmetic logic unit."

As to this phrase, the Court finds that a person of ordinary skill in the art reading the '749 Patent would understand the phrase "push down stack" to mean a last-in, first-out ("LIFO") data storage structure, in which the last item placed (pushed) onto the stack is the first item removed (popped) from the stack.[17] Further, the Court finds that a person of ordinary skill in the art at the time of the invention would understand that a "push down stack" can be implemented using a dedicated top-of-stack register or a logical stack "pointer" to indicate the "top of the stack" element regardless of its location. For example, the written description discusses stack pointers 102 and 104 in Fig. 2.[18]

Finally, with respect to this phrase, the parties dispute whether the "connected to" language should be construed as "directly connected to" or "physically connected to." The claim requires that the push down stack be "connected" to the arithmetic logic unit. The Court finds that a person of

---

[16] The parties did not request the Court to construe the meaning of the phrase "during a single memory cycle."

[17] See, e.g., MODERN DICTIONARY OF ELECTRONICS 603 (7th ed. 1999) (defining a "pushdown stack" as a "circuit that operates in the reverse of a shift register," and explaining that "[w]hereas[] a shift register is a first-in first-out (FIFO) circuit, pushdown stacks are last-in, first-out (LIFO) memories. When data is requested, the stack will read the last data stored, and all other data will move one step closer to the output. Unless memory is emptied, the first data in will never be retrieved."). The same source alternatively defines a "pushdown stack" as "[e]ssentially a last-in, first-out buffer" in which, "[a]s data is added, the stack moves down with the last item, added [sic] taking the top position. Id. Thus, the "[s]tack height varies with the number of stored items, increasing or decreasing with the entering or retrieving of data. The words push (move down) and pop (retrieve the most recently stoked [sic] item) are used to describe its operation." Id.

[18] Referring to Fig. 2, the specification states: "Stack pointer 102, return stack pointer 104, mode register 106 and instruction register 108 are also connected to the internal data bus 90 by lines 110, 112, 114 and 116, respectively." (See '749 Patent, Col. 6:39-42.)

ordinary skill in the art would understand that the stack might be implemented using "pointers," which negates the need to connect the stack directly or physically to the arithmetic logic unit.[19] Therefore, the Court declines to add as a limitation that the connection must be direct or physical.

Accordingly, the Court construes the phrase "push down stack connected to said arithmetic logic unit" to mean:

a last-in-first-out data storage element connected to the arithmetic logic unit.

4. "instruction register"

Claim 1 contains two "wherein" clauses. With respect to the first "wherein" clause, the parties tender for construction the phrase "wherein the microprocessor system comprises an instruction register."[20]

In computer systems, the phrase "instruction register" has a plain and ordinary meaning, namely, a "register in a central processing unit that holds the address of the next instruction to be executed."[21] A person of ordinary skill in the art reading the written description would understand that the inventors are using the phrase with its plain and ordinary meaning:

> Instruction register 108 receives four 8-bit byte instruction words 1-4 on 32-bit internal data bus 90.

('749 Patent, Col. 7:53-55.)[22]

The parties have drawn the Court's attention to a related term that was construed by Judge Ward and that was subsequently affirmed by the Federal Circuit. Judge Ward's construction related to phrases such as "instruction groups" and "operand" in Claim 29 of the '584 Patent. See Tech.

---

[19] See MODERN DICTIONARY OF ELECTRONICS 603 (7th ed. 1999) ("In actual practice, a hardware-implemented pushdown stack is a collection of registers with a counter that serves as a pointer to indicate the most recently loaded register. Registers are unloaded in the reverse of the sequence in which they were loaded.").

[20] The Court notes that both the body of the claim and the first "wherein" clause disclose a microprocessor system *comprising* recited limitations. However, conventional claim language would have the wherein clause formatted to provide that "the microprocessor system *further* comprises . . ." to avoid any confusion between the wherein clause and the body of the claim.

[21] See MICROSOFT COMPUTER DICTIONARY 276 (5th ed. 2002).

[22] The Court notes that the phrase "8-bit byte" is unusual and appears to be redundant.

Props. Ltd., 514 F. Supp. 2d at 931-34. The claims of the '584 Patent deal specifically with an embodiment that includes "variable width operands." (See '584 Patent, Col. 16:7-26.) This particular embodiment requires all operands to be right justified in the instruction register so that the microprocessor can quickly locate the operands of variable width without the need "to specify the different operand sizes." (See '584 Patent, Col. 16:24-26.) However, unlike Claim 29 of the '584 Patent, Claim 1 of the '749 Patent does not contain such phrases. Thus, the Court does not find Judge Ward's construction pertinent.

Because the Court finds that the language of the claim has been used with its plain and ordinary meaning, the Court declines to further construe it.[23]

B. '890 Patent

Claim 11 of the '890 Patent[24] provides:

> A microprocessor, which comprises a main central processing unit and a **separate direct memory access central processing unit** in a single integrated circuit comprising said microprocessor, said main central processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus, said internal data bus being bidirectionally connected to a loop counter, said loop counter being connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register, said stack pointer pointing into said first push down stack, said internal data bus being connected to a memory controller, to a Y register of a return push down stack, an X register and a program counter, said Y register, X register and program counter providing outputs to an internal address bus, said internal address bus providing inputs to said memory controller and to an incrementer, said

[23] The Court notes that in a summary of an in-person interview with the examiner issued on October 25, 1994, the examiner noted with respect to Claim 1: "operand width is variable and right adjusted." (See Chen Decl., Ex. 19, Examiner Interview Summary Record, Docket Item No. 316-20.) The statement appears to have been made in an attempt to distinguish prior art known as "Boufarah," and the Court finds that it may potentially impose a limitation on the type of operands that are to be used and the positioning of the operands in the instruction register. The Court finds that a full understanding of the meaning of this statement and the events that gave rise to it might be relevant to the present analysis. Thus, the Court finds that it would benefit from further briefing as to this issue, as discussed below.

[24] The '890 Patent and the '336 Patent were filed on the same day. However, the '890 Patent was issued earlier than the '336 Patent. (See Chen Decl. ¶¶ 2, 12 (stating that the '890 Patent was issued on June 25, 1996, while the '336 Patent was issued on September 15, 1998).)

> incrementer being connected to said internal data bus, said direct memory access central processing unit providing inputs to said memory controller, said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory.

The parties tender for construction the phrase "separate direct memory access central processing unit."

Claim 11 provides two separate central[25] processing units ("CPU"): a "main" CPU and a "direct memory access" ("DMA") CPU. The Court finds that a person of ordinary skill in the art would understand "CPU" to mean a unit of a computing system that fetches, decodes, and executes programmed instructions.[26] In the written description, the inventors use the term CPU consistently with its plain and ordinary meaning.[27]

Further, the written description criticizes "[c]onventional microprocessors" that use "DMA controllers" because "some processing by the main central processing unit (CPU) of the microprocessor is required."[28] With respect to the DMA CPU, the written description states that an object of the invention is to provide a microprocessor "in which DMA does not require use of the main CPU during DMA requests and responses and which provides very rapid DMA response with predictable response times."[29]

---

[25] The parties agree that a person of ordinary skill would understand "central" processing unit to refer to a processing unit, and that the word "central" does not necessarily connote the primary processor in a particular hierarchy.

[26] See, e.g., MODERN DICTIONARY OF ELECTRONICS 107 (7th ed. 1999) (defining a CPU as "[t]hat unit of a computing system that fetches, decodes, and executes programmed instructions and maintains the status of results as the program is executed").

[27] (See, e.g., '890 Patent, Col. 8:22-24 ("The DMA CPU 72 controls itself and has the ability to fetch and execute instructions. It operates as a co-processor to the main CPU 70 (FIG. 2) for time specific processing.").)

[28] ('890 Patent, Col. 1:52-58.)

[29] ('890 Patent, Col. 2:2-5.)

Accordingly, the Court construes the term "separate direct memory access central processing unit" to mean:

> **a central processing unit that accesses memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit.**

C. '336 Patent

1. Claim 1

Claim 1 of the '336 Patent provides:

> A microprocessor system, comprising
> a single integrated circuit including a central processing unit and an **entire ring oscillator variable speed system clock** in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,
> said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,
> a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;
> an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and
> a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.

The parties tender the phrase "ring oscillator" for construction.

Upon review, the Court finds that one of ordinary skill in the art would understand the phrase "ring oscillator" to mean: "interconnected electronic components comprising multiple odd numbers of inverters arranged in a loop."[30] When a voltage is applied, the ring oscillator generates signals that are used by the processing unit to regulate the timing of its operations. In contrast with a circuit

[30] The parties agree that a "ring oscillator" is "an oscillator having a multiple, odd number of inversions arranged in a loop," which is the construction arrived at by Judge Ward in the Texas action, though they disagree about whether additional limitations should be added to Judge Ward's construction of the term. (See Plaintiffs' Brief at 3; Defendants' Opening Claim Construction Brief for the "Top Ten" Terms at 16-17, Docket Item No. 310 in No. C 08-00877 JW.)

that receives its timing signal from an external clock, a person of ordinary skill in the art reading the patent would understand that Claim 1 claims a "single integrated circuit," fabricated so as to include a "ring oscillator."

At issue is whether the phrase "ring oscillator" should be given a specialized meaning based on statements made by the inventors during reexamination of Claims 4 and 8 of the '148 Patent.[31]

Claim 4 of the '148 Patent claims in pertinent part:

> A microprocessor integrated circuit comprising . . . a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said integrated circuit substrate.

Claim 8 of the '148 Patent has a similarly worded limitation.

During reexamination, the examiner reviewed the allowance of Claims 4 and 8 over U.S. Patent No. 4,689,581 ("Talbot"). The Talbot Patent, which is entitled "Integrated Circuit Phase Locked Loop Timing Apparatus," claims:

> an integrated circuit device . . . and a timing apparatus . . . formed on a common single chip, said timing apparatus comprising a phase locked loop [comprising, *inter alia*] a voltage controlled oscillator arranged to be controlled by [a] voltage signal to produce [an] output timing signal at its output.

(Talbot, Col. 10:48-11:9.)

Preliminarily, the examiner rejected Claims 4 and 8 of the '148 Patent as unpatentable over Talbot. During the course of reexamination proceedings, the examiner conducted an interview with the patent owner and discussed whether Claims 4 and 8 were allowable over Talbot.[32] Afterward,

---

[31] Because the '148 Patent shares the same specification with the '336 Patent and is directly related to the other three Patents-in-Suit, the Court finds that any representation regarding similar terms made by the inventors during the prosecution of the '148 Patent is relevant to its consideration and construction of the terms in the '336 Patent. See Microsoft Corp. v. Multi-Tech Sys., Inc., 357 F.3d 1340, 1350 (Fed. Cir. 2004) ("Any statement of the patentee in the prosecution of a related application as to the scope of the invention would be relevant to claim construction.").

[32] (See Otteson Decl., Ex. X, Ex Parte Reexamination Interview Summary, Docket Item No. 310-2.)

the examiner prepared and sent to the patent owner an "Interview Summary."[33] Specifically, with respect to the discussion of Talbot, the examiner wrote:

> Continuing, the patent owner further argued that the reference of Talbot does not teach of a "ring oscillator." The patent owner discussed features of a ring oscillator, such as being **non-controllable**, and being **variable based on the environment**. **The patent owner argued that these features distinguish over what Talbot teaches**. The examiner will reconsider the current rejection based on a forthcoming response, which will include arguments similar to what was discussed.[34]

In its post-interview submission, the patent owner reiterated the contention that the claim should be allowed because Talbot disclosed a "voltage-controlled oscillator" and not the "ring oscillator" disclosed in the claim:

> Further, Talbot does not teach, disclose, or suggest the ring oscillator recited in claim 4. The Examiner cited col. 3, ll. 26-36, and oscillator circuit 12 shown in FIG. 1 of Talbot as teaching the recited ring oscillator. Talbot discusses a voltage-controlled oscillator (VCO) 12, but does not teach or disclose a ring oscillator.[35]

During the course of these claim construction proceedings, the inventors have continued to maintain that Talbot was overcome during reexamination because it does not disclose a "ring oscillator."[36]

---

[33] An examiner's interview summary may serve as a basis for finding a prosecution disclaimer that narrows the claim scope. See, e.g., Rheox, Inc. v. Entact, Inc., 276 F.3d 1319, 1322 (Fed. Cir. 2002); Biovail Corp. Int'l v. Andrx Pharms., Inc., 239 F.3d 1297, 1302-04 (Fed. Cir. 2001).

[34] (See Chen Decl., Ex. 4, Ex Parte Reexamination Interview Summary, Docket Item No. 316-4 (emphasis added).)

[35] (Otteson Decl., Ex. Y, Remarks/Arguments at 11, hereafter, "Remarks," Docket Item No. 310-3.)

[36] For instance, Defendants argued during the Markman hearing that the inventors' written submission distinguished the Talbot reference because Talbot lacked a ring oscillator and never mentioned a requirement of "non-controllability." Further, Defendants also refer to the inventors' written response on February 21, 2008, which states:

> Further, **Talbot does not teach, disclose, or suggest the ring oscillator** recited in claim 4. ... Talbot discusses a voltage-controlled oscillator (VCO) 12, but **does not teach or disclose a ring oscillator**. Talbot provides two different implementations of the VCO 12 in FIGS. 3-4, **neither one of which is a ring oscillator**. Talbot refers to the oscillator of FIG. 3 as a "frequency controlled oscillator" (col. 7, ll. 21-22) and the oscillator of FIG. 4 simply as a "voltage controlled oscillator" (col. 8, ll. 59-65). As the sole inventor of the cited reference,

The Court has examined the Talbot patent. Although the component is, indeed, referred to as a "voltage-controlled oscillator," declarations and other extrinsic materials that have been tendered during the claim construction proceedings call into question the validity of the inventors' contention to the PTO and to this Court that the "ring oscillator" is different from the "voltage-controlled oscillator" disclosed in Talbot. On the one hand, the Court has received extrinsic evidence that the voltage-controlled oscillator disclosed in Talbot *is* a ring oscillator. On the other hand, arguments have been submitted claiming that the voltage-controlled oscillator of Talbot *is not* a ring oscillator.[37]

Under clear Federal Circuit law, a submission made by an inventor during reexamination is regarded as a disavowal only if the court finds that the allegedly disavowing statement is "so clear as to show reasonable clarity and deliberateness, and so unmistakable as to show unambiguous evidence of disclaimer." Omega Eng'g, Inc. v. Raytek Corp., 334 F.3d 1314, 1325 (Fed. Cir. 2003) (citations omitted).

Here, before arriving at a decision on the definition of the phrase "ring oscillator" in the context of the Talbot reference, the Court finds that it would benefit from further briefing. In the supplement briefs, the declarants shall fully articulate the technical basis for their opinions with respect to whether the voltage-controlled oscillator disclosed in Talbot is or is not a ring oscillator. The Court will return to the construction of the phrase "ring oscillator" following the completion of the supplement briefing.

> Talbot presumably possesses at least ordinary skill in the art, yet Talbot did not characterize either of the disclosed oscillators as ring oscillators. Applicants respectfully assert that the reason they were not characterized by Talbot as ring oscillators is because **they are not ring oscillators**. For at least the foregoing reasons, **Talbot does not teach, disclose, or suggest a ring oscillator** as recited in the claims. (Remarks at 11 (emphases added).)

[37] This issue is important to claim construction, because it is relevant to understanding in what manner the ring oscillator is "non-controllable," as distinguished from the voltage-controlled oscillator disclosed in Talbot. Resolving this conflict might affect how the Court approaches issues with respect to the validity of the patent claim at issue.

2. Claim 6

Claim 6 of the '336 Patent provides:

> A microprocessor system comprising:
> a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;
> an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator **clocking said central processing unit** at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way **as a function of parameter variation** in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and
> an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.

a. "clocking said central processing unit"

The parties tender for construction the phrase "clocking said central processing unit."

Upon review, the Court finds that to one of ordinary skill in the art, the plain and ordinary meaning of "clocking said central processing unit" is to provide a clock signal to the central processing unit.

A further issue tendered with respect to this phrase is whether, based on the written description, the construction should include a limitation of the maximum or optimum frequency of the "clocking" function. In the written description of the '336 Patent, the phrase "maximum frequency possible" is used with respect to an embodiment.[38] A description of an embodiment in the specification may not be imposed as a limitation "unless the patentee has demonstrated a clear

[38] (See '336 Patent, Col. 16:67-17:2 (stating that "[b]y deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast.").)

intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'" Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc., 381 F.3d 1111, 1117 (Fed. Cir. 2004) (citation omitted). Here, the Court finds that the cited language does not demonstrate "a clear intention to limit the claim scope." Id.

Accordingly, the Court construes "clocking said central processing unit" to mean:

providing a timing signal to said central processing unit.

b. "as a function of parameter variation"

The parties tender for construction the phrase "as a function of parameter variation." The full phrase is: "thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way **as a function of parameter variation."**

The disputed issue is whether the phrase requires a mathematical type predetermined functional relationship. Upon review, the Court finds that a person of ordinary skill in the art reading the patent would understand that the phrase "as a function of" is describing a variable that depends on and varies with another.[39] Because neither the written description nor the prosecution history provide a basis for concluding that the phrase should be limited to a narrower definition of an exact mathematical type functional relationship, the Court declines to do so. Having resolved the only dispute tendered with respect to this phrase, the Court declines to construe it further.

3. Claim 10

Claim 10 of the '336 Patent provides:

> In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:
>
> providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a

[39] The Court observes that "function" is a very broad term. See, e.g., MODERN DICTIONARY OF ELECTRONICS 311-12 (7th ed. 1999) (defining "function" as, *inter alia*, a "quantity of value that depends on the value of one or more other quantities" or a "specific purpose of an entity, or its characteristic action," and defining a number of phrases that include the term "function," such as "function codes," "function keys" and a "function table").

first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock and wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock.

The parties have tendered for construction the phrase "providing an entire variable speed clock disposed upon said integrated circuit substrate." There are two issues that are tendered with respect to this language. First, there is a dispute over whether the "variable speed clock" should be defined as limited to a ring oscillator. Here, the Court observes that, in other claims, the inventor discusses a "ring oscillator" as a variable speed system clock. Nonetheless, with respect to this Claim, the Court declines to limit the broader phrase found in Claim 10 to a ring oscillator only.

Second, the parties tender a dispute over the degree of independence between the signal of the "variable speed clock" and any external reference signal. However, upon review the Court finds that this dispute is not pertinent to the construction of the tendered phrase.

Accordingly, the Court construes "providing an entire variable speed clock disposed upon said integrated circuit substrate" to mean:

Providing a variable speed clock that is located entirely on the same semiconductor substrate as the central processing unit.

4. Claim 11

Claim 11 of the '336 Patent provides:

> A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, **wherein said central processing unit operates asynchronously to said input/output interface**.

The parties tender for construction the phrase "wherein said central processing unit operates asynchronously to said input/output interface."

Claim 11 discloses a microprocessor system comprising, among others, a central processing unit and an entire ring oscillator variable speed system clock connected to said central processing unit, an on-chip input/output interface, and "a second clock independent of said ring oscillator variable speed system clock" connected to said input/output interface. The subject phrase is contained in a "wherein" clause that describes the relationship between the timing control signal of the central processing unit and the timing signal of the on-chip input/output interface. The claim discloses that the central processing unit operates "asynchronously" to the input/output interface.

The written description is silent as to whether there is or can be *any* timing relationship between the central processing unit and the input/output interface or between their respective clocks.

The inventors first introduced the term "operates asynchronously to" during the re-examination of the '336 Patent in order to "clarify the meaning of 'independent' as recited in the

claims."[40] The examiner had focused on a reference known as "Kato" that purported to show two clock signals that are "in synchronism with each other." (Id. at 19.) The inventors explained that "Kato does not reveal any teaching that any of the components of the data processing circuit operate asynchronously with each other." (Id.) In support of the "independent" and "asynchronous" nature of its clocks, the inventors cited a textbook that describes what an asynchronous system is:

> An *asynchronous* system is one containing two or more independent clock signals. So long as each clock drives independent logic circuitry, such a system is effectively a collection of independent synchronous systems. **The logical combination of signals derived from independent clocks, however, poses difficulty because of the unpredictability of their phase relationship**.[41]

Reading this prosecution history, a person of ordinary skill would understand that the word "asynchronously"[42] means that the timing signal from one clock is independent from and not derived from the other clock such that a phase relationship between the two clocks is not readily predictable.

Accordingly, the Court construes "wherein said central processing unit operates asynchronously to said input/output interface" to mean:

> **the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them.**

IV. CONCLUSION

The Court has construed the phrases and terms tendered for construction.

On or before **June 29, 2012**, the parties shall meet and confer and file a Joint Statement addressing the following issues:

---

[40] (See Declaration of Eugene Mar in Support of Defendants' Opening Claim Construction Brief, Ex. G, In re Ex Parte Reexamination of U.S. Patent No. 5,809,336 at 17, Docket Item No. 213-2.)

[41] (Id. (citing STEPHEN A. WARD & ROBERT H. HALSTEAD, JR., COMPUTATION STRUCTURES 93 (1990)) (emphasis added).)

[42] One source provides nine different meanings for the term "asychronous." See MODERN DICTIONARY OF ELECTRONICS 40 (7th ed. 1999) (defining the term, *inter alia*, as a "communication method in which data is sent when it is ready without being referenced to a timing clock, rather than waiting until the receiver signals that it is ready to receive" or as referring to "computer program execution [that is] unexpected or unpredictable with respect to the instruction sequence").

(1) A proposed schedule for supplemental briefs consistent with the terms of this Order;

(2) In light of the Court's impending retirement,[43] the Court proposes to assign this case to Magistrate Judge Grewal. In their Statement, the parties shall state whether they jointly consent to having this case immediately reassigned to Judge Grewal. In the event the parties do not consent to the immediate reassignment, the case will remain with Judge Ware and be subject to reassignment in due course.

Dated: June 12, 2012

JAMES WARE
United States District Chief Judge

[43] On April 28, 2012, Chief Judge Ware announced that he plans to "retire in August 2012 as the terms of his current law clerks come to an end." See Chief Judge Ware Announces Transition, *available at* http://www.cand.uscourts.gov/news/82.

THIS IS TO CERTIFY THAT COPIES OF THIS ORDER HAVE BEEN DELIVERED TO:

Deepak Gupta dgupta@fbm.com
Eugene Y. Mar emar@fbm.com
Harold H. Davis harold.davis@klgates.com
James Carl Otteson jim@agilityiplaw.com
Jas S Dhillon jas.dhillon@klgates.com
Jeffrey M. Fisher jfisher@fbm.com
Jeffrey Michael Ratinoff jeffrey.ratinoff@klgates.com
John L. Cooper jcooper@fbm.com
Kyle Dakai Chen kyle.chen@cooley.com
Mark R. Weinstein mweinstein@cooley.com
Michelle Gail Breit mbreit@agilityiplaw.com
Nan E. Joesten njoesten@fbm.com
Paul A. Alsdorf palsdorf@fbm.com
Samuel Citron O'Rourke eupton@whitecase.com
Stephanie Powers Skaff sskaff@fbm.com
Timothy Paar Walker timothy.walker@klgates.com
William Sloan Coats william.coats@kayescholer.com

Dated: June 12, 2012

Richard W. Wieking, Clerk

By: /s/ JW Chambers
William Noble
Courtroom Deputy

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORPORATION, ALLIACENSE LTD., Defendants.	Case No. 5:08-cv-00877 PSG **(Re: Docket Nos. 356, 357, 358, 374)**
HTC CORPORATION, HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORPORATION, ALLIACENSE LTD., Defendants.	Case No. 5:08-cv-00882 PSG **(Re: Docket Nos. 385, 387, 388, 403)**

CLAIM CONSTRUCTION ORDER

In this patent infringement suit, Plaintiffs Acer, Inc., Acer America Corp., Gateway, Inc., and Plaintiffs HTC Corp. and HTC America, Inc. (collectively "Plaintiffs") seek a declaratory

judgment that they do not infringe patents owned by Defendants Technology Properties Ltd., Patriot Scientific Corp., and Alliacense Ltd. (collectively "Defendants").[1] Consistent with Pat. L.R. 4-3(c), the parties seek further construction of terms and phrases in claims in the patents-in-suit.[2] Plaintiffs and Defendants each also seek reconsideration of Judge Ware's earlier constructions of certain terms.[3]

As part of those motions for reconsideration, Plaintiffs seek to file a sur-reply on the grounds that Defendants' reply to their motion for reconsideration introduced new arguments and new evidence.[4] The court GRANTS Plaintiffs' motion to file the sur-reply.

In light of this case's long history and the trial date set for June 24, 2013, the court does not wish to add any further delay to the constructions by its preparation of a complete opinion setting forth its reasoning and analysis. To that end, the court at this time will simply issue its constructions without any significant reasoning and analysis:

CLAIM TERM	**CONSTRUCTION**
"instruction register"	Register that receives and holds one or more instructions for supplying to circuits that interpret the instructions
"ring oscillator"	an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment
"separate DMA CPU"	a central processing unit that accesses memory and that fetches and executes instructions directly and separately of the main central processing unit
"supply the multiple sequential instructions"	provide the multiple sequential instructions in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during

[1] Unless otherwise noted, the docket citations refer to Case No. 5:08-cv-00882 PSG.

[2] *See* Docket Nos. 387, 394.

[3] *See* Docket Nos. 385, 388.

[4] *See* Docket No. 403.

	a single memory cycle
"clocking said CPU"	Providing a timing signal to said central processing unit

The parties should rest assured that the court arrived at these constructions with a full appreciation of not only the relevant intrinsic and extrinsic evidence, but also the Federal Circuit's teaching in *Phillips v. AWH Corp.*,[5] and its progeny. So that the parties may pursue whatever recourse they believe is necessary, a complete opinion will issue before entry of any judgment.

IT IS SO ORDERED.

Dated: December 4, 2012

PAUL S. GREWAL
United States Magistrate Judge

[5] 415 F.3d 1303, 1312-15 (Fed. Cir. 2005).

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORPORATION, ALLIACENSE LTD., Defendants.	Case No. 5:08-cv-00877 PSG **(Re: Docket Nos. 356, 357, 358, 374)**
HTC CORPORATION, HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORPORATION, ALLIACENSE LTD., Defendants.	Case No. 5:08-cv-00882 PSG **(Re: Docket Nos. 385, 387, 388, 403)**

CLAIM CONSTRUCTION ORDER

On November 30, 2012, following reassignment of this case to the undersigned with the consent of the parties and in light of the retirement of Chief Judge Ware, and the completion of an

extended *Markman* hearing, the court issued an order from the bench construing five of the parties' disputed terms. The court provided a written summary of its constructions a few days later.[1] The court now explains its reasoning below.

I. BACKGROUND

In this suit, Plaintiffs Acer, Inc., Acer America Corp., Gateway, Inc., HTC Corp., and HTC America, Inc.[2] seek a declaratory judgment that they do not infringe patents owned by Defendants Technology Properties, Patriot Scientific, and Alliacense (collectively "TPL"). All of the patents at issue relate to various aspects of microprocessors.

On November 30, 2012, the court held a claim construction hearing to consider five disputed terms. Prior to the case being reassigned to the undersigned, Judge Ware considered the same five terms.[3] He construed three of them and asked for more briefing on two of them, although he also provided a tentative construction for the two.[4]

The Eastern District of Texas also has considered related terms in another case that TPL filed in 2006 against unrelated third parties. In that case, Judge Ward held a claim construction hearing and issued a decision construing terms based upon patents with the same specification as the patents at issue in this suit.[5] Several terms he construed overlap with terms at issue here. Although the case resolved before proceeding to trial, TPL appealed a portion of the claim construction ruling to the Federal Circuit with respect to one of the three patents in suit; the Federal Circuit affirmed the district court's judgment against TPL.[6]

---

[1] *See* Docket No. 381.

[2] Barco N.V. was originally a party and was a party to the motions at issue, but is no longer involved in the case.

[3] *See* Docket No. 336.

[4] *See id.*

[5] *See Tech. Properties Ltd. v. Matsushita Elec. Indus. Co., Ltd.*, 514 F. Supp. 2d 916, 927 (E.D. Tex. 2007) *aff'd sub nom.*, 276 F. App'x 1019 (Fed. Cir. 2008). At issue were United States Patent Nos. 5,809,336, 6,598,148, and 5,784,584.

[6] *See Tech. Properties Ltd., Inc. v. Arm, Ltd.*, 276 F. App'x 1019 (Fed. Cir. 2008).

The terms at issue are found in United States Patent No. 5,440,749 (the "'749 Patent") titled "High Performance, Low Cost Microprocessor Architecture,"[7] United States Patent No. 5,809,336 (the "'336 Patent") titled "High Performance Microprocessor Having Variable Speed System Clock,"[8] and United States Patent No. 5,530,890 (the "'890 Patent"), titled "High Performance, Low Cost Microprocessor."[9] All three patents derive from the same original patent application that was subject to a ten-way restriction requirement and eventually resulted in six different patents known as the Moore Microprocessor Portfolio patents, all of which share a common specification.

The '749 Patent claims an invention that accelerates the operation of microprocessors by fetching multiple instructions from memory per memory cycle. Because a CPU can execute instructions faster than it can fetch them from memory, fetching multiple instructions per memory cycle can improve overall performance.

The '336 Patent claims an invention that allows the frequency of a CPU to fluctuate based upon conditions. Traditional microprocessors use fixed frequency clocks to regulate the frequency with which the CPU operates. Fixed clocks generally have to be set lower than the CPU's maximum possible frequency to ensure proper operation under the worst-case conditions. The '336 Patent claims an invention that solves this problem by placing a ring oscillator on the same microchip as the CPU to act as the clock. Because the ring oscillator is on the same microchip and made out of the same components as the CPU, it is subject to the same environmental conditions and thus it will operate at a variable speed based upon conditions allowing the CPU to operate at higher rates during good conditions and lower rates during bad.

The '890 Patent relates to microprocessor architecture and claims a direct memory access mechanism. Most microprocessors have a direct memory access controller that handles the slow operation of reading and writing to memory so that the CPU can execute other instructions while waiting. The patent discloses a direct memory access CPU, which can execute some instructions in addition to reading and writing to memory for the CPU.

---

[7] *See* Docket No. 358-2.

[8] *See* Docket No. 358-6.

[9] *See* Docket No. 368-2.

II. LEGAL STANDARDS

Claim construction is exclusively within the province of the court.[10] "To construe a claim term, the trial court must determine the meaning of any disputed words from the perspective of one of ordinary skill in the pertinent art at the time of filing."[11] This requires a careful review of the intrinsic record, comprised of the claim terms, written description, and prosecution history of the patent.[12] While claim terms "are generally given their ordinary and customary meaning," the claims themselves and the context in which the terms appear "provide substantial guidance as to the meaning of particular claim terms."[13] Indeed, a patent's specification "is always highly relevant to the claim construction analysis."[14] Claims "must be read in view of the specification, of which they are part."[15]

Although the patent's prosecution history "lacks the clarity of the specification and thus is less useful for claim construction purposes," it "can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be."[16] The court also has the discretion to consider extrinsic evidence, including dictionaries, scientific treatises, and testimony from experts and inventors. Such evidence, however, is "less significant than the intrinsic record in determining the legally operative meaning of claim language."[17]

Judge Ware has already considered all of the terms currently before the court. Although the court granted leave for parties to file motions for reconsideration, it will take as its starting point that

---

[10] *See Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 387 (1996).

[11] *Chamberlain Group, Inc. v. Lear Corp.*, 516 F.3d 1331, 1335 (Fed. Cir. 2008).

[12] *See id.*; *Phillips v. AWH Corp*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (internal citations omitted).

[13] *Phillips*, 415 F.3d at 1312, 1314.

[14] *Id.* at 1312-15.

[15] *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996); *see also Ultimax Cement Mfg. Corp v. CTS Cement Mfg. Corp.*, 587 F. 3d 1339, 1347 (Fed. Cir. 2009).

[16] *Phillips*, 415 F.3d at 1317 (internal quotations omitted).

[17] *Id.* (internal quotations omitted).

the earlier constructions are correct. Consistent with Local Rule 7-9, absent newly discovered material facts, change in law, or manifest failure to consider material facts or arguments, the court will not alter any earlier constructions.[18]

III. CLAIM CONSTRUCTION

A. "instruction register"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
Register that receives and holds one or more instructions for supplying to circuits that interpret the instructions, in which any operands that are present must be right-justified in the register	Register that receives and holds one or more instructions for supplying to circuits that interpret the instructions

The parties dispute the construction of "instruction register" as used in claim 1 of the '749 Patent. The term "instruction register" was added to a wherein clause in claim 1 of the '749 patent during reexamination. The patent claims a microprocessor system

> wherein the microprocessor system comprises an instruction register configured to store the multiple sequential instructions and from which instructions are accessed and decoded.[19]

Judge Ware tentatively construed "instruction register" in the '749 patent as having its plain and ordinary meaning.[20] Quoting a dictionary, he determined that instruction register meant a "register in a central processing unit that holds the address of the next instruction to be executed."[21] After construing the term, the court noted that the prosecution history might convince the court to limit its construction and requested more briefing.[22]

The parties agree that the term has a slightly different meaning than the one the court previously adopted because the court's previous definition came from a software dictionary and the patents are hardware-related. The parties agree that the meaning of "instruction register" in the

---

[18] *See Therasense, Inc. v. Becton, Dickinson & Co.*, 560 F. Supp. 2d 835, 844 (N.D. Cal. 2008) (following courts in the Northern District of California that "have required a litigant to meet the Civil Local Rule 7-9 standard when requesting reconsideration of a claim construction").

[19] *See* Docket No. 358-2, Reexam. Cert., col.1 ll.55-60.

[20] *See* Docket No. 336 at 11.

[21] *Id.* at 10 (quoting MICROSOFT COMPUTER DICTIONARY 276 (5th ed. 2002)).

[22] *See id.* at 11 n.23.

context of hardware is a "register that receives and holds one or more instructions for supplying to circuits that interpret the instructions." The court takes this construction as its starting point.

TPL urges the court to keep this construction while Plaintiffs argue for a more limited construction requiring that the operands in the register be right-justified. Even though Judge Ware's prior order indicated he was interested in an explanation of the prosecution history, the parties' arguments remain focused on the specification.

Plaintiffs argue that the specification requires the right-justified limitation for the register that it seeks. The Federal Circuit has instructed that "the specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess" or "reveal an intentional disclaimer."[23] However, only a clear disclaimer can justify narrowing the construction.[24] Where a patent consistently references a certain limitation or a preferred embodiment as the present invention, that also can serve to limit the scope of the invention where no other intrinsic evidence suggests otherwise.[25]

Here, Plaintiffs rely on a section of the patent specification that explains that the patented invention is able to use variable width operands because "operands must be right justified in the instruction register."[26] The specification describes this limitation as necessary to make the "magic" of the patent possible.[27] Plaintiffs argue that this is the equivalent of defining the "present invention," but the intrinsic evidence does not clearly support this limitation.

First, the right justified limitation is not a clear and consistent limitation given the overall context of the patent and the specification. The '749 patent is derived from an application that was subject to a ten-way restriction requirement that eventually resulted in six different patents. The original application, which eventually issued as the '749 patent disclosed all of the inventions in

---

[23] *Phillips*, 415 F.3d at 1316.

[24] *See Voda v. Cordis Corp.*, 536 F.3d 1311, 1320 (Fed. Cir. 2008).

[25] *See Absolute Software, Inc.*, 659 F.3d at 1136.

[26] *See* Docket No. 358-2 at col.18 ll.43-45.

[27] *Id.*

what is now their extensive shared specification.[28] Plaintiffs rely on one small section of the common specification, with the heading "Variable Width Operands," covering about twenty lines of the thirty-three column specification.[29] Although this small section contains strong limiting language, because the specification is common to ten different inventions, it does not necessarily apply to the '749 Patent. In fact, Judge Ware previously held that one of those inventions, disclosed in the '584 patent, deals specifically with variable width operands.[30] But variable width operands are not essential to what is claimed in the '749 Patent. Claim 1 of the '749 Patent, the claim at issue here, does not contain the term operand or require variable width operands. Although parties focus on the '749 patent, the same reasoning applies to the '890 Patent.

Second, the specification actually discloses an embodiment where the operands are not right justified. In one embodiment, the instruction register receives four 8-bit instructions.[31] The specification disclosed two instructions, the "Read-Local-Variable XXXX" and "Write-Local-Variable XXXX," which are fixed width instructions that have a 4-bit opcode and a 4-bit operand.[32] These instructions can go into any of the four 8-bit slots in the instruction register and thus would contain operands that are not right justified.[33] At oral argument, Plaintiffs disputed TPL's characterization of these embodiments, arguing that the "4-bit operands" are not actually operands, but the location in temporary storage where the operand actually exists.[34] Even if the location in temporary storage is not a traditional operand, it acts similarly to one and adds further intrinsic evidence supporting a finding that the right justified limitation does not apply to the '749 and '890 patents.

---

[28] *See generally*, Docket No. 358-2 at col.1-35.

[29] *See* Docket No. 358-2 at col.18 ll.35-56.

[30] *See* Docket No. 336 at 11.

[31] *See* Docket No. 358-2 at col.7 ll.50-58.

[32] *See* Docket No. 358-2 at col.31-32 ll.45-15.

[33] *See generally*, *id.* at col.7 ll.50-58.

[34] *See* Docket No. 382 at 106-07.

Plaintiffs do briefly cite to the prosecution history where, in a handwritten summary of an in-person interview in response to a Patent Office Action rejecting several of the claims of a related patent, the examiner stated "Claim 1: Operand width is variable + right adjusted."[35] Because various claims were withdrawn, however it is unclear to exactly what claim the examiner referred. This is not clear and unmistakable disavowal by the applicant.[36]

The parties agreed upon meaning alone should control. Accordingly, the court construes "instruction register" as the "register that receives and holds one or more instructions for supplying to circuits that interpret the instructions."

B. "ring oscillator"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is (1) non-controllable; and (2) variable based on the temperature, voltage and process parameters in the environment	an oscillator having a multiple, odd number of inversions arranged in a loop

The parties ask the court to construe the term "ring oscillator" as it is used in claim 1 of the '336 Patent. Judge Ware held that one of ordinary skill in the art would understand the term to mean "interconnected electronic components comprising multiple odd numbers of inverters arranged in a loop."[37] However, he ordered more briefing as to whether the court should give the terms a specialized meaning based upon the statements of the inventors during reexamination to distinguish their invention from the Talbot Patent.[38]

Once again, the parties agree on the basic meaning of the term, but dispute additional limitations. They agree that the meaning of the term is at least "an oscillator having a multiple, odd

[35] Docket No. 363-19 at 2.

[36] *See Univ. of Pittsburgh of Commonwealth Sys. of Higher Educ. v. Hedrick*, 573 F.3d 1290, 1297 (Fed. Cir. 2009) (finding a "patentee may limit the meaning of a claim term by making a clear and unmistakable disavowal of scope during prosecution," but an examiner's summary of disavowal may only create a "weak inference" of the disavowal); *3M Innovative Properties Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1373 (Fed. Cir. 2003) (finding that prosecution history "cannot be used to limit the scope of a claim unless the *applicant* took a position before the PTO." (emphasis in the original)).

[37] Docket No. 336 at 13.

[38] *Id.* at 14-16.

number of inversions arranged in a loop." TPL urges the court to adopt meaning alone while the Plaintiffs argue that the term must be further limited to be: (1) non-controllable and (2) variable based on temperature, voltage, and process parameters in the environment. Plaintiffs argue that the prosecution history and specification support their position. As explained below, the prosecution history is too ambiguous to support Plaintiffs' construction in full, but the specification and especially the claim language do support Plaintiffs' second limitation.

1. Prosecution history

A "clear and unmistakable" disavowal by the patentee during prosecution or reexamination can narrow the scope of a claim.[39] However, because the "ongoing negotiations between the inventor and the examiner" can "often produce ambiguities," the doctrine only applies to "unambiguous disavowals."[40]

In the patent examiner's summary of his meeting with the patent owner, he wrote that

> the patent owner further argued that the reference of Talbot does not teach of a 'ring oscillator.' The patent owners discussed features of a ring oscillator, such as being non-controllable and being variable based upon the environment. The patent owner argued that these features distinguish over what Talbot teaches.[41]

The examiner finished his summary noting that he would "reconsider the current rejection based upon a forthcoming response, which will include arguments similar to what was discussed."[42] The subsequent written response argued that the Talbot reference did not teach a ring oscillator generally, and did *not* specifically argue that the ring oscillator was "non-controllable."[43] The examiner accepted this argument and withdrew the rejection.[44]

---

[39] *Grober v. Mako Products, Inc.*, 686 F.3d 1335, 1341 (Fed. Cir. 2012), reh'g denied (Sept. 14, 2012).

[40] *Id.*

[41] Docket No. 357-5 at 5. The interview summary relates to the '148 patent, but it shares the same specification with the '336 patent.

[42] *Id.*

[43] *See id.*

[44] *Id.* at 27.

Plaintiffs argue that the examiner's summary is a clear disavowal that should limit the scope of the claim. The court disagrees. The Federal Circuit has suggested that where, as here, the "disavowal" is only an examiner's summary of a patentee's statement, it only creates a "weak inference" of a disavowal.[45] The subsequent prosecution history does not support Plaintiffs' claim construction because the patent owner appears to have made a different argument in his written reply, simply stating that the Talbot reference did not include a ring oscillator *generally* and not distinguishing the ring oscillator of the '336 Patent based on the examiner's stated exemplary features of ring oscillators.[46]

During prosecution, the patent owner also stated that the "the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so."[47] This statement is not a disavowal because it only affirms that external inputs are "not required." The statement does not clearly impose a prohibition on all types of control.

2. Specification

Plaintiffs also argue that the specification supports their proposed construction. The specification describes the "ring oscillator" as having its frequency "determined by the parameters of temperature, voltage, and process."[48] Although this portion of the specification appears to disclose the preferred embodiment rather than constitute an express limitation on the claimed invention,[49] Claim 1 of the '336 Patent *claims* that the processing frequency of the CPU and the ring

[45] *See Univ. of Pittsburgh*, 573 F.3d at 1297.

[46] *See generally*, *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1124 (Fed. Cir. 2004) (describing a series of exchanges between the patent owner and the examiner as the parties "talking past one another" and finding no clear evidence of a disavowal from the confused exchange).

[47] Docket No. 363-4 at 6.

[48] *See* Docket No. 358-6 at col.16 ll.59-60.

[49] *See Brookhill-Wilk 1, LLC. v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1301-02 (Fed. Cir. 2003) ("statements from the description of the preferred embodiment are simply that-descriptions of a preferred embodiment. . . Absent a clear disclaimer of particular subject matter, the fact that the inventor anticipated that the invention may be used in a particular manner does not limit the scope to that narrow context.")

oscillator vary together due to manufacturing variations, operating voltage, and temperature.[50] The claim itself provides that the "ring oscillator" is "constructed of the same process technology with corresponding manufacturing variations" on the same single integrated circuit so that its performance will fluctuate with the CPU because they are subject to the same "manufacturing variations" and "operating voltage and temperature."[51] During oral argument, TPL admitted that a ring oscillator on the same microprocessor as the CPU will vary based upon voltage, temperature, and process variations.[52] Therefore, based upon the claim language and the specification, the court finds that the disclosed "ring oscillator" varies with voltage, temperature, and process variations.

Even though the claimed "ring oscillator" is "determined by the parameters of temperature, voltage, and process," it does not necessarily follow, as Plaintiffs' argue, that the "ring oscillator" must be non-controllable.[53] The claims do not mention "controllable" or "non-controllable" in relation to the "ring oscillator" and neither does the specification. The term "non-controllable" is only used by the patent examiner in the prosecution history discussed above. Additionally, in the preferred embodiment, the "ring oscillator" is "determined" by temperature, voltage, and process,[54] which suggests at least one embodiment in which the ring oscillator is controlled.

Because of the clear limitation in the claims that temperature, voltage, and process determine the "ring oscillator's" frequency, the court includes those limitations in the construction of the term, but does not find similar support for importing the "non-controllable" limitation. The court therefore construes "ring oscillator" as "an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment."

---

[50] *See* Docket No. 358-6, Reexam. Cert. col.2 ll.3-5.

[51] *Id.* at col.1-2 ll.59-05.

[52] *See* Docket No. 382 at 49:3-7.

[53] *See, e.g., Brookhill-Wilk*, 334 F.3d at 1301-02.

[54] *See* Docket No. 358-6 at col.16 ll.59-60.

C. "separate DMA CPU"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
a central processing unit that accesses memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit	Electrical circuit for reading and writing to memory that is separate from a main CPU

Judge Ware previously construed the term "separate direct memory access central processing unit" ("separate DMA CPU") from Claim 11 of the '890 Patent. Claim 11 claims

> A microprocessor, which comprises a main central processing unit and a separate direct memory access [DMA] central processing unit [CPU] in a single integrated circuit comprising said microprocessor . . .

The court construed "separate DMA CPU," consistent with its plain and ordinary meaning as "a central processing unit that accesses memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit."[55] Plaintiffs urge the court to keep this construction while TPL argues that previously unaddressed parts of the prosecution history support a different construction broad enough to include standard DMA controllers, which do not execute instructions.

TPL's primary argument is that the history of the Moore patents supports a broader construction. TPL argues that the DMA CPU that fetches and executes its own instructions was one of the ten categories of inventions derived from the original application, but not the invention that eventually became the patent at issue, the '890 Patent. As explained above, the original patent application for what became the '749 Patent was subject to a ten-way restriction. A restriction indicates that "two or more independent and distinct inventions are claimed in one application."[56] One of these 10 categories of inventions was focused on a "microprocessor system having a DMA for fetching instruction[s] for a CPU and itself."[57] The patentee eventually abandoned this application. The '890 Patent came from a different category of invention "drawn to a microprocessor architecture."[58] TPL argues that because the '890 Patent came from a different

[55] Docket No. 336 at 13.

[56] 35 U.S.C. § 121.

[57] Docket No. 368-7 at 3.

[58] *Id*. *See also* Docket No. 356 at 3-4.

invention category, it should not be read to include the definition of the "DMA CPU" that was the subject of another invention.

The court disagrees. The fact that one abandoned patent focused on a particular subject matter does not necessarily mean that same subject matter cannot be within the scope of another related patent based upon the same specification. First, restriction requirements have little, if any, evidentiary weight.[59] Second, there is nothing in the claims to suggest that "DMA CPU" should have anything other than its plain and ordinary meaning. Third, the specification supports the plain and ordinary meaning. The specification discloses a "DMA CPU" in figures 2 and 9. When describing figure 2, the specification states that the "DMA CPU 72 controls itself and has the ability to fetch and execute instructions. It operates as a co-processor to the main CPU 70."[60] The "DMA CPU 314" in figure 9 is part of another microprocessor that the specification describes as equivalent to the microprocessor in figure 2.[61] A separate passage in a later section of the specification describes another embodiment where the "DMA processor 72 of the microprocessor 50 has been replaced with a more traditional DMA controller 314."[62] The specification goes on to describe the characteristics of a DMA controller. These sections are clear that a DMA controller is distinct from a DMA CPU and the patent refers to each by name where appropriate. Thus where the patent claims a DMA CPU, it means a DMA CPU and not a DMA controller.

TPL also argues that statements made during reexamination by the requester and the examiner support its position. The court disagrees. First, the examiner and the reexamination requester made the cited statements, not the patent owner.[63] Second, regardless of who made the

[59] *See Honeywell Int'l, Inc. v. ITT Indus., Inc.*, 452 F.3d 1312, 1319 (Fed. Cir. 2006); *Rambus Inc. v. Hynix Semiconductor Inc.*, 569 F. Supp. 2d 946, 962 (N.D. Cal. 2008) ("In laying out the details of the original restriction requirement, the court recognizes its limited evidentiary significance.").

[60] *See* Docket No. 368-2 at col.8 ll.22-24.

[61] *See id.* at col.9 ll.5-6.

[62] *Id.* at col.12 ll.62-65.

[63] *See 3M Innovative Properties Co.*, 350 F.3d at 1373 (finding that prosecution history "cannot be used to limit the scope of a claim unless the *applicant* took a position before the PTO."(emphasis in the original)).

statements, they do not clearly show that the term "DMA CPU" was understood to include a DMA controller.[64]

During oral argument, TPL argued that the term "independently" in the original construction is unsupported.[65] The court agrees with this point. Even if the DMA CPU fetches and executes its own instructions, it cannot do so independently. The reason for putting the CPU and DMA CPU on the same chip is so they can work together.[66] Otherwise, the evidence in support of changing the court's prior construction is unpersuasive.

The court construes "separate DMA CPU" as "a central processing unit that accesses memory and that fetches and executes instructions directly and separately of the main central processing unit."

D. "supply the multiple sequential instructions"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
provide the multiple sequential instructions in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during a single memory cycle without using a prefetch buffer or a one-instruction-wide instruction buffer that supplies on instruction at a time	provide the multiple sequential instructions in parallel to said central processing unit integrated circuit during a single memory cycle

The parties ask the court to construe the phrase "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle," from claim 1 of the '749 patent. Judge Ware previously determined that this phrase was composed of commonly used words that the patentee intended to have their plain and ordinary meaning. Plaintiffs argue for a narrower construction based upon disavowals during reexamination while TPL argues for a broad construction. The parties specifically dispute what limitations the patent places on how the "multiple sequential instructions" are provided to the CPU.

[64] *See id.* at 1346-47 ("An applicant's silence in response to an examiner's characterization of a claim does not reflect the applicant's clear and unmistakable acquiescence to that characterization if the claim is eventually allowed on grounds unrelated to the examiner's unrebutted characterization.").

[65] *See* Docket No. 382 at 121-22.

[66] *See* Docket No. 368-2, Reexam. Cert., col.1 ll.22-24; Docket No. 368-2 at col.8 ll.22-24 (the DMA CPU "operates as a co-processor to the main CPU").

During reexamination, TPL unambiguously disavowed that instructions could be provided to the CPU one-by-one. The PTO issued a reexamination rejecting claims in the '749 Patent, including claim 1, based upon the "Edwards" patent[67] and an article by Doug MacGregor.[68] To distinguish the Edwards patent, TPL argued that in the Edwards patent, "instructions are supplied to a one-instruction-wide instruction buffer, one at a time," while for the '749 Patent "[f]etching multiple instructions into a prefetch buffer and then supplying them one at a time is not sufficient to meet the claim limitation—the supplying of 'multiple sequential instructions to a CPU during a single memory cycle.'"[69] Similarly, in distinguishing the invention in MacGregor, TPL wrote that "non-parallel supplying of instructions to the CPU is not supplying them to the CPU during a single memory cycle as required by the claim."[70] By this language, TPL clearly and unambiguously disavowed supplying instructions to the CPU one-by-one.

Plaintiffs also urge the court to find TPL disavowed specific structures or components in the above statements, but these statements as to structures are not clearly disavowals because they are made in the context of describing the prior art. There may be ways of incorporating such structures consistent with not supplying the instructions one-by-one.

Accordingly, the court construes the phrase "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle" as "provide the multiple sequential instructions in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during a single memory cycle."

E. "clocking said CPU"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
timing the operation of the CPU such that it will always execute at the maximum frequency possible, but never too fast	timing the operation of the CPU

[67] U.S. Patent No. 4,680,698.

[68] Doug MacGregor *et al.*, "The Motorola MC68020," IEEE Micro 101 (August 1984).

[69] Docket No. 358-3 at 27.

[70] *Id.* at 46.

The parties ask the court to construe "clocking said CPU," which appears in claims 1, 6, and 10 of the '336 Patent. Generally speaking, "clocking the CPU" refers to using the system clock to control the speed of the CPU. Judge Ware previously considered "clocking said CPU" and based upon the plain and ordinary meaning of the term, construed it as "providing a timing signal to said central processing unit." The court considered other language in the written description that suggested a more limited construction, but ultimately determined that the patentee had not "demonstrated a clear intention to limit the claim scope."[71] Similarly, Judge Ward construed a longer term[72] from claim 1 containing the term "clocking said CPU" as "an oscillator that generates the signal(s) used for timing the operation of the CPU."[73] In construing the term, Judge Ward similarly did not adopt the type of limiting language that Plaintiffs advocate.

As discussed above and explained in the patent, the disclosed invention uses a variable speed clock—a ring oscillator—that varies with temperature, voltage, and process. The specification states that "[b]y deriving system time from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast."[74] Plaintiffs argue that this is a clear limitation that should be read into the claims. In general, absent a clear intention to limit the scope of a claim, a description of an embodiment should not limit claim language that otherwise has a broader effect.[75] This rule applies even if the patent only describes a single embodiment.[76] Judge Ware previously considered and rejected Plaintiffs attempt to limit the claim based upon the specification and this court agrees. There is no support in the claim language itself for the requirement that the clock always forces the CPU to operate at its maximum frequency. The court finds that operating at

[71] Docket No. 336 at 17-18 (quoting *Innova/Pure Water*, 381 F.3d at 1117).

[72] Judge Ward construed "an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit."

[73] *Tech. Properties Ltd. v. Matsushita Elec. Indus. Co., Ltd.*, 514 F. Supp. 2d 916, 927 (E.D. Tex. 2007) aff'd sub nom., 276 F. App'x 1019 (Fed. Cir. 2008).

[74] *See* Docket No. 358-6 at col.16-17 ll.63-2.

[75] *See Innova/Pure Water*, 381 F.3d at 1117.

[76] *See id.*

the maximum frequency is merely the preferred embodiment and not the only manner in which the invention can operate.

Plaintiffs also try to introduce evidence from the prosecution history to support their argument. Although Plaintiffs quote a section from the prosecution history where the applicants used the magic words "the present invention," what the applicants disclosed is that the present invention includes a variable speed clock on the same microprocessor as the CPU and thus its speed will vary based upon environmental conditions.[77] This is exactly what is claimed in claim 1. The excerpt goes on to explain that one advantage of the variable speed clock is that it "allows the microprocessor to operate at its fastest safe operating speed,"[78] but again, this is just one embodiment and not necessarily a *requirement* of the invention. Plaintiffs' other citations to the prosecution history are similarly unconvincing.

Because the parties have not convinced the court that the prior construction was in error, the Court declines to change its construction. Accordingly, the court construes "clocking said CPU" as "providing a timing signal to said central processing unit."

IV. CONCLUSION

For the reasons set forth above, the court construes the claims as follows:

CLAIM TERM	CONSTRUCTION
"instruction register"	Register that receives and holds one or more instructions for supplying to circuits that interpret the instructions
"ring oscillator"	an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment
"separate DMA CPU"	a central processing unit that accesses memory and that fetches and executes instructions directly and separately of the main central processing unit
"supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle"	provide the multiple sequential instructions in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during

[77] *See* Docket No. 358-9 at 4-5.

[78] *Id.* at 5.

	a single memory cycle
"clocking said CPU"	Providing a timing signal to said central processing unit

Dated: August 21, 2013

PAUL S. GREWAL
United States Magistrate Judge

E-Filed 5/13/2011

IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC.

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED,

Defendants.

Case No. 5:08-cv-00877 JF/HRL

HTC CORPORATION, HTC AMERICA, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED,

Defendants.

Case No. 5:08-cv-00882 JF/HRL

BARCO N.V., a Belgian Corporation

Plaintiff,

v.

TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORP., ALLIACENSE LTD.,

Defendants.

Case No. 5:08-cv-05398 JF/HRL

ORDER[1] GRANTING IN PART AND DENYING IN PART DEFENDANTS' MOTIONS TO AMEND INFRINGEMENT CONTENTIONS

Defendants Technology Properties Ltd., Patriot Scientific Corp., and Alliacense, Ltd. (collectively, "TPL") seek leave to amend their infringement contentions with respect to United States Patent Nos. 5,530,890 ("the '890 patent") and 5,440,749 ("the '749 patent") in each of the above-captioned actions.[2] The Court heard oral argument on April 22, 2011. Because TPL seeks to assert certain claims that it reasonably could not have asserted prior to the reexamination of the patents, the motions will be granted in part and denied in part.

I. BACKGROUND

TPL first sought to amend its preliminary infringement contentions nearly one year ago, after this Court lifted a stay that was imposed pending reexamination of several of the patents-in-suit by the United States Patent and Trademark Office ("USPTO"). Although TPL was permitted to amend its infringement contentions at that time with respect to the '336 patent,[3] the

[1] This disposition is not designated for publication in the official reports

[2] Pursuant to Civil L.R. 3-12, the three actions have been related.

[3] Amendment to the '336 infringement contentions was permitted because all parties agreed that amended invalidity and infringement contentions were needed after the reexamination of the '336 patent. *See* Transcript of Case Management Conference Held on February 12, 2010; Order Following Case Management Conference, filed February 22, 2010.

Court denied TPL's motion to amend its contentions with respect to United States Patent No. 6,598,148 ("the '148 patent") and the '749 and '890 patents, finding that TPL had not been diligent. Order Denying Defendants' Motions to Amend Infringement Contentions, filed September 10, 2010.

TPL now renews its motion to amend its infringement contentions with respect to the '749 and '890 patents based upon subsequent activity by the USPTO.

A. The Reexaminations

In November 2010, the USPTO issued a Notice of Intent to Issue Reexamination Certificate ("NIRC") for the '890 patent. Upon receipt of the NIRC, TPL notified Plaintiffs of its intention to seek leave to assert new claims once the Reexamination Certificate issued. Mar Decl. Ex. B. On March 1, 2011, TPL received the Reexamination Certificate, confirming the patentability of existing claims 5–10 and new claims 11–20. Apart from one clarification to independent claim 11, new claims 11-20 track the patent's original claims 1-10 word-for-word. TPL served the proposed amendments to its infringement contentions the same day. The proposed amended contentions assert claims 7, 9, 11, 12, 13, 17, and 19 against each Plaintiff.

On February 11, 2011, the USPTO issued the NIRC for the '749 patent, confirming the patentability of claims 1-7, 10-20, 21-27, 30, and 34-62. Claim 9 was canceled and replaced by claim 59. TPL expects thirty new claims to be confirmed by the final Reexamination Certificate. Asserting that it wishes to avoid further delay in the instant proceedings, TPL seeks to amend its infringement contentions with respect to the '749 patent before the Certificate issues: it seeks to assert claims 1, 23, 24, 43, 44, 45, 47, 54, 55, and 59 against each Plaintiff. Together, the proposed amendments would add a total of thirteen newly-accused products in the HTC action and one newly-accused product in the Acer action, each of which TPL contends entered or will enter the U.S. market after June 2010, when TPL last attempted to amend its contentions.[4]

II. LEGAL STANDARD

[4] After it filed the instant motions, TPL withdrew its request to add several newly-accused products in the Acer and Barco actions.

An action is governed by the version of the local rules in effect at the time the underlying action is filed. *See Seiko Epson Corp. v. Coretronic Corp.*, No. C 06-06946 MHP, 2008 WL 2563383, at *2 (N.D. Cal. June 23, 2008). Plaintiffs Acer Inc., Acer America Corporation, and Gateway, Inc. (collectively, "Acer") and HTC Corporation and HTC America, Inc. (collectively, "HTC") filed their actions on February 8, 2008. Under the Patent Local Rules in effect at that time, "[a]mendment or modification of the Preliminary or Final Infringement Contentions . . . , other than as expressly permitted in Patent L.R. 3-6, may be made only by order of the Court, which shall be entered only upon a showing of good cause."[5] Patent L.R. 3-7. The Patent Local Rules were amended effective March 1, 2008. Plaintiff Barco, N.V. ("Barco") filed its action on December 1, 2008. The version of Patent Local Rule 3-6 in effect as of that date provides that:

> Amendment of the Infringement Contentions or the Invalidity Contentions may be made only by order of the Court upon a timely showing of good cause. Non-exhaustive examples of circumstances that may, absent undue prejudice to the non-moving party, support a finding of good cause include: (a) a claim construction by the Court different from that proposed by the party seeking amendment; (b) recent discovery of material, prior art despite earlier diligent search; and (c) recent discovery of nonpublic information about the Accused Instrumentality which was not discovered, despite diligent efforts, before the service of the Infringement Contentions.

The Advisory Subcommittee commented that even after March 1, 2008, Patent Local Rule 3-6 would continue to be "regulated by the well-established 'good cause' test." Patent Local Rules Advisory Subcommittee Report at 2. Thus, prior cases discussing the concept of "good cause" remain relevant precedent.

In order to demonstrate good cause, TPL must show first that it was diligent in amending its contentions and then that the non-moving parties will not suffer undue prejudice if the motion to amend is granted. *O2 Micro Int'l Ltd. v. Monolithic Power Sys., Inc.*, 467 F.3d 1355, 1366-68 (Fed. Cir. 2006) (concluding that if a party seeking to amend did not demonstrate diligence, there

---

[5] The applicable version of Patent Local Rule 3-6(a) allows a party alleging infringement to amend its infringement contentions without leave of court if the party believes in good faith that the amendment is required by the court's claim construction ruling or documents produced in connection with the opposing party's invalidity contentions. Here, the Court has not issued a claim construction ruling, nor does TPL allege that it seeks to amend in response to the invalidity contentions served by Plaintiffs.

was "no need to consider the question of prejudice").[6] *See also Johnson v. Mammoth Recreations*, 975 F.2d 604, 609 (9th Cir. 1992) (citation omitted) ("Although the existence or degree of prejudice to the party opposing the modification might supply additional reasons to deny a motion, the focus of the [good cause] inquiry [under Federal Rule of Civil Procedure 16(b)] is upon the moving party's reasons for seeking modification. If that party was not diligent, the inquiry should end."). While the court in *O2 Micro* considered "how quickly the party moves to amend its contentions once a new theory of infringement . . . comes to light," Hon. James Ware & Brian Davy, *The History, Content, Application and Influence of the Northern District of California Patent Local Rules*, 25 SANTA CLARA COMPUTER & HIGH TECH. L.J. 965, 995 (2009), this Court has concluded that "the Court also must address whether the party was diligent in discovering the basis for the proposed amendment." *West v. Jewelry Innovations, Inc.*, No. C07-1812 JF (HRL), 2008 WL 4532558, at *2 (N.D. Cal. Oct. 8, 2008).

The party seeking to amend its contentions bears the burden of establishing diligence. *O2 Micro*, 467 F.3d at 1366-67. "Unlike the liberal policy for amending pleadings, the philosophy behind amending claim charts is decidedly conservative, and designed to prevent the 'shifting sands' approach to claim construction." *LG Elecs. Inc. v. Q-Lity Computer Inc.*, 211 F.R.D. 360, 367 (N.D. Cal. 2002). The rules were "designed to require parties to crystallize their theories of the case early in the litigation and to adhere to those theories once they have been disclosed." *O2 Micro*, 467 F.3d at 1366 n. 12 (quoting *Nova Measuring Instruments Ltd. v. Nanometrics, Inc.*, 417 F. Supp.2d 1121, 1123 (N.D. Cal .2006)). "Nevertheless, judges in this district have recognized that the Patent Local Rules are 'not a straitjacket into which litigants are locked from the moment their contentions are served. There is a modest degree of flexibility, at least near the outset.'" *Halo Electronics, Inc. v. Bel Fuse Inc.*, No. C07-06222 RMW (HRL),

[6] Other factors relevant to this inquiry include "the relevance of the newly-discovered prior art, whether the request to amend is motivated by gamesmanship, [and] the difficulty of locating the prior art." *Acco Brands, Inc. v. PC Guardian Anti-Theft Products, Inc.*, No. C 04-03526 SI, 2008 WL 2168379 at *1 (N.D. Cal., May 22, 2008) (citing *Yodlee, Inc. v. CashEdge, Inc.*, No. C 05-01550 SI, 2007 WL 1454259, at *2-3 (N.D. Cal. May 17, 2007)).

2010 WL 3489593, at * 1 (N.D. Cal. Sep. 3, 2010) (citing *Comcast Cable Communications Corp., LLC v. Finisar Corp.*, No. C06-04206, 2007 WL 716131 at *2 (N.D.Cal. Mar.2, 2007).

III. DISCUSSION

After nearly three years of litigation, this case still is in its early stages. Plaintiffs suggest that TPL's current effort to amend its infringement contentions is motivated by gamesmanship, as evidenced by the fact that TPL did not file the instant motions until after claim construction briefing was complete. In response, TPL argues that the timing of its proposed amendments was dictated by the reexamination process, noting that it kept Plaintiffs abreast of developments in that process until it became clear which claims would emerge and in what form.

A. Non-Opposition

HTC and Acer do not object to the substitution of claims 1 and 2 of the '890 patent by replacement claims 11 and 12,[7] nor do they object to the substitution of claim 9 of the '749 patent by replacement claim 59. Each Plaintiff also agrees to permit amendment with respect to claim 1 of the '749 patent in order to address the new limitations that were added to that claim during the reexamination.

B. Diligence

TPL contends that because it was uncertain which claims would survive reexamination, it could not conduct a detailed infringement analysis prior to the issuance of the NIRCs for the '749 and '890 patents. Although TPL brought its previous motion to amend based in part on claims that stood rejected as of June 2010, it certainly was not required to do so. In the present context, diligence does not require that a party awaiting USPTO action assert all potential claims. Instead of promoting an orderly process, such a request would add confusion and uncertainty to the litigation.

After it received the NIRC for the '890 patent, TPL promptly notified Plaintiffs of its intent to amend its '890 contentions (Mar Decl. Ex. B), and it began investigating products that

[7] Barco also does not object to the substitution of claim 1 of the '890 patent by claim 11.

might infringe the pending claims. *See* Mar. 17, 2011 Brataadiredja Decl. ¶ 4. TPL thus was prepared to serve its amended contentions on the same day that the Reexamination Certificate issued. With respect to the '749 patent, TPL offered to assert claims conditionally based on the NIRC, and it completed its investigation of infringing products and served its proposed amended contentions approximately one month after the NIRC issued. *See* Mar. 25, 2011 Brataadiredja Decl. ¶ 3.

HTC points out that as a matter of law, the scope of the claims asserted under the '749 and '890 patents could not have been altered by the reexaminations. 35 U.S.C. § 305 ("No proposed amended or new claim enlarging the scope of a claim of the patent will be permitted in a reexamination proceeding under this chapter."). Accordingly, HTC contends that the universe of potentially infringing products likewise could not have expanded, and TPL did not need to wait for the issuance of the NIRCs before conducting its renewed investigation into infringing products. However, given the fact that TPL did not know which claims would emerge from the reexamination, it was not unreasonable for TPL to investigate potentially infringing products after the NIRCs were issued.

HTC also argues that public information regarding the newly-accused products was available even before TPL sought to amend its contentions in June 2010. However while, information regarding these products may have been available in the form of press releases or other media, it appears that none of the new instrumentalities actually entered the market until after TPL served its amended contentions in May 2010. *See, e.g.*, Chen Decl. Ex. D (press release indicating that the HTC Aria would be available June 20, 2010);[8] *Id.* Ex. F (article indicating that the HTC Desire was released on August 27, 2010). 35 U.S.C. § 271 prohibits the use or sale of infringing products, not the announcement of intent to sell infringing products. Thus, even if public information about these products was available to it prior to June 2010, TPL

[8] Although TPL submitted a corrected version of its proposed amended contentions to HTC on June 22, 2010, two days after the Aria was released, this correction did not alter the substance of its proposed contentions. *See* Corrected Amended Patent Local Rule 3-1 Preliminary Infringement Contentions, June 25, 2010 Mar Decl. Ex. B.

did not have a legal basis for accusing HTC of infringement until the products actually had entered the market.[9] Moreover, as TPL points out, nothing requires parties to bring a motion to amend each time a new product enters the market, as this could cause undue delay in the proceedings and prejudice to all parties involved.

C. Prejudice

Plaintiffs argue that TPL's attempt to assert claims 7 and 9 of the '890 patent in addition to claims 17 and 19 is unnecessary and prejudicial because the latter are mirror images of the former. Acer observes that in order to promote judicial economy courts frequently limit the number of claims that a patentee may assert. *See, e.g., Auto Wax Co. v. Mark V Products*, No. 3:99-CV-0982-M, 2001 WL 292597, at *1 (N.D. Tex. March 14, 2001) (requiring plaintiff to limit number of claims to be tried from 86 to 19); *Fenster Family Patent Holdings, Inc. v. Siemens Medical Solutions USA*, No. 04-0038-JJF, 2005 WL 2304190, at *3 (D. Del. Sept. 20, 2005) (requiring plaintiff to reduce its 90 claims to 10); *Verizon Calif., Inc. v. Ronald A. Katz Tech. Licensing, L.P.*, 326 F.Supp.2d 1060, 1066 (C.D. Cal. 2003) (requiring plaintiff to select a maximum of three representative claims for each patent it contended was infringed). TPL concedes that "[b]ecause the scope of new independent claim 11 is the same as the scope of original independent claim 1, the infringement theories underlying the claim charts for the new claims are the same as those for the original claims." Mar. 17, 2011 Brataadiredja Decl. ¶ 3. Given that assessment, it appears that the assertion of all four claims would be redundant. Because claim 1 has been canceled and all four claims cover the same ground, logic dictates that TPL be limited to the assertion of claims 17 and 19, which depend from surviving claim 11.

Finally, Plaintiffs argue that they will be prejudiced by having to conduct additional prior art research and by having to brief the new claim terms that were added during reexamination. However, any such prejudice is insufficient to outweigh TPL's right to assert new claims and the

---

[9] For this reason, TPL has sought to accuse conditionally the Acer Iconia, which will be released in the United States later this summer. Perhaps TPL could have taken this approach last year with respect to other HTC products it seeks to accuse now. However, it was not required to do so.

Court's interest in resolving the parties' disputes as comprehensively as is possible.

IV. ORDER

Accordingly, TPL's motions will be GRANTED IN PART AND DENIED IN PART. TPL may amend its infringement contentions to: (a) assert claims 11, 12, 13, 17, and 19 of the '890 patent and claims 1, 23, 24, 43, 44, 45, 47, 54, 55, and 59 of the '749 patent against each Plaintiff; (b) include the thirteen newly-accused HTC instrumentalities; and (c) include conditionally the Acer Iconia. A case management conference is hereby scheduled for June 24, 2011 at 10:30 a.m. for the purpose of setting a new date and briefing schedule for a claim construction hearing.

IT IS SO ORDERED.

DATED: May 13, 2011

JEREMY FOGEL
United States District Judge

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, et al.,

Defendants.

Case No.: 5:08-cv-00882-PSG

ORDER RE: EMERGENCY MOTION FOR ADDENDUM TO JURY INSTRUCTIONS

(Re: Docket Nos. 513, 590)

Before the court is Plaintiff HTC Corporation and HTC America, Inc.'s (collectively "HTC") Emergency Motion for Addendum to Jury Instructions. The parties appeared for a hearing earlier today. After considering the parties' arguments the court rules as follows:

The court's final jury instructions will instruct the jury that the terms "entire ring oscillator variable speed system clock" (in claims 1 and 11), "entire oscillator" (in claims 6 and 13), and "entire variable speed clock" (in claims 10 and 16) are properly understood to exclude any external clock used to generate a signal.[1]

[1] *See* Docket No. 513 at 11.

IT IS SO ORDERED.

Dated: September 20, 2013

PAUL S. GREWAL
United States Magistrate Judge

COOLEY LLP
HEIDI L. KEEFE (178960) (hkeefe@cooley.com)
MARK R. WEINSTEIN (193043) (mweinstein@cooley.com)
RONALD S. LEMIEUX (120822) (rlemieux@cooley.com)
KYLE D. CHEN (239501) (kyle.chen@cooley.com)
Five Palo Alto Square, 4th Floor
3000 El Camino Real
Palo Alto, California 94306-2155
Telephone: (650) 843-5000
Facsimile: (650) 857-0663

STEPHEN R. SMITH (*pro hac vice*) (stephen.smith@cooley.com)
One Freedom Square
Reston Town Center
11951 Freedom Drive
Reston, VA 20190-5656
Telephone: (703) 456-8000
Facsimile: (703) 456-8100

Attorneys for Plaintiffs
HTC CORPORATION and
HTC AMERICA, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION and HTC AMERICA, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED,

Defendants.

Case No. 5:08-cv-00882 PSG

[Related to Case No. 5:08-CV-00877 PSG]

~~[PROPOSED]~~ ORDER GRANTING EMERGENCY MOTION FOR CLARIFICATION OF ORDER ON ADDENDUM TO JURY INSTRUCTIONS

Complaint Filed: February 8, 2008
Trial Date: September 23, 2013

Date: September 23, 2013
Time: 9:00 a.m.
Place: Courtroom 5, 4th Floor
Judge: Hon. Paul S. Grewal

Having considered Defendants' Emergency Motion for Clarification of the Order on Addendum to the Joint Proposed Jury Instructions, the record in this case and all related facts and circumstances, and good cause appearing therefor, IT IS HEREBY ORDERED THAT:

The court's final jury instructions will instruct the jury that the terms "entire ring oscillator variable speed system clock" (in claims 1 and 11), "entire oscillator" (in claims 6 and 13), and "entire variable speed clock" (in claims 10 and 16) are properly understood to exclude any external clock used to generate the signal used to clock the CPU.

IT IS SO ORDERED.

Dated: September 23, 2013

Hon. Paul S. Grewal
United States Magistrate Judge

398111 v2/CO

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, et al.,

Defendants.

Case No.: 5:08-cv-00882-PSG

FINAL JURY INSTRUCTIONS

(Re: Docket Nos. 513, 645)

1. FINAL INSTRUCTIONS

Duty of Jury

Members of the Jury: It is my duty to instruct you on the law.

You must not infer from these instructions or from anything I have said or done as indicating that I have an opinion regarding the evidence or what your verdict should be.

It is your duty to find the facts from all the evidence in the case. To those facts you will apply the law as I give it to you. You must follow the law as I give it to you whether you agree with it or not. And you must not be influenced by any personal likes or dislikes, opinions, prejudices, or sympathy. That means that you must decide the case solely on the evidence before you. You will recall that you took an oath to do so.

In following all my instructions, you must follow all of them and not single out some and ignore others; they are all important.

Burden of Proof – Preponderance of the Evidence

When a party has the burden of proof on any claim or affirmative defense by a preponderance of the evidence, it means you must be persuaded by the evidence that the claim or affirmative defense is more probably true than not true.

You should base your decision on all of the evidence, regardless of which party presented it.

Burden of Proof – Clear and Convincing Evidence

When a party has the burden of proof on any claim or affirmative defense by clear and convincing evidence, it means you must be persuaded by the evidence that the claim or affirmative defense is highly probable. This is a higher standard of proof than proof by a preponderance of the evidence.

You should base your decision on all of the evidence, regardless of which party presented it.

What Is Evidence

The evidence you are to consider in your deliberations in deciding what the facts are consists of:

1. The sworn testimony of any witness;

2. The exhibits which are received into evidence; and

3. Any facts to which the lawyers have agreed.

What Is Not Evidence

In reaching your verdict, you may consider only the testimony and exhibits received into evidence. Certain things are not evidence, and you may not consider them in deciding what the facts are. I will list them for you:

(1) Arguments and statements by lawyers are not evidence. The lawyers are not witnesses. What they have said in their opening statements and their closing arguments, and at other times is intended to help you interpret the evidence, but it is not evidence. If the facts as you remember them differ from the way the lawyers have stated them, your memory of them controls.

(2) Questions and objections by lawyers are not evidence. Attorneys have a duty to their clients to object when they believe a question is improper under the rules of evidence. You should not be influenced by the objection or by the court's ruling on it.

(3) Testimony that has been excluded or stricken, or that you have been instructed to disregard, is not evidence and must not be considered. In addition sometimes testimony and exhibits are received only for a limited purpose; when I have given a limiting instruction, you must follow it.

(4) Anything you may have seen or heard when the court was not in session is not evidence. You are to decide the case solely on the evidence received at the trial.

Evidence for a Limited Purpose

Some evidence may be admitted for a limited purpose only.

When I instruct you that an item of evidence has been admitted for a limited purpose, you must consider it only for that limited purpose and for no other.

Direct and Circumstantial Evidence

Evidence may be direct or circumstantial. Direct evidence is direct proof of a fact, such as testimony by a witness about what that witness personally saw or heard or did. Circumstantial evidence is proof of one or more facts from which you could find another fact. You should consider both kinds of evidence. The law makes no distinction between the weight to be given to either direct or circumstantial evidence. It is for you to decide how much weight to give to any evidence.

Ruling on Objections

There are rules of evidence that control what can be received into evidence. When lawyers asked questions or offered exhibits into evidence and a lawyer on the other side thought it was not permitted by the rules of evidence, that lawyer may have objected. If I overruled the objection, the question was to be answered or the exhibit received. If I sustained the objection, the question was not answered, and the exhibit was not received. Whenever I sustained an objection to a question, you must ignore the question and must not guess what the answer might have been.

Sometimes I may have ordered that evidence be stricken from the record and that you disregard or ignore the evidence. That means that when you are deciding the case, you must not consider the evidence that I told you to disregard.

Credibility of Witnesses

In deciding the facts in this case, you may have to decide which testimony to believe and which testimony not to believe. You may believe everything a witness says, or part of it, or none of it. Proof of a fact does not necessarily depend on the number of witnesses who testify about it.

In considering the testimony of any witness, you may take into account:

(1) The opportunity and ability of the witness to see or hear or know the things testified to;

(2) The witness's memory;

(3) The witness's manner while testifying;

(4) The witness's interest in the outcome of the case and any bias or prejudice;

(5) Whether other evidence contradicted the witness's testimony;

(6) The reasonableness of the witness's testimony in light of all the evidence; and

(7) Any other factors that bear on believability.

The weight of the evidence as to a fact does not necessarily depend on the number of witnesses who testify about it.

No Transcript Available to the Jury

During deliberations, you will have to make your decision based on what you recall of the evidence. You will not have a transcript of the trial.

Taking Notes

I have permitted you to take notes to help you remember the evidence. If you did take notes, you may share them with your fellow jurors as you deliberate. No one will read your notes. They will be destroyed at the conclusion of the case.

Whether or not you took notes, you should rely on your own memory of the evidence. Notes are only to assist your memory. You should not be overly influenced by your notes or those of your fellow jurors.

Jury to Be Guided By Official English Language Translation/Interpretation

Languages other than English were used during this trial.

The evidence to be considered by you is only that provided through the official court interpreters or translators. Although some of you may know the language used, it is important that all jurors consider the same evidence. Therefore, you must accept the English interpretation or translation. You must disregard any different meaning.

Use of Interpreters in Court

You must not make any assumptions about a witness or a party based solely upon the use of an interpreter to assist that witness or party.

Duty to Deliberate

At the conclusion of these final instructions, you will begin your deliberations. When you begin your deliberations, you should elect one member of the jury as your presiding juror. That person will preside over the deliberations and speak for you here in court.

You will then discuss the case with your fellow jurors to reach agreement if you can do so. Your verdict must be unanimous. Each of you must decide the case for yourself, but you should do so only after you have considered all of the evidence, discussed it fully with the other jurors, and listened to the views of your fellow jurors.

Do not hesitate to change your opinion if the discussion persuades you that you should. Do not come to a decision simply because other jurors think it is right.

It is important that you attempt to reach a unanimous verdict but, of course, only if each of you can do so after having made your own conscientious decision. Do not change an honest belief about the weight and effect of the evidence simply to reach a verdict.

Deposition in Lieu of Live Testimony

You heard deposition testimony in this case. A deposition is the sworn testimony of a witness taken before trial. The witness is placed under oath to tell the truth and lawyers for each party may ask questions. The questions and answers are recorded. When a person is unavailable to testify at trial, the deposition of that person may be used at the trial.

You should consider deposition testimony, presented to you in court in lieu of live testimony, insofar as possible, in the same way as if the witness had been present to testify.

Do not place any significance on the behavior or tone of voice of any person reading the questions or answers.

Impeachment Evidence – Witness

The evidence that a witness lied under oath on a prior occasion may be considered, along with all other evidence, in deciding whether or not to believe the witness and how much weight to give to the testimony of the witness and for no other purpose.

Expert Opinion

Some witnesses, because of education or experience, were permitted to state opinions and the reasons for those opinions.

Opinion testimony should be judged just like any other testimony. You may accept it or reject it, and give it as much weight as you think it deserves, considering the witness's education and experience, the reason given for the opinion, and all the other evidence in the case.

Charts and Summaries Not in Evidence

Certain charts and summaries not received in evidence have been shown to you in order to help explain the contents of books, records, documents, or other evidence in the case. They are not themselves evidence or proof of any facts. If they do not correctly reflect the facts or figures shown by the evidence in the case, you should disregard these charts and summaries and determine the facts from the underlying evidence.

Demonstrative Evidence

During the trial, materials have been shown to you to help explain testimony or other evidence in the case. Other materials have also been shown to you during the trial, but they have not been admitted into evidence. You will not be able to review them during your deliberations because they are not themselves evidence or proof of any facts. You may, however, consider the testimony given in connection with those materials.

Communication with Court

If it becomes necessary during your deliberations to communicate with me, you may send a note through the courtroom deputy, signed by your presiding juror or by one or more members of the jury. No member of the jury should ever attempt to communicate with me except by a signed writing; I will communicate with any member of the jury on anything concerning the case only in writing, or here in open court. If you send out a question, I will consult with the parties before answering it, which may take some time. You may continue your deliberations while waiting for the answer to any question. Remember that you are not to tell anyone – including me – how the jury stands, numerically or otherwise, until after you have reached a unanimous verdict or have been discharged. Do not disclose any vote count in any note to the court.

Return of Verdict

A verdict form has been prepared for you. After you have reached unanimous agreement on a verdict, your presiding juror will fill in the form that has been given to you, sign and date it, and advise the court that you are ready to return to the courtroom.

II. PATENT JURY INSTRUCTIONS

Summary of Contentions

I will now summarize for you each party's contentions in this case. I will then tell you what each party must prove to win on each of its contentions.

As I previously explained, HTC filed suit in this court seeking a declaration that no claim of the '336 patent is infringed by HTC.

TPL filed a counter complaint alleging that HTC infringes the '336 patent by making, importing, using, selling, and offering for sale products that TPL argues are covered by claims 6, 7, 9, 13, 14, and 15 of the '336 patent. TPL also argues that HTC's infringement was willful. TPL also argues that HTC actively induced infringement of these claims of the '336 patent by others. TPL is seeking money damages.

Your job will be to decide whether claims 6, 7, 9, 13, 14, and 15 of the '336 patent have been infringed. If you decide that any claim of the '336 patent has been infringed, you will then need to decide any money damages to be awarded to TPL to compensate it for the infringement. You will also need to make a finding as to whether the infringement was willful. If you decide that any infringement was willful, that decision should not affect any damage award you give. I will take willfulness into account later.

Interpretation of Claims

Before you decide whether HTC has infringed the claims of the patent, you will need to understand the patent claims. As I mentioned, the patent claims are numbered sentences at the end of the patent that describe the boundaries of the patent's protection. It is my job as judge to explain to you the meaning of any language in the claims that needs interpretation.

I have interpreted the meaning of some of the language in the patent claims involved in this case. You must accept those interpretations as correct. You should disregard any conflicting interpretation. My interpretation of the language should not be taken as an indication that I have a view regarding the issue of infringement. The decision regarding infringement is yours to make. The Parties have agreed to or the court has interpreted the following terms in the claims at issue. Any terms not construed below should be interpreted according to their plain and ordinary meaning.

U.S. Patent Number 5,809,336 ("the '336 patent")

1. The term "central processing unit" means "an electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions."

2. The term "oscillator" means "[a] circuit capable of maintaining an alternating output."

3. The term "on-chip input/output interface" means "[a] circuit having logic for input/output communications, where that circuit is located on the same semiconductor substrate as the CPU."

4. The term "integrated circuit" means "[a] miniature circuit on a single semiconductor substrate."

5. The term "microprocessor" means "[a]n electronic circuit that interprets and executes programmed instructions."

6. The term "oscillator . . . clocking" means "an oscillator that generates the signal(s) used for timing the operation of the CPU."

7. The term "processing frequency" means "[t]he speed at which the CPU operates."

8. The term "varying . . . in the same way" mean "[i]ncreasing and decreasing proportionally."

9. The term "external clock is operative at a frequency independent of a clock frequency of said oscillator" means "an external clock wherein a change in the frequency of either the external clock or oscillator does not affect the frequency of the other."

10. The term "external memory bus" means "[a] group of conductors coupled between the I/O interface and an external storage device."

11. The term "Off-chip external clock" means "[a] clock not on the integrated circuit substrate."

12. The term "external clock is operative at a frequency independent of a clock frequency of said oscillator" means "[a]n external clock wherein a change in the frequency of either the external clock or oscillator does not affect the frequency of the other."

13. The term "Track" means "[i]ncreasing and decreasing proportionally."

14. The term "clocking said central processing unit" means "providing a timing signal to said central processing unit."

15. The term "wherein said central processing unit operates asynchronously to said input/output interface" means "the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them."

16. The term "ring oscillator" means "an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment."

17. The court has also found that a person of ordinary skill in the art reading the patent would understand that the phrase "as a function of" is describing a variable that depends on and varies with another, though not necessarily in an exact mathematical type functional relationship.

18. The term "entire oscillator" (in claims 6 and 13) is properly understood to exclude any external clock used to generate the signal used to clock the CPU.

Infringement

I will now instruct you on the rules you must follow in deciding whether TPL has proven that HTC has infringed one or more of the asserted claims 6, 7, 9, 13, 14, and 15 of the '336 patent. To prove infringement of any claim, TPL must persuade you that it is more likely than not that HTC has infringed that claim.

Direct Infringement

A patent's claims define what is covered by the patent. A product directly infringes a patent if it is covered by at least one claim of the patent.

Deciding whether a claim has been directly infringed is a two-step process. The first step is to decide the meaning of the patent claim. I have already made this decision, and I have already instructed you as to the meaning of the asserted patent claims. The second step is to decide whether HTC has made, used, sold, offered for sale or imported within the United States a product that is covered by a claim of the '336 patent. If it has, it infringes. You, the jury, make this decision.

With one exception, you must consider each of the asserted claims of the patent individually, and decide whether the HTC products infringe that claim. The one exception to considering claims individually concerns dependent claims. A dependent claim includes all of the requirements of a particular independent claim, plus additional requirements of its own. As a result, if you find that an independent claim is not infringed, you must also find that its dependent claims are not infringed. On the other hand, if you find that an independent claim has been infringed, you must still separately decide whether the additional requirements of its dependent claims have also been infringed.

Whether HTC knew their respective products infringed or even knew of the patent does not matter in determining direct infringement. For purposes of this case, there is one way in which a patent claim may be directly infringed: literal infringement. The following instructions will provide more detail on this type of direct infringement.

Literal Infringement

To decide whether an HTC product literally infringes a claim of the '336 patent, you must compare that product with the patent claim and determine whether every requirement of the claim is included in that product. If so, that product literally infringes that claim. If, however, that product does not have every requirement or element of the patent claim, the product does not literally infringe that claim. You must decide literal infringement for each asserted claim separately and each of the accused HTC products should be separately compared to the invention described in each patent claim they are alleged to infringe.

Unless otherwise excluded by construction of the court, if the patent claim uses the term "comprising," that patent claim is to be understood as an open claim. An open claim is infringed as long as every requirement in the claim is present in an accused HTC product. The fact that an HTC mobile phone also includes other parts will not avoid infringement, as long as it has every requirement in the patent claim.

Inducing Patent Infringement

TPL argues that HTC indirectly infringed by actively inducing another to infringe the '336 patent. In order for there to be inducement of infringement by HTC, someone else must directly infringe a claim of the '336 patent; if there is no direct infringement by anyone, there can be no induced infringement. In order to be liable for inducement of infringement, HTC must:

(1) have intentionally taken action that actually induced direct infringement by another;

(2) have been aware of the '336 patent; and

(3) have known that the acts it was causing would be infringing.

If HTC did not know of the existence of the patent or that the acts it was inducing were infringing, it cannot be liable for inducement unless it actually believed that it was highly probable its actions would encourage infringement of a patent and it took intentional acts to avoid learning the truth. It is not enough that HTC was merely indifferent to the possibility that it might encourage infringement of a patent. Nor is it enough that HTC took a risk that was substantial and unjustified.

If you find that HTC was aware of the patent, but believed that the acts it encouraged did not infringe that patent, or that the patent was invalid, HTC cannot be liable for inducement.

Willful Infringement

In this case, TPL argues that HTC willfully infringed TPL's patent.

To prove willful infringement, TPL must first persuade you that HTC infringed a valid claim of TPL's patent. The requirements for proving such infringement were discussed in my prior instructions. In addition, to prove willful infringement, TPL must persuade you that it is highly probable that prior to the filing of the complaint on February 8, 2008, HTC acted with reckless disregard of the claims of TPL's patent.

To demonstrate such "reckless disregard," TPL must satisfy a two-part test. The first part of the test is objective. TPL must persuade you that HTC acted despite an objectively high likelihood that its actions constituted infringement of a valid patent. The state of mind of HTC is not relevant to this inquiry. Rather, the appropriate inquiry is whether the defenses put forth by HTC fail to raise any substantial question with regard to infringement or validity. Only if you conclude that the defenses fail to raise any substantial question with regard to infringement or validity, do you need to consider the second part of the test.

The second part of the test does depend on the state of mind of HTC. TPL must persuade you that HTC actually knew, or it was so obvious that HTC should have known, that its actions constituted infringement of a valid patent.

In deciding whether HTC acted with reckless disregard for TPL's patent, you should consider all of the facts surrounding the alleged infringement including, but not limited to, the following factors:

(1) Whether HTC acted in a manner consistent with the standards of commerce for its industry;

(2) Whether HTC intentionally copied a product of TPL covered by the patent;

(3) Whether or not HTC made a good-faith effort to avoid infringe the ’336 patent, for example, whether HTC attempted to design around the ’336 patent;

(4) Whether or not HTC tried to cover up its infringement;

(5) Whether or not there is a reasonable basis to believe that HTC did not infringe or had a reasonable defense to infringement.

Burden of Proof

I will instruct you about the measure of damages. By instructing you on damages, I am not suggesting which party should win on any issue. If you find that HTC infringed any valid claim of the '336 patent, you must then determine the amount of money damages to be awarded to TPL to compensate it for the infringement.

The amount of those damages must be adequate to compensate TPL for the infringement. A damages award should put the patent holder in approximately the financial position it would have been in had the infringement not occurred, but in no event may the damages award be less than a reasonable royalty. You should keep in mind that the damages you award are meant to compensate the patent holder and not to punish an infringer.

TPL has the burden to persuade you of the amount of its damages. You should award only those damages that TPL more likely than not suffered. While TPL is not required to prove their damages with mathematical precision, they must prove them with reasonable certainty. TPL is not entitled to damages that are remote or speculative.

Reasonable Royalty

If you determine that any products sold by HTC infringed any valid claims of the '336 patent, then TPL should be awarded a reasonable royalty for all sales associated with each such product infringing a particular patent.

Reasonable Royalty – Definition

A royalty is a payment made to a patent holder in exchange for the right to make, use or sell the claimed invention. This right is called a "license." A reasonable royalty is the payment for the license that would have resulted from a hypothetical negotiation between the patent holder and the infringer taking place at the time when the infringing activity first began. In considering the nature of this negotiation, you must assume that the patent holder and the infringer would have acted reasonably and would have entered into a license agreement. You must also assume that both parties believed the patent was valid and infringed. Your role is to determine what the result of that negotiation would have been. The test for damages is what royalty would have resulted from the hypothetical negotiation and not simply what either party would have preferred.

One way to calculate a royalty is to determine a one-time lump sum payment that the infringer would have paid at the time of the hypothetical negotiation for a license covering all sales of the licensed product both past and future. This differs from payment of an ongoing royalty because, with an ongoing royalty, the licensee pays based on the revenue of actual licensed products it sells. When a one-time lump sum is paid, the infringer pays a single price for a license covering both past and future infringing sales.

It is up to you, based on the evidence, to decide what royalty is appropriate in this case.

Reasonable Royalty – Relevant Factors

In determining the outcome of the hypothetical negotiation, you should consider all facts known to the parties at the time infringement began. Some of the factors you may consider are:

(1) Royalties received by the patent holder for licensing the patent-in-suit, proving or tending to prove an established royalty.

(2) Rates the infringer paid for using other patents comparable to the patent-in-suit.

(3) The nature of the license, i.e., exclusive or nonexclusive, restricted or unrestricted in terms of territory or to whom products covered by the patent claim may be sold.

(4) The patent holder's policy to maintain its patent monopoly by not licensing others or by granting licenses under special conditions designed to preserve its monopoly.

(5) The commercial relationship between the patent holder and infringer, such as whether they are competitors in the same territory in the same line of business.

(6) The effect of selling the patented invention in promoting sales of other products of the infringer, the existing value of the patented invention to the patent holder as a generator of sales of non-patented items, and the extent of such derivative or convoyed sales.

(7) The duration of the patent and the term of the license.

(8) The established profitability of products covered by the patent claim, their commercial success, and their current popularity.

(9) The advantages and benefits of the patented invention over older modes or devices, if any, that had been used to work on similar problems.

(10) The nature of the patented invention, the character of the patent holders' products covered by it, and the benefits to those who have used the invention.

(11) The extent to which the infringer has made use of the patented invention and any evidence probative of the value of that use.

(12) The portion of the profit or selling price that was customary in the business or in comparable businesses allow for the use of the invention or analogous inventions.

(13) The portion of the realizable profits that should be credited to the patented invention as distinguished from non-patented elements, the manufacturing process, business risks, or significant features or improvements added by the infringer.

(14) The opinion and testimony of qualified experts.

(15) The amount that a prudent licensor (such as the patent holder) and a prudent licensee (such as the infringer) would have agreed upon at the time infringement began if both had been reasonably and voluntarily trying to reach an agreement.

No one factor is dispositive, and you should consider the evidence that has been presented to you in this case on each one of the factors. You may also consider any other factors which in your mind would have increased or decreased the royalty the infringer would have been willing to pay and the patent holder would have been willing to accept, acting as normally prudent business people. The final factor establishes the framework which you should use in determining a reasonable royalty, that is, the payment that would have resulted from a negotiation between the patent holder and the infringer taking place at a time when infringement began.

Date of Commencement

Damages that TPL may be awarded by you commence on the date that HTC infringed the '336 patent.

Calculating Damages in Cases of Inducement

In order to recover damages for induced infringement, TPL must either prove that the accused devices necessarily infringe the '336 patent or prove acts of direct infringement by others that were induced by HTC. Because the amount of damages for induced infringement is limited by the number of instances of direct infringement, TPL must further prove the number of direct acts of infringement of the '336 patent—for example, by showing individual acts of direct infringement or by showing that a particular type of HTC products or uses directly infringes.

Patent Term Glossary

A number of terms are defined below for your information and convenience.

Abstract: A brief summary of the technical disclosure in a patent to enable the U.S. Patent and Trademark Office and the public to determine quickly the nature and gist of the technical disclosure in the patent.

Assignment: A transfer of patent rights to another called an "assignee" who upon transfer becomes the owner of the rights assigned.

Claim: Each claim of a patent is a concise, formal definition of an invention and appears at the end of the specification in a separately numbered paragraph. In concept, a patent claim marks the boundaries of the patent in the same way that a legal description in a deed specifies the boundaries of land, i.e. similar to a land owner who can prevent others from trespassing on the bounded property, the inventor can prevent others from using what is claimed. Claims may be independent or dependent. An independent claim stands alone. A dependent claim does not stand alone and refers to one or more other claims. A dependent claim incorporates whatever the other referenced claim or claims say.

Drawings: The drawings are visual representations of the claimed invention contained in a patent application and issued patent, and usually include several figures illustrating various aspects of the claimed invention.

Elements: The required parts of a device or the required steps of a method. A device or method infringes a patent if it contains each and every requirement of a patent claim.

Embodiment: A product or method that contains the claimed invention.

Examination: Procedure before the U.S. Patent and Trademark Office whereby a Patent Examiner reviews the filed patent application to determine if the claimed invention is patentable.

Filing Date: Date a patent application, with all the required sections, has been submitted to the U.S. Patent and Trademark Office.

Infringement: Violation of a patent occurring when someone makes, uses or sells a patented invention without permission of the patent holder, within the United States during the term of the patent. Direct infringement is making, using or selling the patented invention without permission.

Limitation: A required part of an invention set forth in a patent claim. A limitation is a requirement of the invention. The word "limitation" is often used interchangeably with the word "requirement."

Office Action: A written communication from the Patent Examiner to the patent applicant in the course of the application examination process.

Patent: A patent is an exclusive right granted by the U.S. Patent and Trademark Office to an inventor to prevent others from making, using, offering to sell, or selling an invention within the United States, or from importing it into the United States, during the term of the patent. When the patent expires, the right to make, use or sell the invention is dedicated to the public. The patent has three parts, which are a specification, drawings, and claims. The patent is granted after examination by the U.S. Patent and Trademark Office of a patent application filed by the inventor which has these parts, and this examination is called the prosecution history.

Patent and Trademark Office (PTO): An administrative branch of the U.S. Department of Commerce that is charged with overseeing and implementing the federal laws of patents and

trademarks. It is responsible for examining all patent applications and issuing all patents in the United States.

Prior Art: Previously known subject matter in the field of a claimed invention for which a patent is being sought. It includes issued patents, publications, and knowledge deemed to be publicly available such as trade skills, trade practices and the like.

Prosecution History: The prosecution history is the complete written record of the proceedings in the PTO from its initial application to the issued patent. The prosecution history includes the office actions taken by the PTO and the amendments to the patent application filed by the applicant during the examination process.

Reads On: A patent claim "reads on" a device or method when each required part (requirement) of the claim is found in the device or method.

Requirement: A required part or step of an invention set forth in a patent claim. The word "requirement" is often used interchangeably with the word "limitation."

Royalty: A royalty is a payment made to the owner of a patent by anon-owner in exchange or rights to make, use or sell the claimed invention.

Specification (Patent): The specification is a required part of a patent application and an issued patent. It is a written description of the invention and of the manner and process of making and using the claimed invention.

Addendum

A number of the HTC products accused of infringement in this case contain Qualcomm chips. The parties have agreed and HTC has verified that the HTC Phones listed in the table in Exhibit A contain the Qualcomm chips next to them. The parties have also agreed, and Qualcomm has verified, the following facts about the Qualcomm chips listed in Exhibit A:

1. The Qualcomm chips shown in Exhibit A contain the application processors shown in Exhibit A;

2. Each of the Qualcomm chips listed in Exhibit A includes phase locked loops (PLLs) at least one of which is associated with clocking the corresponding application processor;

3. Each of the PLLs in paragraph 2 contains a voltage controlled oscillator or a current controlled oscillator that has a multiple, odd number of inversions arranged in a loop.

4. The terms “application processor,” “clocking,” “voltage controlled oscillator” and “current controlled oscillator” used above come from Qualcomm technical documents produced in this case.

EXHIBIT A

HTC Phones with Qualcomm Chips

HTC Phone(s)	Qualcomm Chip	Application Processor
Mobile Phone Tilt / TyTN II [Kaiser]	MSM7200	ARM 11
HTC Touch Dual [Neon]	MSM7200	ARM 11
Touch Phone P3650 [Polaris]	MSM7200	ARM 11
Mobile Phone S730	MSM7200	ARM 11
HTC Touch Diamond [Diamond]	MSM7201	ARM 11
HTC T-Mobile G1 [Dream]	MSM7201	ARM 11
HTC Touch Phone Fuze [Raphael]	MSM7201	ARM 11
HTC Smartphone Wildfire [Bee]	MSM7625	ARM 11
HTC Shift X9000 [Atlantis]	MSM7500	ARM 11
HTC Smartphone S640 [Iris]	MSM7500	ARM 11
HTC S720 / SMT5800 [Libra]	MSM7500	ARM 11
Mobile Phone XV6800 / HTC PDA Phone P4000 / PPC-6800 [Mogul, Titan]	MSM7500	ARM 11
Touch Phone P3450	MSM7500	ARM 11
HTC Smartphone EVO Shift 4G [Speedy]	MSM7x30	Scorpion
HTC Smartphone G2 [Vision]	MSM7x30	Scorpion
HTC Smartphone Inspire 4G [Ace]	MSM7x30 / MSM8255	Scorpion
HTC Smartphone myTouch 4G [Glacier]	MSM7x30 / MSM8255	Scorpion
HTC Smartphone ThunderBolt	MSM7x30 / MSM8655	Scorpion
HTC Smartphone Desire [Bravo]	QSD8x50	Scorpion
HTC Smartphone Surround [Mondrian]	QSD8x50	Scorpion
HTC Smartphone HD7 [Schubert]	QSD8x50	Scorpion
HTC Smartphone EVO 4G [Supersonic]	QSD8x50	Scorpion

IT IS SO ORDERED.

Dated: September 30, 2013

PAUL S. GREWAL
United States Magistrate Judge

Date Filed	#	Docket Text
10/02/2013	651	**ORDER DENYING 647 MOTION FOR JUDGMENT AS A MATTER OF LAW entered by Magistrate Judge Paul Singh Grewal. (This is a text-only entry generated by the court. There is no document associated with this entry.) (Entered: 10/02/2013)**

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, et al.,

Defendants.

Case No.: 5:08-cv-00882-PSG

FINAL VERDICT FORM

(Re: Docket No. 524)

VERDICT FORM

When answering the following questions and filling out this Verdict Form, please follow the directions provided throughout the form. Your answer to each question must be unanimous. Some of the questions contain legal terms that are defined and explained in detail in the Jury Instructions. Please refer to the Jury Instructions if you are unsure about the meaning or usage of any legal term that appears in the questions below.

We, the jury, unanimously agree to the answers to the following questions and return them under the instructions of this court as our verdict in this case.

I. U.S. Patent No. 5,809,336 ("the '336 patent")

A. Infringement

1. Literal Infringement

1. Do you find that TPL has proven by a preponderance of the evidence that HTC has literally infringed any of the following claims of the '336 patent?

You can only find claims 7 or 9 infringed if you previously found claim 6 infringed. You can only find claims 14 or 15 infringed if you previously found claim 13 infringed.

Claim	Yes (for TPL)	No (for HTC)
6	☑	☐
7	☑	☐
9	☑	☐
13	☑	☐
14	☑	☐
15	☑	☐

2. Inducement

2. Do you find that TPL has proven by a preponderance of the evidence for each of the claims below that HTC:

a. intentionally took an action that actually induced direct infringement of the '336 patent by a third party;

b. was aware of the '336 patent; and

c. knew that the actions, if taken, would cause infringement of the '336 patent?

You can only find claims 7 or 9 infringed if you previously found claim 6 infringed. You can only find claims 14 or 15 infringed if you previously found claim 13 infringed.

Claim	Yes (for TPL)	No (for HTC)
6	☐	☑
7	☐	☑
9	☐	☑
13	☐	☑
14	☐	☑
15	☐	☑

II. Damages

If you have found that HTC has not infringed any claim of the '336 patent please skip Question 3. Only answer Question 3 if you have found that HTC has infringed at least one claim of the '336 patent.

3. To the extent you have found that at least one claim of the '336 patent is infringed, what has TPL proven that it is entitled to as a reasonable royalty for infringement:

One-time (lump sum) payment of $ 958,560 for the life of the patent.

III. Willfulness

4. If you have found that HTC has infringed at least one claim of the '336 patent, has TPL proven that it is highly probable that HTC's infringement was willful?

Yes (for TPL)	No (for HTC)
☐	☑

The foreperson must sign and date this verdict form.

Signed: _____ Date: 10/03/2013

Foreperson

IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

HTC CORPORATION, et al.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, et al.,

Defendants.
_____/

No. CV08-00882 PSG

JUDGMENT IN A CIVIL CASE

(X**) Jury Verdict.** This action came before the court for a trial by jury. The issues have been tried and the jury has rendered its verdict.

() Decision by Court. This action came to trial or hearing before the court. The issues have been tried or heard and a decision has been rendered.

IT IS SO ORDERED AND ADJUDGED that pursuant to the jury verdict filed October 3, 2013, judgment is entered in favor of Defendants.

Dated: October 3, 2013

Richard W. Wieking, Clerk

By: Oscar Rivera
Deputy Clerk

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, et al., Defendants.	Case No. 5:08-cv-00882-PSG **ORDER DENYING PLAINTIFFS' RENEWED MOTION FOR ENTRY OF JUDGMENT AS A MATTER OF LAW** **(Re: Docket No. 671)**

In this patent infringement suit, a jury found that the Plaintiffs in this action, HTC Corporation and HTC America, Inc. infringed a lone patent owned by Defendants Technology Properties Limited, Patriot Scientific Corporation, and Alliacense Limited (collectively, "TPL"). HTC now renews its motion for judgment as a matter of law pursuant to Fed. R. Civ. P. 50(b), arguing that no reasonable jury could have found that HTC infringes any asserted claim of U.S. Patent No. 5,809,336 ("the '336 patent). TPL opposes. The parties appeared for a hearing. After considering their oral arguments and those in the papers, the court DENIES HTC's motion.

I. BACKGROUND

Technology Properties Limited and Alliacense, Limited are California corporations with their principal place of business in Cupertino, California; Patriot Scientific Corporation is a Delaware corporation with its principal place of business in Carlsbad, California. These defendants – Technology Properties Limited, Alliacense, and Patriot (collectively "TPL") – claim ownership of a family of related microprocessor patents. TPL refers to those patents as the Moore Microprocessor Portfolio patents ("MMP patents"), in recognition of co-inventor Charles Moore's contributions.

A. The Long, Winding Road To Trial

HTC filed this suit on February 8, 2008, seeking a judicial declaration that four of the MMP patents – U.S. Patent Nos. 5,809,336 ("the '336 patent"), 5,784,584 ("the '584 patent"), 5,440,749 ("the '749 patent"), and 6,598,148 ("the '148 patent") – are invalid and/or not infringed.[1] TPL counterclaimed for infringement of the '336, '749, '148, and '890 patents on November 21, 2008.[2] On April 25, 2008, TPL filed two complaints in the Eastern District of Texas against HTC alleging infringement of the four patents at issue in the pending declaratory judgment action.[3] On June 4, 2008, TPL filed additional patent infringement actions against HTC in the Eastern District of Texas asserting U.S. Patent No. 5,530,890 ("the '890 patent").[4] On July 10, 2008, HTC amended its complaint before this court, adding claims for declaratory relief with respect to the '890 patent.[5] On February 23, 2009 the parallel Texas litigation was dismissed without prejudice following Judge Fogel's decision to deny TPL's Motion to Dismiss, or in the Alternative, to

[1] *See* Docket No. 1.

[2] *See* Docket No. 60 at 6-8.

[3] *See* Docket No. 16 at 3.

[4] *See* Docket No. 35 at 5.

[5] *See* Docket No. 34.

Transfer Venue in the California action.[6] On March 25, 2010, the court accepted the parties' stipulation to dismiss the '584 patent from this litigation.[7] On August 24, 2012, Technology Properties Limited, Patriot, and Phoenix Digital Solutions initiated an International Trade Commission investigation regarding HTC's alleged infringement of the '336 patent.[8] On July 17, 2013, the court accepted the parties' stipulation to dismiss the '148 and '749 patents from this litigation.[9] On September 19, 2013, the court accepted the parties stipulation to dismiss all claims relating to the '890 patent from this litigation.[10]

In sum, only the '336 patent was considered by the jury at trial.

B. The '336 Patent

The '336 patent issued on September 15, 1998, and describes a microprocessor with an internal variable speed clock, or oscillator, that drives the processor's central processing unit ("CPU").[11] Traditional microprocessors use external, fixed speed crystals to clock the CPU.[12] A CPU's maximum possible processing capacity depends on process, voltage, and temperature

[6] *See* Docket Nos. 49 (denying motion to dismiss, to transfer venue, and to stay) and 88 (granting motion for leave to file motion for reconsideration and denying motion for reconsideration).

[7] *See* Docket No. 152.

[8] *See* Docket No. 561-1. Claims 1, 6, 7, 9-11, and 13-16 were asserted in the investigation. On September 6, 2013, Administrative Law Judge James Gildea issued an Initial Determination from in the ITC proceeding holding that HTC did not violate Section 337 of the Tariff Act of 1930. *See id.*

[9] *See* Docket No. 462.

[10] *See* Docket No. 594.

[11] *See* Docket No. 393-3 at 1 ("A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a Central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor.").

[12] *See id.* at 17:12-14 ("Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations.").

("PVT parameters").[13] An external clock must therefore set the timing of the CPU to suboptimal PVT conditions, resulting in waste of the CPU's processing speed under optimal conditions. The internal, variable clock described in the '336 patent claims real-time adjustment of the timing of the CPU by placing the clock on the chip itself. Thus, the CPU can perform optimally under any set of parameters.[14] The microprocessor nevertheless requires a second external clock because devices other than the CPU do not operate at variable speed.[15]

Independent claim 6 provides:

A microprocessor system comprising:

> a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;
>
> an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

---

[13] *See id.* at 17:21-22 ("Speed may vary by a factor of four depending upon temperature, voltage, and process.").

[14] *See id.* at 17:32-34 ("By decoupling the variable speed of the CPU 70 from the fixed speed of the I/O interface 432, optimum performance can be achieved by each.").

[15] *See id.* at 44-53 ("The designer of a high speed microprocessor must produce a product which operate over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing. Temperature, voltage, and process all affect transistor propagation delays. Traditional CPU designs are done so that with the worse case of the three parameters, the circuit will function at the rated clock speed. The result are designs that must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse case conditions."); *id.* at 16:67-17:10 ("By deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast. For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor 50 will operate slower than normal. Since the microprocessor 50 ring oscillator clock 430 is made from the same transistors on the same die as the latches and gates, it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.").

an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.[16]

C. The Verdict: HTC Infringes

A seven-day jury trial was held to consider whether HTC infringed the '336 patent.[17] At trial, HTC did not contest the validity of the '336 patent. HTC moved for judgment as a matter of law after the close of TPL's case.[18] After two days of deliberations, the jury found that HTC and its accused products literally infringed all asserted claims: 6, 7, 9, 13, 14, and 15.[19] As to damages, the jury made the following findings:

> 3. To the extent you have found that at least one claim of the '336 patent is infringed, what has TPL proven that it is entitled to as a reasonable royalty for infringement:
>
> One-time (lump sum) payment of $958,560 for the life of the patent.[20]

Following the jury verdict HTC filed a renewed motion for judgment as a matter of law that its products do not infringe the '336 patent.[21]

II. LEGAL STANDARDS

Fed. R. Civ. P. 50(b) provides that, upon a renewed motion for judgment as a matter of law, the court may: (1) "allow judgment on the verdict, if the jury returned a verdict," (2) "order a new trial," or (3) "direct the entry of judgment as a matter of law." To grant a Rule 50(b) motion, the court must determine that "the evidence, construed in the light most favorable to the non-moving

---

[16] Docket No. 393-3.

[17] *See* Docket No. 657.

[18] *See* Docket No. 647. HTC also moved for judgment as a matter of law as to willful infringement and damages. The jury returned a verdict that HTC's infringement was not willful. HTC has not renewed its motion for judgment as a matter of law on the issue of damages. *See* Docket No. 654 at 3-4.

[19] *See* Docket No. 654 at 2.

[20] *Id.* at 4.

[21] *See* Docket 671.

party, permits only one reasonable conclusion, and that conclusion is contrary to the jury's."[22] In other words, to set aside the verdict, there must be an absence of "substantial evidence" – meaning "relevant evidence that a reasonable mind would accept as adequate to support a conclusion" – to support the jury's verdict.[23] "Substantial evidence is more than a mere" scintilla;[24] it constitutes "such relevant evidence as reasonable minds might accept as adequate to support a conclusion even if it is possible to draw two inconsistent conclusions from the evidence."[25] In reviewing a motion for judgment as a matter of law, the court "must view the evidence in the light most favorable to the non-moving party and draw all reasonable inferences in its favor."[26] "In ruling on such a motion, the trial court may not weigh the evidence or assess the credibility of witnesses in determining whether substantial evidence exists to support the verdict."[27]

III. DISCUSSION

A. The Jury Considered Substantial Evidence that the Accused Products Involve An "Entire Oscillator"

HTC first disputes the sufficiency of evidence regarding practice of the "entire oscillator" limitation. The court addressed the term in its order granting-in-part summary judgment of

[22] *Callicrate v. Wadsworth Mfg.*, 427 F.3d 1361, 1366 (Fed. Cir. 2005) (*quoting Pavao v. Pagay*, 307 F.3d 915, 918 (9th Cir. 2002)) ("The Ninth Circuit upholds any jury verdict supported by substantial evidence.").

[23] *Id.*

[24] *Chisholm Bris. Farm Equip. Co. v. Int'l Harvester Co.*, 498 F.2d 1137, 1140 (9th Cir. 1974) (*quoting Consol. Edison Co. v. NLRB*, 305 U.S. 197, 229 (1938)).

[25] *Landes Constr. Co. v. Royal Bank of Canada*, 833 F.2d 1365, 1371 (9th Cir. 1987).

[26] *Transbay Auto Serv., Inc. v. Chevron U.S.A., Inc.*, Case No. 3:09-cv-04932 SI, 2013 WL 496098, at *2 (N.D. Cal. Feb. 7, 2013) (*quoting Josephs v. Pacific Bell*, 443 F.3d 1050, 1062 (9th Cir. 2006) ("We must view the evidence in the light most favorable to the nonmoving party – here, Josephs, – and draw all reasonable inferences in that party's favor.")).

[27] *Id.* (citing *Mosesian v. Peat, Marwick, Mitchell & Co.*, 727 F.2d 873, 877 (9th Cir. 1984) ("Neither the district court nor this court may weigh the evidence or order a result it finds more reasonable if substantial evidence supports the jury verdict.")).

non-infringement and no willfulness.[28] The court explained:

> The court agrees with HTC that the disputed limitations are properly understood to exclude any external clock used to generate a signal.[29] Nevertheless, there remains a factual dispute whether HTC's products contain an on-chip ring oscillator that is self-generating and does not rely on an input control to determine its frequency. While HTC's expert says that the PLLs generate the clock, TPL's expert counters that the ring oscillators generate the clock and the PLLs merely buffer or fix the frequency.[30] This is a classic factual question that requires a trial to answer.[31]

HTC argues that the record at trial was uncontroverted that the ring oscillator in all accused HTC products is a phase locked loop ("PLL") and that the frequency output from the PLL is used to clock the CPU in the accused products. In particular, the frequency generated by that PLL relies on an off-chip crystal to set the frequency which is used to clock the CPU. The court's construction teaches that if an off chip crystal is used to clock the CPU, then the accused products fall outside of the claims. Because this was the factual predicate under which the trial was held and all of the evidence at trial demonstrates the PLLs in the accused products necessarily reference an off-chip signal in order to set the frequency to clock the CPU, no reasonable jury could find infringement. At bottom, the evidence was undisputed that the signal that is used to clock the CPU cannot exist but for the existence of the off chip crystal's input – there is nothing to clock the CPU if the off chip crystal is not referenced.

---

[28] *See* Docket No. 585.

[29] The patentee's arguments traversing the prior art narrowed the claims. *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722, 740 (2002) ("A patentee's decision to narrow his claims through amendment may be presumed to be a general disclaimer of the territory between the original claim and the amended claim."); *cf. Saeilo Inc. v. Colt's Mfg. Co.*, 26 F. App'x 966, 973 (Fed. Cir. 2002) ("Where an amendment narrows the scope of a claim for a reason related to the statutory requirements for patentability, prosecution history estoppel acts as a complete bar to the application of the doctrine of equivalents to the amended claim element.").

[30] *Compare* Docket No. 457 at 16 ("the oscillators in the accused products indisputably rely on an external crystal or clock generator to clock" the CPU), *with* Docket No. 470 at 14 ("Each HTC product includes a CPU/system clock – a ***ring oscillator*** within a PLL – that ***generates*** a clock signal ***on its own***, as long as it has a power supply.") (emphasis in original).

[31] Docket No. 585 at 11.

TPL counters that HTC failed to preserve the issue, and that in any event there was sufficient evidence that even if the external crystal can be used to regulate frequency clocking the CPU that is separate and distinct from the generation of the clock. TPL points to testimony from its expert, Dr. Oklobdzija, that because one could remove the crystal and still see a signal, even though that was not how the accused products operate, that suggested to him, an expert in the field, that the crystal was not being used to generate the signal.[32] Oklobdzija also opined that no off-chip crystal is relied upon to generate a clock signal.[33] Even HTC's own expert opined that the external crystal clocks were used in HTC phones as reference signals, not to actually generate the on-chip clock signal itself.[34]

As an initial matter, the court is satisfied that HTC's arguments regarding the meaning of "entire oscillator" were preserved. After the court issued its order denying HTC's motion for summary judgment of non-infringement, HTC filed a motion requesting that the court adopt a jury instruction incorporating a construction of "entire oscillator" consistent with the order. In particular, HTC asked the court to adopt a construction that included two sentences: (1) a first sentence stating that the limitation is "not satisfied by an accused system that uses any external clock to generate a signal," and (2) a second sentence specifying, among other things, that an accused product can infringe only if it "does not rely on an input control to determine its frequency."[35] The court held a hearing on HTC's motion and issued an order adopting a

[32] *See* Docket No. 641, Trial Tr. at 565:15-19 ("The ring oscillator generates the clock regardless, and it will continue to generate the clock even when you disconnect this, the crystal.").

[33] *See id.*, Trial Tr. at 565:22-25 ("Q: Does any on-chip component rely on the off-chip crystal to generate a clock signal? A: No.").

[34] *See* Docket No. 643, Trial Tr. at 1019:23-1020:3 ("Q: And have you heard of the term "Crystal Clock," or "Crystal Oscillator"? A: Yeah. Crystal Oscillator is a component that you put a voltage on the component and then it starts oscillating at a fixed frequency. It's also part of a PLL. It feeds a PLL and makes sure that the PLL has a reference signal.").

[35] Docket No. 590 at 2:19-23; *see also* Docket No. 604 (citing the intrinsic record).

construction of "entire oscillator" based on a modified version of the first sentence of HTC's proposal. The court chose not to adopt the second sentence of HTC's proposal and informed the parties that it would instruct the jury in accordance with its construction.[36]

HTC raised this issue again with the court on the day before closing arguments in the context of jury instructions on the construction of "entire oscillator." During the jury instruction conference with the court, after taking up the jury instruction on claim construction, counsel for HTC asked the court to confirm that HTC's earlier objections and arguments with respect to its proposed two-sentence construction of "entire oscillator" had been preserved for the record. The court confirmed that they were.

> Mr. Weinstein:
>
> I just want to make sure, we understand you -- we had extensive argument about the entire oscillator term. We had a hearing prior to the trial and I just wanted to make sure that the objections that we had regarding the two sentences that we wanted are still preserved.
>
> The court:
>
> They are preserved, absolutely.[37]

Second, HTC's pre-verdict JMOL motion fully raised the argument that the accused HTC products do not infringe because the oscillator in the accused HTC products relies on an input control to determine its frequency.[38] HTC's pre-verdict motion specifically argued, for example, that the "entire oscillator" limitation was not satisfied because "the output frequency of the on-chip clock is expressly calculated, in each instance, based on the input frequency provided by the external clock."[39] HTC's motion explained in detail how the frequency of the on-chip oscillator

---

[36] *See* Docket No. 607 at 1.

[37] Docket No. 695-2, Ex. 16 at 1456:16-21.

[38] *See* Docket No. 647 at 4-6.

[39] *Id.* at 6.

was based on a formula that expressly relies on the frequency input from the external clock, including specific citations to the evidentiary record at trial.[40]

This was sufficient.[41]

As for the merits of the dispute, Oklobdzija took the stand and offered expert testimony that, after considering the accused products, his opinion was that the CPU was clocked by an on-chip crystal. He emphasized that a ring oscillator in an HTC accused product does not use an external crystal/clock to generate a clock signal used by the CPU. In particular, he repeatedly clarified that a ring oscillator generates a clock signal on its own, without relying on external crystals.[42] HTC's technical expert, Mr. Gafford, also admitted that it is the ring oscillator that generates the clock signal for the CPU.[43] Gafford further admits that the external crystal is not used to generate the signal. Rather, its clock is used only to compare with the phase of the ring oscillator's already generated clock signal that has been steeply divided by the frequency divider.[44] As Oklobdzija explained, the ring oscillator generates a very high frequency clock signal on its

---

[40] *See id.* at 4-6.

[41] *See C.B. v. City of Sonora*, 730 F.3d 816, 824 n.5 (9th Cir. 2013) (citing *EEOC v. Go Daddy Software, Inc.*, 581 F.3d 951, 961 (9th Cir. 2009)) (In the Ninth Circuit, "Rule 50(b) 'may be satisfied by an ambiguous or inartfully made motion under Rule 50(a),' and it is given a 'liberal interpretation' to avoid overly harsh results."); *W. Union Co. v. MoneyGram Payment Sys., Inc.*, 626 F.3d 1361, 1367 (Fed. Cir. 2010) (*quoting Blackboard, Inc. v. Desire2Learn, Inc.*, 574 F.3d 1371, 1379-80 (Fed. Cir. 2009) (holding that even "a cursory motion suffices to preserve an issue on JMOL so long as it 'serves the purposes of Rule 50(a), i.e., to alert the court to the party's legal position and to put the opposing party on notice of the moving party's position as to the insufficiency of the evidence.'").

[42] *See* Docket No. 641, Trial Tr. at 565:15-19 ("The ring oscillator generates the clock regardless, and it will continue to generate the clock even when you disconnect this, this crystal."); Trial Tr. 565:22-25 ("Q: Does any on-chip component rely on the off-chip crystal to generate a clock signal? A: No.").

[43] *See* Docket No. 684, Trial Tr. at 1364:18-22 ("Q: So you've got a 2.0 gigahertz clock signal generated by the ring oscillator that's clocking the CPU, and you divide by 100, and that's what this circuitry actually does; correct? A: Yes.").

[44] *See id.*, Trial Tr. at 1364:18-1365:1 ("Q: [The 2.0-gigahertz clock signal generated by the ring oscillator is divided by 100] [t]o get a 20 megahertz signal so that you can do edge matching with the external reference crystal signal in the phase detector, correct? A: Yes.").

own, which must then be divided to obtain a lower frequency so that its phase can be compared to the phase of the external reference.[45] After that, the PLL can make adjustments to the analog voltage/current provided to the ring oscillator to regulate – but not to generate – its frequency.[46]

Even if Oklobdzija's positions were later undermined by other evidence to a degree or diminished through cross-examination, his expert testimony as corroborated by other experts provides sufficient substantial evidence as required under Rule 50(b).

B. The Jury Considered Substantial Evidence of Variation of the Processing Frequency and Entire Oscillator as a Function of PVT

HTC next argues that no reasonable jury could have found infringement because TPL did not provide substantial evidence that the processing frequency of the CPU and entire oscillator "varied as a function of process, voltage, or temperature." In support, HTC claims the accused products "are designed to maintain the target frequency across PVT variations."[47] What's more, none "of the formulae for any Qualcomm, TI or Samsung chip recites any fabrication or operational parameter variation as playing any role in the determination of the PLL output

[45] *See* Docket No. 641, Trial Tr. at 569:2-18 ("Q: Where is the digital to analog converter here? A: It says DAC. DAC means digital to analog converter, the component here (indicating). So this output operation to extend the digital signal to DAC, this DAC just makes the plain voltage out (indicating), this voltage which comes from here (indicating), and produces this voltage which will smoothly move this one in the range we want it to oscillate (indicating). Now, let me go back just one second. This is a divider (indicating), and this is a comparator (indicating). This is what is called a phase detector (indicating). Here is the reference (indicating). This reference is compared with the divided signal here, and what it does is, you can see the switches, it either moves this voltage up or down. These capacitors have been charged and they filter that voltage so it's not jumping up and down, so it's smooth, that voltage, okay, when connected.").

[46] *See id.* at 569:19-22 ("And in this case this is disconnected, but when connected, it's converted into a current some with what digital PLL does, or digital output, same thing, voltage, and it will adjust this VCO, voltage control oscillator, ring oscillator.").

[47] Docket No. 643, Trial Tr. at 1062:2-3 ("Regarding PLL's, I can tell you that PLL's are designed to maintain the target frequency across PVT variations."); Docket No. 640, Trial Tr. at 359:2-8 ("Q: Is the output frequency from the DPLL stable? A: That is part of the specification. In other words, the outer clock is always known to have a known value within a tight range. That's how the specification on the PLL is developed. So yes, the answer is correct, it's stable, it's a known value.").

frequency. The accused HTC products, therefore, do not meet the "varying" limitations as a matter of law."[48]

Again, the court finds substantial evidence supports the jury's verdict. Gafford, HTC's expert, testified that the processing frequency of the CPU and the clock rate of the on-chip oscillator must always vary in the same way.[49] Because the claim limitation is disjunctive, TPL needed to show only that such variation is a function of at least one parameter among the several fabrication or operational parameters (e.g., voltage and temperature). With respect to at least the process / fabrication parameters, TPL met its burden. Process parameters vary from chip to chip because, as Gafford testified, process parameters are the same for components of the same chip, such as the CPU and the on-chip oscillator in each HTC accused product.[50] Gafford also admitted that such process variation between chips results in variation between chips in processing frequency and the associated clock rate.[51]

---

[48] Docket No. 671 at 8.

[49] *See* Docket No. 684, Trial Tr. at 1387:13-1388:1 ("Q: Let me ask you this: the processing frequency of the CPU and the clock rate of the entire oscillator must always vary together; right? A: Yes, they must vary in the same way. Q: They all – they must always vary in the same way, and the reason is that the CPU gets its processing frequency from the clock rate of the entire oscillator; right? A: I believe that's the way—I believe that's how everyone has agreed we're interpreting this element. Q: Okay. Like Dr. Oklobdzija's analogy, if I'm the entire oscillator and you're the CPU and we're shaking hands and I'm moving my hand at two hertz, your hand is also moving at two hertz; correct?

[50] *See id.*, Trial Tr. at 1394:8-11 ("Q: Now, Variations in fabrication parameters, again, are from chip to chip. They're not in the same chip during operation; right? A: Yes."); Trial Tr. at 1393:16-23 ("Q: Now, you also recognized that there have to be process variations among the chips in the HTC accused products; right? A: Yes. Q: Because process variation is endemic to silicon production; correct? A: Yes. Q: You can't get away from it; right? A: Yes.)".

[51] *See id.*, Trial Tr. at 1390:2-11 ("Q: But when we're talking about fabrication variations, those are variations from chip to chip; right? A: Yes. Q: So some chips will have the ability to run faster and some chips will only be able to run at slower speeds; right? A: That's right. Q: And that's why we have a binning step in manufacturing chips; correct? A: As to its effect on the CPU speed, yes, that is what binning does."); Trial Tr. at 1394:8-11 ("Q: Now, Variations in fabrication parameters, again, are from chip to chip. They're not in the same chip during operation; right? A: Yes.").

Evidence of process variation, and therefore processing frequency and clock rate variation, between chips, was shown in all HTC accused products. Qualcomm's representative, Sina Dena, testified, for example, that for the same chip design, Qualcomm separates chips with higher clock speeds at the "high end" or "fast corner of the process," from chips with lower clock speeds at the "slower corner of the process" -- a practice called binning.[52] Qualcomm assigns different product names or designations to chips in different bins even though they have the "same design."[53] In fact, "the higher speed bin products will have potentially a different frequency plan."[54] Qualcomm charges more for such chips.[55] Gafford confirmed that "there have to be process variations among

[52] *See* Docket No. 643, Trial Tr. at 1083:5-14 ("The court: The next question has to do with binning. We've heard much discussion in this trial about binning. When you were describing binning earlier during your testimony, were you referring to binning of a single or common IC design? The witness: Yes. Basically it's – it's – it's the same design which performs, can take higher clock speeds at the high end of the process, at the fast corner of the process and versus, you know, lower clock speed at the slower corner of the process.")

[53] *See id.*, Trial Tr. at 1083:5-14 ("The court: The next question has to do with binning. We've heard much discussion in this trial about binning. When you were describing binning earlier during your testimony, were you referring to binning of a single or common IC design? The witness: Yes. Basically it's – it's – it's the same design which performs, can take higher clock speeds at the high end of the process, at the fast corner of the process and versus, you know, lower clock speed at the slower corner of the process."); Trial Tr. at 1064:14-24 ("Q: Okay. Understood so you change the PLL based on the speed bin that the chip goes in; right? A: Right. And the chips usually are going to have a different identification when they are at the higher speed versus the one that – Q: And I think you called these premium chips, the faster ones, right? A: I don't know if it's premium, but the marketing group. Q: But you're able to charge more money for those chips; right? A: Yes."); 1083:22-23 ("Now, usually when the binning is done, either product name is changed or there is some sort of designation that goes.").

[54] *See id.*, Trial Tr. at 1083:22-1084:5. ("Now, usually when the binning is done, either product name is changed or there is some sort of designation that goes. So it's -- even though you might call it the same design, the higher speed bin products will have potentially a different frequency plan, and it's very simple to manage with a single release of software that we do for these chips. Basically the software reads the fuse space, finds it, okay, this is a faster device, so I'm going to change my PLL plan to a different setting for this particular device.").

[55] *See id.*, Trial Tr. at 1064:10-24 ("A: Now, is there a market for 1.2 Gigahertz? Sure, there is if you do that. So we have a premium for the fast corner process devices, and then the frequency plan, the PLL plan is going to change for that particular group of devices. Q: Okay. Understood so you change the PLL based on the speed bin that the chip goes in; right? A: Right. And the chips usually are going to have a different identification when they are at the higher speed versus the one that – Q: And I think you called these premium chips, the faster ones, right? A: I don't know if it's premium, but the marketing group. Q: But you're able to charge more money for those chips; right? A: Yes.").

the chips in the HTC accused products," "because process variation is endemic to silicon production."[56]

As to the formulae cited by HTC, they merely show how the ring oscillator uses the external crystal clock as a reference, not how the ring oscillator actually generates the clock signal. HTC's own witness, Mr. Fichter, testified that the external crystal clock in the HTC phones serves merely as a reference signal.[57] Dena confirmed that this crystal functions as a reference for the Qualcomm chips used in the HTC phones.[58] Dr. Haroun, a corporate representative from Texas Instruments, also confirmed that the external crystal clock functions as a reference for the TI chips used in the HTC phones.[59] Because the external crystal serves merely as a reference, if that crystal

[56] *See* Docket No. 684, Trial Tr. at 1393:16-23 ("Q: Now, you also recognized that there have to be process variations among the chips in the HTC accused products; right? A: Yes. Q: Because process variation is endemic to silicon production; correct? A: Yes. Q: You can't get away from it; right? A: Yes.)".

[57] *See* Docket No. 643, Trial Tr. at 1019:23-1020:3 ("Q: And have you heard of the term "Crystal Clock," or "Crystal Oscillator"? A: Yeah. Crystal Oscillator is a component that you put a voltage on the component and then it starts oscillating at a fixed frequency. It's also part of a PLL. It feeds a PLL and makes sure that the PLL has a reference signal.").

[58] *See id.*, Trial Tr. at 1044:2-12 ("Q: And at a high level, what is the purpose of a phase lock loop? A: Phase lock loop is used to provide a fixed target frequency clock signal. Q: And generally how is that achieved? A: In the Qualcomm family of chips, basically there's a fixed reference input clock that comes to a box, phase lock loop. There are elements that go into it, we call them L, M, N, different parameters, and the output frequency of the phase lock loop would be a mathematical formula of those elements multiplied by the input reference clock frequency."), Trial Tr. at 1048:10-15 ("Q: Okay. Now, one more last question about this. This TCXO right here, is that a -- what type of signal is that (indicating)? A: It's what you call a reference clock signal fixed at 19.2 and it's extremely important for PLL operation for this signal to be fixed across variation and temperatures (indicating).").

[59] Docket No. 640, Trial Tr. at 350:14-17 ("Q: Now, all of the – now, all of the OMAP chips use PLL's with -- that have a reference signal from an external clock; correct? A: That is correct."). In fact, Dr. Haroun admitted that only the ring oscillator in the TI chips could create or generate the high frequency used to clock the CPU. *Id.* at Trial Tr. at 353:23-354:3 ("Q: Okay. Let me clarify it this way: there's no other portion in the PLL besides the ring osciallator that can create a frequency that's so much higher than the external crystal; correct? A: That is correct. That is where it's -- where the extra edges are generated, yes.").

is disconnected, the ring oscillator will still be able to generate a clock signal.[60] HTC's focus on the formulae therefore ignores the fact that differently binned chips – even if they have the same design – are set to run at different frequencies and sold for different prices.

In sum, substantial evidence supports the jury's infringement verdict.

IT IS SO ORDERED.

Dated: January 21, 2014

PAUL S. GREWAL
United States Magistrate Judge

[60] *See* Docket No. 641, Trial Tr. at 567:8-22 ("Q: So the ring oscillator will still run if you disconnect the crystal? A: Yes, because crystal is not essential to generate the clock. Crystal is not needed to generate the clock.")

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, et al., Defendants.	Case No. 5:08-cv-00882-PSG **ORDER GRANTING-IN-PART HTC'S MOTION TO CORRECT THE JUDGMENT** **(Re: Docket No. 674)**

Both HTC and TPL agree that the court needs to modify the judgment as it currently stands to incorporate the court's prior order dismissing the '890 patent from this case.[1] Where the parties disagree is what form the modified judgment should take. TPL suggests the court hew closely to the present language of the judgment to which both parties previously agreed.[2] HTC believes it

[1] *See* Docket Nos. 674 and 690.

[2] *See* Docket No. 690 at 3 ("pursuant to the Court's Order dismissing U.S. Patent No. 5,530,890 (the "'890 patent") entered September 19, 2013 (Dkt. No. 594), judgment with respect to the '890 patent is entered as follows:

a) Because Defendants cannot establish entitlement to damages in the present action based on the Court's Summary Judgment Order (issued on September 17, 2013 (Dkt. No. 585)), the Court on September 19, 2013 DISMISSED the Fifth Claim for Relief in HTC's First Amended Complaint (seeking a declaration that HTC does not infringe any valid and enforceable claim of the '890 patent), and Count IV of Defendants' Answer and Counterclaim (alleging infringement of the '890 patent), subject to the conditions of the September 19, 2013 Order (Dkt. No. 594);

would be appropriate to go further by describing the dismissal of the '890 patent as entering judgment in its favor.[3]

The court agrees with TPL that moving well beyond the terms of the court's prior order would be unwarranted in this case. The prior order dismissed the '890 patent because HTC prevailed on its motion for partial summary judgment and was able to avoid a portion of TPL's infringement claims and the potential for money damages. But if the claim had proceeded to trial, broader relief to HTC was available. In particular, HTC may have invalidated the patent altogether. Under such circumstances, language characterizing the dismissal of the'890 patent as a complete victory in favor of HTC is not warranted.

b) The September 19, 2013 Order (id.) shall not affect any other claim or counterclaim asserted in the present action, and shall not impair any rights of Defendants or HTC to challenge on appeal any pretrial ruling by the Court for which an appeal is permissible including, without limitation, any challenge to the Summary Judgment Order's application of the intervening rights doctrine;

c) In the event the Federal Circuit reverses the Summary Judgment Order with respect to application of the intervening rights doctrine to the '890 patent, HTC's declaratory judgment claim and Defendants' counterclaim under the '890 patent will be reinstated and proceed unaffected by the dismissal provided in the September 19, 2013 Order (Dkt. No. 594).).

[3] Docket No. 674 at 3 ("**IT IS FURTHER ORDERED AND ADJUDGED** that pursuant to the Joint Request To Dismiss All Claims Relating to U.S. Patent No. 5,530,890 Under F.R.C.P. 41(a)(2) (Dkt. No. 594), the provisions of which are incorporated herein by reference, judgment is hereby entered in favor of Plaintiffs on Defendants' claim of infringement of U.S. Patent No. 5,530,890.").

In any event, the court finds some modification of the language from the proposed order in this case is warranted. The court adopts the following language:

Pursuant to the court's order dismissing U.S. Patent No. 5,530,890 ("the '890 patent") entered September 19, 2013 (Docket No. 594), judgment with respect to the '890 patent is entered as follows:

a) Because Defendants cannot establish entitlement to damages in the present action based on the court's summary judgment order (issued on September 17, 2013 (Docket No. 585)), the court on September 19, 2013 DISMISSED the Fifth Claim for Relief in HTC's First Amended Complaint (seeking a declaration that HTC does not infringe any valid and enforceable claim of the '890 patent), and Count IV of Defendants' Answer and Counterclaim (alleging infringement of the '890 patent), subject to the conditions of the September 19, 2013 order (Docket No. 594);

b) The September 19, 2013 order (Docket No. 594) shall not affect any other claim or counterclaim asserted in the present action, and shall not impair any rights of Defendants or HTC to challenge on appeal any pretrial ruling by the court for which an appeal is permissible including, without limitation, any challenge to the summary judgment order's application of the intervening rights doctrine;

c) In the event the Federal Circuit reverses the summary judgment order with respect to application of the intervening rights doctrine to the '890 patent, HTC's declaratory judgment claim and Defendants' counterclaim under the '890 patent will be reinstated and proceed unaffected by the dismissal provided in the September 19, 2013 order (Docket No. 594).

A revised judgment consistent with this order will issue.

IT IS SO ORDERED.

Dated: January 21, 2014

PAUL S. GREWAL
United States Magistrate Judge

United States District Court
For the Northern District of California

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, et al., Defendants.	Case No. 5:08-cv-00882-PSG **ORDER MODIFYING JUDGMENT** **(Re: Docket No. 674)**

(X) Jury Verdict. This action came before the court for a trial by jury. The issues have been tried and the jury has rendered its verdict.

IT IS SO ORDERED AND ADJUDGED that pursuant to the jury verdict filed October 3, 2013, judgment is entered in favor of Defendants.

IT IS FURTHER ORDERED pursuant to the court's order dismissing U.S. Patent No. 5,530,890 ("the '890 patent") entered September 19, 2013 (Docket No. 594), judgment with respect to the '890 patent is entered as follows:

a) Because Defendants cannot establish entitlement to damages in the present action based on the court's summary judgment order (issued on September 17, 2013 (Docket No. 585)), the court on September 19, 2013 DISMISSED the Fifth Claim for Relief in HTC's First Amended Complaint (seeking a declaration that HTC does not infringe any valid and enforceable claim of the '890 patent), and Count IV of Defendants' Answer and

Counterclaim (alleging infringement of the '890 patent), subject to the conditions of the September 19, 2013 order (Docket No. 594);

b) The September 19, 2013 order (Docket No. 594) shall not affect any other claim or counterclaim asserted in the present action, and shall not impair any rights of Defendants or HTC to challenge on appeal any pretrial ruling by the court for which an appeal is permissible including, without limitation, any challenge to the summary judgment order's application of the intervening rights doctrine;

c) In the event the Federal Circuit reverses the summary judgment order with respect to application of the intervening rights doctrine to the '890 patent, HTC's declaratory judgment claim and Defendants' counterclaim under the '890 patent will be reinstated and proceed unaffected by the dismissal provided in the September 19, 2013 order (Docket No. 594).

IT IS SO ORDERED.

Dated: January 21, 2014

PAUL S. GREWAL
United States Magistrate Judge

ADRMOP,AO279,APPEAL,CLOSED,CONSENT,E−Filing,MEDIATION,REFRAN
>REFSET−EDL,RELATE

U.S. District Court
California Northern District (San Jose)
CIVIL DOCKET FOR CASE #: 5:08−cv−00882−PSG

HTC Corporation et al v. Technology Properties Limited et al
Assigned to: Magistrate Judge Paul Singh Grewal
Referred to: Magistrate Judge Elizabeth D. Laporte (Settlement)
Relate Case Cases: 5:08−cv−00884−JF
5:08−cv−00877−PSG
5:08−cv−05398−PSG
3:10−cv−00816−JW
Case in other court: United States Court of Appeals for the Federal Cir, 14−01076
United States Court of Appeals for the Federal Cir, 14−01317
Cause: 28:2201 Declaratory Judgement

Date Filed: 02/08/2008
Date Terminated: 10/03/2013
Jury Demand: Plaintiff
Nature of Suit: 830 Patent
Jurisdiction: Federal Question

Plaintiff

HTC Corporation represented by **Kyle Dakai Chen**
Cooley Godward Kronish LLP
3000 El Camino Real
Five Palo Alto Square, 4th Floor
Palo Alto, CA 94306
650−843−5019
Fax: 650−857−0663
Email: kyle.chen@cooley.com
LEAD ATTORNEY
ATTORNEY TO BE NOTICED

Mark R. Weinstein
Cooley Godward Kronish LLP
3000 Wl Camino Real
Five Palo Alto Square, 4th Floor
Palo Alto, CA 94306
650−843−5000
Fax: 650−857−0663
Email: mweinstein@cooley.com
LEAD ATTORNEY
ATTORNEY TO BE NOTICED

Brandon D. Baum
Agility IP Law, LLP
149 Commonwealth Drive
Menlo Park, CA 94025
650−228−4800
Fax: 650−318−3483
Email: brandon@baumlegal.com
ATTORNEY TO BE NOTICED

Dena Chen
Cooley LLP
Five Palo Alto Square
3000 El Camino Real
Palo Alto, CA 94306
(650) 843−5000
Fax: (650) 849−7400
Email: dchen@cooley.com

Heidi Lyn Keefe
Cooley Godward Kronish LLP

3000 El Camino Real
Five Palo Alto Square, 4th Floor
Palo Alto, CA 94306
650−843−5000
Fax: 650−857−0663
Email: hkeefe@cooley.com
ATTORNEY TO BE NOTICED

James Carl Otteson
Agility IP Law. LLP
149 Commonwealth Drive
Menlo Park, CA 94025
650−228−4800
Fax: 650−318−−3483
Email: jim@agilityiplaw.com
ATTORNEY TO BE NOTICED

Jason Chia−Sun Fan
Cooley LLP
Five Palo Alto Square, 3000 El Camino Real
Palo Alto, CA 94306
(650) 843−5000
Email: jfan@cooley.com
ATTORNEY TO BE NOTICED

Jennifer Yokoyama
White &Case LLP
3000 El Camino Real
5 Palo Alto Square, 9th Floor
Palo Alto, CA 94306
650−213−0332
Fax: 650−213−8158
Email: jyokoyama@whitecase.com
TERMINATED: 09/24/2009

Lam Khanh Nguyen
Cooley LLP
Five Palo Alto Square
3000 El Camino Real
Palo Alto, CA 94306−2155
650−843−5000
Fax: 650−849−7400
Email: lnguyen@cooley.com
ATTORNEY TO BE NOTICED

Lia Charlotte Smith
Cooley LLP
Five Palo Alto Square, Suite 400
3000 El Camino Real
Palo Alto, CA 94306
(650) 843−5000
Fax: (650) 857−0663
Email: lsmith@cooley.com
ATTORNEY TO BE NOTICED

Matthew James Leary
Cooley LLP
380 Interlocken Crescent
Suite 900
Broomfield, CO 80021−8023
(720) 566−4000
Email: mleary@cooley.com
ATTORNEY TO BE NOTICED

Michael J. Bettinger
KLGates LLP
Four Embarcadero Center, Suite 1200
San Francisco, CA 94111
415−882−8200
Fax: 415−882−8220
Email: mike.bettinger@klgates.com
ATTORNEY TO BE NOTICED

Neil Nalin Desai
Cooley LLP
Five Palo Alto Square
3000 El Camino Real
Palo Alto, CA 94306
650−843−5000
Fax: 650−849−7400
Email: ndesai@cooley.com
ATTORNEY TO BE NOTICED

Ronald Scott Lemieux
IPSingularity
275 Shoreline Drive, Suite 520
Redwood Shores, CA 94065
650−720−4656
Email: rlemieux@ipsingularity.com
ATTORNEY TO BE NOTICED

Samuel Citron O'Rourke
White &Case LLP
3000 El Camino Real
5 Palo Alto Square
9th Floor
Palo Alto, CA 94306
650.213−0332
Fax: 650−213−8158
Email: eupton@whitecase.com
TERMINATED: 02/27/2009

Taryn Lam
Kaye Scholer LLP
Two Palo Alto Square
3000 El Camino Real, Suite 400
Palo Alto, CA 94306−2112
650−319−4503
Fax: 650−319−4903
Email: taryn.lam@kayescholer.com
TERMINATED: 09/24/2009

Wendi Renee Schepler
White &Case LLP
3000 El Camino Real
5 Palo Alto Square
9th Floor
Palo Alto, CA 94306
650−213−0323
Fax: 650−213−8158
Email: wschepler@whitecase.com
TERMINATED: 09/24/2009

William Sloan Coats , III
Greenberg Traurig, LLP
1900 University Ave., 5th Floor
East Palo Alto, CA 94303
650−328−8500
Fax: (650) 328−8505

Email: coatsw@gtlaw.com
TERMINATED: 09/24/2009

Plaintiff

HTC America, Inc. represented by **Kyle Dakai Chen**
(See above for address)
LEAD ATTORNEY
ATTORNEY TO BE NOTICED

Mark R. Weinstein
(See above for address)
LEAD ATTORNEY
ATTORNEY TO BE NOTICED

Brandon D. Baum
(See above for address)
ATTORNEY TO BE NOTICED

Dena Chen
(See above for address)

Heidi Lyn Keefe
(See above for address)
ATTORNEY TO BE NOTICED

James Carl Otteson
(See above for address)
ATTORNEY TO BE NOTICED

Jason Chia−Sun Fan
(See above for address)
ATTORNEY TO BE NOTICED

Jennifer Yokoyama
(See above for address)
TERMINATED: 09/24/2009

Lam Khanh Nguyen
(See above for address)
ATTORNEY TO BE NOTICED

Lia Charlotte Smith
(See above for address)
ATTORNEY TO BE NOTICED

Matthew James Leary
(See above for address)
ATTORNEY TO BE NOTICED

Michael J. Bettinger
(See above for address)
ATTORNEY TO BE NOTICED

Neil Nalin Desai
(See above for address)
ATTORNEY TO BE NOTICED

Ronald Scott Lemieux
(See above for address)
ATTORNEY TO BE NOTICED

Samuel Citron O'Rourke
(See above for address)
TERMINATED: 02/27/2009

Taryn Lam
(See above for address)
TERMINATED: 09/24/2009

Wendi Renee Schepler
(See above for address)
TERMINATED: 09/24/2009

William Sloan Coats , III
(See above for address)
TERMINATED: 09/24/2009

V.

Defendant

Technology Properties Limited represented by **James Carl Otteson**
Agility IP Law. LLP
149 Commonwealth Drive
Suite 1033
Menlo Park, CA 94025
650−227−4800
Fax: 650−318−−3483
Email: jim@agilityiplaw.com
LEAD ATTORNEY
ATTORNEY TO BE NOTICED

Brandon D. Baum
Baum Legal
149 Commonwealth Drive
Menlo Park, CA 94025
650−924−1032
Fax: 650−561−8410
Email: brandon@baumlegal.com
ATTORNEY TO BE NOTICED

Christoper Lee Ogden
Nixon Peabody LLP
200 Page Mill Road
2nd Floor
Palo Alto, CA 94306−2022
650−320−7700
Fax: 866−903−1920
Email: cogden@nixonpeabody.com
TERMINATED: 02/08/2010

David L. Lansky
Agility IP Law, LLP
149 Commonwealth Drive
Menlo Park, CA 94025
650/227−4800
Fax: 650/318−3483
Email: dlansky@agilityiplaw.com
ATTORNEY TO BE NOTICED

Deepak Gupta
Farella Braun Martel LLP
235 Montgomery Street
17th Floor
San Francisco, CA 94104
415−954−4400
Fax: 415−954−4480
Email: dgupta@fbm.com
TERMINATED: 11/16/2011

Eugene Y. Mar
Farella Braun &Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954−4927
Fax: (415) 954−4480
Email: emar@fbm.com
TERMINATED: 11/16/2011

Irvin E. Tyan
Agility IP Law
149 Commonwealth Drive
Menlo Park, CA 94025
650−227−4800
Fax: 650−318−3483
Email: ityan@agilityiplaw.com
ATTORNEY TO BE NOTICED

James R. Farmer
OTTESON LAW GROUP AGILITY IP LAW, LLP
14350 North 87th Street
Suite 190
Scottsdale, AZ 85260
480−646−3434
Fax: 480−646−3438
Email: james.farmer@rocketmail.com
PRO HAC VICE

Jedediah Phillips
Agility IP Law, LLP
149 Commonwealth Drive
Menlo Park, CA 94025
(650) 227−4800
Fax: (650) 318−3483
Email: jed@agilityiplaw.com
ATTORNEY TO BE NOTICED

Jeffrey M. Fisher
Farella Braun &Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
(415) 954−4400
Fax: (415) 954−4480
TERMINATED: 11/16/2011

John L. Cooper
Farella Braun &Martel LLP
Russ Building, 30th Floor
235 Montgomery Street
San Francisco, CA 94104
415/954−4400
Fax: 415−954−4480
Email: jcooper@fbm.com
TERMINATED: 11/16/2011

Michael J. Bettinger
(See above for address)
ATTORNEY TO BE NOTICED

Michelle Gail Breit
Agility IP Law, LLP
149 Commonwealth Drive
Menlo Park, CA 94025

Case4:08-cv-882 As of: 09/09/2014 04:14 PM PDT

650−227−4800
Fax: 650−318−3483
Email: mbreit@agilityiplaw.com
ATTORNEY TO BE NOTICED

Nan E. Joesten
Farella Braun &Martel LLP
235 Montgomery Street
San Francisco, CA 94104
(415) 954−4400
Fax: (415) 954−4480
Email: njoesten@fbm.com
TERMINATED: 11/16/2011

Philip William Marsh
Agility IP Law
149 Commonwealth Drive
Suite 1033
Menlo Park, CA 94025
650−227−4800
Fax: 650−318−3483
Email: phil@agilityiplaw.com
ATTORNEY TO BE NOTICED

Ronald Frank Lopez
Nixon Peabody LLP
One Embarcadero Center
18th Floor
San Francisco, CA 94111−3600
(415) 984−8368
Fax: (866) 293−2789
Email: rflopez@nixonpeabody.com
TERMINATED: 02/08/2010

Stephanie Powers Skaff
Farella Braun and Martel LLP
235 Montgomery Street, 17th Floor
San Francisco, CA 94104
415/954−4400
Fax: 415/954−4480
Email: sskaff@fbm.com
TERMINATED: 11/16/2011

Sushila Chanana
McDermott Will &Emery LLP
275 Middlefield Road
Suite 100
Menlo Park, CA 94025
650−815−7400
Fax: 650−815−7401
Email: schanana@mwe.com
TERMINATED: 02/08/2010

Thomas T. Carmack
Agility IP Law, LLP
149 Commonwealth Drive
Suite 1033
Menlo Park, CA 94025
650−227−4800
Fax: 650−318−3483
Email: tom@agilityiplaw.com
ATTORNEY TO BE NOTICED

Vinh Huy Pham
Attorney at Law

Agility IP Law
149 Commonwealth Drive
Menlo Park, CA 94025
(408) 982−6101
Fax: 6503183483
Email: vpham@agilityiplaw.com
ATTORNEY TO BE NOTICED

Defendant

Patriot Scientific Corporation represented by

Charles T. Hoge
Attorney at Law
350 Tenth Avenue
Suite 1300
San Diego, CA 92101
619−231−8666
Fax: 619−231−9593
Email: choge@knlh.com
LEAD ATTORNEY
ATTORNEY TO BE NOTICED

Philip William Marsh
(See above for address)
LEAD ATTORNEY
ATTORNEY TO BE NOTICED

Thomas T. Carmack
(See above for address)
LEAD ATTORNEY
ATTORNEY TO BE NOTICED

Brandon D. Baum
(See above for address)
ATTORNEY TO BE NOTICED

Christoper Lee Ogden
(See above for address)
TERMINATED: 02/08/2010

David L. Lansky
(See above for address)
ATTORNEY TO BE NOTICED

Eugene Y. Mar
(See above for address)
TERMINATED: 11/16/2011

Irvin E. Tyan
(See above for address)
ATTORNEY TO BE NOTICED

James Carl Otteson
(See above for address)
ATTORNEY TO BE NOTICED

Jedediah Phillips
(See above for address)
ATTORNEY TO BE NOTICED

John L. Cooper
(See above for address)
TERMINATED: 11/16/2011

Michael J. Bettinger
(See above for address)

ATTORNEY TO BE NOTICED

Michelle Gail Breit
(See above for address)
ATTORNEY TO BE NOTICED

Sushila Chanana
(See above for address)
TERMINATED: 02/08/2010

Defendant

Alliacense Limited represented by

James Carl Otteson
(See above for address)
LEAD ATTORNEY
ATTORNEY TO BE NOTICED

Brandon D. Baum
(See above for address)
ATTORNEY TO BE NOTICED

Christoper Lee Ogden
(See above for address)
TERMINATED: 02/08/2010

David L. Lansky
(See above for address)
ATTORNEY TO BE NOTICED

Deepak Gupta
(See above for address)
TERMINATED: 11/16/2011

Eugene Y. Mar
(See above for address)
TERMINATED: 11/16/2011

Irvin E. Tyan
(See above for address)
ATTORNEY TO BE NOTICED

James R. Farmer
(See above for address)
PRO HAC VICE
ATTORNEY TO BE NOTICED

Jedediah Phillips
(See above for address)
ATTORNEY TO BE NOTICED

Jeffrey M. Fisher
(See above for address)
TERMINATED: 11/16/2011

John L. Cooper
(See above for address)
TERMINATED: 11/16/2011

Michael J. Bettinger
(See above for address)
ATTORNEY TO BE NOTICED

Michelle Gail Breit
(See above for address)
ATTORNEY TO BE NOTICED

Nan E. Joesten
(See above for address)
TERMINATED: 11/16/2011

Philip William Marsh
(See above for address)
ATTORNEY TO BE NOTICED

Ronald Frank Lopez
(See above for address)
TERMINATED: 02/08/2010

Stephanie Powers Skaff
(See above for address)
TERMINATED: 11/16/2011

Sushila Chanana
(See above for address)
TERMINATED: 02/08/2010

Thomas T. Carmack
(See above for address)
ATTORNEY TO BE NOTICED

Vinh Huy Pham
(See above for address)
ATTORNEY TO BE NOTICED

V.

Movant

Non Party Texas Instruments Incorporated

represented by **Anupam Sharma**
Covington &Burling LLP
333 Twin Dolphin Drive, Suite 700
Redwood Shores, CA 94065−1418
650−632−4709
Fax: 650−632−4809
Email: asharma@cov.com
ATTORNEY TO BE NOTICED

Miscellaneous

Kwan Chan
2501 Cowper Street
Palo Alto, CA 94301
Technical Advisor
TERMINATED: 08/21/2012

Miscellaneous

Qualcomm Inc.

represented by **Benjamin George Damstedt**
Cooley Godward Kronish LLP
Five Palo Alto Square
3000 El Camino Real
Palo Alto, CA 94306
650−843−5000
Fax: 650−857−0663
Email: bdamstedt@cooley.com
ATTORNEY TO BE NOTICED

James Carl Otteson
(See above for address)
ATTORNEY TO BE NOTICED

Counter−claimant

Technology Properties Limited represented by **Christoper Lee Ogden**
(See above for address)
TERMINATED: 02/08/2010

Eugene Y. Mar
(See above for address)
TERMINATED: 11/16/2011

James R. Farmer
(See above for address)
PRO HAC VICE

James Carl Otteson
(See above for address)
ATTORNEY TO BE NOTICED

Jeffrey M. Fisher
(See above for address)
TERMINATED: 11/16/2011

John L. Cooper
(See above for address)
TERMINATED: 11/16/2011

Michelle Gail Breit
(See above for address)
ATTORNEY TO BE NOTICED

Nan E. Joesten
(See above for address)
TERMINATED: 11/16/2011

Ronald Frank Lopez
(See above for address)
TERMINATED: 02/08/2010

Sushila Chanana
(See above for address)
TERMINATED: 02/08/2010

Counter−claimant

Alliacense Limited represented by **Christoper Lee Ogden**
(See above for address)
TERMINATED: 02/08/2010

Eugene Y. Mar
(See above for address)
TERMINATED: 11/16/2011

James R. Farmer
(See above for address)
PRO HAC VICE
ATTORNEY TO BE NOTICED

James Carl Otteson
(See above for address)
ATTORNEY TO BE NOTICED

Jeffrey M. Fisher
(See above for address)
TERMINATED: 11/16/2011

John L. Cooper
(See above for address)
TERMINATED: 11/16/2011

Michelle Gail Breit
(See above for address)
ATTORNEY TO BE NOTICED

Nan E. Joesten
(See above for address)
TERMINATED: 11/16/2011

Ronald Frank Lopez
(See above for address)
TERMINATED: 02/08/2010

Sushila Chanana
(See above for address)
TERMINATED: 02/08/2010

V.

Counter−defendant

Technology Properties Limited represented by **Christoper Lee Ogden**
(See above for address)
TERMINATED: 02/08/2010

Eugene Y. Mar
(See above for address)
TERMINATED: 11/16/2011

James R. Farmer
(See above for address)
PRO HAC VICE

James Carl Otteson
(See above for address)
ATTORNEY TO BE NOTICED

Jeffrey M. Fisher
(See above for address)
TERMINATED: 11/16/2011

John L. Cooper
(See above for address)
TERMINATED: 11/16/2011

Michelle Gail Breit
(See above for address)
ATTORNEY TO BE NOTICED

Nan E. Joesten
(See above for address)
TERMINATED: 11/16/2011

Ronald Frank Lopez
(See above for address)
TERMINATED: 02/08/2010

Sushila Chanana
(See above for address)
TERMINATED: 02/08/2010

Counter−defendant

Alliacense Limited	represented by	**Christoper Lee Ogden** (See above for address) *TERMINATED: 02/08/2010* **Eugene Y. Mar** (See above for address) *TERMINATED: 11/16/2011* **James R. Farmer** (See above for address) *PRO HAC VICE* *ATTORNEY TO BE NOTICED* **James Carl Otteson** (See above for address) *ATTORNEY TO BE NOTICED* **Jeffrey M. Fisher** (See above for address) *TERMINATED: 11/16/2011* **John L. Cooper** (See above for address) *TERMINATED: 11/16/2011* **Michelle Gail Breit** (See above for address) *ATTORNEY TO BE NOTICED* **Nan E. Joesten** (See above for address) *TERMINATED: 11/16/2011* **Ronald Frank Lopez** (See above for address) *TERMINATED: 02/08/2010* **Sushila Chanana** (See above for address) *TERMINATED: 02/08/2010*

Date Filed	#	Docket Text
02/08/2008	1	COMPLAINT /issued summons against Technology Properties Limited, Patriot Scientific Corporation, Alliacense Limited (Filing fee $ 350, receipt number 54611002555.). Filed byHTC Corporation, HTC America, Inc.. (ga, COURT STAFF) (Filed on 2/8/2008) (ga, COURT STAFF). (Entered: 02/13/2008)
02/08/2008	2	ADR SCHEDULING ORDER: Case Management Statement due by 5/14/2008. Case Management Conference set for 5/21/2008 10:30 AM.. Signed by Judge James Larson on 2/8/08. (Attachments: # 1 Judge Standing Order, # 2 Court Standing Order, # 3 Consent/Decline Form)(ga, COURT STAFF) (Filed on 2/8/2008) (Entered: 02/13/2008)
02/08/2008		CASE DESIGNATED for Electronic Filing. (ga, COURT STAFF) (Filed on 2/8/2008) (Entered: 02/13/2008)
02/13/2008	3	REPORT on the filing of an action regarding PATENT (cc: form mailed to register). (ga, COURT STAFF) (Filed on 2/13/2008) (Entered: 02/13/2008)
03/18/2008	4	CERTIFICATE OF SERVICE by HTC Corporation, HTC America, Inc. *Summons and Complaint (Technology Properties Limited)* (Chen, Kyle) (Filed on 3/18/2008) (Entered: 03/18/2008)

03/18/2008	5	CERTIFICATE OF SERVICE by HTC Corporation, HTC America, Inc. *Summons and Complaint (Alliacense Limited)* (Chen, Kyle) (Filed on 3/18/2008) (Entered: 03/18/2008)
03/18/2008	6	CERTIFICATE OF SERVICE by HTC Corporation, HTC America, Inc. *Summons and Complaint (Patriot Scientific Corporation)* (Chen, Kyle) (Filed on 3/18/2008) (Entered: 03/18/2008)
03/19/2008	12	SUMMONS Returned Executed by HTC Corporation, HTC America, Inc.. Alliacense Limited served on 3/10/2008, answer due 3/31/2008. (ga, COURT STAFF) (Filed on 3/19/2008) (Entered: 03/27/2008)
03/19/2008	13	SUMMONS Returned Executed by HTC Corporation, HTC America, Inc.. Patriot Scientific Corporation served on 3/10/2008, answer due 3/31/2008. (ga, COURT STAFF) (Filed on 3/19/2008) (Entered: 03/27/2008)
03/19/2008	14	SUMMONS Returned Executed by HTC Corporation, HTC America, Inc.. Technology Properties Limited served on 3/10/2008, answer due 3/31/2008. (ga, COURT STAFF) (Filed on 3/19/2008) (Entered: 03/27/2008)
03/21/2008	7	Certificate of Interested Entities by HTC Corporation, HTC America, Inc. (Weinstein, Mark) (Filed on 3/21/2008) (Entered: 03/21/2008)
03/21/2008	8	CERTIFICATE OF SERVICE by HTC Corporation, HTC America, Inc. re 7 Certificate of Interested Entities (Weinstein, Mark) (Filed on 3/21/2008) (Entered: 03/21/2008)
03/26/2008	9	STIPULATION *for Extension of Time for Defendants to Respond to Complaint for Declaratory Judgment* by Technology Properties Limited, Alliacense Limited. (Lopez, Ronald) (Filed on 3/26/2008) (Entered: 03/26/2008)
03/26/2008	10	Declaration in Support of 9 Stipulation *(per General Order 45)* filed byTechnology Properties Limited, Alliacense Limited. (Related document(s) 9) (Lopez, Ronald) (Filed on 3/26/2008) (Entered: 03/26/2008)
03/26/2008	11	CERTIFICATE OF SERVICE by Technology Properties Limited, Alliacense Limited re 9 Stipulation *on Counsel for Patriot Scientific Corporation* (Lopez, Ronald) (Filed on 3/26/2008) (Entered: 03/26/2008)
04/25/2008	15	MOTION to Dismiss for Lack of Jurisdiction *: NOTICE OF MOTION AND MOTION TO DISMISS FOR LACK OF SUBJECT MATTER JURISDICTION, OR TO TRANSFER, OR TO STAY PROCEEDINGS* filed by Technology Properties Limited, Patriot Scientific Corporation, Alliacense Limited. Motion Hearing set for 6/4/2008 09:30 AM in Courtroom F, 15th Floor, San Francisco. (Attachments: # 1 Proposed Order Granting Dismissal, or Alternatively Transfer, or Alternatively Stay)(Ogden, Christopher) (Filed on 4/25/2008) (Entered: 04/25/2008)
04/25/2008	16	Brief re 15 MOTION to Dismiss for Lack of Jurisdiction *: NOTICE OF MOTION AND MOTION TO DISMISS FOR LACK OF SUBJECT MATTER JURISDICTION, OR TO TRANSFER, OR TO STAY PROCEEDINGS −−MEMORANDUM IN SUPPORT−−* filed byTechnology Properties Limited, Patriot Scientific Corporation, Alliacense Limited. (Related document(s) 15) (Ogden, Christopher) (Filed on 4/25/2008) (Entered: 04/25/2008)
04/25/2008	17	Declaration of RONALD F. LOPEZ in Support of 15 MOTION to Dismiss for Lack of Jurisdiction *: NOTICE OF MOTION AND MOTION TO DISMISS FOR LACK OF SUBJECT MATTER JURISDICTION, OR TO TRANSFER, OR TO STAY PROCEEDINGS*, 16 Brief, filed byTechnology Properties Limited, Patriot Scientific Corporation, Alliacense Limited. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Exhibit G, # 8 Exhibit H, # 9 Exhibit I, # 10 Exhibit J, # 11 Exhibit K, # 12 Exhibit L, # 13 Exhibit M, # 14 Exhibit N, # 15 Exhibit O, # 16 Signature attestation)(Related document(s) 15 , 16) (Ogden, Christopher) (Filed on 4/25/2008) (Entered: 04/25/2008)
04/25/2008	18	Declaration of ROGER COOK in Support of 15 MOTION to Dismiss for Lack of Jurisdiction *: NOTICE OF MOTION AND MOTION TO DISMISS FOR LACK OF SUBJECT MATTER JURISDICTION, OR TO TRANSFER, OR TO STAY*

		PROCEEDINGS, 16 Brief, filed byTechnology Properties Limited, Patriot Scientific Corporation, Alliacense Limited. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E)(Related document(s) 15 , 16) (Ogden, Christopher) (Filed on 4/25/2008) (Entered: 04/25/2008)
04/25/2008	19	***** FILED IN ERROR. PLEASE SEE DOCKET # 20 . ***** Declaration of MIKE DAVIS in Support of 15 MOTION to Dismiss for Lack of Jurisdiction *: NOTICE OF MOTION AND MOTION TO DISMISS FOR LACK OF SUBJECT MATTER JURISDICTION, OR TO TRANSFER, OR TO STAY PROCEEDINGS*, 16 Brief, filed byTechnology Properties Limited, Patriot Scientific Corporation, Alliacense Limited. (Related document(s) 15 , 16) (Ogden, Christopher) (Filed on 4/25/2008) Modified on 4/28/2008 (ewn, COURT STAFF). (Entered: 04/25/2008)
04/25/2008	20	Declaration of MIKE DAVIS in Support of 15 MOTION to Dismiss for Lack of Jurisdiction *: NOTICE OF MOTION AND MOTION TO DISMISS FOR LACK OF SUBJECT MATTER JURISDICTION, OR TO TRANSFER, OR TO STAY PROCEEDINGS*, 16 Brief, ****previous filing 19 filed in error**** filed byTechnology Properties Limited, Patriot Scientific Corporation, Alliacense Limited. (Related document(s) 15 , 16) (Ogden, Christopher) (Filed on 4/25/2008) (Entered: 04/25/2008)
04/29/2008	21	RELATED CASE ORDER. Signed by Judge Jeremy Fogel on 4/22/08. (dlm, COURT STAFF) (Filed on 4/29/2008) (Entered: 04/29/2008)
05/01/2008		Pursuant to Related Case Order (21). Case reassigned to District Judge Jeremy Fogel for all further proceedings and Magistrate Judge Howard R. Lloyd for all discovery matters Magistrate Judge James Larson no longer assigned to the case. (tsh, COURT STAFF) (Filed on 5/1/2008) (Entered: 05/01/2008)
05/08/2008	22	CLERK'S NOTICE Case Management Conference set for 5/30/2008 10:30 AM. (dlm, COURT STAFF) (Filed on 5/8/2008) (Entered: 05/08/2008)
05/16/2008	23	ADR Clerks Notice re: Non−Compliance with Court Order. (tjs, COURT STAFF) (Filed on 5/16/2008) (Entered: 05/16/2008)
05/19/2008	24	First MOTION to Amend/Correct *Notice of Motion* filed by Technology Properties Limited, Patriot Scientific Corporation, Alliacense Limited. Motion Hearing set for 8/1/2008 09:00 AM in Courtroom 3, 5th Floor, San Jose. (Chanana, Sushila) (Filed on 5/19/2008) (Entered: 05/19/2008)
05/21/2008	25	STIPULATION *and [Proposed] Order to Continue CMC* by HTC Corporation, HTC America, Inc.. (Chen, Kyle) (Filed on 5/21/2008) (Entered: 05/21/2008)
05/23/2008	26	ORDER GRANTING STIPULATED REQUEST TO CONTINUE CASE MANAGEMENT CONFERENCE re 25 Stipulation filed by HTC America, Inc., HTC Corporation Initial Case Management Conference set for 8/1/2008 10:30 AM. Signed by Judge Jeremy Fogel on 5/23/08. (jfsec, COURT STAFF) (Filed on 5/23/2008) (Entered: 05/23/2008)
05/23/2008	27	STIPULATION and Proposed Order selecting Mediation by HTC Corporation, HTC America, Inc. , *and Technology Properties Limited et al.* (Chen, Kyle) (Filed on 5/23/2008) (Entered: 05/23/2008)
05/28/2008	28	ORDER REFERRING CASE to Mediation. Signed by Judge Jeremy Fogel on 5/28/08. (jfsec, COURT STAFF) (Filed on 5/28/2008) (Entered: 05/28/2008)
05/29/2008	29	ADR Certification (ADR L.R. 3−5b) of discussion of ADR options *BY PARTIES AND COUNSEL* (Chanana, Sushila) (Filed on 5/29/2008) (Entered: 05/29/2008)
06/09/2008	30	ADR Clerks Notice Setting ADR Phone Conference on Wednesday, June 18, 2008 at 1:00 p.m. PDT. The ADR Unit will initiate the call. (af, COURT STAFF) (Filed on 6/9/2008) (Entered: 06/09/2008)
06/18/2008		ADR Remark: ADR Phone Conference held by Daniel Bowling, ADR Program Staff Attorney on 6/18/2008. (af, COURT STAFF) (Filed on 6/18/2008) (Entered: 06/18/2008)

06/20/2008	31	STIPULATION *AND [PROPOSED] ORDER TO EXTEND MEDIATION DEADLINE TO OCT. 27, 2008* by HTC Corporation, HTC America, Inc.. (Chen, Kyle) (Filed on 6/20/2008) (Entered: 06/20/2008)
06/20/2008	32	ADR Certification (ADR L.R. 3−5 b) of discussion of ADR options *signed by Hogo Ho (HTC Corp. and HTC America) and by Kyle Chen (White &Case)* (Chen, Kyle) (Filed on 6/20/2008) (Entered: 06/20/2008)
07/02/2008	33	ORDER Extending ADR (Mediation) Deadline. Signed by Judge Jeremy Fogel on 7/2/08. (jfsec, COURT STAFF) (Filed on 7/2/2008) (Entered: 07/02/2008)
07/10/2008	34	AMENDED COMPLAINT *First Amended Complaint for Declaratory Judgment* against all defendants. Filed byHTC Corporation, HTC America, Inc.. (Chen, Kyle) (Filed on 7/10/2008) (Entered: 07/10/2008)
07/11/2008	35	Memorandum in Opposition *to Defendants' 15 Motion (1) to Dismiss on Grounds of Lack Subject Matter Jurisdiction, (2) in the Alternative to Transfer to the Eastern District of Texas, and (3) in the Alternative, to Stay Pending Appeal in a Related Case Involving the Same Issues* filed byHTC Corporation, HTC America, Inc.. (Chen, Kyle) (Filed on 7/11/2008) Modified on 7/14/2008 (gm, COURT STAFF). (Entered: 07/11/2008)
07/11/2008	36	Declaration of Hogo Ho in Support of 35 Memorandum in Opposition, filed byHTC Corporation, HTC America, Inc.. (Related document(s) 35) (Chen, Kyle) (Filed on 7/11/2008) (Entered: 07/11/2008)
07/11/2008	37	Declaration of Mark F. Lambert in Support of 35 Memorandum in Opposition, filed byHTC Corporation, HTC America, Inc.. (Attachments: # 1 Exhibit A)(Related document(s) 35) (Chen, Kyle) (Filed on 7/11/2008) (Entered: 07/11/2008)
07/11/2008	38	Request for Judicial Notice *Under F.R.E. of Certain Documents Filed in Technology Properties Limited, Inc. v. Fujitsu Limited, et. al., Case No. 2:05−cv−00494−TJW* filed byHTC Corporation, HTC America, Inc.. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F)(Chen, Kyle) (Filed on 7/11/2008) (Entered: 07/11/2008)
07/11/2008	39	Proposed Order re 38 Request for Judicial Notice, by HTC Corporation, HTC America, Inc.. (Chen, Kyle) (Filed on 7/11/2008) (Entered: 07/11/2008)
07/18/2008	40	ADR Clerks Notice Appointing Jack L. Slobodin as Mediator. (af, COURT STAFF) (Filed on 7/18/2008) (Entered: 07/18/2008)
07/18/2008	41	JOINT CASE MANAGEMENT STATEMENT filed by HTC Corporation, HTC America, Inc.. (Chen, Kyle) (Filed on 7/18/2008) (Entered: 07/18/2008)
07/18/2008	42	Reply Memorandum *IN SUPPORT OF DEFENDANTS' 15 MOTION (1) TO DISMISS, (2) TO TRANSFER, OR TO (3) STAY* filed byTechnology Properties Limited, Patriot Scientific Corporation, Alliacense Limited. (Ogden, Christopher) (Filed on 7/18/2008) Modified on 7/21/2008 (gm, COURT STAFF). (Entered: 07/18/2008)
07/18/2008	43	Declaration of SUSHILA CHANANA *IN SUPPORT OF 42 REPLY TO DEFENDANTS' MOTION TO (1) DISMISS, (2) TRANSFER, OR (3) STAY* filed byTechnology Properties Limited. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Exhibit G, # 8 Exhibit H)(Ogden, Christopher) (Filed on 7/18/2008) Modified on 7/21/2008 (gm, COURT STAFF). (Entered: 07/19/2008)
07/21/2008	44	CLERK'S NOTICE Continuing Motion to Dismiss, Motion to Transfer and or Stay and the Case Management Conference for 8/8/2008 9:00 AM. (jfsec, COURT STAFF) (Filed on 7/21/2008) (Entered: 07/21/2008)
07/29/2008		ADR Remark: Mediator would like to conduct the pre mediation telephone conference call at 10:30 a.m. on July 31, 2008. Counsel to confirm their availability for the call directly with mediator as soon as possible. (af, COURT STAFF) (Filed on 7/29/2008) (Entered: 07/29/2008)

07/31/2008		Pre MED phone conference scheduled on Thursday, July 31, 2008 at 10:30 a.m. (af, COURT STAFF) (Filed on 7/31/2008) (Entered: 07/31/2008)
08/05/2008		Set/Reset Hearings: Mediation Hearing set for 10/14/2008 10:00 AM., in the offices of Thelen Reid, 101 Second Street, San Francisco, CA. Briefs are to be submitted to the mediator only 10 days before the mediation. There is a 10−page limit. (af, COURT STAFF) (Filed on 8/5/2008) (Entered: 08/05/2008)
08/06/2008	45	STIPULATION *AND [PROPOSED] ORDER TO CONTINUE HEARINGS ON MOTIONS TO DISMISS, TRANSFER, OR STAY AND CASE MANAGEMENT CONFERENCE* by Technology Properties Limited, Patriot Scientific Corporation, Alliacense Limited. (Chanana, Sushila) (Filed on 8/6/2008) (Entered: 08/06/2008)
08/12/2008	46	ORDER CONTINUING HEARINGS ON MOTION TO DISMISS TRANSFER OR STAY AND CASE MANAGEMENT CONFERENCE re 45 Stipulation, filed by Technology Properties Limited, Alliacense Limited, Patriot Scientific Corporation Further Case Management Conference set for 9/19/2008 9:00 AM. Motion Hearing set for 9/19/2008 09:00 AM. Signed by Judge Jeremy Fogel on 8/12/08. (jfsec, COURT STAFF) (Filed on 8/12/2008) Modified on 9/16/2008 (dlm, COURT STAFF). (Entered: 08/12/2008)
09/11/2008	47	NOTICE by Technology Properties Limited, Patriot Scientific Corporation, Alliacense Limited *NOTICE OF LAW FIRM NAME CHANGE* (Chanana, Sushila) (Filed on 9/11/2008) (Entered: 09/11/2008)
09/19/2008	48	Minute Entry: Motion Hearing held on 9/19/2008 before Judge Jeremy Fogel (Date Filed: 9/19/2008) re 24 First MOTION to Dismiss. Case Management Conference set for 11/7/2008 10:30 AM. (Court Reporter Summer Clanton.) (dlm, COURT STAFF) (Date Filed: 9/19/2008) (Entered: 09/22/2008)
10/21/2008	49	ORDER BY JUDGE JEREMY FOGEL DENYING 15 MOTION TO DISMISS, TO TRANSFER VENUE, AND TO STAY. (jflc2, COURT STAFF) (Filed on 10/21/2008) (Entered: 10/21/2008)
11/07/2008	50	CERTIFICATION OF MEDIATION Session on 10/14/2008, case not settled, phone discussions expected within 2 weeks, mediation continuing. Signed by Mediator, Jack Slobodin, dated 11/4/2008. (af, COURT STAFF) (Filed on 11/7/2008) (Entered: 11/07/2008)
11/07/2008	51	Minute Entry: Further Case Management Conference held on 11/7/2008 before Judge Jeremy Fogel (Date Filed: 11/7/2008). Further Case Management Conference set for 12/19/2008 10:30 AM. (Court Reporter Summer Clanton.) (dlm, COURT STAFF) (Date Filed: 11/7/2008) (Entered: 11/12/2008)
11/12/2008	52	Transcript of Proceedings before Judge Jeremy Fogel. Court Reporter/Transcriber Summer Clanton, Telephone number 408−288−6150. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 2/9/2009. (Clanton, Summer) (Filed on 11/12/2008) (Entered: 11/12/2008)
11/20/2008	53	NOTICE of Substitution of Counsel by Sushila Chanana (Chanana, Sushila) (Filed on 11/20/2008) (Entered: 11/20/2008)
11/20/2008	54	MOTION to Compel *the Depositions and Trial Testimony of Plaintiff HTC's Witnesses in This District* filed by Technology Properties Limited, Alliacense Limited. Motion Hearing set for 12/23/2008 10:00 AM in Courtroom 2, 5th Floor, San Jose. (Chanana, Sushila) (Filed on 11/20/2008) (Entered: 11/20/2008)
11/20/2008	55	Declaration of Sushila Chanana in Support of 54 MOTION to Compel *the Depositions and Trial Testimony of Plaintiff HTC's Witnesses in This District and Exhibit A* filed byTechnology Properties Limited, Alliacense Limited. (Related document(s) 54) (Chanana, Sushila) (Filed on 11/20/2008) (Entered: 11/20/2008)

11/20/2008	56	STIPULATION re 54 MOTION to Compel *the Depositions and Trial Testimony of Plaintiff HTC's Witnesses in This District Request for Order Shortening Time on Defendant's Motion to Compel* by Technology Properties Limited, Alliacense Limited. (Chanana, Sushila) (Filed on 11/20/2008) (Entered: 11/20/2008)
11/20/2008	57	Proposed Order re 56 Stipulation, *Request for Order Shortening Time on Defendant's Motion to Compel the Depositions and Trial Testimony of Plaintiff HTC's Witnesses in This District* by Technology Properties Limited, Alliacense Limited. (Chanana, Sushila) (Filed on 11/20/2008) (Entered: 11/20/2008)
11/20/2008	58	Proposed Order re 54 MOTION to Compel *the Depositions and Trial Testimony of Plaintiff HTC's Witnesses in This District* by Technology Properties Limited, Alliacense Limited. (Chanana, Sushila) (Filed on 11/20/2008) (Entered: 11/20/2008)
11/21/2008	59	STIPULATION AND ORDER re 57 Proposed Order, filed by Technology Properties Limited, Alliacense Limited. Signed by Magistrate Judge Howard R. Lloyd on 11/21/08. (hrllc1, COURT STAFF) (Filed on 11/21/2008) (Entered: 11/21/2008)
11/21/2008	60	*TECHNOLOGY PROPERTIES LIMITED and ALLIACENSE LIMITED's* ANSWER to Amended Complaint *For Declaratory Judgment*, First COUNTERCLAIM against Technology Properties Limited, Alliacense Limited byTechnology Properties Limited, Alliacense Limited. (Chanana, Sushila) (Filed on 11/21/2008) (Entered: 11/21/2008)
12/01/2008	61	Memorandum in Opposition re 54 MOTION to Compel *the Depositions and Trial Testimony of Plaintiff HTC's Witnesses in This District* filed byHTC Corporation, HTC America, Inc.. (Chen, Kyle) (Filed on 12/1/2008) (Entered: 12/01/2008)
12/01/2008	62	DECLARATION of Mark F. Lambert in Opposition to 61 Memorandum in Opposition filed byHTC Corporation, HTC America, Inc.. (Related document(s) 61) (Chen, Kyle) (Filed on 12/1/2008) (Entered: 12/01/2008)
12/05/2008	63	Reply Memorandum re 54 MOTION to Compel *the Depositions and Trial Testimony of Plaintiff HTC's Witnesses in This District* filed byTechnology Properties Limited, Alliacense Limited, Patriot Scientific Corporation. (Ogden, Christoper) (Filed on 12/5/2008) (Entered: 12/05/2008)
12/05/2008	64	Declaration of Ronald F. Lopez in Support of 63 Reply Memorandum, filed byTechnology Properties Limited, Alliacense Limited, Patriot Scientific Corporation. (Related document(s) 63) (Chanana, Sushila) (Filed on 12/5/2008) (Entered: 12/05/2008)
12/11/2008	65	ANSWER TO COUNTERCLAIM 60 Answer to Amended Complaint,, Counterclaim, byHTC Corporation, HTC America, Inc.. (Chen, Kyle) (Filed on 12/11/2008) (Entered: 12/11/2008)
12/15/2008	66	Joinder *of Defendants in Opposition to Barco's Civil L.R. 3−12 Administrative Motion to Consider Whether Cases Should be Related; Filed in Related Case No. 08−cv−00877* by Technology Properties Limited, Alliacense Limited, Patriot Scientific Corporation. (Chanana, Sushila) (Filed on 12/15/2008) (Entered: 12/15/2008)
12/16/2008	67	Minute Entry: Motion Hearing held on 12/16/2008 before Magistrate Judge Howard R. Lloyd (Date Filed: 12/16/2008) re 54 (Tape #FTR.) (pmc, COURT STAFF) (Date Filed: 12/16/2008) (Entered: 12/16/2008)
12/16/2008	68	ORDER by Magistrate Judge Howard R. Lloyd granting in part and denying in part 54 Motion to Compel (hrllc1, COURT STAFF) (Filed on 12/16/2008) (Entered: 12/16/2008)
12/18/2008	69	JOINT CASE MANAGEMENT STATEMENT filed by Technology Properties Limited, Alliacense Limited, HTC Corporation, HTC America, Inc., Patriot Scientific Corporation. (Coats, William) (Filed on 12/18/2008) (Entered: 12/18/2008)

12/18/2008	70	RELATED CASE ORDER. Signed by Judge Jeremy Fogel on 12/17/08. (dlm, COURT STAFF) (Filed on 12/18/2008) (Entered: 12/18/2008)
12/19/2008	71	MOTION for Reconsideration re 49 Order *Denying Motion to Dismiss, or in the alternative, to Transfer Venue* filed by Technology Properties Limited, Alliacense Limited, Patriot Scientific Corporation. (Chanana, Sushila) (Filed on 12/19/2008) (Entered: 12/19/2008)
12/19/2008	72	Declaration of Dan Leckrone *In Support of 71 Motion for Reconsideration of the Court's Order Denying Motion to Dismiss, or in the alternative, to Transfer Venue* filed byTechnology Properties Limited, Alliacense Limited, Patriot Scientific Corporation. (Chanana, Sushila) (Filed on 12/19/2008) Modified on 12/22/2008 (gm, COURT STAFF). (Entered: 12/19/2008)
12/19/2008	73	MOTION for Leave to File *Motion for Reconsideration and Notice of Motion* filed by Technology Properties Limited, Alliacense Limited, Patriot Scientific Corporation. (Chanana, Sushila) (Filed on 12/19/2008) (Entered: 12/19/2008)
12/19/2008	74	Proposed Order *Granting Defendants' 73 Motion for Leave to File Motion for Reconsideration and Granting Defendants' Motion for Reconsideration* by Technology Properties Limited, Alliacense Limited, Patriot Scientific Corporation. (Chanana, Sushila) (Filed on 12/19/2008) Modified on 12/22/2008 (gm, COURT STAFF). (Entered: 12/19/2008)
12/19/2008	76	Minute Entry: Further Case Management Conference held on 12/19/2008 before Judge Jeremy Fogel (Date Filed: 12/19/2008). Further Case Management Conference set for 1/30/2009 09:00 AM. Motion Hearing set for 1/30/2009 09:00 AM. (Court Reporter Kristen Moody.) (dlm, COURT STAFF) (Date Filed: 12/19/2008) (Entered: 12/30/2008)
12/24/2008	75	DEMAND for Trial by Jury by HTC Corporation, HTC America, Inc.. (Chen, Kyle) (Filed on 12/24/2008) (Entered: 12/24/2008)
01/06/2009	77	CLERKS NOTICE Defendants' Motion For Reconsideration is set for hearing on 1/30/2009 at 9:00 a.m. Any response to the motion is due 1/21/2009. Any reply is due 1/28/2009. (jflc2, COURT STAFF) (Filed on 1/6/2009) (Entered: 01/06/2009)
01/21/2009	78	Memorandum in Opposition re 71 MOTION for Reconsideration re 49 Order *Denying Motion to Dismiss, or in the alternative, to Transfer Venue* filed byHTC Corporation, HTC America, Inc.. (Chen, Kyle) (Filed on 1/21/2009) (Entered: 01/21/2009)
01/21/2009	79	DECLARATION of Kyle D. Chen in Opposition to 71 MOTION for Reconsideration re 49 Order *Denying Motion to Dismiss, or in the alternative, to Transfer Venue* filed byHTC Corporation, HTC America, Inc.. (Attachments: # 1 Exhibit A, # 2 Exhibit B)(Related document(s) 71) (Chen, Kyle) (Filed on 1/21/2009) (Entered: 01/21/2009)
01/28/2009	80	Reply Memorandum *DEFENDANTS REPLY IN SUPPORT OF 71 MOTION FOR RECONSIDERATION OF THE COURTS ORDER DENYING MOTION TO DISMISS, OR IN THE ALTERNATIVE, TO TRANSFER VENUE* filed byAlliacense Limited, Technology Properties Limited, Patriot Scientific Corporation. (Chanana, Sushila) (Filed on 1/28/2009) Modified on 1/29/2009 (gm, COURT STAFF). (Entered: 01/28/2009)
01/28/2009	81	*****FILED IN ERROR. PLEASE SEE DOCKET # 83 ***** Declaration *OF SUSHILA CHANANA IN SUPPORT OF DEFENDANTS 80 REPLY FOR ITS MOTION FOR RECONSIDERATION OF THE COURTS ORDER DENYING MOTION TO DISMISS, OR IN THE ALTERNATIVE, TO TRANSFER VENUE* filed byTechnology Properties Limited, Alliacense Limited, Patriot Scientific Corporation. (Chanana, Sushila) (Filed on 1/28/2009) Modified on 1/29/2009 (gm, COURT STAFF). (Entered: 01/28/2009)
01/28/2009	82	*****FILED IN ERROR. PLEASE SEE DOCKET # 83 ***** EXHIBITS re 81 Declaration in Support, *Exhibit A Transcript of CMC on December 19, 2008 in all TPL Cases* filed byTechnology Properties Limited,

		Alliacense Limited, Patriot Scientific Corporation. (Attachments: # 1 Exhibit Exhibit A Transcript of CMC on December 19, 2008 in all TPL Cases)(Related document(s) 81) (Chanana, Sushila) (Filed on 1/28/2009) Modified on 1/29/2009 (gm, COURT STAFF). (Entered: 01/28/2009)
01/28/2009	83	Declaration of Sushila Chanana *in Support of Defendants' 80 Reply for Its Motion for Reconsideration of the Court's Order Denying Motion to Dismiss, or in the Alternative, to Transfer Venue* filed byTechnology Properties Limited, Alliacense Limited, Patriot Scientific Corporation. (Attachments: # 1 Exhibit)(Chanana, Sushila) (Filed on 1/28/2009) Modified on 1/29/2009 (gm, COURT STAFF). (Entered: 01/28/2009)
01/29/2009	84	JOINT CASE MANAGEMENT STATEMENT filed by Technology Properties Limited, Alliacense Limited, HTC Corporation, HTC America, Inc., Patriot Scientific Corporation. (Chen, Kyle) (Filed on 1/29/2009) (Entered: 01/29/2009)
01/30/2009	85	Transcript of Proceedings held on December 19, 2008, before Judge Jeremy Fogel. Court Reporter/Transcriber Kristen Moody, Telephone number (408) 981−6070. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 4/27/2009. (mz, COURT STAFF) (Filed on 1/30/2009) (Entered: 01/30/2009)
01/30/2009	86	Minute Entry: Motion Hearing held on 1/30/2009 before Judge Jeremy Fogel (Date Filed: 1/30/2009) re (80 in 5:08−cv−00877−JF) MOTION for Reconsideration *of the Court's Order Denying Motion to Dismiss, or in the Alternative, to Transfer Venue* filed by Technology Properties Limited, Alliacense Limited, Patriot Scientific Corporation, (73 in 5:08−cv−00882−JF) MOTION for Leave to File *Motion for Reconsideration and Notice of Motion* filed by Technology Properties Limited, Alliacense Limited, Patriot Scientific Corporation, (52 in 5:08−cv−00877−JF) MOTION for Leave to File *First Amended Complaint* filed by Gateway, Inc., Acer America Corporation, Acer, Inc., Further Case Management Conference held on 1/30/2009 before Judge Jeremy Fogel (Date Filed: 1/30/2009). The motions are taken under submission. (Court Reporter Summer Clanton.) (dlm, COURT STAFF) (Date Filed: 1/30/2009) (Entered: 02/02/2009)
02/03/2009	87	Transcript of Proceedings held on 01/30/2009, before Judge Jeremy Fogel. Court Reporter/Transcriber Summer Clanton, Telephone number 408−288−6150. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 5/1/2009. (Clanton, Summer) (Filed on 2/3/2009) (Entered: 02/03/2009)
02/04/2009	88	ORDER by Judge Jeremy Fogel granting (81) Motion for Leave to File and denying (80) Motion for Reconsideration in case 5:08−cv−00877−JF; granting (73) Motion for Leave to File and denying (71) Motion for Reconsideration in case 5:08−cv−00882−JF (jflc1, COURT STAFF) (Filed on 2/4/2009) (Entered: 02/04/2009)
02/27/2009	89	NOTICE of Change In Counsel by Mark R. Weinstein (Weinstein, Mark) (Filed on 2/27/2009) (Entered: 02/27/2009)
02/27/2009	90	Joint MOTION re Proposed Case Schedules filed by Technology Properties Limited, Alliacense Limited, HTC Corporation, HTC America, Inc., Patriot Scientific Corporation. (Chen, Kyle) (Filed on 2/27/2009) (Entered: 02/27/2009)
02/27/2009	91	EXHIBITS re 90 Joint MOTION re Proposed Case Schedules filed byTechnology Properties Limited, Alliacense Limited, HTC Corporation, HTC America, Inc., Patriot Scientific Corporation. (Related document(s) 90) (Chen, Kyle) (Filed on 2/27/2009) (Entered: 02/27/2009)

03/02/2009	92	ORDER BY JUDGE JEREMY FOGEL GRANTING 90 JOINT MOTION REGARDING PROPOSED CASE SCHEDULES.(jflc2, COURT STAFF) (Filed on 3/2/2009) (Entered: 03/02/2009)
03/10/2009	93	MOTION Allow Disclosure of Defendants' Preliminary Infringement Contentions filed by HTC Corporation, HTC America, Inc.. Motion Hearing set for 4/14/2009 10:00 AM in Courtroom 2, 5th Floor, San Jose. (Lam, Taryn) (Filed on 3/10/2009) (Entered: 03/10/2009)
03/10/2009	94	Declaration of Taryn Lam in Support of 93 MOTION Allow Disclosure of Defendants' Preliminary Infringement Contentions filed byHTC Corporation, HTC America, Inc.. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Exhibit G, # 8 Exhibit H, # 9 Exhibit I)(Related document(s) 93) (Lam, Taryn) (Filed on 3/10/2009) (Entered: 03/10/2009)
03/10/2009	95	Proposed Order re 93 MOTION Allow Disclosure of Defendants' Preliminary Infringement Contentions by HTC Corporation, HTC America, Inc.. (Lam, Taryn) (Filed on 3/10/2009) (Entered: 03/10/2009)
03/10/2009	96	MOTION to Seal *Exhibits G−I to the Declaration of Taryn Lam* filed by HTC Corporation, HTC America, Inc.. (Attachments: # 1 Proposed Order)(Lam, Taryn) (Filed on 3/10/2009) (Entered: 03/10/2009)
03/11/2009	97	CERTIFICATE OF SERVICE by HTC Corporation, HTC America, Inc. re 96 MOTION to Seal *Exhibits G−I to the Declaration of Taryn Lam Sealed Exhibits G, H and I* (Chen, Kyle) (Filed on 3/11/2009) (Entered: 03/11/2009)
03/11/2009		Received Exhibit G FILED UNDER SEAL. (gm, COURT STAFF) (Filed on 3/11/2009) (Entered: 03/12/2009)
03/11/2009		Received Exhibit H FILED UNDER SEAL. (gm, COURT STAFF) (Filed on 3/11/2009) (Entered: 03/12/2009)
03/11/2009		Received Exhibit I FILED UNDER SEAL. (gm, COURT STAFF) (Filed on 3/11/2009) (Entered: 03/12/2009)
03/13/2009	98	NOTICE by HTC Corporation, HTC America, Inc. re 96 MOTION to Seal *Exhibits G−I to the Declaration of Taryn Lam Notice of Manual Filing of Exhibits G−I to Declaration of Taryn Lam in Support of Motion to Allow Disclosure of Defendants' Preliminary Infringement Contentions* (Lam, Taryn) (Filed on 3/13/2009) (Entered: 03/13/2009)
03/17/2009	99	Declaration of Sushila Chanana *in Support of (Proposed) Sealing Order* filed byTechnology Properties Limited, Alliacense Limited. (Attachments: # 1 Proposed Order)(Chanana, Sushila) (Filed on 3/17/2009) (Entered: 03/17/2009)
03/24/2009	100	Memorandum in Opposition re 93 MOTION Allow Disclosure of Defendants' Preliminary Infringement Contentions filed byTechnology Properties Limited, Alliacense Limited. (Ogden, Christoper) (Filed on 3/24/2009) (Entered: 03/24/2009)
03/24/2009	101	Declaration of MAC LECKRONE in Support of 100 Memorandum in Opposition *to Plaintiffs' Motion to Allow Disclosure of Defendants' Preliminary Infringement Contentions* filed byTechnology Properties Limited, Alliacense Limited. (Related document(s) 100) (Ogden, Christoper) (Filed on 3/24/2009) (Entered: 03/24/2009)
03/31/2009	102	REPLY to Response to Motion re 93 MOTION Allow Disclosure of Defendants' Preliminary Infringement Contentions filed byHTC Corporation, HTC America, Inc.. (Lam, Taryn) (Filed on 3/31/2009) (Entered: 03/31/2009)
03/31/2009	103	Declaration of Taryn Lam in Support of 102 Reply to Response to Motion *to Allow Disclosure of Defendants' Preliminary Infringement Contentions* filed byHTC Corporation, HTC America, Inc.. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E)(Related document(s) 102) (Lam, Taryn) (Filed on 3/31/2009) (Entered: 03/31/2009)
04/14/2009	104	Minute Entry: Motion Hearing held on 4/14/2009 before Magistrate Judge Howard R. Lloyd (Date Filed: 4/14/2009) re 93 (Tape #FTR.) (pmc, COURT STAFF)

		(Date Filed: 4/14/2009) (Entered: 04/14/2009)
04/15/2009	105	ORDER by Magistrate Judge Howard R. Lloyd granting 96 Motion to Seal (hrllc1, COURT STAFF) (Filed on 4/15/2009) (Entered: 04/15/2009)
04/15/2009	106	EXHIBIT G to Declaration FILED UNDER SEAL. (gm, COURT STAFF) (Filed on 4/15/2009) (Entered: 04/16/2009)
04/15/2009	107	EXHIBIT H to Declaration FILED UNDER SEAL. (gm, COURT STAFF) (Filed on 4/15/2009) (Entered: 04/16/2009)
04/15/2009	108	EXHIBIT I to Declaration FILED UNDER SEAL. (gm, COURT STAFF) (Filed on 4/15/2009) (Entered: 04/16/2009)
05/01/2009	109	MOTION to Stay *All Proceedings Pending Re−Examination of the Patent−In−Suit* filed by HTC Corporation, HTC America, Inc.. Motion Hearing set for 6/5/2009 09:00 AM in Courtroom 3, 5th Floor, San Jose. (Lam, Taryn) (Filed on 5/1/2009) (Entered: 05/01/2009)
05/01/2009	110	Declaration of Taryn Lam in Support of 109 MOTION to Stay *All Proceedings Pending Re−Examination of the Patent−In−Suit* filed byHTC Corporation, HTC America, Inc.. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Exhibit G, # 8 Exhibit H, # 9 Exhibit I−1, # 10 Exhibit I−2, # 11 Exhibit I−3, # 12 Exhibit J, # 13 Exhibit K, # 14 Exhibit L, # 15 Exhibit M, # 16 Exhibit N, # 17 Exhibit O, # 18 Exhibit P)(Related document(s) 109) (Lam, Taryn) (Filed on 5/1/2009) (Entered: 05/01/2009)
05/01/2009	111	Proposed Order re 109 MOTION to Stay *All Proceedings Pending Re−Examination of the Patent−In−Suit [Proposed] Order Granting Plaintiffs HTC Corporation and HTC America, Inc.'s Motion to Stay All Proceedings Pending Re−Examination of the Patent−In−Suit* by HTC Corporation, HTC America, Inc.. (Lam, Taryn) (Filed on 5/1/2009) (Entered: 05/01/2009)
05/01/2009	112	EXHIBITS re 110 Declaration in Support,, *Exhibit Q to Declaration of Taryn Lam* filed byHTC Corporation, HTC America, Inc.. (Related document(s) 110) (Lam, Taryn) (Filed on 5/1/2009) (Entered: 05/01/2009)
05/11/2009	113	STIPULATION Regarding Case Schedule by Technology Properties Limited, Alliacense Limited, HTC Corporation, HTC America, Inc., Patriot Scientific Corporation. (Davis, Harold) (Filed on 5/11/2009) Text modified on 5/12/2009 (bw, COURT STAFF). (Entered: 05/11/2009)
05/13/2009	114	ORDER APPROVING STIPULATION REGARDING CASE SCHEDULE. The hearing on the Motion to Stay Proceedings set for 6/5/2009 is CONTINUED to 6/12/2009 at 9:00 AM in Courtroom 3, 5th Floor, San Jose. Signed by Judge Jeremy Fogel on 5/13/2009. (jflc2, COURT STAFF) (Filed on 5/13/2009) (Entered: 05/13/2009)
05/14/2009	115	ORDER by Magistrate Judge Howard R. Lloyd granting in part and denying in part 93 Motion for disclosure of defendants' Preliminary Infringement Contentions (hrllc1, COURT STAFF) (Filed on 5/14/2009) (Entered: 05/14/2009)
05/15/2009	116	NOTICE of Appearance by Wendi Renee Schepler (Schepler, Wendi) (Filed on 5/15/2009) (Entered: 05/15/2009)
05/20/2009	117	NOTICE of Appearance by Jennifer Yokoyama *for HTC Corporation and HTC America, Inc.* (Yokoyama, Jennifer) (Filed on 5/20/2009) (Entered: 05/20/2009)
05/22/2009	118	Memorandum in Opposition re 109 MOTION to Stay *All Proceedings Pending Re−Examination of the Patent−In−Suit* filed byTechnology Properties Limited, Alliacense Limited, Patriot Scientific Corporation. (Chanana, Sushila) (Filed on 5/22/2009) (Entered: 05/22/2009)
05/22/2009	119	Declaration of Sushila Chanana in Support of 118 Memorandum in Opposition *to HTC's Motion to Stay* filed byTechnology Properties Limited, Alliacense Limited, Patriot Scientific Corporation. (Attachments: # 1 Exhibit A−G, # 2 Exhibit H, # 3 Exhibit I−O, # 4 Exhibit P, # 5 Exhibit Q−T)(Related document(s) 118) (Chanana, Sushila) (Filed on 5/22/2009) (Entered: 05/22/2009)

05/22/2009	120	Proposed Order re 118 Memorandum in Opposition, 119 Declaration in Support, by Technology Properties Limited, Alliacense Limited, Patriot Scientific Corporation. (Chanana, Sushila) (Filed on 5/22/2009) (Entered: 05/22/2009)
05/29/2009	121	Reply in support of 109 MOTION to Stay *All Proceedings Pending Re−Examination of the Patent−In−Suit* filed byHTC Corporation, HTC America, Inc.. (Lam, Taryn) (Filed on 5/29/2009) Modified on 6/1/2009 (gm, COURT STAFF). (Entered: 05/29/2009)
05/29/2009	122	Declaration of Taryn Lam *In Support of HTC Corporation and HTC America, Inc.'s 121 Reply to Motion to Stay All Proceedings Pending Reexamination of the Patents−In−Suit* filed byHTC Corporation, HTC America, Inc.. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C)(Lam, Taryn) (Filed on 5/29/2009) Modified on 6/1/2009 (gm, COURT STAFF). (Entered: 05/29/2009)
06/04/2009	123	MOTION for Extension of Time to File *Notice of Motion and Motion to Enlarge Time to File Joint Claim Construction and PreHearing Statement for Compliance with Patent L.R. 4−3* filed by HTC Corporation, HTC America, Inc.. (Lam, Taryn) (Filed on 6/4/2009) (Entered: 06/04/2009)
06/04/2009	124	Declaration of Taryn Lam in Support of 123 MOTION for Extension of Time to File *Notice of Motion and Motion to Enlarge Time to File Joint Claim Construction and PreHearing Statement for Compliance with Patent L.R. 4−3* filed byHTC Corporation, HTC America, Inc.. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C)(Related document(s) 123) (Lam, Taryn) (Filed on 6/4/2009) (Entered: 06/04/2009)
06/04/2009	125	Proposed Order re 123 MOTION for Extension of Time to File *Notice of Motion and Motion to Enlarge Time to File Joint Claim Construction and PreHearing Statement for Compliance with Patent L.R. 4−3* by HTC Corporation, HTC America, Inc.. (Lam, Taryn) (Filed on 6/4/2009) (Entered: 06/04/2009)
06/09/2009	126	Memorandum in Opposition *to HTC's 123 Motion to Enlarge Time for Compliance with Patent Local Rule 403* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Chanana, Sushila) (Filed on 6/9/2009) Modified on 6/10/2009 (gm, COURT STAFF). (Entered: 06/09/2009)
06/09/2009	127	Declaration of Sushila Chanana in Support of 126 Memorandum in Opposition *to HTC's Motion to Enlarrge Time for Compliance With patent Local Rule 4−3* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Exhibit)(Related document(s) 126) (Chanana, Sushila) (Filed on 6/9/2009) (Entered: 06/09/2009)
06/09/2009	128	Proposed Order re 126 Memorandum in Opposition *to HTC's Motion to Enlarge Time for Compliance with Patent Local Rule 4−3* by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Chanana, Sushila) (Filed on 6/9/2009) (Entered: 06/09/2009)
06/12/2009	132	Minute Entry: Motion Hearing held on 6/12/2009 before Jeremy Fogel (Date Filed: 6/12/2009) re (109 in 5:08−cv−00882−JF) MOTION to Stay *All Proceedings, (126 in 5:08−cv−00877−JF) MOTION to Stay All Proceedings, (42 in 5:08−cv−05398−JF) MOTION FOR EXEMPTION FROM ADR PROCESS. The motions to stay are taken under submission. The motion for exemption is granted. The case management conference is not held. (Court Reporter Summer Clanton.) (dlm, COURT STAFF) (Date Filed: 6/12/2009) (Entered: 06/18/2009)*
06/15/2009	129	STIPULATION *and [Proposed] Order to Continue Time for Parties to Submit Their Proposed Stipulated Protective Order* by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Chanana, Sushila) (Filed on 6/15/2009) (Entered: 06/15/2009)
06/16/2009	130	ORDER BY JUDGE JEREMY FOGEL GRANTING 123 PLAINTIFFS HTC CORPORATION AND HTC AMERICA, INC.'S MOTION TO ENLARGE TIME FOR COMPLIANCE WITH PATENT L.R. 4−3. (jflc2, COURT STAFF) (Filed on 6/16/2009) (Entered: 06/16/2009)
06/17/2009	131	ORDER GRANTING IN PART 126 &109 MOTIONS TO STAY. Signed by Judge Jeremy Fogel on 6/16/09. (jflc3, COURT STAFF) (Filed on 6/17/2009)

		(Entered: 06/17/2009)
06/22/2009	133	Transcript of Proceedings held on 06/12/2009, before Judge Jeremy Fogel. Court Reporter/Transcriber Summer Clanton, Telephone number 408−288−6150. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 9/17/2009. (Clanton, Summer) (Filed on 6/22/2009) (Entered: 06/22/2009)
09/08/2009	134	JOINT CASE MANAGEMENT STATEMENT filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Exhibit)(Chanana, Sushila) (Filed on 9/8/2009) (Entered: 09/08/2009)
09/15/2009	135	Statement re 134 Joint Case Management Statement *Defendants' Supplement* by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Exhibit US'336 Reexam − NIRC)(Chanana, Sushila) (Filed on 9/15/2009) (Entered: 09/15/2009)
09/16/2009	136	NOTICE of Substitution of Counsel by Kyle Dakai Chen (Chen, Kyle) (Filed on 9/16/2009) (Entered: 09/16/2009)
09/18/2009	137	Minute Entry: Further Case Management Conference held on 9/18/2009 before Judge Jeremy Fogel (Date Filed: 9/18/2009). Further Case Management Conference set for 11/6/2009 10:30 AM in Courtroom 3, 5th Floor, San Jose. (Court Reporter Summer Clanton.) (dlm, COURT STAFF) (Date Filed: 9/18/2009) (Entered: 09/21/2009)
09/24/2009	138	ORDER of Substitution of Counsel for Plaintiffs HTC Corporation and HTC America, Inc. re 136 . Signed by Judge Jeremy Fogel on 9/22/09. (dlm, COURT STAFF) (Filed on 9/24/2009) (Entered: 09/24/2009)
10/21/2009	139	CLERKS NOTICE Case Management Conference set for 11/6/2009 is continued to 11/13/2009 10:30 AM in Courtroom 3, 5th Floor, San Jose. (dlm, COURT STAFF) (Filed on 10/21/2009) (Entered: 10/21/2009)
11/03/2009	140	JOINT CASE MANAGEMENT STATEMENT *Second Supplemental* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Chanana, Sushila) (Filed on 11/3/2009) (Entered: 11/03/2009)
11/13/2009	142	Minute Entry: Further Case Management Conference held on 11/13/2009 before Judge Jeremy Fogel (Date Filed: 11/13/2009). Further Case Management Conference set for 2/12/2010 10:30 AM in Courtroom 3, 5th Floor, San Jose. (Court Reporter Summer Clanton.) (dlm, COURT STAFF) (Date Filed: 11/13/2009) (Entered: 11/16/2009)
11/16/2009	141	Transcript of Proceedings held on 11/13/2009, before Judge Jeremy Fogel. Court Reporter/Transcriber Summer Clanton, Telephone number 408−288−6150. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 2/11/2010. (Clanton, Summer) (Filed on 11/16/2009) (Entered: 11/16/2009)
02/05/2010	143	NOTICE by Alliacense Limited, Technology Properties Limited *Defendants' Counsel's Request to Appear Telephonically at 12 February 2010 Case Management Conference* (Attachments: # 1 Proposed Order)(Ogden, Christoper) (Filed on 2/5/2010) (Entered: 02/05/2010)
02/08/2010	144	NOTICE of Substitution of Counsel by John L. Cooper *and Notice of Withdrawal and Request for Court Approval* (Cooper, John) (Filed on 2/8/2010) (Entered: 02/08/2010)

02/08/2010	145	JOINT CASE MANAGEMENT STATEMENT filed by Alliacense Limited, Technology Properties Limited. (Cooper, John) (Filed on 2/8/2010) (Entered: 02/08/2010)
02/08/2010	146	Proposed Order re 144 Notice of Substitution of Counsel by Alliacense Limited, Technology Properties Limited. (Ogden, Christoper) (Filed on 2/8/2010) (Entered: 02/08/2010)
02/12/2010	147	Minute Entry: Motion Hearing held on 2/12/2010 before Judge Jeremy Fogel (Date Filed: 2/12/2010) re (67 in 5:08−cv−05398−JF) MOTION to Dismiss. The Court grants the motion. Further Case Management Conference held on 2/12/2010 before Judge Jeremy Fogel (Date Filed: 2/12/2010). The Court lifts the stay and adopts Acer and Barco's proposed case schedule plus 60 days. (Court Reporter Summer Clanton.) (dlm, COURT STAFF) (Date Filed: 2/12/2010) (Entered: 02/18/2010)
02/22/2010	148	ORDER FOLLOWING CASE MANAGEMENT CONFERENCE. Signed by Judge Jeremy Fogel on 2/22/2010. (jflc2, COURT STAFF) (Filed on 2/22/2010) (Entered: 02/22/2010)
02/22/2010	149	Transcript of Proceedings held on 02/12/2010, before Judge Jeremy Fogel. Court Reporter/Transcriber Summer Clanton, Telephone number 408−288−6150. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 5/24/2010. (Clanton, Summer) (Filed on 2/22/2010) (Entered: 02/22/2010)
02/23/2010	150	ORDER GRANTING REQUEST FOR WITHDRAW OF COUNSEL AND SUBSTITUTION OF COUNSEL BY DEFENDANTS TECHNOLOGY PROPERTIES LIMITED AND ALLIACENSE LIMITED re 144 Notice of Substitution of Counsel filed by Technology Properties Limited. Signed by Judge Jeremy Fogel on 2/12/10. (dlm, COURT STAFF) (Filed on 2/23/2010) (Entered: 02/23/2010)
03/15/2010	151	STIPULATION *Request to Dismiss The Second Claim of Plaintiffs' First Amended Complaint Regarding U.S. Patent No. 5,784,584 and [Proposed] Order Thereon* by Alliacense Limited, Technology Properties Limited. (Cooper, John) (Filed on 3/15/2010) (Entered: 03/15/2010)
03/30/2010	152	STIPULATION AND ORDER TO DISMISS THE SECOND CLAIM OF PLAINTIFFS' FIRST AMENDED COMPLAINT re 151 . Signed by Judge Jeremy Fogel on 3/25/10. (dlm, COURT STAFF) (Filed on 3/30/2010) (Entered: 03/30/2010)
04/13/2010	153	Proposed Order *[Proposed] Stipulated Protective Order* by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 4/13/2010) (Entered: 04/13/2010)
04/19/2010	154	NOTICE by HTC America, Inc., HTC Corporation *Plaintiffs' Administrative Request to File Under Seal (1) Plaintiffs' Motion for Order Prohibiting Improper Contact with HTC Employees by Defendants' Counsel, and (2) Declarations and Exhibits in Support Thereof* (Attachments: # 1 Proposed Order)(Chen, Kyle) (Filed on 4/19/2010) (Entered: 04/19/2010)
04/19/2010	155	MOTION for Order Prohibiting Improper Contact with HTC Employees by Defendants' Counsel filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 5/28/2010 09:00 AM in Courtroom 3, 5th Floor, San Jose. (Chen, Kyle) (Filed on 4/19/2010) (Entered: 04/19/2010)
04/19/2010	156	Brief re 155 MOTION for Order Prohibiting Improper Contact with HTC Employees by Defendants' Counsel filed byHTC America, Inc., HTC Corporation. (Related document(s) 155) (Chen, Kyle) (Filed on 4/19/2010) (Entered: 04/19/2010)
04/19/2010	157	Declaration of Kyle D. Chen in Support of 155 MOTION for Order Prohibiting Improper Contact with HTC Employees by Defendants' Counsel, 156 Brief filed byHTC America, Inc., HTC Corporation. (Related document(s) 155 , 156) (Chen,

		Kyle) (Filed on 4/19/2010) (Entered: 04/19/2010)
04/19/2010	158	Declaration of Becky Nine in Support of 155 MOTION for Order Prohibiting Improper Contact with HTC Employees by Defendants' Counsel, 156 Brief filed byHTC America, Inc., HTC Corporation. (Related document(s) 155 , 156) (Chen, Kyle) (Filed on 4/19/2010) (Entered: 04/19/2010)
04/19/2010	159	Proposed Order re 155 MOTION for Order Prohibiting Improper Contact with HTC Employees by Defendants' Counsel, 156 Brief by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 4/19/2010) (Entered: 04/19/2010)
04/19/2010	160	CERTIFICATE OF SERVICE by HTC America, Inc., HTC Corporation re 158 Declaration in Support, 156 Brief, 157 Declaration in Support, (Chen, Kyle) (Filed on 4/19/2010) (Entered: 04/19/2010)
04/19/2010		Received Memorandum in support of Motion (FILED UNDER SEAL) by HTC America, Inc., HTC Corporation. (gm, COURT STAFF) (Filed on 4/19/2010) (Entered: 04/20/2010)
04/19/2010		Received Declaration of Becky Nine (FILED UNDER SEAL) by HTC America, Inc., HTC Corporation. (gm, COURT STAFF) (Filed on 4/19/2010) (Entered: 04/20/2010)
04/19/2010		Received Declaration of Kyle Chen (FILED UNDER SEAL) by HTC America, Inc., HTC Corporation. (gm, COURT STAFF) (Filed on 4/19/2010) (Entered: 04/20/2010)
04/21/2010	161	STIPULATION AND ORDER re 153 *Stipulated Protective Order* filed by HTC America, Inc., HTC Corporation. Signed by Magistrate Judge Howard R. Lloyd on 4/21/2010. (hrllc1, COURT STAFF) (Filed on 4/21/2010) (Entered: 04/21/2010)
04/22/2010	162	Declaration of Eugene Y. Mar in Support of 154 Notice (Other), Notice (Other) *[Proposed] Sealing Order* filed byAlliacense Limited, Technology Properties Limited. (Attachments: # 1 Proposed Order)(Related document(s) 154) (Mar, Eugene) (Filed on 4/22/2010) (Entered: 04/22/2010)
04/26/2010	163	SEALING ORDER. Signed by Judge Jeremy Fogel on 4/26/2010. (jflc3, COURT STAFF) (Filed on 4/26/2010) (Entered: 04/26/2010)
04/30/2010	164	STIPULATION *and [Proposed] Amended Scheduling Order* by HTC America, Inc., HTC Corporation, Patriot Scientific Corporation, Technology Properties Limited. (Chen, Kyle) (Filed on 4/30/2010) (Entered: 04/30/2010)
05/04/2010	165	Sealed Document. (srm, COURT STAFF) (Filed on 5/4/2010) (Entered: 05/05/2010)
05/04/2010	166	Sealed Document. (srm, COURT STAFF) (Filed on 5/4/2010) (Entered: 05/05/2010)
05/04/2010	167	Sealed Document. (srm, COURT STAFF) (Filed on 5/4/2010) (Entered: 05/05/2010)
05/07/2010	168	MEMORANDUM in Opposition re 155 MOTION for Order Prohibiting Improper Contact with HTC Employees by Defendants' Counsel filed byAlliacense Limited, Technology Properties Limited. (Attachments: # 1 Proposed Order)(Related document(s) 155) (Cooper, John) (Filed on 5/7/2010) (Entered: 05/07/2010)
05/07/2010	169	Declaration of Daniel E. Leckrone in Support of 168 Memorandum in Opposition, *to HTC's Motion for Order Prohibiting Improper Contact with HTC Employees by Defendants' Counsel* filed byAlliacense Limited, Technology Properties Limited. (Attachments: # 1 Exhibit A)(Related document(s) 168) (Cooper, John) (Filed on 5/7/2010) (Entered: 05/07/2010)
05/13/2010	170	Reply to Opposition re 155 MOTION for Order Prohibiting Improper Contact with HTC Employees by Defendants' Counsel filed byHTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 5/13/2010) (Entered: 05/13/2010)
05/19/2010	171	STIPULATION AND ORDER AMENDING SCHEDULING ORDER re 164 . Signed by Judge Jeremy Fogel on 5/17/10. (dlm, COURT STAFF) (Filed on

		5/19/2010) (Entered: 05/19/2010)
05/25/2010	172	ORDER by Judge Jeremy Fogel granting (159) Motion to Relate Case Number CV−10−00816−JF (dlm, COURT STAFF) (Filed on 5/25/2010) (Entered: 05/25/2010)
05/28/2010	173	Minute Entry: Motion Hearing held on 5/28/2010 before Judge Jeremy Fogel (Date Filed: 5/28/2010) re 155 MOTION for Order Prohibiting Improper Contact. The motion is taken under submission. (Court Reporter Summer Fisher.) (dlm, COURT STAFF) (Date Filed: 5/28/2010) (Entered: 05/28/2010)
06/07/2010	174	ORDER BY JUDGE JEREMY FOGEL DENYING 155 PLAINTIFF'S MOTION FOR ORDER PROHIBITING DANIEL LECKRONE FROM CONTACTING HTC EMPLOYEES. (jflc1, COURT STAFF) (Filed on 6/7/2010) (Entered: 06/07/2010)
06/25/2010	175	CLERKS NOTICE The Motion Hearing set for 8/20/2010 is CONTINUED to 9/3/2010 at 9:00 AM in Courtroom 3, 5th Floor, San Jose. (jflc2, COURT STAFF) (Filed on 6/25/2010) (Entered: 06/25/2010)
06/25/2010	176	MOTION to Amend/Correct *MOTION FOR LEAVE TO AMEND INFRINGEMENT CONTENTIONS PURSUANT TO PATENT L.R. 3−7* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. Motion Hearing set for 9/3/2010 09:00 AM in Courtroom 3, 5th Floor, San Jose. (Mar, Eugene) (Filed on 6/25/2010) (Entered: 06/25/2010)
06/25/2010	177	Declaration of Benjamin Chiu in Support of 176 MOTION to Amend/Correct *MOTION FOR LEAVE TO AMEND INFRINGEMENT CONTENTIONS PURSUANT TO PATENT L.R. 3−7* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Related document(s) 176) (Mar, Eugene) (Filed on 6/25/2010) (Entered: 06/25/2010)
06/25/2010	178	Declaration of Eugene Y. Mar in Support of 176 MOTION to Amend/Correct *MOTION FOR LEAVE TO AMEND INFRINGEMENT CONTENTIONS PURSUANT TO PATENT L.R. 3−7* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Exhibit A, # 2 Exhibit B)(Related document(s) 176) (Mar, Eugene) (Filed on 6/25/2010) (Entered: 06/25/2010)
06/25/2010	179	Proposed Order re 176 MOTION to Amend/Correct *MOTION FOR LEAVE TO AMEND INFRINGEMENT CONTENTIONS PURSUANT TO PATENT L.R. 3−7* by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Mar, Eugene) (Filed on 6/25/2010) (Entered: 06/25/2010)
08/13/2010	180	Memorandum in Opposition re 176 MOTION to Amend/Correct *MOTION FOR LEAVE TO AMEND INFRINGEMENT CONTENTIONS PURSUANT TO PATENT L.R. 3−7* filed byHTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 8/13/2010) (Entered: 08/13/2010)
08/13/2010	181	Declaration of Kyle Chen in Support of 180 Memorandum in Opposition *to TPL's Motion for Leave to Amend Preliminary Infringement Contentions* filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Exhibit G)(Related document(s) 180) (Chen, Kyle) (Filed on 8/13/2010) (Entered: 08/13/2010)
08/20/2010	182	RESPONSE in Support re 176 MOTION to Amend/Correct *MOTION FOR LEAVE TO AMEND INFRINGEMENT CONTENTIONS PURSUANT TO PATENT L.R. 3−7* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Mar, Eugene) (Filed on 8/20/2010) (Entered: 08/20/2010)
09/03/2010	183	Minute Entry: Motion Hearing held on 9/3/2010 before Judge Jeremy Fogel (Date Filed: 9/3/2010) re (167 in 5:08−cv−00877−JF) MOTION TO AMEND INFRINGEMENT CONTENTIONS, (176 in 5:08−cv−00882−JF) MOTION TO AMEND INFRINGEMENT CONTENTIONS, (79 in 5:08−cv−05398−JF) MOTION for Attorney Fees *REGARDING UNITED STATES PATENT NO. 5,784,584, (81 in 5:08−cv−05398−JF) MOTION for Entry of Judgment REGARDING U.S. PATENT NO. 5,784,584, (90 in 5:08−cv−05398−JF) MOTION to Amend Infringement Contentions. The motions are taken under submission.*

		(Court Reporter Irene Rodriguez.) (dlm, COURT STAFF) (Date Filed: 9/3/2010) (Entered: 09/07/2010)
09/10/2010	184	ORDER (1) DENYING DEFENDANTS' MOTIONS TO AMEND INFRINGEMENT CONTENTIONS AND (2) DENYING BARCO N.V.'S EX PARTE MOTION FOR LEAVE TO FILE A SURREPLY. Signed by Judge Jeremy Fogel on 9/10/2010. (jflc2, COURT STAFF) (Filed on 9/10/2010) (Entered: 09/10/2010)
09/15/2010	185	STIPULATION *and [Proposed] Order Continuing Case Scheduling Dates* by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Mar, Eugene) (Filed on 9/15/2010) (Entered: 09/15/2010)
09/20/2010	186	STIPULATION AND ORDER CONTINUING CASE SCHEDULING DATES (approving 185 in 5:08−cv−00882−JF, 106 in 5:08−cv−05398−JF. 189 in 5:08−cv−00877−JF). Signed by Judge Jeremy Fogel on 9/20/2010. (jflc2, COURT STAFF) (Filed on 9/20/2010) (Entered: 09/20/2010)
10/21/2010	187	STIPULATION *CONTINUING SCHEDULING DATES* by Alliacense Limited, Technology Properties Limited. (Skaff, Stephanie) (Filed on 10/21/2010) (Entered: 10/21/2010)
10/26/2010	188	STIPULATION AND ORDER CONTINUING CASE SCHEDULING DATES re (192 in 5:08−cv−00877−JF), (187 in 5:08−cv−00882−JF), (108 in 5:08−cv−05398−JF). Signed by Judge Jeremy Fogel on 10/26/10. (dlm, COURT STAFF) (Filed on 10/26/2010) (Entered: 10/26/2010)
10/29/2010	189	CLAIM CONSTRUCTION STATEMENT *and Prehearing Statement [JOINT]* filed by Alliacense Limited, Technology Properties Limited. (Attachments: #1 Exhibit A, #2 Exhibit B, #3 Exhibit C, #4 Exhibit D)(Skaff, Stephanie) (Filed on 10/29/2010) (Entered: 10/29/2010)
11/02/2010	190	Administrative Motion to File Under Seal *Portions of (1) Notice of Motion and Motion to Compel Interrogatory Responses and Production of Documents; Memorandum of Points and Authorities in Support Thereof; and (2) Declaration of Eugene Y. Mar in Support of Motion to Compel Interrogatory Responses and Production of Documents* filed by Alliacense Limited, Technology Properties Limited. (Attachments: #1 Declaration, #2 Proposed Order)(Mar, Eugene) (Filed on 11/2/2010) (Entered: 11/02/2010)
11/02/2010	191	MOTION to Compel *Interrogatory Responses and Production of Documents; Memorandum of Points and Authorities in Support Thereof [REDACTED]* filed by Alliacense Limited, Technology Properties Limited. Motion Hearing set for 12/7/2010 10:00 AM in Courtroom 2, 5th Floor, San Jose. (Attachments: #1 Appendix)(Mar, Eugene) (Filed on 11/2/2010) (Entered: 11/02/2010)
11/02/2010	192	Declaration of Eugene Y. Mar in Support of 191 MOTION to Compel *Interrogatory Responses and Production of Documents; Memorandum of Points and Authorities in Support Thereof [REDACTED]* MOTION to Compel *Interrogatory Responses and Production of Documents; Memorandum of Points and Authorities in Support Thereof [REDACTED]* filed byAlliacense Limited, Technology Properties Limited. (Attachments: #1 Exhibit A, #2 Exhibit B, #3 Exhibit C, #4 Exhibit D, #5 Exhibit E)(Related document(s) 191) (Mar, Eugene) (Filed on 11/2/2010) (Entered: 11/02/2010)
11/02/2010	193	Proposed Order re 191 MOTION to Compel *Interrogatory Responses and Production of Documents; Memorandum of Points and Authorities in Support Thereof [REDACTED]* MOTION to Compel *Interrogatory Responses and Production of Documents; Memorandum of Points and Authorities in Support Thereof [REDACTED]* by Alliacense Limited, Technology Properties Limited. (Mar, Eugene) (Filed on 11/2/2010) (Entered: 11/02/2010)
11/04/2010	194	ORDER GRANTING 190 Defendants' Administrative Motion to File Under Seal. Signed by Magistrate Judge Howard R. Lloyd on 11/4/2010. (hrllc1, COURT STAFF) (Filed on 11/4/2010) (Entered: 11/04/2010)
11/04/2010	195	DOCUMENT E−FILED UNDER SEAL re 194 Order on Administrative Motion to File Under Seal *Notice of Motion and Motion to Compel Interrogatory Responses*

		and Production of Documents; Memorandum of Points and Authorities in Support Thereof by Alliacense Limited, Technology Properties Limited. (Mar, Eugene) (Filed on 11/4/2010) (Entered: 11/04/2010)
11/04/2010	196	DOCUMENT E−FILED UNDER SEAL re 194 Order on Administrative Motion to File Under Seal *Declaration of Eugene Y. Mar in Support of Motion to Compel Interrogatory Responses and Production of Documents* by Alliacense Limited, Technology Properties Limited. (Mar, Eugene) (Filed on 11/4/2010) (Entered: 11/04/2010)
11/09/2010	197	MOTION to Compel filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 12/14/2010 10:00 AM in Courtroom 2, 5th Floor, San Jose. (Chen, Kyle) (Filed on 11/9/2010) (Entered: 11/09/2010)
11/09/2010	198	Declaration of Kyle Chen in Support of 197 MOTION to Compel filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E)(Related document(s) 197) (Chen, Kyle) (Filed on 11/9/2010) (Entered: 11/09/2010)
11/10/2010	199	Proposed Order re 197 MOTION to Compel by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 11/10/2010) (Entered: 11/10/2010)
11/15/2010	200	CLERK'S NOTICE. PLEASE TAKE NOTICE THAT the hearing on Defendants' motion to compel interrogatory responses and production of documents (Docket No. 191), currently set for December 7, 2010, has been continued to **December 14, 2010 at 10:00 a.m.** in Courtroom 2, United States District Court, 280 South First Street, San Jose, California. Oral argument on Defendants' motion will be heard concurrently with oral argument on Plaintiffs' motion to compel responses to Interrogatory Nos. 3 and 4 and Requests for Production of Documents Nos. 3, 5, 6, and 8−11 (Docket No. 197). (hrllc1, COURT STAFF) (Filed on 11/15/2010) (Entered: 11/15/2010)
11/17/2010	201	MOTION to Shorten Time *Pursuant to Civil L.R. 6−3; Memorandum of Points and Authorities in Support Thereof* filed by Alliacense Limited, Technology Properties Limited. (Attachments: # 1 Proposed Order)(Mar, Eugene) (Filed on 11/17/2010) (Entered: 11/17/2010)
11/17/2010	202	Declaration of Eugene Y. Mar in Support of 201 MOTION to Shorten Time *Pursuant to Civil L.R. 6−3; Memorandum of Points and Authorities in Support Thereof* filed byAlliacense Limited, Technology Properties Limited. (Attachments: # 1 Exhibit A)(Related document(s) 201) (Mar, Eugene) (Filed on 11/17/2010) (Entered: 11/17/2010)
11/17/2010	203	MOTION to Compel *Deposition of HTC's Claim Construction Expert; Memorandum of Points and Authorities in Support Thereof* filed by Alliacense Limited, Technology Properties Limited. Motion Hearing set for 11/23/2010 10:00 AM in Courtroom 2, 5th Floor, San Jose. (Attachments: # 1 Proposed Order)(Mar, Eugene) (Filed on 11/17/2010) (Entered: 11/17/2010)
11/17/2010	204	Declaration of Eugene Y. Mar in Support of 203 MOTION to Compel *Deposition of HTC's Claim Construction Expert; Memorandum of Points and Authorities in Support Thereof* filed byAlliacense Limited, Technology Properties Limited. (Attachments: # 1 Exhibit A, # 2 Exhibit B)(Related document(s) 203) (Mar, Eugene) (Filed on 11/17/2010) (Entered: 11/17/2010)
11/18/2010	205	STIPULATION *to Consolidate and Expand Page Limits for Claim Construction Briefing* by Alliacense Limited, Technology Properties Limited. (Mar, Eugene) (Filed on 11/18/2010) (Entered: 11/18/2010)
11/19/2010	206	MOTION Administrative Relief from Claim Construction Scheduling Order filed by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 11/19/2010) (Entered: 11/19/2010)
11/19/2010	207	Declaration of Kyle Chen in Support of 206 MOTION Administrative Relief from Claim Construction Scheduling Order filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit A)(Related document(s) 206) (Chen, Kyle) (Filed on 11/19/2010) (Entered: 11/19/2010)

11/19/2010	208	Memorandum in Opposition re 201 MOTION to Shorten Time *Pursuant to Civil L.R. 6−3; Memorandum of Points and Authorities in Support Thereof* filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit A)(Chen, Kyle) (Filed on 11/19/2010) (Entered: 11/19/2010)
11/19/2010	209	Proposed Order re 206 MOTION Administrative Relief from Claim Construction Scheduling Order by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 11/19/2010) (Entered: 11/19/2010)
11/19/2010	210	CERTIFICATE OF SERVICE by HTC America, Inc., HTC Corporation re 206 MOTION Administrative Relief from Claim Construction Scheduling Order (Chen, Kyle) (Filed on 11/19/2010) (Entered: 11/19/2010)
11/19/2010	211	ORDER DENYING 201 . In light of Plaintiffs' administrative motion before Judge Fogel (Docket No. 206), this Court DENIES Defendants' motion for an order shortening time for hearing their motion to compel. Signed by Magistrate Judge Howard R. Lloyd on 11/19/2010. (hrllc1, COURT STAFF) (Filed on 11/19/2010) (Entered: 11/19/2010)
11/21/2010	212	Memorandum in Opposition re 206 MOTION Administrative Relief from Claim Construction Scheduling Order filed byAlliacense Limited, Technology Properties Limited. (Attachments: # 1 Proposed Order)(Mar, Eugene) (Filed on 11/21/2010) (Entered: 11/21/2010)
11/21/2010	213	Declaration of EUGENE Y. MAR in Support of 212 Memorandum in Opposition *to Plaintiffs' Motion for Administrative Relief from Claim Construction Scheduling Order* filed byAlliacense Limited, Technology Properties Limited. (Attachments: # 1 Exhibit A, # 2 Exhibit B)(Related document(s) 212) (Mar, Eugene) (Filed on 11/21/2010) (Entered: 11/21/2010)
11/23/2010	214	Administrative Motion to File Under Seal *Paragraphs 8−11 and Exhibits A−D of the Declaration of Eugene Y. Mar in Support of Opposition to HTC's Motion to Compel Responses to Interrogatory Nos. 3 and 4 and Requests for Production Nos. 3, 5, 6 and 8−11* filed by Alliacense Limited, Technology Properties Limited. (Attachments: # 1 Declaration, # 2 Proposed Order)(Mar, Eugene) (Filed on 11/23/2010) (Entered: 11/23/2010)
11/23/2010	215	Memorandum in Opposition re 197 MOTION to Compel *Responses to Interrogatory Nos. 3 and 4 and Requests for Production Nos. 3, 5, 6 and 8−11* filed byAlliacense Limited, Technology Properties Limited. (Attachments: # 1 Appendix, # 2 Proposed Order)(Mar, Eugene) (Filed on 11/23/2010) (Entered: 11/23/2010)
11/23/2010	216	Declaration of Eugene Y. Mar in Support of 215 Memorandum in Opposition, *[REDACTED]* filed byAlliacense Limited, Technology Properties Limited. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E)(Related document(s) 215) (Mar, Eugene) (Filed on 11/23/2010) (Entered: 11/23/2010)
11/23/2010	217	Declaration of Mac Leckrone in Support of 215 Memorandum in Opposition, filed byAlliacense Limited, Technology Properties Limited. (Attachments: # 1 Exhibit A, # 2 Exhibit B)(Related document(s) 215) (Mar, Eugene) (Filed on 11/23/2010) (Entered: 11/23/2010)
11/23/2010	218	Memorandum in Opposition re 191 MOTION to Compel *Interrogatory Responses and Production of Documents; Memorandum of Points and Authorities in Support Thereof [REDACTED]* MOTION to Compel *Interrogatory Responses and Production of Documents; Memorandum of Points and Authorities in Support Thereof [REDACTED]* filed byHTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 11/23/2010) (Entered: 11/23/2010)
11/23/2010	219	Declaration of Kyle Chen in Support of 218 Memorandum in Opposition, filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit A, # 2 Exhibit B)(Related document(s) 218) (Chen, Kyle) (Filed on 11/23/2010) (Entered: 11/23/2010)
11/23/2010	220	Declaration of Brad Lin in Support of 218 Memorandum in Opposition, filed byHTC America, Inc., HTC Corporation. (Related document(s) 218) (Chen, Kyle)

		(Filed on 11/23/2010) (Entered: 11/23/2010)
11/24/2010	221	Proposed Order re 218 Memorandum in Opposition, by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 11/24/2010) (Entered: 11/24/2010)
11/30/2010	222	Reply Memorandum re 191 MOTION to Compel *Interrogatory Responses and Production of Documents; Memorandum of Points and Authorities in Support Thereof [REDACTED]* MOTION to Compel *Interrogatory Responses and Production of Documents; Memorandum of Points and Authorities in Support Thereof [REDACTED]* filed byAlliacense Limited, Technology Properties Limited. (Mar, Eugene) (Filed on 11/30/2010) (Entered: 11/30/2010)
11/30/2010	223	Declaration of Eugene Y. Mar in Support of 222 Reply Memorandum, filed byAlliacense Limited, Technology Properties Limited. (Related document(s) 222) (Mar, Eugene) (Filed on 11/30/2010) (Entered: 11/30/2010)
11/30/2010	224	Reply to Opposition re 197 MOTION to Compel filed byHTC America, Inc., HTC Corporation. (Weinstein, Mark) (Filed on 11/30/2010) (Entered: 11/30/2010)
11/30/2010	225	Request for Judicial Notice re 224 Reply to Opposition filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit Exhibit A)(Related document(s) 224) (Weinstein, Mark) (Filed on 11/30/2010) (Entered: 11/30/2010)
12/01/2010	226	ORDER GRANTING IN PART PLAINTIFFS' MOTION 206 FOR ADMINISTRATIVE RELIEF FROM CLAIM CONSTRUCTION SCHEDULING ORDER. Signed by Judge Jeremy Fogel on December 1, 2010. (Entered: 12/01/2010)
12/02/2010	227	STIPULATION AND ORDER TO CONSOLIDATE AND EXPAND PAGE LIMITS FOR CLAIM CONSTRUCTION BRIEFING re (111 in 5:08−cv−05398−JF), (205 in 5:08−cv−00882−JF), (209 in 5:08−cv−00877−JF). Signed by Judge Jeremy Fogel on 11/23/10. (dlm, COURT STAFF) (Filed on 12/2/2010) (Entered: 12/02/2010)
12/09/2010	228	CLAIM CONSTRUCTION STATEMENT *Defendants' Opening Claim Construction Brief* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Cooper, John) (Filed on 12/9/2010) (Entered: 12/09/2010)
12/09/2010	229	Declaration of Eugene Mar in Support of 228 Claim Construction Statement filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Exhibit A through F, # 2 Exhibit G through J, # 3 Exhibit K through L)(Related document(s) 228) (Cooper, John) (Filed on 12/9/2010) (Entered: 12/09/2010)
12/09/2010	230	EXHIBITS re 229 Declaration in Support, *Exhibits M through W to Declaration of Eugene Mar in Support of Defendants' Opening Claim Construction Brief* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Exhibit P through Q, # 2 Exhibit R through W)(Related document(s) 229) (Cooper, John) (Filed on 12/9/2010) (Entered: 12/09/2010)
12/13/2010	231	MOTION for Leave to File *Supplemental Statement in Support of HTC's Opposition to Compel Third Party Documents* filed by HTC America, Inc., HTC Corporation. (Attachments: # 1 Supplement [Proposed] Supplemental Statement, # 2 Proposed Order)(Weinstein, Mark) (Filed on 12/13/2010) (Entered: 12/13/2010)
12/13/2010	232	ORDER GRANTING 214 Defendants' Administrative Motion to File Under Seal. Signed by Magistrate Judge Howard R. Lloyd on 12/13/2010. (hrllc1, COURT STAFF) (Filed on 12/13/2010) (Entered: 12/13/2010)
12/13/2010	233	ORDER DENYING 231 Plaintiffs' Request for Leave to File a Supplemental Statement. Signed by Magistrate Judge Howard R. Lloyd on 12/13/2010. (hrllc1, COURT STAFF) (Filed on 12/13/2010) (Entered: 12/13/2010)
12/14/2010	234	Minute Entry: Motion Hearing held on 12/14/2010 before Magistrate Judge Howard R. Lloyd (Date Filed: 12/14/2010) re 197 , 191 (Court Reporter FTR.) (pmc, COURT STAFF) (Date Filed: 12/14/2010) (Entered: 12/14/2010)

12/28/2010	235	MOTION for Protective Order *[Defendants Technology Property Limited and Alliacense Limited's Motion to Modify the Protective Order]* filed by Alliacense Limited, Technology Properties Limited. Motion Hearing set for 2/1/2011 10:00 AM in Courtroom 2, 5th Floor, San Jose before Magistrate Judge Howard R. Lloyd. (Attachments: #1 Proposed Order)(Joesten, Nan) (Filed on 12/28/2010) (Entered: 12/28/2010)
12/28/2010	236	Declaration of Douglas Lum in Support of 235 MOTION for Protective Order *[Defendants Technology Property Limited and Alliacense Limited's Motion to Modify the Protective Order]* MOTION for Protective Order *[Defendants Technology Property Limited and Alliacense Limited's Motion to Modify the Protective Order]* filed byAlliacense Limited, Technology Properties Limited. (Related document(s) 235) (Joesten, Nan) (Filed on 12/28/2010) (Entered: 12/28/2010)
12/28/2010	237	Declaration of Mac Lekrone in Support of 235 MOTION for Protective Order *[Defendants Technology Property Limited and Alliacense Limited's Motion to Modify the Protective Order]* MOTION for Protective Order *[Defendants Technology Property Limited and Alliacense Limited's Motion to Modify the Protective Order]* filed byAlliacense Limited, Technology Properties Limited. (Related document(s) 235) (Joesten, Nan) (Filed on 12/28/2010) (Entered: 12/28/2010)
12/28/2010	238	Declaration of Nan E. Joesten in Support of 235 MOTION for Protective Order *[Defendants Technology Property Limited and Alliacense Limited's Motion to Modify the Protective Order]* MOTION for Protective Order *[Defendants Technology Property Limited and Alliacense Limited's Motion to Modify the Protective Order]* filed byAlliacense Limited, Technology Properties Limited. (Attachments: #1 Exhibit A)(Related document(s) 235) (Joesten, Nan) (Filed on 12/28/2010) (Entered: 12/28/2010)
01/06/2011	239	Amended MOTION for Protective Order *[Defendants Technology Property Limited and Alliacense Limited's Amended Motion to Modify Protective Order]* filed by Alliacense Limited, Technology Properties Limited. Motion Hearing set for 2/15/2011 10:00 AM in Courtroom 2, 5th Floor, San Jose before Magistrate Judge Howard R. Lloyd. (Joesten, Nan) (Filed on 1/6/2011) (Entered: 01/06/2011)
01/12/2011	240	(1) ORDER DENYING 191 Defendants' Motion to Compel Interrogatory Responses and Production of Documents and (2) INTERIM ORDER RE: 197 Plaintiffs' Motion to Compel Responses to Interrogatory Nos. 3 and 4 and RFP Nos. 3, 5, 6, and 8, 11. Signed by Magistrate Judge Howard R. Lloyd on 1/12/2011. (hrllc1, COURT STAFF) (Filed on 1/12/2011) (Entered: 01/12/2011)
01/13/2011	241	DOCUMENT E−FILED UNDER SEAL re 232 Order on Administrative Motion to File Under Seal *[214−1] Declaration to Administrative Motion to file Under Seal* by Alliacense Limited, Technology Properties Limited. (Mar, Eugene) (Filed on 1/13/2011) (Entered: 01/13/2011)
01/13/2011	242	DOCUMENT E−FILED UNDER SEAL re 232 Order on Administrative Motion to File Under Seal *216 Declaration of Eugene Y Mar in Support of 215 Memorandum in Opposition re 197 Motion to Compel Responses to Interrogatory Nos. 3 and 4 and Requests forProduction Nos. 3, 4, 6 and 8−11* by Alliacense Limited, Technology Properties Limited. (Attachments: #1 Exhibit A, #2 Exhibit B−1, #3 Exhibit B−2, #4 Exhibit C, #5 Exhibit D)(Mar, Eugene) (Filed on 1/13/2011) (Entered: 01/13/2011)
01/21/2011	243	CLAIM CONSTRUCTION STATEMENT *Plaintiffs Consolidated Responsive Claim Construction Brief* filed by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 1/21/2011) (Entered: 01/21/2011)
01/21/2011	244	Declaration of Kyle Chen in Support of 243 Claim Construction Statement *Plaintiffs' Consolidated Responsive Claim Construction Brief* filed byHTC America, Inc., HTC Corporation. (Attachments: #1 Exhibit A, #2 Exhibit B, #3 Exhibit C, #4 Exhibit D, #5 Exhibit E, #6 Exhibit F, #7 Exhibit G, #8 Exhibit H, #9 Exhibit I, #10 Exhibit J, #11 Exhibit K, #12 Exhibit L, #13 Exhibit M, #14 Exhibit N, #15 Exhibit O, #16 Exhibit P, #17 Exhibit Q, #18 Exhibit R, #19 Exhibit S, #20 Exhibit T, #21 Exhibit U, #22 Exhibit V, #23 Exhibit W, #24

		Supplement X, # 25 Exhibit Y, # 26 Exhibit Z)(Related document(s) 243) (Chen, Kyle) (Filed on 1/21/2011) (Entered: 01/21/2011)
01/24/2011	245	CLAIM CONSTRUCTION STATEMENT *(CORRECTED)(Replaces Doc. 243)* filed by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 1/24/2011) (Entered: 01/24/2011)
01/25/2011	246	Administrative Motion to File Under Seal *Confidential Exhibits* filed by HTC America, Inc., HTC Corporation. (Attachments: # 1 Declaration, # 2 Proposed Order)(Chen, Kyle) (Filed on 1/25/2011) (Entered: 01/25/2011)
01/25/2011	247	Memorandum in Opposition re 235 MOTION for Protective Order *[Defendants Technology Property Limited and Alliacense Limited's Motion to Modify the Protective Order]* MOTION for Protective Order *[Defendants Technology Property Limited and Alliacense Limited's Motion to Modify the Protective Order]* filed byHTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 1/25/2011) (Entered: 01/25/2011)
01/25/2011	248	Declaration of Kyle Chen in Support of 247 Memorandum in Opposition, filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F)(Related document(s) 247) (Chen, Kyle) (Filed on 1/25/2011) (Entered: 01/25/2011)
01/26/2011	249	Memorandum in Opposition re 235 MOTION for Protective Order *[Defendants Technology Property Limited and Alliacense Limited's Motion to Modify the Protective Order]* MOTION for Protective Order *[Defendants Technology Property Limited and Alliacense Limited's Motion to Modify the Protective Order] ****[CORRECTED DOCUMENT][REPLACES Doc. No. 247]**** filed byHTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 1/26/2011) (Entered: 01/26/2011)
01/26/2011		***Hearing terminated. The 2/1/2011 hearing date on Defendants' motion to modify the protective order 235 is terminated per Defendants' amended notice of motion re−noticing their motion for hearing on 2/15/2011 239 . (hrllc1, COURT STAFF) (Filed on 1/26/2011) (Entered: 01/26/2011)
02/01/2011	250	Declaration of Mac Leckrone in Support of 246 Administrative Motion to File Under Seal *Confidential Exhibits* filed byAlliacense Limited, Technology Properties Limited. (Related document(s) 246) (Mar, Eugene) (Filed on 2/1/2011) (Entered: 02/01/2011)
02/01/2011	251	***** FILED IN ERROR. REFER TO DOCUMENT 254 . ***** Reply to Opposition re 239 Amended MOTION for Protective Order *[Defendants Technology Property Limited and Alliacense Limited's Amended Motion to Modify Protective Order]*Amended MOTION for Protective Order *[Defendants Technology Property Limited and Alliacense Limited's Amended Motion to Modify Protective Order]* filed byTechnology Properties Limited. (Joesten, Nan) (Filed on 2/1/2011) Modified on 2/2/2011 (feriab, COURT STAFF). (Entered: 02/01/2011)
02/01/2011	252	Declaration of Nan E. Joesten in Support of 254 Reply to Opposition, *to Technology Property Limited's and Alliacense Limited's Motion to Modify the Protective Order* filed byTechnology Properties Limited. (Related document(s) 254) (Joesten, Nan) (Filed on 2/1/2011) Modified on 2/2/2011 (feriab, COURT STAFF). (Entered: 02/01/2011)
02/01/2011	253	Proposed Order re 239 Amended MOTION for Protective Order *[Defendants Technology Property Limited and Alliacense Limited's Amended Motion to Modify Protective Order]*Amended MOTION for Protective Order *[Defendants Technology Property Limited and Alliacense Limited's Amended Motion to Modify Protective Order]* by Technology Properties Limited. (Joesten, Nan) (Filed on 2/1/2011) (Entered: 02/01/2011)
02/01/2011	254	Reply to Opposition re 239 Amended MOTION for Protective Order *[Defendants Technology Property Limited and Alliacense Limited's Amended Motion to Modify Protective Order]*Amended MOTION for Protective Order *[Defendants Technology Property Limited and Alliacense Limited's Amended Motion to Modify Protective Order]* filed byTechnology Properties Limited. (Joesten, Nan) (Filed on

		2/1/2011) (Entered: 02/01/2011)
02/02/2011	255	CLERK'S NOTICE. PLEASE TAKE NOTICE THAT, in view of this court's unavailability, the hearing on Defendants' motion to modify the protective order (Docket No. 235), currently set for February 15, 2011, has been **continued to March 1, 2011 at 10:00 a.m.** in Courtroom 2, United States District Court, 280 South First Street, San Jose, California. Motion Hearing set for 3/1/2011 10:00 AM in Courtroom 2, 5th Floor, San Jose before Magistrate Judge Howard R. Lloyd. (hrllc1, COURT STAFF) (Filed on 2/2/2011) (Entered: 02/02/2011)
02/08/2011	256	CERTIFICATE OF SERVICE by HTC America, Inc., HTC Corporation re 246 Administrative Motion to File Under Seal *Confidential Exhibits* (Chen, Kyle) (Filed on 2/8/2011) (Entered: 02/08/2011)
02/09/2011	257	ORDER GRANTING PLAINTIFFS' ADMINISTRATIVE MOTION 246 TO FILE CONFIDENTIAL EXHIBITS UNDER SEAL. Signed by Judge Jeremy Fogel on February 9, 2011. (jflc1, COURT STAFF) (Filed on 2/9/2011) (Entered: 02/09/2011)
02/11/2011	258	CLAIM CONSTRUCTION STATEMENT *228 CORRECTED Defendants' Opening Claim Construction Brief* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Cooper, John) (Filed on 2/11/2011) (Entered: 02/11/2011)
02/11/2011	259	Declaration of Eugene Mar in Support of 229 Declaration in Support, *[CORRECTED Declaration of Eugene Mar in Support of Defendants' Opening Claim Construction Brief]* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Related document(s) 229) (Cooper, John) (Filed on 2/11/2011) (Entered: 02/11/2011)
02/11/2011	260	Reply Memorandum *in Support of 258 Defendants' [Corrected] Claim Construction Statement* filed byAlliacense Limited, Technology Properties Limited. (Cooper, John) (Filed on 2/11/2011) (Entered: 02/11/2011)
02/11/2011	261	Declaration of Deepak Gupta in Support of 260 Reply Memorandum filed byAlliacense Limited, Technology Properties Limited. (Attachments: # 1 Exhibit 1, # 2 Exhibit 2, # 3 Exhibit 3, # 4 Exhibit 4, # 5 Exhibit 5, # 6 Exhibit 6, # 7 Exhibit 7)(Related document(s) 260) (Gupta, Deepak) (Filed on 2/11/2011) (Entered: 02/11/2011)
02/11/2011	262	STATUS REPORT *Pursuant to January 12, 2011 Order by Judge Lloyd (Doc. 240)* by HTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit A, # 2 Exhibit B)(Chen, Kyle) (Filed on 2/11/2011) (Entered: 02/11/2011)
02/16/2011	263	MOTION Requesting Case Management Conference filed by Alliacense Limited, Technology Properties Limited. (Attachments: # 1 Proposed Order)(Cooper, John) (Filed on 2/16/2011) (Entered: 02/16/2011)
02/22/2011	264	MOTION for Leave to File Surreply in Support of Plaintiffs' Consolidated Responsive Claim Construction Brief re 245 Claim Construction Statement *(Corrected)* filed by HTC America, Inc., HTC Corporation. (Attachments: # 1 Proposed Order)(Chen, Kyle) (Filed on 2/22/2011) (Entered: 02/22/2011)
02/22/2011	265	Declaration of Jas Dhillon in Support of 264 MOTION for Leave to File Surreply in Support of Plaintiffs' Consolidated Responsive Claim Construction Brief re 245 Claim Construction Statement *(Corrected)* MOTION for Leave to File Surreply in Support of Plaintiffs' Consolidated Responsive Claim Construction Brief re 245 Claim Construction Statement *(Corrected)* filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit 1, # 2 Exhibit 2)(Related document(s) 264) (Chen, Kyle) (Filed on 2/22/2011) (Entered: 02/22/2011)
02/22/2011	266	RESPONSE (re 263 MOTION Requesting Case Management Conference) *Opposition in Part to Defendants' Administrative Motion* filed byHTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 2/22/2011) (Entered: 02/22/2011)
02/23/2011	267	ORDER GRANTING DEFENDANTS' ADMINISTRATIVE MOTION FOR A CASE MANAGEMENT CONFERENCE. Signed by Judge Jeremy Fogel on February 23, 2011. (jflc1S, COURT STAFF) (Filed on 2/23/2011) (Entered:

		02/23/2011)
02/28/2011	268	RESPONSE (re 264 MOTION for Leave to File Surreply in Support of Plaintiffs' Consolidated Responsive Claim Construction Brief re 245 Claim Construction Statement *(Corrected)* MOTION for Leave to File Surreply in Support of Plaintiffs' Consolidated Responsive Claim Construction Brief re 245 Claim Construction Statement *(Corrected)*) *[Opposition to Motion]* filed byAlliacense Limited, Technology Properties Limited. (Attachments: # 1 Proposed Order Denying Plaintiffs' Administrative Motion for Leave to File Plaintiffs' Surreply Claim Construction Brief, # 2 Proposed Order Granting Plaintiffs' Administrative Motion for Leave to File Plaintiffs' Surreply Claim Construction Brief)(Cooper, John) (Filed on 2/28/2011) (Entered: 02/28/2011)
02/28/2011	269	Declaration of Nan E. Joesten in Support of 268 Opposition/Response to Motion,,, filed byAlliacense Limited, Technology Properties Limited. (Attachments: # 1 Exhibit A, # 2 Exhibit B)(Related document(s) 268) (Joesten, Nan) (Filed on 2/28/2011) (Entered: 02/28/2011)
03/01/2011	270	Minute Entry: Motion Hearing held on 3/1/2011 before Magistrate Judge Howard R. Lloyd (Date Filed: 3/1/2011) re 235 . (Court Reporter FTR.) (pmc, COURT STAFF) (Date Filed: 3/1/2011) (Entered: 03/01/2011)
03/01/2011	271	ORDER DENYING 235 Defendants' Motion to Modify the Protective Order. Signed by Magistrate Judge Howard R. Lloyd on 3/1/2011. (hrllc1, COURT STAFF) (Filed on 3/1/2011) (Entered: 03/01/2011)
03/04/2011	272	RESPONSE (re 264 MOTION for Leave to File Surreply in Support of Plaintiffs' Consolidated Responsive Claim Construction Brief re 245 Claim Construction Statement *(Corrected)* MOTION for Leave to File Surreply in Support of Plaintiffs' Consolidated Responsive Claim Construction Brief re 245 Claim Construction Statement *(Corrected)*) *** *CORRECTED [Replaces Doc. No. 268] Defendants' Opposition to Plaintiffs' Administrative Motion for Leave to File Consolidated Surreply Claim Construction Brief, and Proposed Surreply in the Alternative* filed byAlliacense Limited, Technology Properties Limited. (Cooper, John) (Filed on 3/4/2011) (Entered: 03/04/2011)
03/10/2011	273	NOTICE of Appearance by Lam Khanh Nguyen (Nguyen, Lam) (Filed on 3/10/2011) (Entered: 03/10/2011)
03/14/2011	274	CASE MANAGEMENT STATEMENT *JOINT CASE MANAGEMENT CONFERENCE STATEMENT* filed by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 3/14/2011) (Entered: 03/14/2011)
03/17/2011	275	MOTION to Amend/Correct *Defendants Notice of Motion and Motion for Leave to Amend Infringement Contentions Pursuant to Patent L.R. 3−7* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. Motion Hearing set for 4/22/2011 09:00 AM in Courtroom 3, 5th Floor, San Jose before Hon. Jeremy Fogel. (Attachments: # 1 Proposed Order)(Mar, Eugene) (Filed on 3/17/2011) (Entered: 03/17/2011)
03/17/2011	276	Declaration of Eugene Y. Mar in Support of 275 MOTION to Amend/Correct *Defendants Notice of Motion and Motion for Leave to Amend Infringement Contentions Pursuant to Patent L.R. 3−7* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F)(Related document(s) 275) (Mar, Eugene) (Filed on 3/17/2011) (Entered: 03/17/2011)
03/17/2011	277	Declaration of Dimas Brataadiredja in Support of 275 MOTION to Amend/Correct *Defendants Notice of Motion and Motion for Leave to Amend Infringement Contentions Pursuant to Patent L.R. 3−7* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Related document(s) 275) (Mar, Eugene) (Filed on 3/17/2011) (Entered: 03/17/2011)
03/18/2011	278	Minute Entry: Motion Hearing held on 3/18/2011 before Jeremy Fogel (Date Filed: 3/18/2011) re (223 in 5:08−cv−00877−JF) MOTION for Leave to File *Second Amended Complaint. The motion is taken under submission. Markman hearing set*

		for 5/10/2011 09:00 AM. (Court Reporter Summer Fisher.) (dlm, COURT STAFF) (Date Filed: 3/18/2011) (Entered: 03/22/2011)
03/23/2011	279	ORDER SCHEDULING BRIEFING FOR MOTION FOR SUMMARY JUDGMENT. Signed by Judge Jeremy Fogel on March 23, 2011. (jflc1S, COURT STAFF) (Filed on 3/23/2011) (Entered: 03/23/2011)
03/23/2011	280	MOTION for Relief from Order Scheduling Briefing for Summary Judgment filed by Alliacense Limited, Technology Properties Limited. (Attachments: # 1 Proposed Order)(Cooper, John) (Filed on 3/23/2011) (Entered: 03/23/2011)
03/24/2011	281	Transcript of Proceedings held on 03/18/2011, before Judge Jeremy Fogel. Court Reporter/Transcriber Summer Fisher, Telephone number 408−288−6150. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 6/22/2011. (Fisher, Summer) (Filed on 3/24/2011) (Entered: 03/24/2011)
03/25/2011	282	MOTION to Amend/Correct *Infringement Contentions for U.S. Patent No. 5,440,749 Pursuant to Patent L.R. 3−7* filed by Alliacense Limited, Technology Properties Limited. Motion Hearing set for 4/22/2011 09:00 AM in Courtroom 3, 5th Floor, San Jose before Hon. Jeremy Fogel. (Attachments: # 1 Proposed Order)(Cooper, John) (Filed on 3/25/2011) (Entered: 03/25/2011)
03/25/2011	283	Declaration of Dimas Brataadiredja in Support of 282 MOTION to Amend/Correct *Infringement Contentions for U.S. Patent No. 5,440,749 Pursuant to Patent L.R. 3−7* filed byAlliacense Limited, Technology Properties Limited. (Related document(s) 282) (Cooper, John) (Filed on 3/25/2011) (Entered: 03/25/2011)
03/25/2011	284	Declaration of Nan E. Joesten in Support of 282 MOTION to Amend/Correct *Infringement Contentions for U.S. Patent No. 5,440,749 Pursuant to Patent L.R. 3−7* filed byAlliacense Limited, Technology Properties Limited. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F)(Related document(s) 282) (Joesten, Nan) (Filed on 3/25/2011) (Entered: 03/25/2011)
03/25/2011	285	STIPULATION re 282 MOTION to Amend/Correct *Infringement Contentions for U.S. Patent No. 5,440,749 Pursuant to Patent L.R. 3−7*, 275 MOTION to Amend/Correct *Defendants Notice of Motion and Motion for Leave to Amend Infringement Contentions Pursuant to Patent L.R. 3−7* by Alliacense Limited, Technology Properties Limited. (Attachments: # 1 Proposed Order)(Joesten, Nan) (Filed on 3/25/2011) (Entered: 03/25/2011)
03/25/2011	286	Declaration of Nan E. Joesten in Support of 285 Stipulation, filed byAlliacense Limited, Technology Properties Limited. (Related document(s) 285) (Joesten, Nan) (Filed on 3/25/2011) (Entered: 03/25/2011)
03/28/2011	287	RESPONSE (re 280 MOTION for Relief from Order Scheduling Briefing for Summary Judgment) *Opposition to Defendants' Motion for Relief from Scheduling Order* filed byHTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 3/28/2011) (Entered: 03/28/2011)
03/31/2011	288	ORDER GRANTING STIPULATED REQUEST TO SET THE BRIEFING SCHEDULE FOR DEFENDANTS' MOTIONS FOR LEAVE TO AMEND INFRINGEMENT CONTENTIONS FOR U.S. PATENT NO. 5,440,749 AND U.S. PATENT NO. 5,530,890. Signed by Judge Jeremy Fogel on March 31, 2011. (jflc1, COURT STAFF) (Filed on 3/31/2011) (Entered: 03/31/2011)
04/05/2011	289	ORDER GRANTING PLAINTIFFS' ADMINISTRATIVE MOTION FOR LEAVE TO FILE PLAINTIFFS' CONSOLIDATED SURREPLY CLAIM CONSTRUCTION BRIEF. Signed by Judge Jeremy Fogel on April 5, 2011. (jflc1, COURT STAFF) (Filed on 4/5/2011) (Entered: 04/05/2011)
04/07/2011	290	ORDER AMENDING BRIEFING SCHEDULE. Signed by Judge Jeremy Fogel on April 7, 2011. (jflc1, COURT STAFF) (Filed on 4/7/2011) (Entered: 04/07/2011)

04/08/2011	291	RESPONSE (re 282 MOTION to Amend/Correct *Infringement Contentions for U.S. Patent No. 5,440,749 Pursuant to Patent L.R. 3−7*, 275 MOTION to Amend/Correct *Defendants Notice of Motion and Motion for Leave to Amend Infringement Contentions Pursuant to Patent L.R. 3−7*) *HTC'S OPPOSITION TO DEFENDANTS' MOTIONS FOR LEAVE TO AMEND INFRINGEMENT CONTENTIONS FOR U.S. PATENT NOS. 5,440,749 AND 5,530,890* filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Proposed Order Proposed Order)(Chen, Kyle) (Filed on 4/8/2011) (Entered: 04/08/2011)
04/08/2011	292	DECLARATION of KYLE D. CHEN in Opposition to 282 MOTION to Amend/Correct *Infringement Contentions for U.S. Patent No. 5,440,749 Pursuant to Patent L.R. 3−7*, 275 MOTION to Amend/Correct *Defendants Notice of Motion and Motion for Leave to Amend Infringement Contentions Pursuant to Patent L.R. 3−7* filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Exhibit G, # 8 Exhibit H, # 9 Exhibit I, # 10 Exhibit J, # 11 Exhibit K, # 12 Exhibit L, # 13 Exhibit M, # 14 Exhibit N, # 15 Exhibit O, # 16 Exhibit P, # 17 Exhibit Q, # 18 Exhibit R)(Related document(s) 282 , 275) (Chen, Kyle) (Filed on 4/8/2011) (Entered: 04/08/2011)
04/08/2011	293	MOTION for Summary Judgment *of Non−Infringement of U.S. Patent Nos. 5,440,749, 5,809,336 and 6,598,148* filed by HTC America, Inc., HTC Corporation. (Attachments: # 1 Proposed Order)(Chen, Kyle) (Filed on 4/8/2011) (Entered: 04/08/2011)
04/08/2011	294	Declaration of KYLE CHEN in Support of 293 MOTION for Summary Judgment *of Non−Infringement of U.S. Patent Nos. 5,440,749, 5,809,336 and 6,598,148* filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit 1, # 2 Exhibit 2, # 3 Exhibit 3, # 4 Exhibit 4, # 5 Exhibit 5, # 6 Exhibit 6)(Related document(s) 293) (Chen, Kyle) (Filed on 4/8/2011) (Entered: 04/08/2011)
04/09/2011	295	Administrative Motion to File Under Seal *Exhibits 3−5 to Chen Declaration iso Motion for Summary Judgment* filed by HTC America, Inc., HTC Corporation. (Attachments: # 1 Proposed Order, # 2 Affidavit)(Chen, Kyle) (Filed on 4/9/2011) (Entered: 04/09/2011)
04/14/2011	296	Declaration of Mac Leckrone in Support of 295 Administrative Motion to File Under Seal *Exhibits 3−5 to Chen Declaration iso Motion for Summary Judgment* filed byAlliacense Limited, Technology Properties Limited. (Related document(s) 295) (Mar, Eugene) (Filed on 4/14/2011) (Entered: 04/14/2011)
04/15/2011	297	REPLY (re 282 MOTION to Amend/Correct *Infringement Contentions for U.S. Patent No. 5,440,749 Pursuant to Patent L.R. 3−7*, 275 MOTION to Amend/Correct *Defendants Notice of Motion and Motion for Leave to Amend Infringement Contentions Pursuant to Patent L.R. 3−7*) *Defendants' Consolidated Reply in Support of Defendants' Motions to Amend Infringement Contentions for U.S. Patent Nos. 5,440,749 (Dkt. No. 282) and 5,530,890 (Dkt. No. 275)* filed byAlliacense Limited, Technology Properties Limited. (Cooper, John) (Filed on 4/15/2011) (Entered: 04/15/2011)
04/15/2011	298	Declaration of Eugene Y. Mar in Support of 297 Reply to Opposition/Response,, *Defendants' Consolidated Reply in Support of Defendants' Motions to Amend Infringement Contentions for U.S. Patent Nos. 5,530,890 (Dkt. No. 275) and 5,440,749 (Dkt. No. 282)* filed byAlliacense Limited, Technology Properties Limited. (Attachments: # 1 Exhibit A, # 2 Exhibit B)(Related document(s) 297) (Mar, Eugene) (Filed on 4/15/2011) (Entered: 04/15/2011)
04/20/2011	299	ORDER GRANTING ADMINISTRATIVE MOTION 295 TO SEAL. Signed by Judge Jeremy Fogel on April 20, 2011. (jflc1, COURT STAFF) (Filed on 4/20/2011) (Entered: 04/20/2011)
04/22/2011	306	Minute Entry: Motion Hearing held on 4/22/2011 before Judge Jeremy Fogel (Date Filed: 4/22/2011) re (282 in 5:08−cv−00882−JF) MOTION to Amend/Correct *Infringement Contentions for U.S. Patent No. 5,440,749 Pursuant to Patent L.R. 3−7* filed by Technology Properties Limited, Alliacense Limited, (178 in 5:08−cv−05398−JF) MOTION to Amend/Correct *Infringement Contentions for U.S. Patent No. 5,440,749 Pursuant to Patent L.R. 3−6* filed by Technology

		Properties Ltd., Alliacense Ltd, (159 in 5:08−cv−05398−JF) MOTION to Amend/Correct *Barcos First Amended Invalidity Contentions (REDACTED)* MOTION to Amend/Correct *Barcos First Amended Invalidity Contentions (REDACTED)* filed by Barco NV, (258 in 5:08−cv−00877−JF) MOTION to Amend/Correct *Infringement Contentions for U.S. Patent No. 5,440,749 Pursuant to Patent L.R. 3−7* filed by Technology Properties Limited, Alliacense Limited, (275 in 5:08−cv−00882−JF) MOTION to Amend/Correct *Defendants Notice of Motion and Motion for Leave to Amend Infringement Contentions Pursuant to Patent L.R. 3−7* filed by Technology Properties Limited, Alliacense Limited, Patriot Scientific Corporation, (249 in 5:08−cv−00877−JF) MOTION to Amend/Correct *Defendants Notice of Motion and Motion for Leave to Amend Infringement Contentions Pursuant to Patent L.R. 3−7* filed by Technology Properties Limited, Alliacense Limited, Patriot Scientific Corporation, (173 in 5:08−cv−05398−JF) MOTION to Amend/Correct *DEFENDANTS NOTICE OF MOTION AND MOTION FOR LEAVE TO AMEND INFRINGEMENT CONTENTIONS FOR U.S. PATENT NO. 5,530,890 PURSUANT TO PATENT L.R. 3−6* filed by Technology Properties Ltd., Alliacense Ltd. The motions are taken under submission. (Court Reporter Summer Fisher.) (dlm, COURT STAFF) (Date Filed: 4/22/2011) (Entered: 04/28/2011)
04/26/2011	300	Administrative Motion to File Under Seal *Portions of Defendants' Opposition to HTC's Motion for Summary Judgment* filed by Alliacense Limited, Technology Properties Limited. (Attachments: # 1 Proposed Order, # 2 Declaration)(Mar, Eugene) (Filed on 4/26/2011) (Entered: 04/26/2011)
04/26/2011	301	RESPONSE (re 293 MOTION for Summary Judgment *of Non−Infringement of U.S. Patent Nos. 5,440,749, 5,809,336 and 6,598,148*) *[REDACTED]* filed byAlliacense Limited, Technology Properties Limited. (Cooper, John) (Filed on 4/26/2011) (Entered: 04/26/2011)
04/26/2011	302	Declaration of Dr. Vojin Oklobdzija in Support of 301 Opposition/Response to Motion filed byAlliacense Limited, Technology Properties Limited. (Related document(s) 301) (Cooper, John) (Filed on 4/26/2011) (Entered: 04/26/2011)
04/26/2011	303	Declaration of Eugene Y. Mar in Support of 301 Opposition/Response to Motion filed byAlliacense Limited, Technology Properties Limited. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit D, # 4 Exhibit E, # 5 Exhibit F, # 6 Exhibit G (part 1), # 7 Exhibit G (part 2), # 8 Exhibit H, # 9 Exhibit I, # 10 Exhibit J, # 11 Exhibit K, # 12 Exhibit L, # 13 Exhibit M)(Related document(s) 301) (Mar, Eugene) (Filed on 4/26/2011) (Entered: 04/26/2011)
04/28/2011	304	Statement *JOINT STATEMENT REQUESTING ORDER ON CLAIM TERMS TO BE CONSTRUED* by Alliacense Limited, HTC America, Inc., HTC Corporation, Patriot Scientific Corporation, Technology Properties Limited. (Cooper, John) (Filed on 4/28/2011) (Entered: 04/28/2011)
04/28/2011	305	Declaration of Nan E. Joesten in Support of 304 Statement *DECLARATION OF NAN E. JOESTEN IN SUPPORT OF JOINT STATEMENT REQUESTING ORDER ON CLAIM TERMS TO BE CONSTRUED* filed byAlliacense Limited, Technology Properties Limited. (Attachments: # 1 Exhibit A)(Related document(s) 304) (Joesten, Nan) (Filed on 4/28/2011) (Entered: 04/28/2011)
04/28/2011	307	ORDER VACATING MARKMAN HEARING. Signed by Judge Jeremy Fogel on April 28, 2011. (jflc3, COURT STAFF) (Filed on 4/28/2011) (Entered: 04/28/2011)
04/28/2011		***Deadlines terminated. Markman Hearing previously set for 5/10/2011 VACATED pursuant to Order issued 4/28/2011. (jflc2, COURT STAFF) (Filed on 4/28/2011) (Entered: 05/04/2011)
05/03/2011	308	CLAIM CONSTRUCTION STATEMENT *Plaintiffs' Consolidated Sur−Reply Claim Construction Brief Pursuant to Court's Order Issued on 4/5/2011 (Doc. No. 289)* filed by HTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit Declaration of Dr. Andrew Wolfe in Support of Plaintiffs' Surreply)(Chen, Kyle) (Filed on 5/3/2011) (Entered: 05/03/2011)

05/03/2011	309	REPLY (re 293 MOTION for Summary Judgment *of Non−Infringement of U.S. Patent Nos. 5,440,749, 5,809,336 and 6,598,148*) filed byHTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 5/3/2011) (Entered: 05/03/2011)
05/03/2011	310	Declaration of Kyle Chen in Support of 309 Reply to Opposition/Response *to 293 HTCS Motion For Summary Judgment of Noninfringement of U.S. Patent Nos. 5,440,749, 5,809,336 And 6,598,148* filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit 7)(Related document(s) 309) (Chen, Kyle) (Filed on 5/3/2011) (Entered: 05/03/2011)
05/12/2011	311	STIPULATION *[Proposed] Stipulated Supplemental Protective Order Governing Discovery from Non−Party Qualcomm, Inc.* by Alliacense Limited, Technology Properties Limited. (Mar, Eugene) (Filed on 5/12/2011) (Entered: 05/12/2011)
05/13/2011	312	ORDER GRANTING IN PART AND DENYING IN PART DEFENDANTS' MOTIONS TO AMEND INFRINGEMENT CONTENTIONS. Signed by Judge Jeremy Fogel on May 13, 2011. (jflc1, COURT STAFF) (Filed on 5/13/2011) (Entered: 05/13/2011)
05/17/2011	313	STIPULATED SUPPLEMENTAL PROTECTIVE ORDER GOVERNING DISCOVERY FROM NON−PARTY QUALCOMM, INC. re 311 . Signed by Magistrate Judge Howard R. Lloyd on 5/17/2011. (hrllc1, COURT STAFF) (Filed on 5/17/2011) (Entered: 05/17/2011)
05/27/2011	314	ORDER GRANTING 300 TECHNOLOGY PROPERTIES LTD.'S AND ALLIACENSE LTD.'S ADMINISTRATIVE MOTION TO SEAL. Signed by Judge Jeremy Fogel on 5/16/2011. (jflc2, COURT STAFF) (Filed on 5/27/2011) (Entered: 05/28/2011)
06/20/2011	315	CLERKS NOTICE−RE TIME CHANGE Case Management Conference set for 6/24/2011 will be heard at 02:30 PM in Courtroom 3, 5th Floor, San Jose. (dlm, COURT STAFF) (Filed on 6/20/2011) (Entered: 06/20/2011)
06/21/2011	316	JOINT CASE MANAGEMENT STATEMENT filed by Alliacense Limited, HTC America, Inc., HTC Corporation, Patriot Scientific Corporation, Technology Properties Limited. (Davis, Harold) (Filed on 6/21/2011) (Entered: 06/21/2011)
06/24/2011	318	Minute Entry: Further Case Management Conference held on 6/24/2011 before Judge Jeremy Fogel (Date Filed: 6/24/2011). Markman hearing set for 11/14/2011 09:00 AM. (Court Reporter Summer Fisher.) (dlm, COURT STAFF) (Date Filed: 6/24/2011) (Entered: 07/05/2011)
06/27/2011	317	Declaration of Douglas Lum in Support of 236 Declaration in Support, *Amended Declaration of Douglas Lum in Support of Defendants Technology Properties Limited and Alliacense Limited's Motion to Modify the Protective Order* filed byAlliacense Limited, Technology Properties Limited. (Related document(s) 236) (Joesten, Nan) (Filed on 6/27/2011) (Entered: 06/27/2011)
08/23/2011	319	CLAIM CONSTRUCTION STATEMENT *and Prehearing Statement Under Patent Local Rule 3−4* filed by Alliacense Limited, Technology Properties Limited. (Attachments: # 1 Exhibit A)(Cooper, John) (Filed on 8/23/2011) (Entered: 08/23/2011)
09/01/2011	320	ORDER REASSIGNING CASE. Case reassigned to Judge Hon. James Ware for all further proceedings. Judge Hon. Jeremy Fogel no longer assigned to the case. Signed by Executive Committee on 09/01/11. (mab, COURT STAFF) (Filed on 9/1/2011) (Entered: 09/01/2011)
09/08/2011	321	CASE MANAGEMENT SCHEDULING ORDER: Case Management Statement due by 9/23/2011. Case Management Conference set for 10/3/2011 10:00 AM.. Signed by Judge James Ware on 9/8/2011. (tlS, COURT STAFF) (Filed on 9/8/2011) (Entered: 09/08/2011)
09/13/2011	322	ORDER RE: DISCOVERY REFERRAL Status Report due by 9/23/2011. Signed by Judge James Ware on 9/13/11. (sis, COURT STAFF) (Filed on 9/13/2011) (Entered: 09/13/2011)

09/20/2011	323	NOTICE by HTC America, Inc., HTC Corporation *CERTIFICATE OF SERVICE RE STANDING ORDER REGARDING CASE MANAGEMENT IN CIVIL CASES* (Chen, Kyle) (Filed on 9/20/2011) (Entered: 09/20/2011)
09/26/2011	324	JOINT CASE MANAGEMENT STATEMENT filed by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 9/26/2011) (Entered: 09/26/2011)
09/29/2011	325	CLERKS NOTICE RESCHEDULING TIME OF CASE MANAGEMENT CONFERENCE Case Management Conference set for 10/3/2011 11:00 AM in Courtroom 9, 19th Floor, San Francisco. (sis, COURT STAFF) (Filed on 9/29/2011) (Entered: 09/29/2011)
10/03/2011	326	Minute Entry: Further Case Management Conference held on 10/3/2011 before James Ware (Date Filed: 10/3/2011). Case Management Statement due by 2/17/2012. Further Case Management Conference set for 2/27/2012 11:00 AM in Courtroom 9, 19th Floor, San Francisco. Claims Construction Hearing set for 1/27/2012 09:00 AM. Motion Hearing set for 2/27/2012 09:00 AM in Courtroom 9, 19th Floor, San Francisco before Hon. James Ware. Tutorial Hearing set for 1/20/2012 09:00 AM in Courtroom 9, 19th Floor, San Francisco. (Court Reporter N/A.) (sis, COURT STAFF) (Date Filed: 10/3/2011) (Entered: 10/04/2011)
10/05/2011	327	FIRST PATENT SCHEDULING ORDER; NOTICE OF INTENT TO APPOINT A SPECIAL MASTER. Signed by Judge James Ware on 10/5/11. (sis, COURT STAFF) (Filed on 10/5/2011) (Entered: 10/05/2011)
11/09/2011	328	NOTICE of Substitution of Counsel by John L. Cooper *NOTICE OF WITHDRAWAL AND SUBSTITUTION OF COUNSEL BY DEFENDANTS TECHNOLOGY PROPERTIES LIMITED AND ALLIACENSE LIMITED AND [PROPOSED] ORDER* (Cooper, John) (Filed on 11/9/2011) (Entered: 11/09/2011)
11/15/2011	329	NOTICE of Appearance by James Carl Otteson *Notice of Appearance of James C. Otteson on Behalf of Defendants Technology Properties Limited and Alliacense Limited* (Otteson, James) (Filed on 11/15/2011) (Entered: 11/15/2011)
11/16/2011	330	NOTICE OF MOTION AND EXPEDITED MOTION FOR RELIEF FROM FIRST PATENT SCHEDULING ORDER UNDER CIVIL LOCAL RULE 6−3; MEMORANDUM IN SUPPORT by Alliacense Limited, Technology Properties Limited (Attachments: #1 Declaration DECLARATION OF JAMES C. OTTESON IN SUPPORT OF EXPEDITED RELIEF FROM FIRST PATENT SCHEDULING ORDER, #2 Proposed Order [PROPOSED] SECOND PATENT SCHEDULING ORDER)(Otteson, James) (Filed on 11/16/2011) Modified on 11/17/2011 (far, COURT STAFF). (Entered: 11/16/2011)
11/16/2011	331	STIPULATION AND ORDER re (229 in 3:08−cv−05398−JW) Notice of Substitution of Counsel filed by Technology Properties Ltd., Alliacense Ltd. Signed by Judge James Ware on 11/16/11. (sis, COURT STAFF) (Filed on 11/16/2011) (Entered: 11/16/2011)
11/17/2011	332	RESPONSE to re 330 Notice (Other), Notice (Other) *Opposition to Defendants' Motion for Relief from First Patent Scheduling Order* by HTC America, Inc., HTC Corporation. (Davis, Harold) (Filed on 11/17/2011) (Entered: 11/17/2011)
11/17/2011	333	NOTICE of Appearance by Michelle Gail Breit *Notice of Appearance of Michelle G. Breit on Behalf of Defendants Technology Properties Limited and Alliacense Limited* (Breit, Michelle) (Filed on 11/17/2011) (Entered: 11/17/2011)
11/18/2011	334	CLAIM CONSTRUCTION STATEMENT *Amended Patent Local Rule 4−3 Joint Claim Construction and Prehearing Statement* filed by HTC America, Inc., HTC Corporation. (Attachments: #1 Exhibit A, #2 Exhibit B, #3 Exhibit C, #4 Exhibit D, #5 Exhibit E)(Chen, Kyle) (Filed on 11/18/2011) (Entered: 11/18/2011)
11/22/2011	335	ORDER denying defendants' motion to extend time; continuing case tutorial to January 26, 2012 by Judge James Ware in case 3:08−cv−00877−JW; denying (330) Motion in case 3:08−cv−00882−JW; denying (231) Motion in case 3:08−cv−05398−JW (jwlc2, COURT STAFF) (Filed on 11/22/2011) (Entered: 11/22/2011)

11/23/2011	336	CLAIM CONSTRUCTION STATEMENT *(Corrected)* filed by Alliacense Limited, Technology Properties Limited. (Otteson, James) (Filed on 11/23/2011) (Entered: 11/23/2011)
12/19/2011	337	NOTICE of Appearance by Brandon D. Baum *on behalf of Defendants Technology Properties Limited and Alliacense Limited* (Baum, Brandon) (Filed on 12/19/2011) (Entered: 12/19/2011)
12/19/2011	338	NOTICE of intent to appoint a technical advisor. Signed by Judge James Ware on December 19, 2011. (Attachments: # 1 Resume of Technical Advisor, Kwan Chan)(jwlc2, COURT STAFF) (Filed on 12/19/2011) (Entered: 12/19/2011)
12/23/2011	339	CLAIM CONSTRUCTION STATEMENT *Defendants' Opening Claim Construction Brief for The "Top Ten" Terms* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Declaration Declaration of James C. Otteson In Support of Defendants' Opening Claim Construction Brief for the "Top Ten" Terms, # 2 Exhibit Exhibit X to Otteson Declaration, # 3 Exhibit Exhibit Y to Otteson Declaration, # 4 Exhibit Exhibit Z to Otteson Declaration, # 5 Exhibit Exhibit AA to Otteson Declaration, # 6 Exhibit Exhibit BB to Otteson Declaration, # 7 Exhibit Exhibit CC to Otteson Declaration, # 8 Exhibit Exhibit DD to Otteson Declaration)(Otteson, James) (Filed on 12/23/2011) (Entered: 12/23/2011)
12/23/2011	340	Proposed Jury Instructions by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited *[Proposed] Jury Instructions Incorporating Defendants' Claim Constructions*. (Otteson, James) (Filed on 12/23/2011) (Entered: 12/23/2011)
12/27/2011	341	ORDER by Judge James Ware in case 3:08−cv−00877−JW; granting (241) Administrative Motion to File Under Seal in case 3:08−cv−05398−JW (sis, COURT STAFF) (Filed on 12/27/2011) (Entered: 12/27/2011)
01/05/2012	342	STIPULATION *TO CONSOLIDATE AND EXPAND PAGE LIMITS FOR CLAIM CONSTRUCTION BRIEFING* by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 1/5/2012) (Entered: 01/05/2012)
01/05/2012	343	STIPULATION AND ORDER re (313 in 3:08−cv−00877−JW) Stipulation filed by Gateway, Inc., Acer America Corporation, Acer, Inc. Signed by Judge James Ware on 1/5/12. (sis, COURT STAFF) (Filed on 1/5/2012) (Entered: 01/05/2012)
01/06/2012	344	CLAIM CONSTRUCTION STATEMENT *Plaintiffs' Consolidated Responsive Claim Construction Brief* filed by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 1/6/2012) (Entered: 01/06/2012)
01/06/2012	345	Declaration of Kyle D. Chen in Support of 344 Claim Construction Statement *Declaration of Kyle D. Chen in Support of Plaintiffs' Consolidated Responsive Claim Construction Brief* filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit 1, # 2 Exhibit 2, # 3 Exhibit 3, # 4 Exhibit 4, # 5 Exhibit 5, # 6 Exhibit 6, # 7 Exhibit 7, # 8 Exhibit 8, # 9 Exhibit 9, # 10 Exhibit 10, # 11 Exhibit 11)(Related document(s) 344) (Chen, Kyle) (Filed on 1/6/2012) (Entered: 01/06/2012)
01/06/2012	346	EXHIBITS re 345 Declaration in Support,, filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit 13, # 2 Exhibit 14, # 3 Exhibit 15, # 4 Exhibit 16, # 5 Exhibit 17, # 6 Exhibit 18, Part 1 of 2, # 7 Exhibit 18, Part 2 of 2, # 8 Exhibit 19, # 9 Exhibit 20, # 10 Exhibit 21, # 11 Exhibit 22)(Related document(s) 345) (Chen, Kyle) (Filed on 1/6/2012) (Entered: 01/06/2012)
01/06/2012	347	Proposed Jury Instructions by HTC America, Inc., HTC Corporation *[Proposed] Jury Instructions Incorporating Plaintiffs' Claim Constructions*. (Chen, Kyle) (Filed on 1/6/2012) (Entered: 01/06/2012)
01/07/2012	348	Administrative Motion to File Under Seal *Plaintiffs' Administrative Motion to File Confidential Exhibits Under Seal* filed by HTC America, Inc., HTC Corporation. (Attachments: # 1 Declaration, # 2 Proposed Order)(Chen, Kyle) (Filed on 1/7/2012) (Entered: 01/07/2012)

01/09/2012	349	CLAIM CONSTRUCTION STATEMENT **CORRECTED* Plaintiffs' Consolidated Responsive Claim Construction Brief* filed by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 1/9/2012) (Entered: 01/09/2012)
01/11/2012	350	ORDER appointing technical advisor. Signed by Judge James Ware on January 11, 2012. (jwlc2, COURT STAFF) (Filed on 1/11/2012) (Entered: 01/11/2012)
01/17/2012	351	CLAIM CONSTRUCTION STATEMENT *(DEFENDANTS' REPLY CLAIM CONSTRUCTION BRIEF FOR THE "TOP TEN" TERMS)* filed by Patriot Scientific Corporation, Technology Properties Limited. (Otteson, James) (Filed on 1/17/2012) (Entered: 01/17/2012)
01/17/2012	352	Declaration of JAMES C. OTTESON in Support of 351 Claim Construction Statement *(IN SUPPORT OF DEFENDANTS' REPLY CLAIM CONSTRUCTION BRIEF FOR THE "TOP TEN" TERMS)* filed byPatriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Exhibit EE, # 2 Exhibit FF, # 3 Exhibit GG, # 4 Exhibit HH)(Related document(s) 351) (Otteson, James) (Filed on 1/17/2012) (Entered: 01/17/2012)
01/17/2012	353	Declaration of BRANDON BAUM *UNDER GENERAL ORDER NO. 45 REGARDING ELECTRONIC FILING OF DEFENDANTS REPLY CLAIM CONSTRUCTION PAPERS* filed byPatriot Scientific Corporation, Technology Properties Limited. (Otteson, James) (Filed on 1/17/2012) (Entered: 01/17/2012)
01/23/2012	354	Proposed Order *re Plaintiffs' Joint Motion for Order Permitting Use of Equipment During Court Hearing* by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 1/23/2012) (Entered: 01/23/2012)
01/24/2012	355	STIPULATION AND ORDER re 354 Proposed Order filed by HTC America, Inc., HTC Corporation. Signed by Judge James Ware on 1/24/12. (sis, COURT STAFF) (Filed on 1/24/2012) (Entered: 01/24/2012)
01/26/2012	356	Minute Entry: Tutorial Hearing held on 1/26/2012 before James Ware (Date Filed: 1/26/2012). (Court Reporter N/A.) (sis, COURT STAFF) (Date Filed: 1/26/2012) (Entered: 01/26/2012)
01/27/2012	357	Minute Entry: Claims Construction / Markman Hearing held on 1/27/2012 before James Ware (Date Filed: 1/27/2012). (Court Reporter Connie Kuhl.) (sis, COURT STAFF) (Date Filed: 1/27/2012) (Entered: 01/27/2012)
02/13/2012	358	ORDER REFERRING MOTION TO SPECIAL MASTER; VACATING FURTHER CASE MANAGEMENT CONFERENCE re (238 in 3:08−cv−05398−JW) MOTION to Strike *PORTIONS OF TPLS INFRINGEMENT CONTENTIONS* filed by Barco NV. Signed by Judge James Ware on 2/13/12. (sis, COURT STAFF) (Filed on 2/13/2012) (Entered: 02/13/2012)
03/14/2012	359	ORDER by Judge James Ware granting 348 Administrative Motion to File Under Seal (sis, COURT STAFF) (Filed on 3/14/2012) (Entered: 03/14/2012)
03/19/2012	360	DOCUMENT E−FILED UNDER SEAL re 359 Order on Administrative Motion to File Under Seal *Exhibit 7 to Declaration of Kyle D. Chen in Support of Plaintiffs' Consolidated Responsive Claim Construction Brief* by HTC America, Inc., HTC Corporation. (Attachments: # 1 Ex. 7 − Part 2, # 2 Ex. 7 − Part 3, # 3 Ex. 7 − Part 4)(Chen, Kyle) (Filed on 3/19/2012) (Entered: 03/19/2012)
03/26/2012	361	ORDER by Judge James Ware denying 293 Motion for Summary Judgment as premature (jwlc2, COURT STAFF) (Filed on 3/26/2012) (Entered: 03/26/2012)
06/07/2012	362	MOTION for leave to appear in Pro Hac Vice *(James R. Farmer)* (Filing fee $ 305, receipt number 0971−6877707.) filed by Alliacense Limited, Technology Properties Limited. (Attachments: # 1 Proposed Order)(Farmer, James) (Filed on 6/7/2012) (Entered: 06/07/2012)
06/12/2012	363	ORDER GRANTING ADMISSION OF ATTORNEY FARMER PRO HAC VICE by Chief Judge James Ware, granting 362 Motion for Pro Hac Vice. (wsn, COURT STAFF) (Filed on 6/12/2012) (Entered: 06/12/2012)
06/12/2012	364	FIRST CLAIM CONSTRUCTION ORDER. Signed by Judge James Ware on June 12, 2012. (jwlc1, COURT STAFF) (Filed on 6/12/2012) (Entered: 06/12/2012)

07/02/2012	365	STIPULATION re 364 Order *on Further Claim Construction* filed by Alliacense Limited, HTC America, Inc., HTC Corporation, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Exhibit A, # 2 Exhibit B)(Baum, Brandon) (Filed on 7/2/2012) (Entered: 07/02/2012)
08/02/2012	366	ORDER REQUIRING PARTIES TO PROVIDE NOTICE RE. REASSIGNMENT TO MAGISTRATE JUDGE GREWAL. Joint Statement due by 8/6/2012. Signed by Chief Judge James Ware on August 2, 2012. (wsn, COURT STAFF) (Filed on 8/2/2012) (Entered: 08/02/2012)
08/06/2012	367	Statement re 366 Order, Set Deadlines/Hearings *Supplemental Statement of Joint Consent to Magistrate Judge Grewal* by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 8/6/2012) (Entered: 08/06/2012)
08/08/2012	368	ORDER by Judge James Ware denying (318) Administrative Motion to File Under Seal in case 3:08−cv−00877−JW (jwlc2, COURT STAFF) (Filed on 8/8/2012) (Entered: 08/08/2012)
08/14/2012	369	CONSENT/DECLINATION to Proceed Before a US Magistrate Judge by HTC America, Inc., HTC Corporation.. (Chen, Kyle) (Filed on 8/14/2012) (Entered: 08/14/2012)
08/15/2012	370	ORDER REASSIGNING CASE. Case reassigned to Judge Magistrate Judge Paul Singh Grewal for all further proceedings. Hon. James Ware no longer assigned to the case. Signed by Executive Committee on 8/15/12. (sv, COURT STAFF) (Filed on 8/15/2012) (Entered: 08/15/2012)
08/15/2012	371	CLERK'S NOTICE SETTING CASE MANAGEMENT CONFERENCE FOLLOWING REASSIGNMENT: Case Management Conference set for 8/28/2012 at 02:00 PM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul S. Grewal. Case Management Statement due by 8/21/2012. *****This is a text only docket entry, there is no document associated with this notice.***** (ofr, COURT STAFF) (Filed on 8/15/2012) (Entered: 08/15/2012)
08/20/2012	372	STIPULATION WITH PROPOSED ORDER *Stipulation to Defer Case Management Conference Currently Set For August 28, 2012 to September 4, 2012* filed by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 8/20/2012) (Entered: 08/20/2012)
08/21/2012	373	STIPULATION TO DEFER CASE MANAGEMENT CONFERENCE CURRENTLY SET FOR AUGUST 28, 2012 TO SEPTEMBER 4, 2012, granting (372 in 5:08−cv−00882−PSG), (288 in 5:08−cv−05398−PSG) and (343 in 5:08−cv−00877−PSG) Stipulation filed by Gateway, Inc., Acer America Corporation, Acer, Inc. 8/28/2012 Case Management Conference continued to 9/4/2012 at 02:00 PM in Courtroom 5, 4th Floor, San Jose. Case Management Statement to be submitted no later than 8/28/2012. Signed by Judge Paul S. Grewal on 8/21/2012. (ofr, COURT STAFF) (Filed on 8/21/2012) (Entered: 08/21/2012)
08/21/2012	374	ORDER NUNC PRO TUNC TERMINATING APPOINTMENT OF TECHNICAL ADVISOR. Signed by Chief Judge James Ware on August 21, 2012. (wsn, COURT STAFF) (Filed on 8/21/2012) (Entered: 08/21/2012)
08/28/2012	375	CASE MANAGEMENT STATEMENT *Joint Case Management Conference Statement* filed by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 8/28/2012) (Entered: 08/28/2012)
08/30/2012	376	CLERK'S NOTICE RESETTING TIME ON 9/4/2012 CASE MANAGEMENT CONFERENCE: 9/4/2012 2:00 PM Case Management Conference reset to 3:00 PM (SPECIAL SET) in Courtroom 5, 4th Floor, San Jose. *****This is a text only docket entry, there is no document associated with this notice.***** (ofr, COURT STAFF) (Filed on 8/30/2012) (Entered: 08/30/2012)
09/04/2012	377	Minute Entry: Case Management Conference held on 9/4/2012 before Magistrate Judge Paul S. Grewal. Case management scheduling order to be issued. (Date Filed: 9/4/2012). (Court Reporter FTR: (3:02 to 3:33.) (ofr, COURT STAFF) (Date Filed: 9/4/2012) (Entered: 09/05/2012)

09/10/2012	378	MOTION for Leave to File *Motion for Reconsideration of Certain Aspects of Claim Construction* filed by Alliacense Limited, Technology Properties Limited. (Attachments: #1 Exhibit 1)(Otteson, James) (Filed on 9/10/2012) (Entered: 09/10/2012)
09/14/2012	379	CASE MANAGEMENT SCHEDULING ORDER: Tutorial and Claims Construction Hearing set for 11/7/2012 at 10:00 AM. Pretrial Conference set for 6/11/2013 at 02:00 PM. Jury Trial set for 6/24/2013 at 09:30 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Signed by Judge Paul S. Grewal on 9/14/2012. (ofrS, COURT STAFF) (Filed on 9/14/2012) (Entered: 09/17/2012)
09/21/2012	380	STIPULATION WITH PROPOSED ORDER *Stipulation to Defer Supplemental Claim Construction Briefing and Hearing Schedule* filed by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 9/21/2012) (Entered: 09/21/2012)
09/25/2012	381	STIPULATION AND ORDER TO DEFER SUPPLEMENTAL CLAIM CONSTRUCTION BRIEFING AND HEARING SCHEDULE by Judge Paul S. Grewal, granting (351) Stipulation in case 5:08−cv−00877−PSG; granting (380) Stipulation in case 5:08−cv−00882−PSG. Exchange of Opening Supplemental Claim Construction Briefs: 10/19/2012. Exchange of Responsive Supplemental Claim Construction Briefs: 11/9/2012. Tutorial and Claims Construction Hearing set for 11/30/2012 at 10:00 a.m. in Courtroom 5, 4th Floor, San Jose. (ofr, COURT STAFF) (Filed on 9/25/2012) (Entered: 09/26/2012)
09/25/2012		Set/Reset Hearing re (352 in 5:08−cv−00877−PSG, 352 in 5:08−cv−00877−PSG, 381 in 5:08−cv−00882−PSG, 381 in 5:08−cv−00882−PSG, 297 in 5:08−cv−05398−PSG, 297 in 5:08−cv−05398−PSG) Order on Stipulation: 11/7/2012 Tutorial and Claims Construction Hearing reset to 11/30/2012 at 10:00 AM in Courtroom 5, 4th Floor, San Jose. (ofr, COURT STAFF) (Filed on 9/25/2012) (Entered: 09/26/2012)
09/25/2012	382	ORDER GRANTING DEFENDANTS' MOTION FOR LEAVE TO FILE MOTION FOR RECONSIDERATION OF CERTAIN ASPECTS OF CLAIM CONSTRUCTION by Judge Paul S. Grewal, granting (349) Motion for Leave to File in case 5:08−cv−00877−PSG; granting (378) Motion for Leave to File in case 5:08−cv−00882−PSG; granting (294) Motion for Leave to File in case 5:08−cv−05398−PSG. Motion for Reconsideration set for 11/30/2012 at 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul S. Grewal. (ofr, COURT STAFF) (Filed on 9/25/2012) (Entered: 09/26/2012)
09/25/2012		Set/Reset Hearing: Motion for Reconsideration set for 11/30/2012 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. (ofr, COURT STAFF) (Filed on 9/25/2012) (Entered: 09/26/2012)
09/28/2012	383	MOTION for Leave to File *Motion for Reconsideration of Certain Aspects of First Claim Construction Order* filed by HTC America, Inc., HTC Corporation. (Weinstein, Mark) (Filed on 9/28/2012) (Entered: 09/28/2012)
10/02/2012	384	ORDER GRANTING PLAINTIFFS' MOTION FOR LEAVE TO FILE MOTION FOR RECONSIDERATION OF CERTAIN ASPECTS OF CLAIM CONSTRUCTION by Judge Paul S. Grewal granting (354) Motion for Leave to File in case 5:08−cv−00877−PSG; granting (383) Motion for Leave to File in case 5:08−cv−00882−PSG; granting (299) Motion for Leave to File in case 5:08−cv−05398−PSG (psglc2, COURT STAFF) (Filed on 10/2/2012) (Entered: 10/02/2012)
10/02/2012		Set/Reset Hearing re (384 in 5:08−cv−00882−PSG, 300 in 5:08−cv−05398−PSG and 355 in 5:08−cv−00877−PSG): Motion Hearing set for 11/30/2012 at 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. (ofr, COURT STAFF) (Filed on 10/2/2012) (Entered: 10/03/2012)
10/19/2012	385	MOTION for Reconsideration re 364 Order *Defendants Motion for Reconsideration of Certain Aspects of Claim Construction* filed by Technology Properties Limited. (Otteson, James) (Filed on 10/19/2012) Modified on 12/5/2012 (ofr, COURT STAFF). (Entered: 10/19/2012)

10/19/2012	386	Administrative Motion to File Under Seal *Plaintiffs Administrative Motion to File Confidential Exhibits Under Seal* filed by HTC America, Inc., HTC Corporation. (Attachments: #1 Declaration, #2 Proposed Order)(Chen, Kyle) (Filed on 10/19/2012) (Entered: 10/19/2012)
10/19/2012	387	CLAIM CONSTRUCTION STATEMENT *Defendants Opening Supplemental Claim Construction Brief* filed by Technology Properties Limited. (Attachments: #1 Declaration of James C. Otteson, #2 Exhibit 1−2 to Otteson Declaration, #3 Exhibit 3−6 to Otteson Declaration, #4 Exhibit 7−9 to Otteson Declaration, #5 Exhibit 10−11 to Otteson Declaration)(Otteson, James) (Filed on 10/19/2012) (Entered: 10/19/2012)
10/19/2012	388	MOTION for Reconsideration *Plaintiffs Motion for Reconsideration of Certain Aspects of First Claim Construction Order* filed by HTC America, Inc., HTC Corporation. (Attachments: #1 Declaration of Kyle D. Chen, #2 Exhibit 1, #3 Exhibit 2, #4 Exhibit 3, #5 Exhibit 4 (Redacted−Public Version), #6 Exhibit 5, #7 Exhibit 6, #8 Exhibit 7, #9 Exhibit 8, #10 Exhibit 9, #11 Proposed Order)(Chen, Kyle) (Filed on 10/19/2012) Modified on 12/5/2012 (ofr, COURT STAFF). Modified on 12/5/2012 (ofr, COURT STAFF). (Entered: 10/19/2012)
10/19/2012	389	CLAIM CONSTRUCTION STATEMENT *Plaintiffs Consolidated Opening Supplemental Claim Construction Brief* filed by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 10/19/2012) (Entered: 10/19/2012)
10/20/2012	390	Declaration of Kyle D. Chen in Support of 389 Claim Construction Statement *in Support of Plaintiffs Consolidated Opening Supplemental Claim Construction Brief* filed byHTC America, Inc., HTC Corporation. (Attachments: #1 Exhibit 1, #2 Exhibit 2, #3 Exhibit 3, #4 Exhibit 4, #5 Exhibit 5, #6 Exhibit 6, #7 Exhibit 7 (Redacted/Public Version), #8 Exhibit 8, #9 Exhibit 9, #10 Exhibit 10, #11 Exhibit 11, #12 Exhibit 12, #13 Exhibit 13, #14 Exhibit 14, #15 Exhibit 15, #16 Exhibit 16, #17 Exhibit 17, #18 Exhibit 18, #19 Exhibit 19, #20 Exhibit 20, #21 Exhibit 21, #22 Exhibit 22, #23 Exhibit 23)(Related document(s) 389) (Chen, Kyle) (Filed on 10/20/2012) (Entered: 10/20/2012)
10/20/2012	391	Declaration of David May in Support of 389 Claim Construction Statement *in Support of Plaintiffs Consolidated Opening Supplemental Claim Construction Brief* filed byHTC America, Inc., HTC Corporation. (Related document(s) 389) (Chen, Kyle) (Filed on 10/20/2012) (Entered: 10/20/2012)
10/20/2012	392	Administrative Motion to File Under Seal *Plaintiffs Administrative Motion to File Confidential Exhibit 7* filed by HTC America, Inc., HTC Corporation. (Attachments: #1 Declaration of Kyle D. Chen, #2 Proposed Order)(Chen, Kyle) (Filed on 10/20/2012) (Entered: 10/20/2012)
10/20/2012	393	Declaration of Dr. Andrew Wolfe in Support of 389 Claim Construction Statement *Plaintiffs' Supplemental Claim Construction Brief* filed byHTC America, Inc., HTC Corporation. (Attachments: #1 Exhibit A, #2 Exhibit B, #3 Exhibit C, #4 Exhibit D, #5 Exhibit E, #6 Exhibit F, #7 Exhibit G, #8 Exhibit H, #9 Exhibit I, #10 Exhibit J, #11 Exhibit K, #12 Exhibit L, #13 Exhibit M, #14 Exhibit N, #15 Exhibit O)(Related document(s) 389) (Chen, Kyle) (Filed on 10/20/2012) (Entered: 10/20/2012)
10/21/2012	394	CLAIM CONSTRUCTION STATEMENT *[CORRECTED] PLAINTFFS' CONSOLIDATED OPENING SUPPLEMENTAL CLAIM CONSTRUCTION BRIEF (TO REPLACE DOCKET NO. 389)* filed by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 10/21/2012) (Entered: 10/21/2012)
10/26/2012	395	Administrative Motion to File Under Seal *Exhibit 4 to the Declaration of Kyle Chen in Support of Motion for Reconsideration and Exhibit 7 to the Declaration of Kyle Chen in Support of Consolidated Opening Supplemental Claim Construction Brief* filed by Technology Properties Limited. (Attachments: #1 Exhibit A, #2 Proposed Order)(Breit, Michelle) (Filed on 10/26/2012) (Entered: 10/26/2012)
11/02/2012	396	RESPONSE (re 388 MOTION for Reconsideration *Plaintiffs Motion for Reconsideration of Certain Aspects of First Claim Construction Order*) filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: #1 Declaration of James C. Otteson, #2 Exhibit A, #3 Exhibit B, #4 Exhibit C, #5 Exhibit D)(Otteson, James) (Filed on 11/2/2012)

		(Entered: 11/02/2012)
11/02/2012	397	RESPONSE (re 385 MOTION for Reconsideration re 364 Order *Defendants Motion for Reconsideration of Certain Aspects of Claim Construction*) filed byHTC America, Inc., HTC Corporation. (Attachments: #1 Declaration of Kyle D. Chen in Support of Opposition, #2 Exhibit 1 to Chen Decl., #3 Exhibit 2 to Chen Decl., #4 Exhibit 3 to Chen Decl., #5 Exhibit 4 to Chen Decl., #6 Exhibit 5 to Chen Decl., #7 Exhibit 6 to Chen Decl., #8 Exhibit 7 to Chen Decl.)(Chen, Kyle) (Filed on 11/2/2012) (Entered: 11/02/2012)
11/09/2012	398	REPLY IN SUPPORT OF ITS MOTION FOR RECONSIDERATION OF CERTAIN ASPECTS OF CLAIM CONSTRUCTION re 385 filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: #1 Declaration of Michelle G. Breit, #2 Exhibit A to Breit Declaration, #3 Exhibit B to Breit Declaration, #4 Exhibit C to Breit Declaration) (Breit, Michelle) (Filed on 11/9/2012) Modified on 11/13/2012 (bw, COURT STAFF). (Entered: 11/09/2012)
11/09/2012	399	Reply Supplemental Claim Construction Brief filed by Technology Properties Limited. (Attachments: #1 Declaration of Michelle G. Breit in Support of Defendants' Reply Supplemental Claim Construction Brief, #2 Exhibit A to Declaration of Michelle G. Breit)(Breit, Michelle) (Filed on 11/9/2012) Modified on 11/13/2012 (bw, COURT STAFF). (Entered: 11/09/2012)
11/09/2012	400	REPLY BRIEF IN SUPPORT OF PLAINTIFFS MOTION FOR RECONSIDERATION OF CERTAIN ASPECTS OF FIRST CLAIM CONSTRUCTION ORDER re 388 filed by HTC America, Inc., HTC Corporation. (Attachments: #1 Declaration (Supplemental) of Kyle D. Chen, #2 Exhibit 10) (Chen, Kyle) (Filed on 11/9/2012) Modified on 11/13/2012 (bw, COURT STAFF). (Entered: 11/09/2012)
11/09/2012	401	CONSOLIDATED RESPONSIVE SUPPLEMENTAL CLAIM CONSTRUCTION BRIEF filed by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 11/9/2012) Modified on 11/13/2012 (bw, COURT STAFF). (Entered: 11/09/2012)
11/09/2012	402	SUPPLEMENTAL DECLARATION OF KYLE D. CHEN IN SUPPORT OF PLAINTIFFS CONSOLIDATED RESPONSIVE CLAIM CONSTRUCTION BRIEF re 401 filed by HTC America, Inc., HTC Corporation. (Attachments: #1 Exhibit 24, #2 Exhibit 25, #3 Exhibit 26, #4 Exhibit 27, #5 Exhibit 28, #6 Exhibit 29, #7 Exhibit 30, #8 Exhibit 31, #9 Exhibit 32, #10 Exhibit 33, #11 Exhibit 34) (Chen, Kyle) (Filed on 11/9/2012) Modified on 11/13/2012 (bw, COURT STAFF). (Entered: 11/09/2012)
11/16/2012	403	MOTION for Leave to File Plaintiffs' Sur−Reply in Support of Their Opposition to Defendants' Motion for Reconsideration of Certain Aspects of First Claim Construction Order filed by HTC America, Inc., HTC Corporation. (Attachments: #1 Exhibit−1: (Proposed Sur−Reply, #2 (Proposed) Order)(Chen, Kyle) (Filed on 11/16/2012) Modified on 11/19/2012 (bwS, COURT STAFF). (Entered: 11/16/2012)
11/19/2012	404	OPPOSITION TO PLAINTIFFS MOTION FOR LEAVE TO FILE SUR−REPLY IN SUPPORT OF THEIR OPPOSITION TO DEFENDANTS MOTION FOR RECONSIDERATION OF CERTAIN ASPECTS OF CLAIM CONSTRUCTION re 403 filed by Alliacense Limited, Technology Properties Limited. (Otteson, James) (Filed on 11/19/2012) Modified on 11/20/2012 (bwS, COURT STAFF). (Entered: 11/19/2012)
11/26/2012	405	NOTICE by HTC America, Inc., HTC Corporation *of Plaintiffs' Joint Motion for Order Permitting Use of Equipment During Court Hearing; [Proposed] Order* (Chen, Kyle) (Filed on 11/26/2012) (Entered: 11/26/2012)
11/28/2012	406	PLAINTIFFS' JOINT MOTION FOR ORDER PERMITTING USE OF EQUIPMENT DURING COURT HEARING; ORDER, granting (405 in 5:08−cv−00882−PSG) Notice (Other) filed by HTC America, Inc., HTC Corporation. Signed by Judge Paul S. Grewal on 11/28/2012. (ofr, COURT STAFF) (Filed on 11/28/2012) (Entered: 11/28/2012)

11/29/2012	407	ORDER RE TELEPHONE APPEARANCES AT CLAIM CONSTRUCTION HEARING by Judge Paul S. Grewal in case 5:08−cv−00877−PSG; granting (320) Motion to Appear by Telephone in case 5:08−cv−05398−PSG (psglc2, COURT STAFF) (Filed on 11/29/2012) (Entered: 11/29/2012)
11/29/2012	408	CLERK'S NOTICE RE: TELEPHONIC APPEARANCE AT 11/30/2012 TUTORIAL/CLAIMS CONSTRUCTION HEARING: Parties requesting to appear telephonically are instructed to contact CourtCall at 866−582−6878 to arrange for telephonic appearance. *****This is a text only docket entry, there is no document associated with this notice.***** (ofr, COURT STAFF) (Filed on 11/29/2012) (Entered: 11/29/2012)
11/30/2012	409	Minute Entry: Tutorial, Claim Construction and Motions for Reconsideration held on 11/30/2012 before Magistrate Judge Paul S. Grewal: The court issues construction from the bench; written order after hearing to be issued. (Court Reporter: Gina Galvan Colin.) (ofr, COURT STAFF) (Date Filed: 11/30/2012) (Entered: 11/30/2012)
12/04/2012	410	CLAIM CONSTRUCTION ORDER re (356, 357, 358 &374 in 5:08−cv−00877−PSG) AND re (385, 387, 388 &403 in 5:08−cv−00882−PSG). Signed by Judge Paul S. Grewal on 12/4/2012. (ofr, COURT STAFF) (Filed on 12/4/2012) (Entered: 12/05/2012)
12/05/2012	411	REPLY (re 385 MOTION for Reconsideration re 364 Order *Defendants Motion for Reconsideration of Certain Aspects of Claim Construction*) ***Plaintiffs' SUR−REPLY in Support of 397 Plaintiffs' OPPOSITION to 385 Defendants' Motion for Reconsideration of Certain Aspects of First Claim Construction Order*** filed byHTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 12/5/2012) (Entered: 12/05/2012)
12/12/2012	412	***** FILED IN ERROR. PLEASE DISREGARD. SEE 413 ****** MOTION to Continue *Defendants' Motion Under Civil Local Rules 6−3 and 7−11 to Continue Trial Date and Corresponding Dates; Memorandum of Points and Authorities* filed by Technology Properties Limited. (Attachments: # 1 Declaration of James C. Otteson, # 2 Exhibit A, # 3 Exhibit B, # 4 Proposed Order Proposed Revised Case Management Order)(Otteson, James) (Filed on 12/12/2012) Modified on 12/13/2012 (bwS, COURT STAFF). (Entered: 12/12/2012)
12/12/2012	413	MOTION to Continue Defendants' Motion Under Civil Local Rules 6−3 and 7−11 to Continue Trial Date and Corresponding Dates; Memorandum of Points and Authorities filed by Technology Properties Limited. (Attachments: # 1 Declaration of James C. Otteson, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6(Proposed) Revised Case Management Order) (Otteson, James) (Filed on 12/12/2012) Modified on 12/14/2012 (bwS, COURT STAFF). (Entered: 12/12/2012)
12/17/2012	414	RESPONSE (re 413 MOTION to Continue *Defendants' Motion Under Civil Local Rules 6−3 and 7−11 to Continue Trial Date and Corresponding Dates; Memorandum of Points and Authorities*) filed byHTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 12/17/2012) (Entered: 12/17/2012)
12/18/2012	415	*****EFILED IN ERROR, PLEASE SEE DOCKET NO. 416 *****ORDER DENYING TPL'S MOTION TO CONTINUE TRIAL by Judge Paul S. Grewal, denying (384) Motion to Continue in case 5:08−cv−00877−PSG; denying (413) Motion to Continue in case 5:08−cv−00882−PSG. (ofr, COURT STAFF) (Filed on 12/18/2012) Modified on 12/19/2012 (ofr, COURT STAFF). (Entered: 12/19/2012)
12/18/2012	416	ORDER DENYING TPL'S MOTION TO CONTINUE TRIAL by Judge Paul S. Grewal, denying (384) Motion to Continue in case 5:08−cv−00877−PSG; denying (413) Motion to Continue in case 5:08−cv−00882−PSG. Signed by Judge Paul S. Grewal on 12/18/2012. (ofr, COURT STAFF) (Filed on 12/18/2012) (Entered: 12/19/2012)
12/21/2012	417	MOTION for Extension of Time to Complete Discovery *Defendants' Unopposed Motion Under Civil Local Rules 6−3 and 7−11 for Modest Extension of Interim Pre−Trial Dates* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Proposed Order Modifying Interim Pre−Trial Dates)(Otteson, James) (Filed on 12/21/2012) (Entered:

		12/21/2012)
12/26/2012	418	ORDER MODIFYING INTERIM PRE−TRIAL DATES by Judge Paul S. Grewal granting 417 Motion for Extension of Time to Complete Discovery (psglc1, COURT STAFF) (Filed on 12/26/2012) (Entered: 12/26/2012)
12/28/2012	419	ORDER by Judge Paul S. Grewal granting (388) Motion for Extension of Time to Complete Discovery in case 5:08−cv−00877−PSG (psglc2, COURT STAFF) (Filed on 12/28/2012) (Entered: 12/28/2012)
01/29/2013	420	Joint MOTION to Continue *(Joint Motion Under Civil Local Rules 6−3 and 7−11 to Permit Depositions of LSI Corporation Out of Time and to Modify Select Interim Pre−Trial Dates)* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Proposed Order)(Otteson, James) (Filed on 1/29/2013) (Entered: 01/29/2013)
01/31/2013	422	ORDER MODIFYING INTERIM PRE−TRIAL DATES by Judge Paul S. Grewal, granting (390) Motion to Continue in case 5:08−cv−00877−PSG and granting (420) Motion to Continue in case 5:08−cv−00882−PSG. (ofr, COURT STAFF) (Filed on 1/31/2013) (Entered: 02/01/2013)
02/01/2013	421	NOTICE of Appearance by Philip William Marsh *on Behalf of Defendants Technology Properties Limited and Alliacense Limited* (Marsh, Philip) (Filed on 2/1/2013) (Entered: 02/01/2013)
02/01/2013	423	NOTICE of Appearance by Thomas T. Carmack *on Behalf of Defendants Technology Properties Limited and Alliacense Limited* (Carmack, Thomas) (Filed on 2/1/2013) (Entered: 02/01/2013)
02/05/2013	424	Administrative Motion to File Under Seal *Administrative Motion for Leave to File Under Seal Defendants' Confidential Emergency Motion to Modify Case Schedule Due to Acer's Discovery Abuses, Declarations Submitted in Support Thereof, and Certain Exhibits Attached to the Declarations* filed by Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Declaration of James C. Otteson, # 2 Proposed Order)(Otteson, James) (Filed on 2/5/2013) (Entered: 02/05/2013)
02/06/2013	425	Statement of Non−Opposition *re 424 Defendants' Emergency Motion to Modify Case Schedule* filed byHTC America, Inc., HTC Corporation. (Weinstein, Mark) (Filed on 2/6/2013) Modified on 2/7/2013 (gmS,). (Entered: 02/06/2013)
02/07/2013	426	MOTION to Shorten Time *on Defendants' Emergency Motion to Modify Case Schedule due to Acer's Discovery Abuses* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Declaration, # 2 Proposed Order)(Otteson, James) (Filed on 2/7/2013) (Entered: 02/07/2013)
02/08/2013	427	CLERK'S NOTICE SETTING STATUS CONFERENCE: Status Conference set for 2/8/2013 at 04:45 PM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Parties requesting to appear telephonically are instructed to contact CourtCall at 866−582−6878 to arrange for telephonic appearance. *****This is a text only docket entry, there is no document associated with this notice.***** (ofr, COURT STAFF) (Filed on 2/8/2013) (Entered: 02/08/2013)
02/08/2013	429	Minute Entry: Motion Hearing held on 2/8/2013 before Magistrate Judge Paul S. Grewal re (394 in 5:08−cv−00877−PSG) MOTION to Compel *DEFENDANTS TO PRODUCE A 30(B)(6) WITNESS FOR CERTAIN TOPICS* and (402 in 5:08−cv−00877−PSG) MOTION to Shorten Time *on Defendants' Emergency Motion to Modify Case Schedule Due to Acer's Discovery Abuses* and (426 in 5:08−cv−00882−PSG): Parties have reached agreement as to plaintiffs motion to compel, withdrawal of motion on file. Acer to complete production of documents discussed in court by 2/15/2013 at 5:00 p.m. Court is open to entertain a motion for sanctions from Technology Properties Limited. Court to issue revised trial schedule. (Court Reporter: Irene Rodriguez.) (ofr, COURT STAFF) (Date Filed: 2/8/2013) (Entered: 02/11/2013)
02/11/2013	428	ORDER DENYING AS MOOT 426 MOTION TO SHORTEN TIME entered by Magistrate Judge Paul Singh Grewal. (This is a text−only entry generated by the

		court. There is no document associated with this entry.) (Entered: 02/11/2013)
02/12/2013	430	MODIFIED CASE MANAGEMENT SCHEDULING ORDER: Pretrial Conference set for 9/10/2013 02:00 PM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Jury Trial set for 9/23/2013 09:30 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Signed by Judge Paul S. Grewal on 2/12/2013. (ofr, COURT STAFF) (Filed on 2/12/2013) (Entered: 02/12/2013)
02/15/2013	431	ORDER RE SEALING MOTIONS by Judge Paul S. Grewal granting (359) Administrative Motion to File Under Seal; granting (364) Administrative Motion to File Under Seal; granting (366) Administrative Motion to File Under Seal; denying (398) Administrative Motion to File Under Seal in case 5:08−cv−00877−PSG; granting (386) Administrative Motion to File Under Seal; granting (392) Administrative Motion to File Under Seal; granting (395) Administrative Motion to File Under Seal; denying (424) Administrative Motion to File Under Seal in case 5:08−cv−00882−PSG (psglc2, COURT STAFF) (Filed on 2/15/2013) (Entered: 02/18/2013)
03/01/2013	432	MOTION to Continue *UNOPPOSED MOTION UNDER CIVIL LOCAL RULES 6−3 AND 7−11 TO EXTEND THE FACT DISCOVERY CUTOFF* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: #1 Proposed Order)(Otteson, James) (Filed on 3/1/2013) (Entered: 03/01/2013)
03/07/2013	433	ORDER GRANTING 432 MOTION TO CONTINUE entered by Magistrate Judge Paul Singh Grewal. (This is a text−only entry generated by the court. There is no document associated with this entry.) (Entered: 03/07/2013)
03/15/2013	434	CLERK'S NOTICE SETTING STATUS CONFERENCE (In Re: Docket Nos. 414 , 416 and 417) in 5:08−cv−00877−PSG: Status Conference set for 3/19/2013 at 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Parties requesting to appear telephonically are instructed to contact CourtCall at 866−582−6878 to arrange for telephonic appearance. *****This is a text only docket entry, there is no document associated with this notice***** (ofr, COURT STAFF) (Filed on 3/15/2013) (Entered: 03/15/2013)
03/19/2013	435	Minute Entry: Status Conference held. (Court Reporter: Summer Fisher.) (ofr, COURT STAFF) (Date Filed: 3/19/2013) (Entered: 03/19/2013)
03/20/2013	436	DOCUMENT E−FILED UNDER SEAL re 431 Order on Administrative Motion to File Under Sea by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 3/20/2013) Modified on 3/21/2013 (bwS, COURT STAFF). (Entered: 03/20/2013)
03/20/2013	437	DOCUMENT E−FILED UNDER SEAL re 431 Order on Administrative Motion to File Under Seal by HTC America, Inc., HTC Corporation. (Attachments: #1 Part 2, #2 Part 3, #3 Part 4) (Chen, Kyle) (Filed on 3/20/2013) Modified on 3/21/2013 (bwS, COURT STAFF). (Entered: 03/20/2013)
03/21/2013	438	NOTICE by Technology Properties Limited *re: Notice of Filing of Chapter 11 Proceeding and Notice of Automatic Stay of Actions* (Penhallegon, Ryan) (Filed on 3/21/2013) (Entered: 03/21/2013)
03/21/2013	439	ORDER RE: STATUS UPDATES (425 in 5:08−cv−00877−PSG) and (438 in 5:08−cv−00882−PSG): Pursuant to 11 U.S.C. § 362, both of the cases in this court are automatically stayed pending resolution of the bankruptcy case. The parties shall submit to the court every 90 days joint letter briefs with updates about the status of the bankruptcy case. Signed by Judge Paul S. Grewal on 3/21/2013. (ofr, COURT STAFF) (Filed on 3/21/2013) (Entered: 03/21/2013)
03/21/2013	440	AMENDED DOCUMENT by Technology Properties Limited. Amendment to 438 Notice (Other) *RE: Amended and Superceded Notice of Filing of Chapter 11 Proceeding and Notice of Automatic Stay of Actions*. (Penhallegon, Ryan) (Filed on 3/21/2013) (Entered: 03/21/2013)
03/21/2013	441	NOTICE by Technology Properties Limited *Notice Clarifying Prior Notice of Filing of Chapter 11 Proceeding and Notice of Automatic Stay of Actions* (Otteson, James) (Filed on 3/21/2013) (Entered: 03/21/2013)

03/27/2013	442	ORDER INVITING BRIEFING RE EFFECT OF AUTOMATIC STAY re (441 in 5:08−cv−00882−PSG) Notice (Other) filed by Technology Properties Limited, (427 in 5:08−cv−00877−PSG) Amended Document filed by Technology Properties Limited, (428 in 5:08−cv−00877−PSG) Notice (Other) filed by Technology Properties Limited, (425 in 5:08−cv−00877−PSG) Notice (Other) filed by Technology Properties Limited, (440 in 5:08−cv−00882−PSG) Amended Document filed by Technology Properties Limited, (438 in 5:08−cv−00882−PSG) Notice (Other) filed by Technology Properties Limited. Signed by Judge Paul S. Grewal on March 27, 2013. (psglc2, COURT STAFF) (Filed on 3/27/2013) (Entered: 03/27/2013)
03/29/2013	443	Letter from James C. Otteson *to Magistrate Judge Paul S. Grewal re Effect of Automatic Stay*. (Attachments: #1 Exhibit A, #2 Exhibit B, #3 Exhibit C)(Otteson, James) (Filed on 3/29/2013) (Entered: 03/29/2013)
04/05/2013	444	Letter from Kyle Chen of Cooley LLP on behalf of HTC Corp. and HTC America, Inc. *in response to this Court's ORDER INVITING BRIEFING RE: EFFECT OF AUTOMATIC STAY issued on March 27, 2013*. (Chen, Kyle) (Filed on 4/5/2013) (Entered: 04/05/2013)
05/13/2013	445	**ORDER RE LIFT OF AUTOMATIC STAY AND SEALING MOTIONS by Judge Paul S. Grewal denying (416) Administrative Motion to File Under Seal; denying (417) Administrative Motion to File Under Seal in case 5:08−cv−00877−PSG (psglc2, COURT STAFF) (Filed on 5/13/2013) (Entered: 05/13/2013)**
05/14/2013	446	CLERK'S NOTICE SETTING PRETRIAL CONFERENCE AND JURY TRIAL: Pretrial Conference set for 9/10/2013 at 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Jury Trial set for 9/23/2013 at 9:30 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. *****This is a text only docket entry, there is no document associated with this notice.***** (ofr, COURT STAFF) (Filed on 5/14/2013) (Entered: 05/14/2013)
05/15/2013	447	NOTICE by Alliacense Limited, Technology Properties Limited *Regarding Filing of Unredacted Version of Letter Dated March 13, 2013 Pursuant to Order Docket Nos. 434 and 445* (Attachments: #1 Attachment A)(Otteson, James) (Filed on 5/15/2013) (Entered: 05/15/2013)
05/15/2013	448	Joint MOTION to Continue *Under Civil Local Rules 6−3 and 7−11 to Modify the Case Schedule* filed by Alliacense Limited, Technology Properties Limited. (Attachments: #1 Proposed Order)(Otteson, James) (Filed on 5/15/2013) (Entered: 05/15/2013)
05/16/2013	449	**ORDER MODIFYING CASE SCHEDULE by Judge Paul S. Grewal, granting (437) Motion to Continue in case 5:08−cv−00877−PSG; granting (448) Motion to Continue in case 5:08−cv−00882−PSG. (ofr, COURT STAFF) (Filed on 5/16/2013) (Entered: 05/16/2013)**
07/02/2013	450	CLERKS NOTICE ADVANCING SEPTEMBER 10, 2013 PRETRIAL CONFERENCE: 9/10/2013 Pretrial Conference advanced to 8/29/2013 at 2:00 PM (SPECIAL SET) in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. *****This is a text only docket entry, there is no document associated with this notice.***** (ofr, COURT STAFF) (Filed on 7/2/2013) (Entered: 07/02/2013)
07/03/2013	451	Joint MOTION to Continue *Under Civil Local Rules 6−3 and 7−11 to Modify the Case Schedule with Regards to Expert Discovery and Dispositive Motion Deadlines* filed by HTC America, Inc., HTC Corporation. (Attachments: #1 Proposed Order)(Chen, Kyle) (Filed on 7/3/2013) (Entered: 07/03/2013)
07/03/2013	452	**ORDER GRANTING MOTION TO MODIFY CASE SCHEDULE by Judge Paul S. Grewal granting (441) Motion to Continue in case 5:08−cv−00877−PSG; granting (451) Motion to Continue in case 5:08−cv−00882−PSG (psglc2, COURT STAFF) (Filed on 7/3/2013) (Entered: 07/03/2013)**

07/09/2013	453	MOTION for SEPARATE TRIAL (from Case No. 08−CV−877) filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 8/13/2013 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 7/23/2013. Replies due by 7/30/2013. (Chen, Kyle) (Filed on 7/9/2013) (Entered: 07/09/2013)
07/10/2013	454	NOTICE of Appearance by Ronald Scott Lemieux (Lemieux, Ronald) (Filed on 7/10/2013) (Entered: 07/10/2013)
07/11/2013	455	STIPULATION WITH PROPOSED ORDER re 452 Order on Motion to Continue, *To Modify the Dispositive Motion Briefing Deadlines* filed by HTC America, Inc., HTC Corporation. (Attachments: # 1 Proposed Order)(Chen, Kyle) (Filed on 7/11/2013) (Entered: 07/11/2013)
07/12/2013	456	**ORDER GRANTING 455 STIPULATION entered by Magistrate Judge Paul Singh Grewal. (This is a text−only entry generated by the court. There is no document associated with this entry.) (Entered: 07/12/2013)**
07/16/2013	457	MOTION for Summary Judgment *Plaintiffs Notice of Motion and Motion for Summary Judgment of Non−Infringement and No Willful Infringement of U.S. Patent No. 5,809,336* filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 8/13/2013 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 7/26/2013. Replies due by 7/31/2013. (Attachments: # 1 Declaration of Kyle Chen, # 2 Exhibit 1, # 3 Exhibit 2, # 4 Exhibit 3 − Part 1, # 5 Exhibit 3 − Part 2, # 6 Exhibit 3 − Part 3, # 7 Exhibit 3 − Part 4, # 8 Exhibit 3 − Part 5, # 9 Exhibit 3 − Part 6, # 10 Exhibit 3 − Part 7, # 11 Exhibit 4, # 12 Exhibit 5, # 13 Exhibit 6, # 14 Exhibit 7, # 15 Exhibit 8, # 16 Exhibit 9, # 17 Exhibit 10, # 18 Exhibit 11, # 19 Exhibit 12, # 20 Exhibit 13, # 21 Exhibit 14, # 22 Exhibit 15, # 23 Exhibit 16, # 24 Exhibit 17, # 25 Declaration of Thomas Gafford, # 26 Exhibit 1, # 27 Exhibit 2, # 28 Proposed Order)(Chen, Kyle) (Filed on 7/16/2013) (Entered: 07/16/2013)
07/16/2013	458	MOTION for Partial Summary Judgment *of non−infringement of U.S. Patent Nos. 5,809,336 and 5,530,890 and no willful infringement of the 890 patent* filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 8/13/2013 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 7/26/2013. Replies due by 7/31/2013. (Attachments: # 1 Exhibit 1, # 2 Exhibit 2, # 3 Exhibit 3, # 4 Exhibit 4, # 5 Exhibit 5, # 6 Exhibit 6, # 7 Exhibit 7, # 8 Exhibit 8, # 9 Exhibit 9, # 10 Proposed Order)(Weinstein, Mark) (Filed on 7/16/2013) (Entered: 07/16/2013)
07/16/2013	459	Declaration of Mark R. Weinstein in Support of 458 MOTION for Partial Summary Judgment *of non−infringement of U.S. Patent Nos. 5,809,336 and 5,530,890 and no willful infringement of the 890 patent* filed byHTC America, Inc., HTC Corporation. (Related document(s) 458) (Weinstein, Mark) (Filed on 7/16/2013) (Entered: 07/16/2013)
07/17/2013	460	Administrative Motion to File Under Seal *Exhibits to the Declarations in Support of Plaintiffs' Motion for Summary Judgment of Non−Infringement and No Willful Infringement (Dkt. No. 457)* filed by HTC America, Inc., HTC Corporation. (Attachments: # 1 Declaration of Kyle Chen, # 2 Proposed Order)(Chen, Kyle) (Filed on 7/17/2013) (Entered: 07/17/2013)
07/17/2013	461	STIPULATION WITH PROPOSED ORDER *REGARDING PATENTS NO LONGER ASSERTED* filed by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 7/17/2013) (Entered: 07/17/2013)
07/18/2013	462	**STIPULATION AND ORDER REGARDING PATENTS NO LONGER ASSERTED by Judge Paul S. Grewal, granting 461 . (ofr, COURT STAFF) (Filed on 7/18/2013) (Entered: 07/18/2013)**
07/19/2013	463	MOTION for leave to appear in Pro Hac Vice − *Application for Admission of Attorney Pro Hac Vice for Stephen Smith* (Filing fee $ 305, receipt number 0971−7861632.) filed by HTC America, Inc., HTC Corporation. (Weinstein, Mark) (Filed on 7/19/2013) (Entered: 07/19/2013)
07/22/2013	464	**ORDER GRANTING APPLICATION FOR ADMISSION OF ATTORNEY STEPHEN R. SMITH PRO HAC VICE by Judge Paul S. Grewal, granting**

		463 . (ofr, COURT STAFF) (Filed on 7/22/2013) (Entered: 07/22/2013)
07/23/2013	465	Administrative Motion to File Under Seal *Exhibits A &B to Defendants Opposition to HTC's Motion for Separate Trial and portions of the Opposition* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: #1 Declaration of Thomas T. Carmack, #2 Proposed Order)(Carmack, Thomas) (Filed on 7/23/2013) (Entered: 07/23/2013)
07/23/2013	466	RESPONSE (re 453 MOTION for SEPARATE TRIAL (from Case No. 08−CV−877)) *[PUBLIC VERSION] of Defendants' Opposition to HTC's Motion for Separate Trial* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: #1 Declaration of Thomas T. Carmack)(Carmack, Thomas) (Filed on 7/23/2013) (Entered: 07/23/2013)
07/23/2013	467	Declaration of Thomas T. Carmack in Support of 460 Administrative Motion to File Under Seal *Exhibits to the Declarations in Support of Plaintiffs' Motion for Summary Judgment of Non−Infringement and No Willful Infringement (Dkt. No. 457)* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Related document(s) 460) (Carmack, Thomas) (Filed on 7/23/2013) (Entered: 07/23/2013)
07/26/2013	468	Administrative Motion to File Under Seal *Defendants' Oppositions to Motions for Summary Judgment and Supporting Declarations* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: #1 Declaration of Philip W. Marsh, #2 Proposed Order)(Marsh, Philip) (Filed on 7/26/2013) (Entered: 07/26/2013)
07/26/2013	469	RESPONSE (re 458 MOTION for Partial Summary Judgment *of non−infringement of U.S. Patent Nos. 5,809,336 and 5,530,890 and no willful infringement of the 890 patent*) filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: #1 Declaration of Tanya Wei, #2 Exhibit A to Wei Declaration, #3 Exhibit B to Wei Declaration, #4 Exhibit C to Wei Declaration, #5 Exhibit D to Wei Declaration, #6 Errata E to Wei Declaration, #7 Exhibit F to Wei Declaration, #8 Exhibit G to Wei Declaration, #9 Declaration of Jed Phillips, #10 Exhibit A to Phillips Declaration, #11 Exhibit B to Phillips Declaration, #12 Exhibit C &D slip sheet)(Carmack, Thomas) (Filed on 7/26/2013) (Entered: 07/26/2013)
07/26/2013	470	RESPONSE (re 457 MOTION for Summary Judgment *Plaintiffs Notice of Motion and Motion for Summary Judgment of Non−Infringement and No Willful Infringement of U.S. Patent No. 5,809,336*) *(PUBLIC VERSION)* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: #1 Declaration of Jed Phillips (PUBLIC VERSION))(Otteson, James) (Filed on 7/26/2013) (Entered: 07/26/2013)
07/26/2013	471	DECLARATION of Irvin Tyan in Opposition to 470 Opposition/Response to Motion, *(PUBLIC VERSION)* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: #1 Exhibit A, #2 Exhibit B, #3 Exhibit C, #4 Exhibit D, #5 Exhibit E, #6 Exhibit F, #7 Exhibit G, #8 Exhibit H, #9 Exhibit P, #10 Exhibit I − O and Q − R slip sheets)(Related document(s) 470) (Tyan, Irvin) (Filed on 7/26/2013) (Entered: 07/26/2013)
07/26/2013	472	DECLARATION of Philip W. Marsh in Opposition to 469 Opposition/Response to Motion,,, 470 Opposition/Response to Motion, *(PUBLIC VERSION)* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: #1 Exhibit A (Declaration of Vojin Oklobdzija) (PUBLIC VERSION))(Related document(s) 469 , 470) (Marsh, Philip) (Filed on 7/26/2013) (Entered: 07/26/2013)
07/30/2013	473	NOTICE of Appearance by Thomas T. Carmack *Notice of Appearance of David Lansky on Behalf of Defendants Technology Properties Limited and Alliacense Limited* (Carmack, Thomas) (Filed on 7/30/2013) (Entered: 07/30/2013)
07/30/2013	474	REPLY (re 453 MOTION for SEPARATE TRIAL (from Case No. 08−CV−877)) filed byHTC America, Inc., HTC Corporation. (Attachments: #1 Declaration of Kyle Chen ISO Reply, #2 Exhibit A to Declaration of Kyle Chen ISO Reply)(Weinstein, Mark) (Filed on 7/30/2013) (Entered: 07/30/2013)

07/31/2013	475	REPLY (re 458 MOTION for Partial Summary Judgment *of non−infringement of U.S. Patent Nos. 5,809,336 and 5,530,890 and no willful infringement of the 890 patent*) filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Declaration (Supplemental) of Mark Weinstein ISO Mtn for Partial Summary Judgment, # 2 Exhibit 10 to Supplemental Declaration of Mark Weinstein, # 3 Declaration (Omnibus) of Thomas A. Gafford ISO Reply Brief, # 4 Exhibit A to Gafford Omnibus Declaration ISO Reply Brief, # 5 Exhibit B to Gafford Omnibus Declaration ISO Reply Brief)(Weinstein, Mark) (Filed on 7/31/2013) (Entered: 07/31/2013)
08/01/2013	476	*** POSTED IN ERROR *** Please see 485 REPLY (re 457 MOTION for Summary Judgment *Plaintiffs Notice of Motion and Motion for Summary Judgment of Non−Infringement and No Willful Infringement of U.S. Patent No. 5,809,336*) *PUBLIC VERSION* filed by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 8/1/2013) Modified on 8/13/2013 (cv, COURT STAFF). (Entered: 08/01/2013)
08/01/2013	477	*** POSTED IN ERROR *** Please see 485 REPLY (re 457 MOTION for Summary Judgment *CORRECTION OF DOCKET 476 PUBLIC VERSION* filed by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 8/1/2013) Modified on 8/13/2013 (cv, COURT STAFF). (Entered: 08/01/2013)
08/01/2013	478	Administrative Motion to File Under Seal *REPLY BRIEF 476 and EXHIBITS 19, 20, 21* filed by HTC America, Inc., HTC Corporation. (Attachments: # 1 Declaration of Kyle Chen ISO Adm Mtn to Seal, # 2 Exhibit, # 3 Exhibit, # 4 Exhibit, # 5 Exhibit, All Exhibits Under Seal **without a Court Order not in compliance to general NO. 62 − ELECTRONIC FILING OF DOCUMENTS UNDER SEAL** # 6 Proposed Order)(Chen, Kyle) (Filed on 8/1/2013) Modified on 8/13/2013 (cv, COURT STAFF). (Entered: 08/01/2013)
08/01/2013	479	CERTIFICATE OF SERVICE by HTC America, Inc., HTC Corporation re 476 Reply to Opposition/Response,,, *Docket 457* (Chen, Kyle) (Filed on 8/1/2013) (Entered: 08/01/2013)
08/02/2013	480	MOTION for leave to appear in Pro Hac Vice (Filing fee $ 305, receipt number 0971−7896961.) filed by HTC America, Inc., HTC Corporation. (Leary, Matthew) (Filed on 8/2/2013) (Entered: 08/02/2013)
08/05/2013	481	**ORDER GRANTING APPLICATION FOR ADMISSION OF ATTORNEY MATTHEW J. LEARY PRO HAC VICE by Judge Paul S. Grewal, granting 480 . (ofr, COURT STAFF) (Filed on 8/5/2013) (Entered: 08/06/2013)**
08/07/2013	482	**ORDER SETTING HEARING RE: SEALING MOTIONS. Signed by Judge Paul S. Grewal on August 7, 2013. (psglc2, COURT STAFF) (Filed on 8/7/2013) (Entered: 08/07/2013)**
08/07/2013		Set Hearing re (482 in 5:08−cv−00882−PSG) Order: Hearing re: Sealing Motions set for 8/13/2013 at 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. (ofr, COURT STAFF) (Filed on 8/7/2013) (Entered: 08/08/2013)
08/09/2013	483	CLERK'S NOTICE RESETTING TIME ON AUGUST 13, 2013 MOTION FOR NEW TRIAL, MOTIONS FOR SUMMARY JUDGMENT AND HEARING RE SEALING MOTIONS (In Re: Docket Nos. 453 , 457 , 458 and 482): 8/13/2013 10:00 AM Motions are reset to 1:30 PM (SPECIAL SET) in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. *****This is a text only docket entry, there is no document associated with this notice.***** (ofr, COURT STAFF) (Filed on 8/9/2013) (Entered: 08/09/2013)
08/12/2013	484	Notice of Withdrawal of Motion − *Plaintiffs' Notice of Withdrawal of Plaintiffs' Motion to Seal* (Chen, Kyle) (Filed on 8/12/2013) (Entered: 08/12/2013)
08/12/2013	485	REPLY (re 457 MOTION for Summary Judgment *Plaintiffs Notice of Motion and Motion for Summary Judgment of Non−Infringement and No Willful Infringement of U.S. Patent No. 5,809,336*) *CORRECTION OF DOCKET # 476 , # 477* filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Supplemental Declaration of Kyle D. Chen, # 2 Exhibit 18, # 3 Exhibit 19, # 4 Exhibit 20, # 5 Exhibit 21, # 6 Exhibit 22)(Chen, Kyle) (Filed on 8/12/2013) (Entered:

		08/12/2013)
08/13/2013	486	Declaration of Damstedt in Support of 465 Administrative Motion to File Under Seal *Exhibits A &B to Defendants Opposition to HTC's Motion for Separate Trial and portions of the Opposition,* 460 Administrative Motion to File Under Seal *Exhibits to the Declarations in Support of Plaintiffs' Motion for Summary Judgment of Non−Infringement and No Willful Infringement (Dkt. No. 457),* 468 Administrative Motion to File Under Seal *Defendants' Oppositions to Motions for Summary Judgment and Supporting Declarations* filed byQualcomm Inc.. (Attachments: # 1 Declaration (Farmer), # 2 Proposed Order)(Related document(s) 465 , 460 , 468) (Damstedt, Benjamin) (Filed on 8/13/2013) (Entered: 08/13/2013)
08/13/2013	487	Declaration of Kyle D. Chen in Support of 468 Administrative Motion to File Under Seal *Defendants' Oppositions to Motions for Summary Judgment and Supporting Declarations* filed byHTC America, Inc., HTC Corporation. (Related document(s) 468) (Chen, Kyle) (Filed on 8/13/2013) (Entered: 08/13/2013)
08/13/2013	507	Minute Entry: Motion Hearing held on 8/13/2013 before Magistrate Judge Paul S. Grewal re 444 , 449 , 452 , 454 , 455 and 491 in 5:08−cv−00877−PSG and 453 , 457 , 458 and 482 in 5:08−cv−00882−PSG: Parties to submit joint submission re: sealing requests for the court's review within one week. Court to issue order after hearing. (Court Reporter: Summer Fisher.) (ofr, COURT STAFF) (Date Filed: 8/13/2013) (Entered: 08/19/2013)
08/15/2013	488	MOTION in Limine *No. 1 Regarding Prior Litigations* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. Motion Hearing set for 8/29/2013 02:00 PM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 8/22/2013. Replies due by 8/29/2013. (Otteson, James) (Filed on 8/15/2013) (Entered: 08/15/2013)
08/15/2013	489	MOTION in Limine *DEFENDANTS MOTION IN LIMINE NO. 2 TO EXCLUDE MR. RUSSELL H. FISHS TESTIMONY* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. Motion Hearing set for 8/29/2013 02:00 PM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 8/22/2013. Replies due by 8/29/2013. (Otteson, James) (Filed on 8/15/2013) (Entered: 08/15/2013)
08/15/2013	490	MOTION in Limine *No. 3 to Preclude Use of Derogatory Characterizations of Patent Holders* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. Motion Hearing set for 8/29/2013 02:00 PM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 8/22/2013. Replies due by 8/29/2013. (Otteson, James) (Filed on 8/15/2013) (Entered: 08/15/2013)
08/15/2013	491	Proposed Voir Dire by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited *Defendants' [Proposed] Special Voir Dire Questions*. (Otteson, James) (Filed on 8/15/2013) (Entered: 08/15/2013)
08/15/2013	492	MOTION in Limine *Defendants' Motion in Limine No. 5 to Exclude the Testimony of David May* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. Motion Hearing set for 8/29/2013 02:00 PM before Magistrate Judge Paul Singh Grewal. Responses due by 8/22/2013. (Attachments: # 1 Declaration of Philip W. Marsh, # 2 Exhibit A − Marsh Declaration, # 3 Exhibit B − Marsh Declaration)(Marsh, Philip) (Filed on 8/15/2013) (Entered: 08/15/2013)
08/15/2013	493	Proposed Form of Verdict by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited *Defendants' [Proposed] Form of Verdict*. (Otteson, James) (Filed on 8/15/2013) (Entered: 08/15/2013)
08/15/2013	494	TRIAL BRIEF *OF DEFENDANTS* by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Otteson, James) (Filed on 8/15/2013) (Entered: 08/15/2013)
08/15/2013	495	MOTION AND MOTION IN LIMINE NO. 4 TO PRECLUDE EXPERT TESTIMONY OF MR. THOMAS A. GAFFORD filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. Motion Hearing set

		for 8/29/2013 02:00 PM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 8/22/2013. Replies due by 8/29/2013. (Attachments: # 1 Declaration DECLARATION OF VINH H. PHAM IN SUPPORT thereof # 2 Exhibit 1 TO DECLARATION OF VINH H. PHAM IN SUPPORT thereof # 3 Exhibit 2 TO DECLARATION OF VINH H. PHAM IN SUPPORT thereof # 4 Exhibit 3 TO DECLARATION OF VINH H. PHAM IN SUPPORT thereof # 5 Exhibit 4 TO DECLARATION OF VINH H. PHAM IN SUPPORT thereof, # 6 Exhibit 5 TO DECLARATION OF VINH H. PHAM IN SUPPORT thereof (Otteson, James) (Filed on 8/15/2013) Modified on 8/16/2013 (cv, COURT STAFF). (Entered: 08/15/2013)
08/15/2013	496	TRIAL BRIEF − *Plaintiffs' Trial Brief* by HTC America, Inc., HTC Corporation. (Attachments: # 1 Appendix A)(Chen, Kyle) (Filed on 8/15/2013) (Entered: 08/15/2013)
08/15/2013	497	*** POSTED IN ERROR *** please see 524 Proposed Form of Verdict by HTC America, Inc., HTC Corporation (Chen, Kyle) (Filed on 8/15/2013) Modified on 8/23/2013 (cv, COURT STAFF). (Entered: 08/15/2013)
08/15/2013	498	JOINT PRETRIAL STATEMENT by Alliacense Limited, HTC America, Inc., HTC Corporation, Patriot Scientific Corporation, Technology Properties Limited (Attachments: # 1 Appendix A, # 2 Appendix B, # 3 Appendix C, # 4 Appendix D, # 5 Appendix E, # 6 Appendix F, # 7 Appendix G, # 8 Appendix H, # 9 Appendix I, # 10 Appendix J, # 11 Appendix K)(Davis, Harold) (Filed on 8/15/2013) Modified on 8/16/2013 (cv, COURT STAFF). (Entered: 08/15/2013)
08/15/2013	499	MOTION in Limine *No. 1 to Preclude Reference to Cooley's Prosecution of the Patents−in−Suit* filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 8/29/2013 02:00 PM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 8/22/2013. Replies due by 8/29/2013. (Attachments: # 1 Proposed Order)(Chen, Kyle) (Filed on 8/15/2013) (Entered: 08/15/2013)
08/15/2013	500	Proposed Voir Dire by HTC America, Inc., HTC Corporation . (Chen, Kyle) (Filed on 8/15/2013) (Entered: 08/15/2013)
08/16/2013	501	MOTION in Limine *No. 2 to Exclude Introduction of Evidence on Hearsay Article "25" Microchips that Shook the World"* filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 8/29/2013 02:00 PM in Courtroom 4, 5th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 8/22/2013. Replies due by 8/29/2013. (Attachments: # 1 Declaration of Kyle D. Chen, # 2 Exhibit A, # 3 Proposed Order)(Chen, Kyle) (Filed on 8/16/2013) (Entered: 08/16/2013)
08/16/2013	502	MOTION in Limine *to Exclude Opinions and Testimony of Dr. Stephen D. Prowse* filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 8/29/2013 02:00 PM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 8/22/2013. Replies due by 8/29/2013. (Weinstein, Mark) (Filed on 8/16/2013) (Entered: 08/16/2013)
08/16/2013	503	MOTION in Limine *No. 4 to Preclude Defendants from Offering Evidence of HTC's Size, Wealth, Overall Revenue or Entire Market Value of the Accused Products* filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 8/29/2013 02:00 PM in Courtroom 4, 5th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 8/22/2013. Replies due by 8/29/2013. (Attachments: # 1 Proposed Order)(Chen, Kyle) (Filed on 8/16/2013) (Entered: 08/16/2013)
08/16/2013	504	MOTION in Limine *No. 3 to Preclude Defendants from Discussing or Entering the Chandrakasan Book into Evidence* filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 8/29/2013 02:00 PM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 8/22/2013. Replies due by 8/29/2013. (Attachments: # 1 Declaration of Kyle D. Chen, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Proposed Order)(Chen, Kyle) (Filed on 8/16/2013) (Entered: 08/16/2013)

08/16/2013	505	Declaration of Mark R. Weinstein in Support of 502 MOTION in Limine *to Exclude Opinions and Testimony of Dr. Stephen D. Prowse* filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F, # 7 Proposed Order)(Related document(s) 502) (Weinstein, Mark) (Filed on 8/16/2013) (Entered: 08/16/2013)
08/16/2013	506	Appendix G − CORRECTION OF DOCKET # [498−7] filed by Alliacense Limited, HTC America, Inc., HTC Corporation, Patriot Scientific Corporation, Technology Properties Limited. (Related document(s) 498) (Chen, Kyle) (Filed on 8/16/2013) Modified on 8/16/2013 (cv, COURT STAFF). (Entered: 08/16/2013)
08/20/2013	508	Joint Administrative Motion to File Under Seal − *Omnibus Motion Regarding Outstanding Motions to Seal* filed by HTC America, Inc., HTC Corporation. (Attachments: # 1 Declaration of Kyle D. Chen, # 2 Declaration of Benjamin Damstedt, # 3 Declaration of David Lansky, # 4 Declaration of Adrienne Dominquez, # 5 Proposed Order)(Chen, Kyle) (Filed on 8/20/2013) (Entered: 08/20/2013)
08/21/2013	509	**FINAL CLAIM CONSTRUCTION ORDER by Judge Paul S. Grewal 356 357 358 374 in case 5:08−cv−00877−PSG; regarding 385 Motion for Reconsideration; 387 388 403 in case 5:08−cv−00882−PSG (psglc2, COURT STAFF) (Filed on 8/21/2013) (Entered: 08/21/2013)**
08/22/2013	510	**ORDER GRANTING JOINT OMNIBUS MOTION REGARDING OUTSTANDING MOTIONS TO SEAL by Judge Paul S. Grewal granting (513) Administrative Motion to File Under Seal; denying as moot (474), (487), and (493) in case 5:08−cv−00877−PSG; granting (508) Administrative Motion to File Under Seal; denying as moot (460), (465), and (468) in case 5:08−cv−00882−PSG (psglc2, COURT STAFF) (Filed on 8/22/2013) (Entered: 08/22/2013)**
08/22/2013	511	RESPONSE (re 499 MOTION in Limine *No. 1 to Preclude Reference to Cooley's Prosecution of the Patents−in−Suit*) *Defendants' Opposition to HTC's Motion in Limine No. 1 to Preclude Reference to Cooley's Prosecution of the Patents−in−Suit* filed byTechnology Properties Limited. (Otteson, James) (Filed on 8/22/2013) (Entered: 08/22/2013)
08/22/2013	512	RESPONSE (re 501 MOTION in Limine *No. 2 to Exclude Introduction of Evidence on Hearsay Article "25" Microchips that Shook the World"*) *Defendants' Opposition to HTC's Motion in Limine No. 2 to Exclude Introduction of Article "25 Microchips That Shook the World"* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Otteson, James) (Filed on 8/22/2013) (Entered: 08/22/2013)
08/22/2013		**Motions terminated: 465 Administrative Motion to File Under Seal filed by Technology Properties Limited, Alliacense Limited, Patriot Scientific Corporation, 460 Administrative Motion to File Under Seal (Dkt. No. 457) filed by HTC America, Inc., HTC Corporation, 468 Administrative Motion to File Under Seal filed by Technology Properties Limited, Alliacense Limited, Patriot Scientific Corporation. pursuant to 510 Order. (cv, COURT STAFF) (Filed on 8/22/2013) (Entered: 08/22/2013)**
08/22/2013	513	Proposed Jury Instructions by Alliacense Limited, HTC America, Inc., HTC Corporation, Patriot Scientific Corporation, Technology Properties Limited *Joint*. (Bettinger, Michael) (Filed on 8/22/2013) (Entered: 08/22/2013)
08/22/2013	514	Proposed Voir Dire by Alliacense Limited, HTC America, Inc., HTC Corporation, Patriot Scientific Corporation, Technology Properties Limited −*Joint Proposed Voir Dire Questions*. (Chen, Kyle) (Filed on 8/22/2013) (Entered: 08/22/2013)
08/22/2013	515	RESPONSE (re 489 MOTION in Limine *DEFENDANTS MOTION IN LIMINE NO. 2 TO EXCLUDE MR. RUSSELL H. FISHS TESTIMONY*) *Plaintiffs Joint Opposition* filed byHTC America, Inc., HTC Corporation. (Davis, Harold) (Filed on 8/22/2013) (Entered: 08/22/2013)
08/22/2013	516	RESPONSE (re 488 MOTION in Limine *No. 1 Regarding Prior Litigations*) *Plaintiffs Joint Opposition To Defendants Motion In Limine No. 1* filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Declaration, # 2 Exhibit 1 to

		Ratinoff Decl., # 3 Exhibit 2 to Ratinoff Decl.)(Ratinoff, Jeffrey) (Filed on 8/22/2013) (Entered: 08/22/2013)
08/22/2013	517	REVISED Proposed Form of Verdict by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited (Otteson, James) (Filed on 8/22/2013) Modified on 8/23/2013 (cv, COURT STAFF). (Entered: 08/22/2013)
08/22/2013	518	RESPONSE (re 490 MOTION in Limine *No. 3 to Preclude Use of Derogatory Characterizations of Patent Holders*) *Plaintiffs' Joint Opposition to Defs' Motion in Limine No. 3* filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Proposed Order)(Chen, Kyle) (Filed on 8/22/2013) (Entered: 08/22/2013)
08/22/2013	519	OBJECTIONS to *Defendants' Submission of Counter Designations and Objections to Plaintiff HTC's Use of Deposition Excerpts and Designated Discovery Responses* by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Appendix A)(Carmack, Thomas) (Filed on 8/22/2013) (Entered: 08/22/2013)
08/22/2013	520	RESPONSE (re 503 MOTION in Limine *No. 4 to Preclude Defendants from Offering Evidence of HTC's Size, Wealth, Overall Revenue or Entire Market Value of the Accused Products*) filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Otteson, James) (Filed on 8/22/2013) (Entered: 08/22/2013)
08/22/2013	521	RESPONSE (re 492 MOTION in Limine *Defendants' Motion in Limine No. 5 to Exclude the Testimony of David May*) filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Declaration of Kyle Chen, # 2 Proposed Order)(Chen, Kyle) (Filed on 8/22/2013) (Entered: 08/22/2013)
08/22/2013	522	OBJECTIONS to *TPL's Deposition Designations* by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 8/22/2013) (Entered: 08/22/2013)
08/22/2013	523	NOTICE by HTC America, Inc., HTC Corporation *of Plaintiffs' Counter−Designations for Witnesses* (Chen, Kyle) (Filed on 8/22/2013) (Entered: 08/22/2013)
08/22/2013	524	AMENDED Proposed Form of Verdict by HTC America, Inc., HTC Corporation *(amendment to − DKT 497)*. (Chen, Kyle) (Filed on 8/22/2013) Modified on 8/23/2013 (cv, COURT STAFF). (Entered: 08/22/2013)
08/22/2013	525	OBJECTIONS to re 493 Proposed Form of Verdict *filed by Defendants* by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 8/22/2013) (Entered: 08/22/2013)
08/22/2013	526	OBJECTIONS to re 500 Proposed Voir Dire, 497 Proposed Form of Verdict *DEFENDANTS' OBJECTIONS TO HTC'S VOIR DIRE AND VERDICT FORMS* by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Carmack, Thomas) (Filed on 8/22/2013) (Entered: 08/22/2013)
08/22/2013	527	Administrative Motion to File Under Seal *Defendants' Opposition to HTC's Motion in Limine No. 3 to Preclude the Chandrakasan Textbook* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Proposed Order)(Carmack, Thomas) (Filed on 8/22/2013) (Entered: 08/22/2013)
08/22/2013	528	EXHIBITS re 521 Opposition/Response to Motion, *to the Declaration of Kyle Chen ISO Opposition to Defs' MIL No. 5* filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D)(Related document(s) 521) (Chen, Kyle) (Filed on 8/22/2013) (Entered: 08/22/2013)
08/22/2013	529	RESPONSE (re 504 MOTION in Limine *No. 3 to Preclude Defendants from Discussing or Entering the Chandrakasan Book into Evidence*, 527 Administrative Motion to File Under Seal *Defendants' Opposition to HTC's Motion in Limine No. 3 to Preclude the Chandrakasan Textbook*) *(PUBLIC VERSION OF OPPOSITION)* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Declaration, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C)(Carmack, Thomas) (Filed on 8/22/2013) (Entered:

		08/22/2013)
08/22/2013	530	Administrative Motion to File Under Seal DOCUMENTS FILED IN SUPPORT OF THEIR OPPOSITION TO PLAINTIFFS MOTIONS TO EXCLUDE THE OPINIONS AND TESTIMONY OF DR. STEPHEN PROWSE filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: #1 Declaration OF DAVID LANSKY IN SUPPORT thereof #2 Proposed Order)(Lansky, David) (Filed on 8/22/2013) Modified on 8/28/2013 (cv, COURT STAFF). (Entered: 08/22/2013)
08/22/2013	531	RESPONSE (re 502 MOTION in Limine *to Exclude Opinions and Testimony of Dr. Stephen D. Prowse*, 530 Administrative Motion to File Under Seal DOCUMENTS FILED IN SUPPORT OF THEIR OPPOSITION TO PLAINTIFFS MOTIONS TO EXCLUDE THE OPINIONS AND TESTIMONY OF DR. STEPHEN PROWSE) filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: #1 Declaration of Mac Leckrone)(Otteson, James) (Filed on 8/22/2013) Modified on 8/28/2013 (cv, COURT STAFF). (Entered: 08/22/2013)
08/22/2013	532	DECLARATION of of David Lansky in Opposition to 531 Opposition/Response to Motion,, 530 Administrative Motion to File Under Seal DOCUMENTS FILED IN SUPPORT OF THEIR OPPOSITION TO PLAINTIFFS MOTIONS TO EXCLUDE THE OPINIONS AND TESTIMONY OF DR. STEPHEN PROWSE filed b Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: #1 Exhibit 1 − 7, #2 Exhibit 8 − 12, #3 Exhibit 13 − 19, #4 Exhibit 20 − 25, #5 Exhibit 26 − 32, #6 Exhibit 33 − 39)(Related document(s) 531 , 530) (Otteson, James) (Filed on 8/22/2013) Modified on 8/28/2013 (cv, COURT STAFF). (Entered: 08/22/2013)
08/22/2013	533	RESPONSE (re 495 MOTION in Limine NO. 4 TO PRECLUDE EXPERT TESTIMONY OF MR. THOMAS A. GAFFORD) filed byHTC America, Inc., HTC Corporation. (Attachments: #1 Declaration Kyle Chen ISO Oppsn to Def MIL No. 4, #2 Exhibit 1 to Kyle Chen's Declaration, #3 Exhibit 2 to Kyle Chen's Declaration, #4 Declaration of Thomas A. Gafford, #5 Proposed Order)(Chen, Kyle) (Filed on 8/22/2013) (Entered: 08/22/2013)
08/23/2013	534	NOTICE by HTC America, Inc., HTC Corporation − *Plaintiffs' Section 282 Statement* (Chen, Kyle) (Filed on 8/23/2013) (Entered: 08/23/2013)
08/26/2013	535	Amended Trial Exhibit List (Appendix J to Joint Pretrial Conference Statement (Dkt. No. 498)) by HTC America, Inc., HTC Corporation.. (Attachments: #1 Appendix J)(Chen, Kyle) (Filed on 8/26/2013) Modified on 8/28/2013 (cv, COURT STAFF). (Entered: 08/26/2013)
08/27/2013	536	Administrative Motion to File Under Seal *Documents Containing LSI Confidential Information* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: #1 Proposed Order)(Lansky, David) (Filed on 8/27/2013) (Entered: 08/27/2013)
08/27/2013	537	NOTICE of Appearance by Irvin E. Tyan *ON BEHALF OF DEFENDANTS TECHNOLOGY PROPERTIES LIMITED AND ALLIACENSE LIMITED* (Tyan, Irvin) (Filed on 8/27/2013) (Entered: 08/27/2013)
08/27/2013	538	NOTICE of Appearance by Jedediah Phillips *ON BEHALF OF DEFENDANTS TECHNOLOGY PROPERTIES LIMITED AND ALLIACENSE LIMITED* (Phillips, Jedediah) (Filed on 8/27/2013) (Entered: 08/27/2013)
08/27/2013	539	NOTICE of Appearance by Vinh Huy Pham *ON BEHALF OF DEFENDANTS TECHNOLOGY PROPERTIES LIMITED AND ALLIACENSE LIMITED* (Pham, Vinh) (Filed on 8/27/2013) (Entered: 08/27/2013)
08/27/2013	540	Declaration of Kyle D. Chen in Support of 457 MOTION for Summary Judgment *Plaintiffs Notice of Motion and Motion for Summary Judgment of Non−Infringement and No Willful Infringement of U.S. Patent No. 5,809,336 AMENDED DECLARATION* filed byHTC America, Inc., HTC Corporation. (Attachments: #1 Exhibit 1, #2 Exhibit 2, #3 Exhibit 3 − Part 1, #4 Exhibit 3 − Part 2, #5 Exhibit 3 − Part 3, #6 Exhibit 3 − Part 4, #7 Exhibit 3 −Part 5, #8

		Exhibit 3 − Part 6, # 9 Exhibit 3 − Part 7, # 10 Exhibit 4, # 11 Exhibit 5, # 12 Exhibit 6, # 13 Exhibit 7, # 14 Exhibit 8, # 15 Exhibit 9, # 16 Exhibit 10, # 17 Exhibit 11, # 18 Exhibit 12, # 19 Exhibit 13, # 20 Exhibit 14, # 21 Exhibit 15, # 22 Exhibit 16, # 23 Exhibit 17)(Related document(s) 457) (Chen, Kyle) (Filed on 8/27/2013) (Entered: 08/27/2013)
08/27/2013	541	Declaration of Thomas A. Gafford in Support of 457 MOTION for Summary Judgment *Plaintiffs Notice of Motion and Motion for Summary Judgment of Non−Infringement and No Willful Infringement of U.S. Patent No. 5,809,336* filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit 1 PUBLIC VERSION, # 2 Exhibit 2)(Related document(s) 457) (Chen, Kyle) (Filed on 8/27/2013) (Entered: 08/27/2013)
08/27/2013	542	DOCUMENT E−FILED UNDER SEAL re 510 Order on Administrative Motion to File Under Seal,,, *Exhibit 1 to the Declaration of Thomas A. Gafford ISO Plf's Motion for Summary Judgment of Non−Infringement* by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 8/27/2013) (Entered: 08/27/2013)
08/27/2013	543	REPLY (re 457 MOTION for Summary Judgment *Plaintiffs Notice of Motion and Motion for Summary Judgment of Non−Infringement and No Willful Infringement of U.S. Patent No. 5,809,336*) *CORRECTION OF DOCKET Nos. 476 477* filed byHTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 8/27/2013) (Entered: 08/27/2013)
08/27/2013	544	Declaration of Kyle D. Chen in Support of 485 Reply to Opposition/Response, 543 Reply to Opposition/Response, *SUPPLEMENTAL DECLARATION* filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit 18, # 2 Exhibit 19, # 3 Exhibit 20, # 4 Exhibit 21, # 5 Exhibit 22)(Related document(s) 485 , 543) (Chen, Kyle) (Filed on 8/27/2013) (Entered: 08/27/2013)
08/27/2013	545	Declaration of Mark R. Weinstein in Support of 502 MOTION in Limine *to Exclude Opinions and Testimony of Dr. Stephen D. Prowse*, 505 Declaration in Support, filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 *** POSTED IN ERROR *** please see 551 Exhibit D − Exhibit D − PUBLIC VERSION, # 5 Exhibit E, # 6 Exhibit F)(Related document(s) 502 , 505) (Weinstein, Mark) (Filed on 8/27/2013) Modified on 8/29/2013 (cv, COURT STAFF). (Entered: 08/27/2013)
08/27/2013	546	DOCUMENT E−FILED UNDER SEAL re 510 Order on Administrative Motion to File Under Seal,,, *Exhibit D to the Declaration of Mark R. Weinstein ISO HTC Daubert Motion to Exclude Damages Opinons of Stephen D. Prowse, Ph.D. DKT Nos. 502, 505, 545* by HTC America, Inc., HTC Corporation. (Weinstein, Mark) (Filed on 8/27/2013) (Entered: 08/27/2013)
08/27/2013	547	Declaration of Kyle D. Chen in Support of 504 MOTION in Limine *No. 3 to Preclude Defendants from Discussing or Entering the Chandrakasan Book into Evidence* filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D)(Related document(s) 504) (Weinstein, Mark) (Filed on 8/27/2013) (Entered: 08/27/2013)
08/28/2013	548	OBJECTIONS to *Plaintiffs' Deposition Counter Designations* by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Carmack, Thomas) (Filed on 8/28/2013) (Entered: 08/28/2013)
08/28/2013	549	OBJECTIONS to *TPL's Proposed Trial Exhibits* by HTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit 1)(Chen, Kyle) (Filed on 8/28/2013) (Entered: 08/28/2013)
08/29/2013	550	OBJECTIONS to *Plaintiffs' Trial Exhibits* by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Phillips, Jedediah) (Filed on 8/29/2013) (Entered: 08/29/2013)
08/29/2013	551	Corrected EXHIBIT D to Weinstein Declaration filed by HTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit D)(Related document(s) 545) (Chen, Kyle) (Filed on 8/29/2013) Modified on 8/29/2013 (cv, COURT STAFF). (Entered: 08/29/2013)

08/29/2013	552	Exhibit List *Defendants' Revised Trial Exhibit List* by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited.. (Phillips, Jedediah) (Filed on 8/29/2013) (Entered: 08/29/2013)
08/29/2013	553	Minute Entry: Pretrial Conference and Hearing on Motions in Limine held 8/29/2013 before Magistrate Judge Paul S. Grewal. Any evidentiary issues to be addressed mornings before trial. Jury instructions deferred until charging conference. The court takes matters under submission; written order after hearing to be issued. (Court Reporter FTR: (2:01 to 4:21) (ofr, COURT STAFF) (Date Filed: 8/29/2013) (Entered: 08/29/2013)
09/03/2013	554	OBJECTIONS to *DEFENDANTS OBJECTIONS AND COUNTER DESIGNATIONS TO PLAINTIFFS SUPPLEMENTAL DEPOSITION DESIGNATIONS* by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Phillips, Jedediah) (Filed on 9/3/2013) (Entered: 09/03/2013)
09/05/2013	555	NOTICE of Change In Counsel by James Carl Otteson *NOTICE OF WITHDRAWAL OF CERTAIN COUNSEL FOR DEFENDANTS TECHNOLOGY PROPERTIES LIMITED AND ALLIACENSE LIMITED* (Otteson, James) (Filed on 9/5/2013) (Entered: 09/05/2013)
09/05/2013	556	EXHIBITS re 466 Opposition/Response to Motion, 467 Declaration in Support, *(EXHIBITS A and B TO THOMAS CARMARCK DECLARATION)* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Exhibit B)(Related document(s) 466 , 467) (Carmack, Thomas) (Filed on 9/5/2013) (Entered: 09/05/2013)
09/05/2013	557	**ORDER GRANTING 527 ADMINISTRATIVE MOTION TO FILE UNDER SEAL entered by Magistrate Judge Paul Singh Grewal. (This is a text−only entry generated by the court. There is no document associated with this entry.) (Entered: 09/05/2013)**
09/05/2013	558	**ORDER GRANTING 530 ADMINISTRATIVE MOTION TO FILE UNDER SEAL entered by Magistrate Judge Paul Singh Grewal. (This is a text−only entry generated by the court. There is no document associated with this entry.) (Entered: 09/05/2013)**
09/05/2013	559	**ORDER GRANTING 536 ADMINISTRATIVE MOTION TO FILE UNDER SEAL entered by Magistrate Judge Paul Singh Grewal. (This is a text−only entry generated by the court. There is no document associated with this entry.) (Entered: 09/05/2013)**
09/05/2013	560	EXHIBITS re 471 Declaration in Opposition, *(EXHIBITS I, J, K, L, AND R TO IRVIN TYAN DECLARATION)* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Exhibit J, # 2 Exhibit K, # 3 Exhibit L, # 4 Exhibit R)(Related document(s) 471) (Tyan, Irvin) (Filed on 9/5/2013) (Entered: 09/05/2013)
09/06/2013	561	NOTICE by HTC America, Inc., HTC Corporation *re Notice of Issuance of Final Initial Determination by the International Trade Commission re U.S. Patent No. 5,809,336* (Attachments: # 1 Exhibit A)(Weinstein, Mark) (Filed on 9/6/2013) (Entered: 09/06/2013)
09/06/2013	562	**ORDER GRANTING 453 MOTION FOR SEPARATE TRIAL entered by Magistrate Judge Paul Singh Grewal. The court plainly has the discretion to order separate trials. That discretion is best exercised by giving HTC the separate trial it wants. The court will preserve the current trial schedule, with Acer first up. HTC should be prepared to begin its trial immediately thereafter. (This is a text−only entry generated by the court. There is no document associated with this entry.) (Entered: 09/06/2013)**
09/06/2013	563	**ORDER DENYING MOTION TO EXCLUDE EXPERT REPORT OF DR. STEPHEN PROWSE by Judge Paul S. Grewal denying 502 Motion in Limine (psglc2, COURT STAFF) (Filed on 9/6/2013) (Entered: 09/06/2013)**
09/06/2013	564	**ORDER ON MOTIONS IN LIMINE by Judge Paul S. Grewal granting in part and denying in part 488 , 489 , 490 , 492 , 495 , 499 , 501 , 503 , and 504**

		(psglc2, COURT STAFF) (Filed on 9/6/2013) (Entered: 09/06/2013)
09/06/2013	565	MOTION to Quash *NON−PARTY TEXAS INSTRUMENTS INCORPORATEDS MOTION TO QUASH THE TRIAL SUBPOENA SERVED BY DEFENDANTS* filed by Texas Instruments Incorporated. Motion Hearing set for 10/15/2013 10:00 AM in Courtroom 4, 5th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 9/20/2013. Replies due by 9/27/2013. (Attachments: #1 Declaration of Ethan Davis, #2 Declaration of Sarah Vollbrecht, #3 Exhibit 1, #4 Exhibit 2, #5 Exhibit 3, #6 Exhibit 4, #7 Exhibit 5, #8 Proposed Order)(Sharma, Anupam) (Filed on 9/6/2013) (Entered: 09/06/2013)
09/10/2013	566	TRANSCRIPT ORDER by HTC America, Inc., HTC Corporation for Court Reporter Summer Fisher. (Chen, Kyle) (Filed on 9/10/2013) (Entered: 09/10/2013)
09/10/2013	567	Transcript of Proceedings held on 08/13/13, before Judge Paul S. Grewal. Court Reporter/Transcriber Summer Fisher, Telephone number 408−288−6150 summer_fisher@cand.uscourts.gov. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 12/9/2013. (Fisher, Summer) (Filed on 9/10/2013) (Entered: 09/10/2013)
09/11/2013	568	Administrative Motion to File Under Seal *Portions of the Expert Report of Stephen D. Prowse* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: #1 Declaration of David Lansky, #2 Declaration of Harold H. Davis, #3 Declaration of Kyle D. Chen, #4 Proposed Order)(Lansky, David) (Filed on 9/11/2013) (Entered: 09/11/2013)
09/11/2013	569	Emergency MOTION to Strike *Defendants' Emergency Motion to Strike HTC's Improper Ex Parte Communication to the Court, and for Sanctions; Memorandum of Points and Authorities* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. Responses due by 9/25/2013. Replies due by 10/2/2013. (Attachments: #1 Declaration of James C. Otteson, #2 Exhibit 1 to Otteson Declaration, #3 Exhibit 2 to Otteson Declaration)(Otteson, James) (Filed on 9/11/2013) (Entered: 09/11/2013)
09/12/2013	570	MOTION to Quash *THE SECOND TRIAL SUBPOENA SERVED BY DEFENDANTS* filed by Texas Instruments Incorporated. Motion Hearing set for 9/17/2013 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 9/13/2013. Replies due by 9/16/2013. (Attachments: #1 Declaration of Sarah Vollbrecht, #2 Exhibit 6, #3 Proposed Order)(Sharma, Anupam) (Filed on 9/12/2013) Modified on 9/19/2013 (ofr, COURT STAFF). (Entered: 09/12/2013)
09/12/2013	571	STIPULATION WITH PROPOSED ORDER re 570 MOTION to Quash *THE SECOND TRIAL SUBPOENA SERVED BY DEFENDANTS − STIPULATED REQUEST FOR ORDER CHANGING TIME AND EXPEDITING BRIEFING SCHEDULE PURSUANT TO CIV. L. R. 6−2* filed by Texas Instruments Incorporated. (Attachments: #1 Declaration of Anupam Sharma, #2 Proposed Order)(Sharma, Anupam) (Filed on 9/12/2013) (Entered: 09/12/2013)
09/12/2013	572	CLERK'S NOTICE RESCHEDULING MOTIONS AND COURT MODIFYING BRIEFING SCHEDULE, Re (567 and 570 in 5:08−cv−00877−PSG) and (565 and 570 in 5:08−cv−00882−PSG): The court modifies the briefing schedule as follows: Opposition by 9/17/2013. No reply will be considered. Motions are rescheduled for 9/20/2013 at 10:00 AM (SPECIAL SET) in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. *****This is a text only docket entry, there is no document associated with this notice.***** (ofr, COURT STAFF) (Filed on 9/12/2013) (Entered: 09/12/2013)
09/12/2013	573	EXHIBITS re 568 Administrative Motion to File Under Seal *Portions of the Expert Report of Stephen D. Prowse (Redacted Version of Expert Report of Dr. Stephen D. Prowse)* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Related document(s) 568) (Lansky, David) (Filed on 9/12/2013) (Entered: 09/12/2013)

09/12/2013	574	RESPONSE (re 569 Emergency MOTION to Strike *Defendants' Emergency Motion to Strike HTC's Improper Ex Parte Communication to the Court, and for Sanctions; Memorandum of Points and Authorities*) filed byHTC America, Inc., HTC Corporation. (Attachments: #1 Declaration Heidi L. Keefe, #2 Exhibit A − Keefe Decl., #3 Exhibit B − Keefe Decl., #4 Exhibit C − Keefe Decl., #5 Declaration Stephen R. Smith, #6 Exhibit A − Smith Decl., #7 Declaration Benjamin Damstedt, #8 Exhibit A − Damstedt Decl.)(Keefe, Heidi) (Filed on 9/12/2013) (Entered: 09/12/2013)
09/12/2013	575	DOCUMENT E−FILED UNDER SEAL re 557 Order on Administrative Motion to File Under Seal *Defendants' Opposition to HTC's Motion in Limine No. 3 to Preclude the Chandrakasan Textbook* by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Otteson, James) (Filed on 9/12/2013) (Entered: 09/12/2013)
09/12/2013	576	DOCUMENT E−FILED UNDER SEAL re 559 Order on Administrative Motion to File Under Seal *Exhibit M to the Omnibus Declaration of Irvin Tyan in Support of Defendants' Oppositions to Plaintiffs' Motions for Summary Judgment* by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Tyan, Irvin) (Filed on 9/12/2013) (Entered: 09/12/2013)
09/13/2013	577	NOTICE by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited *Notice Regarding Defendants' Request for Telephone Hearing re Emergency Motion to Strike HTC's Improper Ex Parte Communication to the Court* (Otteson, James) (Filed on 9/13/2013) (Entered: 09/13/2013)
09/13/2013	578	CLERK'S NOTICE SETTING HEARING re 569 Defendants' Emergency Motion to Strike HTC's Improper Ex Parte Communication to the Court, and for Sanctions: Motion Hearing set for 9/13/2013 at 3:30 PM (SPECIAL SET) in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Counsel is instructed to contact CourtCall at 866−582−6878 to arrange for telephonic appearance. *****This is a text only docket entry, there is no document associated with this notice.***** (ofr, COURT STAFF) (Filed on 9/13/2013) (Entered: 09/13/2013)
09/13/2013	579	Minute Entry: Motion Hearing held on 9/13/2013 before Magistrate Judge Paul S. Grewal re 569 Defendants' Emergency Motion to Strike HTC's Improper Ex Parte Communication to the Court, and for Sanctions: The court will review initial determination. Court to issue order after hearing. (Court Reporter: Summer Fisher.) (ofr, COURT STAFF) (Date Filed: 9/13/2013) (Entered: 09/13/2013)
09/16/2013	580	TRANSCRIPT ORDER for Daily Trial by HTC America, Inc., HTC Corporation. (Lemieux, Ronald) (Filed on 9/16/2013) (Entered: 09/16/2013)
09/16/2013	581	**ORDER GRANTING 568 ADMINISTRATIVE MOTION TO FILE UNDER SEAL entered by Magistrate Judge Paul Singh Grewal. (This is a text−only entry generated by the court. There is no document associated with this entry.) (Entered: 09/16/2013)**
09/16/2013	582	**ORDER DENYING AS MOOT 571 STIPULATION entered by Magistrate Judge Paul Singh Grewal. The briefing and hearing schedule is set in Docket No. 572. (This is a text−only entry generated by the court. There is no document associated with this entry.) (Entered: 09/16/2013)**
09/17/2013	583	TRANSCRIPT ORDER for Daily Trial by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Otteson, James) (Filed on 9/17/2013) (Entered: 09/17/2013)
09/17/2013	584	TRANSCRIPT ORDER by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited for Court Reporter FTR − San Jose. (Carmack, Thomas) (Filed on 9/17/2013) ***TRANSCRIPT ORDER CANCELLED 9/30/2103***. Modified on 11/5/2013 (sp, COURT STAFF). (Entered: 09/17/2013)
09/17/2013	585	**ORDER RE: MOTIONS FOR SUMMARY JUDGMENT by Judge Paul S. Grewal granting−in−part 457 and 458 (psglc2, COURT STAFF) (Filed on 9/17/2013) (Entered: 09/17/2013)**

09/17/2013	586	RESPONSE (re 565 MOTION to Quash *NON−PARTY TEXAS INSTRUMENTS INCORPORATEDS MOTION TO QUASH THE TRIAL SUBPOENA SERVED BY DEFENDANTS*) *DEFENDANTS COMBINED OPPOSITIONS TO NON−PARTY TEXAS INSTRUMENTS MOTIONS TO QUASH TRIAL SUBPOENA* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Declaration DECLARATION OF IRVIN E. TYAN IN SUPPORT OF DEFENDANTS COMBINED OPPOSITIONS TO NON−PARTY TEXAS INSTRUMENTS MOTIONS TO QUASH TRIAL SUBPOENA, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Exhibit G, # 9 Exhibit H, # 10 Exhibit I, # 11 Exhibit J, # 12 Exhibit K, # 13 Exhibit L, # 14 Exhibit M, # 15 Exhibit N)(Tyan, Irvin) (Filed on 9/17/2013) (Entered: 09/17/2013)
09/17/2013	587	Declaration of PHILIP W. MARSH in Support of 586 Opposition/Response to Motion,,, *IN SUPPORT OF DEFENDANTS COMBINED OPPOSITIONS TO NON−PARTY TEXAS INSTRUMENTS MOTIONS TO QUASH TRIAL SUBPOENA* filed byAlliacense Limited, Technology Properties Limited. (Related document(s) 586) (Marsh, Philip) (Filed on 9/17/2013) (Entered: 09/17/2013)
09/18/2013	588	STIPULATION WITH PROPOSED ORDER − *Joint Request to Dismiss All Claims Relating to U.S. Patent No. 5,530,890 Under F.R.C.P. 41(a)(2); Proposed Order Thereon* filed by HTC America, Inc., HTC Corporation. (Weinstein, Mark) (Filed on 9/18/2013) (Entered: 09/18/2013)
09/18/2013	589	Emergency MOTION Clarification re 564 Order on Motion in Limine,,,,,,,, − *Emergency Motion for Clarification of Order on TPL's MIL No. 1* filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 9/20/2013 09:30 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 9/19/2013. (Attachments: # 1 Declaration Kyle D. Chen, # 2 Proposed Order)(Chen, Kyle) (Filed on 9/18/2013) (Entered: 09/18/2013)
09/18/2013	590	Emergency MOTION Addendum re 513 Proposed Jury Instructions filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 9/20/2013 09:30 AM in Courtroom 4, 5th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 9/19/2013. (Attachments: # 1 Declaration Kyle D. Chen, # 2 Proposed Order)(Chen, Kyle) (Filed on 9/18/2013) (Entered: 09/18/2013)
09/18/2013	591	NOTICE by HTC America, Inc., HTC Corporation re 589 Emergency MOTION Clarification re 564 Order on Motion in Limine,,,,,,,, − *Emergency Motion for Clarification of Order on TPL's MIL No. 1*, 590 Emergency MOTION Addendum re 513 Proposed Jury Instructions − *NOTICE REGARDING PLAINTIFFS' REQUEST FOR TELEPHONE HEARING RE EMERGENCY MOTIONS FOR CLARIFICATION AND ADDENDUM TO JURY INSTRUCTIONS* (Chen, Kyle) (Filed on 9/18/2013) (Entered: 09/18/2013)
09/18/2013	592	RESPONSE (re 589 Emergency MOTION Clarification re 564 Order on Motion in Limine,,,,,,,, − *Emergency Motion for Clarification of Order on TPL's MIL No. 1*) *Defendants' Opposition to Emergency Motion for Clarification of Order on TPL's MIL No. 1* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Carmack, Thomas) (Filed on 9/18/2013) (Entered: 09/18/2013)
09/18/2013	593	Exhibit List *DEFENDANTS REVISED TRIAL EXHIBIT LIST* by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited.. (Otteson, James) (Filed on 9/18/2013) (Entered: 09/18/2013)
09/19/2013	594	**ORDER GRANTING JOINT REQUEST TO DISMISS ALL CLAIMS RELATING TO U.S. PATENT NO. 5,530,890 by Judge Paul S. Grewal granting 588 (psglc2, COURT STAFF) (Filed on 9/19/2013) (Entered: 09/19/2013)**
09/19/2013	595	CLERK'S NOTICE SETTING HEARING as to 589 Emergency Motion for Clarification of Order on TPL's MIL No. 1 and 590 Emergency MOTION Addendum re 513 Proposed Jury Instructions: Hearing set for 9/20/2013 at 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. *****This is a text only docket entry, there is no document associated with this notice.***** (ofr, COURT STAFF) (Filed on 9/19/2013) (Entered:

		09/19/2013)
09/19/2013	596	RESPONSE (re 590 Emergency MOTION Addendum re 513 Proposed Jury Instructions) *Defendants' Opposition to Emergency Motion for Addendum to Jury Instructions* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Otteson, James) (Filed on 9/19/2013) (Entered: 09/19/2013)
09/19/2013	597	NOTICE by HTC America, Inc., HTC Corporation − *Joint Motion for Order Granting Permission to Bring Equipment for Use During Trial* (Attachments: # 1 Proposed Order)(Chen, Kyle) (Filed on 9/19/2013) (Entered: 09/19/2013)
09/19/2013	598	MOTION to Appear by Telephone filed by Patriot Scientific Corporation. (Hoge, Charles) (Filed on 9/19/2013) (Entered: 09/19/2013)
09/19/2013	599	DOCUMENT E−FILED UNDER SEAL re 558 Order on Administrative Motion to File Under Seal *(Exhibit A to Declaration of Mac Leckrone ISO Defendants' Opposition to Plaintiffs' Motions in Limine)* by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Lansky, David) (Filed on 9/19/2013) (Entered: 09/19/2013)
09/19/2013	600	DOCUMENT E−FILED UNDER SEAL re 558 Order on Administrative Motion to File Under Seal *(Exhibits 5, 6, and 21 to the Declaration of David Lansky ISO Defendants' Opposition to Plaintiff's Daubert Motion to Exclude Prowse)* by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Exhibit 6, # 2 Exhibit 21)(Lansky, David) (Filed on 9/19/2013) (Entered: 09/19/2013)
09/19/2013	601	**ORDER GRANTING JOINT MOTION FOR PERMISSION TO BRING EQUIPMENT FOR USE DURING TRIAL, granting 597 . Signed by Judge Paul S. Grewal on 9/19/2013. (ofr, COURT STAFF) (Filed on 9/19/2013) (Entered: 09/20/2013)**
09/19/2013	602	**APPLICATION AND ORDER GRANTING DEFENDANT AND COUNTER−CLAIMANT PATRIOTIC SCIENTIFIC CORPORATION'S REQUEST TO APPEAR TELEPHONICALLY AT SEPTEMBER 20, 2013 HEARING by Judge Paul S. Grewal, granting 598 : Counsel is instructed to contact CourtCall at 866−582−6878 to arrange for telephonic appearance. (ofr, COURT STAFF) (Filed on 9/19/2013) (Entered: 09/20/2013)**
09/20/2013	603	DOCUMENT E−FILED UNDER SEAL re 581 Order on Administrative Motion to File Under Seal *(Expert Report of Dr. Stephen D. Prowse)* by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Lansky, David) (Filed on 9/20/2013) (Entered: 09/20/2013)
09/20/2013	604	REPLY (re 590 Emergency MOTION Addendum re 513 Proposed Jury Instructions) *(to Assist the Court in Locating Intrinsic Records of the '336 Patent on the Docket)* filed byHTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 9/20/2013) (Entered: 09/20/2013)
09/20/2013	605	Minute Entry: Motion Hearing held on 9/20/2013 before Magistrate Judge Paul S. Grewal re 565 MOTION to Quash, 570 MOTION to Quash, 589 Emergency MOTION for Clarification and 590 Emergency MOTION for Addendum to Jury Instructions: Non−Party Texas Instruments, Inc.'s Motions to Quash and Plaintiff HTC's Emergency Motion for Addendum to Jury Instructions are taken under submission; written order after hearing to be issued. Plaintiff HTC's Emergency Motion for Clarification is denied. Parties are allotted 1 hour each for opening statements and closing arguments, 15 hours each for direct and cross−examination (exclusive of jury selection), and 30 minutes each for voir dire. 9 jurors will be seated, no alternates, 3 peremptories per side. Attorneys to be present at 9:00 a.m. to address any evidentiary issues. Trial on 9/24/13 to begin at 12:30 p.m. (Court Reporter: Lee−Anne Shortridge.) (ofr, COURT STAFF) (Date Filed: 9/20/2013) (Entered: 09/20/2013)
09/20/2013	606	**ORDER DENYING TEXAS INSTRUMENTS' MOTION TO QUASH THE TRIAL SUBPOENA by Judge Paul S. Grewal denying 565 Motion to Quash; denying 570 Motion to Quash (psglc2, COURT STAFF) (Filed on 9/20/2013) (Entered: 09/20/2013)**

09/20/2013	607	**ORDER RE: EMERGENCY MOTION FOR ADDENDUM TO JURY INSTRUCTIONS by Judge Paul S. Grewal RE: 590 (psglc2, COURT STAFF) (Filed on 9/20/2013) (Entered: 09/20/2013)**
09/20/2013	608	**ORDER RE: PRELIMINARY JURY INSTRUCTIONS 513 . Signed by Judge Paul S. Grewal on September 20, 2013. (psglc2, COURT STAFF) (Filed on 9/20/2013) (Entered: 09/20/2013)**
09/21/2013	609	Emergency MOTION Clarification re 607 Order on Motion for Miscellaneous Relief *re Addendum to Jury Instructions* filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 9/23/2013 09:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 9/22/2013. (Attachments: # 1 Declaration of Kyle D. Chen, # 2 Proposed Order)(Chen, Kyle) (Filed on 9/21/2013) (Entered: 09/21/2013)
09/22/2013	610	Exhibit List *DEFENDANTS REVISED TRIAL EXHIBIT LIST* by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited.. (Otteson, James) (Filed on 9/22/2013) (Entered: 09/22/2013)
09/22/2013	611	NOTICE by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited *(NOTICE OF DEFENDANTS' REQUESTED CHANGES TO PRELIMINARY JURY INSTRUCTIONS)* (Attachments: # 1 Exhibit A, # 2 Exhibit B)(Otteson, James) (Filed on 9/22/2013) (Entered: 09/22/2013)
09/22/2013	612	NOTICE by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited re 609 Emergency MOTION Clarification re 607 Order on Motion for Miscellaneous Relief *re Addendum to Jury Instructions (DEFENDANTS' NOTICE OF NONOPPOSITION TO PLAINIFFS' EMERGENCY MOTION FOR CLARIFICATION OF ORDER ON ADDENDUM TO JURY INSTRUCTIONS)* (Attachments: # 1 Proposed Order)(Otteson, James) (Filed on 9/22/2013) (Entered: 09/22/2013)
09/22/2013	613	OBJECTIONS to re 611 Notice (Other), *Defendants' Requested Changes to Preliminary Jury Instructions* by HTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit 1)(Chen, Kyle) (Filed on 9/22/2013) (Entered: 09/22/2013)
09/23/2013	614	Emergency MOTION Emergency Motion for Limiting Jury Instruction filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. Motion Hearing set for 9/23/2013 09:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 10/7/2013. Replies due by 10/15/2013. (Attachments: # 1 Proposed Order)(Carmack, Thomas) (Filed on 9/23/2013) (Entered: 09/23/2013)
09/23/2013	615	**ORDER RE: REVISIONS TO PRELIMINARY JURY INSTRUCTIONS. Signed by Judge Paul S. Grewal on September 23, 2013. (psglc2, COURT STAFF) (Filed on 9/23/2013) (Entered: 09/23/2013)**
09/23/2013	616	**ORDER GRANTING EMERGENCY MOTION FOR CLARIFICATION OF ORDER ON ADDENDUM TO JURY INSTRUCTIONS by Judge Paul S. Grewal granting 609 (psglc2, COURT STAFF) (Filed on 9/23/2013) (Entered: 09/23/2013)**
09/23/2013	617	**ORDER GRANTING EMERGENCY MOTION FOR LIMITING INSTRUCTION by Judge Paul S. Grewal granting 614 (psglc2, COURT STAFF) (Filed on 9/23/2013) (Entered: 09/23/2013)**
09/23/2013	618	STIPULATION filed by Alliacense Limited, HTC America, Inc., HTC Corporation, Patriot Scientific Corporation, Qualcomm Inc., Technology Properties Limited. (Otteson, James) (Filed on 9/23/2013) (Entered: 09/23/2013)
09/23/2013	624	Minute Entry: Jury Selection and Trial (Day 1) begun on 9/23/2013 before Magistrate Judge Paul S. Grewal. (Court Reporter: Lee−Anne Shortridge.) (ofr, COURT STAFF) (Date Filed: 9/23/2013) (Entered: 09/24/2013)
09/23/2013	625	AMENDED Minute Entry Correcting Case Number: Jury Selection and Trial (Day 1) begun on 9/23/2013 before Magistrate Judge Paul S. Grewal. Jury Trial (Day 2) set for 9/24/2013 at 9:00 AM in Courtroom 5, 4th Floor, San Jose. (Court Reporter:

		Lee−Anne Shortridge.) (ofr, COURT STAFF) (Date Filed: 9/23/2013) (Entered: 09/24/2013)
09/24/2013	619	Emergency MOTION to Strike *and Motion for Limiting Instruction Regarding Mr. Moore's Testimony Regarding Green Arrays* filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 9/24/2013 09:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 9/24/2013. (Attachments: # 1 Proposed Order)(Chen, Kyle) (Filed on 9/24/2013) (Entered: 09/24/2013)
09/24/2013	620	Emergency MOTION Addendum to Jury Instructions re 618 Stipulation *(JOINT EMERGENCY MOTION FOR ADDENDUM TO JURY INSTRUCTIONS RE QUALCOMM STIPULATION)* filed by Alliacense Limited, HTC America, Inc., HTC Corporation, Patriot Scientific Corporation, Technology Properties Limited. Motion Hearing set for 9/24/2013 09:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 9/24/2013. Replies due by 9/24/2013. (Attachments: # 1 Proposed Order)(Otteson, James) (Filed on 9/24/2013) (Entered: 09/24/2013)
09/24/2013	621	Emergency MOTION Curative Instruction regarding Opening Statement *(DEFENDANTS' EMERGENCY MOTION FOR CURATIVE INSTRUCTION REGARDING OPENING STATEMENT)* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. Motion Hearing set for 9/24/2013 09:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 9/24/2013. Replies due by 9/24/2013. (Attachments: # 1 Proposed Order)(Otteson, James) (Filed on 9/24/2013) (Entered: 09/24/2013)
09/24/2013	622	Emergency MOTION to Strike *and Motion for Limiting Instruction Regarding Mr. Moore's Testimony Regardng Green Arrays* filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 9/24/2013 09:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 10/8/2013. Replies due by 10/15/2013. (Keefe, Heidi) (Filed on 9/24/2013) (Entered: 09/24/2013)
09/24/2013	623	**ORDER GRANTING JOINT EMERGENCY MOTION FOR ADDENDUM TO JURY INSTRUCTIONS RE: QUALCOMM STIPULATION by Judge Paul S. Grewal granting 620 (psglc2, COURT STAFF) (Filed on 9/24/2013) (Entered: 09/24/2013)**
09/24/2013	626	RESPONSE (re 621 Emergency MOTION Curative Instruction regarding Opening Statement *(DEFENDANTS' EMERGENCY MOTION FOR CURATIVE INSTRUCTION REGARDING OPENING STATEMENT)*) filed byHTC America, Inc., HTC Corporation. (Keefe, Heidi) (Filed on 9/24/2013) (Entered: 09/24/2013)
09/24/2013	627	Minute Entry: Jury Trial (Day 2) held on 9/24/2013 before Magistrate Judge Paul S. Grewal. (Court Reporter: Lee−Anne Shortridge.) (ofr, COURT STAFF) (Date Filed: 9/24/2013) (Entered: 09/25/2013)
09/25/2013	628	Minute Entry: Jury Trial (Day 3) held on 9/25/2013 before Magistrate Judge Paul S. Grewal (Court Reporter: Lee−Anne Shortridge.) (ofr, COURT STAFF) (Date Filed: 9/25/2013) (Entered: 09/26/2013)
09/26/2013	629	Minute Entry: Jury Trial (Day 4) held on 9/26/2013 before Magistrate Judge Paul S. Grewal. (Court Reporter: Lee−Anne Shortridge.) (ofr, COURT STAFF) (Date Filed: 9/26/2013) (Entered: 09/27/2013)
09/27/2013	630	Emergency MOTION for Hearing *for Curative Instruction* filed by HTC America, Inc., HTC Corporation. (Attachments: # 1 Proposed Order)(Chen, Kyle) (Filed on 9/27/2013) (Entered: 09/27/2013)
09/27/2013	644	Minute Entry: Jury Trial (Day 5) held on 9/27/2013 before Magistrate Judge Paul S. Grewal (Court Reporter: Lee−Anne Shortridge.) (ofr, COURT STAFF) (Date Filed: 9/27/2013) (Entered: 09/30/2013)
09/29/2013	631	NOTICE of Appearance by Dena Chen (Chen, Dena) (Filed on 9/29/2013) (Entered: 09/29/2013)

09/29/2013	632	NOTICE of Appearance by Lia Charlotte Smith (Smith, Lia) (Filed on 9/29/2013) (Entered: 09/29/2013)
09/29/2013	633	Emergency MOTION enforcement of MIL order re 564 Order on Motion in Limine,,,,,,,, filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 9/30/2013 09:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 9/30/2013. (Attachments: # 1 Proposed Order)(Chen, Kyle) (Filed on 9/29/2013) (Entered: 09/29/2013)
09/29/2013	634	Emergency MOTION Clarification of Court's Order Excluding Exhibits 1517, 1519, 1528 and 1536 filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 9/30/2013 09:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 9/30/2013. (Attachments: # 1 Proposed Order)(Chen, Kyle) (Filed on 9/29/2013) (Entered: 09/29/2013)
09/29/2013	635	Emergency MOTION order to exclude the undisclosed applications on the HTC Thunderbolt filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 9/30/2013 09:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 9/30/2013. (Attachments: # 1 Declaration of Kyle D. Chen, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Proposed Order)(Chen, Kyle) (Filed on 9/29/2013) (Entered: 09/29/2013)
09/30/2013	636	RESPONSE (re 633 Emergency MOTION enforcement of MIL order re 564 Order on Motion in Limine,,,,,,,,) *(OPPOSIION TO EMERGENCY MOTION TO ENFORCE MIL ORDER)* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Phillips, Jedediah) (Filed on 9/30/2013) (Entered: 09/30/2013)
09/30/2013	637	RESPONSE (re 634 Emergency MOTION Clarification of Court's Order Excluding Exhibits 1517, 1519, 1528 and 1536) *(OPPOSITION TO EMERGENCY MOTION TO CLARIFY THE COURT'S ORDER EXCLUDING EXHIBITS)* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Lansky, David) (Filed on 9/30/2013) (Entered: 09/30/2013)
09/30/2013	638	RESPONSE (re 635 Emergency MOTION order to exclude the undisclosed applications on the HTC Thunderbolt) *(DEFENDANTS' OPPOSITION TO EMERGENCY MOTION REGARDING APPLICATION ON THE THUNDERBOLT PHONE [EXHIBIT 1628])* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: # 1 Declaration of Thomas T. Carmack, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D)(Carmack, Thomas) (Filed on 9/30/2013) (Entered: 09/30/2013)
09/30/2013	639	Transcript of Proceedings held on 9−23−13, before Judge Paul S. Grewal. Court Reporter/Transcriber Lee−Anne Shortridge, Telephone number 408−287−4580 email: lee−anne_shortridge@cand.uscourts.gov. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 12/30/2013. (Related documents(s) 583 , 580) (las,) (Filed on 9/30/2013) (Entered: 09/30/2013)
09/30/2013	640	Transcript of Proceedings held on 9−24−13, before Judge Paul S. Grewal. Court Reporter/Transcriber Lee−Anne Shortridge, Telephone number 408−287−4580 email: lee−anne_shortridge@cand.uscourts.gov. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 12/30/2013. (Related documents(s) 583 , 580) (las,) (Filed on 9/30/2013) (Entered: 09/30/2013)
09/30/2013	641	Transcript of Proceedings held on 9−24−13, before Judge Paul S. Grewal. Court Reporter/Transcriber Lee−Anne Shortridge, Telephone number 408−287−4580 email: lee−anne_shortridge@cand.uscourts.gov. Per General Order No. 59 and

		Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 12/30/2013. (Related documents(s) 583 , 580) (las,) (Filed on 9/30/2013) (Entered: 09/30/2013)
09/30/2013	642	Transcript of Proceedings held on 9−26−13, before Judge Paul S. Grewal. Court Reporter/Transcriber Lee−Anne Shortridge, Telephone number 408−287−4580 email: lee−anne_shortridge@cand.uscourts.gov. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 12/30/2013. (Related documents(s) 583 , 580) (las,) (Filed on 9/30/2013) (Entered: 09/30/2013)
09/30/2013	643	Transcript of Proceedings held on 9−27−13, before Judge Paul S. Grewal. Court Reporter/Transcriber Lee−Anne Shortridge, Telephone number 408−287−4580 email: lee−anne_shortridge@cand.uscourts.gov. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 12/30/2013. (Related documents(s) 583 , 580) (las,) (Filed on 9/30/2013) (Entered: 09/30/2013)
09/30/2013	645	**PROPOSED FINAL JURY INSTRUCTIONS. Signed by Judge Paul S. Grewal on September 30, 2013. (psglc2, COURT STAFF) (Filed on 9/30/2013) (Entered: 09/30/2013)**
09/30/2013	646	**FINAL JURY INSTRUCTIONS. Signed by Judge Paul S. Grewal on September 30, 2013. (psglc2, COURT STAFF) (Filed on 9/30/2013) (Entered: 09/30/2013)**
09/30/2013	652	Minute Entry: Jury Trial (Day 6) held on 9/30/2013 before Magistrate Judge Paul S Grewal (Court Reporter: Lee−Anne Shortridge.) (ofr, COURT STAFF) (Date Filed: 9/30/2013) (Entered: 10/02/2013)
10/01/2013	647	MOTION for Judgment as a Matter of Law filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 10/1/2013 12:30 PM in Courtroom 4, 5th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 10/1/2013. (Chen, Kyle) (Filed on 10/1/2013) (Entered: 10/01/2013)
10/01/2013	648	NOTICE of Appearance by Neil Nalin Desai (Desai, Neil) (Filed on 10/1/2013) (Entered: 10/01/2013)
10/01/2013	649	RESPONSE (re 647 MOTION for Judgment as a Matter of Law) *DEFENDANTS OPPOSITION TO HTCS MOTION FOR JUDGMENT AS A MATTER OF LAW OF NON−INFRINGEMENT [PER F.R.C.P. 50(A)]* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Tyan, Irvin) (Filed on 10/1/2013) (Entered: 10/01/2013)
10/01/2013	650	**FINAL VERDICT FORM. Signed by Judge Paul S. Grewal on October 1, 2013. (psglc2, COURT STAFF) (Filed on 10/1/2013) (Entered: 10/01/2013)**
10/01/2013	657	Minute Entry: Jury Trial (Day 7) held on 10/1/2013 before Magistrate Judge Paul S. Grewal (Court Reporter: Lee−Anne Shortridge.) (ofr, COURT STAFF) (Date Filed: 10/1/2013) (Entered: 10/04/2013)
10/02/2013	651	**ORDER DENYING 647 MOTION FOR JUDGMENT AS A MATTER OF LAW entered by Magistrate Judge Paul Singh Grewal. (This is a text−only entry generated by the court. There is no document associated with this entry.) (Entered: 10/02/2013)**

10/02/2013	658	Minute Entry: Jury Trial (Day 8) held on 10/2/2013 before Magistrate Judge Paul S. Grewal (Court Reporter: Lee−Anne Shortridge.) (ofr, COURT STAFF) (Date Filed: 10/2/2013) (Entered: 10/04/2013)
10/03/2013	653	NOTICE of Appearance by Jason Chia−Sun Fan (Fan, Jason) (Filed on 10/3/2013) (Entered: 10/03/2013)
10/03/2013	654	JURY VERDICT. (ofr, COURT STAFF) (Filed on 10/3/2013) (Entered: 10/03/2013)
10/03/2013	655	**JUDGMENT. (ofr, COURT STAFF) (Filed on 10/3/2013) (Entered: 10/03/2013)**
10/03/2013	656	Jury Notes. (ofr, COURT STAFF) (Filed on 10/3/2013) (Entered: 10/03/2013)
10/03/2013	659	Minute Entry: Jury Trial completed on 10/3/2013 before Magistrate Judge Paul S. Grewal (Court Reporter: Lee−Anne Shortridge.) (ofr, COURT STAFF) (Date Filed: 10/3/2013) (Entered: 10/04/2013)
10/07/2013	660	NOTICE of Intent to Request Redaction of Transcript by Kyle Dakai Chen (Chen, Kyle) (Filed on 10/7/2013) (Entered: 10/07/2013)
10/07/2013	661	STIPULATION WITH PROPOSED ORDER *REGARDING TRIAL EXHIBITS* filed by Alliacense Limited, HTC America, Inc., HTC Corporation, Patriot Scientific Corporation, Technology Properties Limited. (Chen, Kyle) (Filed on 10/7/2013) (Entered: 10/07/2013)
10/08/2013	662	**STIPULATION AND ORDER REGARDING TRIAL EXHIBITS by Judge Paul S. Grewal, granting 661 . (ofr, COURT STAFF) (Filed on 10/8/2013) (Entered: 10/08/2013)**
10/08/2013		Remark: Plaintiffs Exhibits Retrieved. (ofr, COURT STAFF) (Filed on 10/8/2013) (Entered: 10/09/2013)
10/09/2013		Remark: Defendants Exhibits Retrieved. (ofr, COURT STAFF) (Filed on 10/9/2013) (Entered: 10/09/2013)
10/17/2013	663	*** POSTED IN ERROR *** please see amended 669 BILL OF COSTS by Patriot Scientific Corporation. (Hoge, Charles) (Filed on 10/17/2013) Modified on 11/1/2013 (cv, COURT STAFF). (Entered: 10/17/2013)
10/17/2013	664	*** POSTED IN ERROR *** please see amended 670 BILL OF COSTS *by TECHNOLOGY PROPERTIES LIMITED and ALLIACENSE LIMITED* by Alliacense Limited, Technology Properties Limited. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F)(Lansky, David) (Filed on 10/17/2013) Modified on 11/1/2013 (cv, COURT STAFF). (Entered: 10/17/2013)
10/18/2013	665	NOTICE by HTC America, Inc., HTC Corporation re 660 Notice of Intent to Request Redaction of Transcript − *HTC's NOTICE OF WITHDRAWAL OF THEIR NOTICE OF INTENT TO REQUEST REDACTION OF TRANSCRIPT (DKT. NO. 660)* (Chen, Kyle) (Filed on 10/18/2013) (Entered: 10/18/2013)
10/25/2013	666	Transcript of Proceedings held on 10−1−13, before Judge Paul S. Grewal. Court Reporter/Transcriber Lee−Anne Shortridge, Telephone number 408−287−4580 email: lee−anne_shortridge@cand.uscourts.gov. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 1/7/2014. (Related documents(s) 583 , 580) (las,) (Filed on 10/25/2013) (Entered: 10/25/2013)
10/25/2013	667	Transcript of Proceedings held on 10−2−13, before Judge Paul S. Grewal. Court Reporter/Transcriber Lee−Anne Shortridge, Telephone number 408−287−4580 email: lee−anne_shortridge@cand.uscourts.gov. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until

		the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 1/7/2014. (Related documents(s) 583 , 580) (las,) (Filed on 10/25/2013) (Entered: 10/25/2013)
10/25/2013	668	Transcript of Proceedings held on 10−3−313, before Judge Paul S. Grewal. Court Reporter/Transcriber Lee−Anne Shortridge, Telephone number 408−287−4580 email: lee−anne_shortridge@cand.uscourts.gov. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 1/7/2014. (Related documents(s) 583 , 580) (las,) (Filed on 10/25/2013) (Entered: 10/25/2013)
10/31/2013	669	BILL OF COSTS − *Amendment to* 663 Bill of Costs by Patriot Scientific Corporation. (Hoge, Charles) (Filed on 10/31/2013) Modified on 11/1/2013 (cv, COURT STAFF). (Entered: 10/31/2013)
10/31/2013	670	BILL OF COSTS *(AMENDMENT to 664* by Alliacense Limited, Technology Properties Limited. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D, # 5 Exhibit E, # 6 Exhibit F)(Lansky, David) (Filed on 10/31/2013) Modified on 11/1/2013 (cv, COURT STAFF). (Entered: 10/31/2013)
10/31/2013	671	MOTION for Judgment as a Matter of Law *RENEWED MOTION FOR ENTRY OF JUDGMENT AS A MATTER OF LAW OF NON−INFRINGEMENT [PER FED. R. CIV. P. 50(B)]* filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 12/10/2013 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 11/14/2013. Replies due by 11/21/2013. (Attachments: # 1 Declaration of Kyle D. Chen ISO Renewed Motion for Entry of JMOL of Non−Infringement, # 2 Exhibit 1, # 3 Exhibit 2, # 4 Exhibit 3, # 5 Exhibit 4, # 6 Exhibit 5, # 7 Exhibit 6, # 8 Exhibit 7, # 9 Exhibit 8, # 10 Exhibit 9, # 11 Exhibit 10, # 12 Exhibit 11, # 13 Exhibit 12, # 14 Exhibit 13, # 15 Exhibit 14, # 16 Exhibit 15, # 17 Proposed Order)(Chen, Kyle) (Filed on 10/31/2013) (Entered: 10/31/2013)
10/31/2013	672	Request for Judicial Notice *OF RESPONSE OF THE OFFICE OF UNFAIR IMPORT INVESTIGATIONS TO THE PRIVATE PARTIES' PETITIONS FOR REVIEW* filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit A)(Chen, Kyle) (Filed on 10/31/2013) (Entered: 10/31/2013)
10/31/2013	673	Administrative Motion to File Under Seal *CONFIDENTIAL EXHIBITS ISO PLAINTIFFS' RENEWED MOTION FOR ENTRY OF JUDGMENT AS A MATTER OF LAW OF NON−INFRINGEMENT [DKT. 671]* filed by HTC America, Inc., HTC Corporation. (Attachments: # 1 Declaration of Kyle D. Chen ISO Administrative Motion to File Confidential Exhibits Under Seal, # 2 Proposed Order, # 3 Exhibit 4, # 4 Exhibit 5, # 5 Exhibit 6, # 6 Exhibit 7, # 7 Exhibit 8, # 8 Exhibit 11, # 9 Exhibit 13)(Chen, Kyle) (Filed on 10/31/2013) (Entered: 10/31/2013)
10/31/2013	674	MOTION TO CORRECT THE 10/3/2013 654 JUDGMENT PURSUANT TO RULE 60(A) OR IN THE ALTERNATIVE TO AMEND THE JUDGMENT PURSUANT TO RULE 59(E) filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 12/10/2013 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 11/14/2013. Replies due by 11/21/2013. (Attachments: # 1 Proposed Order)(Chen, Kyle) (Filed on 10/31/2013) Modified on 11/12/2013 (cv, COURT STAFF). (Entered: 10/31/2013)
11/01/2013	675	CERTIFICATE OF SERVICE by HTC America, Inc., HTC Corporation re 673 Administrative Motion to File Under Seal *CONFIDENTIAL EXHIBITS ISO PLAINTIFFS' RENEWED MOTION FOR ENTRY OF JUDGMENT AS A MATTER OF LAW OF NON−INFRINGEMENT [DKT. 671]*, 671 Proof of Service re Sealed Exhibits 4−8, 11 and 13 (Chen, Kyle) (Filed on 11/1/2013) Modified on 11/4/2013 (cv, COURT STAFF). (Entered: 11/01/2013)

11/04/2013	676	NOTICE OF APPEAL to the Federal Circuit by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. Filing fee $ 455, receipt number 0971−8134216. Appeal Record due by 12/4/2013. (Otteson, James) (Filed on 11/4/2013) (Entered: 11/04/2013)
11/04/2013	677	Declaration of Benjamin Damstedt in Support of 673 Administrative Motion to File Under Seal *CONFIDENTIAL EXHIBITS ISO PLAINTIFFS' RENEWED MOTION FOR ENTRY OF JUDGMENT AS A MATTER OF LAW OF NON−INFRINGEMENT [DKT. 671]* filed byQualcomm Inc.. (Related document(s) 673) (Damstedt, Benjamin) (Filed on 11/4/2013) (Entered: 11/04/2013)
11/04/2013	678	OBJECTIONS to re 669 Bill of Costs − *HTC's Objections to Patriot's Amended Bill of Costs* by HTC America, Inc., HTC Corporation. (Attachments: # 1 Declaration Kyle D. Chen, # 2 Exhibit A, # 3 Exhibit B)(Chen, Kyle) (Filed on 11/4/2013) (Entered: 11/04/2013)
11/04/2013	679	OBJECTIONS to re 670 Amended Bill of Costs by HTC America, Inc., HTC Corporation. (Attachments: # 1 Declaration Kyle D. Chen, # 2 Exhibit A, # 3 Exhibit B1, # 4 Exhibit B2, # 5 Exhibit B3, # 6 Exhibit C, # 7 Exhibit D1, # 8 Exhibit D2, # 9 Exhibit D3, # 10 Exhibit D4, # 11 Exhibit E, # 12 Exhibit F, # 13 Exhibit G1, # 14 Exhibit G2, # 15 Exhibit H)(Chen, Kyle) (Filed on 11/4/2013) Modified on 11/5/2013 (cv, COURT STAFF). (Entered: 11/04/2013)
11/05/2013	680	***TRANSCRIPT ORDER REQUEST CANCELLED 11/5/13***TRANSCRIPT ORDER by Alliacense Limited, Technology Properties Limited for Court Reporter FTR − San Jose. (Carmack, Thomas) (Filed on 11/5/2013) Modified on 11/5/2013 (sp, COURT STAFF). (Entered: 11/05/2013)
11/05/2013	681	CORRECTED OBJECTIONS to re 669 Amended Bill of Costs, 678 Objection, COSTS by HTC America, Inc., HTC Corporation. (Attachments: # 1 Declaration Kyle D. Chen, # 2 Exhibit A, # 3 Exhibit B)(Chen, Kyle) (Filed on 11/5/2013) Modified on 11/5/2013 (cv, COURT STAFF). (Entered: 11/05/2013)
11/05/2013	682	TRANSCRIPT ORDER by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited for Court Reporter Lee−Anne Shortridge. (Carmack, Thomas) (Filed on 11/5/2013) (Entered: 11/05/2013)
11/07/2013	683	Transmission of Docket Sheet to the Federal Circuit Court of Appeals as to 676 Notice of Appeal to the Federal Circuit. (cv, COURT STAFF) (Filed on 11/7/2013) (Additional attachment(s) added on 11/7/2013: # 1 Supplement Cover Sheet) (cv, COURT STAFF). Modified on 11/7/2013 (cv, COURT STAFF). (Entered: 11/07/2013)
11/08/2013	684	Transcript of Proceedings held on 9−30−13, before Judge Paul S. Grewal. Court Reporter/Transcriber Lee−Anne Shortridge, Telephone number 408−287−4580 email: lee−anne_shortridge@cand.uscourts.gov. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 1/7/2014. (las,) (Filed on 11/8/2013) (Entered: 11/08/2013)
11/08/2013	685	Transcript of Proceedings held on 9−22−2013, before Judge Paul S. Grewal. Court Reporter/Transcriber Lee−Anne Shortridge, Telephone number 408−287−4580 email: lee−anne_shortridge@cand.uscourts.gov. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 2/6/2014. (Related documents(s) 682) (las,) (Filed on 11/8/2013) Modified on 11/21/2013 (sp, COURT STAFF). (Entered: 11/08/2013)
11/08/2013	686	NOTICE of Change In Counsel by Kyle Dakai Chen − *NOTICE OF WITHDRAWAL OF CERTAIN COUNSEL FOR PLAINTIFFS* (Chen, Kyle) (Filed on 11/8/2013) (Entered: 11/08/2013)

11/11/2013	687	MOTION to continue 674 MOTION previously set for 12/10/13, but needs to be continued due to a trial scheduling conflict involving lead attorneys for HTC. (Chen, Kyle) (Filed on 11/11/2013) Modified on 11/12/2013, (counsel selected incorrect event.) (cv, COURT STAFF). Modified on 11/12/2013 (cv, COURT STAFF). (Entered: 11/11/2013)
11/11/2013	688	MOTION to continue the 671 MOTION to January 7, 2014 at 10:00 a.m. The hearing was previously noticed for December 10, 2013, but needs to be continued due to a trial scheduling conflict involving lead attorneys for HTC. (Chen, Kyle) (Filed on 11/11/2013) Modified on 11/12/2013 (cv, COURT STAFF). (Entered: 11/11/2013)
11/11/2013	689	JOINT ADMINISTRATIVE MOTION FOR LEAVE TO FILE ADDITIONAL BRIEFING RE: DEFENDANTS AMENDED BILLS OF COSTS by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Attachments: #1 Proposed Order GRANTING JOINT ADMINISTRATIVE MOTION FOR LEAVE TO FILE ADDITIONAL BRIEFING(Lansky, David) (Filed on 11/11/2013) Modified on 11/12/2013 (cv, COURT STAFF). (Entered: 11/11/2013)
11/13/2013	692	ORDER of USCA for the Federal Circuit − The appeal is,DEACTIVATED. The appeal will be reactivated upon entry of the orderdisposing of the last such outstanding motion.as to 676 Notice of Appeal to the Federal Circuit, filed by Technology Properties Limited, Alliacense Limited, Patriot Scientific Corporation (cv, COURT STAFF) (Filed on 11/13/2013) (Entered: 11/14/2013)
11/14/2013	690	RESPONSE (re 674 MOTION TO CORRECT THE 654 JUDGMENT PURSUANT TO RULE 60(A) OR IN THE ALTERNATIVE TO AMEND THE JUDGMENT PURSUANT TO RULE 59(E)) *OPPOSITION TO PLAINTIFFS MOTION TO CORRECT THE JUDGMENT PURSUANT TO RULE 60(a) OR, IN THE ALTERNATIVE, TO AMEND THE JUDGMENT PURSUANT TO RULE 59(e) (Dkt. No. 674)* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Lansky, David) (Filed on 11/14/2013) (Entered: 11/14/2013)
11/14/2013	691	RESPONSE (re 671 MOTION for Judgment as a Matter of Law *RENEWED MOTION FOR ENTRY OF JUDGMENT AS A MATTER OF LAW OF NON−INFRINGEMENT [PER FED. R. CIV. P. 50(B)]*) *DEFENDANTS OPPOSITION TO HTCS RENEWED MOTION FOR JUDGMENT AS A MATTER OF LAW OF NON−INFRINGEMENT [PER F.R.C.P. 50(b)]* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Otteson, James) (Filed on 11/14/2013) (Entered: 11/14/2013)
11/20/2013	693	TRANSCRIPT ORDER by HTC America, Inc., HTC Corporation for Court Reporter Lee−Anne Shortridge. (Chen, Kyle) (Filed on 11/20/2013) (Entered: 11/20/2013)
11/21/2013	694	REPLY (re 674 MOTION TO CORRECT THE 654 JUDGMENT PURSUANT TO RULE 60(A) OR IN THE ALTERNATIVE TO AMEND THE JUDGMENT PURSUANT TO RULE 59(E)) filed byHTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 11/21/2013) (Entered: 11/21/2013)
11/21/2013	695	REPLY (re 671 MOTION for Judgment as a Matter of Law *RENEWED MOTION FOR ENTRY OF JUDGMENT AS A MATTER OF LAW OF NON−INFRINGEMENT [PER FED. R. CIV. P. 50(B)]*) filed byHTC America, Inc., HTC Corporation. (Attachments: #1 Declaration Supplemental Declaration of Kyle D Chen ISO Renewed Motion for Entry of Judgment etc., #2 Exhibit 16, #3 Exhibit 17, #4 Exhibit 18, #5 Exhibit 19)(Chen, Kyle) (Filed on 11/21/2013) (Entered: 11/21/2013)
12/13/2013	696	**ORDER GRANTING 689 MOTION FOR LEAVE TO FILE entered by Magistrate Judge Paul Singh Grewal. (This is a text−only entry generated by the court. There is no document associated with this entry.) (Entered: 12/13/2013)**
12/13/2013	697	**ORDER GRANTING 673 ADMINISTRATIVE MOTION TO FILE UNDER SEAL entered by Magistrate Judge Paul Singh Grewal. (This is a text−only entry generated by the court. There is no document associated with this**

		entry.) (Entered: 12/13/2013)
12/16/2013	698	DOCUMENT E−FILED UNDER SEAL re 697 Order on Administrative Motion to File Under Seal − 673 *ADMINISTRATIVE MOTION TO FILE UNDER SEAL − CONFIDENTIAL EXHIBITS 4−8, 11 and 13 ISO PLAINTIFFS' RENEWED MOTION FOR ENTRY OF JUDGMENT AS A MATTER OF LAW OF NON−INFRINGEMENT [DKT. 671]* by HTC America, Inc., HTC Corporation. (Attachments: #1 Exhibit 4, #2 Exhibit 5, #3 Exhibit 6, #4 Exhibit 7, #5 Exhibit 8, #6 Exhibit 11, #7 Exhibit 13)(Chen, Kyle) (Filed on 12/16/2013) (Entered: 12/16/2013)
12/18/2013	699	RESPONSE to re 679 Objection, *(RESPONSE TO HTC'S OBJECTIONS TO TPL'S AMENDED BILL OF COSTS)* by Alliacense Limited, Technology Properties Limited. (Lansky, David) (Filed on 12/18/2013) (Entered: 12/18/2013)
12/18/2013	700	BILL OF COSTS *(SECOND AMENDED BILL OF COSTS)* by Alliacense Limited, Technology Properties Limited. (Attachments: #1 Exhibit A, #2 Exhibit B, #3 Exhibit C, #4 Exhibit D, #5 Exhibit E, #6 Exhibit F)(Lansky, David) (Filed on 12/18/2013) (Entered: 12/18/2013)
12/30/2013	701	CLERK'S NOTICE RESETTING TIME ON JANUARY 7, 2014 MOTIONS: Plaintiffs' 1/7/2014 10:00 AM Renewed Motion for Entry of Judgment as a Matter of Law (Dkt. No. 671) and Motion to Correct Judgment (Dkt. No. 674) are reset to 1:30 PM (SPECIAL SET) in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. *****This is a text only docket entry, there is no document associated with this notice.***** (ofr, COURT STAFF) (Filed on 12/30/2013) (Entered: 12/30/2013)
12/30/2013	702	OBJECTIONS to re 700 Bill of Costs, 699 Response (Non Motion) −*HTC'S REPLY IN SUPPORT OF ITS OBJECTIONS TO TPLS AMENDED BILL OF COSTS AND OBJECTIONS TO TPLS SECOND AMENDED BILL OF COSTS* by HTC America, Inc., HTC Corporation. (Attachments: #1 Declaration Kyle D. Chen, #2 Exhibit I, #3 Exhibit J1, #4 Exhibit J2, #5 Exhibit J3, #6 Exhibit K, #7 Exhibit L1, #8 Exhibit L2, #9 Exhibit L3, #10 Exhibit L4, #11 Exhibit M, #12 Exhibit N, #13 Exhibit O1, #14 Exhibit O2)(Chen, Kyle) (Filed on 12/30/2013) (Entered: 12/30/2013)
01/06/2014		Set/Reset Transcript Deadlines re 643 Transcript,,. Release of Transcript Restriction set for 12/30/2013. (cv, COURT STAFF) (Filed on 1/6/2014) (Entered: 01/06/2014)
01/07/2014	703	Minute Entry: Motion Hearing held on 1/7/2014 before Magistrate Judge Paul S. Grewal re 671 RENEWED MOTION for Entry of Judgment as a Matter of Law of Non− Infringement and 674 MOTION to Correct the Judgment or in the Alternative to Amend the Judgment: The court takes matters under submission; written order to be issued. Parties to discuss possible referral to a Magistrate Judge for settlement. (Court Reporter FTR: (1:34 to 2:07) (ofr, COURT STAFF) (Date Filed: 1/7/2014) (Entered: 01/08/2014)
01/13/2014	704	Costs Taxed in amount of $ 113255.63 against HTC Corporation and HTC America Inc regarding Second Amended Bill of Costs (700). (srm, COURT STAFF) (Filed on 1/13/2014) (Entered: 01/13/2014)
01/13/2014	705	Costs Taxed in amount of $ 59,483.12 against HTC Corporation and HTC America Inc. regarding Amended Bill of Costs (669). (srm, COURT STAFF) (Filed on 1/13/2014) (Entered: 01/13/2014)
01/21/2014	706	MOTION Review of Clerk's Taxation of Costs re 704 Costs Taxed filed by Alliacense Limited, Technology Properties Limited. Motion Hearing set for 3/18/2014 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 2/4/2014. Replies due by 2/11/2014. (Attachments: #1 Proposed Order)(Lansky, David) (Filed on 1/21/2014) (Entered: 01/21/2014)
01/21/2014	707	**ORDER DENYING PLAINTIFFS' RENEWED MOTION FOR ENTRY OF JUDGMENT AS A MATTER OF LAW by Judge Paul S. Grewal denying 671 (psglc2, COURT STAFF) (Filed on 1/21/2014) (Entered: 01/21/2014)**

01/21/2014	708	**ORDER GRANTING−IN−PART HTC'S MOTION TO CORRECT THE JUDGMENT by Judge Paul S. Grewal granting−in−part 674 (psglc2, COURT STAFF) (Filed on 1/21/2014) (Entered: 01/21/2014)**
01/21/2014	709	**ORDER MODIFYING JUDGMENT. Signed by Judge Paul S. Grewal on January 21, 2014. (psglc2, COURT STAFF) (Filed on 1/21/2014) (Entered: 01/21/2014)**
01/21/2014	710	MOTION for Bill of Costs *for Court's Review of Taxed Costs Pursuant to Fed. R. Civ. P. 54(d)(1)* filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 2/25/2014 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 2/4/2014. Replies due by 2/11/2014. (Attachments: #1 Proposed Order Proposed Order)(Chen, Kyle) (Filed on 1/21/2014) (Entered: 01/21/2014)
01/24/2014	711	TRANSCRIPT ORDER by HTC America, Inc., HTC Corporation for Court Reporter FTR − San Jose. (Chen, Kyle) (Filed on 1/24/2014) (Entered: 01/24/2014)
02/04/2014	712	RESPONSE (re 710 MOTION for Bill of Costs *for Court's Review of Taxed Costs Pursuant to Fed. R. Civ. P. 54(d)(1)*) *(DEFENDANTS' OPPOSITION TO HTC'S MOTION FOR COURT'S REVIEW OF TAXED COSTS PURSUANT TO FED. R. CIV.P.54(d)(1))* filed byAlliacense Limited, Technology Properties Limited. (Lansky, David) (Filed on 2/4/2014) (Entered: 02/04/2014)
02/04/2014	713	BILL OF COSTS by HTC America, Inc., HTC Corporation. (Attachments: #1 Exhibit A, #2 Exhibit B, #3 Exhibit C, #4 Exhibit D, #5 Exhibit E, #6 Exhibit F)(Chen, Kyle) (Filed on 2/4/2014) (Entered: 02/04/2014)
02/04/2014	714	MOTION to Find Plaintiffs as Prevailing Parties and to Tax Costs against Defendants re 713 Bill of Costs filed by HTC America, Inc., HTC Corporation. Motion Hearing set for 3/18/2014 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 2/18/2014. Replies due by 2/25/2014. (Attachments: #1 Proposed Order)(Chen, Kyle) (Filed on 2/4/2014) (Entered: 02/04/2014)
02/04/2014	715	RESPONSE (re 706 MOTION Review of Clerk's Taxation of Costs re 704 Costs Taxed) − *HTCs Opposition to TPLs Motion Seeking Review of Clerks Taxation of Costs* filed byHTC America, Inc., HTC Corporation. (Attachments: #1 Declaration Kyle D. Chen, #2 Exhibit 1)(Chen, Kyle) (Filed on 2/4/2014) (Entered: 02/04/2014)
02/11/2014	716	REPLY (re 706 MOTION Review of Clerk's Taxation of Costs re 704 Costs Taxed) *IN SUPPORT OF MOTION SEEKING REVIEW OF CLERK'S TAXATION OF COSTS* filed byAlliacense Limited, Technology Properties Limited. (Lansky, David) (Filed on 2/11/2014) (Entered: 02/11/2014)
02/11/2014	717	STIPULATION WITH PROPOSED ORDER re 710 MOTION for Bill of Costs *for Court's Review of Taxed Costs Pursuant to Fed. R. Civ. P. 54(d)(1) − STIPULATION AND [PROPOSED] ORDER REGARDING THE HEARING DATE OF HTCS MOTION FOR COURTS REVIEW OF TAXED COSTS PURSUANT TO FED. R. CIV. P. 54(d)(1)* filed by HTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 2/11/2014) (Entered: 02/11/2014)
02/11/2014	718	REPLY (re 710 MOTION for Bill of Costs *for Court's Review of Taxed Costs Pursuant to Fed. R. Civ. P. 54(d)(1)*) − *HTC'S REPLY BRIEF IN SUPPORT OF MOTION FOR COURT'S REVIEW OF TAXED COSTS PURSUANT TO FED. R. CIV. P. 54(d)(1)* filed byHTC America, Inc., HTC Corporation. (Attachments: #1 Declaration Kyle Chen)(Chen, Kyle) (Filed on 2/11/2014) (Entered: 02/11/2014)
02/13/2014	719	**ORDER SETTING HEARING by Judge Paul S. Grewal granting−in−part 717 (psglc2, COURT STAFF) (Filed on 2/13/2014) (Entered: 02/13/2014)**
02/13/2014	720	CLERK'S NOTICE RE TELEPHONIC APPEARANCE AT MARCH 6, 2014 MOTIONS HEARING: Parties requesting to appear telephonically are instructed to contact CourtCall at 866−582−6878 to arrange for telephonic appearance. *****This is a text only docket entry, there is no document associated with this notice.***** (ofr, COURT STAFF) (Filed on 2/13/2014) (Entered: 02/13/2014)

02/18/2014	721	RESPONSE (re 714 MOTION to Find Plaintiffs as Prevailing Parties and to Tax Costs against Defendants re 713 Bill of Costs) *(DEFENDANTS' OPPOSITION)* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Lansky, David) (Filed on 2/18/2014) (Entered: 02/18/2014)
02/18/2014	722	MOTION for Leave to File *SUR−REPLY IN SUPPORT OF OPPOSITION TO DEFS' MOTION SEEKING REVIEW OF CLERK'S TAXATION OF COSTS* filed by HTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit A, # 2 Declaration Declaration of Kyle D. Chen, # 3 Proposed Order)(Chen, Kyle) (Filed on 2/18/2014) (Entered: 02/18/2014)
02/19/2014	723	STIPULATION WITH PROPOSED ORDER *REGARDING PENDING MOTIONS ON COSTS AND REGARDING HTC'S BILL OF COSTS* filed by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Lansky, David) (Filed on 2/19/2014) (Entered: 02/19/2014)
02/19/2014	724	Request for Judicial Notice *of Notice of Commission Determination Finding No Violation of Section 337; Termination of Investigation* filed byHTC America, Inc., HTC Corporation. (Attachments: # 1 Exhibit A)(Chen, Kyle) (Filed on 2/19/2014) (Entered: 02/19/2014)
02/20/2014	725	NOTICE OF APPEAL to the Federal Circuit by HTC America, Inc., HTC Corporation. Filing fee $ 505, receipt number 0971−8390454. Appeal Record due by 3/24/2014. (Chen, Kyle) (Filed on 2/20/2014) (Entered: 02/20/2014)
02/20/2014	726	**ORDER GRANTING STIPULATION REGARDING PENDING MOTIONS ON COSTS AND HTC'S BILL OF COSTS by Judge Paul S. Grewal granting 723 (psglc2, COURT STAFF) (Filed on 2/20/2014) (Entered: 02/20/2014)**
02/20/2014	727	RESPONSE (re 722 MOTION for Leave to File *SUR−REPLY IN SUPPORT OF OPPOSITION TO DEFS' MOTION SEEKING REVIEW OF CLERK'S TAXATION OF COSTS*) *(DEFENDANTS' OPPOSITION)* filed byAlliacense Limited, Patriot Scientific Corporation, Technology Properties Limited. (Lansky, David) (Filed on 2/20/2014) (Entered: 02/20/2014)
02/25/2014	728	Transmission of Notice of Appeal and Docket Sheet to the Federal Circuit Court of Appeals as to 725 Notice of Appeal to the Federal Circuit. Filing fee $ 455. Appeal Record due by 3/27/2014. (cv, COURT STAFF) (Filed on 2/25/2014) (Entered: 02/25/2014)
02/25/2014		Appeal Remark − acknowledging receipt from the Federal Circuit re 725 . (cv, COURT STAFF) (Filed on 2/25/2014) (Entered: 02/25/2014)
02/25/2014	729	TRANSCRIPT ORDER by Technology Properties Limited for Court Reporter Summer Fisher. (Carmack, Thomas) (Filed on 2/25/2014) (Entered: 02/25/2014)
02/25/2014	730	CLERK'S NOTICE RE COURT REFERRAL TO CHIEF MAGISTRATE JUDGE ELIZABETH D. LAPORTE FOR SETTLEMENT: The court refers matter to Chief Magistrate Judge Elizabeth D. Laporte for Settlement. Counsel is instructed to contact Judge Laporte's Courtroom Deputy Kristen Melen at 415−522−3694 to coordinate dates for a Settlement Conference. *****This is a text only docket entry, there is no document associated with this notice.***** (ofr, COURT STAFF) (Filed on 2/25/2014) (Entered: 02/25/2014)
02/25/2014	731	REPLY (re 714 MOTION to Find Plaintiffs as Prevailing Parties and to Tax Costs against Defendants re 713 Bill of Costs) filed byHTC America, Inc., HTC Corporation. (Chen, Kyle) (Filed on 2/25/2014) (Entered: 02/25/2014)
02/26/2014	732	Transcript of Proceedings held on 1−27−2012, before Judge James Ware. Official Court Reporter Connie Kuhl, CSR, RPR, RMR, CRR, connie.kuhl.realtime@gmail.com, Telephone number 415−431−2020. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerk's Office public terminal or may be purchased through the Court Reporter until the deadline for the Release of Transcript Restriction. After that date, it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 5/7/2012. (ck, COURT STAFF) (Filed on 2/26/2014) (Entered: 02/26/2014)

02/27/2014	733	**ORDER GRANTING 722 MOTION FOR LEAVE TO FILE entered by Magistrate Judge Paul Singh Grewal. (This is a text−only entry generated by the court. There is no document associated with this entry.) (Entered: 02/27/2014)**
02/27/2014	734	*** POSTED IN ERROR *** please see amended 735 Supplemental Brief filed by HTC America, Inc., HTC Corporation. (Related document(s) 706 , 716) (Chen, Kyle) (Filed on 2/27/2014) Modified on 2/28/2014 (cv, COURT STAFF). (Entered: 02/27/2014)
02/28/2014	735	Supplemental Brief re 706 MOTION Review of Clerk's Taxation of Costs re 704 Costs Taxed , 716 Reply to Opposition/Response, − *HTC'S SUR−REPLY IN SUPPORT OF ITS OPPOSITION* amendment to 734 filed by HTC America, Inc., HTC Corporation. (Related document(s) 706 , 716) (Chen, Kyle) (Filed on 2/28/2014) Modified on 2/28/2014 (cv, COURT STAFF). (Entered: 02/28/2014)
02/28/2014	736	Transcript of Proceedings held on 04/22/11, before Judge Jeremy Fogel. Court Reporter/Transcriber Summer Fisher, Telephone number 408−288−6150 summer_fisher@cand.uscourts.gov. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 5/29/2014. (Related documents(s) 729) (Fisher, Summer) (Filed on 2/28/2014) (Entered: 02/28/2014)
02/28/2014	737	Transcript of Proceedings held on November 30, 2012, before Judge Paul S. Grewal. Court Reporter/Transcriber Georgina Galvan Colin, Telephone number (408) 888−6697. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Release of Transcript Restriction set for 5/29/2014. (mz, COURT STAFF) (Filed on 2/28/2014) (Entered: 02/28/2014)
03/03/2014	738	Transcript of Proceedings held on 1/7/2014, before Judge Paul S. Grewal. Court Reporter/Transcriber Joan Columbini, Telephone number 415 255−6842. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. Redaction Request due 3/27/2014. Redacted Transcript Deadline set for 4/7/2014. Release of Transcript Restriction set for 6/4/2014. (Related documents(s) 711) (Columbini, Joan) (Filed on 3/3/2014) Modified on 3/6/2014 (sp, COURT STAFF). (Entered: 03/03/2014)
03/05/2014	739	TRANSCRIPT ORDER by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited for Court Reporter Summer Clanton. (Carmack, Thomas) (Filed on 3/5/2014) (Entered: 03/05/2014)
03/06/2014	740	Minute Entry: Motion Hearing held on 3/6/2014 before Magistrate Judge Paul S. Grewal re 706 MOTION for Review of Clerk's Taxation of Costs, 710 MOTION for Court's Review of Taxed Costs Pursuant to Fed. R. Civ. P. 54(d)(1) and 714 MOTION to Find Plaintiffs as Prevailing Parties and to Tax Costs against Defendants. The court takes matters under submission; written order to be issued. (Court Reporter: Summer Fisher) (ofr, COURT STAFF) (Date Filed: 3/6/2014) (Entered: 03/06/2014)
03/06/2014	741	NOTICE by HTC America, Inc., HTC Corporation re 725 Notice of Appeal to the Federal Circuit − *SERVICE OF TRANSCRIPT PURCHASE ORDER FORM* (Keefe, Heidi) (Filed on 3/6/2014) (Entered: 03/06/2014)
03/07/2014	742	CLERKS NOTICE SCHEDULING A TELEPHONIC STATUS/SETTLEMENT CONFERNCE WITH JUDGE LAPORTE: Telephonic Conference set for

		3/10/2014 09:30 AM in Courtroom E, 15th Floor, San Francisco. *This is a text only docket entry, there is no document associated with this notice.* (knm, COURT STAFF) (Filed on 3/7/2014) (Entered: 03/07/2014)
03/10/2014	743	Appeal Remark − Notification that transcript has been completed. re 741 Transcript Purchase Oder 725 Notice of Appeal. *** copy mailed to the Federal Circuit *** (cv, COURT STAFF) (Filed on 3/10/2014) Modified on 3/10/2014 (cv, COURT STAFF). (Entered: 03/10/2014)
03/10/2014	744	TRANSCRIPT ORDER by HTC America, Inc., HTC Corporation for Court Reporter Summer Fisher. (Chen, Kyle) (Filed on 3/10/2014) (Entered: 03/10/2014)
03/11/2014	745	**Order Setting Settlement Conference on Costs before Magistrate Judge Laporte: Settlement Conference set for 4/8/2014 01:30 PM in Courtroom E, 15th Floor, San Francisco. Signed by Judge Elizabeth D Laporte on 3/11/2014. (knm, COURT STAFF) (Filed on 3/11/2014) (Entered: 03/11/2014)**
03/12/2014	746	TRANSCRIPT ORDER by Alliacense Limited, Patriot Scientific Corporation, Technology Properties Limited for Court Reporter Connie Kuhl. (Carmack, Thomas) (Filed on 3/12/2014) (Entered: 03/12/2014)
04/09/2014	747	Minute Entry: Settlement Conference− case did not settle (Date Filed: 4/9/2014). Telephonic Further Settlement Conference set for 5/7/2014 02:00 PM in Courtroom E, 15th Floor, San Francisco. (Court Reporter N/A.) (knm, COURT STAFF) (Date Filed: 4/9/2014) (Entered: 04/09/2014)

US005809336A

United States Patent [19]

Moore et al.

[11] **Patent Number: 5,809,336**

[45] **Date of Patent: Sep. 15, 1998**

[54] **HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK**

[75] Inventors: **Charles H. Moore**, Woodside; **Russell H. Fish, III**, Mt. View, both of Calif.

[73] Assignee: **Patriot Scientific Corporation**, San Diego, Calif.

[21] Appl. No.: **484,918**

[22] Filed: **Jun. 7, 1995**

Related U.S. Application Data

[62] Division of Ser. No. 389,334, Aug. 3, 1989, Pat. No. 5,440,749.

[51] **Int. Cl.**[6] **G06F 1/04**

[52] **U.S. Cl.** **395/845**

[58] **Field of Search** 395/500, 551, 395/555, 845

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,967,104	6/1976	Brantingham	364/709.09
3,980,993	9/1976	Bredart et al.	395/550
4,003,028	1/1977	Bennett et al.	395/742
4,042,972	8/1977	Gruner et al.	395/389
4,050,096	9/1977	Bennett	395/494
4,112,490	9/1978	Pohlman et al.	395/287
4,315,308	2/1982	Jackson	395/853
4,338,675	7/1982	Palmer	364/748
4,398,265	8/1983	Puhl et al.	395/882
4,453,229	6/1984	Schaire	395/250
4,503,500	3/1985	Magan	395/800
4,539,655	9/1985	Trussell et al.	395/280
4,553,201	11/1985	Pollack	395/183.22
4,627,082	12/1986	Pelgrom et al.	377/63
4,670,837	6/1987	Sheets	395/550
4,680,698	7/1987	Edwards et al.	395/800
4,761,763	8/1988	Hicks	395/286
5,414,862	5/1995	Suzuki et al.	395/750

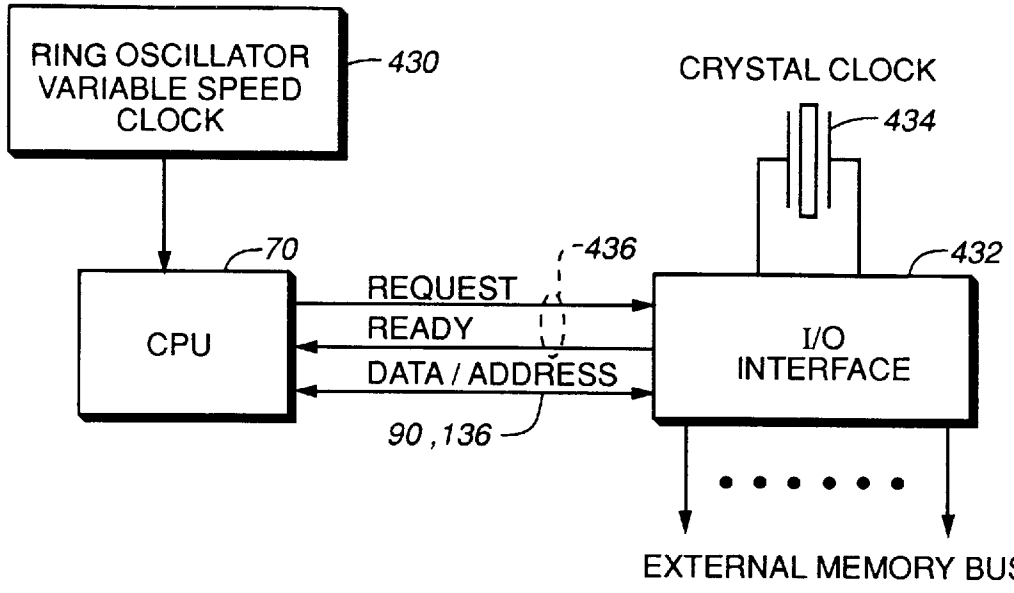
Primary Examiner—David Y. Eng

Attorney, Agent, or Firm—Cooley Godward LLP

[57] **ABSTRACT**

A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.

10 Claims, 19 Drawing Sheets



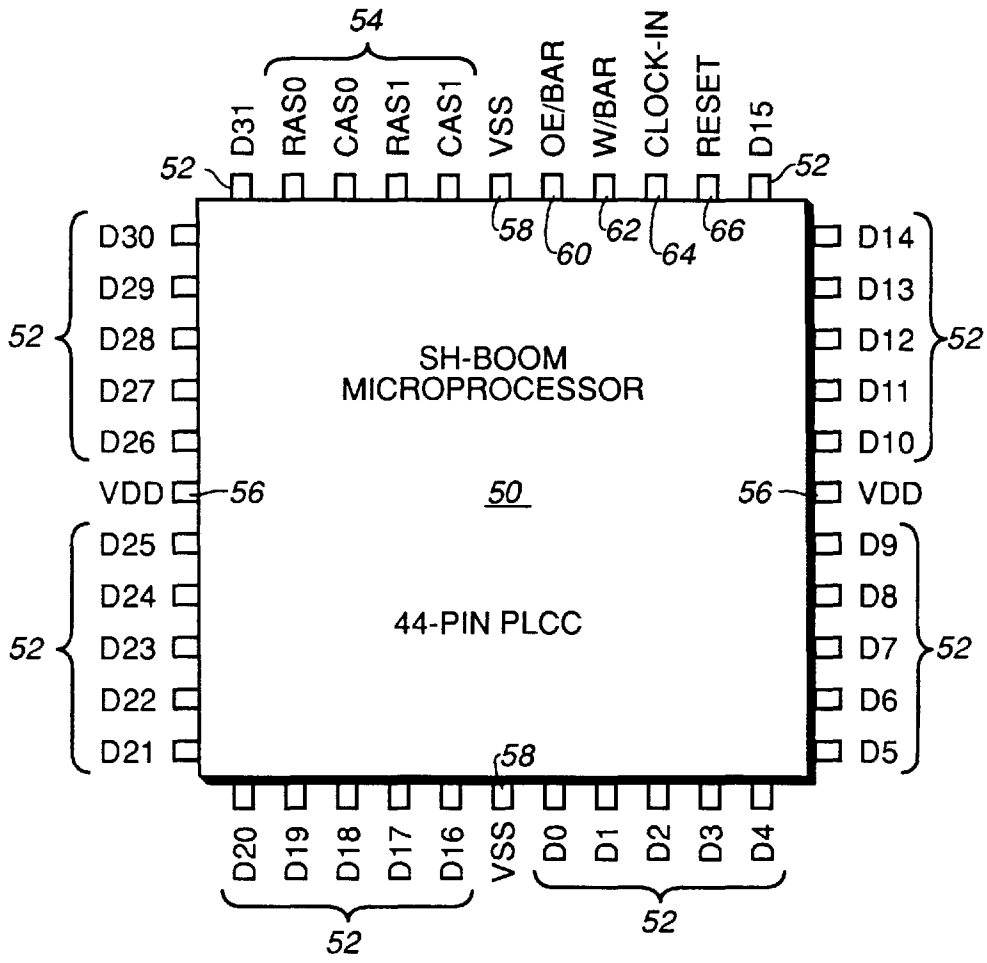

54
D31
RAS0
CAS0
RAS1
CAS1
VSS
OE/BAR
W/BAR
CLOCK-IN
RESET
D15
52
58
60
62
64
66
D30
D29
D28
D27
D26
VDD
56
SH-BOOM
MICROPROCESSOR
50
44-PIN PLCC
D14
D13
D12
D11
D10
D25
D24
D23
D22
D21
D9
D8
D7
D6
D5
D20
D19
D18
D17
D16
D0
D1
D2
D3
D4

FIG._1

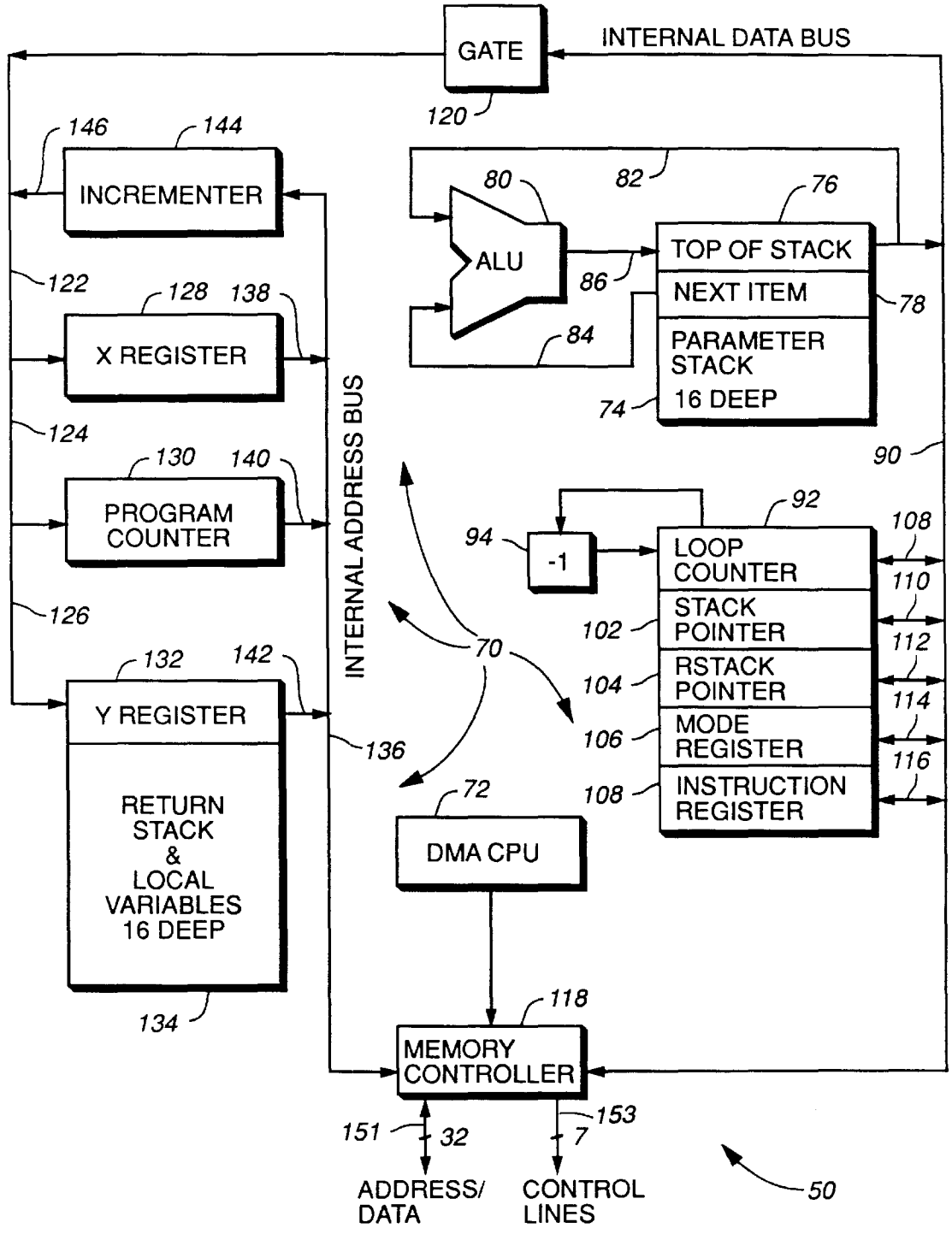

GATE
INTERNAL DATA BUS
120
146
144
INCREMENTER
80
82
76
ALU
TOP OF STACK
NEXT ITEM
PARAMETER STACK
16 DEEP
86
84
78
74
122
128
138
X REGISTER
124
130
140
PROGRAM COUNTER
126
INTERNAL ADDRESS BUS
90
92
94
-1
LOOP COUNTER
STACK POINTER
RSTACK POINTER
MODE REGISTER
INSTRUCTION REGISTER
108
110
112
114
116
102
104
106
108
70
132
142
Y REGISTER
136
RETURN STACK & LOCAL VARIABLES 16 DEEP
134
72
DMA CPU
118
MEMORY CONTROLLER
151
32
153
7
ADDRESS/ DATA
CONTROL LINES
50

FIG._2

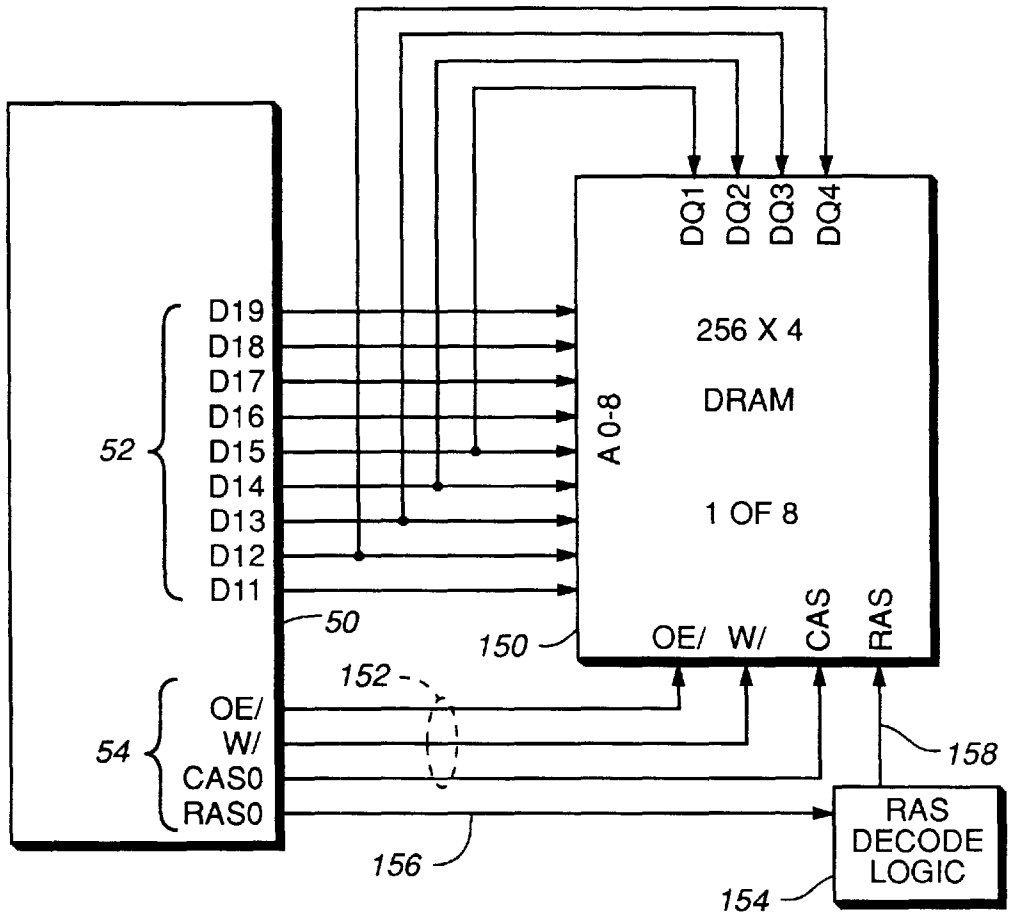

DQ1
DQ2
DQ3
DQ4
256 X 4
DRAM
1 OF 8
A 0-8
OE/
W/
CAS
RAS
D19
D18
D17
D16
D15
D14
D13
D12
D11
52
50
150
152
OE/
W/
CAS0
RAS0
54
156
158
RAS
DECODE
LOGIC
154

FIG._3

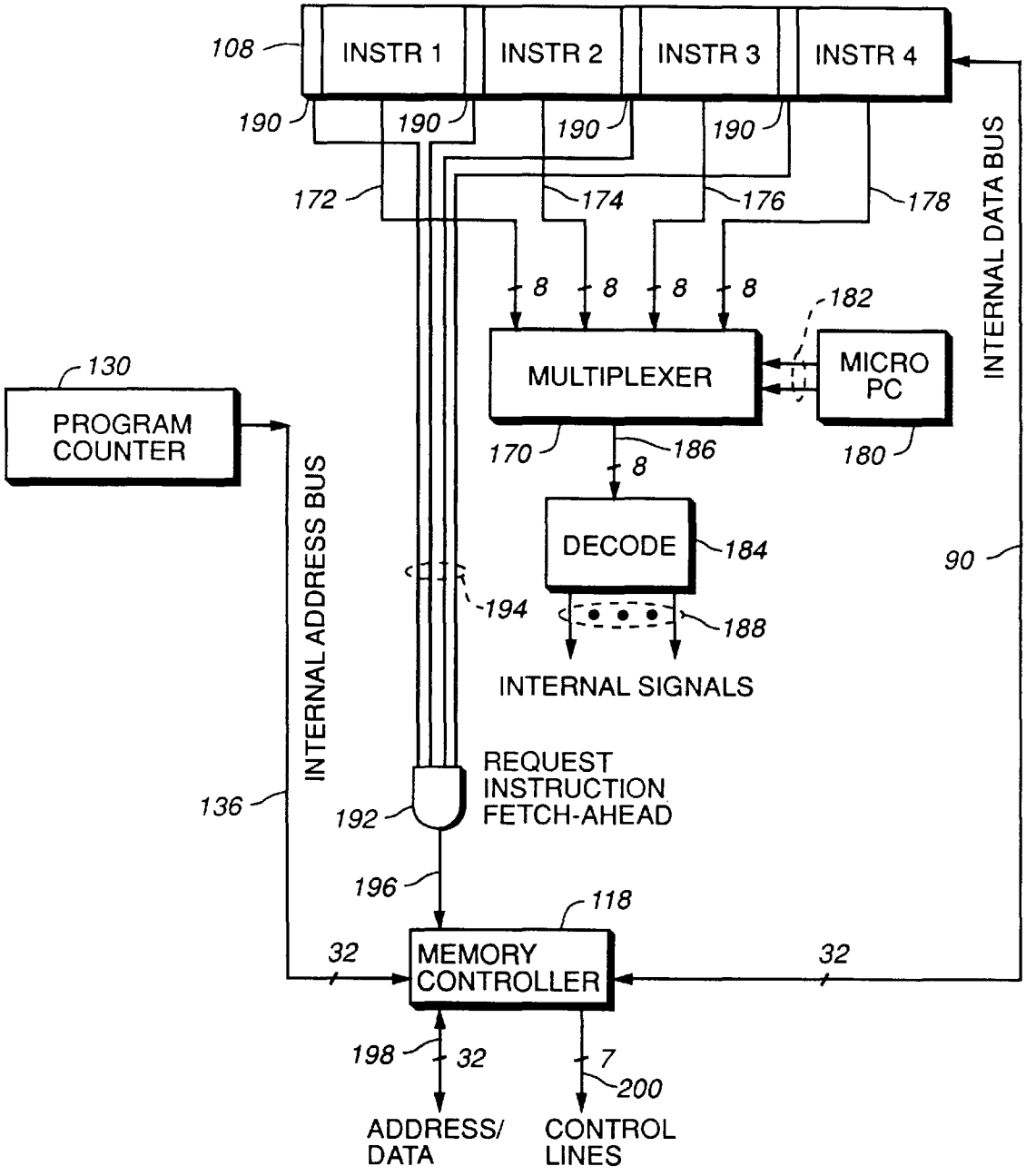

108
INSTR 1
INSTR 2
INSTR 3
INSTR 4
190
190
190
190
172
174
176
178
8
8
8
8
182
MULTIPLEXER
MICRO PC
130
PROGRAM COUNTER
170
186
180
8
DECODE
184
90
194
188
INTERNAL SIGNALS
INTERNAL ADDRESS BUS
INTERNAL DATA BUS
REQUEST INSTRUCTION FETCH-AHEAD
136
192
196
118
32
MEMORY CONTROLLER
32
198
32
7
200
ADDRESS/ DATA
CONTROL LINES

FIG._4

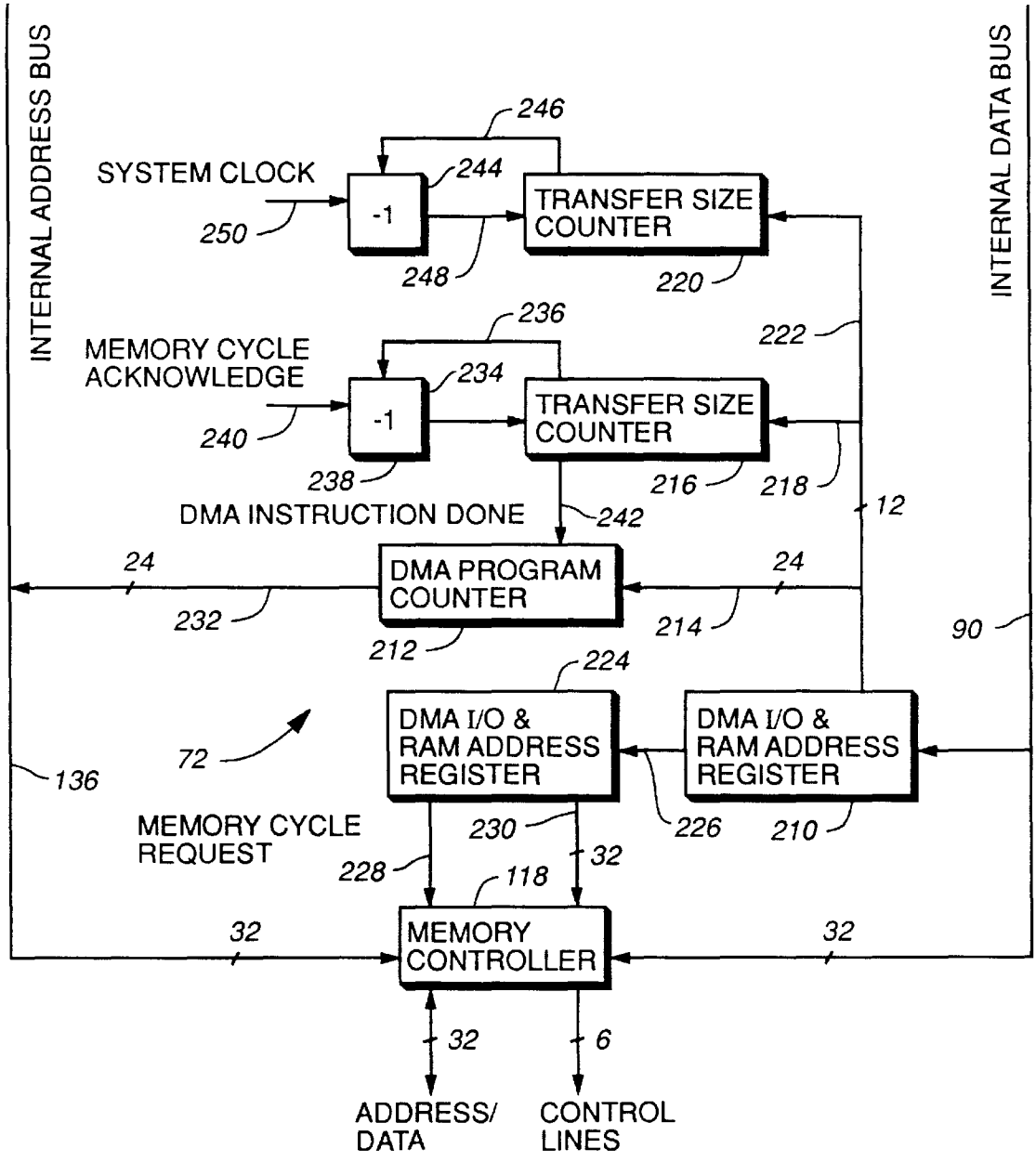

INTERNAL ADDRESS BUS
INTERNAL DATA BUS
SYSTEM CLOCK
250
-1
244
246
248
TRANSFER SIZE COUNTER
220
222
MEMORY CYCLE ACKNOWLEDGE
240
-1
234
236
238
TRANSFER SIZE COUNTER
216
218
12
DMA INSTRUCTION DONE
242
24
232
DMA PROGRAM COUNTER
212
24
214
90
224
72
136
DMA I/O & RAM ADDRESS REGISTER
DMA I/O & RAM ADDRESS REGISTER
MEMORY CYCLE REQUEST
230
226
210
228
32
118
32
MEMORY CONTROLLER
32
32
6
ADDRESS/ DATA
CONTROL LINES

FIG._5

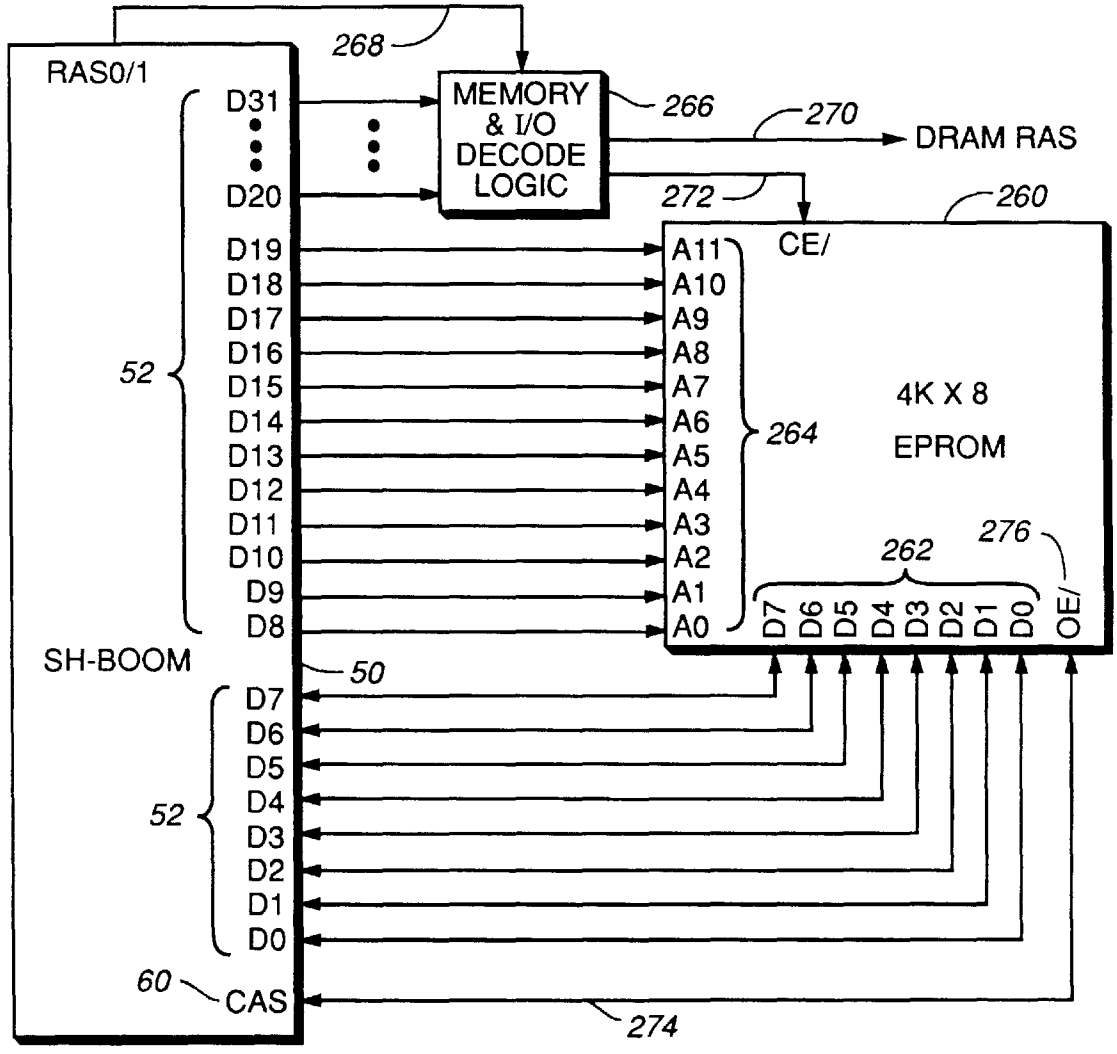

268
RAS0/1
D31
D20
MEMORY & I/O DECODE LOGIC
266
270
DRAM RAS
272
260
CE/
D19
D18
D17
D16
D15
D14
D13
D12
D11
D10
D9
D8
52
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
264
4K X 8
EPROM
262
276
D7
D6
D5
D4
D3
D2
D1
D0
OE/
SH-BOOM
50
52
60
CAS
274

FIG._6

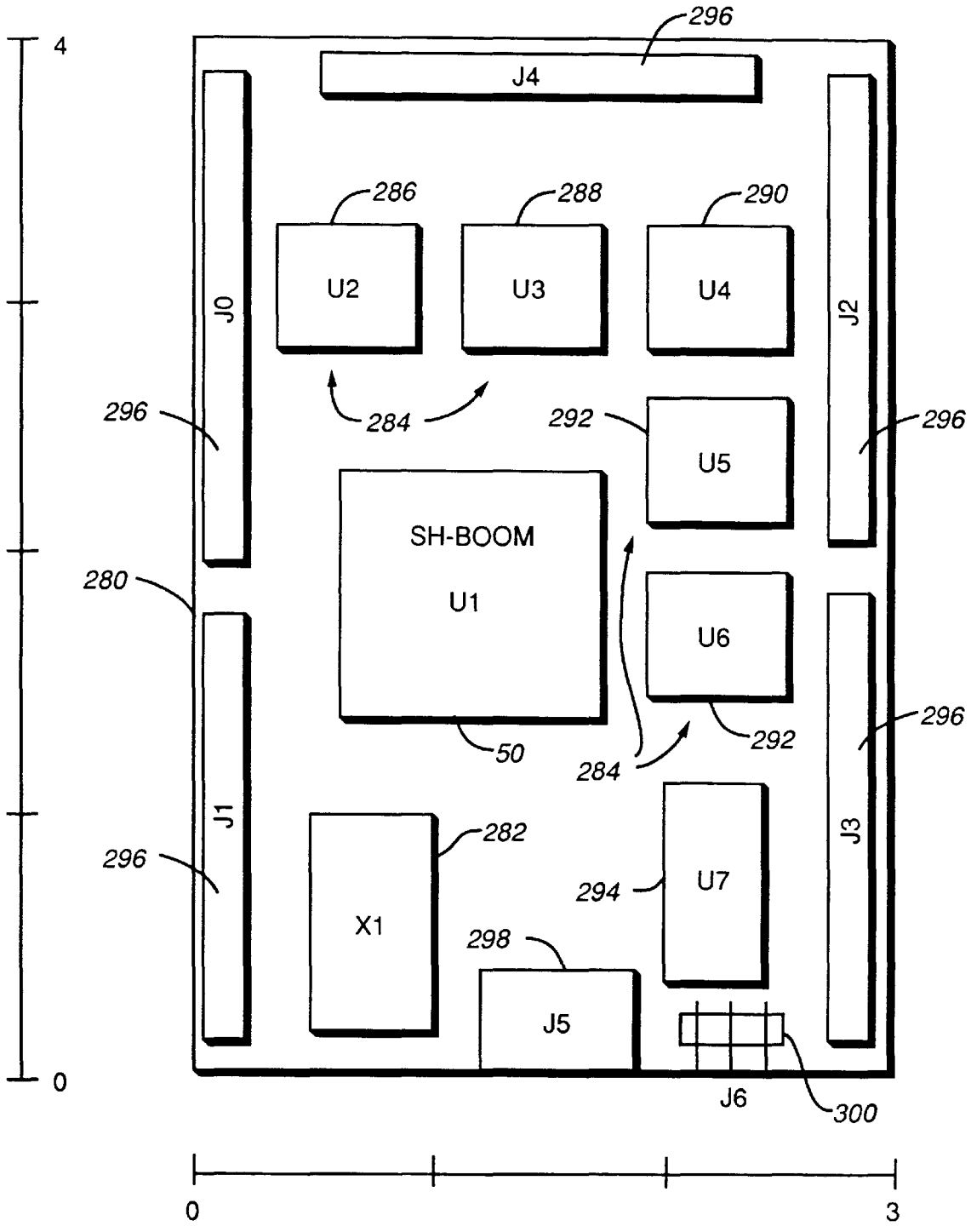

296
J4
286
288
290
U2
U3
U4
J0
J2
296
284
292
U5
296
SH-BOOM
U1
280
U6
296
50
292
284
J1
J3
296
282
294
U7
X1
298
J5
J6
300
4
0
0
3

FIG._7

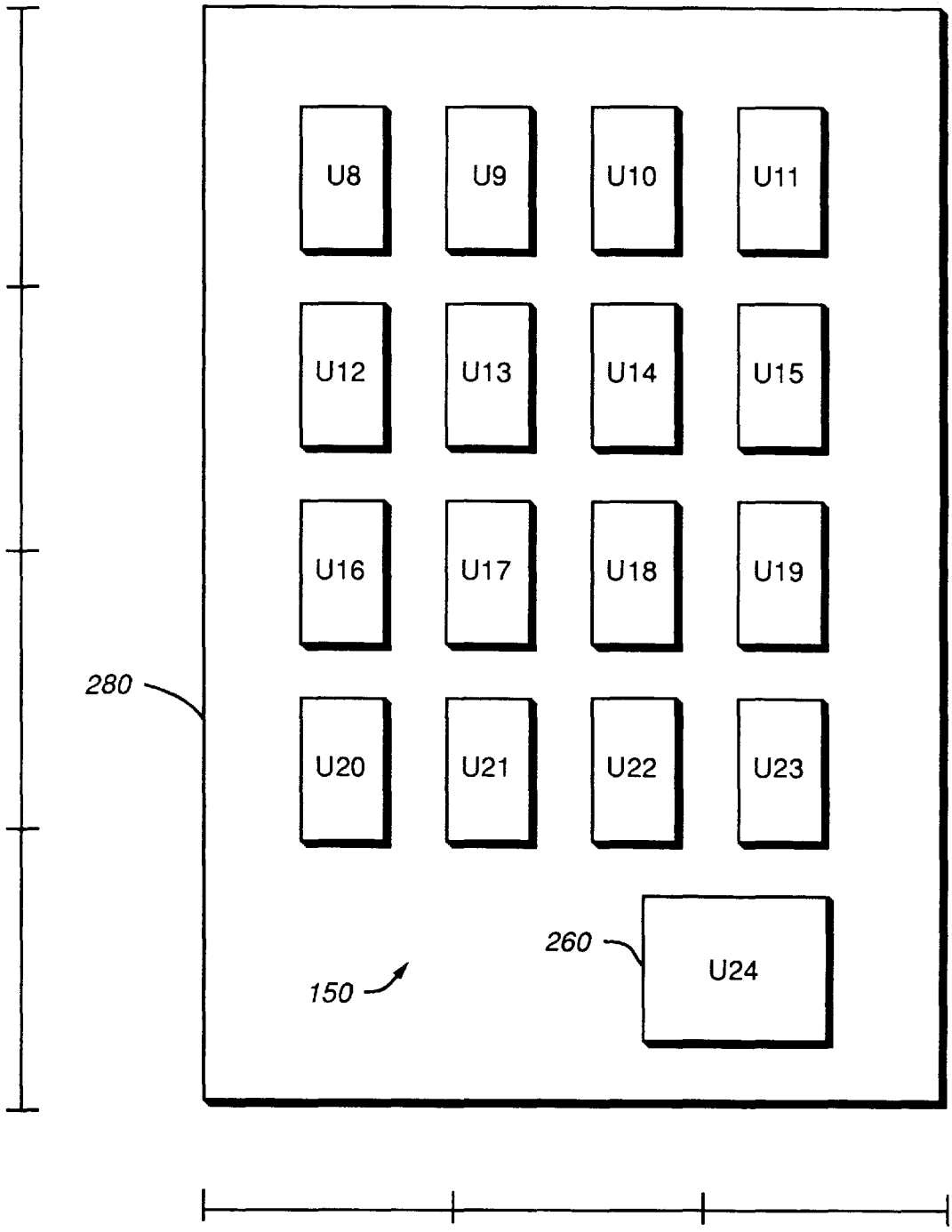

U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
280
260
150

FIG._8

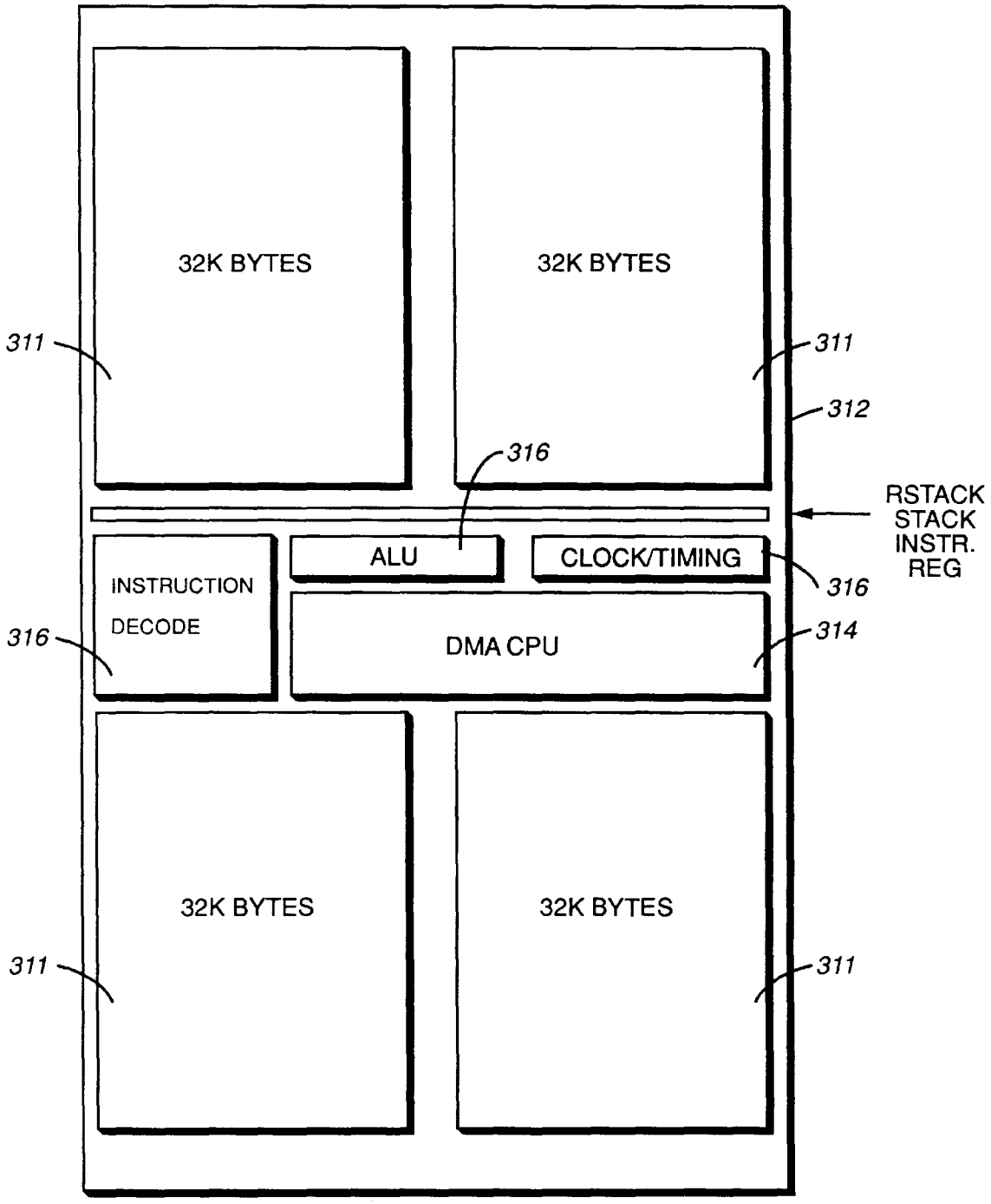

32K BYTES
32K BYTES
311
311
312
316
RSTACK
STACK
INSTR.
REG
ALU
CLOCK/TIMING
316
INSTRUCTION
DECODE
316
DMA CPU
314
32K BYTES
32K BYTES
311
311

FIG._9

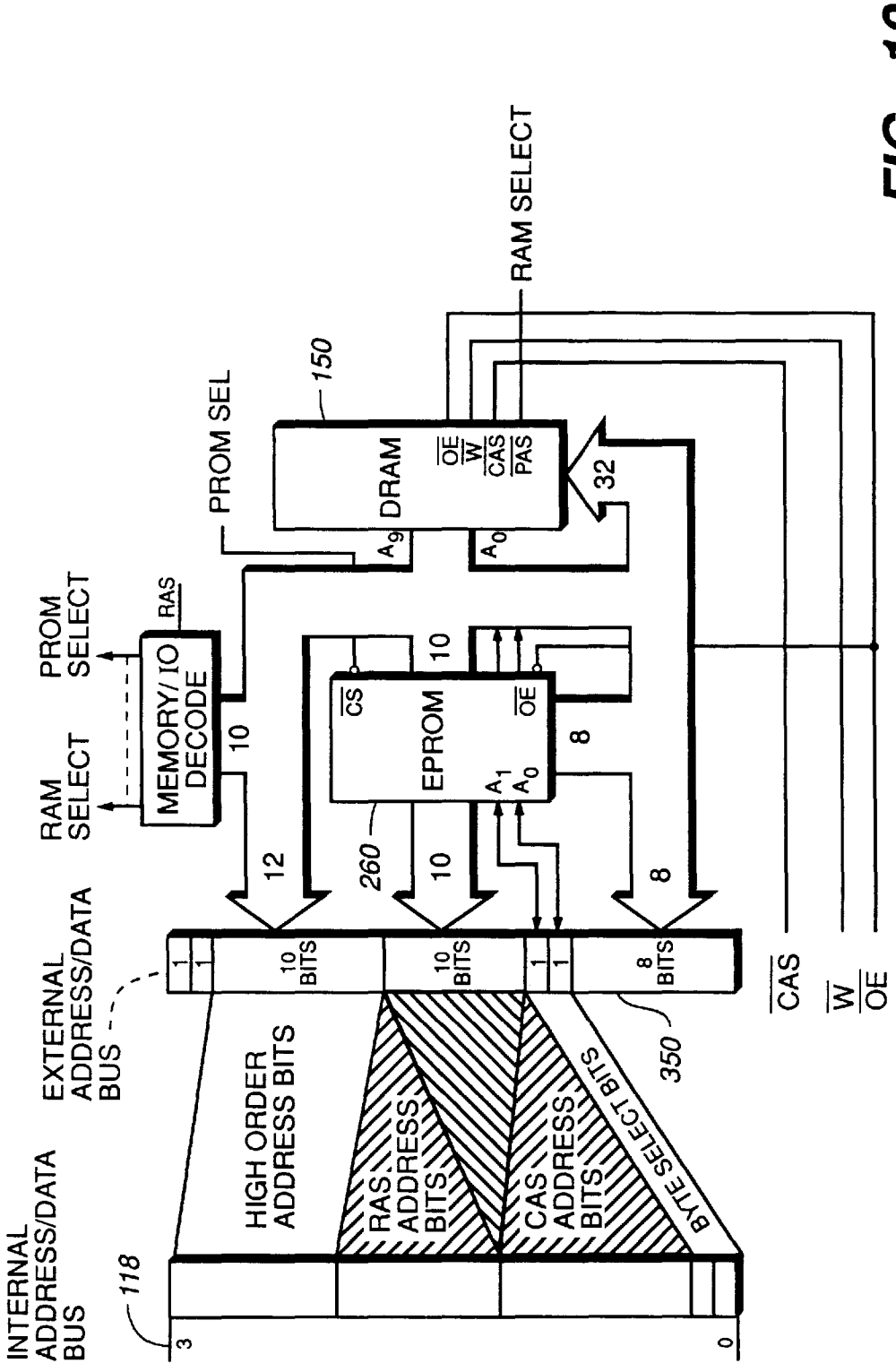
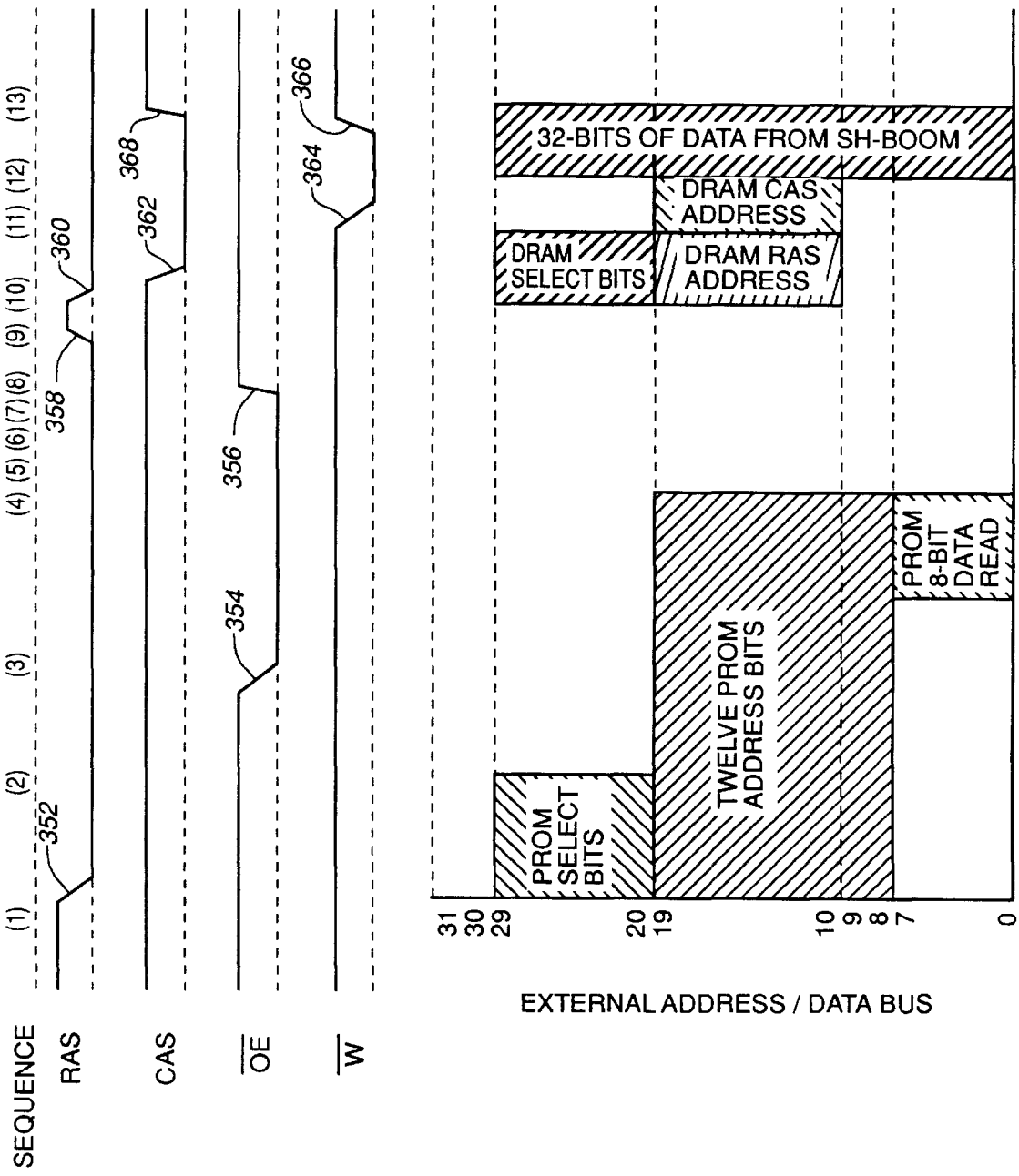

RAM SELECT
PROM SEL
150
DRAM
OE
W
CAS
PAS
32
A9
A0
PROM SELECT
RAS
MEMORY/IO DECODE
10
RAM SELECT
CS
EPROM
OE
A1
A0
10
8
12
260
10
8
EXTERNAL ADDRESS/DATA BUS
1
1
10 BITS
10 BITS
1
1
8 BITS
CAS
W
OE
350
HIGH ORDER ADDRESS BITS
RAS ADDRESS BITS
CAS ADDRESS BITS
BYTE SELECT BITS
INTERNAL ADDRESS/DATA BUS
118
3
0

FIG._10

FIG._11


SEQUENCE
RAS
CAS
OE
W
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(10)
(11)
(12)
(13)
352
354
356
358
360
362
364
366
368
32-BITS OF DATA FROM SH-BOOM
DRAM CAS ADDRESS
DRAM SELECT BITS
DRAM RAS ADDRESS
PROM SELECT BITS
TWELVE PROM ADDRESS BITS
PROM 8-BIT DATA READ
31
30
29
20
19
10
9
8
7
0
EXTERNAL ADDRESS / DATA BUS

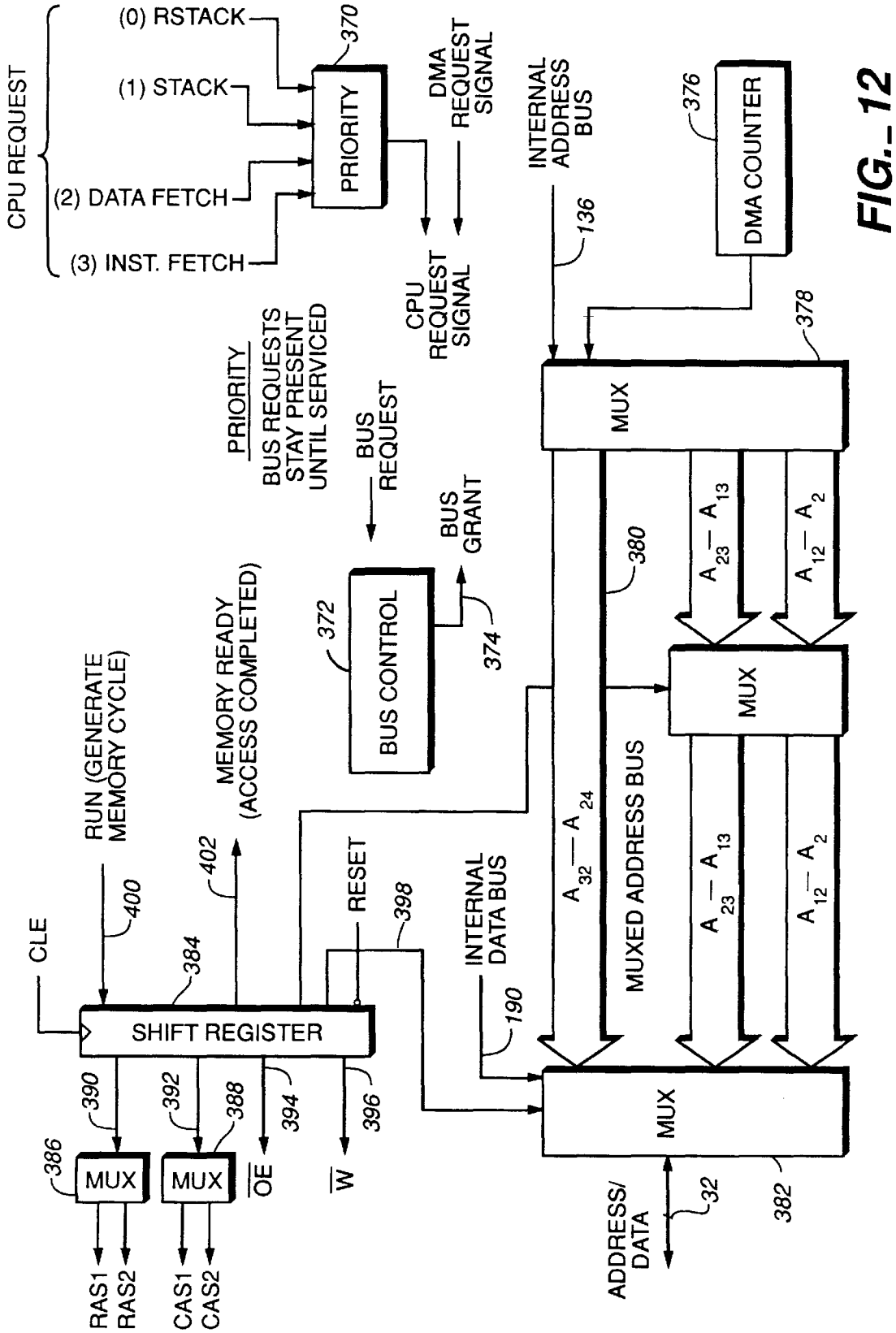

CPU REQUEST
(0) RSTACK
(1) STACK
(2) DATA FETCH
(3) INST. FETCH
370
PRIORITY
DMA REQUEST SIGNAL
CPU REQUEST SIGNAL
INTERNAL ADDRESS BUS
136
376
DMA COUNTER
378
MUX
PRIORITY
BUS REQUESTS STAY PRESENT UNTIL SERVICED
BUS REQUEST
BUS GRANT
372
BUS CONTROL
374
380
A23 — A13
A12 — A2
MUX
MEMORY READY (ACCESS COMPLETED)
RUN (GENERATE MEMORY CYCLE)
402
400
RESET
398
INTERNAL DATA BUS
A32 — A24
MUXED ADDRESS BUS
CLE
384
SHIFT REGISTER
190
390
392
388
394
396
386
MUX
MUX
OE
W
MUX
ADDRESS/ DATA
32
382
RAS1
RAS2
CAS1
CAS2

FIG._12

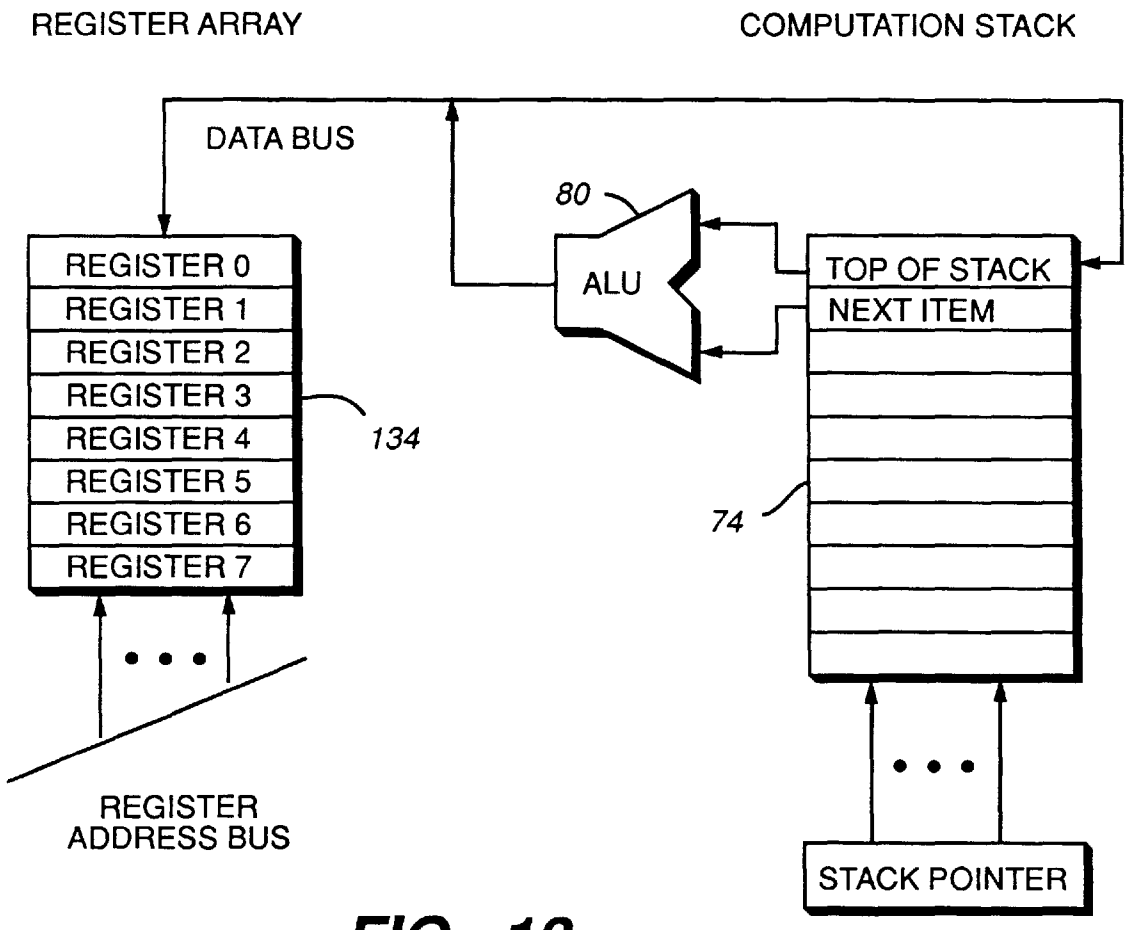

REGISTER ARRAY
COMPUTATION STACK
DATA BUS
80
ALU
REGISTER 0
REGISTER 1
REGISTER 2
REGISTER 3
REGISTER 4
REGISTER 5
REGISTER 6
REGISTER 7
134
TOP OF STACK
NEXT ITEM
74
REGISTER
ADDRESS BUS
STACK POINTER

FIG._13

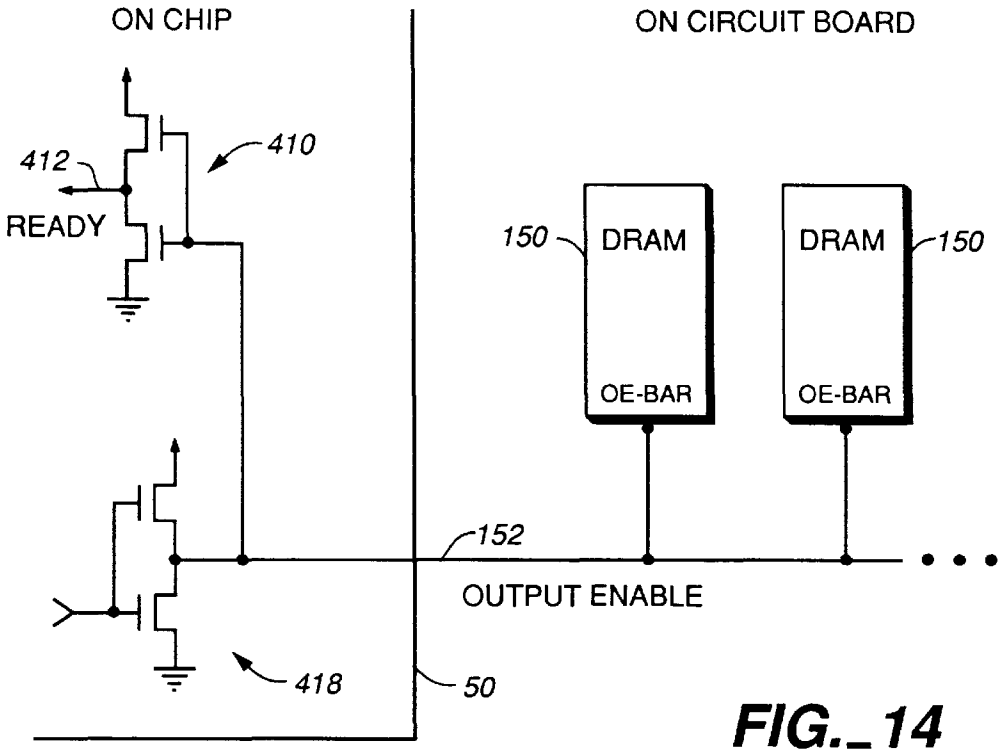

ON CHIP
ON CIRCUIT BOARD
412
410
READY
150
DRAM
OE-BAR
DRAM
150
OE-BAR
152
OUTPUT ENABLE
418
50

FIG._14

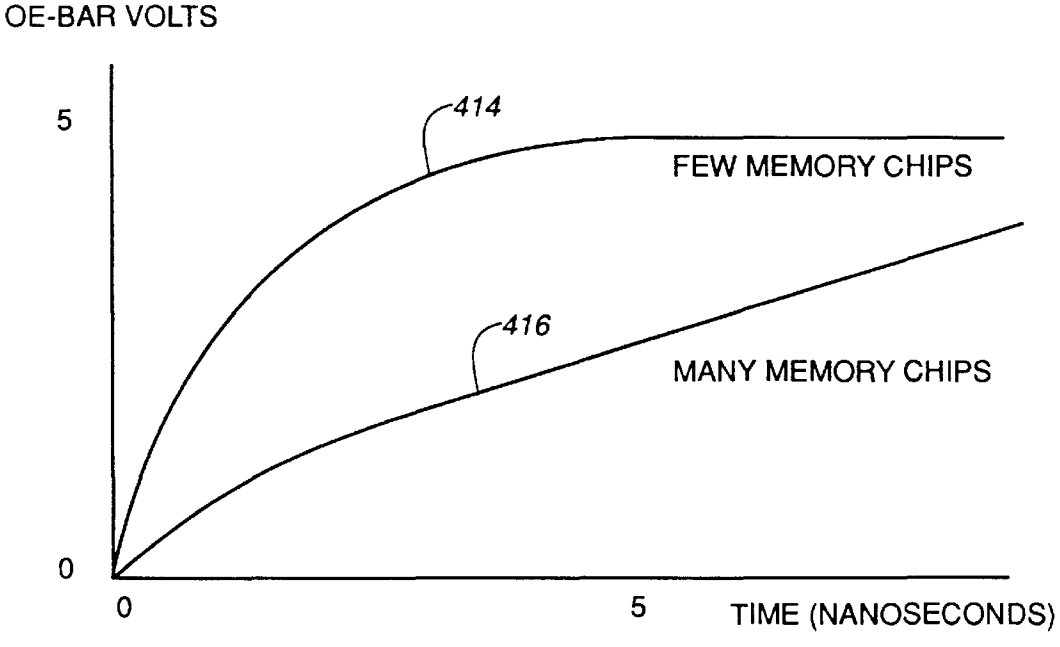

OE-BAR VOLTS
5
414
FEW MEMORY CHIPS
416
MANY MEMORY CHIPS
0
0
5
TIME (NANOSECONDS)

FIG._15

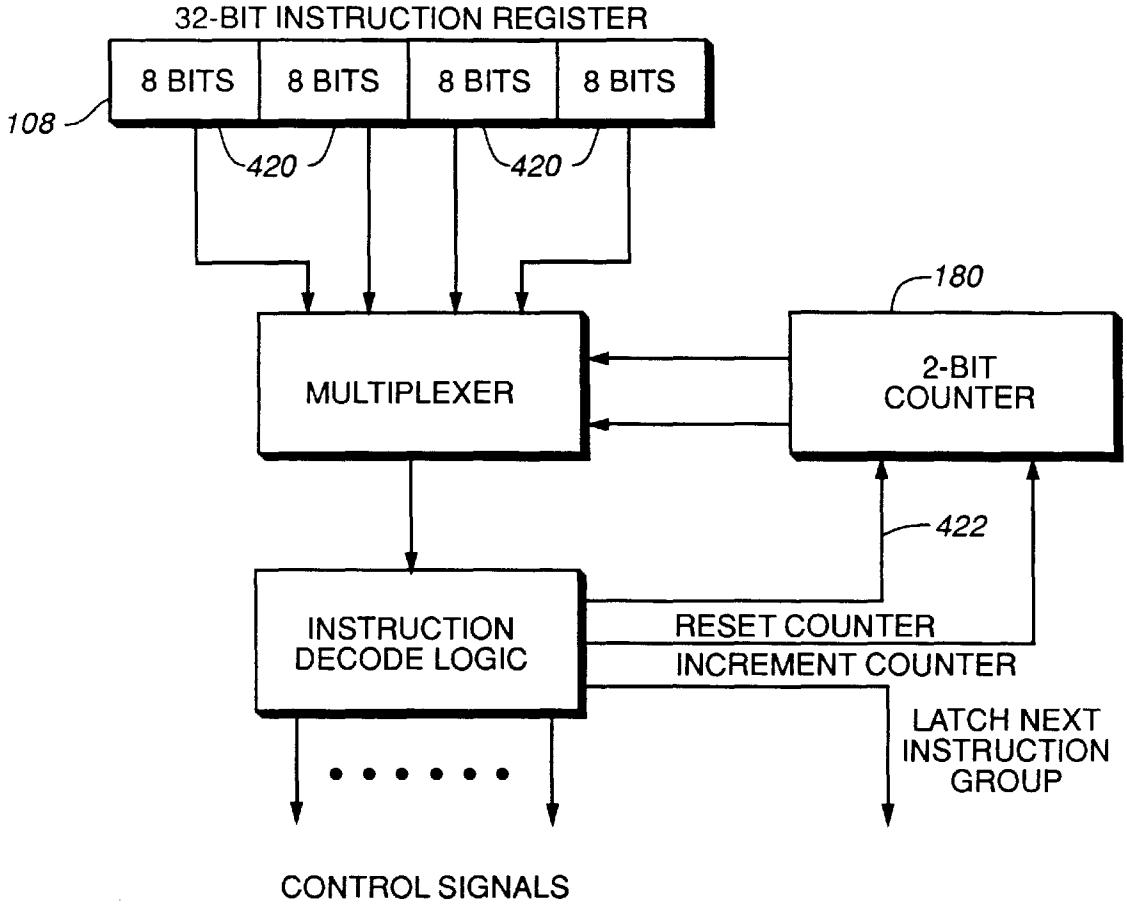

32-BIT INSTRUCTION REGISTER
8 BITS
8 BITS
8 BITS
8 BITS
108
420
420
180
MULTIPLEXER
2-BIT COUNTER
422
INSTRUCTION DECODE LOGIC
RESET COUNTER
INCREMENT COUNTER
LATCH NEXT INSTRUCTION GROUP
CONTROL SIGNALS

FIG._16

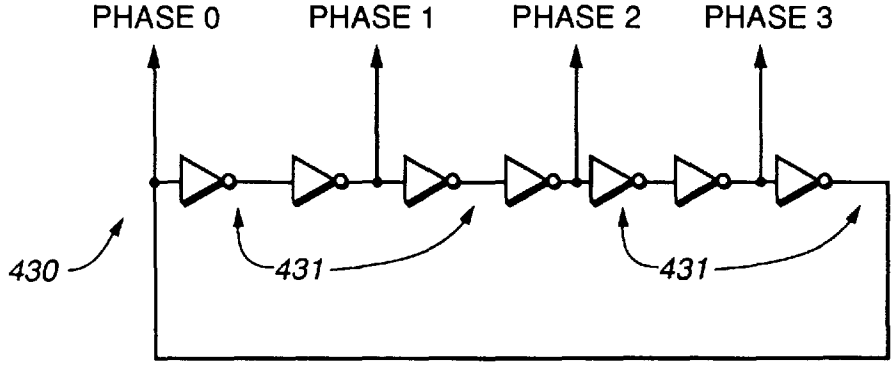

PHASE 0
PHASE 1
PHASE 2
PHASE 3
430
431
431

FIG._18

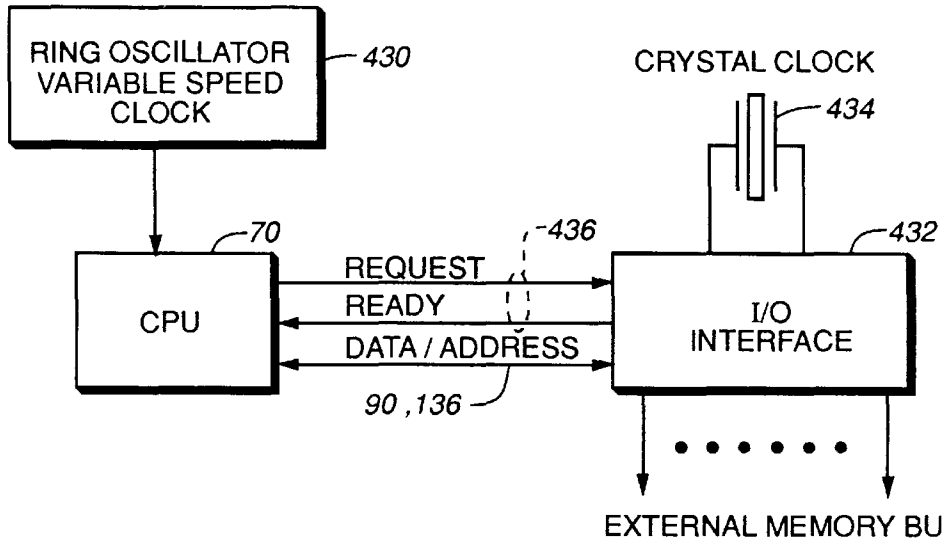

RING OSCILLATOR
VARIABLE SPEED
CLOCK
430
CRYSTAL CLOCK
434
70
436
432
CPU
REQUEST
READY
DATA / ADDRESS
I/O
INTERFACE
90 ,136
EXTERNAL MEMORY BUS

FIG._17

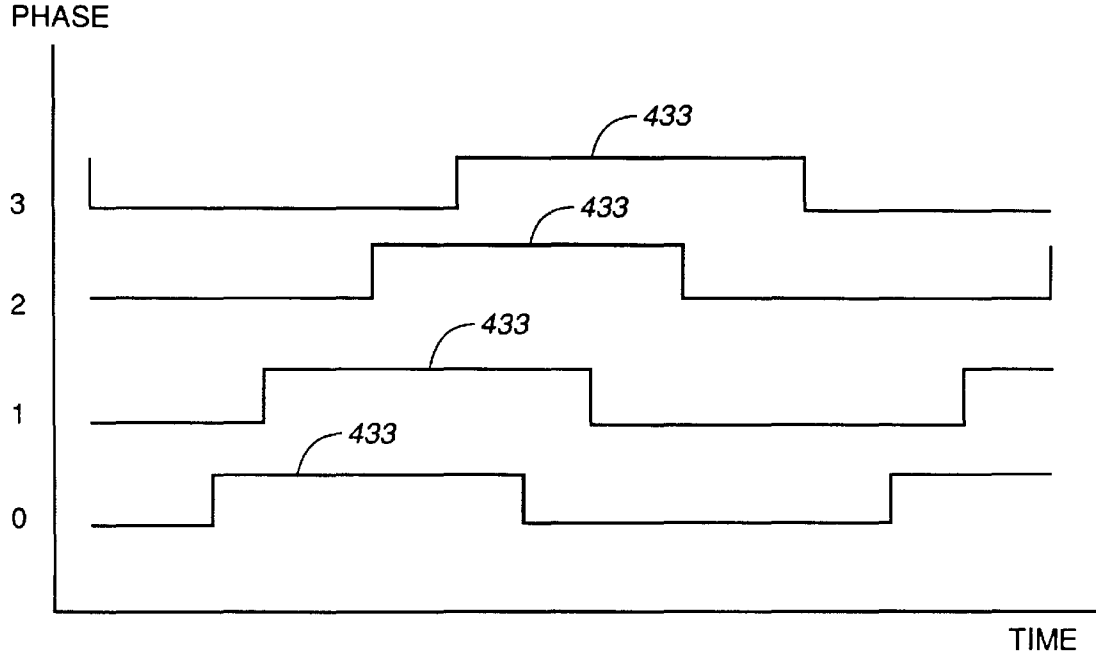

PHASE
433
433
433
433
3
2
1
0
TIME

FIG._19

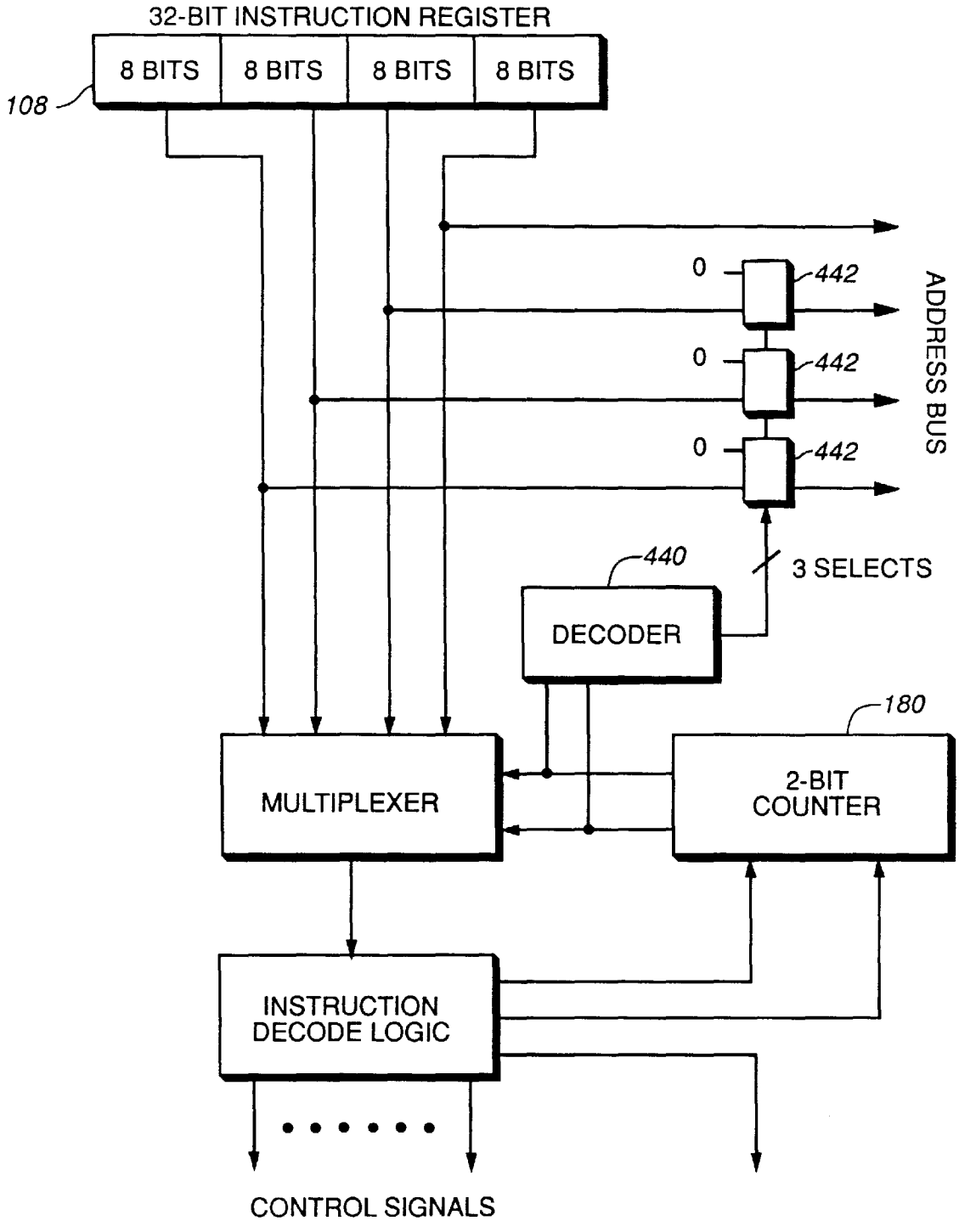

32-BIT INSTRUCTION REGISTER
8 BITS
8 BITS
8 BITS
8 BITS
108
0
442
0
442
0
442
ADDRESS BUS
440
3 SELECTS
DECODER
180
MULTIPLEXER
2-BIT COUNTER
INSTRUCTION DECODE LOGIC
CONTROL SIGNALS

FIG._20

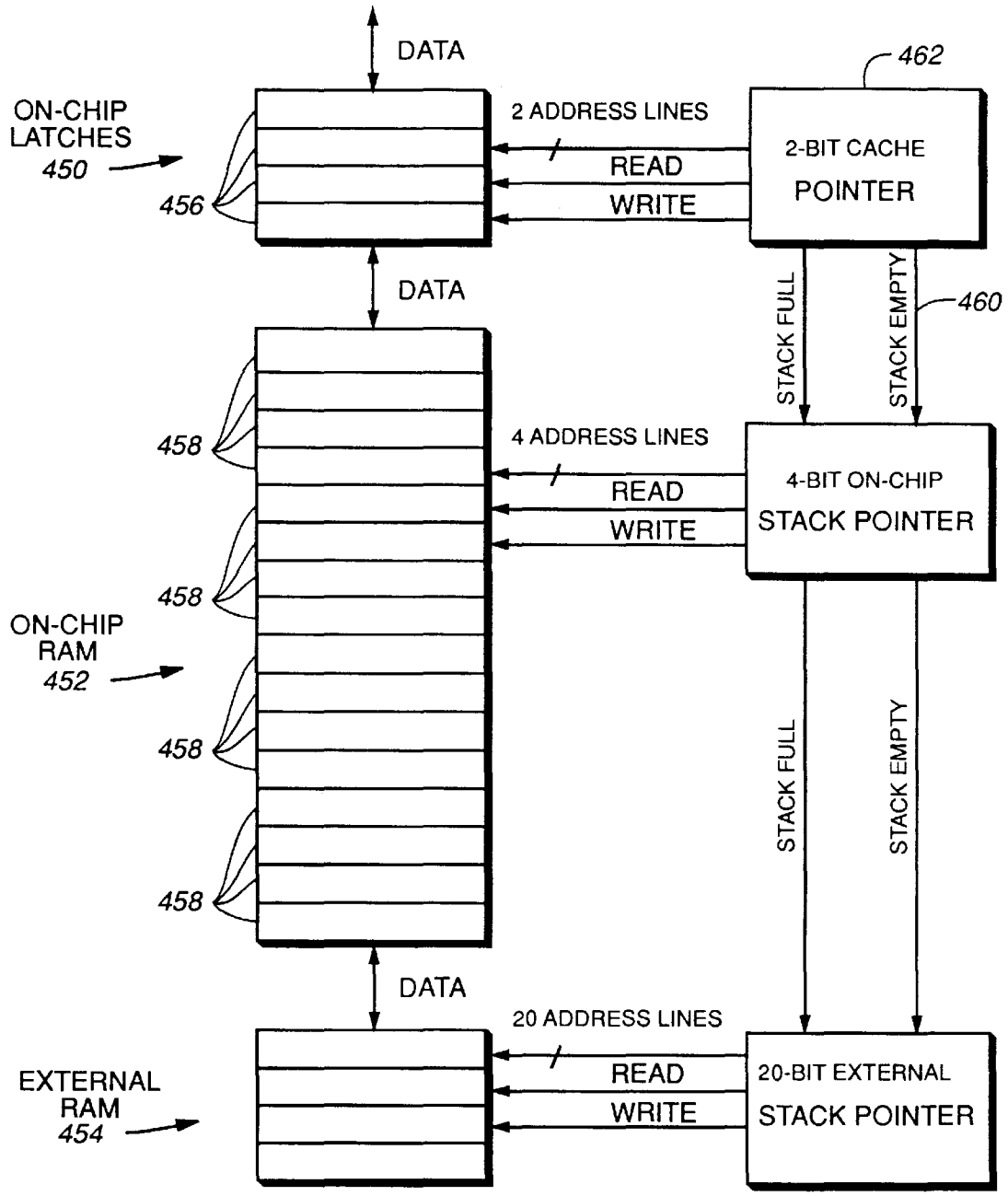

DATA
462
ON-CHIP
LATCHES
450
2 ADDRESS LINES
READ
WRITE
2-BIT CACHE
POINTER
456
DATA
STACK FULL
STACK EMPTY
460
458
4 ADDRESS LINES
READ
WRITE
4-BIT ON-CHIP
STACK POINTER
458
ON-CHIP
RAM
452
458
STACK FULL
STACK EMPTY
458
DATA
20 ADDRESS LINES
READ
WRITE
20-BIT EXTERNAL
STACK POINTER
EXTERNAL
RAM
454

FIG._21

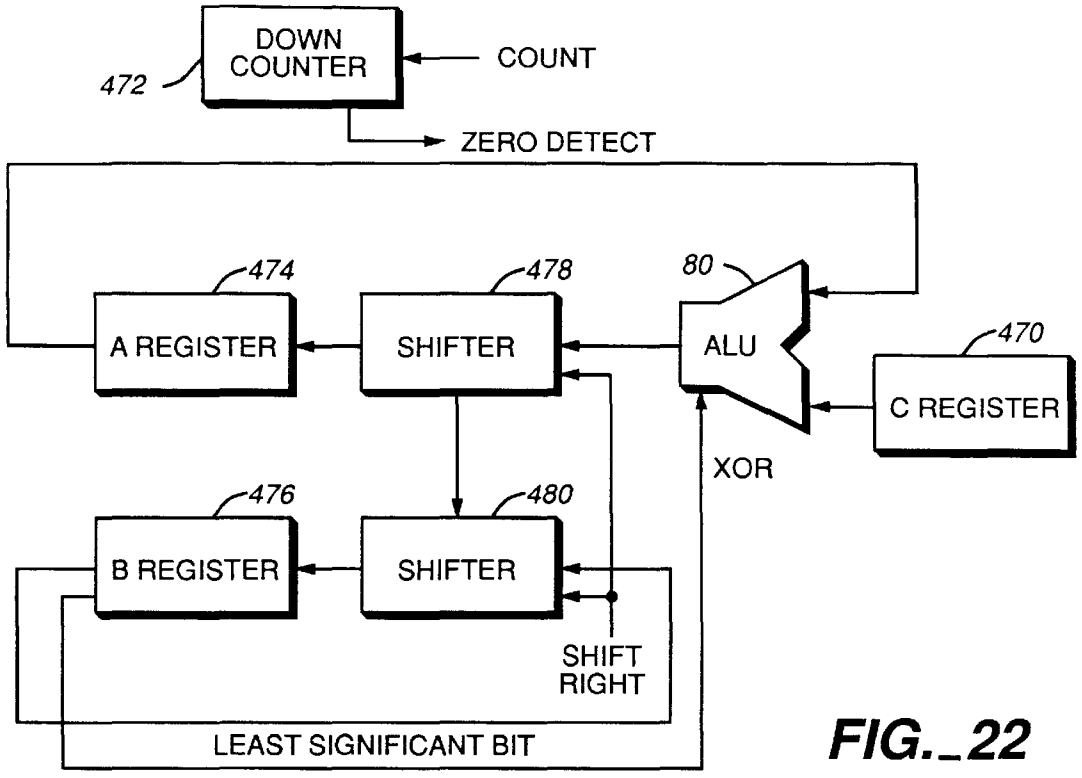

DOWN COUNTER
472
COUNT
ZERO DETECT
474
A REGISTER
478
SHIFTER
80
ALU
470
C REGISTER
XOR
476
B REGISTER
480
SHIFTER
SHIFT RIGHT
LEAST SIGNIFICANT BIT

FIG._22

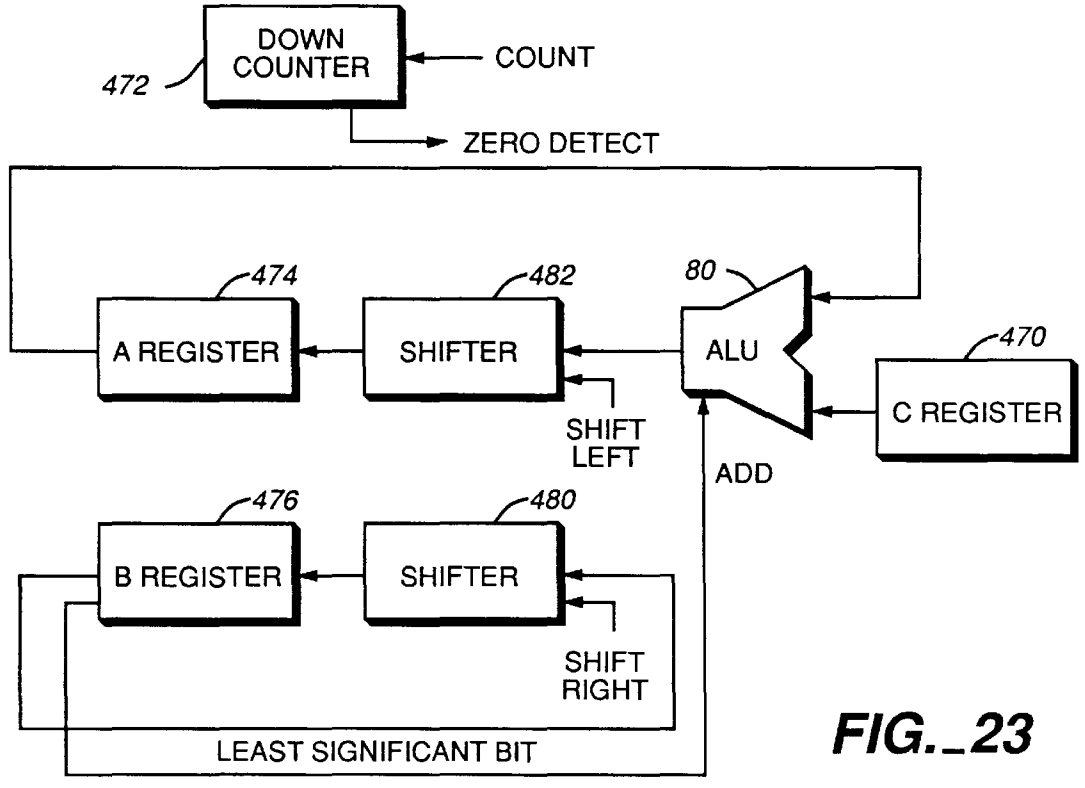

DOWN COUNTER
472
COUNT
ZERO DETECT
474
A REGISTER
482
SHIFTER
80
ALU
470
C REGISTER
SHIFT LEFT
ADD
476
B REGISTER
480
SHIFTER
SHIFT RIGHT
LEAST SIGNIFICANT BIT

FIG._23

HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a division of U.S. application Ser. No. 07/389,334, filed Aug. 3, 1989, now U.S. Pat. No. 5,440,749.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to a simplified, reduced instruction set computer (RISC) microprocessor. More particularly, it relates to such a microprocessor which is capable of performance levels of, for example, 20 million instructions per second (MIPS) at a price of, for example, 20 dollars.

2. Description of the Prior Art

Since the invention of the microprocessor, improvements in its design have taken two different approaches. In the first approach, a brute force gain in performance has been achieved through the provision of greater numbers of faster transistors in the microprocessor integrated circuit and an instruction set of increased complexity. This approach is exemplified by the Motorola 68000 and Intel 80X86 microprocessor families. The trend in this approach is to larger die sizes and packages, with hundreds of pinouts.

More recently, it has been perceived that performance gains can be achieved through comparative simplicity, both in the microprocessor integrated circuit itself and in its instruction set. This second approach provides RISC microprocessors, and is exemplified by the Sun SPARC and the Intel 8960 microprocessors. However, even with this approach as conventionally practiced, the packages for the microprocessor are large, in order to accommodate the large number of pinouts that continue to be employed. A need therefore remains for further simplification of high performance microprocessors.

With conventional high performance microprocessors, fast static memories are required for direct connection to the microprocessors in order to allow memory accesses that are fast enough to keep up with the microprocessors. Slower dynamic random access memories (DRAMs) are used with such microprocessors only in a hierarchical memory arrangement, with the static memories acting as a buffer between the microprocessors and the DRAMs. The necessity to use static memories increases cost of the resulting systems.

Conventional microprocessors provide direct memory accesses (DMA) for system peripheral units through DMA controllers, which may be located on the microprocessor integrated circuit, or provided separately. Such DMA controllers can provide routine handling of DMA requests and responses, but some processing by the main central processing unit (CPU) of the microprocessor is required.

SUMMARY OF THE INVENTION

Accordingly, it is an object of this invention to provide a microprocessor with a reduced pin count and cost compared to conventional microprocessors.

It is another object of the invention to provide a high performance microprocessor that can be directly connected to DRAMs without sacrificing microprocessor speed.

It is a further object of the invention to provide a high performance microprocessor in which DMA does not require use of the main CPU during DMA requests and responses and which provides very rapid DMA response with predictable response times.

The attainment of these and related objects may be achieved through use of the novel high performance, low cost microprocessor herein disclosed. In accordance with one aspect of the invention, a microprocessor system in accordance with this invention has a central processing unit, a dynamic random access memory and a bus connecting the central processing unit to the dynamic random access memory. There is a multiplexing means on the bus between the central processing unit and the dynamic random access memory. The multiplexing means is connected and configured to provide row addresses, column addresses and data on the bus.

In accordance with another aspect of the invention, the microprocessor system has a means connected to the bus for fetching instructions for the central processing unit on the bus. The means for fetching instructions is configured to fetch multiple sequential instructions in a single memory cycle. In a variation of this aspect of the invention, a programmable read only memory containing instructions for the central processing unit is connected to the bus. The means for fetching instructions includes means for assembling a plurality of instructions from the programmable read only memory and storing the plurality of instructions in the dynamic random access memory.

In another aspect of the invention, the microprocessor system includes a central processing unit, a direct memory access processing unit and a memory connected by a bus. The direct memory access processing unit includes means for fetching instructions for the central processing unit and for fetching instructions for the direct memory access processing unit on the bus.

In a further aspect of the invention, the microprocessor system, including the memory, is contained in an integrated circuit. The memory is a dynamic random access memory, and the means for fetching multiple instructions includes a column latch for receiving the multiple instructions.

In still another aspect of the invention, the microprocessor system additionally includes an instruction register for the multiple instructions connected to the means for fetching instructions. A means is connected to the instruction register for supplying the multiple instructions in succession from the instruction register. A counter is connected to control the means for supplying the multiple instructions to supply the multiple instructions in succession. A means for decoding the multiple instructions is connected to receive the multiple instructions in succession from the means for supplying the multiple instructions. The counter is connected to said means for decoding to receive incrementing and reset control signals from the means for decoding. The means for decoding is configured to supply the reset control signal to the counter and to supply a control signal to the means for fetching instructions in response to a SKIP instruction in the multiple instructions. In a modification of this aspect of the invention, the microprocessor system additionally has a loop counter connected to receive a decrement control signal from the means for decoding. The means for decoding is configured to supply the reset control signal to the counter and the decrement control signal to the loop counter in response to a MICROLOOP instruction in the multiple instructions. In a further modification to this aspect of the invention, the means for decoding is configured to control

the counter in response to an instruction utilizing a variable width operand. A means is connected to the counter to select the variable width operand in response to the counter.

In a still further aspect of the invention, the microprocessor system includes an arithmetic logic unit. A first push down stack is connected to the arithmetic logic unit. The first push down stack includes means for storing a top item connected to a first input of the arithmetic logic unit and means for storing a next item connected to a second input of the arithmetic logic unit. The arithmetic logic unit has an output connected to the means for storing a top item. The means for storing a top item is connected to provide an input to a register file. The register file desirably is a second push down stack, and the means for storing a top item and the register file are bidirectionally connected.

In another aspect of the invention, a data processing system has a microprocessor including a sensing circuit and a driver circuit, a memory, and an output enable line connected between the memory, the sensing circuit and the driver circuit. The sensing circuit is configured to provide a ready signal when the output enable line reaches a predetermined electrical level, such as a voltage. The microprocessor is configured so that the driver circuit provides an enabling signal on the output enable line responsive to the ready signal.

In a further aspect of the invention, the microprocessor system has a ring counter variable speed system clock connected to the central processing unit. The central processing unit and the ring counter variable speed system clock are provided in a single integrated circuit. An input/output interface is connected to exchange coupling control signals, addresses and data with the input/output interface. A second clock independent of the ring counter variable speed system clock is connected to the input/output interface.

In yet another aspect of the invention, a push down stack is connected to the arithmetic logic unit. The push down stack includes means for storing a top item connected to a first input of the arithmetic logic unit and means for storing a next item connected to a second input of the arithmetic logic unit. The arithmetic logic unit has an output connected to the means for storing a top item. The push down stack has a first plurality of stack elements configured as latches and a second plurality of stack elements configured as a random access memory. The first and second plurality of stack elements and the central processing unit are provided in a single integrated circuit. A third plurality of stack elements is configured as a random access memory external to the single integrated circuit. In this aspect of the invention, desirably a first pointer is connected to the first plurality of stack elements, a second pointer connected to the second plurality of stack elements, and a third pointer is connected to the third plurality of stack elements. The central processing unit is connected to pop items from the first plurality of stack elements. The first stack pointer is connected to the second stack pointer to pop a first plurality of items from the second plurality of stack elements when the first plurality of stack elements are empty from successive pop operations by the central processing unit. The second stack pointer is connected to the third stack pointer to pop a second plurality of items from the third plurality of stack elements when the second plurality of stack elements are empty from successive pop operations by the central processing unit.

In another aspect of the invention, a first register is connected to supply a first input to the arithmetic logic unit. A first shifter is connected between an output of the arithmetic logic unit and the first register. A second register is connected to receive a starting polynomial value. An output of the second register is connected to a second shifter. A least significant bit of the second register is connected to The arithmetic logic unit. A third register is connected to supply feedback terms of a polynomial to the arithmetic logic unit. A down counter, for counting down a number corresponding to digits of a polynomial to be generated, is connected to the arithmetic logic unit. The arithmetic logic unit is responsive to a polynomial instruction to carry out an exclusive OR of the contents of the first register with the contents of the third register if the least significant bit of the second register is a "ONE" and to pass the contents of the first register unaltered if the least significant bit of the second register is a "ZERO", until the down counter completes a count. The polynomial to be generated results in said first register.

In still another aspect of the invention, a result register is connected to supply a first input to the arithmetic logic unit. A first, left shifting shifter is connected between an output of the arithmetic logic unit and the result register. A multiplier register is connected to receive a multiplier in bit reversed form. An output of the multiplier register is connected to a second, right shifting shifter. A least significant bit of the multiplier register is connected to the arithmetic logic unit. A third register is connected to supply a multiplicand to said arithmetic logic unit. A down counter, for counting down a number corresponding to one less than the number of digits of the multiplier, is connected to the arithmetic logic unit. The arithmetic logic unit is responsive to a multiply instruction to add the contents of the result register with the contents of the third register, when the least significant bit of the multiplier register is a "ONE" and to pass the contents of the result register unaltered, until the down counter completes a count. The product results in the result register.

The attainment of the foregoing and related objects, advantages and features of the invention should be more readily apparent to those skilled in the art, after review of the following more detailed description of the invention, taken together with the drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an external, plan view of an integrated circuit package incorporating a microprocessor in accordance with the invention.

FIG. **2** is a block diagram of a microprocessor in accordance with the invention.

FIG. **3** is a block diagram of a portion of a data processing system incorporating the microprocessor of FIGS. **1** and **2**.

FIG. **4** is a more detailed block diagram of a portion of the microprocessor shown in FIG. **2**.

FIG. **5** is a more detailed block diagram of another portion of the microprocessor shown in FIG. **2**.

FIG. **6** is a block diagram of another portion of the data processing system shown in part in FIG. **3** and incorporating the microprocessor of FIGS. **1**–**2** and **4**–**5**.

FIGS. **7** and **8** are layout diagrams for the data processing system shown in part in FIGS. **3** and **6**.

FIG. **9** is a layout diagram of a second embodiment of a microprocessor in accordance with the invention in a data processing system on a single integrated circuit.

FIG. **10** is a more detailed block diagram of a portion of the data processing system of FIGS. **7** and **8**.

FIG. **11** is a timing diagram useful for understanding operation of the system portion shown in FIG. **12**.

FIG. **12** is another more detailed block diagram of a further portion of the data processing system of FIGS. **7** and **8**.

FIG. **13** is a more detailed block diagram of a portion of the microprocessor shown in FIG. **2**.

FIG. **14** is a more detailed block and schematic diagram of a portion of the system shown in FIGS. **3** and **7–8**.

FIG. **15** is a graph useful for understanding operation of the system portion shown in FIG. **14**.

FIG. **16** is a more detailed block diagram showing part of the system portion shown in FIG. **4**.

FIG. **17** is a more detailed block diagram of a portion of the microprocessor shown in FIG. **2**.

FIG. **18** is a more detailed block diagram of part of the microprocessor portion shown in FIG. **17**.

FIG. **19** is a set of waveform diagrams useful for understanding operation of the part of the microprocessor portion shown in FIG. **18**.

FIG. **20** is a more detailed block diagram showing another part of the system portion shown in FIG. **4**.

FIG. **21** is a more detailed block diagram showing another part of the system portion shown in FIG. **4**.

FIGS. **22** and **23** are more detailed block diagrams showing another part of the system portion shown in FIG. **4**.

DETAILED DESCRIPTION OF THE INVENTION

Overveiw

The microprocessor of this invention is desirably implemented as a 32-bit microprocessor optimized for:

HIGH EXECUTION SPEED, and

LOW SYSTEM COST.

In this embodiment, the microprocessor can be thought of as 20 MIPS for 20 dollars. Important distinguishing features of the microprocessor are:

Uses low-cost commodity DYNAMIC RAMS to run 20 MIPS

4 instruction fetch per memory cycle

On-chip fast page-mode memory management

Runs fast without external cache

Requires few interfacing chips

Crams 32-bit CPU in 44 pin SOJ package

The instruction set is organized so that most operations can be specified with 8-bit instructions. Two positive products of this philosophy are:

Programs are smaller,

Programs can execute much faster.

The bottleneck in most computer systems is the memory bus. The bus is used to fetch instructions and fetch and store data. The ability to fetch four instructions in a single memory bus cycle significantly increases the bus availability to handle data.

Turning now to the drawings, more particularly to FIG. **1**, there is shown a packaged 32-bit microprocessor **50** in a 44-pin plastic leadless chip carrier, shown approximately 100 times its actual size of about 0.8 inch on a side. The fact that the microprocessor **50** is provided as a 44-pin package represents a substantial departure from typical microprocessor packages, which usually have about 200 input/output (I/O) pins. The microprocessor **50** is rated at 20 million instructions per second (MIPS). Address and data lines **52**, also labelled D**0**–D**31**, are shared for addresses and data without speed penalty as a result of the manner in which the microprocessor **50** operates, as will be explained below.

DYNAMIC RAM

In addition to the low cost 44-pin package, another unusual aspect of the high performance microprocessor **50** is that it operates directly with dynamic random access memories (DRAMs), as shown by row address strobe (RAS) and column address strobe (CAS) I/O pins **54**. The other I/O pins for the microprocessor **50** include V_{DD} pins **56**, V_{SS} pins **58**, output enable pin **60**, write pin **62**, clock pin **64** and reset pin **66**.

All high speed computers require high speed and expensive memory to keep up. The highest speed static RAM memories cost as much as ten times as much as slower dynamic RAMs. This microprocessor has been optimized to use low-cost dynamic RAM in high-speed page-mode. Page-mode dynamic RAMs offer static RAM performance without the cost penalty. For example, low-cost 85 nsec. dynamic RAMs access at 25 nsec when operated in fast page-mode. Integrated fast page-mode control on the microprocessor chip simplifies system interfacing and results in a faster system.

Details of the microprocessor **50** are shown in FIG. **2**. The microprocessor **50** includes a main central processing unit (CPU) **70** and a separate direct memory access (DMA) CPU **72** in a single integrated circuit making up the microprocessor **50**. The main CPU **70** has a first **16** deep push down stack **74**, which has a top item register **76** and a next item register **78**, respectively connected to provide inputs to an arithmetic logic unit (ALU) **80** by lines **82** and **84**. An output of the ALU **80** is connected to the top item register **76** by line **86**. The output of the top item register at **82** is also connected by line **88** to an internal data bus **90**.

A loop counter **92** is connected to a decrementer **94** by lines **96** and **98**. The loop counter **92** is bidirectionally connected to the internal data bus **90** by line **100**. Stack pointer **102**, return stack pointer **104**, mode register **106** and instruction register **108** are also connected to the internal data bus **90** by lines **110**, **112**, **114** and **116**, respectively. The internal data bus **90** is connected to memory controller **118** and to gate **120**. The gate **120** provides inputs on lines **122**, **124**, and **126** to X register **128**, program counter **130** and Y register **132** of return push down stack **134**. The X register **128**, program counter **130** and Y register **132** provide outputs to internal address bus **136** on lines **138**, **140** and **142**. The internal address bus provides inputs to the memory controller **118** and to an incrementer **144**. The incrementer **144** provides inputs to the X register, program counter and Y register via lines **146**, **122**, **124** and **126**. The DMA CPU **72** provides inputs to the memory controller **118** on line **148**. The memory controller **118** is connected to a RAM (not shown) by address/data bus **150** and control lines **152**.

FIG. **2** shows that the microprocessor **50** has a simple architecture. Prior art RISC microprocessors are substantially more complex in design. For example, the SPARC RISC microprocessor has three times the gates of the microprocessor **50**, and the Intel 8960 RISC microprocessor has 20 times the gates of the microprocessor **50**. The speed of this microprocessor is in substantial part due to this simplicity. The architecture incorporates push down stacks and register write to achieve this simplicity.

The microprocessor **50** incorporates an I/O that has been tuned to make heavy use of resources provided on the integrated circuit chip. On chip latches allow use of the same I/O circuits to handle three different things: column addressing, row addressing and data, with a slight to non-existent speed penalty. This triple bus multiplexing results in fewer buffers to expand, fewer interconnection lines, fewer I/O pins and fewer internal buffers.

The provision of on-chip DRAM control gives a performance equal to that obtained with the use of static RAMs. As a result, memory is provided at ¼ the system cost of static RAM used in most RISC systems.

The microprocessor **50** fetches 4 instructions per memory cycle; the instructions are in an 8-bit format, and this is a 32-bit microprocessor. System speed is therefore 4 times the memory bus bandwidth. This ability enables the microprocessor to break the Von Neumann bottleneck of the speed of getting the next instruction. This mode of operation is possible because of the use of a push down stack and register array. The push down stack allows the use of implied addresses, rather than the prior art technique of explicit addresses for two sources and a destination.

Most instructions execute in 20 nanoseconds in the microprocessor **50**. The microprocessor can therefore execute instructions at 50 peak MIPS without pipeline delays. This is a function of the small number of gates in the microprocessor **50** and the high degree of parallelism in the architecture of the microprocessor.

FIG. **3** shows how column and row addresses are multiplexed on lines D**8**–D**14** of the microprocessor **50** for addressing DRAM **150** from I/O pins **52**. The DRAM **150** is one of eight, but only one DRAM **150** has been shown for clarity. As shown, the lines D**11**–D**18** are respectively connected to row address inputs A**0**–A**8** of the DRAM **150**. Additionally, lines D**12**–D**15** are connected to the data inputs DQ**1**–DQ**4** of the DRAM **150**. The output enable, write and column address strobe pins **54** are respectively connected to the output enable, write and column address strobe inputs of the DRAM **150** by lines **152**. The row address strobe pin **54** is connected through row address strobe decode logic **154** to the row address strobe input of the DRAM **150** by lines **156** and **158**.

D**0**–D**7** pins **52** (FIG. **1**) are idle when the microprocessor **50** is outputting multiplexed row and column addresses on D**11**–D**18** pins **52**. The D**0**–D**7** pins **52** can therefore simultaneously be used for I/O when right justified I/O is desired. Simultaneous addressing and I/O can therefore be carried out.

FIG. **4** shows how the microprocessor **50** is able to achieve performance equal to the use of static RAMS with DRAMs through multiple instruction fetch in a single clock cycle and instruction fetch-ahead. Instruction register **108** receives four 8-bit byte instruction words 1–4 on 32-bit internal data bus **90**. The four instruction byte 1–4 locations of the instruction register **108** are connected to multiplexer **170** by busses **172**, **174**, **176** and **178**, respectively. A microprogram counter **180** is connected to the multiplexer **170** by lines **182**. The multiplexer **170** is connected to decoder **184** by bus **186**. The decoder **184** provides internal signals to the rest of the microprocessor **50** on lines **188**.

Most significant bits **190** of each instruction byte 1–4 location are connected to a 4-input decoder **192** by lines **194**. The output of decoder **192** is connected to memory controller **118** by line **196**. Program counter **130** is connected to memory controller **118** by internal address bus **136**, and the instruction register **108** is connected to the memory controller **118** by the internal data bus **90**. Address/data bus **198** and control bus **200** are connected to the DRAMS **150** (FIG. **3**).

In operation, when the most significant bits **190** of remaining instructions 1–4 are "1" in a clock cycle of the microprocessor **50**, there are no memory reference instructions in the queue. The output of decoder **192** on line **196** requests an instruction fetch ahead by memory controller **118** without interference with other accesses. While the current instructions in instruction register **108** are executing, the memory controller **118** obtains the address of the next set of four instructions from program counter **130** and obtains that set of instructions. By the time the current set of instructions has completed execution, the next set of instructions is ready for loading into the instruction register.

Details of the DMA CPU **72** are provided in FIG. **5**. Internal data bus **90** is connected to memory controller **118** and to DMA instruction register **210**. The DMA instruction register **210** is connected to DMA program counter **212** by bus **214**, to transfer size counter **216** by bus **218** and to timed transfer interval counter **220** by bus **222**. The DMA instruction register **210** is also connected to DMA I/O and RAM address register **224** by line **226**. The DMA I/O and RAM address register **224** is connected to the memory controller **118** by memory cycle request line **228** and bus **230**. The DMA program counter **212** is connected to the internal address bus **136** by bus **232**. The transfer size counter **216** is connected to a DMA instruction done decrementer **234** by lines **236** and **238**. The decrementer **234** receives a control input on memory cycle acknowledge line **240**. When transfer size counter **216** has completed its count, it provides a control signal to DMA program counter **212** on line **242**. Timed transfer interval counter **220** is connected to decrementer **244** by lines **246** and **248**. The decrementer **244** receives a control input from a microprocessor system clock on line **250**.

The DMA CPU **72** controls itself and has the ability to fetch and execute instructions. It operates as a co-processor to the main CPU **70** (FIG. **2**) for time specific processing.

FIG. **6** shows how the microprocessor **50** is connected to an electrically programmable read only memory (EPROM) **260** by reconfiguring the data lines **52** so that some of the data lines **52** are input lines and some of them are output lines. Data lines **52** D**0**–D**7** provide data to and from corresponding data terminals **262** of the EPROM **260**. Data lines **52** D**9**–D**18** provide addresses to address terminals **264** of the EPROM **260**. Data lines **52** D**19**–D**31** provide inputs from the microprocessor **50** to memory and I/O decode logic **266**. RAS 0/1 control line **268** provides a control signal for determining whether the memory and I/O decode logic provides a DRAM RAS output on line **270** or a column enable output for the EPROM **260** on line **272**. Column address strobe terminal **60** of the microprocessor **50** provides an output enable signal on line **274** to the corresponding terminal **276** of the EPROM **260**.

FIGS. **7** and **8** show the front and back of a one card data processing system **280** incorporating the microprocessor **50**, MSM514258-10 type DRAMs **150** totalling 2 megabytes, a Motorola 50 MegaHertz crystal oscillator clock **282**, I/O circuits **284** and a 27256 type EPROM **260**. The I/O circuits **284** include a 74HC04 type high speed hex inverter circuit **286**, an IDT39C828 type 10-bit inverting buffer circuit **288**, an IDT39C822 type 10-bit inverting register circuit **290**, and two IDT39C823 type 9-bit non-inverting register circuits **292**. The card **280** is completed with a MAX12V type DC-DC converter circuit **294**, 34-pin dual AMP type headers **296**, a coaxial female power connector **298**, and a 3-pin AMP right angle header **300**. The card **280** is a low cost, imbeddable product that can be incorporated in larger systems or used as an internal development tool.

The microprocessor **50** is a very high performance (50 MHz) RISC influenced 32-bit CPU designed to work closely with dynamic RAM. Clock for clock, the microprocessor **50** approaches the theoretical performance limits possible with a single CPU configuration. Eventually, the microprocessor **50** and any other processor is limited by the bus bandwidth and the number of bus paths. The critical conduit is between the CPU and memory.

One solution to the bus bandwidth/bus path problem is to integrate a CPU directly onto the memory chips, giving every memory a direct bus the CPU. FIG. **9** shows another microprocessor **310** that is provided integrally with 1 mega-

bit of DRAM **311** in a single integrated circuit **312**. Until the present invention, this solution has not been practical, because most high performance CPUs require from 500,000 to 1,000,000 transistors and enormous die sizes just by themselves. The microprocessor **310** is equivalent to the microprocessor **50** in FIGS. **1–8**. The microprocessors **50** and **310** are the most transistor efficient high performance CPUs in existence, requiring fewer than 50,000 transistors for dual processors **70** and **72** (FIG. **2**) or **314** and **316** (less memory). The very high speed of the microprocessors **50** and **310** is to a certain extent a function of the small number of active devices. In essence, the less silicon gets in the way, the faster the electrons can get where they are going.

The microprocessor **310** is therefore the only CPU suitable for integration on the memory chip die **312**. Some simple modifications to the basic microprocessor **50** to take advantage of the proximity to the DRAM array **311** can also increase the microprocessor **50** clock speed by **50** percent, and probably more.

The microprocessor **310** core on board the DRAM die **312** provides most of the speed and functionality required for a large group of applications from automotive to peripheral control. However, the integrated CPU **310**/DRAM **311** concept has the potential to redefine significantly the way multiprocessor solutions can solve a spectrum of very compute intensive problems. The CPU **310**/DRAM **311** combination eliminates the Von Neumann bottleneck by distributing it across numerous CPU/DRAM chips **312**. The microprocessor **310** is a particularly good core for multiprocessing, since it was designed with the SDI targeting array in mind, and provisions were made for efficient interprocessor communications.

Traditional multiprocessor implementations have been very expensive in addition to being unable to exploit fully the available CPU horsepower. Multiprocessor systems have typically been built up from numerous board level or box level computers. The result is usually an immense amount of hardware with corresponding wiring, power consumption and communications problems. By the time the systems are interconnected, as much as 50 percent of the bus speed has been utilized just getting through the interfaces.

In addition, multiprocessor system software has been scarce. A multiprocessor system can easily be crippled by an inadequate load-sharing algorithm in the system software, which allows one CPU to do a great deal of work and the others to be idle. Great strides have been made recently in systems software, and even UNIX V.4 may be enhanced to support multiprocessing. Several commercial products from such manufacturers as DUAL Systems and UNISOFT do a credible job on 68030 type microprocessor systems now.

The microprocessor **310** architecture eliminates most of the interface friction, since up to 64 CPU **310**/RAM **311** processors should be able to intercommunicate without buffers or latches. Each chip **312** has about 40 MIPS raw speed, because placing the DRAM **311** next to the CPU **310** allows the microprocessor **310** instruction cycle to be cut in half, compared to the microprocessor **50**. A 64 chip array of these chips **312** is more powerful than any other existing computer. Such an array fits on a 3×5 card, cost less than a FAX machine, and draw about the same power as a small television.

Dramatic changes in price/performance always reshape existing applications and almost always create new ones. The introduction of microprocessors in the mid 1970s created video games, personal computers, automotive computers, electronically controlled appliances, and low cost computer peripherals.

The integrated circuit **312** will find applications in all of the above areas, plus create some new ones. A common generic parallel processing algorithm handles convolution/Fast Fourier Transform (FFT)/pattern recognition. Interesting product possibilities using the integrated circuit **312** include high speed reading machines, real-time speech recognition, spoken language translation, real-time robot vision, a product to identify people by their faces, and an automotive or aviation collision avoidance system.

A real time processor for enhancing high density television (HDTV) images, or compressing the HDTV information into a smaller bandwidth, would be very. feasible. The load sharing in HDTV could be very straightforward. Splitting up the task according to color and frame would require 6, 9 or 12 processors. Practical implementation might require 4 meg RAMs integrated with the microprocessor **310**.

The microprocessor **310** has the following specifications:

CONTROL LINES
4—POWER/GROUND
1—CLOCK
32—DATA I/O
4—SYSTEM CONTROL
EXTERNAL MEMORY FETCH
EXTERNAL MEMORY FETCH AUTOINCREMENT X
EXTERNAL MEMORY FETCH AUTOINCREMENT Y
EXTERNAL MEMORY WRITE
EXTERNAL MEMORY WRITE AUTOINCREMENT X
EXTERNAL MEMORY WRITE AUTOINCREMENT Y
EXTERNAL PROM FETCH
LOAD ALL X REGISTERS
LOAD ALL Y REGISTERS
LOAD ALL PC REGISTERS
EXCHANGE X AND Y
INSTRUCTION FETCH
ADD TO PC
ADD TO X
WRITE MAPPING REGISTER
READ MAPPING REGISTER
REGISTER CONFIGURATION
MICROPROCESSOR **310** CPU **316** CORE
COLUMN LATCH**1** (1024 BITS) 32×32 MUX
STACK POINTER (16 BITS)
COLUMN LATCH**2** (1024 BITS) 32×32 MUX
RSTACK POINTER (16 BITS)
PROGRAM COUNTER 32 BITS
X0 REGISTER 32 BITS (ACTIVATED ONLY FOR ON-CHIP ACCESSES)
Y0 REGISTER 32 BITS (ACTIVATED ONLY FOR ON-CHIP ACCESSES)
LOOP COUNTER 32 BITS
DMA CPU **314** CORE
DMA PROGRAM COUNTER 24 BITS
INSTRUCTION REGISTER 32 BITS
I/O & RAM ADDRESS REGISTER 32 BITS
TRANSFER SIZE COUNTER 12 BITS
INTERVAL COUNTER 12 BITS

To offer memory expansion for the basic chip **312**, an intelligent DRAM can be produced. This chip will be optimized for high speed operation with the integrated circuit **312** by having three on-chip address registers: Program Counter, X Register and Y register. As a result, to access the intelligent DRAM, no address is required, and a total access cycle could be as short as 10 nsec. Each

expansion DRAM would maintain its own copy of the three registers and would be identified by a code specifying its memory address. Incrementing and adding to the three registers will actually take place on the memory chips. A maximum of 64 intelligent DRAM peripherals would allow a large system to be created without sacrificing speed by introducing multiplexers or buffers.

There are certain differences between the microprocessor **310** and the microprocessor **50** that arise from providing the microprocessor **310** on the same die **312** with the DRAM **311**. Integrating the DRAM **311** allows architectural changes in the microprocessor **310** logic to take advantage of existing on-chip DRAM **311** circuitry. Row and column design is inherent in memory architecture. The DRAMs **311** access random bits in a memory array by first selecting a row of 1024 bits, storing them into a column latch, and then selecting one of the bits as the data to be read or written.

The time required to access the data is split between the row access and the column access. Selecting data already stored in a column latch is faster than selecting a random bit by at least a factor of six. The microprocessor **310** takes advantage of this high speed by creating a number of column latches and using them as caches and shift registers. Selecting a new row of information may be thought of as performing a 1024-bit read or write with the resulting immense bus bandwidth.

1. The microprocessor **50** treats its 32-bit instruction register **108** (see FIGS. **2** and **4**) as a cache for four 8-bit instructions. Since the DRAM **311** maintains a 1024-bit latch for the column bits, the microprocessor **310** treats the column latch as a cache for 128 8-bit instructions. Therefore, the next instruction will almost always be already present in the cache. Long loops within the cache are also possible and more useful than the 4 instruction loops in the microprocessor **50**.

2. The microprocessor **50** uses two 16×32-bit deep register arrays **74** and **134** (FIG. **2**) for the parameter stack and the return stack. The microprocessor **310** creates two other 1024-bit column latches to provide the equivalent of two 32×32-bit arrays, which can be accessed twice as fast as a register array.

3. The microprocessor **50** has a DMA capability which can be used for I/O to a video shift register. The microprocessor **310** uses yet another 1024-bit column latch as a long video shift register to drive a CRT display directly. For color displays, three on-chip shift registers could also be used. These shift registers can transfer pixels at a maximum of 100 MHz.

4. The microprocessor **50** accesses memory via an external 32-bit bus. Most of the memory **311** for the microprocessor **310** is on the same die **312**. External access to more memory is made using an 8-bit bus. The result is a smaller die, smaller package and lower power consumption than the microprocessor **50**.

5. The microprocessor **50** consumes about a third of its operating power charging and discharging the I/O pins and associated capacitances. The DRAMs **150** (FIG. **8**) connected to the microprocessor **50** dissipate most of their power in the I/O drivers. A microprocessor **310** system will consume about one-tenth the power of a microprocessor **50** system, since having the DRAM **311** next to the processor **310** eliminates most of the external capacitances to be charged and discharged.

6. Multiprocessing means splitting a computing task between numerous processors in order to speed up the solution. The popularity of multiprocessing is limited by the expense of current individual processors as well as the limited interprocessor communications ability. The microprocessor **310** is an excellent multiprocessor candidate, since the chip **312** is a monolithic computer complete with memory, rendering it low-cost and physically compact.

The shift registers implemented with the microprocessor **310** to perform video output can also be configured as interprocessor communication links. The INMOS transputer attempted a similar strategy, but at much lower speed and without the performance benefits inherent in the microprocessor **310** column latch architecture. Serial I/O is a prerequisite for many multiprocessor topologies because of the many neighbor processors which communicate. A cube has 6 neighbors. Each neighbor communicates using these lines:

DATA IN
CLOCK IN
READY FOR DATA
DATA OUT
DATA READY?
CLOCK OUT

A special start up sequence is used to initialize the on-chip DRAM **311** in each of the processors.

The microprocessor **310** column latch architecture allows neighbor processors to deliver information directly to internal registers or even instruction caches of other chips **312**. This technique is not used with existing processors, because it only improves performance in a tightly coupled DRAM system.

7. The microprocessor **50** architecture offers two types of looping structures: LOOP-IF-DONE and MICRO-LOOP. The former takes an 8-bit to 24-bit operand to describe the entry point to the loop address. The latter performs a loop entirely within the 4 instruction queue and the loop entry point is implied as the first instruction in the queue. Loops entirely within the queue run without external instruction fetches and execute up to three times as fast as the long loop construct. The microprocessor **310** retains both constructs with a few differences. The microprocessor **310** microloop functions in the same fashion as the microprocessor **50** operation, except the queue is 1024-bits or 128 8-bit instructions long. The microprocessor **310** microloop can therefore contain jumps, branches, calls and immediate operations not possible in the 4 8-bit instruction microprocessor **50** queue.

Microloops in the microprocessor **50** can only perform simple block move and compare functions. The larger microprocessor **310** queue allows entire digital signal processing or floating point algorithms to loop at high speed in the queue.

The microprocessor **50** offers four instructions to redirect execution:

CALL
BRANCH
BRANCH-IF-ZERO
LOOP-IF-NOT-DONE

These instructions take a variable length address operand 8, 16 or 24 bits long. The microprocessor **50** next address logic treats the three operands similarly by adding or subtracting them to the current program counter. For the microprocessor **310**, the 16 and 24-bit operands function in the same manner as the 16 and 24-bit operands in the microprocessor **50**. The 8-bit class operands are reserved to operate entirely within the instruction queue. Next address decisions can therefore be made quickly, because only 10 bits of addresses are affected, rather than 32. There is no carry or borrow generated past the 10 bits.

8. The microprocessor **310** CPU **316** resides on an already crowded DRAM die **312**. To keep chip size as small as

possible, the DMA processor **72** of the microprocessor **50** has been replaced with a more traditional DMA controller **314**. DMA is used with the microprocessor **310** to perform the following functions:

Video output to a CRT

Multiprocessor serial communications

8-bit parallel I/O

The DMA controller **314** can maintain both serial and parallel transfers simultaneously. The following DMA sources and destinations are supported by the microprocessor **310**:

DESCRIPTION	I/O	LINES
1. Video shift register	OUTPUT	1 to 3
2. Multiprocessor serial	BOTH	6 lines/channel
3. 8-bit parallel	BOTH	8 data, 4 control

The three sources use separate 1024-bit buffers and separate I/O pins. Therefore, all three may be active simultaneously without interference.

The microprocessor **310** can be implemented with either a single multiprocessor serial buffer or separate receive and sending buffers for each channel, allowing simultaneous bidirectional communications with six neighbors simultaneously.

FIGS. **10** and **11** provide details of the PROM DMA used in the microprocessor **50**. The microprocessor **50** executes faster than all but the fastest PROMs. PROMS are used in a microprocessor **50** system to store program segments and perhaps entire programs. The microprocessor **50** provides a feature on power-up to allow programs to be loaded from low-cost, slow speed PROMs into high speed DRAM for execution. The logic which performs this function is part of the DMA memory controller **118**. The operation is similar to DMA, but not identical, since four 8-bit bytes must be assembled on the microprocessor **50** chip, then written to the DRAM **150**.

The microprocessor **50** directly interfaces to DRAM **150** over a triple multiplexed data and address bus **350**, which carries RAS addresses, CAS addresses and data. The EPROM **260**, on the other hand, is read with non-multiplexed busses. The microprocessor **50** therefore has a special mode which unmultiplexes the data and address lines to read 8 bits of EPROM data. Four 8-bit bytes are read in this fashion. The multiplexed bus **350** is turned back on, and the data is written to the DRAM **150**.

When the microprocessor **50** detects a RESET condition, the processor stops the main CPU **70** and forces a mode **0** (PROM LOAD) instruction into the DMA CPU **72** instruction register. The DMA instruction directs the memory controller to read the EPROM **260** data at 8 times the normal access time for memory. Assuming a 50 MHz microprocessor **50**, this means an access time of 320 nsec. The instruction also indicates:

The selection address of the EPROM **260** to be loaded,

The number of 32-bit words to transfer,

The DRAM **150** address to transfer into.

The sequence of activities to transfer one 32-bit word from EPROM **260** to DRAM **150** are:

1. RAS goes low at **352**, latching the EPROM **260** select information from the high order address bits. The EPROM **260** is selected.
2. Twelve address bits (consisting of what is normally DRAM CAS addresses plus two byte select bits are placed on the bus **350** going to the EPROM **260** address pins. These signals will remain on the lines until the data from the EPROM **260** has been read into the microprocessor **50**. For the first byte, the byte select bits will be binary 00.
3. CAS goes low at **354**, enabling the EPROM **260** data onto the lower 8 bits of the external address/data bus **350**. NOTE: It is important to recognize that, during this part of the cycle, the lower 8 bits of the external data/address bus are functioning as inputs, but the rest of the bus is still acting as outputs.
4. The microprocessor **50** latches these eight least significant bits internally and shifts them 8 bits left to shift them to the next significant byte position.
5. Steps 2, 3 and 4 are repeated with byte address 01.
6. Steps 2, 3 and 4 are repeated with byte address 10.
7. Steps 2, 3 and 4 are repeated with byte address 11.
8. CAS goes high at **356**, taking the EPROM **260** off the data bus.
9. RAS goes high at **358**, indicating the end of the EPROM **260** access.
10. RAS goes low at **360**, latching the DRAM select information from the high order address bits. At the same time, the RAS address bits are latched into the DRAM **150**. The DRAM **150** is selected.
11. CAS goes low at **362**, latching the DRAM **150** CAS addresses.
12. The microprocessor **50** places the previously latched EPROM **260** 32-bit data onto the external address/data bus **350**. W goes low at **364**, writing the 32 bits into the DRAM **150**.
13. W goes high at **366**. CAS goes high at **368**. The process continues with the next word.

FIG. **12** shows details of the microprocessor **50** memory controller **118**. In operation, bus requests stay present until they are serviced. CPU **70** requests are prioritized at **370** in the order of: 1, Parameter Stack; 2, Return Stack; 3, Data Fetch; 4, Instruction Fetch. The resulting CPU request signal and a DMA request signal are supplied as bus requests to bus control **372**, which provides a bus grant signal at **374**. Internal address bus **136** and a DMA counter **376** provide inputs to a multiplexer **378**. Either a row address or a column address are provided as an output to multiplexed address bus **380** as an output from the multiplexer **378**. The multiplexed address bus **380** and the internal data bus **90** provide address and data inputs, respectively, to multiplexer **382**. Shift register **384** supplies row address strobe (RAS) **1** and **2** control signals to multiplexer **386** and column address strobe (CAS) **1** and **2** control signals to multiplexer **388** on lines **390** and **392**. The shift register **384** also supplies output enable (OE) and write (W) signals on lines **394** and **396** and a control signal on line **398** to multiplexer **382**. The shift register **384** receives a RUN signal on line **400** to generate a memory cycle and supplies a MEMORY READY signal on line **402** when an access is complete.

STACK/REGISTER ARCHITECTURE

Most microprocessors use on-chip registers for temporary storage of variables. The on-chip registers access data faster than off-chip RAM. A few microprocessors use an on-chip push down stack for temporary storage.

A stack has the advantage of faster operation compared to on-chip registers by avoiding the necessity to select source and destination registers. (A math or logic operation always uses the top two stack items as source and the top of stack as destination.) The stack's disadvantage is that it makes some operations clumsy. Some compiler activities in particular require on-chip registers for efficiency.

As shown in FIG. **13**, the microprocessor **50** provides both on-chip registers **134** and a stack **74** and reaps the benefits of both.

BENEFITS:

1. Stack math and logic is twice as fast as those available on an equivalent register only machine. Most programmers and optimizing compilers can take advantage of this feature.
2. Sixteen registers are available for on-chip storage of local variables which can transfer to the stack for computation. The accessing of variables is three to four times as fast as available on a strictly stack machine.

The combined stack **74**/register **134** architecture has not been used previously due to inadequate understanding by computer designers of optimizing compilers and the mix of transfer versus math/logic instructions.

ADAPTIVE MEMORY CONTROLLER

A microprocessor must be designed to work with small or large memory configurations. As more memory loads are added to the data, address, and control lines, the switching speed of the signals slows down. The microprocessor **50** multiplexes the address/data bus three ways, so timing between the phases is critical. A traditional approach to the problem allocates a wide margin of time between bus phases so that systems will work with small or large numbers of memory chips connected. A speed compromise of as much as 50% is required.

As shown in FIG. **14**, the microprocessor **50** uses a feedback technique to allow the processor to adjust memory bus timing to be fast with small loads and slower with large ones. The OUTPUT ENABLE (OE) line **152** from the microprocessor **50** is connected to all memories **150** on the circuit board. The loading on the output enable line **152** to the microprocessor **50** is directly related to the number of memories **150** connected. By monitoring how rapidly OE **152** goes high after a read, the microprocessor **50** is able to determine when the data hold time has been satisfied and place the next address on the bus.

The level of the OE line **152** is monitored by CMOS input buffer **410** which generates an internal READY signal on line **412** to the microprocessor's memory controller. Curves **414** and **416** of the FIG. **15** graph show the difference in rise time likely to be encountered from a lightly to heavily loaded memory system. When the OE line **152** has reached a predetermined level to generate the READY signal, driver **418** generates an OUTPUT ENABLE signal on OE line **152**.

SKIP WITHIN THE INSTRUCTION CACHE

The microprocessor **50** fetches four 8-bit instructions each memory cycle and stores them in a 32-bit instruction register **108**, as shown in FIG. **16**. A class of "test and skip" instructions can very rapidly execute a very fast jump operation within the four instruction cache.

SKIP CONDITIONS:

Always

ACC non-zero

ACC negative

Carry flag equal logic one

Never

ACC equal zero

ACC positive

Carry flag equal logic zero

The SKIP instruction can be located in any of the four byte positions **420** in the 32-bit instruction register **108**. If the test is successful, SKIP will jump over the remaining one, two, or three 8-bit instructions in the instruction register **108** and cause the next four-instruction group to be loaded into the register **108**. As shown, the SKIP operation is implemented by resetting the 2-bit microinstruction counter **180** to zero on line **422** and simultaneously latching the next instruction group into the register **108**. Any instructions following the SKIP in the instruction register are overwritten by the new instructions and not executed.

The advantage of SKIP is that optimizing compilers and smart programmers can often use it in place of the longer conditional JUMP instruction. SKIP also makes possible microloops which exit when the loop counts down or when the SKIP jumps to the next instruction group. The result in very fast code.

Other machines (such as the PDP-8 and Data General NOVA) provide the ability to skip a single instruction. The microprocessor **50** provides the ability to skip up to three instructions.

MICROLOOP IN THE INSTRUCTION CACHE

The microprocessor **50** provides the MICROLOOP instruction to execute repetitively from one to three instructions residing in the instruction register **108**. The microloop instruction works in conjunction with the LOOP COUNTER **92** (FIG. **2**) connected to the internal data bus **90**. To execute a microloop, the program stores a count in LOOP COUNTER **92**. MICROLOOP may be placed in the first, second, third, or last byte **420** of the instruction register **108**. If placed in the first position, execution will just create a delay equal to the number stored in LOOP COUNTER **92** times the machine cycle. If placed in the second, third, or last byte **420**, when the microloop instruction is executed, it will test the LOOP COUNT for zero. If zero, execution will continue with the next instruction. If not zero, the LOOP COUNTER **92** is decremented and the 2-bit microinstruction counter is cleared, causing the preceding instructions in the instruction register to be executed again.

Microloop is useful for block move and search operations. By executing a block move completely out of the instruction register **108**, the speed of the move is doubled, since all memory cycles are used by the move rather than being shared with instruction fetching. Such a hardware implementation of microloops is much faster than conventional software implementation of a comparable function.

OPTIMAL CPU CLOCK SCHEME

The designer of a high speed microprocessor must produce a product which operate over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing. Temperature, voltage, and process all affect transistor propagation delays. Traditional CPU designs are done so that with the worse case of the three parameters, the circuit will function at the rated clock speed. The result are designs that must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse case conditions.

The microprocessor **50** uses the technique shown in FIGS. **17–19** to generate the system clock and its required phases. Clock circuit **430** is the familiar "ring oscillator" used to test process performance. The clock is fabricated on the same silicon chip as the rest of the microprocessor **50**.

The ring oscillator frequency is determined by the parameters of temperature, voltage, and process. At room temperature, the frequency will be in the neighborhood of 100 MHZ. At 70 degrees Centigrade, the speed will be 50 MHZ. The ring oscillator **430** is useful as a system clock, with its stages **431** producing phase 0-phase 3 outputs **433** shown in FIG. **19**, because its performance tracks the parameters which similarly affect all other transistors on the same silicon die. By deriving system timing from the ring

oscillator **430**, CPU **70** will always execute at the maximum frequency possible, but never too fast. For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor **50** will operate slower than normal. Since the microprocessor **50** ring oscillator clock **430** is made from the same transistors on the same die as the latches and gates, it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.

ASYNCHRONOUS/SYNCHRONOUS CPU

Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor **50** provides a dual-clock scheme as shown in FIG. **17**, with the CPU **70** operating a synchronously to I/O interface **432** forming part of memory controller **118** (FIG. **2**) and the I/O interface **432** operating synchronously with the external world of memory and I/O devices. The CPU **70** executes at the fastest speed possible using the adaptive ring counter clock **430**. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor **50** for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface **432**, speed of which is controlled by a conventional crystal clock **434**. The interface **432** processes requests for memory accesses from the microprocessor **50** and acknowledges the presence of I/O data. The microprocessor **50** fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. By decoupling the variable speed of the CPU **70** from the fixed speed of the I/O interface **432**, optimum performance can be achieved by each. Recoupling between the CPU **70** and the interface **432** is accomplished with handshake signals on lines **436**, with data/addresses passing on bus **90**, **136**.

ASYNCHRONOUS/SYNCHRONOUS CPU IMBEDDED ON A DRAM CHIP

System performance is enhanced even more when the DRAM **311** and CPU **314** (FIG. **9**) are located on the same die. The proximity of the transistors means that DRAM **311** and CPU **314** parameters will closely follow each other. At room temperature, not only would the CPU **314** execute at 100 MHZ, but the DRAM **311** would access fast enough to keep up. The synchronization performed by the I/O interface **432** would be for DMA and reading and writing I/O ports. In some systems (such as calculators) no I/O synchronization at all would be required, and the I/O clock would be tied to the ring counter clock.

VARIABLE WIDTH OPERANDS

Many microprocessors provide variable width operands. The microprocessor **50** handles operands of 8, 16, or 24 bits using the same op-code. FIG. **20** shows the 32-bit instruction register **108** and the 2-bit microinstruction register **180** which selects the 8-bit instruction. Two classes of microprocessor **50** instructions can be greater than 8-bits, JUMP class and IMMEDIATE. A JUMP or IMMEDIATE op-code is 8-bits, but the operand can be 8, 16, or 24 bits long. This magic is possible because operands must be right justified in the instruction register. This means that the least significant bit of the operand is always located in the least significant bit of the instruction register. The microinstruction counter **180** selects which 8-bit instruction to execute. If a JUMP or IMMEDIATE instruction is decoded, the state of the 2-bit microinstruction counter selects the required 8, 16, or 24 bit operand onto the address or data bus. The unselected 8-bit bytes are loaded with zeros by operation of decoder **440** and gates **442**. The advantage of this technique is the saving of a number of op-codes required to specify the different operand sizes in other microprocessors.

TRIPLE STACK CACHE

Computer performance is directly related to the system memory bandwidth. The faster the memories, the faster the computer. Fast memories are expensive, so techniques have been developed to move a small amount of high-speed memory around to the memory addresses where it is needed. A large amount of slow memory is constantly updated by the fast memory, giving the appearance of a large fast memory array. A common implementation of the technique is known as a high-speed memory cache. The cache may be thought of as fast acting shock absorber smoothing out the bumps in memory access. When more memory is required than the shock can absorb, it bottoms out and slow speed memory is accessed. Most memory operations can be handled by the shock absorber itself.

The microprocessor **50** architecture has the ALU **80** (FIG. **2**) directly coupled to the top two stack locations **76** and **78**. The access time of the stack **74** therefore directly affects the execution speed of the processor. The microprocessor **50** stack architecture is particularly suitable to a triple cache technique, shown in FIG. **21** which offers the appearance of a large stack memory operating at the speed of on-chip latches **450**. Latches **450** are the fastest form of memory device built on the chip, delivering data in as little as 3 nsec. However latches **450** require large numbers of transistors to construct. On-chip RAM **452** requires fewer transistors than latches, but is slower by a factor of five (15 nsec access). Off-chip RAM **150** is the slowest storage of all. The microprocessor **50** organizes the stack memory hierarchy as three interconnected stacks **450**, **452** and **454**. The latch stack **450** is the fastest and most frequently used. The on-chip RAM stack **452** is next. The off-chip RAM stack **454** is slowest. The stack modulation determines the effective access time of the stack. If a group of stack operations never push or pull more than four consecutive items on the stack, operations will be entirely performed in the 3 nsec latch stack. When the four latches **456** are filled, the data in the bottom of the latch stack **450** is written to the top of the on-chip RAM stack **452**. When the sixteen locations **458** in the on-chip RAM stack **452** are filled, the data in the bottom of the on-chip RAM stack **452** is written to the top of the off-chip RAM stack **454**. When popping data off a full stack **450**, four pops will be performed before stack empty line **460** from the latch stack pointer **462** transfers data from the on-chip RAM stack **452**. By waiting for the latch stack **450** to empty before performing the slower on-chip RAM access, the high effective speed of the latches **456** are made available to the processor. The same approach is employed with the on-chip RAM stack **452** and the off-chip RAM stack **454**.

POLYNOMIAL GENERATION INSTRUCTION

Polynomials are useful for error correction, encryption, data compression, and fractal generation. A polynomial is generated by a sequence of shift and exclusive OR operations. Special chips are provided for this purpose in the prior art.

The microprocessor **50** is able to generate polynomials at high speed without external hardware by slightly modifying how the ALU **80** works. As shown in FIG. **21**, a polynomial is generated by loading the "order" (also known as the feedback terms) into C Register **470**. The value thirty one (resulting in 32 iterations) is loaded into DOWN COUNTER **472**. A register **474** is loaded with zero. B register **476** is loaded with the starting polynomial value. When the POLY

instruction executes, C register **470** is exclusively ORed with A register **474** if the least significant bit of B register **476** is a one. Otherwise, the contents of the A register **474** passes through the ALU **80** unaltered. The combination of A and B is then shifted right (divided by 2) with shifters **478** and **480**. The operation automatically repeats the specified number of iterations, and the resulting polynomial is left in A register **474**.

FAST MULTIPLY

Most microprocessors offer a 16×16 or 32×32 bit multiply instruction. Multiply when performed sequentially takes one shift/add per bit, or 32 cycles for 32 bit data. The microprocessor **50** provides a high speed multiply which allows multiplication by small numbers using only a small number of cycles. FIG. **23** shows the logic used to implement the high speed algorithm. To perform a multiply, the size of the multiplier less one is placed in the DOWN COUNTER **472**. For a four bit multiplier, the number three would be stored in the DOWN COUNTER **472**. Zero is loaded into the A register **474**. The multiplier is written bit reversed into the B Register **476**. For example, a bit reversed five (binary 0101) would be written into B as 1010. The multiplicand is written into the C register **470**. Executing the FAST MULT instruction will leave the result in the A Register **474**, when the count has been completed. The fast multiply instruction is important because many applications scale one number by a much smaller number. The difference in speed between multiplying a 32×32 bit and a 32×4 bit is a factor of 8. If the least significant bit of the multiplier is a "ONE", the contents of the A register **474** and the C register **470** are added. If the least significant bit of the multiplier is a "ZERO", the contents of the A register are passed through the ALU **80** unaltered. The output of the ALU **80** is shifted left by shifter **482** in each iteration. The contents of the B register **476** are shifted right by the shifter **480** in each iteration.

INSTRUCTION EXECUTION PHILOSOPHY

The microprocessor **50** uses high speed D latches in most of the speed critical areas. Slower on-chip RAM is used as secondary storage.

The microprocessor **50** philosophy of instruction execution is to create a hierarchy of speed as follows:

Logic and D latch transfers	1 cycle	20 nsec
Math	2 cycles	40 nsec
Fetch/store on-chip RAM	2 cycles	40 nsec
Fetch/store in current RAS page	4 cycles	80 nsec
Fetch/store with RAS cycle	11 cycles	220 nsec

With a 50 MHZ clock, many operations can be performed in 20 nsec. and almost everything else in 40 nsec.

To maximize speed, certain techniques in processor design have been used. They include:

Eliminating arithmetic operations on addresses,

Fetching up to four instructions per memory cycle,

Pipelineless instruction decoding

Generating results before they are needed,

Use of three level stack caching.

PIPELINE PHILOSOPHY

Computer instructions are usually broken down into sequential pieces, for example: fetch, decode, register read, execute, and store. Each piece will require a single machine cycle. In most Reduced Instruction Set Computer (RISC) chips, instruction require from three to six cycles.

RISC instructions are very parallel. For example, each of 70 different instructions in the SPARC (SUN Computer's RISC chip) has five cycles. Using a technique called "pipelining", the different phases of consecutive instructions can be overlapped.

To understand pipelining, think of building five residential homes. Each home will require in sequence, a foundation, framing, plumbing and wiring, roofing, and interior finish. Assume that each activity takes one week. To build one house will take five weeks.

But what if you want to build an entire subdivision? You have only one of each work crew, but when the foundation men finish on the first house, you immediately start them on the second one, and so on. At the end of five weeks, the first home is complete, but you also have five foundations. If you have kept the framing, plumbing, roofing, and interior guys all busy, from five weeks on, a new house will be completed each week.

This is the way a RISC chip like SPARC appears to execute an instruction in a single machine cycle. In reality, a RISC chip is executing one fifth of five instructions each machine cycle. And if five instructions stay in sequence, an instruction will be completed each machine cycle.

The problems with a pipeline are keeping the pipe full with instructions. Each time an out of sequence instruction such as a BRANCH or CALL occurs, the pipe must be refilled with the next sequence. The resulting dead time to refill the pipeline can become substantial when many IF/THEN/ELSE statements or subroutines are encountered.

THE PIPELINE APPROACH

The microprocessor **50** has no pipeline as such. The approach of this microprocessor to speed is to overlap instruction fetching with execution of the previously fetched instruction(s). Beyond that, over half the instructions (the most common ones) execute entirely in a single machine cycle of 20 nsec. This is possible because:

1. Instruction decoding resolves in 2.5 nsec.
2. Incremented/decremented and some math values are calculated before they are needed, requiring only a latching signal to execute.
3. Slower memory is hidden from high speed operations by high-speed D latches which access in 4 nsec.

The disadvantage for this microprocessor is a more complex chip design process. The advantage for the chip user is faster ultimate throughput since pipeline stalls cannot exist. Pipeline synchronization with availability flag bits and other such pipeline handling is not required by this microprocessor.

For example, in some RISC machines an instruction which tests a status flag may have to wait for up to four cycles for the flag set by the previous instruction to be available to be tested. Hardware and software debugging is also somewhat easier because the user doesn't have to visualize five instructions simultaneously in the pipe.

OVERLAPPING INSTRUCTION FETCH/EXECUTE

The slowest procedure the microprocessor **50** performs is to access memory. Memory is accessed when data is read or written. Memory is also read when instructions are fetched. The microprocessor **50** is able to hide fetch of the next instruction behind the execution of the previously fetched instruction(s). The microprocessor **50** fetches instructions in 4-byte instruction groups. An instruction group may contain from one to four instructions. The amount of time required to execute the instruction group ranges from 4 cycles for simple instructions to 64 cycles for a multiply.

When a new instruction group is fetched, the microprocessor instruction decoder looks at the most significant bit of all four of the bytes. The most significant bit of an instruction determines if a memory access is required. For example, CALL, FETCH, and STORE all require a memory access to

execute. If all four bytes have nonzero most significant bits, the microprocessor initiates the memory fetch of the next sequential 4-byte instruction group. When the last instruction in the group finishes executing, the next 4-byte instruction group is ready and waiting on the data bus needing only to be latched into the instruction register. If the 4-byte instruction group required four or more cycles to execute and the next sequential access was a column address strobe (CAS) cycle, the instruction fetch was completely overlapped with execution.

INTERNAL ARCHITECTURE

The microprocessor **50** architecture consists of the following:

PARAMETER STACK	<---> ALU* <--->	Y REGISTER RETURN STACK
<---32 BITS---> 16 DEEP Used for math and logic.		<---32 BITS---> 16 DEEP Used for subroutine and interrupt return addresses as well as local variables.
Push down stack. Can overflow into off-chip RAM.		Push down stack. Can overflow into off-chip RAM. Can also be accessed relative to top of stack.

LOOP COUNTER (32-bits, can decrement by 1) Used by class of test and loop instructions.

X REGISTER (32-bits, can increment or decrement by 4). Used to point to RAM locations.

PROGRAM COUNTER (32-bits, increments by 4). Points to 4-byte instruction groups in RAM.

INSTRUCTION REG (32-Bits). Holds 4-byte instruction groups while they are being decoded and executed.

MODE - A register with mode and status bits.

MODE-BITS:

- Slow down memory accesses by 8 if "1". Run full speed if "0". (Provided for access to slow EPROM.)
- Divide the system clock by 1023 if "1" to reduce power consumption. Run full speed if "0". (On-chip counters slow down if this bit is set.)
- Enable external interrupt 1.
- Enable external interrupt 2.
- Enable external interrupt 3.
- Enable external interrupt 4.
- Enable external interrupt 5.
- Enable external interrupt 6.
- Enable external interrupt 7.

ON-CHIP MEMORY LOCATIONS:

MODE-BITS	
DMA-POINTER	
DMA-COUNTER	
STACK-POINTER	- Pointer into Parameter Stack.
STACK-DEPTH	- Depth of on-chip Parameter Stack
RSTACK-POINTER	- Pointer into Return Stack
RSTACK-DEPTH	- Depth of on-chip Return Stack

*Math and logic operations use the TOP item and NEXT to top Parameter Stack items as the operands. The result is pushed onto the Parameter Stack. *Return addresses from subroutines are placed on the Return Stack. The Y REGISTER is used as a pointer to RAM locations. Since the Y REGISTER is the top item of the Return Stack, nesting of indices is straightforward.

ADDRESSING MODE HIGH POINTS

The data bus is 32-bits wide. All memory fetches and stores are 32-bits. Memory bus addresses are 30 bits. The least significant 2 bits are used to select one-of-four bytes in some addressing modes. The Program Counter, X Register, and Y Register are implemented as D latches with their outputs going to the memory address bus and the bus incrementer/decrementer. Incrementing one of these registers can happen quickly, because the incremented value has already rippled through the inc/dec logic and need only be clocked into the latch. Branches and Calls are made to 32-bit word boundaries.

INSTRUCTION SET

32-BIT INSTRUCTION FORMAT

The thirty two bit instructions are CALL, BRANCH, BRANCH-IF-ZERO, and LOOP-IF-NOT-DONE. These instructions require the calculation of an effective address. In many computers, the effective address is calculated by adding or subtracting an operand with the current Program Counter. This math operation requires from four to seven machine cycles to perform and can definitely bog down machine execution. The microprocessor's strategy is to perform the required math operation at assembly or linking time and do a much simpler "Increment to next page" or "Decrement to previous page" operation at run time. As a result, the microprocessor branches execute in a single cycle.

24-BIT OPERAND FORM:

Byte 1	Byte 2	Byte 3	Byte 4
WWWWWW XX -	YYYYYYYY -	YYYYYYYY -	YYYYYYYY

With a 24-bit operand, the current page is considered to be defined by the most significant 6 bits of the Program Counter.

16-BIT OPERAND FORM: QQQQQQQQ-WWWWWW XX-YYYYYYYY-YYYYYYYY With a 16-bit operand, the current page is considered to be defined by the most significant 14 bits of the Program Counter.

8-BIT OPERAND FORM: QQQQQQQQ-QQQQQQQQ-WWWWWW XX-YYYYYYYY With an 8-bit operand, the current page is considered to be defined by the most significant 22 bits of the Program Counter.

QQQQQQQQ—Any 8-bit instruction.

WWWWWW—Instruction op-code.

XX—Select how the address bits will be used:

00—Make all high-order bits zero. (Page zero addressing)

01—Increment the high-order bits. (Use next page)

10—Decrement the high-order bits. (Use previous page)

11—Leave the high-order bits unchanged. (Use current page)

YYYYYYYY—The address operand field. This field is always shifted left two bits (to generate a word rather than byte address) and loaded into the Program Counter. The microprocessor instruction decoder figures out the width of the operand field by the location of the instruction op-code in the four bytes.

The compiler or assembler will normally use the shortest operand required to reach the desired address so that the leading bytes can be used to hold other instructions. The effective address is calculated by combining:

The current Program Counter,

The 8, 16, or 24 bit address operand in the instruction, Using one of the four allowed addressing modes.

EXAMPLES OF EFFECTIVE ADDRESS CALCULATION

Example 1

Byte 1	Byte 2	Byte 3	Byte 4
QQQQQQQQ	QQQQQQQQ	00000011	10011000

The "QQQQQQQQs" in Byte 1 and 2 indicate space in the 4-byte memory fetch which could be hold two other

instructions to be executed prior to the CALL instruction. Byte 3 indicates a CALL instruction (six zeros) in the current page (indicated by the 11 bits). Byte 4 indicates that the hexadecimal number **98** will be forced into the Program Counter bits **2** through **10**. (Remember, a CALL or BRANCH always goes to a word boundary so the two least significant bits are always set to zero). The effect of this instruction would be to CALL a subroutine at WORD location HEX 98 in the current page. The most significant 22 bits of the Program Counter define the current page and will be unchanged.

Example 2

Byte 1	Byte 2	Byte 3	Byte 4
000001 01	00000001	00000000	00000000

If we assume that the Program Counter was HEX 0000 0156 which is binary:

00000000 00000000 00000001 01010110=OLD PROGRAM COUNTER.

Byte 1 indicates a BRANCH instruction op code (000001) and "01" indicates select the next page. Byte 2,3, and 4 are the address operand. These 24-bits will be shifted to the left two places to define a WORD address. HEX 0156 shifted left two places is HEX 0558. Since this is a 24-bit operand instruction, the most significant 6 bits of the Program Counter define the current page. These six bits will be incremented to select the next page. Executing this instruction will cause the Program Counter to be loaded with HEX 0400 0558 which is binary:

00000100 00000000 00000101 01011000=NEW PROGRAM COUNTER.

INSTRUCTIONS

CALL-LONG

0000 00XX-YYYYYYYY-YYYYYYYY-YYYYYYYY

Load the Program Counter with the effective WORD address specified. Push the current PC contents onto the RETURN STACK.

OTHER EFFECTS: CARRY or modes, no effect. May cause Return Stack to force an external memory cycle if on-chip Return Stack is full.

BRANCH

0000 01XX-YYYYYYYY-YYYYYYYY-YYYYYYYY

Load the Program Counter with the effective WORD address specified.

OTHER EFFECTS: NONE

BRANCH-IF-ZERO

0000 10XX-YYYYYYYY-YYYYYYYY-YYYYYYYY

Test the TOP value on the Parameter Stack. If the value is equal to zero, load the Program Counter with the effective WORD address specified. If the TOP value is not equal to zero, increment the Program Counter and fetch and execute the next instruction.

OTHER EFFECTS: NONE

LOOP-IF-NOT-DONE

0000 11YY-(XXXX XXXX)-(XXXX XXXX)-(XXXX XXXX)

If the LOOP COUNTER is not zero, load the Program Counter with the effective WORD address specified. If the LOOP COUNTER is zero, decrement the LOOP COUNTER, increment the Program Counter and fetch and execute the next instruction.

OTHER EFFECTS: NONE

8-BIT INSTRUCTIONS PHILOSOPHY

Most of the work in the microprocessor **50** is done by the 8-bit instructions. Eight bit instructions are possible with the microprocessor because of the extensive use of implied stack addressing. Many 32-bit architectures use 8-bits to specify the operation to perform but use an additional 24-bits to specify two sources and a destination.

For math and logic operations, the microprocessor **50** exploits the inherent advantage of a stack by designating the source operand(s) as the top stack item and the next stack item. The math or logic operation is performed, the operands are popped from the stack, and the result is pushed back on the stack. The result is a very efficient utilization of instruction bits as well as registers. A comparable situation exists between Hewlett Packard calculators (which use a stack) and Texas Instrument calculators which don't. The identical operation on an HP will require one half to one third the keystrokes of the TI.

The availability of 8-bit instructions also allows another architectural innovation, the fetching of four instructions in a single 32-bit memory cycle. The advantages of fetching multiple instructions are:

Increased execution speed even with slow memories,

Similar performance to the Harvard (separate data and instruction busses) without the expense,

Opportunities to optimize groups of instructions,

The capability to perform loops within this mini-cache.

The microloops inside the four instruction group are effective for searches and block moves.

SKIP INSTRUCTIONS

The microprocessor **50** fetches instructions in 32-bit chunks called 4-byte instruction groups. These four bytes may contain four 8-bit instructions or some mix of 8-bit and 16 or 24-bit instructions. SKIP instructions in the microprocessor skip any remaining instructions in a 4-byte instruction group and cause a memory fetch to get the next 4-byte instruction group. Conditional SKIPs when combined with 3-byte BRANCHES will create conditional BRANCHES. SKIPs may also be used in situations when no use can be made of the remaining bytes in a 4-instruction group. A SKIP executes in a single cycle, whereas a group of three NOPs would take three cycles.

SKIP-ALWAYS—Skip any remaining instructions in this 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group.

SKIP-IF-ZERO—If the TOP item of the Parameter Stack is zero, skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is not zero, execute the next sequential instruction.

SKIP-IF-POSITIVE—If the TOP item of the Parameter Stack has a the most significant bit (the sign bit) equal to "0", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is not "0", execute the next sequential instruction.

SKIP-IF-NO-CARRY—If the CARRY flag from a SHIFT or arithmetic operation is not equal to "1", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the CARRY is equal to "1", execute the next sequential instruction.

SKIP-NEVER (NOP) execute the next sequential instruction. (Delay one machine cycle).

SKIP-IF-NOT-ZERO—If the TOP item on the Parameter Stack is not equal to "0", skip any remaining instructions

in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is equal "0", execute the next sequential instruction.

SKIP-IF-NEGATIVE—If the TOP item on the Parameter Stack has its most significant bit (sign bit) set to "1", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item has its most significant bit set to "0", execute the next sequential instruction.

SKIP-IF-CARRY—If the CARRY flag is set to "1" as a result of SHIFT or arithmetic operation, skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the CARRY flag is "0", execute the next sequential instruction.

MICROLOOPS

Microloops are a unique feature of the microprocessor architecture which allows controlled looping within a 4-byte instruction group. A microloop instruction tests the LOOP COUNTER for "0" and may perform an additional test. If the LOOP COUNTER is not "0" and the test is met, instruction execution continues with the first instruction in the 4-byte instruction group, and the LOOP COUNTER is decremented. A microloop instruction will usually be the last byte in a 4-byte instruction group, but it can be any byte. If the LOOP COUNTER is "0" or the test is not met, instruction execution continues with the next instruction. If the microloop is the last byte in the 4-byte instruction group, the most significant 30-bits of the Program Counter are incremented and the next 4-byte instruction group is fetched from memory. On a termination of the loop on LOOP COUNTER equal to "0", the LOOP COUNTER will remain at "0". Microloops allow short iterative work such as moves and searches to be performed without slowing down to fetch instructions from memory.

EXAMPLE

Byte 1 FETCH-VIA-X-AUTO-INCREMENT	Byte 2 STORE-VIA-Y-AUTOINCREMENT
Byte 3 ULOOP-UNTIL-DONE	Byte 4 QQQQQQQQ

This example will perform a block move. To initiate the transfer, X will be loaded with the starting address of the source. Y will be loaded with the starting address of the destination. The LOOP COUNTER will be loaded with the number of 32-bit words to move. The microloop will FETCH and STORE and count down the LOOP COUNTER until it reaches zero. QQQQQQQQ indicates any instruction can follow.

MICROLOOP INSTRUCTIONS

ULOOP-UNTIL-DONE—If the LOOP COUNTER is not "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0", continue execution with the next instruction.

ULOOP-IF-ZERO—If the LOOP COUNTER is not "0" and the TOP item on the Parameter Stack is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

ULOOP-IF-POSITIVE—If the LOOP COUNTER is not "0" and the most significant bit (sign bit) is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

ULOOP-IF-NOT-CARRY-CLEAR—If the LOOP COUNTER is not "0" and the floating point exponents found in TOP and NEXT are not aligned, continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the exponents are aligned, continue execution with the next instruction. This instruction is specifically designed for combination with special SHIFT instructions to align two floating point numbers.

ULOOP-NEVER—(DECREMENT-LOOP-COUNTER) Decrement the LOOP COUNTER. Continue execution with the next instruction.

ULOOP-IF-NOT-ZERO—If the LOOP COUNTER is not "0" and the TOP item of the Parameter Stack is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

ULOOP-IF-NEGATIVE—If the LOOP COUNTER is not "0" and the most significant bit (sign bit) of the TOP item of the Parameter Stack is "1", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the most significant bit of the Parameter Stack is "0", continue execution with the next instruction.

ULOOP-IF-CARRY-SET—If the LOOP COUNTER is not "0" and the exponents of the floating point numbers found in TOP and NEXT are not aligned, continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the exponents are aligned, continue execution with the next instruction.

RETURN FROM SUBROUTINE OR INTERRUPT

Subroutine calls and interrupt acknowledgements cause a redirection of normal program execution. In both cases, the current Program Counter is pushed onto the Return Stack, so the microprocessor can return to its place in the program after executing the subroutine or interrupt service routine.

NOTE: When a CALL to subroutine or interrupt is acknowledged the Program Counter has already been incremented and is pointing to the 4-byte instruction group following the 4-byte group currently being executed. The instruction decoding logic allows the microprocessor to perform a test and execute a return conditional on the outcome of the test in a single cycle. A RETURN pops an address from the Return Stack and stores it to the Program Counter.

RETURN INSTRUCTIONS

RETURN-ALWAYS—Pop the top item from the Return Stack and transfer it to the Program Counter.

RETURN-IF-ZERO—If the TOP item on the Parameter Stack is "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-POSITIVE—If the most significant bit (sign bit) of the TOP item on the Parameter Stack is a "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-CARRY-CLEAR—If the exponents of the floating point numbers found in TOP and NEXT are not aligned, pop the top item from the Return Stack and

transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-NEVER (NOP)—Execute the next instruction.

RETURN-IF-NOT-ZERO—If the TOP item on the Parameter Stack is not "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-NEGATIVE—If the most significant bit (sign bit) of the TOP item on the Parameter Stack is a "1", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-CARRY-SET—If the exponents of the floating point numbers found in TOP and NEXT are aligned, pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

HANDLING MEMORY FROM DYNAMIC RAM

The microprocessor **50**, like any RISC type architecture, is optimized to handle as many operations as possible on-chip for maximum speed. External memory operations take from 80 nsec. to 220 nsec. compared with on-chip memory speeds of from 4 nsec. to 30 nsec. There are times when external memory must be accessed.

External memory is accessed using three registers:

X-REGISTER—A 30-bit memory pointer which can be used for memory access and simultaneously incremented or decremented.

Y-REGISTER—A 30-bit memory pointer which can be used for memory access and simultaneously incremented or decremented.

PROGRAM-COUNTER—A 30-bit memory pointer normally used to point to 4-byte instruction groups. External memory may be accessed at addresses relative to the PC. The operands are sometimes called "Immediate" or "Literal" in other computers. When used as memory pointer, the PC is also incremented after each operation.

MEMORY LOAD & STORE INSTRUCTIONS

FETCH-VIA-X—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. X is unchanged.

FETCH-VIA-Y—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. Y is unchanged.

FETCH-VIA-X-AUTOINCREMENT—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of X to point to the next 32-bit word address.

FETCH-VIA-Y-AUTOINCREMENT—Fetch the 32-bit memory content pointed to by Y and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of Y to point to the next 32-bit word address.

FETCH-VIA-X-AUTODECREMENT—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. After fetching, decrement the most significant 30 bits of X to point to the previous 32-bit word address.

FETCH-VIA-Y-AUTODECREMENT—Fetch the 32-bit memory content pointed to by Y and push it onto the Parameter Stack. After fetching, decrement the most significant 30 bits of Y to point to the previous 32-bit word address.

STORE-VIA-X—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. X is unchanged.

STORE-VIA-Y—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. Y is unchanged.

STORE-VIA-X-AUTOINCREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. After storing, increment the most significant 30 bits of X to point to the next 32-bit word address.

STORE-VIA-Y-AUTOINCREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. After storing, increment the most significant 30 bits of Y to point to the next 32-bit word address.

STORE-VIA-X-AUTODECREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. After storing, decrement the most significant 30 bits of X to point to the previous 32-bit word address.

STORE-VIA-Y-AUTODECREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. After storing, decrement the most significant 30 bits of Y to point to the previous 32-bit word address.

FETCH-VIA-PC—Fetch the 32-bit memory content pointed to by the Program Counter and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of the Program Counter to point to the next 32-bit word address.

*NOTE When this instruction executes, the PC is pointing to the memory location following the instruction. The effect is of loading a 32-bit immediate operand. This is an 8-bit instruction and therefore will be combined with other 8-bit instructions in a 4-byte instruction fetch. It is possible to have from one to four FETCH-VIA-PC instructions in a 4-byte instruction fetch. The PC increments after each execution of FETCH-VIA-PC, so it is possible to push four immediate operands on the stack. The four operands would be the found in the four memory locations following the instruction.

BYTE-FETCH-VIA-X—Fetch the 32-bit memory content pointed to by the most significant 30 bits of X. Using the two least significant bits of X, select one of four bytes from the 32-bit memory fetch, right justify the byte in a 32-bit field and push the selected byte preceded by leading zeros onto the Parameter Stack.

BYTE-STORE-VIA-X—Fetch the 32-bit memory content pointed to by the most significant 30 bits of X. Pop the TOP item from the Parameter Stack. Using the two least significant bits of X place the least significant byte into the 32-bit memory data and write the 32-bit entity back to the location pointed to by the most significant 30 bits of X.

OTHER EFFECTS OF MEMORY ACCESS INSTRUCTIONS:

Any FETCH instruction will push a value on the Parameter Stack **74**. If the on-chip stack is full, the stack will overflow into off-chip memory stack resulting in an additional memory cycle. Any STORE instruction will pop a value from the Parameter Stack **74**. If the on-chip stack is empty, a memory cycle will be generated to fetch a value from off-chip memory stack.

HANDLING ON-CHIP VARIABLES

High-level languages often allow the creation of LOCAL VARIABLES. These variables are used by a particular procedure and discarded. In cases of nested procedures, layers of these variables must be maintained. On-chip storage is up to five times faster than off-chip RAM, so a means of keeping local variables on-chip can make operations run faster. The microprocessor **50** provides the capability for both on-chip storage of local variables and nesting of multiple levels of variables through the Return Stack.

The Return Stack **134** is implemented as 16 on-chip RAM locations. The most common use for the Return Stack **134** is storage of return addresses from subroutines and interrupt calls. The microprocessor allows these 16 locations to also be used as addressable registers. The 16 locations may be read and written by two instructions which indicate a Return Stack relative address from 0–15. When high-level procedures are nested, the current procedure variables push the previous procedure variables further down the Return Stack **134**. Eventually, the Return Stack will automatically overflow into off-chip RAM.

ON-CHIP VARIABLE INSTRUCTIONS

READ-LOCAL-VARIABLE XXXX—Read the XXXXth location relative to the top of the Return Stack. (XXXX is a binary number from 0000–1111). Push the item read onto the Parameter Stack.

OTHER EFFECTS: If the Parameter Stack is full, the push operation will cause a memory cycle to be generated as one item of the stack is automatically stored to external RAM. The logic which selects the location performs a modulo **16** subtraction. If four local variables have been pushed onto the Return Stack, and an instruction attempts to READ the fifth item, unknown data will be returned.

WRITE-LOCAL-VARIABLE XXXX—Pop the TOP item of the Parameter Stack and write it into the XXXXth location relative to the top of the Return Stack. (XXXX is a binary number from 0000–1111.)

OTHER EFFECTS: If the Parameter Stack is empty, the pop operation will cause a memory cycle to be generated to fetch the Parameter Stack item from external RAM. The logic which selects the location performs a modulo **16** subtraction. If four local variables have been pushed onto the Return Stack, and an instruction attempts to WRITE to the fifth item, it is possible to clobber return addresses or wreak other havoc.

REGISTER AND FLIP-FLOP TRANSFER AND PUSH INSTRUCTIONS

DROP—Pop the TOP item from the Parameter Stack and discard it.

SWAP—Exchange the data in the TOP Parameter Stack location with the data in the NEXT Parameter Stack location.

DUP—Duplicate the TOP item on the Parameter Stack and push it onto the Parameter Stack.

PUSH-LOOP-COUNTER—Push the value in LOOP COUNTER onto the Parameter Stack.

POP-RSTACK-PUSH-TO-STACK—Pop the top item from the Return Stack and push it onto the Parameter Stack.

PUSH-X-REG—Push the value in the X Register onto the Parameter Stack.

PUSH-STACK-POINTER—Push the value of the Parameter Stack pointer onto the Parameter Stack.

PUSH-RSTACK-POINTER—Push the value of the Return Stack pointer onto the Return Stack.

PUSH-MODE-BITS—Push the value of the MODE REGISTER onto the Parameter Stack.

PUSH-INPUT—Read the 10 dedicated input bits and push the value (right justified and padded with leading zeros) onto the Parameter Stack.

SET-LOOP-COUNTER—Pop the TOP value from the Parameter Stack and store it into LOOP COUNTER.

POP-STACK-PUSH-TO-RSTACK—Pop the TOP item from the Parameter Stack and push it onto the Return Stack.

SET-X-REG—Pop the TOP item from the Parameter Stack and store it into the X Register.

SET-STACK-POINTER—Pop the TOP item from the Parameter Stack and store it into the Stack Pointer.

SET-RSTACK-POINTER—Pop the TOP item from the Parameter

Stack and store it into the Return Stack Pointer.

SET-MODE-BITS—Pop the TOP value from the Parameter Stack and store it into the MODE BITS.

SET-OUTPUT—Pop the TOP item from the Parameter Stack and output it to the 10 dedicated output bits.

OTHER EFFECTS: Instructions which push or pop the Parameter Stack or Return Stack may cause a memory cycle as the stacks overflow back and forth between on-chip and off-chip memory.

LOADING A SHORT LITERAL

A special case of register transfer instruction is used to push an 8-bit literal onto the Parameter Stack. This instruction requires that the 8-bits to be pushed reside in the last byte of a 4-byte instruction group. The instruction op-code loading the literal may reside in ANY of the other three bytes in the instruction group.

EXAMPLE

BYTE 1 LOAD-SHORT-LITERAL BYTE 4 00001111	BYTE 2 QQQQQQQQ	BYTE 3 QQQQQQQQ

In this example, QQQQQQQQ indicates any other 8-bit instruction. When Byte 1 is executed, binary 00001111(HEX 0f) from Byte 4 will be pushed (right justified and padded by leading zeros) onto the Parameter Stack. Then the instructions in Byte 2 and Byte 3 will execute. The microprocessor instruction decoder knows not to execute Byte 4. It is possible to push three identical 8-bit values as follows:

BYTE 1 LOAD-SHORT-LITERAL BYTE 3 LOAD-SHORT-LITERAL SHORT-LITERAL-INSTRUCTION	BYTE 2 LOAD-SHORT-LITERAL BYTE 4 00001111

LOAD-SHORT-LITERAL—Push the 8-bit value found in Byte 4 of the current 4-byte instruction group onto the Parameter Stack.

LOGIC INSTRUCTIONS

Logical and math operations used the stack for the source of one or two operands and as the destination for results. The stack organization is a particularly convenient arrangement for evaluating expressions. TOP indicates the top value on the Parameter Stack **74**. NEXT indicates the next to top value on the Parameter Stack **74**.

AND—Pop TOP and NEXT from the Parameter Stack, perform the logical AND operation on these two operands, and push the result onto the Parameter Stack.

OR—Pop TOP and NEXT from the Parameter Stack, perform the logical OR operation on these two operands, and push the result onto the Parameter Stack.

XOR—Pop TOP and NEXT from the Parameter Stack, perform the logical exclusive OR on these two operands, and push the result onto the Parameter Stack.

BIT-CLEAR—Pop TOP and NEXT from the Parameter Stack, toggle all bits in NEXT, perform the logical AND operation on TOP, and push the result onto the Parameter Stack. (Another way of understanding this instruction is thinking of it as clearing all bits in TOP that are set in NEXT.)

MATH INSTRUCTIONS

Math instruction pop the TOP item and NEXT to top item of the Parameter Stack **74** to use as the operands. The results are pushed back on the Parameter Stack. The CARRY flag is used to latch the "33rd bit" of the ALU result.

ADD—Pop the TOP item and NEXT to top item from the Parameter Stack, add the values together and push the result back on the Parameter Stack. The CARRY flag may be changed.

ADD-WITH-CARRY—Pop the TOP item and the NEXT to top item from the Parameter Stack, add the values together. If the CARRY flag is "1" increment the result. Push the ultimate result back on the Parameter Stack. The CARRY flag may be changed.

ADD-X—Pop the TOP item from the Parameter Stack and read the third item from the top of the Parameter Stack. Add the values together and push the result back on the Parameter Stack. The CARRY flag may be changed.

SUB—Pop the TOP item and NEXT to top item from the Parameter Stack, Subtract NEXT from TOP and push the result back on the Parameter Stack. The CARRY flag may be changed.

SUB-WITH-CARRY—Pop the TOP item and NEXT to top item from the Parameter Stack. Subtract NEXT from TOP. If the CARRY flag is "1" increment the result. Push the ultimate result back on the Parameter Stack. The CARRY flag may be changed.

SUB-X—

SIGNED-MULT-STEP—

UNSIGNED-MULT-STEP—

SIGNED-FAST-MULT—

FAST-MULT-STEP—

UNSIGNED-DIV-STEP—

GENERATE-POLYNOMIAL—

ROUND—

COMPARE—Pop the TOP item and NEXT to top item from the Parameter Stack. Subtract NEXT from TOP. If the result has the most significant bit equal to "0" (the result is positive), push the result onto the Parameter Stack. If the result has the most significant bit equal to "1" (the result is negative), push the old value of TOP onto the Parameter Stack. The CARRY flag may be affected.

SHIFT/ROTATE

SHIFT-LEFT—Shift the TOP Parameter Stack item left one bit. The CARRY flag is shifted into the least significant bit of TOP.

SHIFT-RIGHT—Shift the TOP Parameter Stack item right one bit. The least significant bit of TOP is shifted into the CARRY flag. Zero is shifted into the most significant bit of TOP.

DOUBLE-SHIFT-LEFT—Treating the TOP item of the Parameter Stack as the most significant word of a 64-bit number and the NEXT stack item as the least significant word, shift the combined 64-bit entity left one bit. The CARRY flag is shifted into the least significant bit of NEXT.

DOUBLE-SHIFT-RIGHT—Treating the TOP item of the Parameter Stack as the most significant word of a 64-bit number and the NEXT stack item as the least significant word, shift the combined 64-bit entity right one bit. The least significant bit of NEXT is shifted into the CARRY flag. Zero is shifted into the most significant bit of TOP.

OTHER INSTRUCTIONS

FLUSH-STACK—Empty all on-chip Parameter Stack locations into off-chip RAM. (This instruction is useful for multitasking applications). This instruction accesses a counter which holds the depth of the on-chip stack and can require from none to 16 external memory cycles.

FLUSH-RSTACK—Empty all on-chip Return Stack locations into off-chip RAM. (This instruction is useful for multitasking applications). This instruction accesses a counter which holds the depth of the on-chip Return Stack and can require from none to 16 external memory cycles.

It should further be apparent to those skilled in the art that various changes in form and details of the invention as shown and described may be made. It is intended that such changes be included within the spirit and scope of the claims appended hereto.

What is claimed is:

1. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.

2. The microprocessor system of claim **1** in which said second clock is a fixed frequency clock.

3. In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:

providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;

using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;

providing an on chip input/output interface for the microprocessor integrated circuit; and

clocking the input/output interface with a second clock independent of the ring oscillator system clock.

4. The method of claim **3** in which the second clock is a fixed frequency clock.

5. The method of claim **3** further including the step of:

transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.

6. A microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and

the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;

an on-chip input/output interface, connected between said said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

7. The microprocessor system of claim **6** wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

8. The microprocessor system of claim **6** wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.

9. The microprocessor system of claim **6** wherein said oscillator comprises a ring oscillator.

10. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

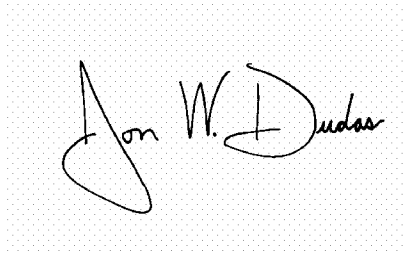
PATENT NO. : 5,809,336
APPLICATION NO. : 08/484918
DATED : September 15, 1998
INVENTOR(S) : Moore et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 34,
Line 25, delete "oscillator" and insert --variable speed clock--.

Signed and Sealed this

Twenty-second Day of May, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office

US005809336C1

(12) EX PARTE REEXAMINATION CERTIFICATE (7235th)

United States Patent

Moore et al.

(10) Number: US 5,809,336 C1

(45) Certificate Issued: Dec. 15, 2009

(54) **HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK**

(75) Inventors: **Charles H. Moore**, Woodside, CA (US); **Russell H. Fish, III**, Mt. View, CA (US)

(73) Assignee: **Patriot Scientific Corporation**, San Diego, CA (US)

Reexamination Request:
No. 90/008,306, Oct. 19, 2006
No. 90/008,237, Nov. 17, 2006
No. 90/008,474, Jan. 30, 2007

Reexamination Certificate for:

Patent No.:	**5,809,336**
Issued:	**Sep. 15, 1998**
Appl. No.:	**08/484,918**
Filed:	**Jun. 7, 1995**

Certificate of Correction issued May 22, 2007.

Related U.S. Application Data

(62) Division of application No. 07/389,334, filed on Aug. 3, 1989, now Pat. No. 5,440,749.

(51) **Int. Cl.**

G06F 7/76	(2006.01)
G06F 7/48	(2006.01)
G06F 12/08	(2006.01)
G06F 7/78	(2006.01)
G06F 9/30	(2006.01)
G06F 9/32	(2006.01)
G06F 15/76	(2006.01)
G06F 15/78	(2006.01)
G06F 7/52	(2006.01)
G06F 9/38	(2006.01)
G06F 7/58	(2006.01)

(52) **U.S. Cl.** **710/25**; 711/E12.02; 712/E9.016; 712/E9.028; 712/E9.046; 712/E9.055; 712/E9.057; 712/E9.058; 712/E9.062; 712/E9.078; 712/E9.08; 712/E9.081

(58) **Field of Classification Search** ..... None
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,603,934	A	9/1971	Heath, Jr. et al.
3,696,414	A	10/1972	Allen et al.
3,849,765	A	11/1974	Hamano
3,878,513	A	4/1975	Werner
3,919,695	A	11/1975	Gooding
3,924,245	A	12/1975	Eaton et al.

(Continued)

FOREIGN PATENT DOCUMENTS

EP	0 200 797 A1	11/1986
EP	0 208 287	1/1987
EP	113 516 B1	6/1988

(Continued)

OTHER PUBLICATIONS

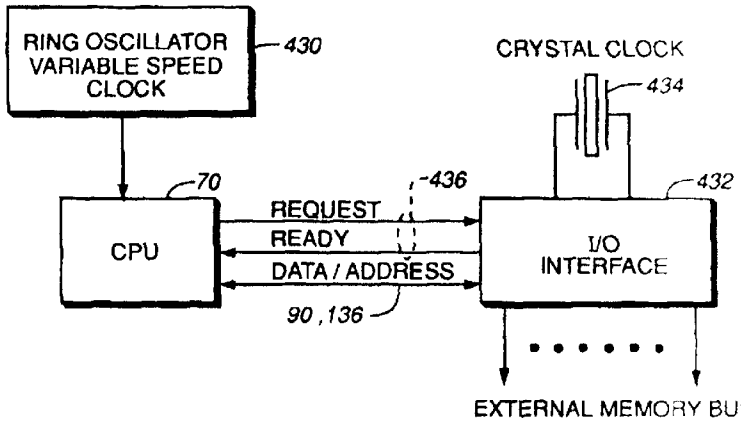
Memorandum Opinion and Order filed Jun. 15, 2007 in 2:05–CV–494 (TJW).
Plaintiffs Technology Property Limited's and Patriot Scientific Corporation's Claim Construction Brief filed Mar. 19, 2007 in 2:05–CV–494 (TJW).

(Continued)

Primary Examiner—Sam Rimell

(57) **ABSTRACT**

A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.



U.S. PATENT DOCUMENTS

3,967,104	A	6/1976	Brantingham et al.
3,968,501	A	7/1976	Gilbert
3,976,977	A	8/1976	Porter et al.
3,980,993	A	9/1976	Bredart et al.
4,003,028	A	1/1977	Bennett et al.
4,003,033	A	1/1977	O'Keefe et al.
4,037,090	A	7/1977	Raymond, Jr.
4,042,972	A	8/1977	Gruner et al.
4,050,058	A	9/1977	Garlic
4,050,096	A	9/1977	Bennett et al.
4,067,058	A	1/1978	Brandstaetter et al.
4,067,059	A	1/1978	Derchak
4,075,691	A	2/1978	Davis et al.
4,079,455	A	3/1978	Ozga
4,107,773	A	8/1978	Gilbreath et al.
4,110,822	A	8/1978	Porter et al.
4,112,490	A	9/1978	Pohlman et al.
4,125,871	A	11/1978	Martin
4,128,873	A	12/1978	Lamiaux
4,144,562	A	3/1979	Cooper
4,217,637	A	8/1980	Faulkner et al.
4,223,380	A	9/1980	Antonaccio et al.
4,223,880	A	9/1980	Brems
4,224,676	A	9/1980	Appelt
4,236,152	A	11/1980	Masuzawa et al.
4,242,735	A	12/1980	Sexton
4,253,785	A	3/1981	Bronstein
4,255,785	A	3/1981	Chamberlin
4,292,668	A	9/1981	Miller et al.
4,295,193	A	10/1981	Pomerene
4,305,045	A	12/1981	Metz et al.
4,315,305	A	2/1982	Siemon
4,315,308	A	2/1982	Jackson
4,317,227	A	2/1982	Skerlos
4,320,467	A	3/1982	Glass
4,321,706	A	3/1982	Craft
4,328,557	A	5/1982	Gastinel
4,334,268	A	6/1982	Boney et al.
4,335,447	A	6/1982	Jerrim
4,338,675	A	7/1982	Palmer et al.
4,348,720	A	9/1982	Blahut et al.
4,348,743	A	9/1982	Dozier
4,354,228	A	10/1982	Moore et al.
4,358,728	A	11/1982	Hashimoto
4,361,869	A	11/1982	Johnson et al.
4,364,112	A	12/1982	Onodera et al.
4,376,977	A	3/1983	Bruinshorst
4,382,279	A	5/1983	Ugon
4,390,946	A	6/1983	Lane
4,396,979	A	8/1983	Mor et al.
4,398,263	A	8/1983	Ito
4,398,265	A	8/1983	Puhl et al.
4,402,042	A	8/1983	Guttag
4,403,303	A	9/1983	Howes et al.
4,412,283	A	10/1983	Mor et al.
4,425,628	A	1/1984	Bedard et al.
4,449,201	A	5/1984	Clark
4,450,519	A	5/1984	Guttag et al.
4,462,073	A	7/1984	Grondalski
4,463,421	A	7/1984	Laws
4,467,810	A	8/1984	Vollmann
4,471,426	A	9/1984	McDonough
4,472,789	A	9/1984	Sibley
4,488,217	A	12/1984	Binder et al.
4,494,021	A	1/1985	Bell et al.
4,509,115	A	4/1985	Manton et al.
4,538,239	A	8/1985	Magar
4,539,655	A	9/1985	Trussell et al.
4,541,045	A	9/1985	Kromer, III
4,541,111	A	9/1985	Takashima et al.
4,553,201	A	11/1985	Pollack et al.
4,556,063	A	12/1985	Thompson et al.
4,562,537	A	12/1985	Barnett et al.
4,566,063	A	1/1986	Zolnowsky
4,577,282	A	3/1986	Caudel et al.
4,607,332	A	8/1986	Goldberg
4,616,338	A	10/1986	Helen et al.
4,626,798	A	12/1986	Fried
4,626,985	A	12/1986	Briggs
4,626,988	A	12/1986	George
4,627,082	A	12/1986	Pelgrom et al.
4,630,195	A	12/1986	Hester et al.
4,630,934	A	12/1986	Arber
4,641,246	A	2/1987	Halbert et al.
4,649,471	A	3/1987	Briggs et al.
4,660,155	A	4/1987	Thaden et al.
4,660,180	A	4/1987	Tanimura et al.
4,665,495	A	5/1987	Thaden
4,670,837	A	6/1987	Sheets
4,679,166	A	7/1987	Berger et al.
4,680,698	A	7/1987	Edwards et al.
4,689,581	A	8/1987	Talbot
4,691,124	A	9/1987	Ledzius et al.
4,698,750	A	10/1987	Wilkie et al.
4,701,884	A	10/1987	Aoki et al.
4,704,678	A	11/1987	May
4,708,490	A	11/1987	Arber
4,709,329	A	11/1987	Hecker
4,710,648	A	12/1987	Hanamura et al.
4,713,749	A	12/1987	Magar et al.
4,714,994	A	12/1987	Oklobdzija
4,720,812	A	1/1988	Kao et al.
4,724,517	A	2/1988	May
4,739,475	A	4/1988	Mensch, Jr.
4,750,111	A	6/1988	Crosby, Jr. et al.
4,758,948	A	7/1988	May et al.
4,760,521	A	7/1988	Rehwald et al.
4,761,763	A	8/1988	Hicks
4,763,297	A	8/1988	Uhlenhoff
4,766,567	A	8/1988	Kato
4,772,888	A	9/1988	Kimura
4,777,591	A	10/1988	Chang et al.
4,780,814	A	10/1988	Hayek
4,783,734	A	11/1988	May et al.
4,787,032	A	11/1988	Culley
4,794,526	A	12/1988	May et al.
4,797,850	A	1/1989	Amitai
4,803,621	A	2/1989	Kelly
4,805,091	A	2/1989	Thiel et al.
4,809,169	A	2/1989	Sfarti et al.
4,809,269	A	2/1989	Gulick
4,811,208	A	3/1989	Myers et al.
4,816,989	A	3/1989	Finn et al.
4,816,996	A	3/1989	Hill et al.
4,819,151	A	4/1989	May
4,833,599	A	5/1989	Colwell et al.
4,835,738	A	5/1989	Niehaus et al.
4,837,563	A	6/1989	Mansfield et al.
4,837,682	A	6/1989	Culler
4,853,841	A	8/1989	Richter
4,860,198	A	8/1989	Takenaka
4,868,735	A	9/1989	Moller et al.
4,870,562	A	9/1989	Kimoto et al.
4,872,003	A	10/1989	Yoshida
4,882,710	A	11/1989	Hashimoto et al.
4,890,225	A	12/1989	Ellis, Jr. et al.
4,899,275	A	2/1990	Sachs et al.
4,907,225	A	3/1990	Gulick et al.
4,910,703	A	3/1990	Ikeda et al.
4,912,632	A	3/1990	Gach et al.
4,914,578	A	4/1990	MacGregor et al.

4,926,323	A	5/1990	Baror et al.
4,931,748	A	6/1990	McDermott et al.
4,931,986	A	6/1990	Daniel et al.
4,933,835	A	6/1990	Sachs
4,942,553	A	7/1990	Dalrymple et al.
4,956,811	A	9/1990	Kajigaya et al.
4,959,782	A	9/1990	Tulpule et al.
4,967,326	A	10/1990	May
4,967,352	A	10/1990	Keida et al.
4,967,398	A	10/1990	Jamoua et al.
4,974,157	A	11/1990	Winfield et al.
4,979,102	A	12/1990	Tokuume
4,980,821	A	12/1990	Koopman et al.
4,988,892	A	1/1991	Needle
4,989,113	A	1/1991	Asal
4,989,133	A	1/1991	May et al.
4,989,135	A	1/1991	Miki
4,990,847	A	2/1991	Ishimaru et al.
5,008,816	A	4/1991	Fogg, Jr. et al.
5,013,985	A	5/1991	Itoh et al.
5,021,991	A	6/1991	MacGregor et al.
5,022,395	A	6/1991	Russie
5,023,689	A	6/1991	Sugawara
5,031,092	A	7/1991	Edwards et al.
5,036,300	A	7/1991	Nicolai
5,036,460	A	7/1991	Takahira et al.
5,047,921	A	9/1991	Kinter et al.
5,053,952	A	10/1991	Koopman, Jr. et al.
5,068,781	A	11/1991	Gillett, Jr. et al.
5,070,451	A	12/1991	Moore et al.
5,081,574	A	1/1992	Larsen et al.
5,091,846	A	2/1992	Sachs et al.
5,097,437	A	3/1992	Larson et al.
5,103,499	A	4/1992	Miner et al.
5,109,495	A	4/1992	Fite et al.
5,121,502	A	6/1992	Rau et al.
5,127,091	A	6/1992	Boufarah et al.
5,127,092	A	6/1992	Gupta et al.
5,134,701	A	7/1992	Mueller et al.
5,146,592	A	9/1992	Pfeiffer et al.
5,148,385	A	9/1992	Frazier
5,157,772	A	10/1992	Watanabe
5,179,689	A	1/1993	Leach et al.
5,179,734	A	1/1993	Candy et al.
5,226,147	A	7/1993	Fujishima et al.
5,237,699	A	8/1993	Little et al.
5,239,631	A	8/1993	Boury et al.
5,241,636	A	8/1993	Kohn
5,261,057	A	11/1993	Coyle et al.
5,261,082	A	11/1993	Ito et al.
5,261,109	A	11/1993	Cadambi et al.
5,325,513	A	6/1994	Tanaka et al.
5,339,448	A	8/1994	Tanaka et al.
5,353,417	A	10/1994	Fuoco et al.
5,353,427	A	10/1994	Fujishima et al.
5,379,438	A	1/1995	Bell et al.
5,410,654	A	4/1995	Foster et al.
5,410,682	A	4/1995	Sites et al.
5,414,862	A	5/1995	Suzuki et al.
5,421,000	A	5/1995	Fortino et al.
5,440,749	A	8/1995	Moore et al.
5,459,846	A	10/1995	Hyatt
5,511,209	A	4/1996	Mensch, Jr.
5,530,890	A	6/1996	Moore et al.
5,537,565	A	7/1996	Hyatt
5,604,915	A	2/1997	Moore et al.
5,659,703	A	8/1997	Moore et al.
5,784,584	A	7/1998	Moore et al.
6,598,148	B1	7/2003	Moore et al.

FOREIGN PATENT DOCUMENTS

EP	0288649	11/1988
JP	58-25710 A	2/1983
JP	61-127228 A	6/1984
JP	61-138356 A	6/1986
JP	62-145413	6/1987
JP	05-189383	7/1998

OTHER PUBLICATIONS

Defendants' Brief Regarding Construction of Disputed Claim Terms of the 336 and 148 Patents filed Apr. 2, 2007 in 2:05–CV–494 (TJW).

Defendants' Brief Regarding Construction of Disputed Claim Terms of the 584 Patent filed Apr. 2, 2007 in 2:05–CV–494 (TJW).

Plaintiffs' Claim Construction Reply Brief filed Apr. 9, 2007 in 2:05–CV–494 (TJW).

Defendants' Unopposed Motion for Leave to File a Sur–Reply Brief Regarding Claim Construction filed Apr. 19, 2007 in 2:05–CV–494 (TJW).

Defendants' Sur–Reply Brief Regarding Construction of Disputed Claim Terms of the 336 Patent filed Apr. 29, 2007 in 2:05–CV–494 (TJW).

Declaration of Roger L. Cook in Support of Plaintiffs Technology Property Limited's and Patriot Scientific Corporations's Claim Construction Brief filed Mar. 19, 2007 in 2:05–CV–00494 (TJW).

Supplemental Declaration of Roger L. Cook in Support of Plaintiffs Technology Property Limited's and Patriot Scientific Corporations's Claim Construction Brief filed Apr. 9, 2007 in 2:05–CV–00494 (TJW).

Declaration of David J. Lender filed Apr. 2, 2007 in 2:05–CV–00494 (TJW).

Supplemental Declaration of Alvin M. Despain in Support of Plaintiffs' Reply Claim Construction Brief filed Apr. 9, 2007 in 2:05–CV–0049 (TJW).

Declaration of Alvin M. Despain in Support of Plaintiffs' Claim Construction Brief filed Mar. 19, 2007 in 2:05–CV–00494 (TJW).

Nakamura et al., "Microprocessors—Special Purpose," 1987 lEEE lnternational Solid–State Circuits Conference, Feb. 26, 1987.

Transputer Reference Manual, lNMOS Limited 1988.

Horwitz et al., "A 20–MlPS Peak, 32–bit Microprocessor with On–Chip Cache," *IEEE Journal of Solid State Circuits*, SC–22(5):790–799 (Oct. 1987).

Submicron Systems Architecture Project, Caltech Computer Science Technical Report, Nov. 1, 1991.

Stevens, C. W., "The Transputer," *IEEE*, pp. 292–300 (1985).

Bosshart et al., "A 533K–Transistor LlSP Processor Chip", *IEEE Journal of Solid State Circuits*, SC–22(5): 808–819 (Oct. 1987).

Jguppi et al., "A 20 Mips Sustained 32b CMOS with 64b Data Bus," *IEEE Int'l Solid State Circuits Conf.*, pp. 84–86 (1989).

May, D., "The lnfluence of VLSl Technology on Computer Architecture," pp. 247–256.

"Motorola MC68HC11A8 HCMOS Single–Chip Microcomputer," table of contents and introduction (1985).

"Motorola MC146805H2, advance information," pp. 1–12.

"MC68332 32–Bit Microcontroller System lntegration User's Manual Preliminary Edition, Revision 0.8," (1989).

The Ring Oscillator VCO Schematic.

"lNMOS T800 Transputer Data Sheet," (Apr. 1987).
"lNMOS T414 Transputer Preliminary Data Sheet," (Feb. 1987).
"lNMOS T212 Transputer Preliminary Data Sheet," (Aug. 1987).
"lNMOS M212 Disk Processor Product Overview," (Oct. 1987).
Budinich et al., eds. *International Conference on the Impact of Digital Microelectronics & Microprocessors on Particle Physics*, pp. 204–213 (1988).
lNMOS Presentation given at Jun. 15, 1988 Workshop on Computer Architecture.
Moore, P., "lNMOS Technical Note 15: lMS B005 Design of a Disk Controller board with drives," Dec. 3, 1986.
Matthys R. J., *Crystal Oscillator Circuits*, pp. 25–64 (1983).
Elliot et al., eds. *Scientific Applications of Multiprocessors* Prentice Hall (1988).
Transputer Reference Manual, Cover page, lntroduction and pp. 73and 96, lNMOS Limited (1988).
"lNMOS lMS T414 Transputer," (Jun. 1987).
"lNMOS lMS T414 Engineering Data," pp. 107–163.
"lNMOS Engineering Data, lMS T414M Transputer, Extended Temperature," (Aug. 1987).
"SM550 High Speed CMOS 4–bit Microcomputer SM–550 Series," (1982) document in Japanese.
"MC88100 RlSC Microprocessor User's Manual," Motorola (1989).
Mead et al., eds., *Introduction of VLSI Systems*, Addison Wesley Publishers, (1980).
Moelands, A. P. M., "Serial l/O with the MA B8400 series microcomputers," *Electronic Components and Applications*, 3(1):38–46 (1980).
Stanley, R. C., "Microprocessors in brief," *IBM J. Res. Develop.*, 29(2):110–118 (Mar. 1985).
"MC68332 User's Manual," Motorola (1995).
"TMS370 Microcontroller Family User's Guide," Texas lnstruments (1996).
"lNMOS Preliminary Data lMS T800 transputer," (Apr. 1987).
"lNMOS Engineering Data lMS T212 transputer Preliminary," (Aug. 1987).
"lNMOS Product Overview lMS M212 disc processor," (Oct. 1987).
"MN18882 LSl User's Manual," (document in Japanese).
"MN1880 (MN18882) lnstruction Manual," (document in Japanese).
"MN188166 User's Manual," (document in Japanese).
Paker, Y., *Multi–Processor Systems*, pp. 1–23 (1983).
"HP Sacajawea External Reference Specification Preliminary Version 1.1," (Jan. 14, 1987).
"Data sheet MOS lntegrated Circuit uPD75008," NEC (1989).
Product Brochure by Motorola for MC146805H2.
Shyam, M., "Hardware External Reference Specification for Enhanced Champion/Paladin," Revision of Nov. 11, 1986.
Fish deposition transcript, vols. 1 and 2, held Jun. 25, 2007 and Jun. 26, 2007 in case No. 2–05CV–494 (TJW).
Exhibit 4 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); memo of Sep. 12, 1992 Fish to Higgins re: ShBoom Patents.
Exhibit 5 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Sep. 11, 1992 Higgins to Falk re: patent application for High Performance Low Cost Microprocessor.
Exhibit 6 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Sep. 30, 1992 Higgins to Falk re: patent application for High Performance Low Cost Microprocessor.
Exhibit 8 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Mostek 1981 3870/F8 Microcomputer Data Book (1981).
Exhibit 9 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); "lC Master 1980", pp. 2016–2040, published by Fairchild (1980).
Exhibit 10 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of May 12, 1992, Fish to Higgens.
Exhibit 12 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Agreement executed Jan. 3, 1989 between PTA lnc. and Chuck Moore, dba Computer Cowboys.
Exhibit 13 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Oki japan MSH–Boom 96000 Schematic (Jul. 13, 1989).
Exhibit 14 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Assignment of U.S. Appl. No. 07/389,334 from Fish to Fish Family Trust.
Exhibit 15 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Stock Purchase and Technology Transfer Agreement between Fish Family Trust, Helmut Falk, and Nanotronics Corporation (Aug. 16, 1991).
Exhibit 16 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); fax of Jul. 16, 2004Mmarshall to Suanders and Heptig w/ attached Jul. 15, 2004 memo from Beatie re: Fish and Moore.
Exhibit 17 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Fax of Jul. 29, 2004, Heptig to Marshall with attached executed agreement.
Exhibit 18 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Plaintiffs' Second Amended Complaint filed Sep. 22, 2006 in 3:06–CV–00815.
Exhibit 19 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Settlement Agreement between Patriot Scientific Corporation, Fish, and the trustee of Fish Family Trust.
Exhibit 21 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Comparisons of RlSC Chips (Dec. 11, 1988).
Exhibit 22 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); VL86C010 An Affordable 32–bit RlSC Microprocessor System, VLSl Technology, lnc.
Exhibit 23 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); VY86Cxxx ARM 32–Bit CMOS product literature, EDN (Nov. 21, 1991).
Exhibit 24 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Apr. 26, 1989 lreland to Fish w/ copy of Apr. 17, 1989 article in Electronic News titled "35ns 256K Device, VLSl Debuts SRAM Designed With Hitachi,".
Exhibit 28 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); lntroduction to RlSC Technology, LSl Logic Corporation (Apr. 1988).
Exhibit 29 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); "SH–Boom Patent Documentation," (Jun. 21, 1989).
Exhibit 30 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); "Sh–Boom Licensing Strategy," (Jan. 19, 1990).

Exhibit 31 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); "Transputer lncludes Multiprocessing protocol," Jan. 2, 1991.
Exhibit 32 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); article titled "lNMOS details next Transputer," (Apr. 18, 1991).
Exhibit 33 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Articles from Electronic World News.
Exhibit 35 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); lNMOS Preliminary Data lMS T414 transputer.
Exhibit 36 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Comparison of lntel 80960 and Sh–Boom Microprocessors (1989).
Exhibit 37 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Memo of Jul. 13, 1989, Fish to Chu w/ attached comparison of MlPS 2000 to Sh–Boom.
Exhibit 38 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); fax of Jun. 10, 1992 Fish to Higgins w/ attached document titled State of the Prior Art ShBoom Microprocessor.
Exhibit 39 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Apr. 12, 1989 Time and Responsibility Schedule.
Exhibit 40 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); handwritten note.
Exhibit 41 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); memo of Jun. 1989 to PT Acquisitions, lnc. re: fees due for searches conducted.
Exhibit 42 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); memo of Jun. 28, 1992 Fish to Higgins re: Dialog Patents re: ShBoom.
Exhibit 43 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Aug. 6, 1998 Haerr to Turner transmitting documents.
Exhibit 44 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Declaration of Moore re: U.S. Appl. No. 08/484,918.
Exhibit 45 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); fax of Nov. 3, 1989, Leckrone to Fish with attached draft license agreement between PT Acquisitions and Oki Electric lndustries.
Exhibit 46 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Nov. 29, 1989 Fish to Slater re: Japanese "borrowing" Sh–Boom 50 MHz RlSC Chip.
Exhibit 47 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Dec. 29, 1989 Leckrone to Fish re: ShBoom project.
Exhibit 48 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Jul. 16, 1990 Fish to Leckron re: attorney client relationship and conflict of interest.
Exhibit 49 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Jul. 24, 1990 Leckrone to Fish re: letter of Jul. 16, 1990 (EX 48).
Exhibit 50 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Aug. 27, 1990 Moore to Fish re: ShBoom confidentiality.
Exhibit51 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); PT Acquisitions / Alliance Semiconductor Corp. Manufacturing Agreement (Jul. 20 1990).
Exhibit 52 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Feb. 6, 1990 to PT Acquisitions from Dun & Bradstreet Receivable Recovery Systems re: final notice for payment of account.
National Semiconductor HPC16400/HPC36400/HPC46400 High–Performance microControllers with HDLC Controller product literature.
NEC Data Sheet Mos lntegrated Circuit uPD7225 Programmable LCD Controller/Driver. Part Nos. uPD7225G00, uPD7225G01, uPD7225GB–3B7.
NEC Electronics lnc. High–End, 8–Bit, Single–Chip CMOS Microcomputers product literature.
NEC Electronics lnc. uPD78C10/C11/C14 8–Bit, Single–Chip CMOS Microcomputers with A/D Converter product literature.
NEC Electronics lnc. Microcomputer Products Single–Chip Products Data Book vol. 1 of 2 cover page.
NEC Electronics lnc. Microcomputer Products Microprocessors, Peripherals, & DSP Products Data Book vol. 2 of 2 cover page.
NEC Electronics lnc. MOS lntegrated Circuit uPD70208H, 70216H Data Sheet, V40HL, V50HL, 16/8; 16–Bit Microprocessor.
NEC Electronics lnc. MOS lntegrated Circuit uPD7225 Programmable LCD Controller/Driver.
Signetics Microprocessor Data manual cover page.
Signetics Microprocessor Products Data manual, 8×330 Floppy Disk Formatter/Controller product specification.
Signetics Microprocessor Products Data manual, SC96AH Series Single–Chip 16–Bit Microcontrollers preliminary specification.
Realtime DSP; The TMS320C30 Course, Revision 3 (educational document re programming Digital Signal Processor microprocessor).
Texas lnstruments TMS320C30 Digital Signal Processor product literature.
Texas lnstruments TMS320C30 Digital Signal Processor product literature.
Texas lnstruments TMS34010 Graphics System Processor product literature.
Texas lnstruments TMS320 DSP Designer's Notebok, Using a TMS320C30 Serial Port as an Asynchronous RS–232 Port Application Brief: SPRA240.
UK application 8233733 as filed Nov. 26, 1982.
Office Action of Jan. 31, 2000 in U.S. Appl. No. 09/124,623.
TPL lnfringement Contention for the TLCS–900/L Series.
TPL lnfringement Contention for Toshiba Microcontroller.
TPL lnfringement Contention for Toshiba TC35273.
Duell, C. H., "Everything that can be invented has been invented," 2 pages downloaded from http://www.tplgroup.net/patents/index.php.
Alliacense Product Report, NEC Microcontroller, UPD789473, B Bit Microcontroller, pp. 1–38.
Mostek Corp., Advertisement, EDN, Nov. 20, 1976.
Guttag, K.M., "The TMS34010: An Embedded Microprocessor," *IEEE Micro*, 8(3):39–52 (May 1988).
"8–Bit Single–Chip Microprocessor Data Book," Hitachi America Ltd., Table of Contents and pp. 251–279) Jul. 1985).
Request for Reexamination of U.S. Patent 6,598,148 as filed Sep. 21, 2006.
Office action of Nov. 22, 2006 in application No. 90/008, 227.
Toshiba TLCS–42, 47, 470 User's Manual Published in Apr. 1986.
Fukui et al., "High Speed CMOS 4–bit Microcomputer SM550 Series," published 1982, 1983.

lntel 80386 Programmer's Reference Manual, published by lntel (1986).
Fairchild Microcomputers, F8/3870, F6800, Bit Slice, lC Master 1980, pp. 1, 2016–2040 (1980).
Mostek Corp., "Mostek 1981 3870/F8 Microcomputer Data Book", Feb. 1981, pp. lll–76 through lll–77, lll–100 through lll–129, and Vl–1 through Vl–31.
lBM Systems Reference Library, lBM System/360 Model 67 Functional Characteristics, File No. S360–01, Form A27–2719–0, published by lBM (1967).
Anderson, D.W., The lBM System/360 Model 91: Machine Philosophy and lnstruction Handling, lBM Journal, (1967).
GE–625/ 635 Programming Reference Manual, revised Jan. 1966.
Clipper™ 32–Bit Microprocessor, lntroductions to the Cliper Architecture, published by Fairchild in 1986.
Simpson et al., "The lBM RT PC Romp processor and memory management unit architecture," *IBM systems Journal*, 26(4):346–360.
M68300 Family MC68332 User's Manual, published by Motorola, lnc. in 1995.
Ditzel et al., "The Hardware Architecture of the Crisp Microprocessor," AT & T lnformation Systems, ACM, pp. 309–319 and table of contents (1987).
i860 64–Bit Microprocessor, published by lntel Corporation Feb. 1989.
Rau et al., "The Cydra 5 Departmental Supercomputer, Design Philosophies, Decisions, and Trade–offs," *IEEE* pp. 12–36 (1989).
Datasheet for lntel 4004 Single Chip 4–Bit 9–Channel Microprocessor, pp. 8–15 to 8–23.
lntel MCS–4 Micro Computer Set (Nov. 1971).
lntel 8008 8–Bit Parallel Central Processor Unit published by lntel (Nov. 1972).
iAPX 386 High Performance 32–Bit Microprocessor Product Review, published by lntel (Apr. 1984).
lntel 80386 Programmer's Reference Manual, published in lntel (1986).
Motorola MC68020 32–Bit Microprocessor User's Manual (1984).
Thornton, J. E., "Design of a Computer, The Control Data 6600," published by Advanced Design Laboratory (1970).
6400/6500/6600 Computer Reference Manual, published by Control Data® (1965, 1966, 1967).
Grishman, R., "Assembly Language Programming for the Control Data 6600 and Cyber Series Algorithmics".
Hennessy et al., "MlPS: A Microprocessor Architecture," *IEEE*, pp. 17–22 (1982).
Hennessy et al., "Hardware/software tradeoff for increased performance," *Proceedings of the Symposium on Architectural Support for Programming Languages and Operating Systems*, pp. 2–11, ACM, Apr. 1982.
Hennessy et al., "MlPS: A VLSl Processor Architecture, Technical Report 223," Computer Systems Laboratory, Department of Electrical Engineering and Computer Science, Standford University Nov. 1981.
Gross et al., "Measurement and evaluation of MlPS architecture and processor," *ACM Trans. Computer Systems*, pp. 229–257 Aug. 1988.
Bit Sparc lnteger Unit B5000 Datasheet attached to a presentation by Anant Agrawal in 1989.
Sequin et al., "Design and lmplementation of RlSC1," pp. 276–298 from *VLSI Architecture*, B. Randell and P.C. Treleaven, editors, Prentice Hall, 1983.
Ungar et al., "Architecture of SOAR: Smalltalk on a RlSC," *Proceedings of the 11th Annual International Symposium on Computer Architecture ISCA '84*. ACM Press, New York, NY, pp. 188–197 (1984).
Cray–l Computer System Hardware Reference Manual, Publication No. 2240004, Rev C, Nov. 4, 1997.
Acorn Computers, Ltd., Acorn RlSC Machine CPU Software Manual, lssue 1.00 Oct. 1985.
Patterson et al., "Architecture of a VLSl lnstruction Cache for A RlSC," *ACM*, pp. 108–116 (1983).
Patterson, D. A., "Reduced lnstruction Set Computers" *Communication of the ACM*, 28(1):8–21, Jan. 1985.
Patterson, D. A., "RlSC watch", pp. 11–19 (Mar. 1984).
Sherburne, R. W., "Processor Design Tradeoffs in VLSl," U.C. Berkeley, May 1984. PhD Dissertation.
Excerpt from A Seymour Cray Perspective http://research.Microsoft.com/users/gbell/craytalk/std001.htm (Slide 1).
Excerpt from A Seymour Cray Perspective htpp.//research.microsoft.com/users/gbell/craytalk/std029.htm (Slide 29).
RlSC Roots: CDC 6600 (1965).
http://www.bitsavers.org/pdf/tdc/6x00/.
Simpson, R.O., "The lBM RT Personal computer," *BYTE*, 11(11):43–78 (Oct. 1986).
Ryan, D.P., "lntel's 80960: An Architecture Optimized for Embedded Control," *IEEE, Micro,* published in Jun. 1988.
Waters, F., "lBM RT Personal Computer Technology," lBM Corp. 1986.
Alliacense Product Report, USP 5784584, TLCS–900/H1 Series TMP92C820, Toshiba Microcontroller TMP92C820 / TLCS–900/H1 Series 16–bit Microcontroller, pp. 1–9, filed Aug. 14, 2006 in 2:05–CV–00494–TJW.
Alliacense Product Report, NEC Microcomputer, USP 5784584, V850E2 32 Bit Microcontroller, pp. 1–8 (2006).
"8 bit Dual 1–chip Microcomputer MN1890 Series User's Manual," translation of original Japanese language document, by Matsushita Electric lndustrial Co., Ltd. Semiconductor Sales Division.
Sibigtroth, J. M., "Motorola's MC68HC11: Definition and Design of a VLSl Microprocessor," *IEEE Micro* 4(1):54–65 (1984).
"Specification Sheet, MN18882 (Book)," translation of the Japanese language original, Code No. MlG0175, Matsushita Electronics lndustry Corporation, Microcomputer Products Division, Oct. 2, 1990.
"DS5000 Soft Microcontroller User's Guide Preliminary V 1.0," Dallas Semiconductor.
MN188166 User's Manual, Japanese language document with English translation.
Alliacense Product Report—Preliminary Review, USP 5,440,749; GPS Car Navigation Main Processor.
Alliacense Product Report—Preliminary Review, USP 5,440,749; GSP Navigation System GPS Chipset.
Alliacense Product Report—Preliminary Review, USP 5,440,749; GPS Navigation System Main Microprocessor.
Alliacense Product Report—Preliminary Review, USP 5,440,749; Kyocera Digital Camera Finecam S3R lmage Processor.
Alliacense Product Report—Preliminary Review, USP 5,440,749; PDA/Mobile Navigation, GPS Processor.
Motorola MC68020 32–bit Microprocessor User's Manual, 2nd Edition, Rev. 1, Prentice–Hall, 1985.
Barron et al., "The Transputer," *Electronics*, pp. 109–115 (1983).

Burroughs Corporation, "Burroughs B7700 Systems Reference Manual," 1973.
Fiasconaro, J., "Microarchitecture of the HP9000 Series 500 CPU," *Microarchitecture of VLSI Computers, NATO ASI Series No. 96*, Antognetti, eds., pp. 55–81.
MacGregor et al., "The Motorola MC68020," *IEEE Micro*, 4(4):103–118 (1984).
Best et al., "An Advanced–Architecture CMOS/SOS Microprocessor", lEEE Micro, vol. 2, No. 3, vol. 2, No. 3 (Jul. 1982), pp. 10–26.
Technology Properties Limited (TPL), Moore Microprocessor Patent (MMP) Portfolio, downloaded from <<www.tpl-group.net/patents/index.php>> downloaded on Aug. 3, 2006, 3 pages total.
Acorn's R1SC Leapfrog, Acorn User special issue, Jun. 1987; 59: 149–153.
Agrawal, et al., "Design Considerations for a Bipolar lmplementation of SPARC," Compcon Spring apos;88. Thirty–Third lEEE Computer Society lnternational Conference, Digest of Papers, Feb. 29–Mar. 3, 1988, pp. 6–9.
Agrawal, "An 80 MHz Bipolar ECL lmplementation of SPARC," Sun Microsystems, lnc., Jun. 25, 1989, 40 pages total.
ARM Datasheet, Part No. 1 85250 0360 0, lssue No. 1 (Mar. 17, 1987).
Atmel SPARC lnstruction Set, "Assembly Language Syntax," Rev. 4168C–AERO–08/01, 2002.
Bagula, "A 5V Self–Adaptive Microcomputer with 16Kb of #2 Program Storage and Security," lEEE lnternational Solid–State Circuit Conference, 1983, pp. 34–35.
Bayko, Great Microprocessors of the Past and Present (V 11.7.0), downloaded from: <<http://web.archive.org/web/20010107210400/http://bwrc.eecs.berkeley.edu/ClC/Archive/cup_history.html>>, Feb. 2007, 60 pages total.
Books Review: Operating Systems A Systematic View, William S. Davis, Addison–Wesley Publishing Company, lnc., 1987; 26(4):453–454.
Bourke, "Character Synchronization During Overrun Conditions," Delphion, lBM Technical Disclosure Bulletin, Dec. 1977.
Burroughs Corporation, "Burroughs B5500 lnformation Processing System Reference Manual," 1973.
CAL Run Fortran Guide, University of California, Computer Center, Berkeley, 292 pages total, (Sep. 1974).
CDC 6000 Computer Systems—Cobol lnstant 6000, Version 3; Control Data Publication No. 60327600A (Apr. 1971).
CDC 6000 Computer Systems, 7600 Computer Systems: Fortran Extended lnstant 6000 Version 3, 7600 Version 1; Control Publication No. 60305900A (May 1971).
CDC 6000 Computer Systems/7600 Computer Systems: Fortran Extended Reference Manual, 6000 Version 3, 7600 Version 1; Control Data Publication No. 60329100, Revision D (1972).
CDC 6000 Series Computer System, 6642 Distributive Data Path Operation and Programming Reference Manual; Control Data Publication No. 60376300C (Mar. 1979).
CDC 6000 Series Computer Systems—Chippewa Operating System Documentation, vol. l, Preliminary Edition (updated May 1966).
CDC 6000 Series Computer Systems—Chippewa Operating System Documentation, vol. ll, Preliminary Edition, Peripheral Packages and Overlays (Oct. 1965).
CDC 6000 Series Computer Systems—Chippewa Operating System Documentation, vol. lll, Preliminary Edition, DSD—The Systems Display, (Nov. 1965).
CDC 6000 Series Computer Systems Ascent General lnformation Manual; Control Data Publication No. 60135400 (Feb. 66).
CDC 6000 Series Computer Systems Chippewa Operating System Reference Manual; Control Data Publication No. 60134400 (Dec. 1965).
CDC 6000 Series Computer Systems Hardware Reference Manual; Control Data Publication No. 60100000 (Aug. 1978).
CDC 6000 Series Computer Systems/ 7600 Computer System: 6000 Compass Version 2, 7600 Versions 1 & 2 Reference Manual; Control Data Publication No. 60279900, Revision D, (1970, 1971, 1972).
CDC 6000 Series Computer Systems: Chippewa Operating System Fortran Reference Manual; Control Data Publication No. 60132700A (May 1966).
CDC 6000 Series Computer Systems: Peripheral Equipment Reference Manual; Control Data Publication No. 60156100, Revision J (Mar. 1970).
CDC 6000 Series Computer Systems: Site Preparation and lnstallation Manual; Control Data Publication No. 60142400, Revision B (Sep. 1965).
CDC 6000 Series Computer Systems: Fortran Extended General lnformation, Control Data Publication No. 60176400 (Oct. 1966).
CDC 6000 Series Fortran Extended 4.0, lnternal Maintenance Specifications , (1971).
CDC 6000 Series lntroduction and Peripheral Processors Training Manual, Second Edition, Control Data Publication No. 60250400 (Nov. 1968).
CDC 6400 Central Processor, Control Data Publication No. 60257200 (Feb. 1967).
CDC 6400/6500/6600 Ascent–to–Compass Translator; Control Data Publication No. 60191000 (Mar. 1967).
CDC 6400/6500/6600 Computer System lnput/Output Specification; Control Data Publication No. 60045100 (Sep. 1967).
CDC 6400/6500/6600 Computer System lnstant SMM; Control Data Publication No. 60299500 (Nov. 1969).
CDC 6400/6500/6600/ Computer Systems Compass Reference Manual; Data 60190900, Revision B (Mar. 1969).
CDC 6400/6500/6600 Computer Systems Reference Manual; Control Data Publication No. 60100000, Revision K (Aug. 1970).
CDC 6400/6500/6600 Extended Core Storage Systems Reference Manual; Control Data Publication No. 60225100, (Feb. 1968).
CDC 6400/6500/6600 Jovial General lnformation Manual; Control Data Publication No. 60252100A (Mar. 1969).
CDC 6400/6500/6600 Computer Systems: Ascent/Asper Reference Manual; Control Data Publication No. 60172700 (Jul. 1966).
CDC 6400/6600 Fortan Conversion Guide; Data Publication No. 60175500 (Aug. 1966).
CDC 6400/6600 Systems Bulletin (Oct. 10, 1968), 84 pages.
CDC 6400/6600, Export/lmport 8231 Reference Manual; Data Publication No. 60189100 (Apr. 1967).
CDC 6600 Central Processor vol. 1; Control & Memory; Data Control Publication Nol. 021067 (Mar. 1967).
CDC 6600 Central Processor, vol. 2, Functional Units; Control Data Publication No. 60239700 (Mar. 1967).

CDC 6600 Chassis Tabs; Control Data Publication No. 63016700A (Apr. 1965).
CDC 6600 Chassis Tabs; Control Data Publication No. 63019800 (Mar. 1965).
CDC 6600 Chippewa Operating System; Control Data Publication No. 60124500, Revision C (Apr. 1965).
CDC 6600 Computer System 6601 A–J, 6613A/B/C, 6604A/B/C, 6614–A/B/C/ Central Processor (including Functional Units) vol. 1, Diagrams & Circuit Description; Control Data Publication No. 60119300BT (Jan. 1968).
CDC 6600 Computer System 6601 A–J, 6613A/B/C, 6604A/B/C/, 6614–A/B/C Peripheral and Control Processor/Central Memory/Clock/Extended Core Storage Coupler (Std Opt 10102 and/or Spec Opt 60080)/Power Wiring, vol. 2, Diagrams & Circuit Descriptions; Control Data Publication No. 60119300BT (Jan. 1968).
CDC 6600 Computer System Operating System/Reference Manual, SIPROS66, 1st ed.; Control Data Publication No. 60101800A (1965).
CDC 6600 Computer System Programming System/Reference Manual, vol. 1. Ascent; Control Data Publication No. 601016008 (1965).
CDC 6600 Computer System Programming System/Reference Manual, vol. 2, Asper; Control Data Publication No. 60107008 (1965).
CDC 6600 Computer System Programming vol. 3, Fortran 66; Control Data Publication No. 60101500B (1965).
CDC 6600 Computer Training Manual vol. 2, Preliminary Edition, Section 7.2 Shift Functional Units, 164 pages.
CDC 6600 Data Channel Equipment 6602–B/6612–A, 6603–B, 6622–A, 6681–B, 6682–A6683–A, S.O. 60022, 60028, 60029, Diagrams & Circuit Description' Control Data Publication No. 60125000, Revision G (Jun. 1966).
CDC 6600 Training Manual; Control Data Publication No. 60147400, Revision A (Jun. 1965).
CDC 6603—A/B/C Disk File Controller Reference Manual; Control Data Publication No. 60334000 (1970).
CDC 6638 Disk File Subsystem Training Supplement; Control Data Publication 602500800A (Oct. 1968).
CDC 6638 Disk File System Standard Option 10037–A, 6639–A/B File Controller—Diagrams and Circuit Description/Maintenance/Maintenance Aids/Parts List/Wire Lists/Chassis Tabs; Control Data No. 60227300, Revision H (Mar. 1974).
CDC 6639—A/B Disk File Controller Reference Manual; Control Data Publication No. 60334100E (Aug. 1973).
CDC 6639 Disk Controller Training Manual Test Edition (Sep. 1967), 28 pages.
CDC APL Version 2 Reference Manual, CDC Operating Systems :NOS; Control Data Publication No. 60454000F (Nov. 1980).
CDC Basic Version 3 Reference Manual: NOS 1 & NOS/BE 1; Control Data Publication No. 19983900G (Oct. 1980).
CDC Chippewa Operating System, Document Class ERS, System No. E012, Version 1.1; External Reference Specifications—Chippewa Operating System, (Jun. 1966).
CDC Chippewa Operating System, Document Class SIR, System No. E012, Version 1.0, (Mar. 3, 1966).
CDC Chippewa Operating System, Document Class SIR, System No. E012, Version 1.1, (Mar. 3, 1966).
CDC Cobol Version 4 Instant Manual, Cyber 170 Series, Cyber 70 Models 72, 73, 74, 6000 Series; Control Data Publication No. 60497000A (Feb. 1976).
CDC Cobol Version 5 Instant Manual, Operating Systems: NOS 1/BE 1; Control Data Publication No. 60497300B (Feb. 198).
CDC Codes/Control Data 6400/6500/6600 Computer Systems; Control Data Publication No. 60141900, Revision C (1966, 1967).
CDC Codes/Control Data 6400/6500/6600/6700 Computer Systems; Control Data Publication No. 60141900, Revision D (1966, 1967).
CDC Codes/Control Data 6600; Control Data Publication No. 60141900, Revision A (May 1965).
CDC Compass Version3 Instant, Operating Systems: NOS 1, NOS 2, NOS/BE 1, Scope 2; Control Data Publication No. 60492800D (Jun. 1982).
CDC Course No. FH4010–1C, NOS Analysis, Student Handbook, Revision C (Apr. 1980).
CDC Course No. FH4010–4C NOS Analysis, Study Dump (Apr. 1980).
CDC Cyber 170 Models 720, 730, 740, 750 and 760 Model 176 (Level B/C) Computer Systems, Codes; Control Data Publication No. 60456920C, (Jun. 1981).
CDC Cyber 70 Computer Systems Models 72, 73, 74, 6000 Computer Systems: Fortran Reference Manual Models 72, 73, 74 Version 2.3, 6000 Version 2.3; Control Data Publication No. 19980400, Revision F (Jul. 1972).
CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems—ALGOL Reference Manual, Cyber 70 Series Version 4, 6000 Series Version 4, 7600 Series Version 4; Control Data Publication No. 60384700A (Aug. 1973).
CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems: Cobol Instant Models 72, 73, 74 Version 4, Model 76 Version 1, 6000 Version 4; Control Data Publication No. 60328400A (Dec. 1971).
CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems: Fortran Extended Instant Models 72, 73, 74 Version 4, Model 76 Version 2, 7600 Version 2, 6000 Version 4; Control Data Publication No. 60357900A (Nov. 1971).
CDC Cyber 70 Computer Systems Models 72, 73, 74, 76 7600 Computer System, 6000 Computer Systems: Fortran Extended Reference Manual Models 72, 73, 74 Version 4, Model 76 Version 2, 6000 Version 4; Control Data Publication No. 60306600A (Oct. 1971).
CDC Cyber 70 Series 6000 Series Computer Systems: APL *Cyber Reference Manual; Control Data Publication No. 19980400B (Jul. 1973).
CDC Cyber 70 Series Computer Systems 72, 73, 74, 6000 Series Computer Systems—Kornos 2.1 Workshop Reference Manual; Control Data Publication No. 97404700D (1976).
CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, Krono 2.1 Operator Guide; Control Data Guide; Control Data Publication 60407700A (Jun. 1973).
CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, Kronos 2.1 Installation Handbook; Control Data Publication No. 60407500A (Jun. 1973).
CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, Kronos 2.1 Time–Sharing User's Reference Manual; Control Data Publication No. 60407600B (May 1974).

CDC Cyber 70/ Model 76 Computer System, 7600 Computer System: Fortran Run, Version 2 Reference Manual; Control Data 60360700C (May 1974).
CDC Cyber Interactive Debug Version 1 Guide for Users of Fortran Extended Version 4, CDC Operating Systems: NOS 1, NOS/ BE1, Control Data Publication No. 60482700A (Feb. 1979).
CDC Cyber Interactive Debug Version 1 Guide for Users of Fortran Version 5, Operating Systems: NOS 1, NOS/ BE 1; Control Data Publication No. 6048100C (Sep. 1984).
CDC Cyber Interactive Debug Version 1 Reference Manual, NOS 1, NOS 2, NOS/ BE 1; Data Control Publication No. 60481400D (Jun. 1984).
CDC Cyber Loader Version 1 Instant, CDC Operating System NOS1, NOS/ BE 1; Control Data Publication No. 60449800C (Aug. 1979).
CDC Disk Storage Subsystem—Operation and Programming Manual; Control Data Publication No. 60383900, Version T (1972–1980).
CDC Fortran Extended 2.0, Document Class ERS, System No. C012, (Dec. 1966).
CDC Fortran Extended 2.0, Document Class IMS, Internal Maintenance Specifications—64/65/6600 V Fortran Extended Version 2 (Mar. 1969).
CDC Fortran Extended Version 4 Instant Manual, Operating Systems: NOS 1, NOS/BE, 1 Scope 2; Control Data Publication No. 60497900B (Jun. 1981).
CDC Fortran Extended, Sales Technical Memorandum (May 1967).
CDC Fortran Version 5 Instant, CDC Operating System: NOS 1, NOS/ BE 1, Scope 2; Control Data Publication No. 60483900A (Jan. 1981).
CDC GED Fortran Extended 1.0, Product No. C012, Dept. No. 254, Project No. 4P63FTN (Aug. 1967).
CDC Instant 6400/3500/6500 Simula; Control Data Publication No. 60235100, Revision A (Feb. 1969).
CDC Instant 6400/6500/6600 Compass; Control Data Publication No. 60191900, Revision A (1968).
CDC Instant Fortran 2.3 (6000 Series); Data Publication No. 60189500D (May 1969).
CDC Internal Maintenance Specification; Fortran V5.; Control Data Publication No. 77987506A.
CDC Internal Maintenance Specification; Fortran V5.; Control Data Publication No. 77987506A.
CDC Kronos 2.1 Reference Manual vol. 1 of 2; Control Data Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems; Control Data Publication No. 60407000D (Jun. 1975).
CDC Kronos 2.1 Time–Sharing User's Reference Manual, Cyber 70 Series Models 72, 73, 74, 6000 Series Computer Systems; Control Data Publication No. 60407600D (Jun. 1975).
CDC Model dd 60A Computer Control Console/Customer Engineering Manual; Control Data Publication No. 82100010 (Mar. 1965).
CDC Model dd60b Computer Control Console/Customer Engineering Manual/ Control Data Publication No. 82103500 (Feb. 1967).
CDC Network Products: Network Access Method Version 1, Network Definition Language Reference Manual; Control Data Publication No. 60480000J (May 1981).
CDC Network Products: Network Terminal User's Instant—Operating System NOS 1; Control Data Publication No. 60456270C, (Oct. 1980).
CDC NOS 2 Operations Handbook; Control Data Publication No. 60459310, (Aug. 1994).
CDC NOS Version 1 Applications Programmer's Instant, CDC Computer Systems; Cyber 170 Series, Cyber 70 Models, 71, 72, 73, 74, 6000 Series; Control Data Publication No. 60436000H (Jan. 1980).
CDC NOS Version 1 Internal Maintenance Specification vol. 1 of 3; Control Data Publication No. 60454300B (Aug. 1979).
CDC NOS Version 1 Internal Maintenance Specification vol. 2 of 3; Control Data Publication No. 60454300B (Aug. 1979).
CDC NOS Version 1 Internal Maintenance Specification vol. 3 of 3; Control Data Publication No. 60454300B (Aug. 1979).
CDC NOS Version 1 Operator's Guide, CDC Computer Systems: Cyber 170 Series, Cyber 70 Model 71, 72, 73, 74, 6000 Series (Dec. 1980).
CDC NOS Version 1 Reference Manual vol. 1 of 2, CDC Computer Systems: Cyber 170 Series, Cyber 70 Models 71,72, 73, 74, 6000 Series; Control Data Publication No. 60435400J (1979).
CDC NOS Version 1 Reference Manual vol. 2 of 2, CDC Computer Systems: Cyber 170 Series, Cyber 70 Models 71, 72, 73, 74, 6000 Series; Control Data Publication No. 60445300E (1977).
CDC NOS Version 1 System Maintenance Reference Manual; Control Data Publication No. 60455380H (Apr. 1981).
CDC NOS Version 2 Analysis Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60459300D (Oct. 84).
CDC NOS Version 2 Analysis Handbook; Control Data Publication No. 60459300U (Jul. 1994).
CDC NOS Version 2 Installation Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60459320E_(Mar. 1985).
CDC NOS Version 2 Operation/Analysis Handbook, Cyber 170, Cyber 70 Models 71, 72, 73, 74 6000, Control Data Publication No. 60459310C (Oct. 1983).
CDC NOS Version 2 System Maintenance Reference Manual, Cyber 170, Cyber 70 Models 71, 72, 73 74, 6000; Control Data Publication No. 60459300C (Oct. 1983).
CDC NOS/BE Version 1 Diagnostic Handbook, Cyber 180; Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publicaton No. 60494400–V (1986).
CDC NOS/BE Version 1 Installation Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60494300AB (Dec. 1988).
CDC NOS/BE Version 1 Reference Manual, Cyber 170 Series, Cyber 70 Models 71, 72, 73, 74, 6000 Series; Control Data Publication No. 60493800M 1981.
CDC Outline of Reports on Feasibility Study of 64/6600 Fortran Ver 3.0 and Conversational Fortran, Fortran Study Project, Product No. X010, Dept. No. 254, Project No. 4P63, (Jun. 1966).
CDC Pascal Version 1 Reference Manual, Operating Systems: NOS 2; Control Data Publication No. 60497700 (Sep. 1983).
CDC Pascal Version 1 Reference Manual, Operating Systems: NOS 2; Control Data Publication No. 60497700A (Dec. 1982).

CDC PL/1 Version 1 Instant, CDC Operating Systems: NOS 1, NOS/ BE1, Control Data Publication No. 60483700A (Nov. 1979).
CDC Simscript 11.5 Instant, Control Data Publication No. 84000450B (Sep. 1978).
CDC Sort/Merge Version 4 and 1 Instant, Operating Systems: NOS 1, NOS/BE 1, Scope 2; Control Data Publication No. 60497600C (Jan. 1981).
CDC Sort/Merge Vision 5 Reference Manual, Operating Systems: NOS 2, NOS/ BE 1; Control Data Publication No. 60484800C (Feb. 1984).
CDC SYMPL Version 1 Instant, NOS 1, NOS/BE 1, Scope 2; Control Data Publication No. 60482600A (May 1978).
CDC SYMPL Version 1 Users Guide, Operating Systems: NOS 1, NOS/BE 1, Scope 2; Control Data Publication No. 60499800B (Apr. 1978).
CDC Update Instant, Cyber 170 Series, Cyber 70 Series, 6000 Series, 7600 Computer Systems; Control Data Publication No. 60450000A (Nov. 75).
CDC Update Reference Manual Operating Systems: Scope 3.4, Kronos 2.1; Control Data Publication No. 60342500, Revision H (1971–1976).
CDC Xedit Version 3 Reference Manual, Operating System: NOS 1; Control Data Publication No. 60455730B (Aug. 1979).
Chippewa Laboratories Fortran Compiler Run, Preliminary Edition, CDC 6000 Series Computer Systems, (Apr. 1966).
Cho et al., WAM 3.6: A 40K Cache Memory and Memory Management Unit, ISSCC '86, Feb. 19, 1986.
Cordell, II et al., "Advanced Interactive Executive Program Development Enviornment," IBM Systems Journal, 1987; 26(4):381–382.
Crawford, "The i486 Executing Instructions in One Clock Cycle," IEEE Micro, pp. 28–36 (Feb. 1990).
Disk Routines and Overlays, Chippewa Operating System, CDC Development Division—Applications, (Nov. 1965).
Dowsing et al., "Computer Architecture: A First Course, Chapter 6: Architecture and the Designer," Van Nostrand Reinhold (UK) Co. Ltd., pp. 126–139.
Evans et al., "An Experimental 512–bit Nonvolatile Memory with Ferroelectric Storage Cell," IEEE Journal of Solid–State Circuits, 23(5):1171–1175.
Field Maintenance Print Set, KA780–01–01 Rev. A.
Fisher et al., "Very Long Instruction Word Architectures and the ELI–512," ACM pp. 140–150 (1983).
Furber, VSLI RISC Architecture and Organization, Chapter 3: Commercial VLSI RISC, pp. 124–129, Marcel Dekker, Inc., 1989.
GB Patent Application 8233733, INMOS, Ltd. Microcomputer, filed Nov. 26, 1962.
GE 600 Series, publication.
Gershon, Preface, IBM Systems Journal 26(4):324–325.
Green et al., "A Perspective on Advanced Peer–to–Peer Networking," IBM Systems Journal, 1987; 26(4):414–428.
Grimes et al., "64–bit Processor, The Intel i860 64–Bit Processor: A General–Purpose CPU with 3D Graphics Capabilities", published by Intel, p. 85 (Jul. 1989).
Hansen, "A RISC Microprocessor with Integral MMU and Cache Interface," ICCD '86, pp. 145–148, 1986.
Hennessy et al., "Hardware/software Tradeoff for Increased Performance," Technical Report No. 22.8, Computer Systems Laboratory, Feb. 1983, 24 pages.
Hennessy et al., "The MIPS Machine", COMPCON, IEEE, Spring 1982, pp. 2–7.
Hennessy, "Performance Issues in VLSI Processor Design," IEEE on VLSI in Computers, pp. 153–156 (1983).
Hinton, 80960—Next Generation, Compcon Spring 89, IEEE, 13–18 (1989).
Hollingsworth et al., "The Fairchild Clipper: Instruction Set Architecture and Processor Implementation," Report No. UCB/CSD 87/329, Computer Science Division (EECS), University of California Berkeley, California, (Feb. 11, 1987).
HP 9000 Instrument Controllers, Technical Specifications Guide, Oct. 1989.pdf.
HP 9000 Series Computer Systems, HP–UX Reference 09000–090004, Preliminary Nov. 1982.
Hughes, "Off–Chip Module Clock Controller", Delphion, IBM Technical Disclosure Bulletin, Sep. 1989.
Hunter, "Introduction to the Clipper Architecture," IEEE Micro, pp. 6–26 (Aug. 1987).
IBM RT PC, BYTE 1986 Extra Edition, Inside The IBM PCs, pp. 60–78.
INMOS Limited, IMS T424 Transputer Reference Manual, 1984.
Intel 388Tm DX Microprocessor 32–Bit CHMOS Microprocessor With Integrated Memory Management (1995).
Intel 80960CA User's Manual published by Intel (1989).
Intel Architecture Optimization Manual, Order No. 242816–003, published by Intel (1997).
Intel Architecture Software Developer's Manual, vol. 1; Basic Architecture, published by Intel (1997).
Intel 8080A/8080A–1/8080A–2, 8–Bit N–Channel Microprocessor, Order No. 231453–001, Its Respective Manufacturer (Nov. 1986).
Johnson et al., "A Variable Delay Line PLL for CPU–Coprocessor Synchronization," IEEE Journal of Solid–State Circuits, 23(5): 1218–1223, Oct. 1988.
Katevenis et al., "Reduced Instruction Set Computer Architecture for VLSI," Doctoral Dissertation, Oct. 1983.
Katevenis et al., "The RISC II Micro–Architecture," Journal of VLSI and Computer Systems, 1(2):138–152 (1984).
Kipp, "Micron Technology Inc. Reports Financial Results," Business Wire, New York, Sep. 26, 1988.
Kohn et al., "Introducing Intel i860 64–Bit Microprocessor," Intel Corporation, IEEE Micro (Aug. 1989).
Koopman, "RTX 4000," Proceedings of 1989 Rochester Forth Conference, pp. 84–86.
Koopman, "The WISC Concept: A proposal for a writable instruction set computer," BYTE, pp. 187–193. (Apr. 1987).
Koopman, Jr. et al. "MVP Microcoded CPU/16 Architecture," Proceedings of 1986 Rochester Forth Conference, pp. 277–280.
Koopman, Jr. et al., "WISC Technologies, Inc., Writable Instruction Set, Stack Oriented Computers: The WISC Concept," 1987 Rochester Forth Conference, Journal of Forth Application and Research, 5(1):49–71.
Koopman, Jr., Slack Computers: the new wave, 1989.
Loucks et al., "Advanced interactive Executive (AIX) Operating System Overview," IBM Systems Journal, 1987; 26(4):326–345.
Matick, "Self–Clocked Cache," Delphion, IBM Technical Disclosure Bulletin, Apr. 1985.
Miller, Frequency Modulated Ring Oscillator for a Mode Regulated Substrate Bias Generator, Delphion, IBM Technical Disclosure Bulletin, Sep. 1989.
Mills et al, "Box Structured Information Systems," IBM Systems Journal, 1987; 26(4):395–413.

MMP Portfolio, News Release: Roland Becomes 50th Licensee, Setting a Major Milestone in Moore Microprocessor Patent Licensing Program, 3 pages (May 1, 2009).

Moussouris et al., "A CMOS RISC Processor Integrated System Functions," Proceedings of 31st IEEE Computer Society International Conference, Cathedral Hill Hotel, San Francisco, CA Mar. 3–6, 1986, pp .126–131, 1986.

Olson, Semiconductor Die with Wiring Skirt (Packaging Structure), Delphion, IBM Technical Disclosure Bulletin, Jul. 1978.

O'Neil, "Pipeline Memory System for Drams", Delphion, IBM Technical Disclosure Bulletin, May 1989.

Patterson et al., "RISC I: A Reduced Instruction Set VLSI Computer," Proceedings of the 8th annual symposium on Computer Architecture on Computer Architecture, Miinneapolis, Minnesota, pp. 443–457 (May 1981).

Pountain, "The Archimedea A310," BYTE, 1987.

Przybyiski et al., "Organization and VLSI Implementation of MIPS," Technical Report CSL–TR–84–259, Apr. 1984.

Przybyiski, "The Design Verification and Testing of MIPS", 1984 Conference on Advanced Research in VLSI, pp. 100–109.

Roche et al., "Method of Assuring a Two–Cycle Start, Zero Cycle Stop, Non–Chopping on Chip Clock Control Throughout a VLSI Clock System," Delphion, IBM Technical Disclosure Bulletin, Sep. 1989.

Rowen et al., "A Pipelined 32b NMOS Microprocessors and Microcontrollers," IEEE International Solids–State Circuits Conference, pp. 180–181, 1984.

Rubinfeld et al., "The CVAX CPU, A CMOS VAX Microprocessor Chip", International Conference on Computer Design, Oct. 1987.

Sanamrad et al., "A Hardware System Analysis Processor," IEEE, Aug. 1987, pp. 73–80.

Shih, "Microprogramming Heritage of RISC Design," Proceedings of the 23rd annual workshop and symposium on Microprogramming and microarchitecture, pp. 275–280 (1990).

Sultan et al., "Implementing System–36 Advanced Peer–to–Peer Networking," IBM Systems Journal, 1987; 26(4):429–452.

Thornton, J. E., "Considerations in Computer Design Leading Up To the Control Data 6600," Control Data Chippewa Laboratory (1970).

VAX 11/780 Architecture Handbook vol. 1, 1977–1978, 2–7 and G–8.

VAX 8800 System Technical Description vol. 2, EK–KA881–TD–PRE, Section 6, Instruction Box (IBOX), Preliminary Edition (Jul. 1986).

VAX Maintenance Handbook; VAX–11/780, EK–VAXV2–HB–002, 1983 Edition.

VL86C010 RISC Family Data Manual, Application Specific Logic Product Division, 1987.

Waters et al., "AIX Usability Enhancements and Human Factors," IBM Systems Journal, 1987; 26(4):383–394.

Williams, "Chip Set Tackles Laptop Design Issues, Offers Flat–Panel VGA Control," Computer Design, Oct. 15, 1988; 27(19):21–22.

IEEE Std 796–1983, Microcomputer System Bus, pp. 9–46 (Dec. 1983).

Mead & Conway, Introduction to VLSI Systems, pp. 1–429 (1980).

EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

ONLY THOSE PARAGRAPHS OF THE SPECIFICATION AFFECTED BY AMENDMENT ARE PRINTED HEREIN.

Column 17, lines 12–37:

Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor **50** provides a dual-clock scheme as shown in FIG. **17**, with the CPU **70** operating **[**a synchronously**]** *asynchronously* to I/O interface **432** forming part of memory controller **118** (FIG. **2**) and the I/O interface **432** operating synchronously with the external world of memory and I/O devices. The CPU **70** executes at the fastest speed possible using the adaptive ring counter clock **430**. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor **50** for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface **432**, speed of which is controlled by a conventional crystal clock **434**. The interface **432** processes requests for memory accesses from the microprocessor **50** and acknowledges the presence of I/O data. The microprocessor **50** fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. By decoupling the variable speed of the CPU **70** from the fixed speed of the I/O interface **432**, optimum performance can be achieved by each. Recoupling between the CPU **70** and the interface **432** is accomplished with handshake signals on lines **436**, with data/addresses passing on bus **90**, **136**.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

Claims **3**–**5** and **8** are cancelled.

Claims **1**, **6** and **10** are determined to be patentable as amended.

Claims **2**, **7** and **9**, dependent on an amended claim, are determined to be patentable.

New claims **11**–**16** are added and determined to be patentable.

1. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, *wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.*

6. A microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an *off-chip* external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an *off-chip* external clock, independent of said oscillator, connected to said input/output interface wherein said *off-chip* external clock is operative at a frequency independent of a clock frequency of said oscillator *and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.*

10. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an **[**on chip**]** *on-chip* input/output interface between said central processing unit and an *off-chip* external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an *off-chip* external clock wherein said *off-chip* external clock is operative at a frequency independent of a clock frequency of said variable speed clock *and wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock.*

11. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein said central processing unit operates asynchronously to said input/output interface.

12. The microprocessor system of claim 11, in which said second clock is a fixed frequency clock.

13. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;

an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and further wherein said central processing unit operates asynchronously to said input/output interface.

14. The microprocessor system of claim 13 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

15. The microprocessor system of claim 13 wherein said oscillator comprises a ring oscillator.

16. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock, wherein said central processing unit operates asychronously to said input/output interface.

* * * * *

US005809336C2

(12) **EX PARTE REEXAMINATION CERTIFICATE** (7887th)

United States Patent
Moore et al.

(10) **Number: US 5,809,336 C2**
(45) **Certificate Issued: Nov. 23, 2010**

(54) **HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK**

(75) Inventors: **Charles H. Moore**, 410 Star Hill Rd., Woodside, CA (US) 94062; **Russell H. Fish, III**, Mt. View, CA (US)

(73) Assignee: **Charles H. Moore**, Incline Village, NV (US)

Reexamination Request:
No. 90/009,457, Aug. 24, 2009

Reexamination Certificate for:

Patent No.:	**5,809,336**
Issued:	**Sep. 15, 1998**
Appl. No.:	**08/484,918**
Filed:	**Jun. 7, 1995**

Reexamination Certificate C1 5,809,336 issued Dec. 15, 2009

Certificate of Correction issued May 22, 2007.

Related U.S. Application Data

(62) Division of application No. 07/389,334, filed on Aug. 3, 1989, now Pat. No. 5,440,749.

(51) **Int. Cl.**

G06F 7/76	(2006.01)
G06F 7/48	(2006.01)
G06F 12/08	(2006.01)
G06F 7/78	(2006.01)
G06F 9/30	(2006.01)
G06F 9/32	(2006.01)
G06F 15/76	(2006.01)
G06F 15/78	(2006.01)
G06F 7/52	(2006.01)
G06F 9/38	(2006.01)
G06F 7/58	(2006.01)

(52) **U.S. Cl.** **710/25**; 711/E12.02; 712/E9.016; 712/E9.028; 712/E9.046; 712/E9.055; 712/E9.057; 712/E9.058; 712/E9.062; 712/E9.078; 712/E9.08; 712/E9.081

(58) **Field of Classification Search** ..... None
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,348,743	A	9/1982	Dozier
4,691,124	A	9/1987	Ledzius et al.
4,766,567	A	8/1988	Kato
4,853,841	A	8/1989	Richter
4,931,748	A	6/1990	McDermott et al.
5,809,336	A	9/1998	Moore et al.

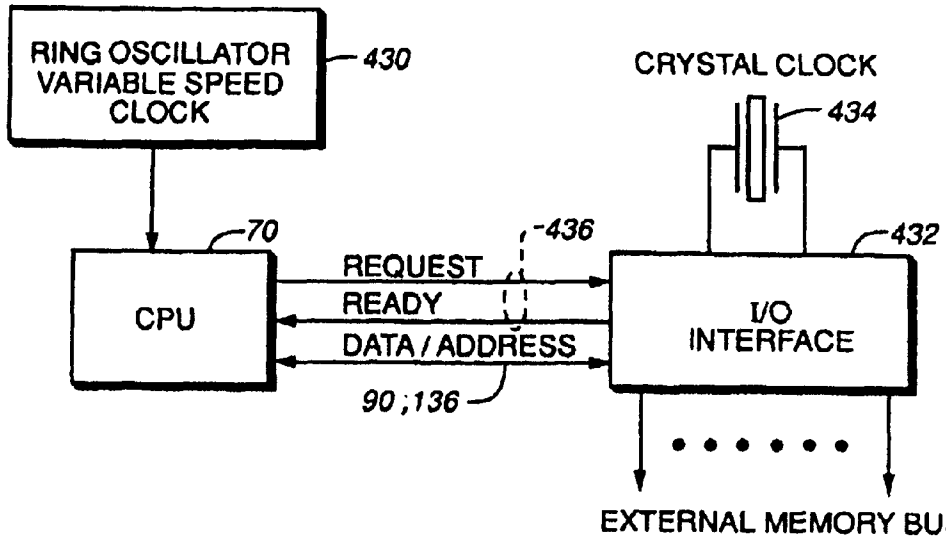
OTHER PUBLICATIONS

U.S. Patent No. 5,809,336, as certified by Ex Parte Reexamination Certificate (7235th) U.S. 5,809,336 C1, issued Dec. 15, 2009, 51 pages.
In re Recreative Technologies Corp., 83 F.3d 1394, 38 USPQ 2.d 1776 (Fed. Cir. 1996), 6 pages.

Primary Examiner—B. James Peikari

(57) **ABSTRACT**

A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and the ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.



EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

NO AMENDMENTS HAVE BEEN MADE TO THE PATENT

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claims **1**, **2**, **6**, **7** and **9-16** is confirmed.

Claims **3-5** and **8** were previously cancelled.

* * * * *

US005530890A

United States Patent [19]

Moore et al.

[11] Patent Number: 5,530,890

[45] Date of Patent: Jun. 25, 1996

[54] **HIGH PERFORMANCE, LOW COST MICROPROCESSOR**

[75] Inventors: **Charles H. Moore**, Woodside; **Russell H. Fish, III**, Mt. View, both of Calif.

[73] Assignee: **Nanotronics Corporation**, Eagle Point, Oreg.

[21] Appl. No.: **480,206**

[22] Filed: **Jun. 7, 1995**

Related U.S. Application Data

[62] Division of Ser. No. 389,334, Aug. 3, 1989, Pat. No. 5,440,749.

[51] **Int. Cl.**[6] **G06F 9/22**

[52] **U.S. Cl.** **395/800**; 364/931; 364/925.6; 364/937.1; 364/965.4; 364/232.8; 364/244.3

[58] **Field of Search** 395/375, 500, 395/775, 800

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,603,934	9/1971	Heath	395/181
4,003,033	1/1977	O'Keefe et al.	395/287
4,037,090	7/1977	Raymond	364/706
4,042,972	8/1977	Grunes et al.	395/375
4,050,058	9/1977	Garlic	395/800
4,067,058	1/1978	Derchak	395/740
4,079,455	3/1978	Ozga	395/800
4,110,822	8/1978	Porter	395/375
4,125,871	11/1978	Martin	395/550
4,128,873	12/1978	Lamiaux	395/183.06
4,253,785	3/1981	Chamberlin	375/375
4,354,228	10/1982	Moore et al.	395/800
4,376,977	3/1983	Brunshorst	395/375
4,382,279	5/1983	Mgon	395/800
4,403,303	9/1983	Howes et al.	395/500
4,450,519	5/1984	Guttag et al.	395/800
4,463,421	7/1984	Laws	395/325
4,538,239	8/1985	Magar	364/759

(List continued on next page.)

OTHER PUBLICATIONS

C. Whitby–Strevans, "The transputer", *The 12th Annual International Symposium on Computer Architecture, Conference Proceeings,* Jun. 17–19, 1985, pp. 292–300.

D. W. Best et al., "An Advanced–Architecture CMOS/SOS Microprocessor", *IEEE Micro,* vol. 2, No. 3, Aug. 1982, pp. 11–25.

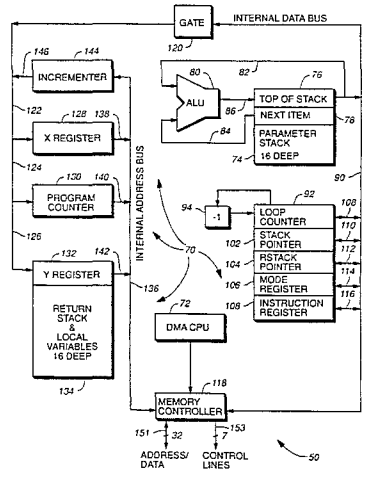
Primary Examiner—David Y. Eng

Attorney, Agent, or Firm—Cooley Godward Castro Huddleson & Tatum

[57] **ABSTRACT**

A microprocessor (**50**) includes a main central processing unit (CPU) (**70**) and a separate direct memory access (DMA) CPU (**72**) in a single integrated circuit making up the microprocessor (**50**). The main CPU (**70**) has a first 16 deep push down stack (**74**), which has a top item register (**76**) and a next item register (**78**), respectively connected to provide inputs to an arithmetic logic unit (ALU) (**80**) by lines (**82**) and (**84**). An output of the ALU (**80**) is connected to the top item register (**76**) by line (**86**). The output of the top item register at (**82**) is also connected by line (**88**) to an internal data bus (**90**). A loop counter (**92**) is connected to a decrementer (**94**) by lines (**96**) and (**98**). The loop counter (**92**) is bidirectionally connected to the internal data bus (**90**) by line (**100**). Stack pointer (**102**), return stack pointer (**104**), mode register (**106**) and instruction register (**108**) are also connected to the internal data bus (**90**) by lines (**110**), (**112**), (**114**) and (**116**), respectively. The internal data bus (**90**) is connected to memory controller (**118**) and to gate (**120**). The gate (**120**) provides inputs on lines (**122**), (**124**), and (**126**) to X register (**128**), program counter (**130**) and Y register (**132**) of return push down stack (**134**). The X register (**128**), program counter (**130**) and Y register (**132**) provide outputs to internal address bus (**136**) on lines (**138**), (**140**) and (**142**). The internal address bus provides inputs to the memory controller (**118**) and to an incrementer (**144**). The incrementer (**144**) provides inputs to the X register, program counter and Y register via lines (**146**), (**122**), (**124**) and (**126**). The DMA CPU (**72**) provides inputs to the memory controller (**118**) on line (**148**). The memory controller (**118**) is connected to a RAM by address/data bus (**150**) and control lines (**152**).

10 Claims, 19 Drawing Sheets



U.S. PATENT DOCUMENTS

4,541,045	9/1985	Kromer	395/375
4,562,537	12/1985	Barnett et al.	395/375
4,577,282	3/1986	Candel et al.	395/800
4,607,332	8/1986	Goldberg	395/375
4,626,988	12/1986	George et al.	395/375
4,649,471	3/1987	Briggs	395/325
4,665,495	5/1987	Thaden	345/185
4,709,329	11/1987	Hecker	395/275
4,713,749	12/1987	Magar et al.	395/375
4,714,994	12/1987	Oklobdzija et al.	395/375
4,720,812	1/1988	Kao et al.	395/700
4,772,888	9/1988	Kimura	340/825.5
4,777,591	10/1988	Chang et al.	395/800
4,787,032	11/1988	Culley et al.	395/725
4,803,621	2/1989	Kelly	395/400
4,860,198	8/1989	Takenaka	395/307
4,870,562	9/1989	Kimoto	395/550
4,931,986	6/1990	Daniel et al.	395/550
5,036,460	7/1991	Takahira	395/425
5,070,451	12/1991	Moore et al.	395/375
5,127,091	6/1992	Bonfarah	395/375

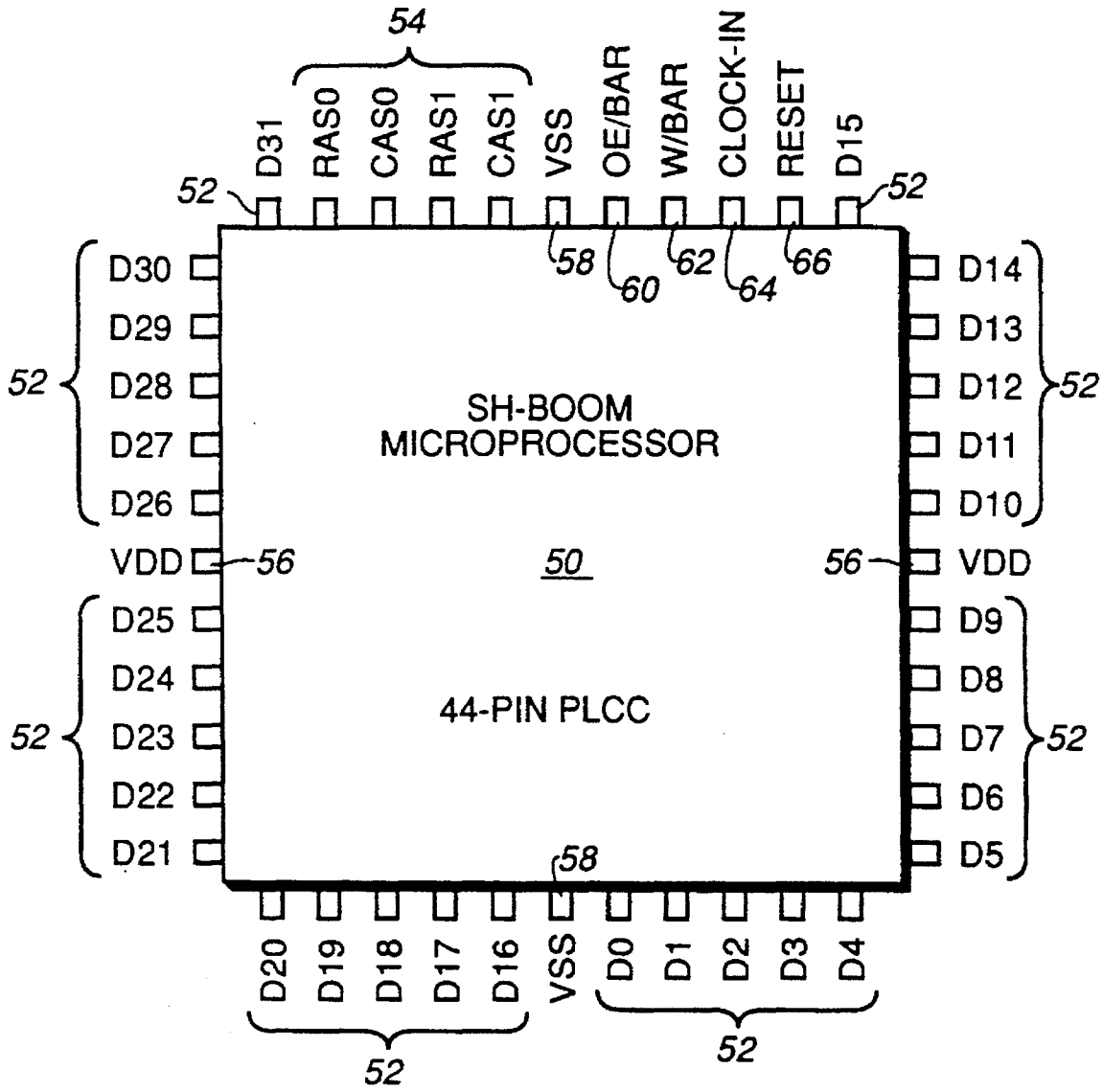

54
D31
RAS0
CAS0
RAS1
CAS1
VSS
OE/BAR
W/BAR
CLOCK-IN
RESET
D15
52
58
60
62
64
66
D30
D29
D28
D27
D26
VDD
D25
D24
D23
D22
D21
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
SH-BOOM
MICROPROCESSOR
50
44-PIN PLCC
56
D20
D19
D18
D17
D16
D0
D1
D2
D3
D4

FIG._1

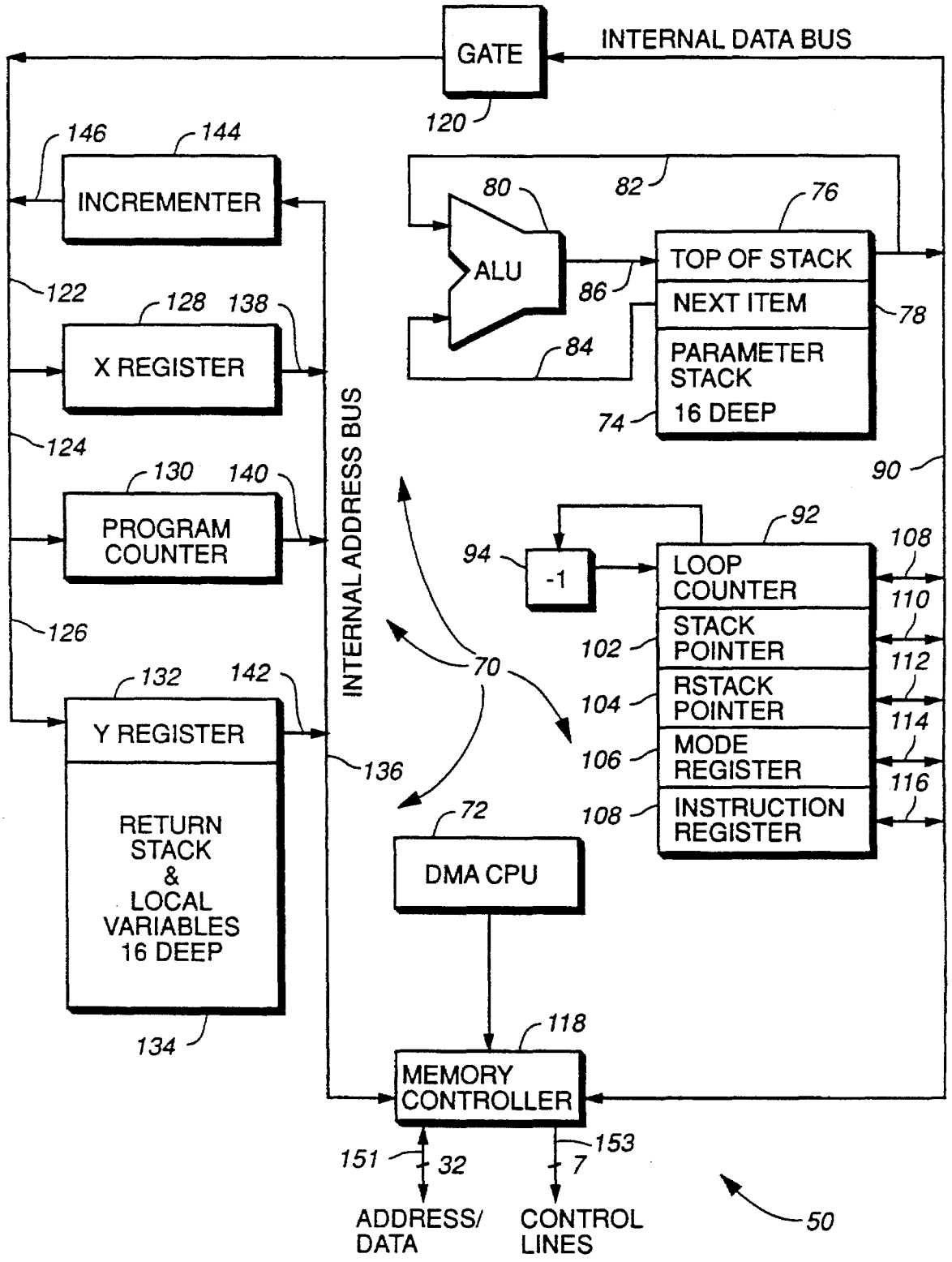

GATE
INTERNAL DATA BUS
120
146
144
INCREMENTER
80
82
76
ALU
TOP OF STACK
NEXT ITEM
PARAMETER STACK
16 DEEP
86
84
74
78
122
128
138
X REGISTER
124
130
140
PROGRAM COUNTER
126
INTERNAL ADDRESS BUS
90
92
94
-1
LOOP COUNTER
STACK POINTER
RSTACK POINTER
MODE REGISTER
INSTRUCTION REGISTER
108
110
112
114
116
102
104
106
108
70
132
142
Y REGISTER
136
RETURN STACK & LOCAL VARIABLES 16 DEEP
134
72
DMA CPU
118
MEMORY CONTROLLER
151
32
153
7
ADDRESS/ DATA
CONTROL LINES
50

FIG._2

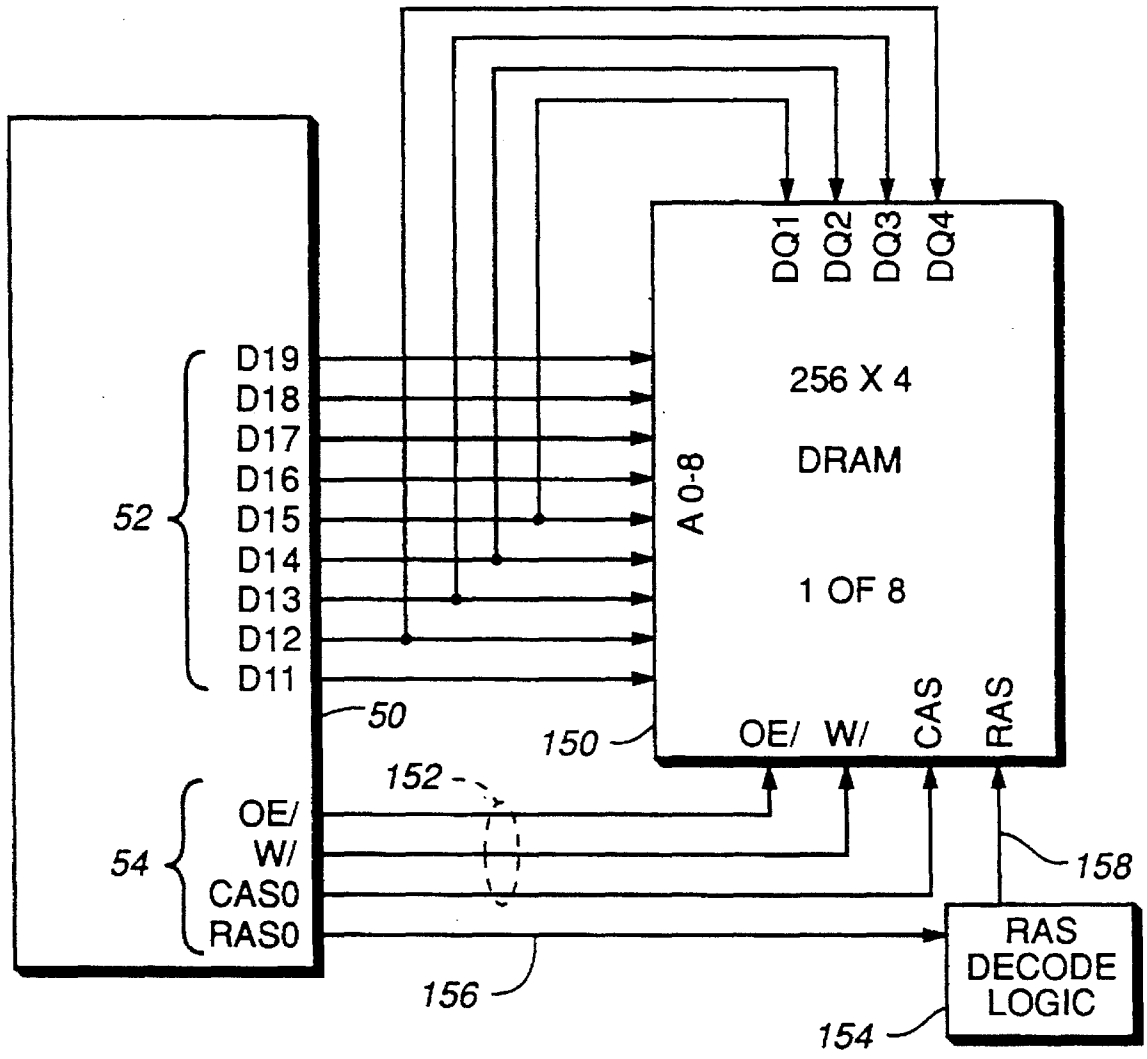

DQ1
DQ2
DQ3
DQ4
256 X 4
DRAM
1 OF 8
A 0-8
OE/
W/
CAS
RAS
D19
D18
D17
D16
D15
D14
D13
D12
D11
52
50
150
152
54
OE/
W/
CAS0
RAS0
156
158
RAS
DECODE
LOGIC
154

FIG._3

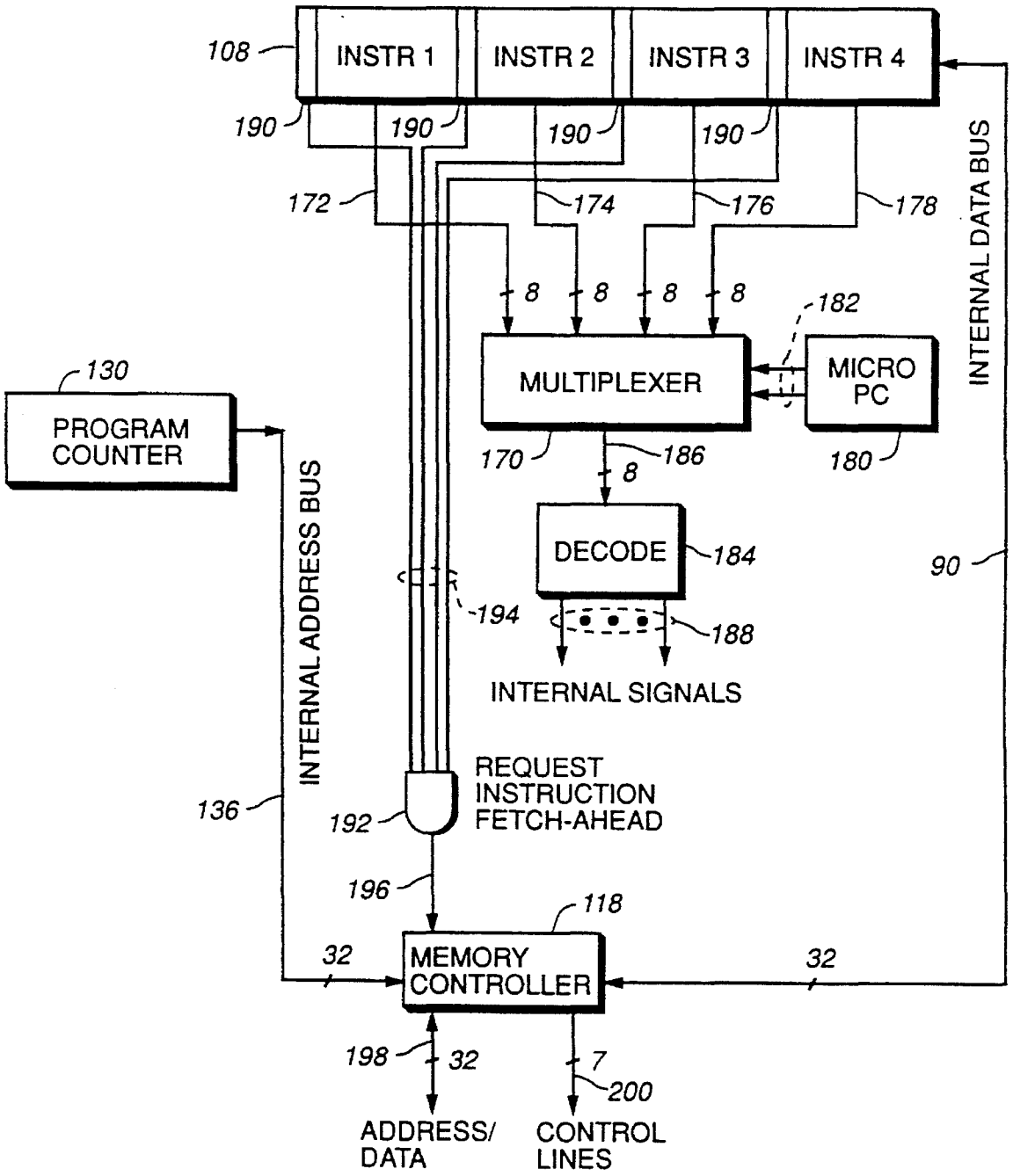

108
INSTR 1
INSTR 2
INSTR 3
INSTR 4
190
190
190
190
172
174
176
178
8
8
8
8
182
MULTIPLEXER
MICRO PC
INTERNAL DATA BUS
130
PROGRAM COUNTER
170
186
180
8
DECODE
184
90
194
188
INTERNAL SIGNALS
INTERNAL ADDRESS BUS
REQUEST INSTRUCTION FETCH-AHEAD
136
192
196
118
32
MEMORY CONTROLLER
32
198
32
7
200
ADDRESS/ DATA
CONTROL LINES

FIG._4

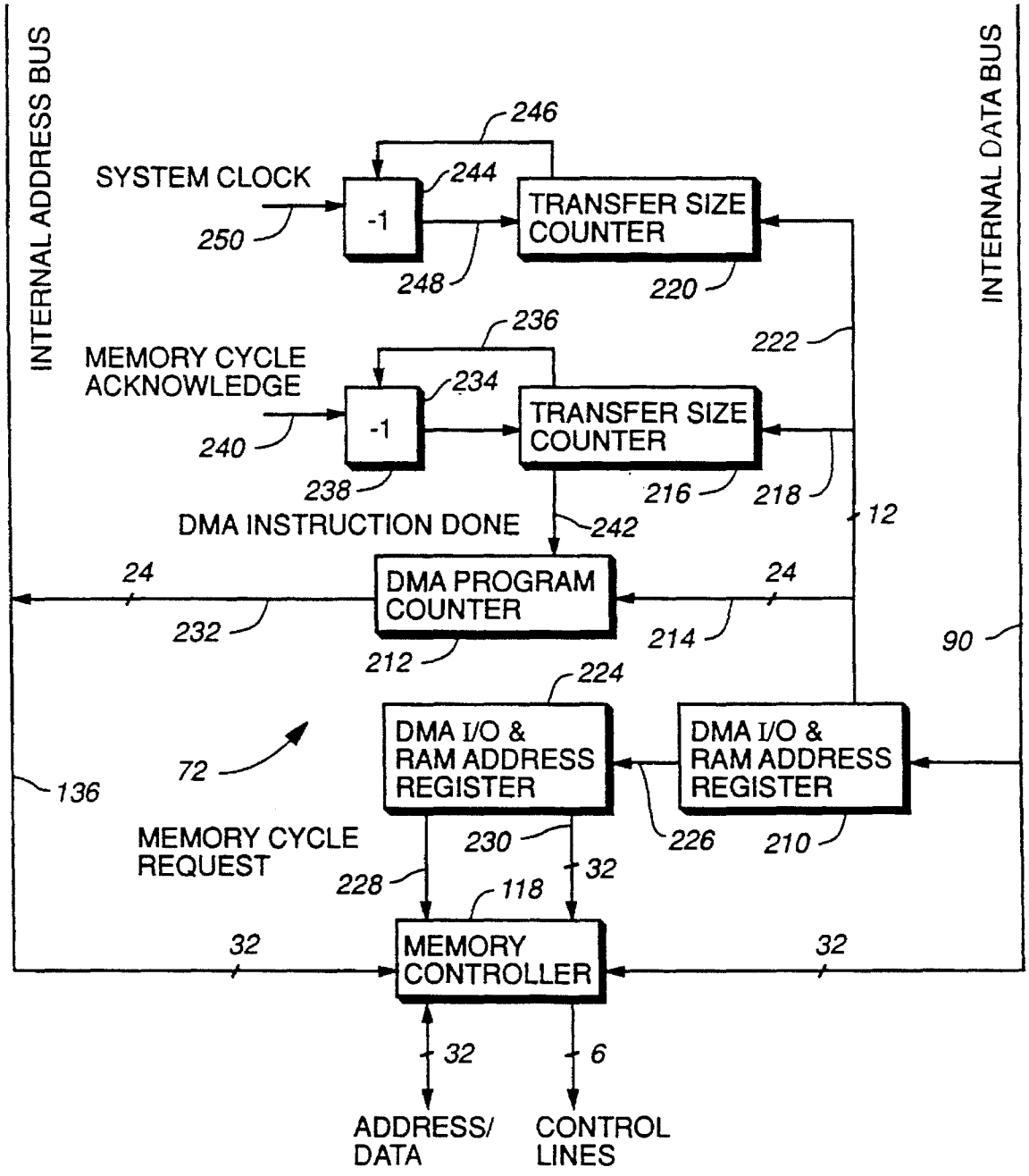

INTERNAL ADDRESS BUS
INTERNAL DATA BUS
SYSTEM CLOCK
246
244
-1
TRANSFER SIZE COUNTER
250
248
220
MEMORY CYCLE ACKNOWLEDGE
236
234
-1
TRANSFER SIZE COUNTER
240
238
216
218
222
12
DMA INSTRUCTION DONE
242
24
DMA PROGRAM COUNTER
24
232
214
212
90
224
DMA I/O & RAM ADDRESS REGISTER
DMA I/O & RAM ADDRESS REGISTER
72
136
MEMORY CYCLE REQUEST
230
226
210
228
32
118
32
MEMORY CONTROLLER
32
32
6
ADDRESS/ DATA
CONTROL LINES

FIG._5

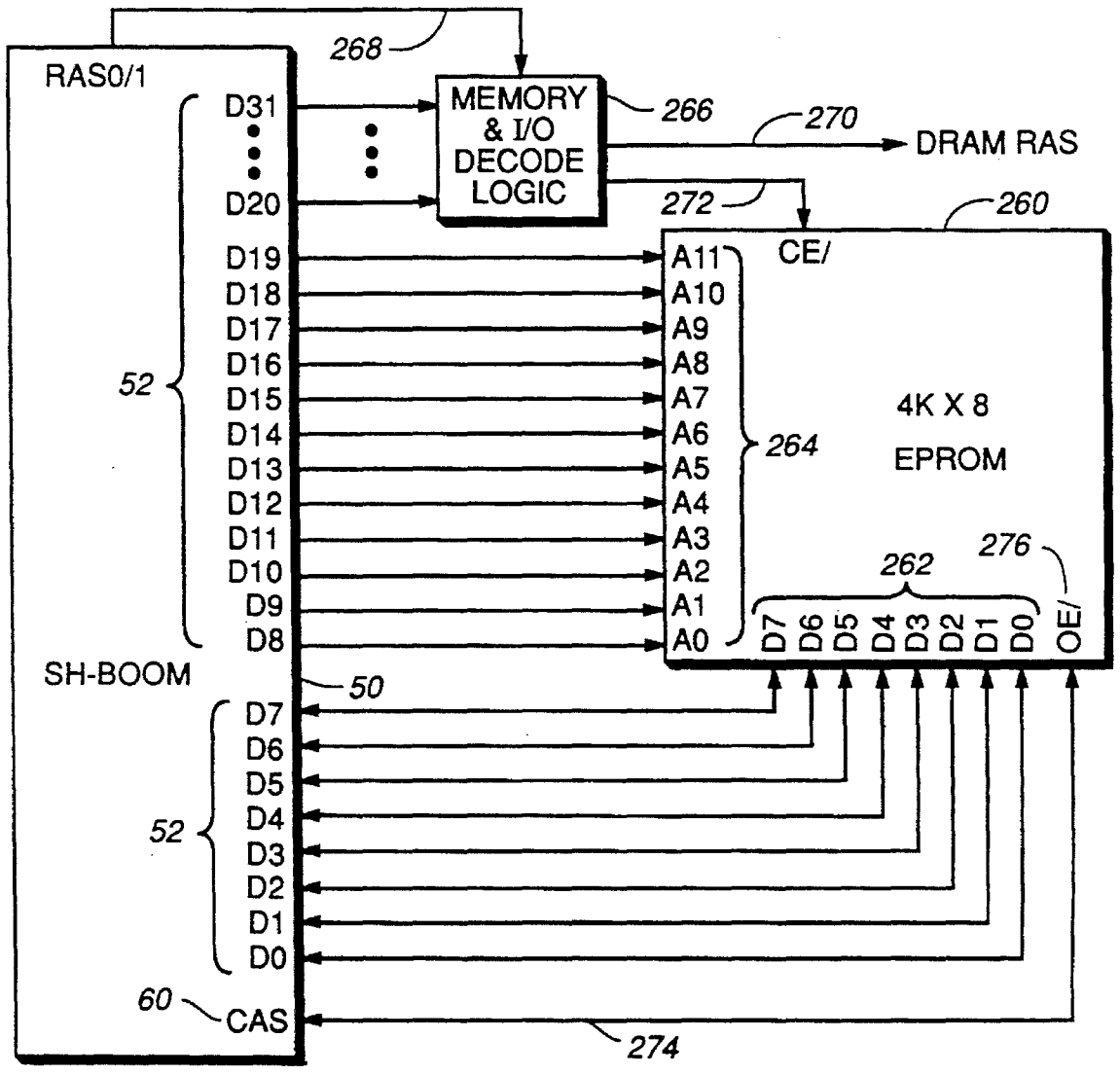

268
RAS0/1
D31
D20
MEMORY & I/O DECODE LOGIC
266
270
DRAM RAS
272
260
D19
D18
D17
D16
D15
D14
D13
D12
D11
D10
D9
D8
52
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
CE/
4K X 8
EPROM
264
276
262
D7
D6
D5
D4
D3
D2
D1
D0
OE/
SH-BOOM
50
52
60
CAS
274

FIG._6

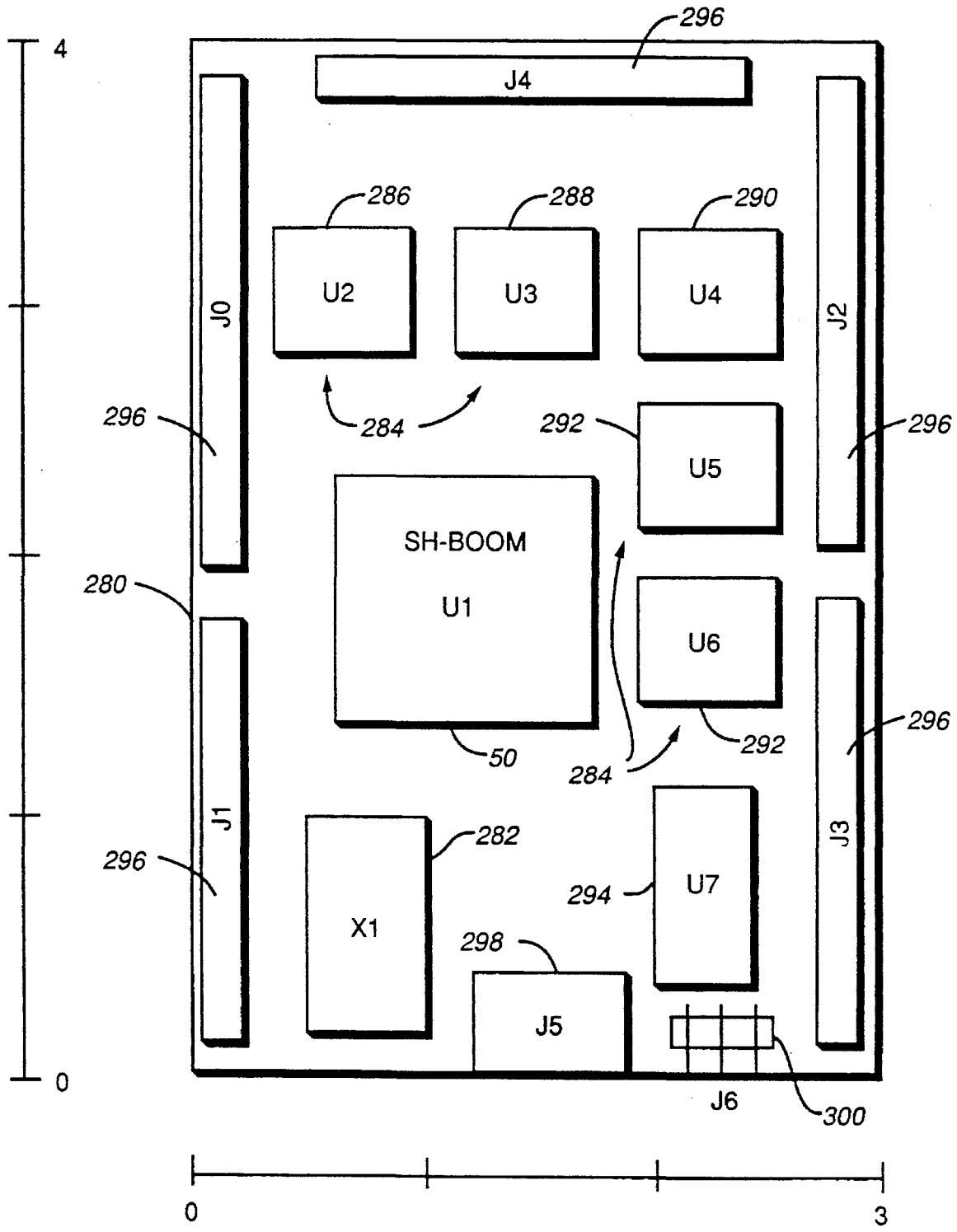

296
J4
J0
J2
286
288
290
U2
U3
U4
284
296
292
296
U5
SH-BOOM
U1
280
U6
296
50
284
292
J1
J3
296
282
294
U7
X1
298
J5
J6
300
4
0
0
3

FIG._7

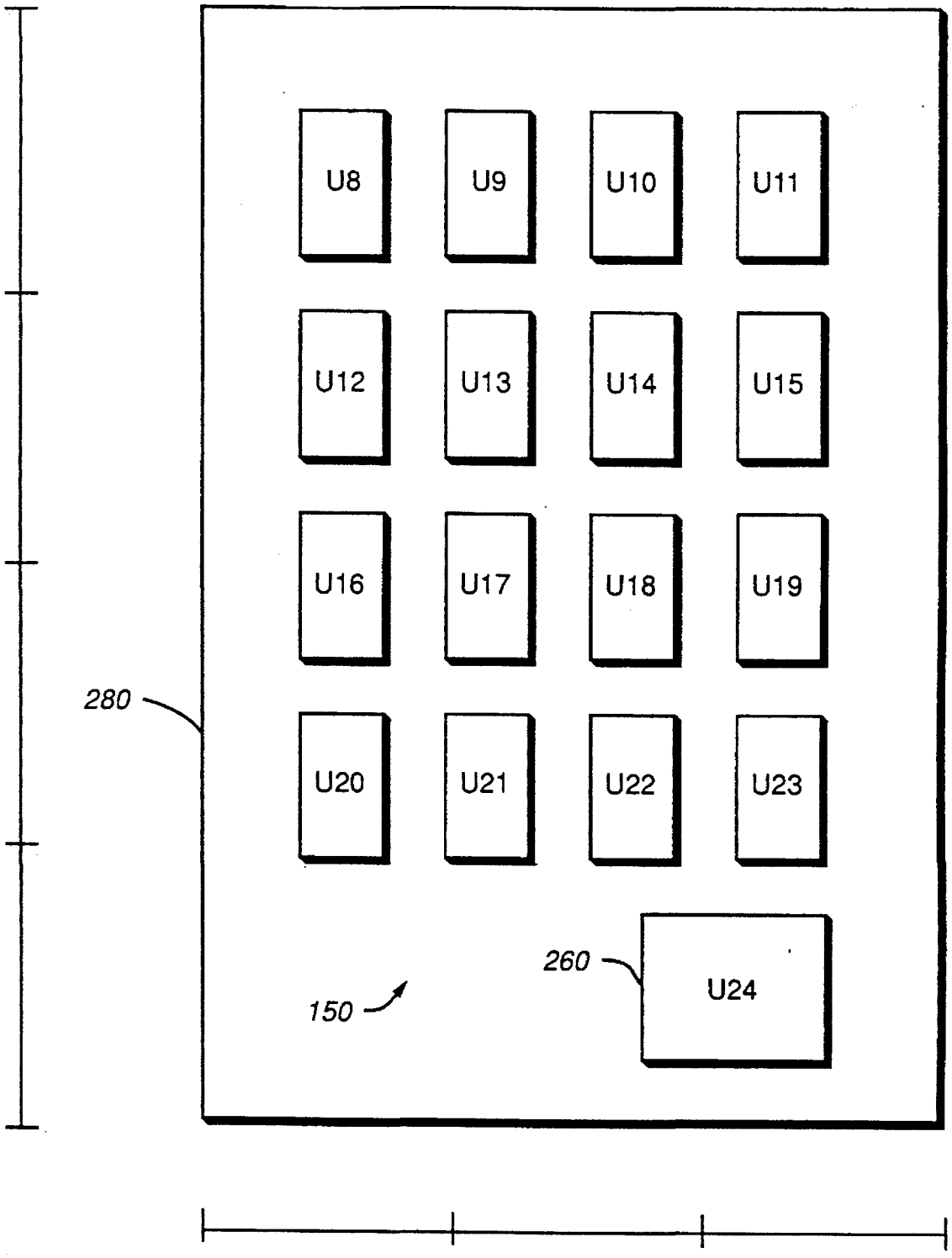

U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
280
U20
U21
U22
U23
260
U24
150

FIG._8

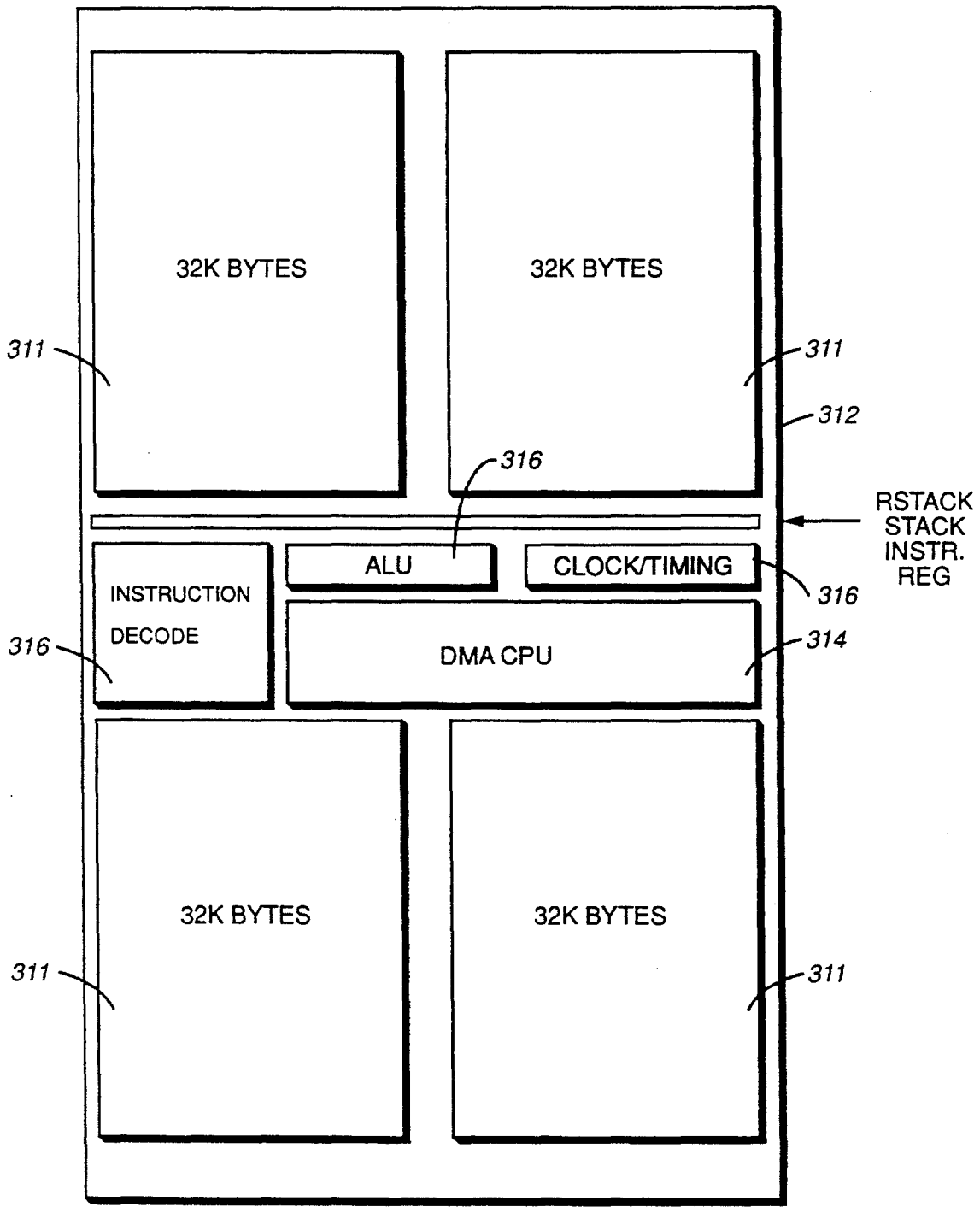

32K BYTES
32K BYTES
311
311
312
316
RSTACK
STACK
INSTR.
REG
ALU
CLOCK/TIMING
316
INSTRUCTION
DECODE
316
DMA CPU
314
32K BYTES
32K BYTES
311
311

FIG._9

FIG._10

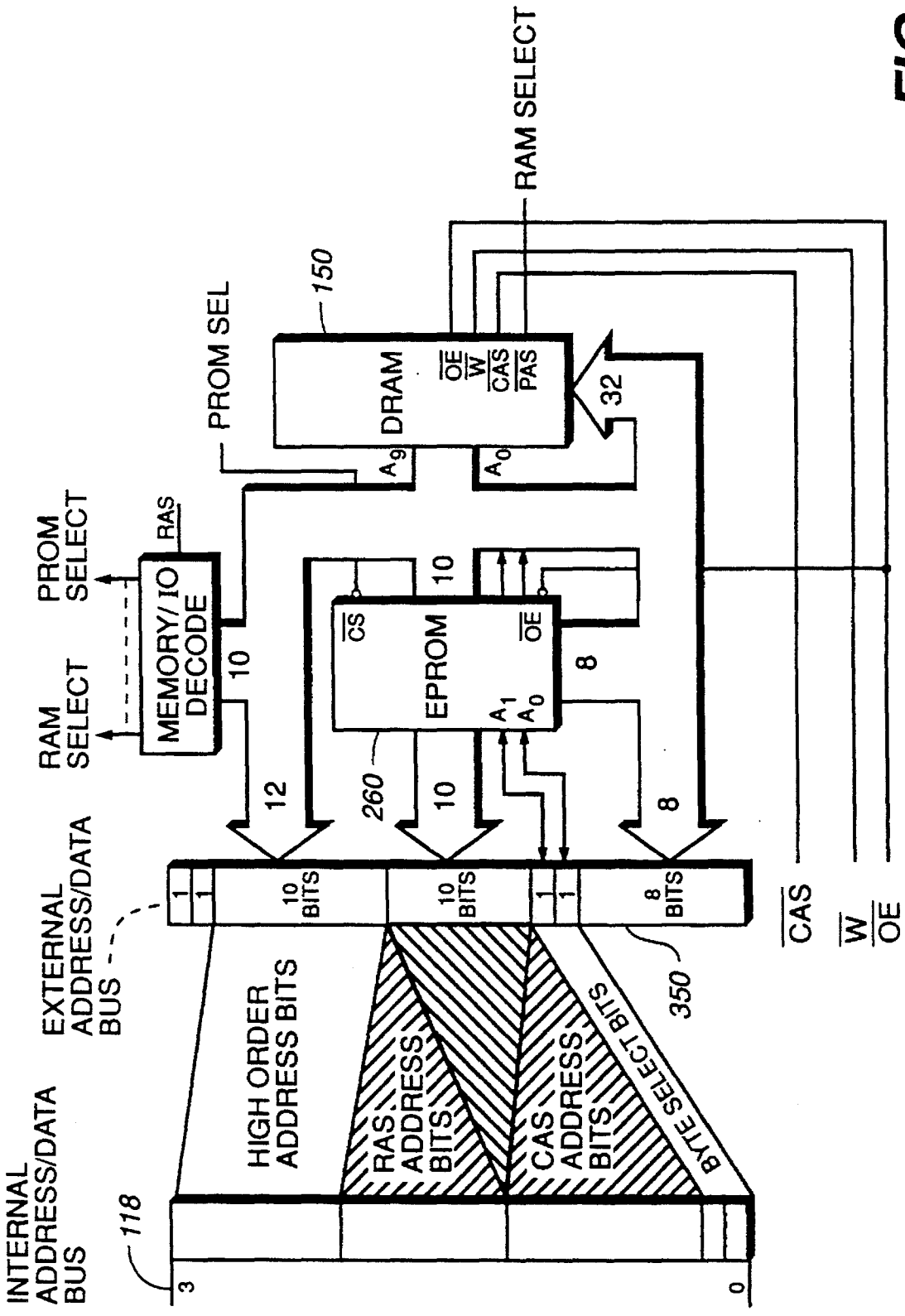
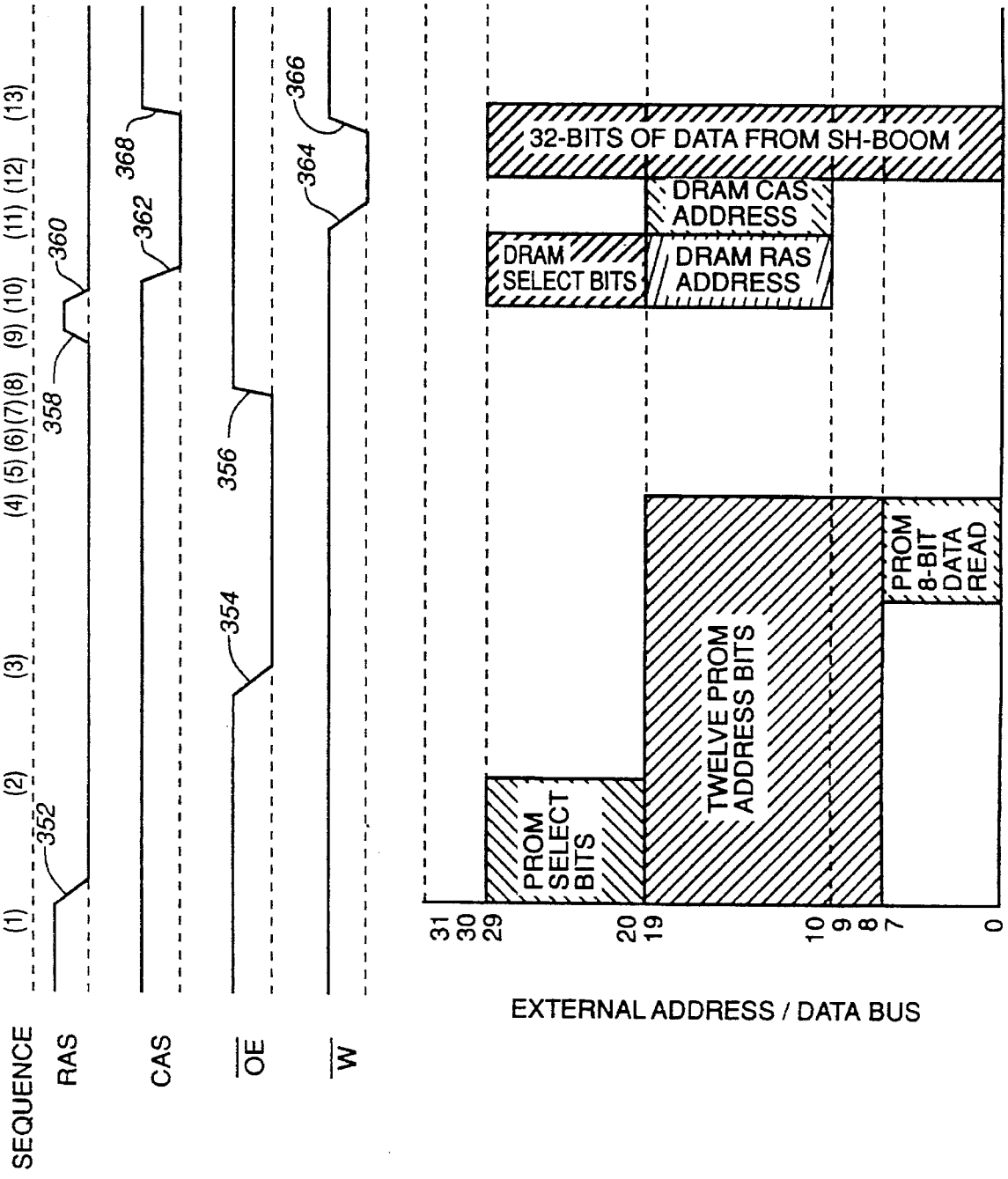
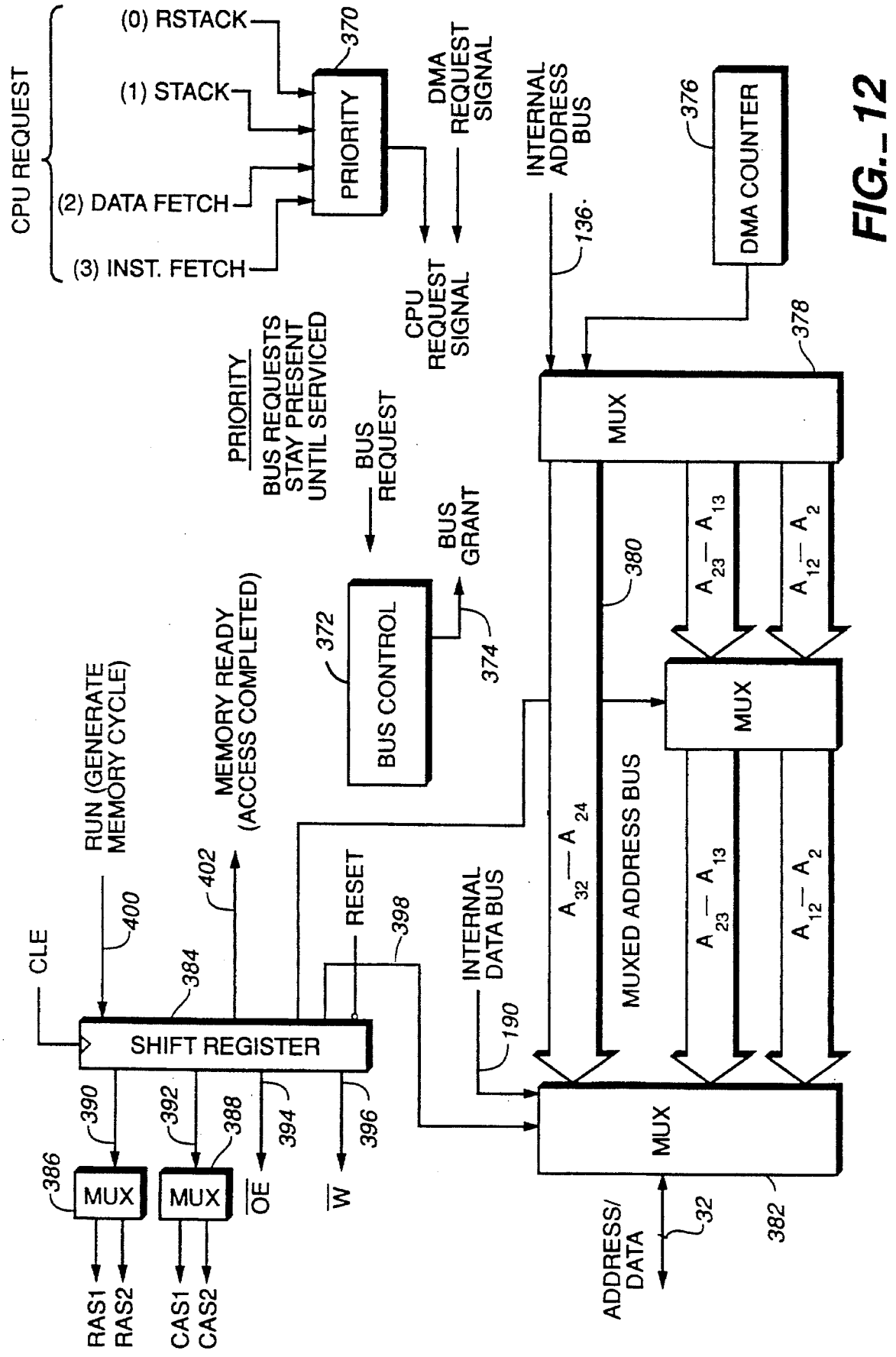

RAM SELECT
150
PROM SEL
DRAM
OE
W
CAS
RAS
32
A9
A0
PROM SELECT
RAS
MEMORY/IO DECODE
10
RAM SELECT
CS
EPROM
OE
A1
A0
10
8
12
260
10
8
EXTERNAL ADDRESS/DATA BUS
1
1
10 BITS
10 BITS
1
1
8 BITS
CAS
W
OE
350
HIGH ORDER ADDRESS BITS
RAS ADDRESS BITS
CAS ADDRESS BITS
BYTE SELECT BITS
INTERNAL ADDRESS/DATA BUS
118
3
0

FIG._11


SEQUENCE
RAS
CAS
OE
W
(1)
(2)
(3)
(4) (5) (6) (7) (8)
(9) (10)
(11) (12)
(13)
352
354
356
358
360
362
364
366
368
32-BITS OF DATA FROM SH-BOOM
DRAM CAS ADDRESS
DRAM SELECT BITS
DRAM RAS ADDRESS
PROM SELECT BITS
TWELVE PROM ADDRESS BITS
PROM 8-BIT DATA READ
31 30 29
20 19
10 9 8 7
0
EXTERNAL ADDRESS / DATA BUS


CPU REQUEST
(0) RSTACK
(1) STACK
(2) DATA FETCH
(3) INST. FETCH
PRIORITY
370
DMA REQUEST SIGNAL
CPU REQUEST SIGNAL
INTERNAL ADDRESS BUS
136
DMA COUNTER
376
FIG._12
PRIORITY
BUS REQUESTS STAY PRESENT UNTIL SERVICED
BUS REQUEST
BUS GRANT
MUX
378
380
BUS CONTROL
372
374
MEMORY READY (ACCESS COMPLETED)
RUN (GENERATE MEMORY CYCLE)
400
402
RESET
398
CLE
384
SHIFT REGISTER
INTERNAL DATA BUS
190
MUXED ADDRESS BUS
A32 — A24
A23 — A13
A12 — A2
390
392
388
394
396
386
MUX
OE
W
RAS1
RAS2
CAS1
CAS2
ADDRESS/ DATA
32
382

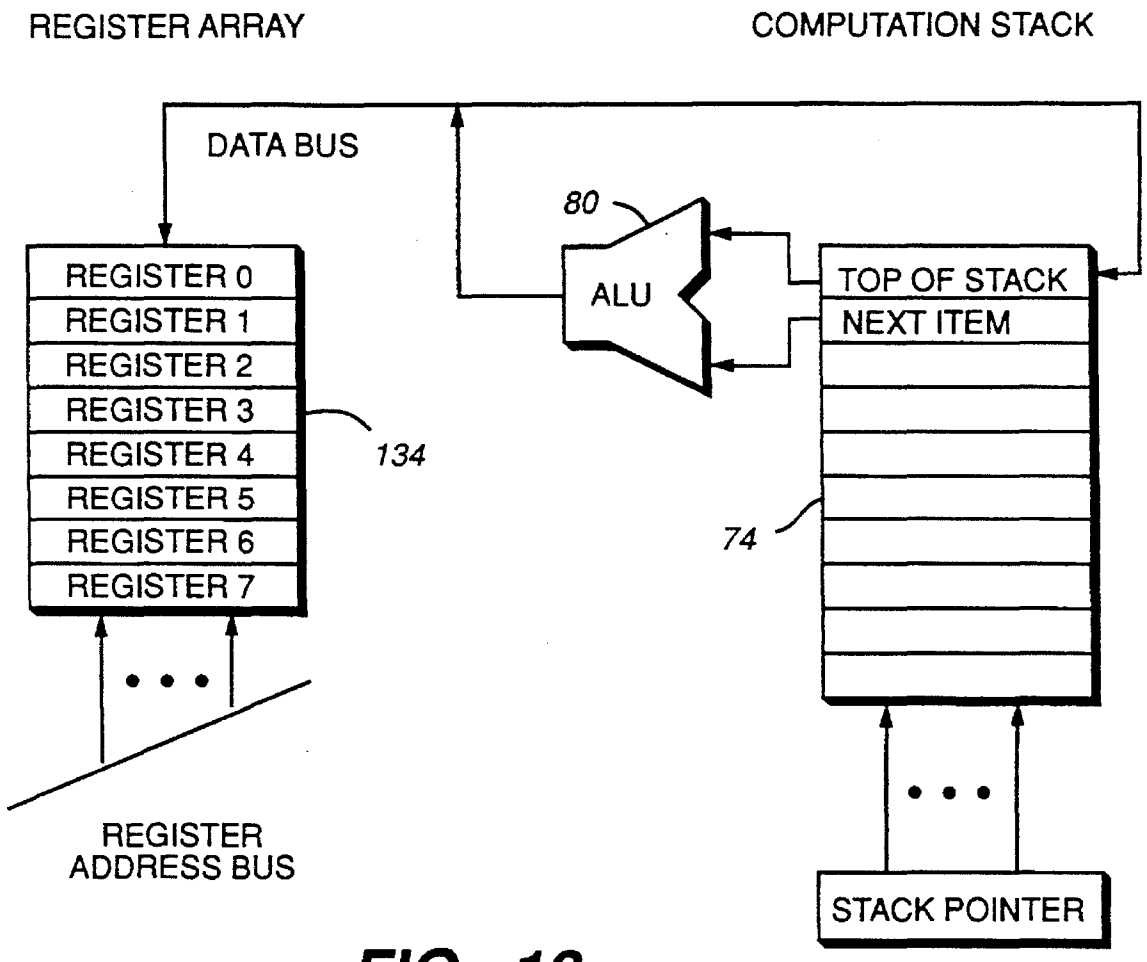

REGISTER ARRAY
COMPUTATION STACK
DATA BUS
80
ALU
REGISTER 0
REGISTER 1
REGISTER 2
REGISTER 3
REGISTER 4
REGISTER 5
REGISTER 6
REGISTER 7
134
TOP OF STACK
NEXT ITEM
74
REGISTER
ADDRESS BUS
STACK POINTER

FIG._13

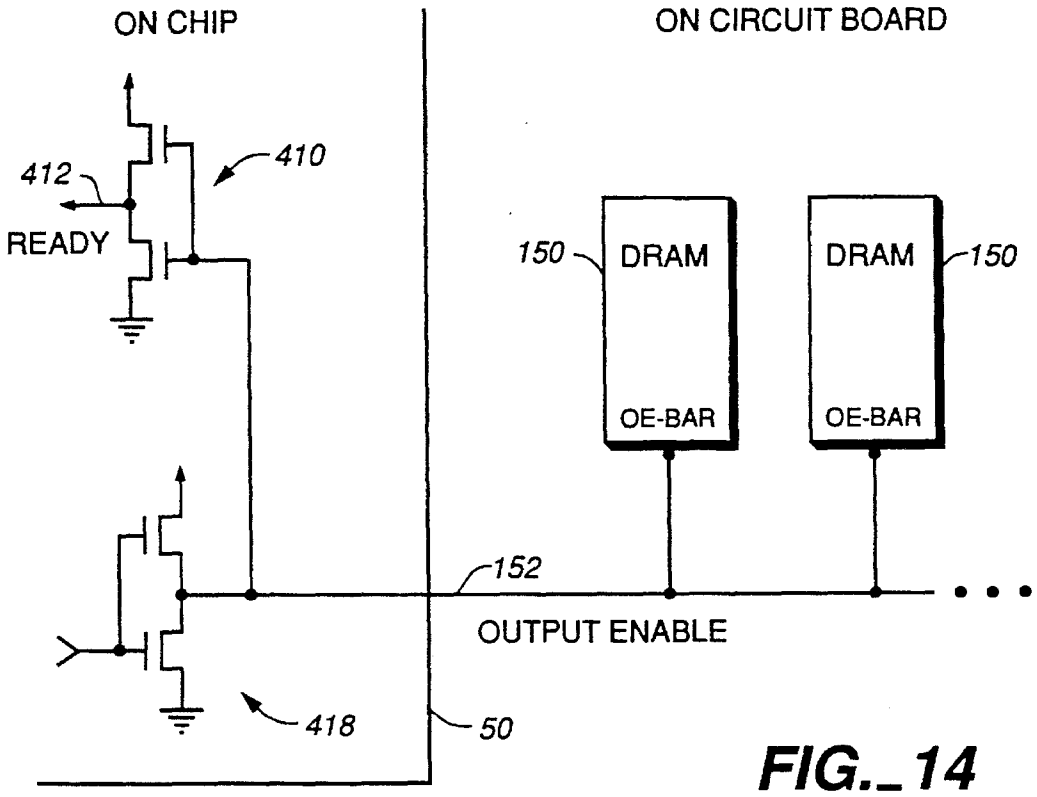

ON CHIP
ON CIRCUIT BOARD
412
410
READY
150
DRAM
OE-BAR
DRAM
150
OE-BAR
152
OUTPUT ENABLE
418
50

FIG._14

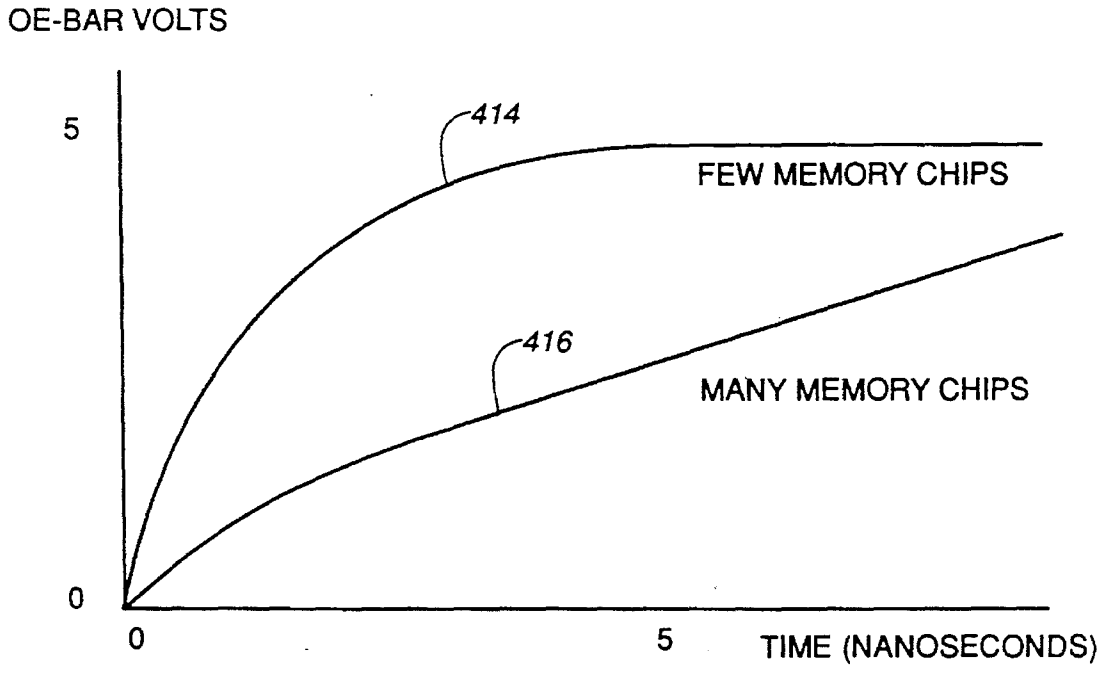

OE-BAR VOLTS
5
414
FEW MEMORY CHIPS
416
MANY MEMORY CHIPS
0
0
5
TIME (NANOSECONDS)

FIG._15

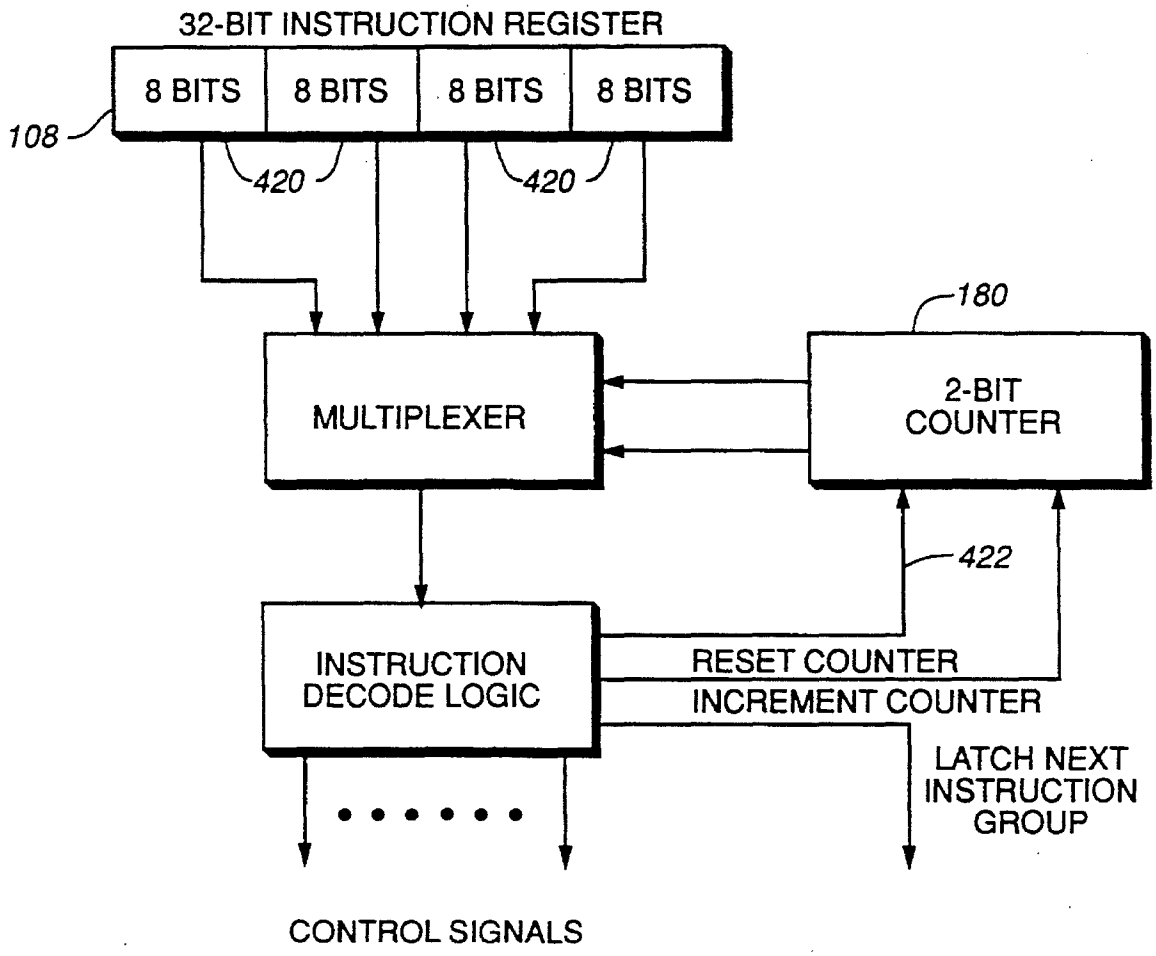

32-BIT INSTRUCTION REGISTER
8 BITS
8 BITS
8 BITS
8 BITS
108
420
420
180
MULTIPLEXER
2-BIT COUNTER
422
INSTRUCTION DECODE LOGIC
RESET COUNTER
INCREMENT COUNTER
LATCH NEXT INSTRUCTION GROUP
CONTROL SIGNALS

FIG._16

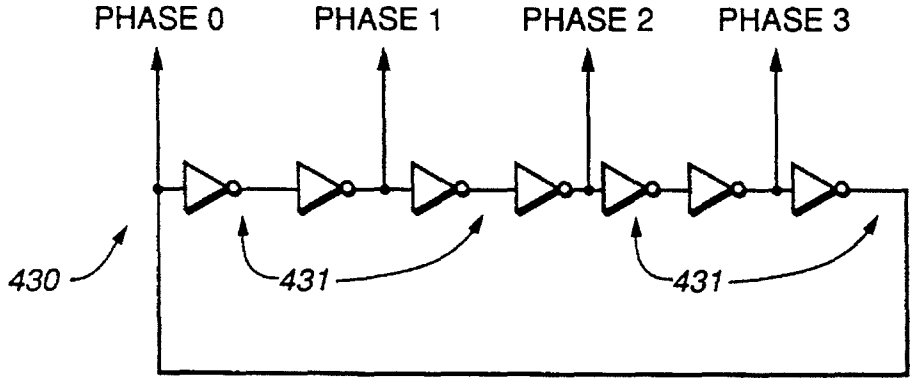

PHASE 0
PHASE 1
PHASE 2
PHASE 3
430
431
431

FIG._18

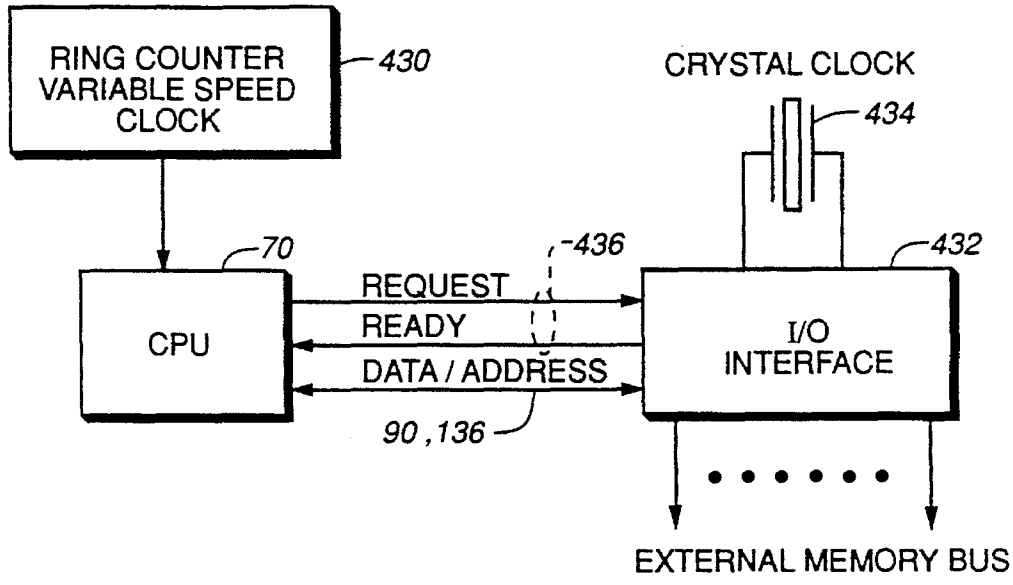

RING COUNTER VARIABLE SPEED CLOCK
430
CRYSTAL CLOCK
434
70
436
432
CPU
REQUEST
READY
DATA / ADDRESS
I/O INTERFACE
90 ,136
EXTERNAL MEMORY BUS

FIG._17

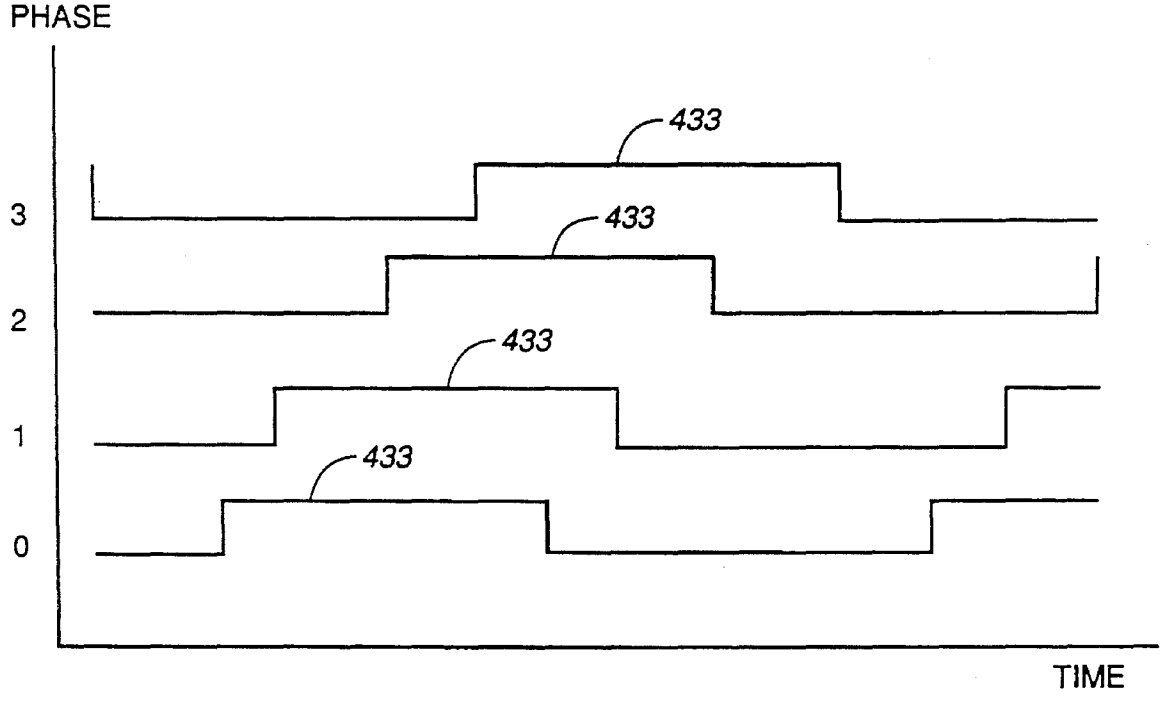

PHASE
433
433
433
433
3
2
1
0
TIME

FIG._19

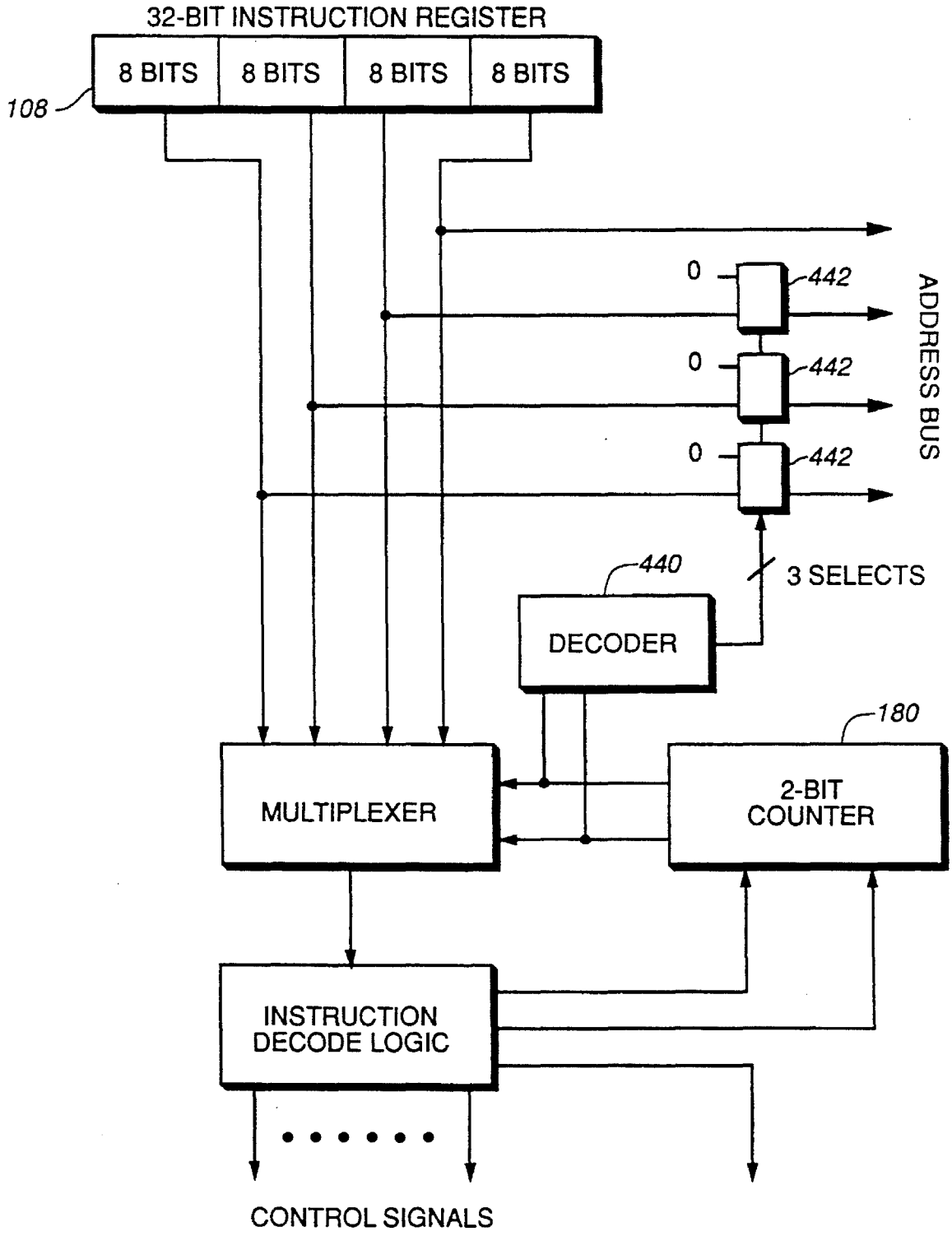

32-BIT INSTRUCTION REGISTER
8 BITS
8 BITS
8 BITS
8 BITS
108
0
442
0
442
0
442
ADDRESS BUS
440
3 SELECTS
DECODER
180
MULTIPLEXER
2-BIT COUNTER
INSTRUCTION DECODE LOGIC
CONTROL SIGNALS

FIG._20

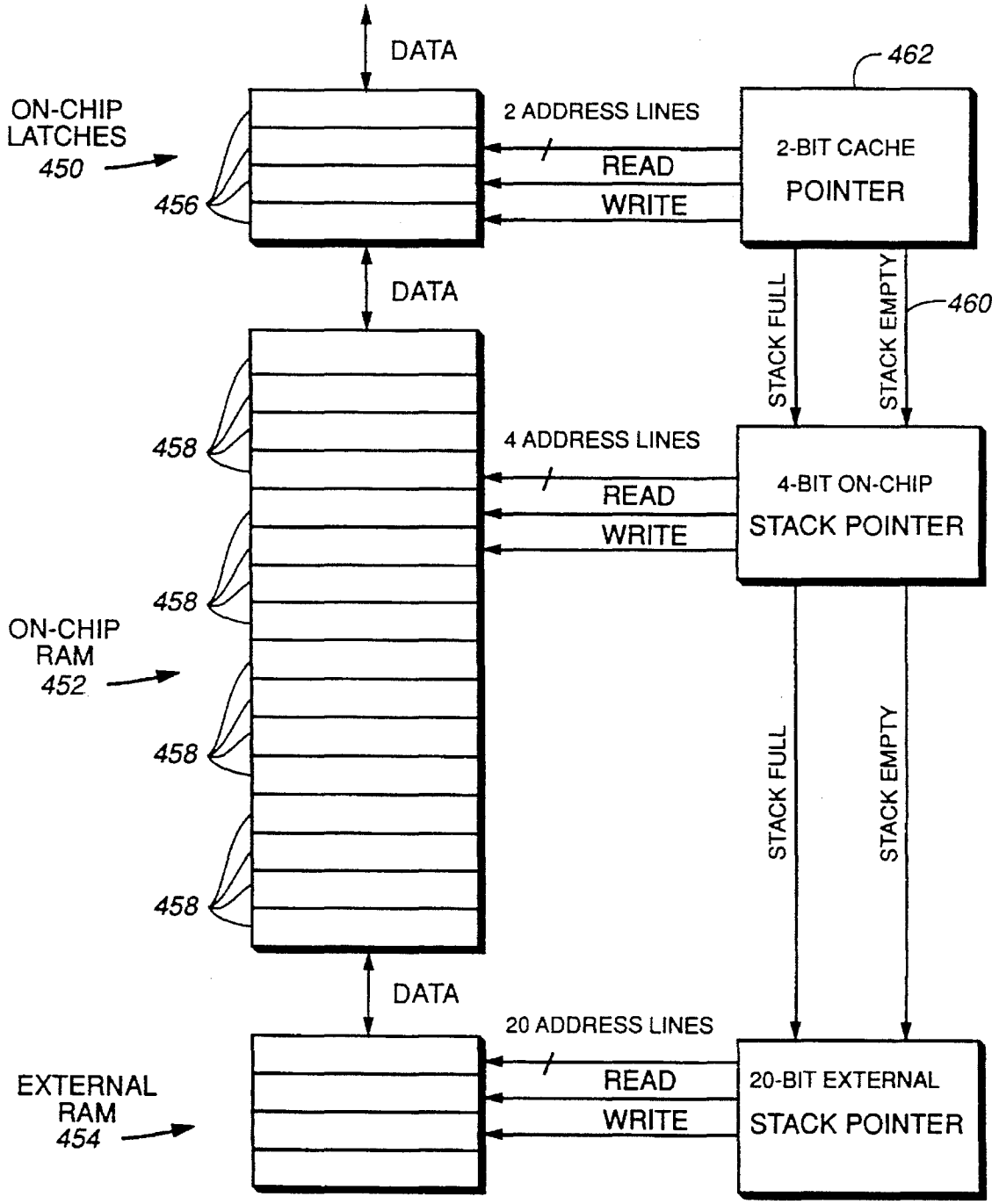

DATA
462
ON-CHIP LATCHES
450
2 ADDRESS LINES
READ
WRITE
2-BIT CACHE POINTER
456
DATA
STACK FULL
STACK EMPTY
460
458
4 ADDRESS LINES
READ
WRITE
4-BIT ON-CHIP STACK POINTER
458
ON-CHIP RAM
452
458
STACK FULL
STACK EMPTY
458
DATA
20 ADDRESS LINES
READ
WRITE
20-BIT EXTERNAL STACK POINTER
EXTERNAL RAM
454

FIG._21

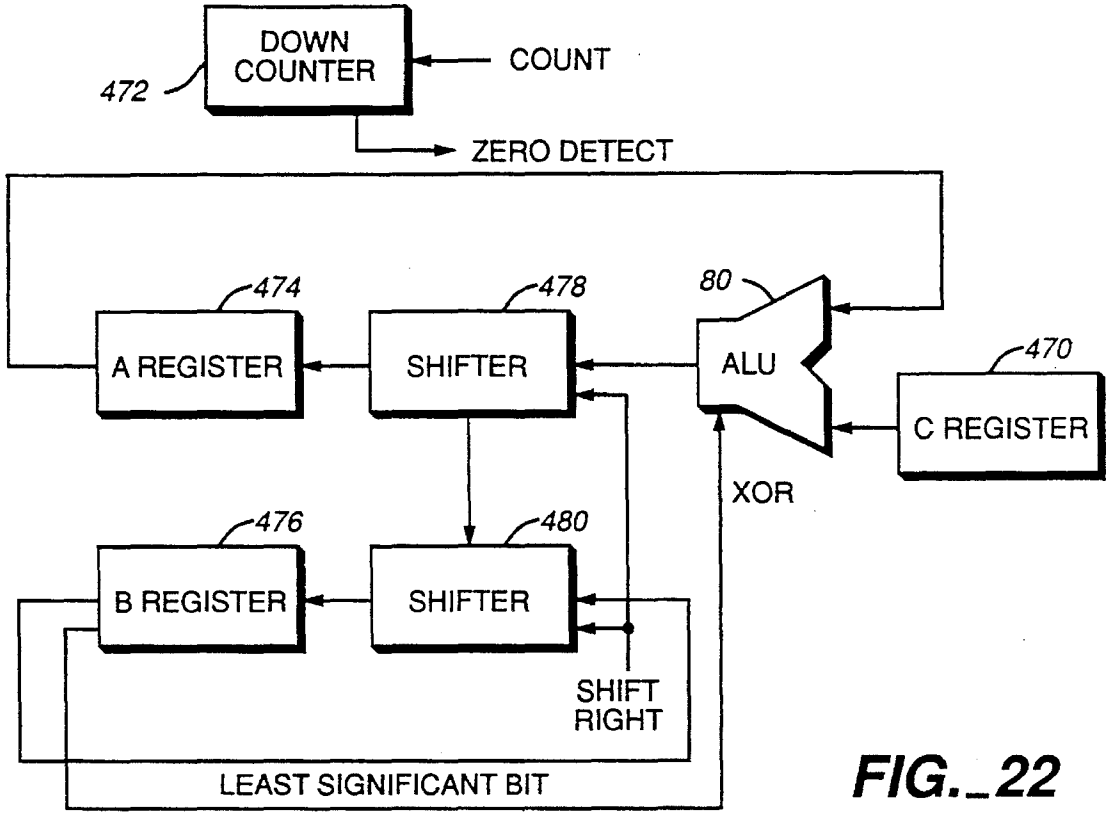

DOWN COUNTER
472
COUNT
ZERO DETECT
474
A REGISTER
478
SHIFTER
80
ALU
470
C REGISTER
XOR
476
B REGISTER
480
SHIFTER
SHIFT RIGHT
LEAST SIGNIFICANT BIT

FIG._22

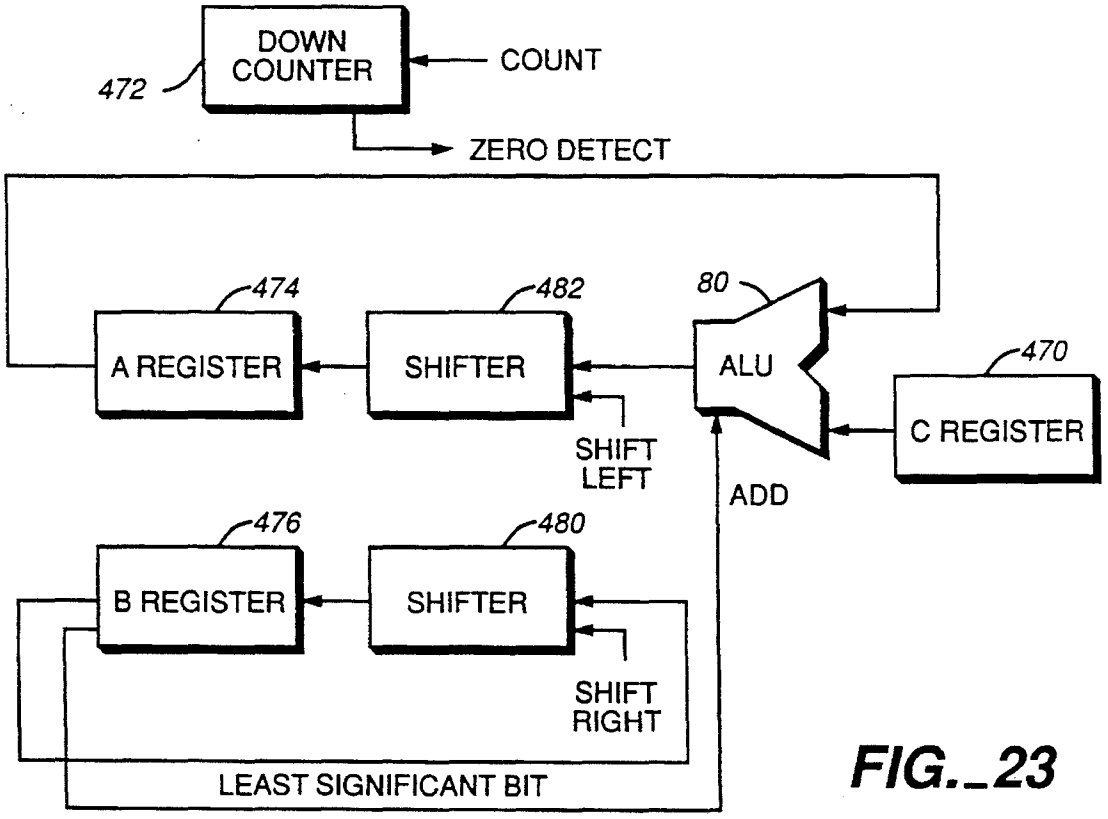

DOWN COUNTER
472
COUNT
ZERO DETECT
474
A REGISTER
482
SHIFTER
80
ALU
470
C REGISTER
SHIFT LEFT
ADD
476
B REGISTER
480
SHIFTER
SHIFT RIGHT
LEAST SIGNIFICANT BIT

FIG._23

HIGH PERFORMANCE, LOW COST MICROPROCESSOR

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a division of U.S. application Ser. No. 07/389,334, filed Aug. 3, 1989, now U.S. Pat. No. 5,440,749.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to a simplified, reduced instruction set computer (RISC) microprocessor. More particularly, it relates to such a microprocessor which is capable of performance levels of, for example, 20 million instructions per second (MIPS) at a price of, for example, 20 dollars.

2. Description of the Prior Art

since the invention of the microprocessor, improvements in its design have taken two different approaches. In the first approach, a brute force gain in performance has been achieved through the provision of greater numbers of faster transistors in the microprocessor integrated circuit and an instruction set of increased complexity. This approach is exemplified by the Motorola 68000 and Intel 80X86 microprocessor families. The trend in this approach is to larger die sizes and packages, with hundreds of pinouts.

More recently, it has been perceived that performance gains can be achieved through comparative simplicity, both in the microprocessor integrated circuit itself and in its instruction set. This second approach provides RISC microprocessors, and is exemplified by the Sun SPARC and the Intel 8960 microprocessors. However, even with this approach as conventionally practiced, the packages for the microprocessor are large, in order to accommodate the large number of pinouts that continue to be employed. A need therefore remains for further simplification of high performance microprocessors.

With conventional high performance microprocessors, fast static memories are required for direct connection to the microprocessors in order to allow memory accesses that are fast enough to keep up with the microprocessors. Slower dynamic random access memories (DRAMs) are used with such microprocessors only in a hierarchical memory arrangement, with the static memories acting as a buffer between the microprocessors and the DRAMs. The necessity to use static memories increases cost of the resulting systems.

Conventional microprocessors provide direct memory accesses (DMA) for system peripheral units through DMA controllers, which may be located on the microprocessor integrated circuit, or provided separately. Such DMA controllers can provide routine handling of DMA requests and responses, but some processing by the main central processing unit (CPU) of the microprocessor is required.

SUMMARY OF THE INVENTION

Accordingly, it is an object of this invention to provide a microprocessor with a reduced pin count and cost compared to conventional microprocessors.

It is another object of the invention to provide a high performance microprocessor that can be directly connected to DRAMs without sacrificing microprocessor speed.

It is a further object of the invention to provide a high performance microprocessor in which DMA does not require use of the main CPU during DMA requests and responses and which provides very rapid DMA response with predictable response times.

The attainment of these and related objects may be achieved through use of the novel high performance, low cost microprocessor herein disclosed. In accordance with one aspect of the invention, a microprocessor system in accordance with this invention has a central processing unit, a dynamic random access memory and a bus connecting the central processing unit to the dynamic random access memory. There is a multiplexing means on the bus between the central processing unit and the dynamic random access memory. The multiplexing means is connected and configured to provide row addresses, column addresses and data on the bus.

In accordance with another aspect of the invention, the microprocessor system has a means connected to the bus for fetching instructions for the central processing unit on the bus. The means for fetching instructions is configured to fetch multiple sequential instructions in a single memory cycle. In a variation of this aspect of the invention, a programmable read only memory containing instructions for the central processing unit is connected to the bus. The means for fetching instructions includes means for assembling a plurality of instructions from the programmable read only memory and storing the plurality of instructions in the dynamic random access memory.

In another aspect of the invention, the microprocessor system includes a central processing unit, a direct memory access processing unit and a memory connected by a bus. The direct memory access processing unit includes means for fetching instructions for the central processing unit and for fetching instructions for the direct memory access processing unit on the bus.

In a further aspect of the invention, the microprocessor system, including the memory, is contained in an integrated circuit. The memory is a dynamic random access memory, and the means for fetching multiple instructions includes a column latch for receiving the multiple instructions.

In still another aspect of the invention, the microprocessor system additionally includes an instruction register for the multiple instructions connected to the means for fetching instructions. A means is connected to the instruction register for supplying the multiple instructions in succession from the instruction register. A counter is connected to control the means for supplying the multiple instructions to supply the multiple instructions in succession. A means for decoding the multiple instructions is connected to receive the multiple instructions in succession from the means for supplying the multiple instructions. The counter is connected to said means for decoding to receive incrementing and reset control signals from the means for decoding. The means for decoding is configured to supply the reset control signal to the counter and to supply a control signal to the means for fetching instructions in response to a SKIP instruction in the multiple instructions. In a modification of this aspect of the invention, the microprocessor system additionally has a loop counter connected to receive a decrement control signal from the means for decoding. The means for decoding is configured to supply the reset control signal to the counter and the decrement control signal to the loop counter in response to a MICROLOOP instruction in the multiple instructions. In a further modification to this aspect of the invention, the means for decoding is configured to control

the counter in response to an instruction utilizing a variable width operand. A means is connected to the counter to select the variable width operand in response to the counter.

In a still further aspect of the invention, the microprocessor system includes an arithmetic logic unit. A first push down stack is connected to the arithmetic logic unit. The first push down stack includes means for storing a top item connected to a first input of the arithmetic logic unit and means for storing a next item connected to a second input of the arithmetic logic unit. The arithmetic logic unit has an output connected to the means for storing a top item. The means for storing a top item is connected to provide an input to a register file. The register file desirably is a second push down stack, and the means for storing a top item and the register file are bidirectionally connected.

In another aspect of the invention, a data processing system has a microprocessor including a sensing circuit and a driver circuit, a memory, and an output enable line connected between the memory, the sensing circuit and the driver circuit. The sensing circuit is configured to provide a ready signal when the output enable line reaches a predetermined electrical level, such as a voltage. The microprocessor is configured so that the driver circuit provides an enabling signal on the output enable line responsive to the ready signal.

In a further aspect of the invention, the microprocessor system has a ring counter variable speed system clock connected to the central processing unit. The central processing unit and the ring counter variable speed system clock are provided in a single integrated circuit. An input/output interface is connected to exchange coupling control signals, addresses and data with the input/output interface. A second clock independent of the ring counter variable speed system clock is connected to the input/output interface.

In yet another aspect of the invention, a push down stack is connected to the arithmetic logic unit. The push down stack includes means for storing a top item connected to a first input of the arithmetic logic unit and means for storing a next item connected to a second input of the arithmetic logic unit. The arithmetic logic unit has an output connected to the means for storing a top item. The push down stack has a first plurality of stack elements configured as latches and a second plurality of stack elements configured as a random access memory. The first and second plurality of stack elements and the central processing unit are provided in a single integrated circuit. A third plurality of stack elements is configured as a random access memory external to the single integrated circuit. In this aspect of the invention, desirably a first pointer is connected to the first plurality of stack elements, a second pointer connected to the second plurality of stack elements, and a third pointer is connected to the third plurality of stack elements. The central processing unit is connected to pop items from the first plurality of stack elements. The first stack pointer is connected to the second stack pointer to pop a first plurality of items from the second plurality of stack elements when the first plurality of stack elements are empty from successive pop operations by the central processing unit. The second stack pointer is connected to the third stack pointer to pop a second plurality of items from the third plurality of stack elements when the second plurality of stack elements are empty from successive pop operations by the central processing unit.

In another aspect of the invention, a first register is connected to supply a first input to the arithmetic logic unit. A first shifter is connected between an output of the arithmetic logic unit and the first register. A second register is connected to receive a starting polynomial value. An output of the second register is connected to a second shifter. A least significant bit of the second register is connected to The arithmetic logic unit. A third register is connected to supply feedback terms of a polynomial to the arithmetic logic unit. A down counter, for counting down a number corresponding to digits of a polynomial to be generated, is connected to the arithmetic logic unit. The arithmetic logic unit is responsive to a polynomial instruction to carry out an exclusive OR of the contents of the first register with the contents of the third register if the least significant bit of the second register is a "ONE" and to pass the contents of the first register unaltered if the least significant bit of the second register is a "ZERO", until the down counter completes a count The polynomial to be generated results in said first register.

In still another aspect of the invention, a result register is connected to supply a first input to the arithmetic logic unit. A first, left shifting shifter is connected between an output of the arithmetic logic unit and the result register. A multiplier register is connected to receive a multiplier in bit reversed form. An output of the multiplier register is connected to a second, right shifting shifter. A least significant bit of the multiplier register is connected to the arithmetic logic unit. A third register is connected to supply a multiplicand to said arithmetic logic unit. A down counter, for counting down a number corresponding to one less than the number of digits of the multiplier, is connected to the arithmetic logic unit. The arithmetic logic unit is responsive to a multiply instruction to add the contents of the result register with the contents of the third register, when the least significant bit of the multiplier register is a "ONE" and to pass the contents of the result register unaltered, until the down counter completes a count. The product results in the result register.

The attainment of the foregoing and related objects, advantages and features of the invention should be more readily apparent to those skilled in the art, after review of the following more detailed description of the invention, taken together with the drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an external, plan view of an integrated circuit package incorporating a microprocessor in accordance with the invention.

FIG. **2** is a block diagram of a microprocessor in accordance with the invention.

FIG. **3** is a block diagram of a portion of a data processing system incorporating the microprocessor of FIGS. **1** and **2**.

FIG. **4** is a more detailed block diagram of a portion of the microprocessor shown in FIG. **2**.

FIG. **5** is a more detailed block diagram of another portion of the microprocessor shown in FIG. **2**.

FIG. **6** is a block diagram of another portion of the data processing system shown in part in FIG. **3** and incorporating the microprocessor of FIGS. **1–2** and **4–5**.

FIGS. **7** and **8** are layout diagrams for the data processing system shown in part in FIGS. **3** and **6**.

FIG. **9** is a layout diagram of a second embodiment of a microprocessor in accordance with the invention in a data processing system on a single integrated circuit.

FIG. **10** is a more detailed block diagram of a portion of the data processing system of FIGS. **7** and **8**.

FIG. **11** is a timing diagram useful for understanding operation of the system portion shown in FIG. **12**.

FIG. **12** is another more detailed block diagram of a further portion of the data processing system of FIGS. **7** and **8**.

FIG. **13** is a more detailed block diagram of a portion of the microprocessor shown in FIG. **2**.

FIG. **14** is a more detailed block and schematic diagram of a portion of the system shown in FIGS. **3** and **7–8**.

FIG. **15** is a graph useful for understanding operation of the system portion shown in FIG. **14**.

FIG. **16** is a more detailed block diagram showing part of the system portion shown in FIG. **4**.

FIG. **17** is a more detailed block diagram of a portion of the microprocessor shown in FIG. **2**.

FIG. **18** is a more detailed block diagram of part of the microprocessor portion shown in FIG. **17**.

FIG. **19** is a set of waveform diagrams useful for understanding operation of the part of the microprocessor portion shown in FIG. **18**.

FIG. **20** is a more detailed block diagram showing another part of the system portion shown in FIG. **4**.

FIG. **21** is a more detailed block diagram showing another part of the system portion shown in FIG. **4**.

FIGS. **22** and **23** are more detailed block diagrams showing another part of the system portion shown in FIG. **4**.

DETAILED DESCRIPTION OF THE INVENTION

OVERVIEW

The microprocessor of this invention is desirably implemented as a 32-bit microprocessor optimized for:

HIGH EXECUTION SPEED, and

LOW SYSTEM COST.

In this embodiment, the microprocessor can be thought of as 20 MIPS for 20 dollars. Important distinguishing features of the microprocessor are:

Uses low-cost commodity DYNAMIC RAMS to run 20 MIPS

4 instruction fetch per memory cycle

On-chip fast page-mode memory management

Runs fast without external cache

Requires few interfacing chips

Crams 32-bit CPU in 44 pin SOJ package

The instruction set is organized so that most operations can be specified with 8-bit instructions. Two positive products of this philosophy are:

Programs are smaller,

Programs can execute much faster.

The bottleneck in most computer systems is the memory bus. The bus is used to fetch instructions and fetch and store data. The ability to fetch four instructions in a single memory bus cycle significantly increases the bus availability to handle data.

Turning now to the drawings, more particularly to FIG. **1**, there is shown a packaged 32-bit microprocessor **50** in a 44-pin plastic leadless chip carrier, shown approximately 100 times its actual size of about 0.8 inch on a side. The fact that the microprocessor **50** is provided as a 44-pin package represents a substantial departure from typical microprocessor packages, which usually have about 200 input/output (I/O) pins. The microprocessor **50** is rated at 20 million instructions per second (MIPS). Address and data lines **52**, also labelled D**0**–D**31**, are shared for addresses and data without speed penalty as a result of the manner in which the microprocessor **50** operates, as will be explained below.

DYNAMIC RAM

In addition to the low cost 44-pin package, another unusual aspect of the high performance microprocessor **50** is that it operates directly with dynamic random access memories (DRAMs), as shown by row address strobe (RAS) and column address strobe (CAS) I/O pins **54**. The other I/O pins for the microprocessor **50** include V_{DD} pins **56**, V_{SS} pins **58**, output enable pin **60**, write pin **62**, clock pin **64** and reset pin **66**.

All high speed computers require high speed and expensive memory to keep up. The highest speed static RAM memories cost as much as ten times as much as slower dynamic RAMs. This microprocessor has been optimized to use low-cost dynamic RAM in high-speed page-mode. Page-mode dynamic RAMs offer static RAM performance without the cost penalty. For example, low-cost 85 nsec. dynamic RAMs access at 25 nsec when operated in fast page-mode. Integrated fast page-mode control on the microprocessor chip simplifies system interfacing and results in a faster system.

Details of the microprocessor **50** are shown in FIG. **2**. The microprocessor **50** includes a main central processing unit (CPU) **70** and a separate direct memory access (DMA) CPU **72** in a single integrated circuit making up the microprocessor **50**. The main CPU **70** has a first 16 deep push down stack **74**, which has a top item register **76** and a next item register **78**, respectively connected to provide inputs to an arithmetic logic unit (ALU) **80** by lines **82** and **84**. An output of the ALU **80** is connected to the top item register **76** by line **86**. The output of the top item register at **82** is also connected by line **88** to an internal data bus **90**.

A loop counter **92** is connected to a decrementer **94** by lines **96** and **98**. The loop counter **92** is bidirectionally connected to the internal data bus **90** by line **100**. Stack pointer **102**, return stack pointer **104**, mode register **106** and instruction register **108** are also connected to the internal data bus **90** by lines **110**, **112**, **114** and **116**, respectively. The internal data bus **90** is connected to memory controller **118** and to gate **120**. The gate **120** provides inputs on lines **122**, **124**, and **126** to X register **128**, program counter **130** and Y register **132** of return push down stack **134**. The X register **128**, program counter **130** and Y register **132** provide outputs to internal address bus **136** on lines **138**, **140** and **142**. The internal address bus provides inputs to the memory controller **118** and to an incrementer **144**. The incrementer **144** provides inputs to the X register, program counter and Y register via lines **146**, **122**, **124** and **126**. The DMA CPU **72** provides inputs to the memory controller **118** on line **148**. The memory controller **118** is connected to a RAM (not shown) by address/data bus **150** and control lines **152**.

FIG. **2** shows that the microprocessor **50** has a simple architecture. Prior art RISC microprocessors are substantially more complex in design. For example, the SPARC RISC microprocessor has three times the gates of the microprocessor **50**, and the Intel 8960 RISC microprocessor has 20 times the gates of the microprocessor **50**. The speed of this microprocessor is in substantial part due to this simplicity. The architecture incorporates push down stacks and register write to achieve this simplicity.

The microprocessor **50** incorporates an I/O that has been tuned to make heavy use of resources provided on the integrated circuit chip. On chip latches allow use of the same I/O circuits to handle three different things: column addressing, row addressing and data, with a slight to non-existent speed penalty. This triple bus multiplexing results in fewer buffers to expand, fewer interconnection lines, fewer I/O pins and fewer internal buffers.

The provision of on-chip DRAM control gives a performance equal to that obtained with the use of static RAMs. As a result, memory is provided at ¼ the system cost of static RAM used in most RISC systems.

The microprocessor **50** fetches 4 instructions per memory cycle; the instructions are in an 8-bit format, and this is a 32-bit microprocessor. System speed is therefore 4 times the memory bus bandwidth. This ability enables the microprocessor to break the Von Neumann bottleneck of the speed of getting the next instruction. This mode of operation is possible because of the use of a push down stack and register array. The push down stack allows the use of implied addresses, rather than the prior art technique of explicit addresses for two sources and a destination.

Most instructions execute in 20 nanoseconds in the microprocessor **50**. The microprocessor can therefore execute instructions at 50 peak MIPS without pipeline delays. This is a function of the small number of gates in the microprocessor **50** and the high degree of parallelism in the architecture of the microprocessor.

FIG. **3** shows how column and row addresses are multiplexed on lines D8–D14 of the microprocessor **50** for addressing DRAM **150** from I/O pins **52**. The DRAM **150** is one of eight, but only one DRAM **150** has been shown for clarity. As shown, the lines D11–D18 are respectively connected to row address inputs A0–A8 of the DRAM **150**. Additionally, lines D12–D15 are connected to the data inputs DQ1–DQ4 of the DRAM **150**. The output enable, write and column address strobe pins **54** are respectively connected to the output enable, write and column address strobe inputs of the DRAM **150** by lines **152**. The row address strobe pin **54** is connected through row address strobe decode logic **154** to the row address strobe input of the DRAM **150** by lines **156** and **158**.

D0–D7 pins **52** (FIG. **1**) are idle when the microprocessor **50** is outputting multiplexed row and column addresses on D11–D18 pins **52**. The D0–D7 pins **52** can therefore simultaneously be used for I/O when right justified I/O is desired. Simultaneous addressing and I/O can therefore be carried out.

FIG. **4** shows how the microprocessor **50** is able to achieve performance equal to the use of static RAMS with DRAMs through multiple instruction fetch in a single clock cycle and instruction fetch-ahead. Instruction register **108** receives four 8-bit byte instruction words **1–4** on 32-bit internal data bus **90**. The four instruction byte **1–4** locations of the instruction register **108** are connected to multiplexer **170** by busses **172**, **174**, **176** and **178**, respectively. A microprogram counter **180** is connected to the multiplexer **170** by lines **182**. The multiplexer **170** is connected to decoder **184** by bus **186**. The decoder **184** provides internal signals to the rest of the microprocessor **50** on lines **188**.

Most significant bits **190** of each instruction byte **1–4** location are connected to a 4-input decoder **192** by lines **194**. The output of decoder **192** is connected to memory controller **118** by line **196**. Program counter **130** is connected to memory controller **118** by internal address bus **136**, and the instruction register **108** is connected to the memory controller **118** by the internal data bus **90**. Address/data bus **198** and control bus **200** are connected to the DRAMS **150** (FIG. **3**).

In operation, when the most significant bits **190** of remaining instructions **1–4** are "1" in a clock cycle of the microprocessor **50**, there are no memory reference instructions in the queue. The output of decoder **192** on line **196** requests an instruction fetch ahead by memory controller **118** without interference with other accesses. While the current instructions in instruction register **108** are executing, the memory controller **118** obtains the address of the next set of four instructions from program counter **130** and obtains that set of instructions. By the time the current set of instructions has completed execution, the next set of instructions is ready for loading into the instruction register.

Details of the DMA CPU **72** are provided in FIG. **5**. Internal data bus **90** is connected to memory controller **118** and to DMA instruction register **210**. The DMA instruction register **210** is connected to DMA program counter **212** by bus **214**, to transfer size counter **216** by bus **218** and to timed transfer interval counter **220** by bus **222**. The DMA instruction register **210** is also connected to DMA I/O and RAM address register **224** by line **226**. The DMA I/O and RAM address register **224** is connected to the memory controller **118** by memory cycle request line **228** and bus **230**. The DMA program counter **212** is connected to the internal address bus **136** by bus **232**. The transfer size counter **216** is connected to a DMA instruction done decrementer **234** by lines **236** and **238**. The decrementer **234** receives a control input on memory cycle acknowledge line **240**. When transfer size counter **216** has completed its count, it provides a control signal to DMA program counter **212** on line **242**. Timed transfer interval counter **220** is connected to decrementer **244** by lines **246** and **248**. The decrementer **244** receives a control input from a microprocessor system clock on line **250**.

The DMA CPU **72** controls itself and has the ability to fetch and execute instructions. It operates as a co-processor to the main CPU **70** (FIG. **2**) for time specific processing.

FIG. **6** shows how the microprocessor **50** is connected to an electrically programmable read only memory (EPROM) **260** by reconfiguring the data lines **52** so that some of the data lines **52** are input lines and some of them are output lines. Data lines **52** D0–D7 provide data to and from corresponding data terminals **262** of the EPROM **260**. Data lines **52** D9–D18 provide addresses to address terminals **264** of the EPROM **260**. Data lines **52** D19–D31 provide inputs from the microprocessor **50** to memory and I/O decode logic **266**. RAS **0/1** control line **268** provides a control signal for determining whether the memory and I/O decode logic provides a DRAM RAS output on line **270** or a column enable output for the EPROM **260** on line **272**. Column address strobe terminal **60** of the microprocessor **50** provides an output enable signal on line **274** to the corresponding terminal **276** of the EPROM **260**.

FIGS. **7** and **8** show the front and back of a one card data processing system **280** incorporating the microprocessor **50**, MSM514258-10 type DRAMs **150** totalling 2 megabytes, a Motorola 50 MegaHertz crystal oscillator clock **282**, I/O circuits **284** and a 27256 type EPROM **260**. The I/O circuits **284** include a 74HC04 type high speed hex inverter circuit **286**, an IDT39C828 type 10-bit inverting buffer circuit **288**, an IDT39C822 type 10-bit inverting register circuit **290**, and two IDT39C823 type 9-bit non-inverting register circuits **292**. The card **280** is completed with a MAX12V type DC—DC converter circuit **294**, 34-pin dual AMP type headers **296**, a coaxial female power connector **298**, and a 3-pin AMP right angle header **300**. The card **280** is a low cost, imbeddable product that can be incorporated in larger systems or used as an internal development tool.

The microprocessor **50** is a very high performance (50 MHz) RISC influenced 32-bit CPU designed to work closely with dynamic RAM. Clock for clock, the microprocessor **50** approaches the theoretical performance limits possible with a single CPU configuration. Eventually, the microprocessor **50** and any other processor is limited by the bus bandwidth and the number of bus paths. The critical conduit is between the CPU and memory.

One solution to the bus bandwidth/bus path problem is to integrate a CPU directly onto the memory chips, giving every memory a direct bus the CPU. FIG. **9** shows another microprocessor **310** that is provided integrally with 1 mega-

bit of DRAM **311** in a single integrated circuit **312**. Until the present invention, this solution has not been practical, because most high performance CPUs require from 500,000 to 1,000,000 transistors and enormous die sizes just by themselves. The microprocessor **310** is equivalent to the microprocessor **50** in FIGS. **1–8**. The microprocessors **50** and **310** are the most transistor efficient high performance CPUs in existence, requiring fewer than 50,000 transistors for dual processors **70** and **72** (FIG. **2**) or **314** and **316** (less memory). The very high speed of the microprocessors **50** and **310** is to a certain extent a function of the small number of active devices. In essence, the less silicon gets in the way, the faster the electrons can get where they are going.

The microprocessor **310** is therefore the only CPU suitable for integration on the memory chip die **312**. Some simple modifications to the basic microprocessor **50** to take advantage of the proximity to the DRAM array **311** can also increase the microprocessor **50** clock speed by 50 percent, and probably more.

The microprocessor **310** core on board the DRAM die **312** provides most of the speed and functionality required for a large group of applications from automotive to peripheral control. However, the integrated CPU **310**/DRAM **311** concept has the potential to redefine significantly the way multiprocessor solutions can solve a spectrum of very compute intensive problems. The CPU **310**/DRAM **311** combination eliminates the Von Neumann bottleneck by distributing it across numerous CPU/DRAM chips **312**. The microprocessor **310** is a particularly good core for multiprocessing, since it was designed with the SDI targeting array in mind, and provisions were made for efficient interprocessor communications.

Traditional multiprocessor implementations have been very expensive in addition to being unable to exploit fully the available CPU horsepower. Multiprocessor systems have typically been built up from numerous board level or box level computers. The result is usually an immense amount of hardware with corresponding wiring, power consumption and communications problems. By the time the systems are interconnected, as much as 50 percent of the bus speed has been utilized just getting through the interfaces.

In addition, multiprocessor system software has been scarce. A multiprocessor system can easily be crippled by an inadequate load-sharing algorithm in the system software, which allows one CPU to do a great deal of work and the others to be idle. Great strides have been made recently in systems software, and even UNIX V.4 may be enhanced to support multiprocessing. Several commercial products from such manufacturers as DUAL Systems and UNISOFT do a credible job on 68030 type microprocessor systems now.

The microprocessor **310** architecture eliminates most of the interface friction, since up to 64 CPU **310**/RAM **311** processors should be able to intercommunicate without buffers or latches. Each chip **312** has about 40 MIPS raw speed, because placing the DRAM **311** next to the CPU **310** allows the microprocessor **310** instruction cycle to be cut in half, compared to the microprocessor **50**. A 64 chip array of these chips **312** is more powerful than any other existing computer. Such an array fits on a 3×5 card, cost less than a FAX machine, and draw about the same power as a small television.

Dramatic changes in price/performance always reshape existing applications and almost always create new ones. The introduction of microprocessors in the mid 1970s created video games, personal computers, automotive computers, electronically controlled appliances, and low cost computer peripherals.

The integrated circuit **312** will find applications in all of the above areas, plus create some new ones. A common generic parallel processing algorithm handles convolution/Fast Fourier Transform (FFT)/pattern recognition. Interesting product possibilities using the integrated circuit **312** include high speed reading machines, real-time speech recognition, spoken language translation, real-time robot vision, a product to identify people by their faces, and an automotive or aviation collision avoidance system.

A real time processor for enhancing high density television (HDTV) images, or compressing the HDTV information into a smaller bandwidth, would be very feasible. The load sharing in HDTV could be very straightforward. Splitting up the task according to color and frame would require 6, 9 or 12 processors. Practical implementation might require 4 meg RAMs integrated with the microprocessor **310**.

The microprocessor **310** has the following specifications:

CONTROL LINES
4 - POWER/GROUND
1 - CLOCK
32 - DATA I/O
4 - SYSTEM CONTROL
EXTERNAL MEMORY FETCH
EXTERNAL MEMORY FETCH AUTOINCREMENT X
EXTERNAL MEMORY FETCH AUTOINCREMENT Y
EXTERNAL MEMORY WRITE
EXTERNAL MEMORY WRITE AUTOINCREMENT X
EXTERNAL MEMORY WRITE AUTOINCREMENT Y
EXTERNAL PROM FETCH
LOAD ALL X REGISTERS
LOAD ALL Y REGISTERS
LOAD ALL PC REGISTERS
EXCHANGE X AND Y
INSTRUCTION FETCH
ADD TO PC
ADD TO X
WRITE MAPPING REGISTER
READ MAPPING REGISTER
REGISTER CONFIGURATION
MICROPROCESSOR **310** CPU **316** CORE
COLUMN LATCH**1** (1024 BITS) 32×32 MUX
STACK POINTER (16 BITS)
COLUMN LATCH**2** (1024 BITS) 32×32 MUX
RSTACK POINTER (16 BITS)
PROGRAM COUNTER 32 BITS
X**0** REGISTER 32 BITS (ACTIVATED ONLY FOR ON-CHIP ACCESSES)
Y**0** REGISTER 32 BITS (ACTIVATED ONLY FOR ON-CHIP ACCESSES)
LOOP COUNTER 32 BITS
DMA CPU **314** CORE
DMA PROGRAM COUNTER 24 BITS
INSTRUCTION REGISTER 32 BITS
I/O & RAM ADDRESS REGISTER 32 BITS
TRANSFER SIZE COUNTER 12 BITS
INTERVAL COUNTER 12 BITS

To offer memory expansion for the basic chip **312**, an intelligent DRAM can be produced. This chip will be optimized for high speed operation with the integrated circuit **312** by having three on-chip address registers: Program Counter, X Register and Y register. As a result, to access the intelligent DRAM, no address is required, and a total access cycle could be as short as 10 nsec. Each expansion DRAM would maintain its own copy of the three registers and would be identified by a code specifying its memory address. Incrementing and adding to the three

registers will actually take place on the memory chips. A maximum of 64 intelligent DRAM peripherals would allow a large system to be created without sacrificing speed by introducing multiplexers or buffers.

There are certain differences between the microprocessor **310** and the microprocessor **50** that arise from providing the microprocessor **310** on the same die **312** with the DRAM **311**. Integrating the DRAM **311** allows architectural changes in the microprocessor **310** logic to take advantage of existing on-chip DRAM **311** circuitry. Row and column design is inherent in memory architecture. The DRAMs **311** access random bits in a memory array by first selecting a row of 1024 bits, storing them into a column latch, and then selecting one of the bits as the data to be read or written.

The time required to access the data is split between the row access and the column access. Selecting data already stored in a column latch is faster than selecting a random bit by at least a factor of six. The microprocessor **310** takes advantage of this high speed by creating a number of column latches and using them as caches and shift registers. Selecting a new row of information may be thought of as performing a 1024-bit read or write with the resulting immense bus bandwidth.

1. The microprocessor **50** treats its 32-bit instruction register **108** (see FIGS. **2** and **4**) as a cache for four 8-bit instructions. Since the DRAM **311** maintains a 1024-bit latch for the column bits, the microprocessor **310** treats the column latch as a cache for 128 8-bit instructions. Therefore, the next instruction will almost always be already present in the cache. Long loops within the cache are also possible and more useful than the 4 instruction loops in the microprocessor **50**.

2. The microprocessor **50** uses two 16×32-bit deep register arrays **74** and **134** (FIG. **2**) for the parameter stack and the return stack. The microprocessor **310** creates two other 1024-bit column latches to provide the equivalent of two 32×32-bit arrays, which can be accessed twice as fast as a register array.

3. The microprocessor **50** has a DMA capability which can be used for I/O to a video shift register. The microprocessor **310** uses yet another 1024-bit column latch as a long video shift register to drive a CRT display directly. For color displays, three on-chip shift registers could also be used. These shift registers can transfer pixels at a maximum of 100 MHz.

4. The microprocessor **50** accesses memory via an external 32-bit bus. Most of the memory **311** for the microprocessor **310** is on the same die **312**. External access to more memory is made using an 8-bit bus. The result is a smaller die, smaller package and lower power consumption than the microprocessor **50**.

5. The microprocessor **50** consumes about a third of its operating power charging and discharging the I/O pins and associated capacitances. The DRAMs **150** (FIG. **8**) connected to the microprocessor **50** dissipate most of their power in the I/O drivers. A microprocessor **310** system will consume about one-tenth the power of a microprocessor **50** system, since having the DRAM **311** next to the processor **310** eliminates most of the external capacitances to be charged and discharged.

6. Multiprocessing means splitting a computing task between numerous processors in order to speed up the solution. The popularity of multiprocessing is limited by the expense of current individual processors as well as the limited interprocessor communications ability. The microprocessor **310** is an excellent multiprocessor candidate, since the chip **312** is a monolithic computer complete with memory, rendering it low-cost and physically compact.

The shift registers implemented with the microprocessor **310** to perform video output can also be configured as interprocessor communication links. The INMOS transputer attempted a similar strategy, but at much lower speed and without the performance benefits inherent in the microprocessor **310** column latch architecture. Serial I/O is a prerequisite for many multiprocessor topologies because of the many neighbor processors which communicate. A cube has 6 neighbors. Each neighbor communicates using these lines:

DATA IN
CLOCK IN
READY FOR DATA
DATA OUT
DATA READY?
CLOCK OUT

A special start up sequence is used to initialize the on-chip DRAM **311** in each of the processors.

The microprocessor **310** column latch architecture allows neighbor processors to deliver information directly to internal registers or even instruction caches of other chips **312**. This technique is not used with existing processors, because it only improves performance in a tightly coupled DRAM system.

7. The microprocessor **50** architecture offers two types of looping structures: LOOP-IF-DONE and MICRO-LOOP. The former takes an 8-bit to 24-bit operand to describe the entry point to the loop address. The latter performs a loop entirely within the 4 instruction queue and the loop entry point is implied as the first instruction in the queue. Loops entirely within the queue run without external instruction fetches and execute up to three times as fast as the long loop construct. The microprocessor **310** retains both constructs with a few differences. The microprocessor **310** microloop functions in the same fashion as the microprocessor **50** operation, except the queue is 1024-bits or 128 8-bit instructions long. The microprocessor **310** microloop can therefore contain jumps, branches, calls and immediate operations not possible in the 4 8-bit instruction microprocessor **50** queue.

Microloops in the microprocessor **50** can only perform simple block move and compare functions. The larger microprocessor **310** queue allows entire digital signal processing or floating point algorithms to loop at high speed in the queue.

The microprocessor **50** offers four instructions to redirect execution:

CALL
BRANCH
BRANCH-IF-ZERO
LOOP-IF-NOT-DONE

These instructions take a variable length address operand 8, 16 or 24 bits long. The microprocessor **50** next address logic treats the three operands similarly by adding or subtracting them to the current program counter. For the microprocessor **310**, the 16 and 24-bit operands function in the same manner as the 16 and 24-bit operands in the microprocessor **50**. The 8-bit class operands are reserved to operate entirely within the instruction queue. Next address decisions can therefore be made quickly, because only 10 bits of addresses are affected, rather than 32. There is no carry or borrow generated past the 10 bits.

8. The microprocessor **310** CPU **316** resides on an already crowded DRAM die **312**. To keep chip size as small as possible, the DMA processor **72** of the microprocessor **50** has been replaced with a more traditional DMA controller **314**. DMA is used with the microprocessor **310** to perform the following functions:

Video output to a CRT

Multiprocessor serial communications
8-bit parallel I/O

The DMA controller **314** can maintain both serial and parallel transfers simultaneously. The following DMA sources and destinations are supported by the microprocessor **310**:

DESCRIPTION	I/O	LINES
1. Video shift register	OUTPUT	1 to 3
2. Multiprocessor serial	BOTH	6 lines/channel
3. 8-bit parallel	BOTH	8 data, 4 control

The three sources use separate 1024-bit buffers and separate I/O pins. Therefore, all three may be active simultaneously without interference.

The microprocessor **310** can be implemented with either a single multiprocessor serial buffer or separate receive and sending buffers for each channel, allowing simultaneous bidirectional communications with six neighbors simultaneously.

FIGS. **10** and **11** provide details of the PROM DMA used in the microprocessor **50**. The microprocessor **50** executes faster than all but the fastest PROMs. PROMS are used in a microprocessor **50** system to store program segments and perhaps entire programs. The microprocessor **50** provides a feature on power-up to allow programs to be loaded from low-cost, slow speed PROMs into high speed DRAM for execution. The logic which performs this function is part of the DMA memory controller **118**. The operation is similar to DMA, but not identical, since four 8-bit bytes must be assembled on the microprocessor **50** chip, then written to the DRAM **150**.

The microprocessor **50** directly interfaces to DRAM **150** over a triple multiplexed data and address bus **350**, which carries RAS addresses, CAS addresses and data. The EPROM **260**, on the other hand, is read with non-multiplexed busses. The microprocessor **50** therefore has a special mode which unmultiplexes the data and address lines to read 8 bits of EPROM data. Four 8-bit bytes are read in this fashion. The multiplexed bus **350** is turned back on, and the data is written to the DRAM **150**.

When the microprocessor **50** detects a RESET condition, the processor stops the main CPU **70** and forces a mode **0** (PROM LOAD) instruction into the DMA CPU **72** instruction register. The DMA instruction directs the memory controller to read the EPROM **260** data at 8 times the normal access time for memory. Assuming a 50 MHz microprocessor **50**, this means an access time of 320 nsec. The instruction also indicates:

The selection address of the EPROM **260** to be loaded,
The number of 32-bit words to transfer,
The DRAM **150** address to transfer into.

The sequence of activities to transfer one 32-bit word from EPROM **260** to DRAM **150** are:

1. RAS goes low at **352**, latching the EPROM **260** select information from the high order address bits. The EPROM **260** is selected.
2. Twelve address bits (consisting of what is normally DRAM CAS addresses plus two byte select bits are placed on the bus **350** going to the EPROM **260** address pins. These signals will remain on the lines until the data from the EPROM **260** has been read into the microprocessor **50**. For the first byte, the byte select bits will be binary 00.
3. CAS goes low at **354**, enabling the EPROM **260** data onto the lower 8 bits of the external address/data bus **350**. NOTE: It is important to recognize that, during this part of the cycle, the lower 8 bits of the external data/address bus are functioning as inputs, but the rest of the bus is still acting as outputs.
4. The microprocessor **50** latches these eight least significant bits internally and shifts them 8 bits left to shift them to the next significant byte position.
5. Steps **2**, **3** and **4** are repeated with byte address **01**.
6. Steps **2**, **3** and **4** are repeated with byte address **10**.
7. Steps **2**, **3** and **4** are repeated with byte address **11**.
8. CAS goes high at **356**, taking the EPROM **260** off the data bus.
9. RAS goes high at **358**, indicating the end of the EPROM **260** access.
10. RAS goes low at **360**, latching the DRAM select information from the high order address bits. At the same time, the RAS address bits are latched into the DRAM **150**. The DRAM **150** is selected.
11. CAS goes low at **362**, latching the DRAM **150** CAS addresses.
12. The microprocessor **50** places the previously latched EPROM **260** 32-bit data onto the external address/data bus **350**. W goes low at **364**, writing the 32 bits into the DRAM **150**.
13. W goes high at **366**. CAS goes high at **368**. The process continues with the next word.

FIG. **12** shows details of the microprocessor **50** memory controller **118**. In operation, bus requests stay present until they are serviced. CPU **70** requests are prioritized at **370** in the order of: 1, Parameter Stack; 2, Return Stack; 3, Data Fetch; 4, Instruction Fetch. The resulting CPU request signal and a DMA request signal are supplied as bus requests to bus control **372**, which provides a bus grant signal at **374**. Internal address bus **136** and a DMA counter **376** provide inputs to a multiplexer **378**. Either a row address or a column address are provided as an output to multiplexed address bus **380** as an output from the multiplexer **378**. The multiplexed address bus **380** and the internal data bus **90** provide address and data inputs, respectively, to multiplexer **382**. Shift register **384** supplies row address strobe (RAS) **1** and **2** control signals to multiplexer **386** and column address strobe (CAS) **1** and **2** control signals to multiplexer **388** on lines **390** and **392**. The shift register **384** also supplies output enable (OE) and write (W) signals on lines **394** and **396** and a control signal on line **398** to multiplexer **382**. The shift register **384** receives a RUN signal on line **400** to generate a memory cycle and supplies a MEMORY READY signal on line **402** when an access is complete.

STACK/REGISTER ARCHITECTURE

Most microprocessors use on-chip registers for temporary storage of variables. The on-chip registers access data faster than off-chip RAM. A few microprocessors use an on-chip push down stack for temporary storage.

A stack has the advantage of faster operation compared to on-chip registers by avoiding the necessity to select source and destination registers. (A math or logic operation always uses the top two stack items as source and the top of stack as destination.) The stack's disadvantage is that it makes some operations clumsy. Some compiler activities in particular require on-chip registers for efficiency.

As shown in FIG. **13**, the microprocessor **50** provides both on-chip registers **134** and a stack **74** and reaps the benefits of both.

BENEFITS:

1. Stack math and logic is twice as fast as those available on an equivalent register only machine. Most program-

mers and optimizing compilers can take advantage of this feature.

2. Sixteen registers are available for on-chip storage of local variables which can transfer to the stack for computation. The accessing of variables is three to four times as fast as available on a strictly stack machine.

The combined stack **74**/register **134** architecture has not been used previously due to inadequate understanding by computer designers of optimizing compilers and the mix of transfer versus math/logic instructions.

ADAPTIVE MEMORY CONTROLLER

A microprocessor must be designed to work with small or large memory configurations. As more memory loads are added to the data, address, and control lines, the switching speed of the signals slows down. The microprocessor **50** multiplexes the address/data bus three ways, so timing between the phases is critical. A traditional approach to the problem allocates a wide margin of time between bus phases so that systems will work with small or large numbers of memory chips connected. A speed compromise of as much as 50% is required.

As shown in FIG. **14**, the microprocessor **50** uses a feedback technique to allow the processor to adjust memory bus timing to be fast with small loads and slower with large ones. The OUTPUT ENABLE (OE) line **152** from the microprocessor **50** is connected to all memories **150** on the circuit board. The loading on the output enable line **152** to the microprocessor **50** is directly related to the number of memories **150** connected. By monitoring how rapidly OE **152** goes high after a read, the microprocessor **50** is able to determine when the data hold time has been satisfied and place the next address on the bus.

The level of the OE line **152** is monitored by CMOS input buffer **410** which generates an internal READY signal on line **412** to the microprocessor's memory controller. Curves **414** and **416** of the FIG. **15** graph show the difference in rise time likely to be encountered from a lightly to heavily loaded memory system. When the OE line **152** has reached a predetermined level to generate the READY signal, driver **418** generates an OUTPUT ENABLE signal on OE line **152**.

SKIP WITHIN THE INSTRUCTION CACHE

The microprocessor **50** fetches four 8-bit instructions each memory cycle and stores them in a 32-bit instruction register **108**, as shown in FIG. **16**. A class of "test and skip" instructions can very rapidly execute a very fast jump operation within the four instruction cache.

SKIP CONDITIONS:

Always
ACC non-zero
ACC negative
Carry flag equal logic one
Never
ACC equal zero
ACC positive
Carry flag equal logic zero

The SKIP instruction can be located in any of the four byte positions **420** in the 32-bit instruction register **108**. If the test is successful, SKIP will jump over the remaining one, two, or three 8-bit instructions in the instruction register **108** and cause the next four-instruction group to be loaded into the register **108**. As shown, the SKIP operation is implemented by resetting the 2-bit microinstruction counter **180** to zero on line **422** and simultaneously latching the next instruction group into the register **108**. Any instructions following the SKIP in the instruction register are overwritten by the new instructions and not executed.

The advantage of SKIP is that optimizing compilers and smart programmers can often use it in place of the longer conditional JUMP instruction. SKIP also makes possible microloops which exit when the loop counts down or when the SKIP jumps to the next instruction group. The result is very fast code.

Other machines (such as the PDP-**8** and Data General NOVA) provide the ability to skip a single instruction. The microprocessor **50** provides the ability to skip up to three instructions.

MICROLOOP IN THE INSTRUCTION CACHE

The microprocessor **50** provides the MICROLOOP instruction to execute repetitively from one to three instructions residing in the instruction register **108**. The microloop instruction works in conjunction with the LOOP COUNTER **92** (FIG. **2**) connected to the internal data bus **90**. To execute a microloop, the program stores a count in LOOP COUNTER **92**. MICROLOOP may be placed in the first, second, third, or last byte **420** of the instruction register **108**. If placed in the first position, execution will just create a delay equal to the number stored in LOOP COUNTER **92** times the machine cycle. If placed in the second, third, or last byte **420**, when the microloop instruction is executed, it will test the LOOP COUNT for zero. If zero, execution will continue with the next instruction. If not zero, the LOOP COUNTER **92** is decremented and the 2-bit microinstruction counter is cleared, causing the preceding instructions in the instruction register to be executed again.

Microloop is useful for block move and search operations. By executing a block move completely out of the instruction register **108**, the speed of the move is doubled, since all memory cycles are used by the move rather than being shared with instruction fetching. Such a hardware implementation of microloops is much faster than conventional software implementation of a comparable function.

OPTIMAL CPU CLOCK SCHEME

The designer of a high speed microprocessor must produce a product which operate over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing. Temperature, voltage, and process all affect transistor propagation delays. Traditional CPU designs are done so that with the worse case of the three parameters, the circuit will function at the rated clock speed. The result are designs that must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse case conditions.

The microprocessor **50** uses the technique shown in FIGS. **17–19** to generate the system clock and its required phases. Clock circuit **430** is the familiar "ring oscillator" used to test process performance. The clock is fabricated on the same silicon chip as the rest of the microprocessor **50**.

The ring oscillator frequency is determined by the parameters of temperature, voltage, and process. At room temperature, the frequency will be in the neighborhood of 100 MHZ. At 70 degrees Centigrade, the speed will be 50 MHZ. The ring oscillator **430** is useful as a system clock, with its stages **431** producing phase 0-phase **3** outputs **433** shown in FIG. **19**, because its performance tracks the parameters which similarly affect all other transistors on the same silicon die. By deriving system timing from the ring oscillator **430**, CPU **70** will always execute at the maximum frequency possible, but never too fast. For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor **50** will operate slower than normal. Since the microprocessor **50** ring oscillator clock **430** is made from the same transistors on the same die as the latches and gates, it too will

operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.

ASYNCHRONOUS/SYNCHRONOUS CPU

Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor **50** provides a dual-clock scheme as shown in FIG. **17**, with the CPU **70** operating asynchronously to I/O interface **432** forming part of memory controller **118** (FIG. **2**) and the I/O interface **432** operating synchronously with the external world of memory and I/O devices. The CPU **70** executes at the fastest speed possible using the adaptive ring oscillator clock **430**. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor **50** for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface **432**, speed of which is controlled by a conventional crystal clock **434**. The interface **432** processes requests for memory accesses from the microprocessor **50** and acknowledges the presence of I/O data. The microprocessor **50** fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. By decoupling the variable speed of the CPU **70** from the fixed speed of the I/O interface **432**, optimum performance can be achieved by each. Recoupling between the CPU **70** and the interface **432** is accomplished with hand shake signals on lines **436**, with data/addresses passing on bus **90**, **136**.

ASYNCHRONOUS/SYNCHRONOUS CPU IMBEDDED ON A DRAM CHIP

System performance is enhanced even more when the DRAM **311** and CPU **314** (FIG. **9**) are located on the same die. The proximity of the transistors means that DRAM **311** and CPU **314** parameters will closely follow each other. At room temperature, not only would the CPU **314** execute at 100 MHZ, but the DRAM **311** would access fast enough to keep up. The synchronization performed by the I/O interface **432** would be for DMA and reading and writing I/O ports. In some systems (such as calculators) no I/O synchronization at all would be required, and the I/O clock would be tied to the ring counter clock.

VARIABLE WIDTH OPERANDS

Many microprocessors provide variable width operands. The microprocessor **50** handles operands of 8, 16, or 24 bits using the same op-code. FIG. **20** shows the 32-bit instruction register **108** and the 2-bit microinstruction register **180** which selects the 8-bit instruction. Two classes of microprocessor **50** instructions can be greater than 8-bits, JUMP class and IMMEDIATE. A JUMP or IMMEDIATE op-code is 8-bits, but the operand can be 8, 16, or 24 bits long. This magic is possible because operands must be right justified in the instruction register. This means that the least significant bit of the operand is always located in the least significant bit of the instruction register. The microinstruction counter **180** selects which 8-bit instruction to execute. If a JUMP or IMMEDIATE instruction is decoded, the state of the 2-bit microinstruction counter selects the required 8, 16, or 24 bit operand onto the address or data bus. The unselected 8-bit bytes are loaded with zeros by operation of decoder **440** and gates **442**. The advantage of this technique is the saving of a number of op-codes required to specify the different operand sizes in other microprocessors.

TRIPLE STACK CACHE

Computer performance is directly related to the system memory bandwidth. The faster the memories, the faster the computer. Fast memories are expensive, so techniques have been developed to move a small amount of high-speed memory around to the memory addresses where it is needed. A large amount of slow memory is constantly updated by the fast memory, giving the appearance of a large fast memory array. A common implementation of the technique is known as a high-speed memory cache. The cache may be thought of as fast acting shock absorber smoothing out the bumps in memory access. When more memory is required than the shock can absorb, it bottoms out and slow speed memory is accessed. Most memory operations can be handled by the shock absorber itself.

The microprocessor **50** architecture has the ALU **80** (FIG. **2**) directly coupled to the top two stack locations **76** and **78**. The access time of the stack **74** therefore directly affects the execution speed of the processor. The microprocessor **50** stack architecture is particularly suitable to a triple cache technique, shown in FIG. **21** which offers the appearance of a large stack memory operating at the speed of on-chip latches **450**. Latches **450** are the fastest form of memory device built on the chip, delivering data in as little as 3 nsec. However latches **450** require large numbers of transistors to construct. On-chip RAM **452** requires fewer transistors than latches, but is slower by a factor of five (15 nsec access). Off-chip RAM **150** is the slowest storage of all. The microprocessor **50** organizes the stack memory hierarchy as three interconnected stacks **450**, **452** and **454**. The latch stack **450** is the fastest and most frequently used. The on-chip RAM stack **452** is next. The off-chip RAM stack **454** is slowest. The stack modulation determines the effective access time of the stack. If a group of stack operations never push or pull more than four consecutive items on the stack, operations will be entirely performed in the 3 nsec latch stack. When the four latches **456** are filled, the data in the bottom of the latch stack **450** is written to the top of the on-chip RAM stack **452**. When the sixteen locations **458** in the on-chip RAM stack **452** are filled, the data in the bottom of the on-chip RAM stack **452** is written to the top of the off-chip RAM stack **454**. When popping data off a full stack **450**, four pops will be performed before stack empty line **460** from the latch stack pointer **462** transfers data from the on-chip RAM stack **452**. By waiting for the latch stack **450** to empty before performing the slower on-chip RAM access, the high effective speed of the latches **456** are made available to the processor. The same approach is employed with the on-chip RAM stack **452** and the off-chip RAM stack **454**.

POLYNOMIAL GENERATION INSTRUCTION

Polynomials are useful for error correction, encryption, data compression, and fractal generation. A polynomial is generated by a sequence of shift and exclusive OR operations. Special chips are provided for this purpose in the prior art.

The microprocessor **50** is able to generate polynomials at high speed without external hardware by slightly modifying how the ALU **80** works. As shown in FIG. **21**, a polynomial is generated by loading the "order" (also known as the feedback terms) into C Register **470**. The value thirty one (resulting in 32 iterations) is loaded into DOWN COUNTER **472**. A register **474** is loaded with zero. B register **476** is loaded with the starting polynomial value. When the POLY instruction executes, C register **470** is exclusively ORed with A register **474** if the least significant bit of B register **476** is a one. Otherwise, the contents of the A register **474** passes through the ALU **80** unaltered. The combination of A and B is then shifted right (divided by 2) with shifters **478** and **480**. The operation automatically repeats the specified number of iterations, and the resulting polynomial is left in A register **474**.

FAST MULTIPLY

Most microprocessors offer a 16×16 or 32×32 bit multiply instruction. Multiply when performed sequentially takes one shift/add per bit, or 32 cycles for 32 bit data. The microprocessor **50** provides a high speed multiply which allows multiplication by small numbers using only a small number of cycles. FIG. **23** shows the logic used to implement the high speed algorithm. To perform a multiply, the size of the multiplier less one is placed in the DOWN COUNTER **472**. For a four bit multiplier, the number three would be stored in the DOWN COUNTER **472**. Zero is loaded into the A register **474**. The multiplier is written bit reversed into the B Register **476**. For example, a bit reversed five (binary 0101) would be written into B as 1010. The multiplicand is written into the C register **470**. Executing the FAST MULT instruction will leave the result in the A Register **474**, when the count has been completed. The fast multiply instruction is important because many applications scale one number by a much smaller number. The difference in speed between multiplying a 32×32 bit and a 32×4 bit is a factor of 8. If the least significant bit of the multiplier is a "ONE", the contents of the A register **474** and the C register **470** are added. If the least significant bit of the multiplier is a "ZERO", the contents of the A register are passed through the ALU **80** unaltered. The output of the ALU **80** is shifted left by shifter **482** in each iteration. The contents of the B register **476** are shifted right by the shifter **480** in each iteration.

INSTRUCTION EXECUTION PHILOSOPHY

The microprocessor **50** uses high speed D latches in most of the speed critical areas. Slower on-chip RAM is used as secondary storage.

The microprocessor **50** philosophy of instruction execution is to create a hierarchy of speed as follows:

Logic and D latch transfers	1 cycle	20 nsec
Math	2 cycles	40 nsec
Fetch/store on-chip RAM	2 cycles	40 nsec
Fetch/store in current RAS page	4 cycles	80 nsec
Fetch/store with RAS cycle	11 cycles	220 nsec

With a 50 MHZ clock, many operations can be performed in 20 nsec. and almost everything else in 40 nsec.

To maximize speed, certain techniques in processor design have been used. They include:

Eliminating arithmetic operations on addresses,
Fetching up to four instructions per memory cycle,
Pipelineless instruction decoding
Generating results before they are needed,
Use of three level stack caching.

PIPELINE PHILOSOPHY

Computer instructions are usually broken down into sequential pieces, for example: fetch, decode, register read, execute, and store. Each piece will require a single machine cycle. In most Reduced Instruction Set Computer (RISC) chips, instruction require from three to six cycles.

RISC instructions are very parallel. For example, each of 70 different instructions in the SPARC (SUN Computer's RISC chip) has five cycles. Using a technique called "pipelining", the different phases of consecutive instructions can be overlapped.

To understand pipelining, think of building five residential homes. Each home will require in sequence, a foundation, framing, plumbing and wiring, roofing, and interior finish. Assume that each activity takes one week. To build one house will take five weeks.

But what if you want to build an entire subdivision? You have only one of each work crew, but when the foundation men finish on the first house, you immediately start them on the second one, and so on. At the end of five weeks, the first home is complete, but you also have five foundations. If you have kept the framing, plumbing, roofing, and interior guys all busy, from five weeks on, a new house will be completed each week.

This is the way a RISC chip like SPARC appears to execute an instruction in a single machine cycle. In reality, a RISC chip is executing one fifth of five instructions each machine cycle. And if five instructions stay in sequence, an instruction will be completed each machine cycle.

The problems with a pipeline are keeping the pipe full with instructions. Each time an out of sequence instruction such as a BRANCH or CALL occurs, the pipe must be refilled with the next sequence. The resulting dead time to refill the pipeline can become substantial when many IF/THEN/ELSE statements or subroutines are encountered.

THE PIPELINE APPROACH

The microprocessor **50** has no pipeline as such. The approach of this microprocessor to speed is to overlap instruction fetching with execution of the previously fetched instruction(s). Beyond that, over half the instructions (the most common ones) execute entirely in a single machine cycle of 20 nsec. This is possible because:

1. Instruction decoding resolves in 2.5 nsec.
2. Incremented/decremented and some math values are calculated before they are needed, requiring only a latching signal to execute.
3. Slower memory is hidden from high speed operations by high-speed D latches which access in 4 nsec.

The disadvantage for this microprocessor is a more complex chip design process. The advantage for the chip user is faster ultimate throughput since pipeline stalls cannot exist. Pipeline synchronization with availability flag bits and other such pipeline handling is not required by this microprocessor.

For example, in some RISC machines an instruction which tests a status flag may have to wait for up to four cycles for the flag set by the previous instruction to be available to be tested. Hardware and software debugging is also somewhat easier because the user doesn't have to visualize five instructions simultaneously in the pipe.

OVERLAPPING INSTRUCTION FETCH/EXECUTE

The slowest procedure the microprocessor **50** performs is to access memory. Memory is accessed when data is read or written. Memory is also read when instructions are fetched. The microprocessor **50** is able to hide fetch of the next instruction behind the execution of the previously fetched instruction(s). The microprocessor **50** fetches instructions in 4-byte instruction groups. An instruction group may contain from one to four instructions. The amount of time required to execute the instruction group ranges from 4 cycles for simple instructions to 64 cycles for a multiply.

When a new instruction group is fetched, the microprocessor instruction decoder looks at the most significant bit of all four of the bytes. The most significant bit of an instruction determines if a memory access is required. For example, CALL, FETCH, and STORE all require a memory access to execute. If all four bytes have nonzero most significant bits, the microprocessor initiates the memory fetch of the next sequential 4-byte instruction group. When the last instruction in the group finishes executing, the next 4-byte instruction group is ready and waiting on the data bus needing only to be latched into the instruction register. If the 4-byte instruction group required four or more cycles to execute and the next sequential access was a column address strobe (CAS) cycle, the instruction fetch was completely overlapped with execution.

INTERNAL ARCHITECTURE

The microprocessor **50** architecture consists of the following:

PARAMETER STACK	<--> ALU* <-->	Y REGISTER RETURN STACK
<--- 32 BITS --- > 16 DEEP		<---32 BITS---> 16 DEEP
Used for math and logic.		Used for subroutine and interrupt return addresses as well as local variables.
Push down stack. Can overflow into off-chip RAM.		Push down stack. Can overflow into off-chip RAM. Can also be accessed relative to top of stack.
LOOP COUNTER		(32-bits, can decrement by 1) Used by class of test and loop instructions.
X REGISTER		(32-bits, can increment or decrement by 4). Used to point to RAM locations.
PROGRAM COUNTER		(32-bits, increments by 4). Points to 4-byte instruction groups in RAM.
INSTRUCTION REG		(32-Bits). Holds 4-byte instruction groups while they are being decoded and executed.

*Math and logic operations use the TOP item and NEXT to top Parameter Stack items as the operands. The result is pushed onto the Parameter Stack.

*Return addresses from subroutines are placed on the Return Stack. The Y REGISTER is used as a pointer to RAM locations. Since the Y REGISTER is the top item of the Return Stack, nesting of indices is straightforward.

MODE - A register with mode and status bits.

MODE-BITS:

Slow down memory accesses by 8 if "1". Run full speed if "0". (Provided for access to slow EPROM.)

Divide the system clock by 1023 if "1" to reduce power consumption. Run full speed if "0". (On-chip counters slow down if this bit is set.)

Enable external interrupt 1.

Enable external interrupt 2.

Enable external interrupt 3.

Enable external interrupt 4.

Enable external interrupt 5.

Enable external interrupt 6.

Enable external interrupt 7.

ON-CHIP MEMORY LOCATIONS:

MODE-BITS	
DMA-POINTER	
DMA-COUNTER	
STACK-POINTER	Pointer into Parameter Stack.
STACK-DEPTH	Depth of on-chip Parameter Stack
RSTACK-POINTER	Pointer into Return Stack
RSTACK-DEPTH	Depth of on-chip Return Stack

ADDRESSING MODE HIGH POINTS

The data bus is 32-bits wide. All memory fetches and stores are 32-bits. Memory bus addresses are 30 bits. The least significant 2 bits are used to select one-of-four bytes in some addressing modes. The Program Counter, X Register, and Y Register are implemented as D latches with their outputs going to the memory address bus and the bus incrementer/decrementer. Incrementing one of these registers can happen quickly, because the incremented value has already rippled through the inc/dec logic and need only be clocked into the latch. Branches and Calls are made to 32-bit word-boundaries.

INSTRUCTION SET

32-BIT INSTRUCTION FORMAT

The thirty two bit instructions are CALL, BRANCH, BRANCH-IF-ZERO, and LOOP-IF-NOT-DONE. These instructions require the calculation of an effective address. In many computers, the effective address is calculated by adding or subtracting an operand with the current Program Counter. This math operation requires from four to seven machine cycles to perform and can definitely bog down machine execution. The microprocessor's strategy is to perform the required math operation at assembly or linking time and do a much simpler "Increment to next page" or "Decrement to previous page" operation at run time. As a result, the microprocessor branches execute in a single cycle.

24-BIT OPERAND FORM:

Byte 1 Byte 2 Byte 3 Byte 4

WWWWWW XX - YYYYYYYY - YYYYYYYY - YYYYYYYY

With a 24-bit operand, the current page is considered to be defined by the most significant 6 bits of the Program Counter.

16-BIT OPERAND FORM:

QQQQQQQQ - WWWWWW XX - YYYYYYYY - YYYYYYYY

With a 16-bit operand, the current page is considered to be defined by the most significant 14 bits of the Program Counter.

8-BIT OPERAND FORM:

QQQQQQQQ - QQQQQQQQ - WWWWWW XX - YYYYYYYY

With an 8-bit operand, the current page is considered to be defined by the most significant 22 bits of the Program Counter.

QQQQQQQQ - Any 8-bit instruction.

WWWWWW - Instruction op-code.

XX - Select how the address bits will be used:

00 - Make all high-order bits zero. (Page zero addressing)

01 - Increment the high-order bits. (Use next page)

10 - Decrement the high-order bits. (Use previous page)

11 - Leave the high-order bits unchanged. (Use current page)

YYYYYYYY - The address operand field. This field is always shifted left two bits (to generate a word rather than byte address) and loaded into the Program Counter. The microprocessor instruction decoder figures out the width of the operand field by the location of the instruction op-code in the four bytes.

The compiler or assembler will normally use the shortest operand required to reach the desired address so that the leading bytes can be used to hold other instructions. The effective address is calculated by combining:

The current Program Counter,

The 8, 16, or 24 bit address operand in the instruction, Using one of the four allowed addressing modes.

EXAMPLES OF EFFECTIVE ADDRESS CALCULATION

Example 1:

Byte 1	Byte 2	Byte 3	Byte 4
QQQQQQQQ	QQQQQQQQ	00000011	10011000

The "QQQQQQQQs" in Byte **1** and **2** indicate space in the 4-byte memory fetch which could be hold two other instructions to be executed prior to the CALL instruction. Byte **3** indicates a CALL instruction (six zeros) in the current page (indicated by the 11 bits). Byte **4** indicates that the hexadecimal number 98 will be forced into the Program Counter bits **2** through **10**. (Remember, a CALL or BRANCH always goes to a word boundary so the two least

significant bits are always set to zero). The effect of this instruction would be to CALL a subroutine at WORD location HEX 98 in the current page. The most significant 22 bits of the Program Counter define the current page and will be unchanged.

Example 2:

Byte 1	Byte 2	Byte 3	Byte 4
000001 01	00000001	00000000	00000000

If we assume that the Program Counter was HEX 0000 0156 which is binary:

00000000 00000000 00000001 01010110 = OLD PROGRAM COUNTER.

Byte **1** indicates a BRANCH instruction op code (000001) and "01" indicates select the next page. Byte **2**,**3**, and **4** are the address operand . These 24-bits will be shifted to the left two places to define a WORD address. HEX 0156 shifted left two places is HEX 0558. Since this is a 24-bit operand instruction, the most significant 6 bits of the Program Counter define the current page. These six bits will be incremented to select the next page. Executing this instruction will cause the Program Counter to be loaded with HEX 0400 0558 which is binary:

00000100 00000000 00000101 01011000 = NEW PROGRAM COUNTER.

INSTRUCTIONS

CALL-LONG

0000 00XX - YYYYYYYY - YYYYYYYY - YYYYYYYY

Load the Program Counter with the effective WORD address specified. Push the current PC contents onto the RETURN STACK.

OTHER EFFECTS: CARRY or modes, no effect. May cause Return Stack to force an external memory cycle if on-chip Return Stack is full.

BRANCH

0000 01XX - YYYYYYYY - YYYYYYYY - YYYYYYYY

Load the Program Counter with the effective WORD address specified.

OTHER EFFECTS: NONE

BRANCH-IF-ZERO

0000 10XX - YYYYYYYY - YYYYYYYY - YYYYYYYY

Test the TOP value on the Parameter Stack. If the value is equal to zero, load the Program Counter with the effective WORD address specified. If the TOP value is not equal to zero, increment the Program Counter and fetch and execute the next instruction.

OTHER EFFECTS: NONE

LOOP-IF-NOT-DONE

0000 11YY - (XXXX XXXX) - (XXXX XXXX) - (XXXX XXXX)

If the LOOP COUNTER is not zero, load the Program Counter with the effective WORD address specified. If the LOOP COUNTER is zero, decrement the LOOP COUNTER, increment the Program Counter and fetch and execute the next instruction.

OTHER EFFECTS: NONE

8-BIT INSTRUCTIONS PHILOSOPHY

Most of the work in the microprocessor **50** is done by the 8-bit instructions. Eight bit instructions are possible with the microprocessor because of the extensive use of implied stack addressing. Many 32-bit architectures use 8-bits to specify the operation to perform but use an additional 24-bits to specify two sources and a destination.

For math and logic operations, the microprocessor **50** exploits the inherent advantage of a stack by designating the source operand(s) as the top stack item and the next stack item. The math or logic operation is performed, the operands are popped from the stack, and the result is pushed back on the stack. The result is a very efficient utilization of instruction bits as well as registers. A comparable situation exists between Hewlett Packard calculators (which use a stack) and Texas Instrument calculators which don't. The identical operation on an HP will require one half to one third the keystrokes of the TI.

The availability of 8-bit instructions also allows another architectural innovation, the fetching of four instructions in a single 32-bit memory cycle. The advantages of fetching multiple instructions are:

Increased execution speed even with slow memories,

Similar performance to the Harvard (separate data and instruction busses) without the expense,

Opportunities to optimize groups of instructions,

The capability to perform loops within this mini-cache. The microloops inside the four instruction group are effective for searches and block moves.

SKIP INSTRUCTIONS

The microprocessor **50** fetches instructions in 32-bit chunks called 4-byte instruction groups. These four bytes may contain four 8-bit instructions or some mix of 8-bit and 16 or 24-bit instructions. SKIP instructions in the microprocessor skip any remaining instructions in a 4-byte instruction group and cause a memory fetch to get the next 4-byte instruction group. Conditional SKIPs when combined with 3-byte BRANCHES will create conditional BRANCHES. SKIPs may also be used in situations when no use can be made of the remaining bytes in a 4-instruction group. A SKIP executes in a single cycle, whereas a group of three NOPs would take three cycles.

SKIP-ALWAYS -	skip any remaining instructions in this 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group.
SKIP-IF-ZERO -	If the TOP item of the Parameter Stack is zero, skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is not zero, execute the next sequential instruction.
SKIP-IF-POSITIVE -	If the TOP item of the Parameter Stack has a the most significant bit (the sign bit) equal to "0", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is not "0", execute the next sequential instruction.

-continued

SKIP-IF-NO-CARRY -	If the CARRY flag from a SHIFT or arithmetic operation is not equal to "1", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the CARRY is equal to "1", execute the next sequential instruction.
SKIP-NEVER (NOP)	Execute the next sequential instruction. (Delay one machine cycle).
SKIP-IF-NOT-ZERO -	If the TOP item on the Parameter Stack is not equal to "0", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is equal 0", execute the next sequential instruction.
SKIP-IF-NEGATIVE -	If the TOP item on the Parameter Stack has its most significant bit (sign bit) set to "1", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item has its most significant bit set to "0", execute the next sequential instruction.
SKIP-IF-CARRY -	If the CARRY flag is set to "1" as a result of SHIFT or arithmetic operation, skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the CARRY flag is "0", execute the next sequential instruction.

MICROLOOPS

Microloops are a unique feature of the microprocessor architecture which allows controlled looping within a 4-byte instruction group. A microloop instruction tests the LOOP COUNTER for "0" and may perform an additional test. If the LOOP COUNTER is not "0" and the test is met, instruction execution continues with the first instruction in the 4-byte instruction group, and the LOOP COUNTER is decremented. A microloop instruction will usually be the last byte in a 4-byte instruction group, but it can be any byte. If the LOOP COUNTER is "0" or the test is not met, instruction execution continues with the next instruction. If the microloop is the last byte in the 4-byte instruction group, the most significant 30-bits of the Program Counter are incremented and the next 4-byte instruction group is fetched from memory. On a termination of the loop on LOOP COUNTER equal to "0", the LOOP COUNTER will remain at "0". Microloops allow short iterative work such as moves and searches to be performed without slowing down to fetch instructions from memory.

EXAMPLE:

Byte 1 FETCH-VIA-X-AUTOINCREMENT	Byte 2 STORE-VIA-Y-AUTO-INCREMENT
Byte 3 ULOOP-UNTIL-DONE	Byte 4 QQQQQQQQ

This example will perform a block move. To initiate the transfer, X will be loaded with the starting address of the source. Y will be loaded with the starting address of the destination. The LOOP COUNTER will be loaded with the number of 32-bit words to move. The microloop will FETCH and STORE and count down the LOOP COUNTER until it reaches zero. QQQQQQQQ indicates any instruction can follow.

MICROLOOP INSTRUCTIONS

ULOOP-UNTIL-DONE—If the LOOP COUNTER is not "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0", continue execution with the next instruction.

ULOOP-IF-ZERO—If the LOOP COUNTER is not "0" and the TOP item on the Parameter Stack is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

ULOOP-IF-POSITIVE—If the LOOP COUNTER is not "0" and the most significant bit (sign bit) is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

ULOOP-IF-NOT-CARRY-CLEAR—If the LOOP COUNTER is not "0" and the floating point exponents found in TOP and NEXT are not aligned, continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the exponents are aligned, continue execution with the next instruction. This instruction is specifically designed for combination with special SHIFT instructions to align two floating point numbers.

ULOOP-NEVER—(DECREMENT-LOOP-COUNTER) Decrement the LOOP COUNTER. Continue execution with the next instruction.

ULOOP-IF-NOT-ZERO—If the LOOP COUNTER is not "0" and the TOP item of the Parameter Stack is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

ULOOP-IF-NEGATIVE—If the LOOP COUNTER is not "0" and the most significant bit (sign bit) of the TOP item of the Parameter Stack is "1", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the most significant bit of the Parameter Stack is "0", continue execution with the next instruction.

ULOOP-IF-CARRY-SET—If the LOOP COUNTER is not "0" and the exponents of the floating point numbers found in TOP and NEXT are not aligned, continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the exponents are aligned, continue execution with the next instruction.

RETURN FROM SUBROUTINE OR INTERRUPT

Subroutine calls and interrupt acknowledgements cause a redirection of normal program execution. In both cases, the current Program Counter is pushed onto the Return Stack, so the microprocessor can return to its place in the program after executing the subroutine or interrupt service routine.

NOTE: When a CALL to subroutine or interrupt is acknowledged the Program Counter has already been incremented and is pointing to the 4-byte instruction group following the 4-byte group currently being executed. The instruction decoding logic allows the microprocessor to

perform a test and execute a return conditional on the outcome of the test in a single cycle. A RETURN pops an address from the Return Stack and stores it to the Program Counter.

RETURN INSTRUCTIONS	
RETURN-ALWAYS -	Pop the top item from the Return Stack and transfer it to the Program Counter.
RETURN-IF-ZERO -	If the TOP item on the Parameter Stack is "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.
RETURN-IF-POSITIVE -	If the most significant bit (sign bit) of the TOP item on the Parameter Stack is a "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.
RETURN-IF-CARRY-CLEAR -	If the exponents of the floating point numbers found in TOP and NEXT are not aligned, pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.
RETURN-NEVER - (NOP)	Execute the next instruction.
RETURN-IF-NOT-ZERO -	If the TOP item on the Parameter Stack is not "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.
RETURN-IF-NEGATIVE -	If the most significant bit (sign bit) of the TOP item on the Parameter Stack is a "1", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.
RETURN-IF-CARRY-SET -	If the exponents of the floating point numbers found in TOP and NEXT are aligned, pop the top item from the Return Stack and transfer it to the Program. Counter. Otherwise execute the next instruction.

HANDLING MEMORY FROM DYNAMIC RAM

The microprocessor **50**, like any RISC type architecture, is optimized to handle as many operations as possible on-chip for maximum speed. External memory operations take from 80 nsec. to 220 nsec. compared with on-chip memory speeds of from 4 nsec. to 30 nsec. There are times when external memory must be accessed.

External memory is accessed using three registers:

X-REGISTER—A 30-bit memory pointer which can be used for memory access and simultaneously incremented or decremented.

Y-REGISTER—A 30-bit memory pointer which can be used for memory access and simultaneously incremented or decremented.

PROGRAM-COUNTER—A 30-bit memory pointer normally used to point to 4-byte instruction groups. External memory may be accessed at addresses relative to the PC. The operands are sometimes called "Immediate" or "Literal" in other computers. When used as memory pointer, the PC is also incremented after each operation.

MEMORY LOAD & STORE INSTRUCTIONS

FETCH-VIA-X—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. X is unchanged.

FETCH-VIA-Y—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. Y is unchanged.

FETCH-VIA-X-AUTOINCREMENT—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of X to point to the next 32-bit word address.

FETCH-VIA-Y-AUTOINCREMENT—Fetch the 32-bit memory content pointed to by Y and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of Y to point to the next 32-bit word address.

FETCH-VIA-X-AUTODECREMENT—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. After fetching, decrement the most significant 30 bits of X to point to the previous 32-bit word address.

FETCH-VIA-Y-AUTODECREMENT—Fetch the 32-bit memory content pointed to by Y and push it onto the Parameter Stack. After fetching, decrement the most significant 30 bits of Y to point to the previous 32-bit word address.

STORE-VIA-X—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. X is unchanged.

STORE-VIA-Y—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. Y is unchanged.

STORE-VIA-X-AUTOINCREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. After storing, increment the most significant 30 bits of X to point to the next 32-bit word address.

STORE-VIA-Y-AUTOINCREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. After storing, increment the most significant 30 bits of Y to point to the next 32-bit word address.

STORE-VIA-X-AUTODECREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. After storing, decrement the most significant 30 bits of X to point to the previous 32-bit word address.

STORE-VIA-Y-AUTODECREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. After storing, decrement the most significant 30 bits of Y to point to the previous 32-bit word address.

FETCH-VIA-PC—Fetch the 32-bit memory content pointed to by the Program Counter and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of the Program Counter to point to the next 32-bit word address.

*NOTE When this instruction executes, the PC is pointing to the memory location following the instruction. The effect is of loading a 32-bit immediate operand. This is an 8-bit instruction and therefore will be combined with other 8-bit instructions in a 4-byte instruction fetch. It is possible to have from one to four FETCH-VIA-PC instructions in a 4-byte instruction fetch. The PC incre-

ments after each execution of FETCH-VIA-PC, so it is possible to push four immediate operands on the stack. The four operands would be the found in the four memory locations following the instruction.

BYTE-FETCH-VIA-X—Fetch the 32-bit memory content pointed to by the most significant 30 bits of X. Using the two least significant bits of X, select one of four bytes from the 32-bit memory fetch, right justify the byte in a 32-bit field and push the selected byte preceded by leading zeros onto the Parameter Stack.

BYTE-STORE-VIA-X—Fetch the 32-bit memory content pointed to by the most significant 30 bits of X. Pop the TOP item from the Parameter Stack. Using the two least significant bits of X place the least significant byte into the 32-bit memory data and write the 32-bit entity back to the location pointed to by the most significant 30 bits of X.

OTHER EFFECTS OF MEMORY ACCESS INSTRUCTIONS:

Any FETCH instruction will push a value on the Parameter Stack **74**. If the on-chip stack is full, the stack will overflow into off-chip memory stack resulting in an additional memory cycle. Any STORE instruction will pop a value from the Parameter Stack **74**. If the on-chip stack is empty, a memory cycle will be generated to fetch a value from off-chip memory stack.

HANDLING ON-CHIP VARIABLES

High-level languages often allow the creation of LOCAL VARIABLES. These variables are used by a particular procedure and discarded. In cases of nested procedures, layers of these variables must be maintained. On-chip storage is up to five times faster than off-chip RAM, so a means of keeping local variables on-chip can make operations run faster. The microprocessor **50** provides the capability for both on-chip storage of local variables and nesting of multiple levels of variables through the Return Stack.

The Return Stack **134** is implemented as 16 on-chip RAM locations. The most common use for the Return Stack **134** is storage of return addresses from subroutines and interrupt calls. The microprocessor allows these 16 locations to also be used as addressable registers. The 16 locations may be read and written by two instructions which indicate a Return Stack relative address from 0–15. When high-level procedures are nested, the current procedure variables push the previous procedure variables further down the Return Stack **134**. Eventually, the Return Stack will automatically overflow into off-chip RAM.

ON-CHIP VARIABLE INSTRUCTIONS

READ-LOCAL-VARIABLE XXXX—Read the XXXXth location relative to the top of the Return Stack. (XXXX is a binary number from 0000–1111). Push the item read onto the Parameter Stack.

OTHER EFFECTS: If the Parameter Stack is full, the push operation will cause a memory cycle to be generated as one item of the stack is automatically stored to external RAM. The logic which selects the location performs a modulo 16 subtraction. If four local variables have been pushed onto the Return Stack, and an instruction attempts to READ the fifth item, unknown data will be returned.

WRITE-LOCAL-VARIABLE XXXX—Pop the TOP item of the Parameter Stack and write it into the XXXXth location relative to the top of the Return Stack. (XXXX is a binary number from 0000–1111.)

OTHER EFFECTS: If the Parameter Stack is empty, the pop operation will cause a memory cycle to be generated to fetch the Parameter Stack item from external RAM. The logic which selects the location performs a modulo 16 subtraction. If four local variables have been pushed onto the Return Stack, and an instruction attempts to WRITE to the fifth item, it is possible to clobber return addresses or wreak other havoc.

REGISTER AND FLIP-FLOP TRANSFER AND PUSH INSTRUCTIONS

DROP—Pop the TOP item from the Parameter Stack and discard it.

SWAP—Exchange the data in the TOP Parameter Stack location with the data in the NEXT Parameter Stack location.

DUP—Duplicate the TOP item on the Parameter Stack and push it onto the Parameter Stack.

PUSH-LOOP-COUNTER—Push the value in LOOP COUNTER onto the Parameter Stack.

POP-RSTACK-PUSH-TO-STACK—Pop the top item from the Return Stack and push it onto the Parameter Stack.

PUSH-X-REG—Push the value in the X Register onto the Parameter Stack.

PUSH-STACK-POINTER—Push the value of the Parameter Stack pointer onto the Parameter Stack.

PUSH-RSTACK-POINTER—Push the value of the Return Stack pointer onto the Return Stack.

PUSH-MODE-BITS—Push the value of the MODE REGISTER onto the Parameter Stack.

PUSH-INPUT—Read the 10 dedicated input bits and push the value (right justified and padded with leading zeros) onto the Parameter Stack.

SET-LOOP-COUNTER—Pop the TOP value from the Parameter Stack and store it into LOOP COUNTER.

POP-STACK-PUSH-TO-RSTACK—Pop the TOP item from the Parameter Stack and push it onto the Return Stack.

SET-X-REG—Pop the TOP item from the Parameter Stack and store it into the X Register.

SET-STACK-POINTER—Pop the TOP item from the Parameter Stack and store it into the Stack Pointer.

SET-RSTACK-POINTER—Pop the TOP item from the Parameter Stack and store it into the Return Stack Pointer.

SET-MODE-BITS—Pop the TOP value from the Parameter Stack and store it into the MODE BITS.

SET-OUTPUT—Pop the TOP item from the Parameter Stack and output it to the 10 dedicated output bits.

OTHER EFFECTS: Instructions which push or pop the Parameter Stack or Return Stack may cause a memory cycle as the stacks overflow back and forth between on-chip and off-chip memory.

LOADING A SHORT LITERAL

A special case of register transfer instruction is used to push an 8-bit literal onto the Parameter Stack. This instruction requires that the 8-bits to be pushed reside in the last byte of a 4-byte instruction group. The instruction op-code loading the literal may reside in ANY of the other three bytes in the instruction group.

EXAMPLE:

BYTE 1	BYTE 2	BYTE 3
LOAD-SHORT-LITERAL	QQQQQQQQ	QQQQQQQQ
BYTE 4		
00001111		

In this example, QQQQQQQQ indicates any other 8-bit instruction. When Byte **1** is executed, binary 00001111 (HEX 0f) from Byte **4** will be pushed (right justified and padded by leading zeros) onto the Parameter Stack. Then the instructions in Byte **2** and Byte **3** will execute. The microprocessor instruction decoder knows not to execute Byte **4**. It is possible to push three identical 8-bit values as follows:

BYTE 1	BYTE 2
LOAD-SHORT-LITERAL	LOAD-SHORT-LITERAL
BYTE 3	BYTE 4
LOAD-SHORT-LITERAL	00001111
SHORT-LITERAL-INSTRUCTION	
LOAD-SHORT-LITERAL -	Push the 8-bit value found in Byte 4 of the current 4-byte instruction group onto the Parameter Stack.

LOGIC INSTRUCTIONS

Logical and math operations used the stack for the source of one or two operands and as the destination for results. The stack organization is a particularly convenient arrangement for evaluating expressions. TOP indicates the top value on the Parameter Stack **74**. NEXT indicates the next to top value on the Parameter Stack **74**.

AND—Pop TOP and NEXT from the Parameter Stack, perform the logical AND operation on these two operands, and push the result onto the Parameter Stack.

OR—Pop TOP and NEXT from the Parameter Stack, perform the logical OR operation on these two operands, and push the result onto the Parameter Stack.

XOR—Pop TOP and NEXT from the Parameter Stack, perform the logical exclusive OR on these two operands, and push the result onto the Parameter Stack.

BIT-CLEAR—Pop TOP and NEXT from the Parameter Stack, toggle all bits in NEXT, perform the logical AND operation on TOP, and push the result onto the Parameter Stack. (Another way of understanding this instruction is thinking of it as clearing all bits in TOP that are set in NEXT.)

MATH INSTRUCTIONS

Math instruction pop the TOP item and NEXT to top item of the Parameter Stack **74** to use as the operands. The results are pushed back on the Parameter Stack. The CARRY flag is used to latch the "33rd bit" of the ALU result.

ADD—Pop the TOP item and NEXT to top item from the Parameter Stack, add the values together and push the result back on the Parameter Stack. The CARRY flag may be changed.

ADD-WITH-CARRY—Pop the TOP item and the NEXT to top item from the Parameter Stack, add the values together. If the CARRY flag is "1" increment the result. Push the ultimate result back on the Parameter Stack. The CARRY flag may be changed.

ADD-X—Pop the TOP item from the Parameter Stack and read the third item from the top of the Parameter Stack. Add the values together and push the result back on the Parameter Stack. The CARRY flag may be changed.

SUB—Pop the TOP item and NEXT to top item from the Parameter Stack, Subtract NEXT from TOP and push the result back on the Parameter Stack. The CARRY flag may be changed.

SUB-WITH-CARRY—Pop the TOP item and NEXT to top item from the Parameter Stack. Subtract NEXT from TOP. If the CARRY flag is "1" increment the result. Push the ultimate result back on the Parameter Stack. The CARRY flag may be changed.

SUB-X—

SIGNED-MULT-STEP—

UNSIGNED-MULT-STEP—

SIGNED-FAST-MULT—

FAST-MULT-STEP—

UNSIGNED-DIV-STEP—

GENERATE-POLYNOMIAL

ROUND—

COMPARE—Pop the TOP item and NEXT to top item from the Parameter Stack. Subtract NEXT from TOP. If the result has the most significant bit equal to "0" (the result is positive), push the result onto the Parameter Stack. If the result has the most significant bit equal to "1" (the result is negative), push the old value of TOP onto the Parameter Stack. The CARRY flag may be affected.

SHIFT/ROTATE

SHIFT-LEFT—Shift the TOP Parameter Stack item left one bit. The CARRY flag is shifted into the least significant bit of TOP.

SHIFT-RIGHT—Shift the TOP Parameter Stack item right one bit. The least significant bit of TOP is shifted into the CARRY flag. Zero is shifted into the most significant bit of TOP.

DOUBLE-SHIFT-LEFT—Treating the TOP item of the Parameter Stack as the most significant word of a 64-bit number and the NEXT stack item as the least significant word, shift the combined 64-bit entity left one bit. The CARRY flag is shifted into the least significant bit of NEXT.

DOUBLE-SHIFT-RIGHT—Treating the TOP item of the Parameter Stack as the most significant word of a 64-bit number and the NEXT stack item as the least significant word, shift the combined 64-bit entity right one bit. The least significant bit of NEXT is shifted into the CARRY flag. Zero is shifted into the most significant bit of TOP.

OTHER INSTRUCTIONS

FLUSH-STACK—Empty all on-chip Parameter Stack locations into off-chip RAM. (This instruction is useful for multitasking applications). This instruction accesses a counter which holds the depth of the on-chip stack and can require from none to 16 external memory cycles.

FLUSH-RSTACK—Empty all on-chip Return Stack locations into off-chip RAM. (This instruction is useful for multitasking applications). This instruction accesses a counter which holds the depth of the on-chip Return Stack and can require from none to 16 external memory cycles.

It should further be apparent to those skilled in the art that various changes in form and details of the invention as shown and described may be made. It is intended that such changes be included within the spirit and scope of the claims appended hereto.

What is claimed is:

1. A microprocessor, which comprises a main central processing unit and a separate direct memory access central processing unit in a single integrated circuit comprising said microprocessor, said main central processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus, said internal data bus being bidirectionally connected to a loop counter, said loop counter being connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register, said internal data bus being connected to a memory controller, to a Y register of a return push down stack, an X register and a program counter, said Y register, X register and program counter providing outputs to an internal address bus, said internal address bus providing inputs to said memory controller and to an incrementer, said incrementer being connected to said internal data bus, said direct memory access central processing unit providing inputs to said memory controller, said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory.

2. The microprocessor of claim 1 in which said memory controller includes a multiplexing means between said central processing unit and said address/data bus, said multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus.

3. The microprocessor of claim 1 in which said memory controller includes means for fetching instructions for said central processing unit on said address/data bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle.

4. The microprocessor of claim 3 additionally comprising means connected to said means for fetching instructions for determining if multiple instructions fetched by said means for fetching instructions require a memory access, said means for fetching instructions fetching additional multiple instructions if the multiple instructions do not require a memory access.

5. The microprocessor of claim 3 in which said microprocessor and a dynamic random access memory are contained in a single integrated circuit and said means for fetching instructions includes a column latch for receiving the multiple instructions.

6. The microprocessor of claim 1 in which said microprocessor includes a sensing circuit and a driver circuit, and an output enable line for connection between the random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level, said microprocessor being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

7. The microprocessor of claim 1 additionally comprising a ring oscillator variable speed system clock connected to said main central processing unit, said main central processing unit and said ring oscillator variable speed system clock being provided in a single integrated circuit.

8. The microprocessor of claim 7 in which said memory controller includes an input/output interface connected to exchange coupling control signals, addresses and data with said main central processing unit, said microprocessor additionally including a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.

9. The microprocessor of claim 1 in which said first push down stack has a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit.

10. The microprocessor of claim 9 additionally comprising a first pointer connected to said first plurality of stack elements, a second pointer connected to said second plurality of stack elements, and a third pointer connected to said third plurality of stack elements, said central processing unit being connected to pop items from said first plurality of stack elements, said first stack pointer being connected to said second stack pointer to pop a first plurality of items from said second plurality of stack elements when said first plurality of stack elements are empty from successive pop operations by said central processing unit, said second stack pointer being connected to said third stack pointer to pop a second plurality of items from said third plurality of stack elements when said second plurality of stack elements are empty from successive pop operations by said central processing unit.

* * * * *

US005530890C1

(12) EX PARTE REEXAMINATION CERTIFICATE (8052nd)

United States Patent
Moore et al.

(10) **Number: US 5,530,890 C1**
(45) **Certificate Issued: Mar. 1, 2011**

(54) **HIGH PERFORMANCE, LOW COST MICROPROCESSOR**

(75) Inventors: **Charles H. Moore**, Woodside, CA (US); **Russell H. Fish, III**, Mt. View, CA (US)

(73) Assignee: **Patriot Scientific Corporation**, San Diego, CA (US)

Reexamination Request:
No. 90/009,388, Jan. 16, 2009

Reexamination Certificate for:
Patent No.: **5,530,890**
Issued: **Jun. 25, 1996**
Appl. No.: **08/480,206**
Filed: **Jun. 7, 1995**

Related U.S. Application Data

(62) Division of application No. 07/389,334, filed on Aug. 3, 1989, now Pat. No. 5,440,749.

(51) **Int. Cl.**
G06F 15/76 (2006.01)

(52) **U.S. Cl.** **712/32**; 711/E12.02; 712/E9.016; 712/E9.028; 712/E9.046; 712/E9.055; 712/E9.057; 712/E9.058; 712/E9.062; 712/E9.078; 712/E9.08; 712/E9.081

(58) **Field of Classification Search** ..... None
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,603,934 A 9/1971 Heath, Jr. et al.
3,696,414 A 10/1972 Allen et al.
3,810,117 A 5/1974 Healey
3,849,765 A 11/1974 Hamano
3,878,513 A 4/1975 Werner

(Continued)

FOREIGN PATENT DOCUMENTS

EP 113516 A2 7/1984
EP 200797 A1 11/1986

(Continued)

OTHER PUBLICATIONS

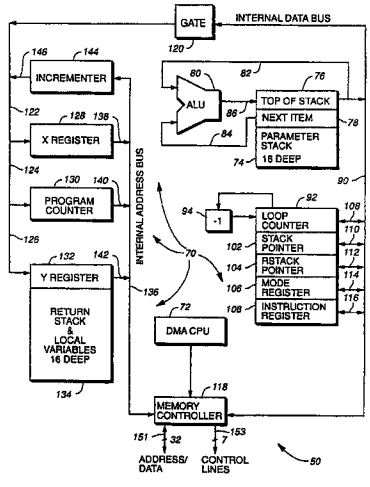
"35ns 256K Device, VLSI Debuts SRAM Designed With Hitachi," Electronic News, p. 25 (Apr. 17, 1989).

(Continued)

Primary Examiner—Joseph R. Pokrzywa

(57) **ABSTRACT**

A microprocessor (**50**) includes a main central processing unit (CPU) (**70**) and a separate direct memory access (DMA) CPU (**72**) in a single integrated circuit making up the microprocessor (**50**). The main CPU (**70**) has a first 16 deep push down stack (**74**), which has a top item register (**76**) and a next item register (**78**), respectively connected to provide inputs to an arithmetic logic unit (ALU) (**80**) by lines (**82**) and (**84**). An output of the ALU (**80**) is connected to the top item register (**76**) by line (**86**). The output of the top item register (**82**) is also connected by line (**88**) to an internal data bus (**90**). A loop counter (**92**) is connected to a decrementer (**94**) by lines (**96**) and (**98**). The loop counter (**92**) is birectionally connected to the internal data bus (**90**) by line (**100**). Stack pointer (**102**), return stack pointer (**104**), mode register (**106**) and instruction register (**108**) are also connected to the internal data bus (**90**) by lines (**110**), (**112**), (**114**) and (**116**), respectively. The internal data bus (**90**) is connected to memory controller (**118**) and to gate (**120**). The gate (**120**) provides inputs on lines (**122**), (**124**), and (**126**) to X register (**128**), program counter (**130**) and Y register (**132**) of return push down stack (**134**). The X register (**128**), program counter (**130**) and Y register (**132**) provide outputs to internal address bus (**136**) on lines (**138**), (**140**) and (**142**). The internal address bus provides inputs to the memory controller (**118**) and to an incremeter (**144**). The incrementer (**144**) provides inputs to the X register, program counter and Y register via lines (**146**), (**122**), (**124**) and (**126**). The DMA CPU (**72**) provides inputs to the memory controller (**118**) on line (**148**). The memory controller (**118**) is connected to RAM by address/data bus (**150**) and control lines (**152**).



U.S. PATENT DOCUMENTS

3,919,695	A	11/1975	Gooding
3,924,245	A	12/1975	Eaton et al.
3,930,688	A	1/1976	Rau et al.
3,967,104	A	6/1976	Brantingham et al.
3,968,501	A	7/1976	Gilbert
3,969,706	A	7/1976	Proebsting et al.
3,976,977	A	8/1976	Porter et al.
3,980,993	A	9/1976	Bredart et al.
3,988,717	A	10/1976	Kisylia
4,003,028	A	1/1977	Bennett et al.
4,003,033	A	1/1977	O'Keefe et al.
4,016,545	A	4/1977	Lipovski
4,037,090	A	7/1977	Raymond, Jr.
4,042,972	A	8/1977	Gruner et al.
4,050,058	A	9/1977	Garlic
4,050,096	A	9/1977	Bennett et al.
4,050,297	A	9/1977	Pettingell et al.
4,067,058	A	1/1978	Brandstaetter et al.
4,067,059	A	1/1978	Derchak
4,075,691	A	2/1978	Davis et al.
4,079,338	A	3/1978	Kronlage
4,079,455	A	3/1978	Ozga
4,107,773	A	8/1978	Gilbreath et al.
4,110,822	A	8/1978	Porter et al.
4,112,490	A	9/1978	Pohlman et al.
4,125,871	A	11/1978	Martin
4,128,873	A	12/1978	Lamiaux
4,144,562	A	3/1979	Cooper
4,181,938	A	1/1980	Suzuki et al.
4,215,401	A	7/1980	Holsztynski et al.
4,217,637	A	8/1980	Faulkner et al.
4,217,652	A	8/1980	Klaus et al.
4,223,380	A	9/1980	Antonaccio et al.
4,223,880	A	9/1980	Brems
4,224,676	A	9/1980	Appelt
4,236,152	A	11/1980	Masuzawa et al.
4,240,137	A	12/1980	Matsumoto et al.
4,242,735	A	12/1980	Sexton
4,253,785	A	3/1981	Bronstein
4,255,785	A	3/1981	Chamberlin
4,292,668	A	9/1981	Miller et al.
4,295,193	A	10/1981	Pomerene
4,305,045	A	12/1981	Metz et al.
4,315,305	A	2/1982	Siemon
4,315,308	A	2/1982	Jackson
4,317,227	A	2/1982	Skerlos
4,320,467	A	3/1982	Glass
4,321,706	A	3/1982	Craft
4,328,557	A	5/1982	Gastinel
4,334,268	A	6/1982	Boney et al.
4,335,447	A	6/1982	Jerrim
4,338,675	A	7/1982	Palmer et al.
4,348,720	A	9/1982	Blahut et al.
4,348,743	A	9/1982	Dozier
4,354,228	A	10/1982	Moore et al.
4,358,728	A	11/1982	Hashimoto
4,361,869	A	11/1982	Johnson et al.
4,364,112	A	12/1982	Onodera et al.
4,376,977	A	3/1983	Bruinshorst
4,382,279	A	5/1983	Ugon
4,390,946	A	6/1983	Lane
4,396,979	A	8/1983	Mor et al.
4,398,263	A	8/1983	Ito
4,398,265	A	8/1983	Puhl et al.
4,402,042	A	8/1983	Guttag
4,403,303	A	9/1983	Howes et al.
4,412,283	A	10/1983	Mor et al.
4,425,628	A	1/1984	Bedard et al.
4,449,201	A	5/1984	Clark
4,450,519	A	5/1984	Guttag et al.
4,453,229	A	6/1984	Schaire
4,462,073	A	7/1984	Grondalski
4,463,421	A	7/1984	Laws
4,467,420	A	8/1984	Murakami et al.
4,467,444	A	8/1984	Harmon, Jr. et al.
4,467,810	A	8/1984	Vollmann
4,471,426	A	9/1984	McDonough
4,472,789	A	9/1984	Sibley
4,488,217	A	12/1984	Binder et al.
4,488,227	A	12/1984	Miu et al.
4,491,938	A	1/1985	Leach
4,494,021	A	1/1985	Bell et al.
4,494,187	A	1/1985	Simpson
4,503,500	A	3/1985	Magar
4,509,115	A	4/1985	Manton et al.
4,538,239	A	8/1985	Magar
4,539,655	A	9/1985	Trussell et al.
4,541,045	A	9/1985	Kromer, III
4,541,111	A	9/1985	Takashima et al.
4,553,201	A	11/1985	Pollack, Jr.
4,556,063	A	12/1985	Thompson et al.
4,558,176	A	12/1985	Arnold et al.
4,562,537	A	12/1985	Barnett et al.
4,566,063	A	1/1986	Zolnowsky et al.
4,571,709	A	2/1986	Skupnjak et al.
4,577,282	A	3/1986	Caudel et al.
4,586,127	A	4/1986	Horvath
4,607,332	A	8/1986	Goldberg
4,616,338	A	10/1986	Helen et al.
4,626,798	A	12/1986	Fried
4,626,985	A	12/1986	Briggs
4,626,988	A	12/1986	George
4,627,082	A	12/1986	Pelgrom et al.
4,630,195	A	12/1986	Hester et al.
4,630,934	A	12/1986	Arber
4,641,246	A	2/1987	Halbert et al.
4,649,471	A	3/1987	Briggs et al.
4,660,155	A	4/1987	Thaden et al.
4,660,180	A	4/1987	Tanimura et al.
4,665,495	A	5/1987	Thaden
4,670,837	A	6/1987	Sheets
4,679,166	A	7/1987	Berger et al.
4,680,698	A	7/1987	Edwards et al.
4,689,581	A	8/1987	Talbot
4,691,124	A	9/1987	Ledzius et al.
4,698,750	A	10/1987	Wilkie et al.
4,701,884	A	10/1987	Aoki et al.
4,704,678	A	11/1987	May
4,708,490	A	11/1987	Arber
4,709,329	A	11/1987	Hecker
4,710,648	A	12/1987	Hanamura et al.
4,713,749	A	12/1987	Magar et al.
4,714,994	A	12/1987	Oklobdzija et al.
4,718,081	A	1/1988	Brenig
4,720,812	A	1/1988	Kao et al.
4,724,517	A	2/1988	May
4,739,475	A	4/1988	Mensch, Jr.
4,750,111	A	6/1988	Crosby, Jr. et al.
4,758,948	A	7/1988	May et al.
4,760,521	A	7/1988	Rehwald et al.
4,761,763	A	8/1988	Hicks
4,763,297	A	8/1988	Uhlenhoff
4,766,567	A	8/1988	Kato
4,772,888	A	9/1988	Kimura
4,777,591	A	10/1988	Chang et al.
4,780,814	A	10/1988	Hayek
4,782,439	A	11/1988	Borkar et al.
4,783,734	A	11/1988	May et al.
4,783,764	A	11/1988	Tsuchiya et al.
4,787,032	A	11/1988	Culley
4,791,590	A	12/1988	Ku et al.

4,794,526	A		12/1988	May et al.
4,794,558	A		12/1988	Thompson
4,797,850	A		1/1989	Amitai
4,803,621	A		2/1989	Kelly
4,805,091	A		2/1989	Thiel et al.
4,809,169	A		2/1989	Sfarti et al.
4,809,269	A		2/1989	Gulick
4,811,208	A		3/1989	Myers et al.
4,816,989	A		3/1989	Finn et al.
4,816,996	A		3/1989	Hill et al.
4,819,151	A		4/1989	May
4,833,599	A		5/1989	Colwell et al.
4,835,733	A		5/1989	Powell
4,835,738	A		5/1989	Niehaus et al.
4,837,563	A		6/1989	Mansfield et al.
4,837,682	A		6/1989	Culler
4,847,752	A		7/1989	Akashi
4,847,757	A		7/1989	Smith
4,849,875	A		7/1989	Fairman et al.
4,853,841	A		8/1989	Richter
4,860,198	A		8/1989	Takenaka
4,868,735	A		9/1989	Moller et al.
4,870,562	A		9/1989	Kimoto et al.
4,872,003	A		10/1989	Yoshida
4,882,710	A		11/1989	Hashimoto et al.
4,885,785	A		12/1989	Reynolds et al.
4,890,225	A		12/1989	Ellis, Jr. et al.
4,899,275	A		2/1990	Sachs et al.
4,907,225	A		3/1990	Gulick et al.
4,910,703	A		3/1990	Ikeda et al.
4,912,632	A		3/1990	Gach et al.
4,914,578	A		4/1990	MacGregor et al.
4,924,384	A		5/1990	Hao et al.
4,926,323	A		5/1990	Baror et al.
4,931,748	A		6/1990	McDermott et al.
4,931,986	A		6/1990	Daniel et al.
4,933,835	A		6/1990	Sachs et al.
4,942,553	A		7/1990	Dalrymple et al.
4,956,811	A		9/1990	Kajigaya et al.
4,959,782	A		9/1990	Tulpule et al.
4,967,326	A		10/1990	May
4,967,352	A		10/1990	Keida et al.
4,967,398	A		10/1990	Jamoua et al.
4,969,091	A		11/1990	Muller
4,974,157	A		11/1990	Winfield et al.
4,979,102	A		12/1990	Tokuume
4,980,821	A		12/1990	Koopman et al.
4,984,176	A		1/1991	Van den Heuvel
4,988,892	A		1/1991	Needle
4,989,113	A	*	1/1991	Asal 710/22
4,989,133	A		1/1991	May et al.
4,989,135	A		1/1991	Miki
4,990,847	A		2/1991	Ishimaru et al.
5,008,816	A		4/1991	Fogg, Jr. et al.
5,013,985	A		5/1991	Itoh et al.
5,021,991	A		6/1991	MacGregor et al.
5,022,395	A		6/1991	Russie
5,023,689	A		6/1991	Sugawara
5,031,092	A		7/1991	Edwards et al.
5,036,300	A		7/1991	Nicolai
5,036,460	A		7/1991	Takahira et al.
5,047,921	A		9/1991	Kinter et al.
5,053,952	A		10/1991	Koopman, Jr. et al.
5,068,781	A		11/1991	Gillett, Jr. et al.
5,070,451	A		12/1991	Moore et al.
5,081,574	A		1/1992	Larsen et al.
5,091,846	A		2/1992	Sachs et al.
5,097,437	A		3/1992	Larson
5,103,499	A		4/1992	Miner et al.
5,107,457	A		4/1992	Hayes et al.
5,109,495	A		4/1992	Fite et al.
5,121,502	A		6/1992	Rau et al.
5,127,091	A		6/1992	Boufarah et al.
5,127,092	A		6/1992	Gupta et al.
5,133,064	A		7/1992	Hotta et al.
5,134,701	A		7/1992	Mueller et al.
5,146,592	A		9/1992	Pfeiffer et al.
5,148,385	A		9/1992	Frazier
5,157,772	A		10/1992	Watanabe
5,179,689	A		1/1993	Leach et al.
5,179,734	A		1/1993	Candy et al.
5,187,799	A		2/1993	McAuley et al.
5,226,147	A		7/1993	Fujishima et al.
5,237,699	A		8/1993	Little et al.
5,239,631	A		8/1993	Boury et al.
5,241,636	A		8/1993	Kohn
5,261,057	A		11/1993	Coyle et al.
5,261,082	A		11/1993	Ito et al.
5,261,109	A		11/1993	Cadambi et al.
5,325,513	A		6/1994	Tanaka et al.
5,339,448	A		8/1994	Tanaka et al.
5,353,417	A		10/1994	Fuoco et al.
5,353,427	A		10/1994	Fujishima et al.
5,379,438	A		1/1995	Bell et al.
5,410,654	A		4/1995	Foster et al.
5,410,682	A		4/1995	Sites et al.
5,414,862	A		5/1995	Suzuki et al.
5,421,000	A		5/1995	Fortino et al.
5,440,749	A		8/1995	Moore et al.
5,459,846	A		10/1995	Hyatt
5,511,209	A		4/1996	Mensch, Jr.
5,530,890	A		6/1996	Moore et al.
5,537,565	A		7/1996	Hyatt
5,604,915	A		2/1997	Moore et al.
5,659,703	A		8/1997	Moore et al.
5,809,336	A		9/1998	Moore et al.
5,874,584	A		2/1999	Wear et al.
6,598,148	B1		7/2003	Moore et al.

FOREIGN PATENT DOCUMENTS

EP	208287	A2	1/1987
EP	0 238 810		9/1987
EP	288649	A1	11/1988
EP	0 786 730		6/2000
GB	8233733		11/1982
JP	57-20979		2/1982
JP	57-196334		12/1982
JP	58025710	A	2/1983
JP	58-103043		6/1983
JP	61127228	A	6/1986
JP	61138356	A	6/1986
JP	62145413	A	6/1987
JP	63-026753		2/1988
JP	5189383	A	7/1993
WO	WO 81/00473		2/1981
WO	8803091	A1	5/1988
WO	WO 91/02311		2/1991

OTHER PUBLICATIONS

"IBM RT Personal Computer Technology," IBM Corp. 1986. (collection of papers by developers).

Acorn Computers, Ltd., Acorn RISC Machine CPU Software Manual, Issue 1.00 Oct. 1985.

Acorn's RISC leapfrog, Acorn User special issue, Jun. 1987; 59: 149–153.

Agrawal et al., "Design Considerations for a Bipolar Implementation of SPARC," Compcon Spring apos;88. Thirty–Third IEEE Computer Society International Conference, Digest of Papers, Feb. 29–Mar. 3, 1988, pp. 6–9.

Agrawal, "An 80 MHz Bipolar ECL Implementation of SPARC," Sun Microsystems, Inc., Jun. 25, 1989, 40 pages total.

Alliacense Product Report—Preliminary Review, USP 5,440,749; GPS Car Navigation Main Processor.

Alliacense Product Report—Preliminary Review, USP 5,440,749; GPS Navigation System GPS Chipset.

Alliacense Product Report—Preliminary Review, USP 5,440,749; GPS Navigation System Main Microprocessor.

Alliacense Product Report—Preliminary Review, USP 5,440,749; Kyocera Digital Camera Finecam S3R Image Processor.

Alliacense Product Report—Preliminary Review, USP 5,440,749; PDA/Mobile Navigation, GPS Processor.

Alliacense U.S. Patent No. 5,784,584 Product Report, NEC Microcomputer, V850E2 32 Bit Microcontroller, pp. 1–8 (2006).

Alliacense U.S. Patent No. 5,784,584 Product Report, TLCS–900/H1 Series TMP92C820, Toshiba Microcontroller TMP92C820 / TCLS–900/H1 Series 16–bit Microcontroller, pp. 1–9 (2006).

Alliacense U.S. Patent No. 5,809,336 Product Report, Toshiba Microcontroller TMP93CS44/S45 / TLCS–900/L Series 16–bit Microcontroller (2006).

Alliacense U.S. Patent No. 5,809,336 Product Report, NEC Microcontroller UDP789478, 8 Bit Microcontroller, 38 pages (2006).

Alliacense U.S. Patent No. 5,809,336 Product Report, Toshiba Microcontroller TMP92CZ26 / TMP92CW26, 32 bit Microcontroller (2006).

Alliacense U.S. Patent No. 5,809,336 Product Report, Toshiba MPEG–4 Audiovisual LSI TC35273 MPEG–4 Audiovisual Code LSI (2006).

Anderson, D.W., The IBM System/360 Model 91: Machine Philosophy and Instruction Handling, IBM Journal, IBM, Jan. 1967, pp. 8–24.

ARM Datasheet, Part No. 1 85250 0360 0, Issue No. 1 (Mar. 17, 1987).

ATMEL SPARC Instruction Set, "Assembly Language Syntax," Rev. 4168C–AERO–08/01, 2002.

Bagula, "A 5V Self–Adaptive Microcomputer with 16Kb of #2 Program Storage and Security," IEEE International Solid–State Circuit Conference, 1983, pp. 34–35.

Bayko, Great Microprocessors of the Past and Present (V 11.7.0), downloaded from: <<http://web.archive.org/web/20010107210400/http://bwrc.eecs.berkeley.edu/CIC/Archive/cup_history.html>>, Feb. 2007, 60 pages total.

Bit SPARC Integer Unit B5000 Datasheet attached to a presentation by Anant Agrawal in 1989, 28 pages.

Books Review: Operating Systems A Systematic View, William S. Davis, Addison–Wesley Publishing Company, Inc., 1987; 26(4):453–454.

Bosshart et al., "A 533K–Transistor LISP Processor Chip," IEEE Journal of Solid State Circuits, SC–22(5): 808–819 (Oct. 1987).

Bourke, "Character Synchronization During Overrun Conditions," Delphion, IBM Technical Disclosure Bulletin, Dec. 1977.

Cal Run Fortran Guide, University of California, Computer Center, Berkeley, 292 pages total. (Sep. 1974).

CDC 6000 Computer Systems—COBOL Instant 6000, Version 3; Control Data Publication No. 60327600A (Apr. 1971).

CDC 6000 Computer Systems, 7600 Computer Systems: Fortran Extended Instant 6000 Version 3, 7600 Version 1; Control Publication No. 60305900A (May 1971).

CDC 6000 Computer Systems/ 7600 Computer Systems: Fortran Extended Reference Manual, 6000 Version 3, 7600 Version 1; Control Data Publication No. 60329100, Revision D (1972).

CDC 6000 Series Computer System, 6642 Distributive Data Path Operation and Programming Reference Manual; Control Data Publication No. 60376300C (Mar. 1979).

CDC 6000 Series Computer Systems—Chippewa Operating System Documentation, vol. I, Preliminary Edition (updated May 1966).

CDC 6000 Series Computer Systems—Chippewa Operating System Documentation, vol. II, Preliminary Edition, Peripheral Packages and Overlays (Oct. 1965).

CDC 6000 Series Computer Systems—Chippewa Operating System Documentation, vol. III, Preliminary Edition, DSD—The Systems Display, (Nov. 1965).

CDC 6000 Series Computer Systems Ascent General Information Manual; Control Data Publication No. 60135400 (Feb. 1966).

CDC 6000 Series Computer Systems Chippewa Operating System Reference Manual; Control Data Publication No. 60134400 (Dec. 1965).

CDC 6000 Series Computer Systems Hardware Reference Manual; Control Data Publication No. 60100000 (Aug. 1978).

CDC 6000 Series Computer Systems/ 7600 Computer System: 6000 Compass Version 2, 7600 Versions 1 &2 Reference Manual; Control Data Publication No. 60279900, Revision D. (1970, 1971, 1972).

CDC 6000 Series Computer Systems: Chippewa Operating System Fortran Reference Manual; Control Data Publication No. 60132700A (May 1966).

CDC 6000 Series Computer Systems: Peripheral Equipment Reference Manual; Control Data Publication No. 60156100, Revision J (Mar. 1970).

CDC 6000 Series Computer Systems: Site Preparation and Installation Manual; Control Data Publication No. 60142400, Revision B (Sep. 1965).

CDC 6000 Series Computer Systems: FORTRAN Extended General Information, Control Data Publication No. 60176400 (Oct. 1966).

CDC 6000 Series FORTRAN Extended 4.0, Internal Maintenance Specifications, (1971).

CDC 6000 Series Introduction and Peripheral Processors Training Manual, Second Edition; Control Data Publication No. 60250400 (Nov. 1968).

CDC 6400 Central Processor; Control Data Publication No. 60257200 (Feb. 1967).

CDC 6400/6500/6600 Ascent–To–Compass Translator; Control Data Publication No. 60191000 (Mar. 1967).

CDC 6400/6500/6600 Computer System Input/Output Specification; Control Data Publication No. 60045100 (Sep. 1967).

CDC 6400/6500/6600 Computer System Instant SMM; Control Data Publication No. 60299500 (Nov. 1969).

CDC 6400/6500/6600 Computer Systems Compass Reference Manual; Data 60190900, Revision B (Mar. 1969).

CDC 6400/6500/6600 Computer Systems Reference Manual; Control Data Publication No. 60100000, Revision K (Aug. 1970).

CDC 6400/6500/6600 Computer Systems Reference Manual; Control Data Publication No. 60100000D (1965, 1966, 1967).
CDC 6400/6500/6600 Extended Core Storage Systems Reference Manual; Control Data Publication No. 60225100, (Feb. 1968).
CDC 6400/6500/6600 Jovial General Information Manual; Control Data Publication No. 60252100A (Mar. 1969).
CDC 6400/6600 Computer Systems: Ascent/Asper Reference Manual; Control Data Publication No. 60172700 (Jul. 1966).
CDC 6400/6600 Fortan Conversion Guide; Data Publication No. 60175500 (Aug. 1966).
CDC 6400/6600 Systems Bulletin (Oct. 10, 1966), 84 pages.
CDC 6400/6600, Export/Import 8231 Reference Manual; Data Publication No. 60189100 (Apr. 1967).
CDC 6600 Central Processor vol. 1; Control &Memory; Data Control Publication No. 020167 (Mar. 1967).
CDC 6600 Central Processor, vol. 2; Functional Units; Control Data Publication No. 60239700 (Mar. 1967).
CDC 6600 Chassis Tabs; Control Data Publication No. 63016700A (Apr. 1965).
CDC 6600 Chassis Tabs; Control Data Publication No. 63019800 (Mar. 1965).
CDC 6600 Chippewa Operating System; Control Data Publication No. 60124500, Revision C (Apr. 1965).
CDC 6600 Computer System 6601 A–J, 6613A/B/C, 6604A/B/C, 6614–A/B/C Central Processor (Including Functional Units) vol. 1, Diagrams & Circuit Description; Control Data Publication No. 60119300BT(Jan. 1968).
CDC 6600 Computer System 6601 A–J, 6613A/B/C, 6604A/B/C, 6614–A/B/C Peripheral and Control MW Processor/Central Memory/Clock/Extended Core Storage Coupler (Std Opt 10102 and/or Spec Opt 60080)/ Power Wiring, vol. 2, Diagrams & Circuit Descriptions; Control Data Publication No. 60119300BT (Jan. 1968).
CDC 6600 Computer System Operating System/Reference Manual, SIPROS66, 1st ed.; Control Data Publication No. 60101800A (1965).
CDC 6600 Computer System Programming System/Reference Manual, vol. 1. Ascent; Control Data Publication No. 60101600B (1965).
CDC 6600 Computer System Programming System/Reference Manual, vol. 2. Asper; Control Data Publication No. 60101700B (1965).
CDC 6600 Computer System Programming vol. 3, Fortran 66; Control Data Publication No. 60101500B (1965).
CDC 6600 Computer Training Manual vol. 2, Preliminary Edition, Section 7.2 Shift Functional Units, 164 pages.
CDC 6600 Data Channel Equipment 6602–B/6612–A, 6603–B, 6622–A, 6681–B, 6682–A/6683–A, S. O. 60022, 60028,60029, Diagrams & Circuit Description' Control Data Publication No. 60125000, Revision G (Jun. 1966).
CDC 6600 Training Manual; Control Data Publication No. 60147400, Revision A (Jun. 1965).
CDC 6603—A/B/C Disk File Controller Reference Manual; Control Data Publication No. 60334000 (1970).
CDC 6638 Disk File Subsystem Training Supplement; Control Data Publication No. 602500800A (Oct. 1968).
CDC 6638 Disk File System: Standard Option 10037–A, 6639–A/B File Controller—Diagrams and Circuit Description/Maintenance/Maintenance Aids/Parts List/Wire Lists/ Chassis Tabs; Control Data Publication No. 60227300, Revision H (Mar. 1974).
CDC 6639—A/B Disk File Controller Reference Manual; Control Data Publication No. 60334100E (Aug. 1973).
CDC 6639 Disk Controller Training Manual Test Edition (Sep. 1967), 28 pages.
CDC APL Version 2 Reference Manual, CDC Operating Systems: NOS; Control Data Publication No. 60454000F (Nov. 1980).
CDC Basic Version 3 Reference Manual: NOS 1 &NOS/BE 1; Control Data Publication No. 19983900G (Oct. 1980).
CDC Chippewa Operating System, Document Class ERS, System No. E012, Version 1.1; External Reference Specifications—Chippewa Operating System, (Jun. 1966).
CDC Chippewa Operating System, Document Class SIR, System No. E012, Version 1.0, (Mar. 3, 1966).
CDC Chippewa Operating System, Document Class SIR, System No. E012, Version 1.1, (Mar. 3, 1966).
CDC Cobol Version 4 Instant Manual, Cyber 170 Series, Cyber 70 Models 72, 73, 74, 6000 Series; Control Data Publication No. 60497000A (Feb. 1976).
CDC Cobol Version 5 Instant Manual,Operating Systems: NOS 1/BE 1; Control Data Publication No. 60497300B (Feb. 1981).
CDC Codes/Control Data 6400/6500/6600 Computer Systems; Control Data Publication No. 60141900, Revision C (Jun. 15, 1967).
CDC Codes/Control Data 6400/6500/6600/6700 Computer Systems; Control Data Publication No. 60141900, Revision D (Jun. 10, 1970).
CDC Codes/Control Data 6600; Control Data Publication No. 60141900, Revision A (May 1965).
CDC Compass Version3 Instant, Operating Systems: NOS 1, NOS 2, NOS/ BE 1, Scope 2; Control Data Publication No. 60492800D (Jun. 1982).
CDC Course No. FH4010–1C, NOS Analysis, Student Handout, Revision C (Apr. 1980).
CDC Course No. FH4010–4C NOS Analysis, Study Dump (Apr. 1980).
CDC Cyber 170 Models 720, 730, 740, 750 and 760 Model 176 (Level B/C) Computer Systems, Codes; Control Data Publication No. 60456920C, (Jun. 1981).
CDC Cyber 70 Computer Systems Models 72,73,74,6000 Computer Systems: Fortran Reference Manual Models 72,73,74 Version 2.3; 6000 Version 2.3; Control Data Publication No. 19980400, Revision F (Jul. 1972).
CDC Cyber 70 Computer Systems Models 72,73,74,76,7600 Computer System, 6000 Computer Systems—ALGOL Reference Manual, Cyber 70 Series Version 4, 6000 Series Version 4, 7600 Series Version 4; Control Data Publication No. 60384700A (Aug. 1973).
CDC Cyber 70 Computer Systems Models 72,73,74,76,7600 Computer System, 6000 Computer Systems: Cobol Instant Models 72, 73, 74 Version 4, Model 76 Version 1,6000 Version 4; Control Data Publication No. 60328400A (Dec. 1971).
CDC Cyber 70 Computer Systems Models 72,73,74,76,7600 Computer System, 6000 Computer OA Systems: Fortran Extended Instant Models 72, 73, 74 Version 4, Model 76 Version 2,7600 Version 2; Control Data Publication No. 60357900A (Nov. 1971).
CDC Cyber 70 Computer Systems Models 72,73,74,76,7600 Computer System, 6000 Computer Systems: Fortran Extended Reference Manual Models 72, 73, 74 Version 4, Model 76 Version 2,6000 Version 4; Control Data Publication No. 60305600A (Oct. 1971).

CDC Cyber 70 Series 6000 Series Computer Systems: APL *Cyber Reference Manual; Control Data Publication No. 19980400B (Jul. 1973).

CDC Cyber 70 Series Computer Systems Models 72,73,74, 6000 Series Computer Systems—Kornos 2.1 Workshop Reference Manual; Control Data Publication No. 974047000 (1976).

CDC Cyber 70 Series Models 72/73/74,6000 Series Computer Systems, Krono 2.1 Operator Guide; Control Data Publication Guide Control Data Publication No. 60407700A (Jun. 1973).

CDC Cyber 70 Series Models 72/73/74,6000 Series Computer Systems, Kronos 2.1 Installation Handbook; Control Data Publication No. 60407500A (Jun. 1973).

CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, Kronos 2.1 Time–Sharing User's Reference Manual; Control Data Publication No. 60407600B (May 1974).

CDC Cyber 701 Model 76 Computer System, 7600 Computer System: Fortran Run, Version 2 Reference Manual; Control Data Publication No. 60360700C (May 1974).

CDC Cyber Interactive Debug Version 1 Guide for Users of Fortran Extended Version 4, CDC Operating Systems: NOS 1, NOS/BE 1, Control Data Publication No. 60482700A (Feb. 1979).

CDC Cyber Interactive Debug Version 1 Guide for Users of Fortran Version 5, Operating Systems: NOS 1, NOS / BE 1, Control Data Publication No. 60484100C (Sep. 1984).

CDC Cyber Interactive Debug Version 1 Reference Manual, NOS 1, NOS 2, NOS/ BE 1, Data Control Publication No. 60481400D (Jun. 1984).

CDC Cyber Loader Version 1 Instant, CDC Operating System NOS1, NOS/BE 1, Control Data Publication No. 60449800C (Aug. 1979).

CDC Disk Storage Subsystem—Operation and Programming Manual; Control Data Publication No. 60363900, Version T (1972–1980).

CDC Fortran Extended 2.0, Document Class ERS, System No. C012, (Dec. 1966).

CDC Fortran Extended 2.0, Document Class IMS, Internal Maintenance Specifications—64/65/6600 V Fortran Extended Version 2 (Mar. 1969).

CDC Fortran Extended Version 4 Instant Manual, Operating Systems: NOS 1, NOS/BE 1, Scope 2; Control Data Publication No. 60497900B (Jun. 1981).

CDC Fortran Extended, Sales Technical Memorandum (May 1967).

CDC Fortran Extended Version 5 Instant, CDC Operating Systems: NOS 1, NOS/BE 1, Scope 2; Control Data Publication No. 60483900A (Jan. 1981).

CDC GED Fortran Extended 1.0, Product No. C012, Dept. No. 254, Project No. 4P63FTN (Aug. 1967).

CDC Instant 6400/3500/6500 Simula; Control Data Publication No. 60235100, Revision A (Feb. 1969).

CDC Instant 6400/6500/6600 Compass; Control Data Publication No. 60191900, Revision A (1968).

CDC Instant Fortran 2.3 (6000 Series); Data Publication No. 60189500D (May 1969).

CDC Internal Maintenance Specification: Fortran V5, Part 1; Control Data Publication No. 77987506A.

CDC Internal Maintenance Specification: Fortran V5, Part 2; Control Data Publication No. 77987506A.

CDC Kronos 2.1 Reference Manual vol. 1 of 2; Control Data Cyber 70 Series Models 72/76/74, 6000 Series Computer Systems; Control Data Publication No. 60407000D (Jun. 1975).

CDC Model dd 60A Computer Control Console/Customer Engineering Manual; Control Data Publication No. 82100010 (Mar. 1965).

CDC Model dd60b Computer Control Console/Customer Engineering Manual; Control Data Publication No. 82103500 (Feb. 1967).

CDC Network Products: Network Access Method Version 1, Network Definition Language Reference Manual; Control Data Publication No. 60480000J (May 1981).

CDC Network Products: Network Terminal User's Instant—Operating System NOS 1; Control Data Publication No. 60455270C (Oct. 1980).

CDC NOS 2 Operations Handbook; Control Data Publication No. 60459310, (Aug. 1994).

CDC NOS Version 1 Applications Programmer's Instant, CDC Computer Systems: Cyber 170 Series, Cyber 70 Models 71,72,73,74,6000 Series; Control Data Publication No. 60436000H (Jan. 1980).

CDC NOS Version 1 Internal Maintenance Specification vol. 1 of 3; Control Data Publication No. 60454300B (Aug. 1979).

CDC NOS Version 1 Internal Maintenance Specification vol. 2 of 3; Control Data Publication No. 60454300B (Aug. 1979).

CDC NOS Version 1 Internal Mainenance Specification vol. 3 of 3; Control Data Publication No. 60454300B (Aug. 1979).

CDC NOS Version 1 Operator's Guide, CDC Computer Systems: Cyber 170 Series, Cyber 70 Model 71, 72,73,74,6000 Series (Dec. 1980).

CDC NOS Version 1 Reference Manual vol. 1 of 2, CDC Computer Systems: Cyber 170 Series, Cyber 70 Models 71,72,73,74,6000 Series; Control Data Publication No. 60435400J (1979).

CDC NOS Version 1 Reference Manual vol. 2 of 2, CDC Computer Systems: Cyber 170 Series, Cyber 70 Models 71, 72, 73, 74,6000 Series; Control Data Publication No. 60445300E (1977).

CDC NOS Version 1 System Maintenance Reference Manual; Control Data Publication No. 60455380H (Apr. 1981).

CDC NOS Version 2 Analysis Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60459300D (Oct. 1984).

CDC NOS Version 2 Analysis Handbook, Control Data Publication No. 60459300U (Jul. 1994).

CDC NOS Version 2 Installation Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60459320E_(Mar. 1985).

CDC NOS Version 2 Operation/Analysis Handbook, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000, Control Data Publication No. 60459310C (Oct. 1983).

CDC NOS Version 2 System Maintenance Reference Manual, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60459300C (Oct. 1983).

CDC NOS/BE Version 1 Diagnostic Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71,72,73,74, 6000; Control Data Publication No. 60494400–V (1986).

CDC NOS/BE Version 1 Installation Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71,72,73,74, 6000; Control Data Publication No. 60494300aB (Dec. 1986).
CDC NOS/BE Version 1 Reference Manual, Cyber 170 Series, Cyber 70 Models 71, 72, 73, 74, 6000 Series; Control Data Publication No. 60493800M (1981).
CDC Outline of Reports on Feasibility Study of 64/6600 Fortran Ver 3.0 and Conversational Fortran, Fortran Study Project, Product No. X010, Dept No. 254, Project No. 4P63, (Jun. 1966).
CDC Pascal Version 1 Reference Manual, Operating Systems: NOS 2; Control Data Publication No. 60497700 (Sep. 1983).
CDC Pascal Version 1 Reference Manual, Operating Systems: NOS 2; Control Data Publication No. 60497700A (Dec. 1982).
CDC PL/1 Version 1 Instant, CDC Operating Systems: NOS 1, NOS/ BE 1; Control Data Publication No. 60483700A (Nov. 1979).
CDC Simscript 11.5 Instant; Control Data Publication No. 84000450B (Sep. 1978).
CDC Sort/Merge Version 4 and 1 Instant, Operating Systems: NOS 1, NOS/BE 1, Scope 2; Control Data Publication No. 60497600C (Jan. 1981).
CDC Sort/Merge Version 5 Reference Manual, Operating Systems: NOS 2, NOS/BE 1, Control Data Publication No. 60484800C (Feb. 1984).
CDC SYMPL Version 1 Instant, NOS 1, NOS/BE 1, Scope 2; Control Data Publication No. 60482600A (May 1978).
CDC SYMPL Version 1 Users Guide, Operating Systems: NOS 1, NOS/BE 1, Scope 2; Control Data Publication No. 60499800B (Apr. 1978).
CDC Update Instant, Cyber 170 Series, Cyber 70 Series, 6000 Series, 7600 Computer Systems; Control Data Publication No. 60450000A (Nov. 1975).
CDC Update Reference Manual Operating Systems: Scope 3.4, Kronos 2.1; Control Data Publication No. 60342500, Revision H (1971–1976).
CDC Xedit Version 3 Reference Manual, Operating System: NOS 1; Control Data Publication No. 60455730B (Aug. 1979).
Chippewa Laboratories Fortran Compiler Run, Preliminary Edition, CDC 6000 Series Computer Systems, (Apr. 1966).
Cho et al., WAM 3.6: A 40K Cache Memory and Memory Management Unit, ISSCC '86, Feb. 19, 1986.
Cho et al., "The Memory Architecture and the Cache and Memory Management Unit for the Fairchild Clipper Processor," Report No. UCB/CSD 86/289, Computer Science Division (EECS), University of California (Apr. 1986).
CLIPPERTM 32–Bit Microprocessor, Introduction to the Clipper Architecture, published by Fairchild in 1986.
Cordell, II et al., "Advanced Interactive Executive Program Development Environment," IBM Systems Journal, 1987; 26(4):361–382.
Crawford, "The i486 Executing Instructions in One Clock Cycle," IEEE Micro, pp. 28–36 (Feb. 1990).
Cray–1 Computer System Hardware Reference Manual, Publication No. 2240004, Rev C, Nov. 4, 1977.
Disk Routines and Overlays, Chippewa Operating System, CDC Development Division—Applications, (Nov. 1965).
Ditzel et al., "The Hardware Architecture of the Crisp Microprocessor," AT &T Information Systems, ACM, pp. 309–319 and table of contents (1987).
DS5000 Soft Microcontroller User's Guide Preliminary V 1.0, Dallas Semiconductor.
Duell. C. H., "Everything that can be invented has been invented," 2 pages downloaded from http://www.tplgroup.net/patents/index.php.
Evans et al., "An Experimental 512–bit Nonvolatile Memory with Ferroelectric Storage Cell," IEEE Journal of Solid–Sate Circuits, 23(5):1171–1175.
Excerpt from A Seymour Cray Perspective http//research.microsoft.com/users/gbell/craytalk/sld029.htm (Slide 29).
Excerpts from A Seymour Cray Perspective http//research.Microsoft.com/users/gbell/craytalk/sld001.htm (Slide 1).
Fiasconaro, J., "Microarchitecture of the HP9000 Series 500 CPU," Microarchitecture of VLSI Computers, NATO ASI Series No. 96, Antognetti, eds., pp. 55–81.
Field Maintenance Print Set, KA780–01–01 Rev. A.
Fisher et al., "Very Long Instruction Word Architectures and the ELI–512," ACM pp. 140–150 (1983).
Fukui et al., "High Speed CMOS 4–bit Microcomputer SM550 Series," pp. 107–109 published 1982, 1983. (Document in Japanese).
Furber, VSLI RISC Architecture and Organization, Chapter 3: Commercial VLSI RISC, pp. 124–129, Marcel Dekker, Inc., 1989.
GE 600 Series, publication.
GE–625 / 635 Programming Reference Manual, revised Jan. 1996.
Gershon, Preface, IBM Systems Journal 26(4):324–325.
Green et al., "A Perspective on Advanced Peer–to–Peer Networking," IBM Systems Journal, 1987; 26(4):414–428.
Grimes et al., "64 bit Processor, The Intel i860 64–Bit Processor: A General–Purpose CPU with 3D Graphics Capabilities", published by Intel, p. 85 (Jul. 1989).
Grishman, R., "Assembly Language Programming for the Control Data 6000 and Cyber Series Algorithmics".
Grondalski et al., "Microprocessors–Special Purpose—THPM 16.3: A VLSI Chip Set for a Massively Parallel Architecture," 1987 IEEE International Solid–State Circuits Conference, Feb. 26, 1987, pp. 1998–198.
Gross et al., "Measurement and evaluation of MIPS architecture and processor," ACM Trans. Computer Systems, pp. 229–257 Aug. 1988.
Guttag, "The TMS34010: An Embedded Microprocessor", IEEE Micro, vol. 8, No. 3, May 1988, pp. 39–52.
Hansen, "A RISC Microprocessor with Integral MMU and Cache Interface," ICCD '86, pp. 145–148, 1986.
Hennessy et al., "Hardware/software tradeoff for increased performance," Proceedings of the Symposium on Architectural Support for Programming Languages and Operating Systems pp. 2–11. ACM, Apr. 1982.
Hennessy et al., "Hardware/software tradeoff for increased performance," Technical Report No. 22.8, Computer Systems Laboratory, Feb. 1983, 24 pages.
Hennessy et al., "MIPS: A Microprocessor Architecture," IEEE, pp. 17–22 (1982).
Hennessy et al., "MIPS: A VLSI Processor Architecture" VLSI Systems and Computer, Kung eds., Carnegi–Mellon University, pp. 337–346 (1981).
Hennessy et al., "The MIPS Machine", Compcon, IEEE, Spring 1982, pp. 2–7.
Hennessy, "Performance Issues in VLSI Processor Design," IEEE on VLSI in Computers, , pp. 153–156. (1983).
Hinton, 80960—Next Generation, Compcon Spring 89, IEEE, 13–16 (1989).

Hitachi America Ltd., "8–Bit Single–Chip Microprocessor Data Book", Jul. 1985, Table of Contents and pp. 251–279.
Hollingsworth et al., "The Fairchild Clipper: Instruction Set Architecture and Processor Implementation," Report No. UCB/CSD 87/329, Computer Science Division (EECS), University of California Berkeley, California, (Feb. 11, 1987).
Horowitz et al., "A 20—MIPS Peak, 32–bit Microprocessor with On–Chip Cache," IEEE Journal of Solid State Circuits, SC–22(5):790–799 (Oct. 1987).
HP 9000 Instrument Controllers, Technical Specifications Guide, Oct. 1989.
HP 9000 Series Computer Systems, HP–UX Reference 09000–090004, Preliminary Nov. 1982.
HP Sacajawea External Reference Specification Preliminary Version 1.1 (Jan. 14, 1987).
Hughes, "Off–Chip Module Clock Controller," Delphion, IBM Technical Disclosure Bulletin, Sep. 1989.
Hunter, "Introduction to the Clipper Architecture," IEEE Micro, pp. 6–26 (Aug. 1987).
IBM RT PC, Byte 1986 Extra Edition, Inside The IBM PCs, pp. 60–78.
IBM Systems Reference Library, IBM System/360 Model 67 Functional Characteristics, File No. S360–01, Form A27–2719–0, published by IBM (1967).
IEEE Std 796–1983, Microcomputer System Bus, pp. 9–46.
Index of/pdf/cdc/6x00, downloaded from http://www.bitsavers.org/pdf/cdc/6x00/.
INMOS Engineering Data, IMS T414M Transputer, Extended Temperature, (Aug. 1987).
INMOS IMS T212 Engineering Data Preliminary Data Sheet (Aug. 1987).
INMOS IMS T414 Data Sheet, (Jun. 1987).
INMOS IMS T414 Transputer, Engineering Data, pp. 107–163.
INMOS IMS T414 Transputer, Preliminary Data (Feb. 1987).
INMOS M212 Disk Processor Product Overview Oct. 1987, 12 pages total.
Intel 386TM DX Microprocessor 32–Bit CHMOS Microprocessor With Integrated Memory Management (1995).
Intel 4004 Data Sheet Single Chip 4–Bit 9–Channel Microprocessor, pp. 8–15 to 8–23.
Intel 8008 8–Bit Parallel Central Processor Unit, published by Intel (Nov. 1972), Users Manual.
Intel 80960CA User's Manual published by Intel (1989).
Intel Architecture Optimization Manual, Order No. 242816–003, published by Intel (1997).
Intel Architecture Software Developer's Manual, vol. 1: Basic Architecture, published by Intel (1997).
Intel i860 64–Bit Microprocessor, Intel Corporation Feb. 1989.
Intel MCS–4 Micro Computer Set, Integrated Circuit Engineering Collection (Nov. 1971).
Intel, iAPX 386 High Performance 32–Bit Microprocessor Product Review (Apr. 1984).
Intel 8080A/8080A–1/8080A–2, 8–Bit N–Channel Microprocessor, Order No. 231453–001, Its Respective Manufacturer (Nov. 1986).
Jguppi et al., "A 20 MIPS Sustained 32b CMOS with 64b Data Bus," IEEE Int'l Solid State Circuits Conf., pp. 84–86 (1989).
Johnson et al., "A Variable Delay Line PLL for CPU–Coprocessor Synchronization," IEEE Journal of Solid–State Circuits, 23(5): 1218–1223, Oct. 1988.
Katevenis et al., "Reduced Instruction Set Computer Architecture for VLSI," Doctoral Dessertation, Oct. 1983.
Katevenis et al., "The RISC II Micro–Architecture," Journal of VLSI and Computer Systems, 1(2): 138–152 (1984).
Kipp, "Micron Technology Inc. Reports Financial Results," Business Wire, New York, Sep. 26, 1988.
Kohn et al., "Introducing Intel i860 64–Bit Microprocessor," Intel Corporation, IEEE Micro (Aug. 1989).
Koopman, "RTX 4000," Proceedings of 1989 Rochester Forth Conference, pp. 84–86.
Koopman, "The WISC Concept: A proposal for a writable instruction set computer," Byte, pp. 187–193. (Apr. 1987).
Koopman, Jr. et al. "MVP Microcoded CPU/16 Architecture," Proceedings of 1986 Rochester Forth Conference, pp. 277–280.
Koopman, Jr. et al., "WISC Technologies, Inc., Writable Instruction Set, Stack Oriented Computers: The WISC Concept," 1987 Rochester Forth Conference, Journal of Forth Application and Research, 5(1):49–71.
"Stack Computers: the new wave, Chapter 5.2: Architecture of the FRISC 3 (SC32)", Philip Koopman, 1989, 9 pages.
Loucks et al., "Advanced Interactive Executive (AIX) Operating System Overview," IBM Systems Journal, 1987; 26(4):326–345.
LSI Logic Corporation MIPS Architecture RISC Technology Backgrounder, "Introduction to RISC Technology," LSI Logic Corporation (Apr. 1988).
Matick, "Self–Clocked Cache," Delphion, IBM Technical Disclosure Bulletin, Apr. 1985.
Matsushita Electric, 8 bit Dual1–chip Microcomputer MN1890 Series User's Manual, translation of original Japanese language document, by Matsushita Electric Industrial Co., Ltd. Semiconductor Sales Division.
Matsushita Electronics Corporation, MN1880 (MN18882) Instruction Manual, (document in Japanese), 1988.
Matsushita Electronics Corporation, MN188166 User's Manual, Japanese language document.
Matsushita Electronics Corporation, MN18882 LSI User's Manual, Japanese language document, 1987.
Matsushita Electronics Corporation, Specification Sheet, MN18882 (Book1) translation of the Japanese language original, Code No. MIG0175, Matsushita Electronics Industry Corporation, Microcomputer Products Division, Oct. 22, 1990.
Matthys R. J., Crystal Oscillator Circuits, John Wiley &Sons, pp. 25–64 (1983).
May, "The Transputer and Occam," International Conference on the Impact of Digital Microelectronics and Microprocessors on Particle Physics, held Mar. 28–30, 1988, published by World Scientific in 1988, Budnich, eds. pp. 205–211.
May, D., "The Influence of VLSI Technology on Computer Architecture," INMOS Ltd., pp. 247–256 (1988).
Mead et al., eds., Introduction to VLSI Systems, Addison Wesley Publishers, (1980), 144 pages.
Miller, Frequency Modulated Ring Oscillator for a Mode Regulated Substrate Bias Generator, Delphion, IBM Technical Disclosure Bulletin, Sep. 1989.
Mills et al., "Box Structured Information Systems," IBM Systems Journal, 1987; 26(4):395–413.

Minyard, Using a TMS320C30 Serial Port as an Asynchronous RS–232 Port, Application Brief: SPRA240, Texas Instruments (May 1994).
MMP Portfolio, News Release: Roland Becomes 50th Licensee, Setting a Major Milestone in Moore Microprocessor Patent Licensing Program, 3 pages (May 1, 2009).
Moelands, A. P. M., "Serial I/O with the MAB8400 series microcomputers," Electronic Components and Applications, 3(1):38–46 (1980).
Moore, P., "INMOS Technical Note 15: IMS B005 Design of a Disk Controller board with drives," Dec. 3, 1986.
Mostek Corp., Adverisement, EDN, Nov. 20, 1976.
Motorola Inc., MC 68332 32–Bit Microcontroller System Integration User's Manual Preliminary Edition, Revision 0.8, (1989).
Motorola MC146805H2, Advance Information, pp. 1–12.
Motorola MC68HC11A8 HCMOS Single–Chip Microcomputer, table of contents and introduction (1985).
Motorola Semiconductors MC146805H2, Product Brochure.
Motorola, "How to Take Control" product brochure by Motorola (1988).
Motorola, MC68300 Family MC68332 User's Manual, (1995).
Moussouris et al., "A CMOS RISC Processor Integrated System Functions," Proceedings of 31st IEEE Computer Society International Conference, Cathedral Hill Hotel, San Francisco, CA Mar. 3–6, 1986, pp. 126–131, 1986.
National Semiconductor HPC16400/HPC36400/HPC46400 High–Performance MicroControllers with HDLC Controller product literature.
NEC Data Sheet MOS Integrated Circuit uPD75008, 4 bit Single–Chip Microcomputer (1989).
NEC Electronics Inc. High–End, 8–Bit, Single–Chip CMOS Microcomputers product literature.
NEC Electronics Inc. Microcomputer Products Microprocessors, Peripherals, & DSP Products Data Book vol. 2 of 2 cover page.
NEC Electronics Inc. Microcomputer Products Single–Chip Products Data Book vol. 1 of 2 cover page.
NEC Electronics Inc. MOS Integrated Circuit uPD70208H, 70216H Data Sheet, V40HL, V50HL 16/8, 16–Bit Microprocessor (1995).
NEC Electronics Inc. MOS Integrated Circuit uPD7225 Programmable LCD Controller/Driver (1986, 1999).
NEC Electronics Inc. uPD78C10/C11/C14 8–Bit, Single–Chip CMOS Microcomputers with A/D Converter product literature.
Olson, Semiconductor Die with Wiring Skirt (Packaging Structure), Delphion, IBM Technical Disclosure Bulletin, Jul. 1978.
O'Neil, "Pipeline Memory System for Drams", Delphion, IBM Technical Disclosure Bulletin, May 1989.
Paker, Y, Multi–Processor Systems, Academic Press, pp. 1–23 (1983).
Patterson et al., "Architecture of a VLSI Instruction Cache for a RISC," ACM, pp. 108–116 (1983).
Patterson et al., "RISC I: A Reduced Instruction Set VLSI Computer," Proceedings of the 8th annual symposium on Computer Architecture on Computer Architecture, Minneapolis, Minnesota, pp. 443–457 (May 1981).
Patterson, "RISC Watch", ACM, vol. 12 (1):11–19 (Mar. 1984).
Patterson, D. A., "Reduced Instruction Set Computers" Communication of the ACM, 28(1):.8–21, Jan. 1985.
Pountain, "The Archimedes A310," Byte, 1987.
Przybyiski et al., "Organizational and VLSI Implementation of MIPS," Technical Report: CSL–TR–84–259, Apr. 1984.
Przybyiski, "The Design Verification and Testing of MIPS", 1984 Conference on Advanced Research in VLSI, pp. 100–109.
Rau et al., "The Cydra 5 Departmental Supercomputer, Design Philosophies, Decisions, and Tradeoffs," IEEE, pp. 12–36 (1989).
Reekie, Realtime DSP: The TMS320C30 Course, Revision 3 (Feb. 20, 1994).
RISC Roots: CDC 6000 (1965) www.//bwrc.eecs.berkeley.edu/CIC/archive/cpu_history.html, downloaded Oct. 27, 2006.
Roche et al., "Method of Assuming a Two–Cycle Start, Zero Cycle Stop, Non–Chopping on Chip Clock Control Throughout a VLSI Clock System," Delphion, IBM Technical Disclosure Bulletin, Sep. 1989.
Rowen et al., "A Pipelined 32b NMOS Microprocessors and Microcontrollers," IEEE International Solida–State Circuits Conference, pp. 180–181, 1984.
Rubinfeld et al., "The CVAX CPU, A CMOS VAX Microprocessor Chip", International Conference on Computer Design, Oct. 1987.
Ryan, D.P., "Intel's 80960: An Architecture Optimized for Embedded Control," IEEE Micro, published in Jun. 1988.
Sanamrad et al., "A Hardware Syntactic Analysis Processor," IEEE, Aug. 1987, pp. 73–80.
Sequin et al., "Design and Implementation of RISC I," pp. 276–298 from VLSI Architecture, B. Randell and P.C. Treleaven, editors, Prentice Hall, 1983.
Shepherd et al., "Current and Future Transputers," INMOS Presentation given at Jun. 15, 1988 Workshop on Computer Architecture.
Sherburne, R. W., "Processor Design Tradeoffs in VLSI," U.C. Berkeley, May 1984. PhD Dissertation.
Shih, "Microprogramming Heritage of RISC Design," Proceedings of the 23rd annual workshop and symposium on Microprogramming and microarchitecture, pp. 275–280. (1990).
Shyam, "Hardware External Reference Specification for Enhanced Champion/Paladin," Revision of Nov. 11, 1986.
Sibigtroth, J. M., "Motorola's MC68HC11: Definition and Design of a VLSI Microprocessor," IEEE Micro, 4(1):54–65 (1984).
Signetics Microprocessor Data manual cover page.
Signetics Microprocessor Products Data manual, 8X330 Floppy Disk Formatter/Controller product specification.
Signetics Microprocessor Products Data manual, SC96AH Series Single–Chip 16–Bit Microcontrollers preliminary specification.
Simpson et al., "The IBM RT PC ROMP Processor and Memory Management Unit Archiecture," IBM systems Journal, Dec. 1987; 26(4):346–360.
Simpson, R.O., "The IBM RT Personal Computer," Byte 11 (11):43–78 (Oct. 1986).
Skruhak et al., "Modular Design of a High Performance 32–bit Microcontroller," IEEE 1989 Custom Integrated Circuits Conference, pp. 23.8.1–23.8.4 (1989).
Stanley, R. C., "Microprocessors in brief," IBM J. Res. Develop., 29(2):110–118 (Mar. 1985).

Submicron Systems Architecture Project, Caltech Computer Science Technical Report, Nov. 1, 1991.
Sultan et al., "Implementing System–36 Advanced Peer–to–Peer Networking," IBM Systems Journal, 1987; 26(4):429–452.
Texas Instrument, "TMS 370 Microcontroller Family User's Guide," (1996), 873 pages.
Texas Instruments TMS320C30 Digital Signal Processor product literature, SPRS032A (Apr. 1996, Revised Jun. 1997).
Texas Instruments TMS34010 Graphics System Processor product literature.
The Ring Oscillator VCO Schematic, 1 page.
Thornton, J. E., "Considerations in Computer Design Leading Up To the Control Data 6600," Control Data Chippewa Laboratory (1970).
Thornton, J. E., "Design of a Computer, The Control Data 6600," published by Advanced Design Laboratory (1970).
Toshiba TLCS–42, 47, 470 User's Manual Published in Apr. 1986.
Ungar et al., "Architecture of SOAR: Smalltalk on a RISC," Proceedings of the 11th Annual International Symposium on Computer Architecture ISCA '84. ACM Press, New York, NY pp. 188–197 (1984).
VAX 11/780 Architecture Handbook vol. 1, 1977–1978, 2–7 and G–8.
VAX 8800 System Technical Description vol. 2, EK–KA881–TD–PRE, Section 6, Instruction Box (IBOX), Preliminary Edition (Jul. 1986).
VAX Maintenance Handbook: VAX–11/780, EK–VAXV2–HB–002, 1983 Edition.
Waters et al., "AIX Usability Enhancements and Human Factors," IBM Systems Journal, 1987; 26(4):383–394.
Whiteby–Streven, "Transputer Technical Notes from INMOS," Google Groups; comp.sys.transputer, dated Sep. 7, 1988.
Williams, "Chip Set Tackles Laptop Design Issues, Offers Flat–Panel VGA Control," Computer Design, Oct. 15, 1988; 27(19):21–22.
Agrawal, "Bipolar ECL Implementation," The SPARC Technical Papers, Catanzaro, eds., Springer–Verlag, NY, pp. 201–211. (1991).
Gill et al. Summary of MIPS Instruction. CSL Technical Note No. 237, Computer Systems Laboratory, Stanford University, Nov. 1983. 50 pages total.
Hennessy et al., "Design of a High Performance VSL Processor," Third Caltech Conference on Very Large Scale Integration, Bryant eds., California Institute of Technology, Computer Science Press, pp. 33–54. (1983).
Horowitz et al., "A 32b Microprocessor with On–Chip 2Kbyte Instruction Cache," IEEE International Solid State Circuits Conference, pp. 30, 31 and 328 (1987).
Knapp, "Frequency Stability Analysis of Transistorized Crystal Oscillator," IEEE Transactions on Instrumentation and Measurement, vol. 12, No. 1, pp. 2–5. (Jun. 1963).
Nicoud et al., "The Transputer Instruction Set," IEEE Micro, vol. 9, No. 3, pp. 60–75 (May 1989).
Parasuraman, "High Performance Microprocessor Architectures," Proceedings of the IEEE, vol. 64, No. 6, pp. 851–859. (Jun. 1976).
Walls et al., "A Frequency–Lock System for Improved Quartz Crystal Oscillator Performance," IEEE Transactions on Instrumentation and Measurement, vol. IM–27, No. 3, pp. 249–252 (Sep. 1978).
Acorn Computers Limited; "ARM Datasheet, Part No. 1 85250 0360 0"; Issue No. 1.0; Mar. 17, 1987.
Barron, I. et al.; "Transputer does 5 or more MIPS even when not used in parallel"; Electronics; McGraw–Hill; vol. 56, No. 23; Nov. 17, 1983; pp. 109–115.
Best et al.; "An Advanced–Architecture CMOS/SOS Microprocessor"; IEEE Micro; vol. 2, No. 3; Jul. 1982; pp. 10–26.
Burroughs Corp.; "Burroughs B5500 Information Processing Systems Reference Manual"; 1964.
Dowsing and Woodhams; "Computer Architecture, A First Course"; Van Nostrand Reinhold Co., Ltd. (UK); 1985; pp. 126–139.
Haley, A. et al.; "Forth as Machine Code"; Electronics & Wireless World; vol. 93; No. 1616; Jun. 1987; pp. 584–587.
IC Master; "F8/3870 F6800 Bit–Slice Faichild Microcomputers"; United Technical Publications; 1980; pp. 2016–2040.
INMOS Limited; "IMS T212 Transputer Data Sheet"; Aug. 1987.
INMOS Limited; "IMS T414 Transputer Data Sheet"; Feb. 1987.
INMOS Limited; "IMS T424 Transputer Reference Manual"; Nov. 1984; p. i–62.
INMOS Limited; "IMS T800 Transputer Data Sheet"; Apr. 1987.
Intel; "80386 Programmer's Reference Manual"; 1986.
Koopman, Jr., Philip; "Stack Computers, the new wave"; 1989.
Motorola; "Motorola MC68020 32–Bit Microprocessor User's Manual, Second Edition"; Prentice–Hall; 1985.
Proebsting et al.; "A TTL Compatible 4096–bit N–channel RAM"; Solid–State Circuits Conference; Digest of Technical Papers; 1973 IEEE International vol. XVI; Feb. 1973; pp. 28–29.
Schoeffler, J.; "Microprocessor Architecture"; Industrial Electronics and Control Instrumentation, IEEE Transactions on; vol. IECI–22, issue 3; Aug. 1975; pp. 256–272.
Whitby–Strevens, C.; "The Transputer"; The 12th Annual International Symposium on Computer Architecture, Conference Proceedings; Jun. 17–19, 1985; pp. 292–300.
VLSI Technologies, Inc.; "VL86C010 RISC Family Data Manual"; 1987.
PCT Appl. No. PCT/US90/04245, International Search Report dated Jan. 23, 1991.
EP Appln No. 97200767.8, European Search Report (illegible date).
JP Appln No. 1990–511130.
"A single chip digital signal processor, Part I—architecture and addressing", Richard Pickvance, Electronic Engineering, Feb. 1985, vol. 57, No. 698, pp. 53–56, 59 and 63.
"The Architecture of the SC32 Forth Engine", Hayes et al., The Journal of Forth Application and Research, 1989, vol. 5, No. 4, pp. 493–506.
"Machine Forth, Machine Forth for the ARM processor", Reuben Thomas, Aug. 23, 1999, 10 pages.
"Stack Computers; the new wave, Chapter 5.2: Architecture of the FRISC 3 (SC32)", Philip Koopman, 1989, 9 pages.
The Motorola MC68020, MacGregor, D. et al., IEEE Micro, vol. 4, issue 4, Aug. 1984, pp. 101–118.
MC68020 32–Bit Microprocessor User's Manual, Motorola, Prentice–Hall, 1984.
MOSTEK 1981 3870 / F8 Microcomputer Data Book Feb. 1981, pp. III–76—VI–11.
F8/3870 F6800 Bit–Slice Fairchild Microcomputers United Technical Publications, IC Master, 1980, pp. 2016–2040.
80386 Programmer's Reference Manual Intel, 1986.
Transputer Reference Manual INMOS, Prentice Hall, 1988.

* cited by examiner

EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claims **5-10** is confirmed.

Claims **1-4** are cancelled.

New claims **11-20** are added and determined to be patentable.

11. A microprocessor, which comprises a main central processing unit and a separate direct memory access central processing unit in a single integrated circuit comprising said microprocessor, said main central processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus, said internal data bus being bidirectionally connected to a loop counter, said loop counter being connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register, said stack pointer pointing into said first push down stack, said internal data bus being connected to a memory controller, to a Y register of a return push down stack, an X register and a program counter, said Y register, X register and program counter providing outputs to an internal address bus, said internal address bus providing inputs to said memory controller and to an incrementer, said incrementer being connected to said internal data bus, said direct memory access central processing unit providing inputs to said memory controller, said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory.

12. The microprocessor of claim 11 in which said memory controller includes a multiplexing means between said central processing unit and said address/data bus, said multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus.

13. The microprocessor of claim 11 in which said memory controller includes means for fetching instructions for said central processing unit on said address/data bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle.

14. The microprocessor of claim 13 additionally comprising means connected to said means for fetching instructions for determining if multiple instructions fetched by said means for fetching instructions require a memory access, said means for fetching instructions fetching additional multiple instructions if the multiple instructions do not require a memory access.

15. The microprocessor of claim 13 in which said microprocessor and a dynamic random access memory are contained in a single integrated circuit and said means for fetching instructions includes a column latch for receiving the multiple instructions.

16. The microprocessor of claim 11 in which said microprocessor includes a sensing circuit and a driver circuit, and an output enable line for connection between the random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level, said microprocessor being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

17. The microprocessor of claim 11 additionally comprising a ring oscillator variable speed system clock connected to said main central processing unit, said main central processing unit and said ring oscillator variable speed clock being provided in a single integrated circuit.

18. The microprocessor of claim 17 in which said memory controller includes an input/output interface connected to exchange coupling control signals, addresses and data with said main central processing unit, said microprocessor additionally including a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.

19. The microprocessor of claim 11 in which said first push down stack has a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit.

20. The microprocessor of claim 19 additionally comprising a first pointer connected to said first plurality of stack elements, a second pointer connected to said second plurality of stack elements, and a third pointer connected to said plurality of stack elements, said central processing unit being connected to pop items from said first plurality of stack elements, said first stack pointer connected to said second stack pointer to pop a first plurality of items from said second plurality of stack elements when said first plurality of stack elements are empty from successive pop operations by said central processing unit, said second stack pointer being connected to said third stack pointer to pop a second plurality of items from said third plurality of stack elements when said second plurality of stack elements are empty from successive pop operations by said central processing unit.

* * * * *

Stays are appropriate where, as here, a stay: (1) will simplify the issues in the case; (2) will not prejudice TPL; and (3) is being requested at an early stage of the case. First, the outcomes of the reexaminations will simplify the issues here. Where the claims are rejected, this litigation will end. Where the claims are amended, there will be no past infringement or damages. If any claims survive, the Court will have the benefit of the PTO's analysis of the patents-in-suit and TPL's statements made during the reexaminations to assess possible prosecution history estoppel in claim construction. Second, a stay will not unduly prejudice or tactically disadvantage TPL. Given its on-going practice of offering to license the patents-in-suit, monetary damages will clearly be adequate for TPL. In addition, having waited three years to cause this case to be brought, TPL is obviously in no hurry to have its claims against HTC adjudicated by this Court. Finally, this case is still at an early stage – only minimal discovery has taken place to date, and the parties have not even completed the negotiation of the protective order as of the filing of this motion. No dispositive motions have been filed, and the Court has set no dates for claim construction hearing, close of discovery, or trial.

For at least the reasons stated above, HTC's motion to stay should be granted.

II. BACKGROUND AND RELEVANT FACTS

A. Reexaminations Against Patents-in-Suit

i. U.S. Patent No. 5,809,336

Three reexaminations are pending against the '336 patent (the first one was initiated in November 2006). On March 17, 2009, the PTO issued a *final* Office Action rejecting all claims (1 – 20) of the '336 patent. Declaration of Taryn Lam in Support of Plaintiffs' Motion to Stay All Proceedings Pending Reexamination of the Patents-in-Suit ("Lam Decl."), filed herewith, Ex. B.

ii. U.S. Patent No. 5,530,890

One reexamination is pending against the '890 patent (initiated in January 2009). On April 8, 2009, the PTO initiated a reexamination against all claims (1 – 9) of the '890 patent after finding a "substantial new question of patentability" in light of various prior art. *Id.*, Ex. D.

iii. U.S. Patent No. 5,440,749

(8) a final rejection of claims 29 – 54 of the '584 patent on December 5, 2008 that led to an amendment of claim 29 and cancellation of claims 30 – 54.

The ultimate outcomes of these reexaminations will dramatically simplify the issues in question and trial of the case.

"The primary purpose of the reexamination procedure is to 'eliminate trial of that issue [of patent invalidity] (when the [claim] is canceled) or to facilitate trial of that issue by providing the district court with the expert view of the [USPTO] (when a claim survives the reexamination proceeding).'" *ASCII*, 844 F. Supp. at 1380 (quoting *Gould*, 705 F.2d at 1342). As has been noted by this Court, the claims of a patent are likely be canceled, amended or narrowed during reexamination. *See Target*, 1995 WL 20470, at *2. Each of these possible outcomes brings with it a separate mechanism for simplifying this case.

First, statistically speaking, the most likely result is that the claims of the patents subject to reexamination will be canceled or significantly narrowed during the reexamination process. According to the Patent Office's published statistics, *ex parte* reexaminations result in canceled or modified claims seventy-five percent (75%) of the time, leaving only twenty-five percent (25%) of reexaminations that result in all claims being confirmed. *See* Lam Decl., Ex. Q. Cancellation of claims that have not already received final rejection is particularly likely in the present case given that all the Patents-in-Suit share the same specification, and the PTO has already rejected most of the asserted claims. *Id.*, Exs. A, C, E, G, J, and L-M.

Second, to the extent the claims subject to reexamination are narrowed during reexamination proceedings, the scope of this case will be significantly reduced by the doctrine of "intervening rights." *See* 35 U.S.C. §§ 307(b), 252. For example, as to any amended or new claim that issues from the reexamination: (1) HTC would have no liability for any allegedly infringing activities that took place prior to the date of issuance of the reexamination certificate; and (2) HTC would be entitled to continue to use the accused products as they existed prior to the issuance of the reexamination certificate. *See* 35 U.S.C. § 252; *Eng'd Data Prods., Inc. v. GBS Corp*., 506 F. Supp. 2d 461, 475-76 (D. Colo. 2007) (summary judgment granted to defendant based on intervening rights acquired when plaintiff substantively amended its claims during reexamination).

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

DO NOT USE IN PALM PRINTER

(THIRD PARTY REQUESTER'S CORRESPONDENCE ADDRESS)

FISH & RICHARDSON, P.C.
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

MAILED

APR 03 2009

CENTRAL REEXAMINATION UNIT

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/009,388*.

PATENT NO. *5530890*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

PTOL-465 (Rev.07-04)

Order Granting / Denying Request For Ex Parte Reexamination	**Control No.** 90/009,388	**Patent Under Reexamination** 5530890	
	Examiner JOSEPH R. POKRZYWA	**Art Unit** 3992	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

The request for *ex parte* reexamination filed *16 January 2009* has been considered and a determination has been made. An identification of the claims, the references relied upon, and the rationale supporting the determination are attached.

Attachments: a)☐ PTO-892, b)☐ PTO/SB/08, c)☒ Other: *PTO-1449*

1. ☒ The request for *ex parte* reexamination is GRANTED.

RESPONSE TIMES ARE SET AS FOLLOWS:

For Patent Owner's Statement (Optional): TWO MONTHS from the mailing date of this communication (37 CFR 1.530 (b)). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).**

For Requester's Reply (optional): TWO MONTHS from the **date of service** of any timely filed Patent Owner's Statement (37 CFR 1.535). **NO EXTENSION OF THIS TIME PERIOD IS PERMITTED.** If Patent Owner does not file a timely statement under 37 CFR 1.530(b), then no reply by requester is permitted.

2. ☐ The request for *ex parte* reexamination is DENIED.

This decision is not appealable (35 U.S.C. 303(c)). Requester may seek review by petition to the Commissioner under 37 CFR 1.181 within ONE MONTH from the mailing date of this communication (37 CFR 1.515(c)). **EXTENSION OF TIME TO FILE SUCH A PETITION UNDER 37 CFR 1.181 ARE AVAILABLE ONLY BY PETITION TO SUSPEND OR WAIVE THE REGULATIONS UNDER 37 CFR 1.183.**

In due course, a refund under 37 CFR 1.26 (c) will be made to requester:

a) ☐ by Treasury check or,

b) ☐ by credit to Deposit Account No. _____, or

c) ☐ by credit to a credit card account, unless otherwise notified (35 U.S.C. 303(c)).

cc:Requester (if third party requester)

Obviously, cancellation of any claim resolves all infringement and validity issues with respect to that claim. Similarly, amendment of a claim narrows the case issues, reduces the trial's complexity and length, narrows or resolves discovery issues relating to prior art and damages, and encourages settlement or dismissal.[2] *See Tse v. Apple Inc.*, No. C 06-06573, 2007 WL 2904279, at *3 (N.D. Cal. Oct. 4, 2007) (citing *Pegasus Dev. Corp. v. DirecTV, Inc.*, 2003 WL 21105073 (D. Del. 2003)); *Target Therapeutics, Inc. v. Scimed Life Systems, Inc.*, No. C-94-20775, 1995 WL 20470, at *2 (N.D. Cal. Jan. 13, 1995) ("Absent a stay, the parties may end up conducting a significantly wider scope of discovery than necessary, and the court may waste time examining the validity of claims which are modified or eliminated altogether during reexamination."). Thus, proceeding with the present litigation while claim scope and validity are in constant flux at the PTO would lead to a "tremendous waste of the time and resources of all those involved." *Ricoh Co., Ltd. v. Aeroflex Inc.*, Nos. C03-04669, C03-02289, 2006 WL 3708069, at *5 (N.D. Cal. Dec. 14, 2006); *see also KLA-Tencor Corp. v. Nanometrics, Inc.*, No. C 05-03116, 2006 WL 708661, at *4 (N.D. Cal. Mar. 16, 2006).

TPL's argument that the reexaminations are unlikely to substantially change the asserted claims is directly contradicted by both the facts of these advanced reexaminations with their cancelled and modified claims and by the PTO's statistics on *ex parte* reexaminations. *See* Lam Decl., Ex. Q; *Tse*, 2007 WL 2904279, at *3 (rejecting similar assertion as contravened by PTO statistics); *KLA-Tencor*, 2006 WL 708661, at *4 (noting that statistics suggest that "in a typical case there is a substantial probability a reexamination will have a major impact on the issues to be resolved in the litigation.") (citations omitted). The likelihood that the reexamination results will assist the Court and simplify the issues is "increased significantly" where the reexamination has resulted in a rejection of the asserted claims. *See Ricoh*, 2006 WL 3708069, at *4. TPL's unfounded hope that its claims will survive simply is not supportable.

---

[2] Under the doctrine of intervening rights, substantive amendments to claims will narrow the scope of HTC's liability and damages exposure. Contrary to TPL's insinuations, the doctrine is broadly applied. *See Laitram Corp. v. NEC Corp.*, 163 F.3d 1342, 1348 (Fed. Cir. 1998) (noting that "it is difficult to conceive of many situations in which the scope of a rejected claim that became allowable when amended is not substantively changed by the amendment").

voluntarily cancelled by Defendants. Now, with the reexaminations for the '749 and '148 Patents merged, an additional three-month stay would likewise be beneficial to allow final actions for a majority of the remaining patents-in-suit.[2]

Such a stay will not prejudice the Defendants, as demonstrated by the reexamination experience of the '336 Patent, because none of the claims survived the reexamination in their original form, with all of them either significantly amended or completely cancelled. In particular, the Examiner has added limitations to the now undeniably narrower claims to specifically overcome prior art that was not overcome before.

Among the '336 Patent's original claims 1 through 10, all independent claims 1, 6, 9 and 10 have been amended (hence so have been their dependent claims 2 and 7), while claims 3, 4, 5 and 8 have been cancelled. Because all the (remaining) asserted claims 1, 6, 7, 9 and 10 of the '336 Patent have been amended, intervening rights apply and Defendants will not be allowed to accuse Acer, HTC or any other parties or non-parties of infringing the '336 Patent for any product sold prior to the issuance of the upcoming Reexamination Certificate. 35 U.S.C. § 252; *Seattle Box Co. v. Industrial Crat. & Pack. Inc.*, 731 F.2d 818 (Fed. Cir. 1984). Hence, all products identified in Defendants' Patent Local Rule 3-1 disclosures are free form any claim of infringement of the '336 Patent. The '749, '890 and '148 reexaminations will likely have a similar result.

Additionally, the patentee's actions to date in the reexaminations have provided further intrinsic evidence that will inform the Court's claim construction on the amended claims of the '336 Patent and the other asserted patents should Defendants assert them after the Reexamination Certificate issues. All of the patents share a common specification and recite several identical claim elements that will need to be construed (e.g., the term "ring oscillator" is recited in asserted claims of all four of the patents-in-suit). It is therefore likely that proceedings in the reexaminations will further clarify and inform the Court's claim construction.

Plaintiff Barco's Statement

[2] TPL has made no claim of infringement against Acer or HTC as to the '584 Patent.

permitted in a reexamination proceeding under this chapter."). TPL asserts in its motion, in fact, that "the newly issued claims have the same scope as the original claims…."[2] '890 Motion (Doc. No. 275) at 1-2. Any HTC product that allegedly infringes the '749 and '890 patents post-reexamination, therefore, could have been accused under the originally-issued claims.

Nothing that took place in the reexaminations prevented TPL from undertaking an analysis of accused products long ago. Indeed, when TPL brought its first motion for leave to amend its infringement contentions in June 2010, several asserted claims of the '749 and '890 patents stood *rejected* in the reexaminations. *See* Chen Decl. ¶¶ 18-19. That did not stop TPL from bringing its previous motion, seeking leave to accuse additional HTC products of infringing those rejected claims. TPL's disingenuous attempt to use unrelated developments in the reexaminations as an excuse for its lengthy delay in undertaking its accused product analysis should be rejected.[3]

2. The Proposed Amendments Confirm TPL's Lack of Diligence.

The vast majority of the HTC products that are the subject of TPL's proposed amendment were introduced before the claim construction briefing started in December 2010. Chen Decl. ¶¶ 3-17. TPL's attempt to add the HTC Desire and HTC EVO 4G products is particularly instructive in showing its lack of diligence.

TPL argues that in performing its analysis of HTC products (which, as noted above, began after February 11, 2011 as to the '749 patent), TPL "reviewed press releases and other publicly available information on new HTC product releases." '749 Motion at 4. The press releases for the HTC Desire and HTC EVO 4G products, however, were published on HTC's website more

---

[2] HTC does not concede that the newly issued claims have the same scope as the original claims, but rather, contends that the new claims are narrower. In any event, TPL's assertion that the new claims have the same scope as the original claims demonstrates that it could not reasonably have believed that it had to await the issuance of the new claims before beginning its investigation of HTC products.

[3] TPL's reliance on the ongoing reexaminations is also belied by the fact that it is seeking to add accused HTC products as to claim 3 of the '749 patent, which was not amended during the reexaminations and was not previously asserted in this case. TPL's previous motion for leave to amend, which this Court denied, also attempted to add claim 3.

TPL argues that HTC would not have to conduct additional prior art searches because the reexamined claims cannot be larger in scope than the originally-issued claims. As noted, however, the new claims introduce narrowing limitations that will require additional analysis to locate those limitations in the prior art. This prejudice is compounded by the fact that TPL is proposing to nearly double the number of asserted claims under the '749 and '890 patents.

TPL cites to *Advanced Micro Devices v. Samsung Electronics*, No. C-08-00986, 2010 WL 1293374, at *3 (N.D. Cal. Mar. 31, 2010), to argue that "because the scope of new claims are the same as the scope of the originally asserted claims, the proposed amendments do not alter any theories of infringement." '890 Motion at 7. However, in *Advanced Micro Devices*, the accused products in the final infringement contentions ("FIC") were previously identified by the defendant, believing that those products were already accused of infringement, and communicated to the plaintiff. *Id*. at *1. "The only thing 'new' about the products accused in the FIC is the fact that they are grouped into ten categories, rather than the four categories named in the PIC [(preliminary infringement contentions)]." *Id*. at *2. *Advanced Micro Devices* in no way supports TPL's attempt to accuse additional products or assert new claims at this late stage.

TPL also misapplies *Performance Pricing, Inc. v. Google Inc.* to argue that the Court should allow TPL "to include allegations that would provide an 'alternative means' of infringement." '890 Motion at 7. That case, however, did not involve reexamined claims or an attempt to add accused products. *Performance Pricing, Inc. v. Google Inc.*, No. 2:07-cv-432, slip op. at 1 (E.D. Tex. Sept. 15, 2009) ("Plaintiff represents that the Amended Contentions did not accuse any new [defendant] products or services of infringement…."). The plaintiff there was merely "asking the [c]ourt for leave to amend its Infringement Contentions to add a doctrine of equivalents infringement analysis." *Id*.[5]

[5] TPL argues that if its motion is denied, it may file a separate lawsuit with respect to its proposed amendments. This is the same threat TPL made in its earlier motion for leave to amend. This Court declined to consider this argument the last time, reasoning that "[b]ecause TPL has not filed separate actions predicated on its proposed amended infringement contentions, any opinion on the propriety of such theoretical actions would be premature." September 10, 2010 Order at 10:5-7. Nor has TPL brought a new action against HTC based on the proposed amendments that are the subject of the present motion. HTC will therefore not address this argument beyond

> microprocessor, . . . said direct memory access central processing unit providing inputs to said memory controller . . .

'890 patent, 32:44-47 (Mar Decl., Exh. K). The plain meaning of the claim language is confirmed by the '890 specification, which describes and illustrates a main CPU and a separate DMA CPU in a single integrated circuit making up a microprocessor. '890 patent, 6:17-20. The parties agree that "CPU" means "an electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions." (JCCS Ex. A, No. 7 Dkt. 305).

Given the foregoing, construction of the term should be straightforward based on ordinary meaning of the claimed structure, and TPL's proposed construction captures the essence of such ordinary meaning. Plaintiffs, on the other hand, do not offer a structural definition of the claimed term. Instead, they restate the term with extraneous functional limitations that are not supported by the specification, in particular, prohibiting ***any*** operation of the DMA with assistance, no matter how minor, of the main CPU. Yet the claim language includes no such prohibition, nor is there support for such limitation in the specification. In contrast, TPL's construction is correct because it describes the "DMA CPU" as properly distinct ("separate") from the main CPU, in keeping with the claim structure, and defines the DMA CPU in accordance with the specification, as an "electrical circuit for reading and writing to memory."

The specification includes at least two preferred embodiments of the DMA CPU. The first is shown in Figure 2, where the microprocessor 50 has a separate DMA CPU 72 with "the ability to fetch and execute instructions." '749 patent, 8:22-23; Mar Decl., Exh. M. "[A] second embodiment of a microprocessor in accordance with the invention," shown in Figure 9, discloses a DRAM die with on-chip memory and a "DMA CPU" 314. *Id*., 4:61-62. Here, "the DMA processor 72 of the microprocessor 50 has been replaced with a more traditional DMA controller." *Id*., 12:63-65 (emphasis added). This "more traditional DMA controller" is one that functions more as a traditional state machine, without the ability to fetch its own instructions that characterizes a CPU. *See, e.g., id*., 1:55-58, Background of the Invention (DMA controllers in conventional microprocessors "can provide routine handling of DMA requests and responses, but some processing by the main central processing unit (CPU) of the microprocessor is required.").

that Figure 13 shows exactly the same arrangement as Figure 2, with precisely the same "direct coupling" between the top and next item registers and the ALU, as shown in the figures.

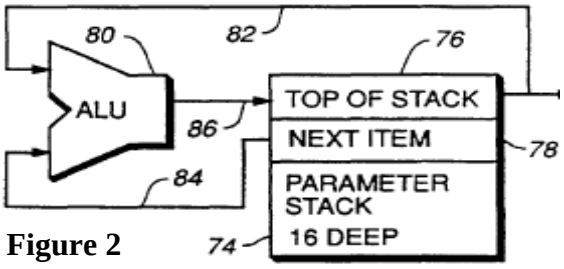


Figure 2

TPL's assertion that the "STACK POINTER" in Figure 13 (of which the relevant portion is reproduced at right) is connected to the first push down stack is similarly baseless. *See* Opening Br. at 21:4-5. The stack pointer shown in Figure 13 is not used to communicate to the ALU at all. It is instead pointing to the *bottom* of the first push down stack. *See* '749, Fig. 13. Finally, TPL's argument based on the stack architecture in Figure 21 is similarly inapposite. Nothing in Figure 21 shows an ALU, let alone any connection between any push-down stack with top and next item registers and the ALU. Instead, the stack pointer is used only to manage inter-stack operations of the "triple cache stack architecture" illustrated in Figure 21. '336, 18:23-27.

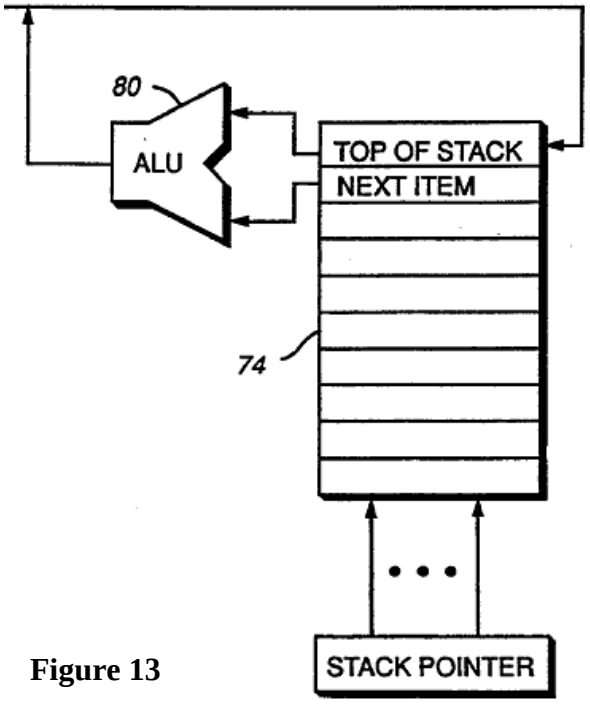


Figure 13

The primary flaw in TPL's arguments regarding Figure 13 and 21 is that it ignores the specific term at issue here, the "**first** push down stack **connected to said arithmetic logic unit**." The portions of the figures cited by TPL relate to other stacks in the specification that are not the first push down stack. One such example is the "second push down stack" that is separately recited in claim 10. But the claim language itself confirms that the "**first** push down stack" is the one depicted in Figures 2 and 13 as item 74, because it is the only push down stack in the specification that is "connected to said arithmetic logic unit" ***and*** has a "top item" register and a "next item" register connected to inputs of the ALU, as expressly recited in the claim language. TPL's attempt to point to details of other stacks that are not the "first push down stack" is unavailing.

United States Patent [19]

Talbot

[11] **Patent Number: 4,689,581**

[45] **Date of Patent: Aug. 25, 1987**

[54] **INTEGRATED CIRCUIT PHASE LOCKED LOOP TIMING APPARATUS**

[75] Inventor: **Gerald R. Talbot**, Bristol, United Kingdom

[73] Assignee: **Inmos Limited**, Bristol, United Kingdom

[21] Appl. No.: **756,434**

[22] PCT Filed: **Nov. 2, 1984**

[86] PCT No.: **PCT/GB84/00375**

§ 371 Date: **Jul. 3, 1985**

§ 102(e) Date: **Jul. 3, 1985**

[87] PCT Pub. No.: **WO85/02076**

PCT Pub. Date: **May 9, 1985**

[30] **Foreign Application Priority Data**

Nov. 4, 1983 [GB] United Kingdom 8329511

[51] **Int. Cl.**[4] **H03L 7/08**; H03L 7/18

[52] **U.S. Cl.** ..... **331/1 A**; 331/8; 331/17; 331/25; 331/34; 331/111; 331/113 R

[58] **Field of Search** ..... 331/1 A, 8, 17, 25, 331/34; 357/51

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,930,304	1/1976	Keller et al.	357/51 X
4,034,309	7/1977	Vaughn	331/1 A
4,093,873	6/1978	Vannier et al.	331/51 X
4,141,209	2/1979	Barnett et al.	357/51 X
4,210,875	7/1980	Beasom	330/277
4,494,021	1/1985	Bell et al.	331/25 X
4,524,333	6/1985	Iwata et al.	331/25 X

OTHER PUBLICATIONS

Brooks et al, "High Capacity Electronics System for a Compact, Battery-Operated Computer," Hewlett-Packard Journal, vol. 34, No. 6, Jun. 1983, pp. 10–15.

Primary Examiner—Siegfried H. Grimm
Attorney, Agent, or Firm—Edward D. Manzo

[57] **ABSTRACT**

An integrated circuit device includes a timing apparatus arranged to produce timing signals whose frequency is a multiple of that of a clock signal. The timing apparatus, which includes a phase locked loop, is formed on a single chip and no external components are necessary. The phase locked loop includes a convertor and filter circuit (**11**), the convertor (**14**) including two transistor current sources (**19,24**) whose current magnitude is determined by a current reference circuit (**13**) including current mirror transistors (**28, 31**). The current sources (**19, 24**) are controlled by increase and decrease output signals from a phase and frequency comparator (**7**) such that the output of the convertor (**14**) depends upon the mark space ratio of the comparator output signals. The output of the convertor (**14**) is filtered and then fed as a control voltage to a voltage controlled oscillator (**12**). The oscillator output is fed by way of a divider to the phase comparator (**7**) and also provides the high frequency input timing signal for a logic device, such as a microcomputer (**2**). As the timing apparatus is fabricated using MOS technology, it is not possible to forecast its performance accurately. Surprisingly, it has been found that the timing apparatus of the invention is capable of exhibiting closed loop stability without further trimming. However, to ensure that such closed loop stability can always be obtained, additional components, for varying the parameters of the circuits may be provided, said components being connectible into the circuit by programmable switches, such as laser fuses (as **33, 42**).

24 Claims, 4 Drawing Figures

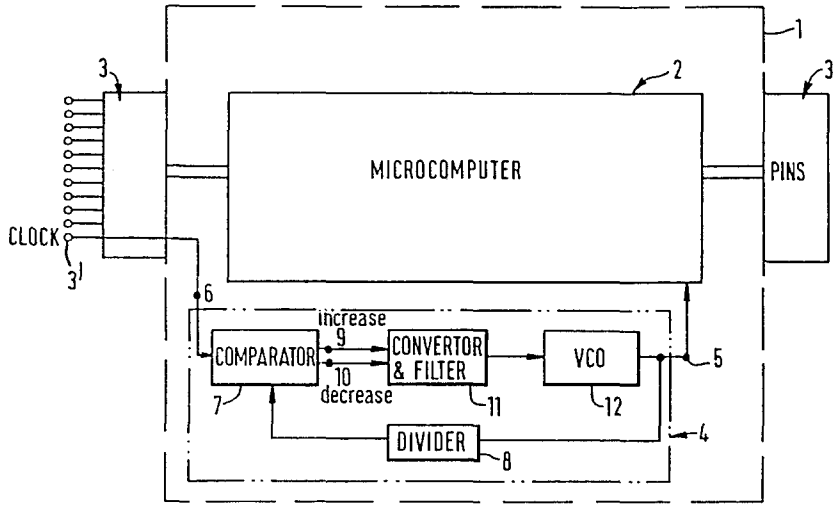


FIG. 1

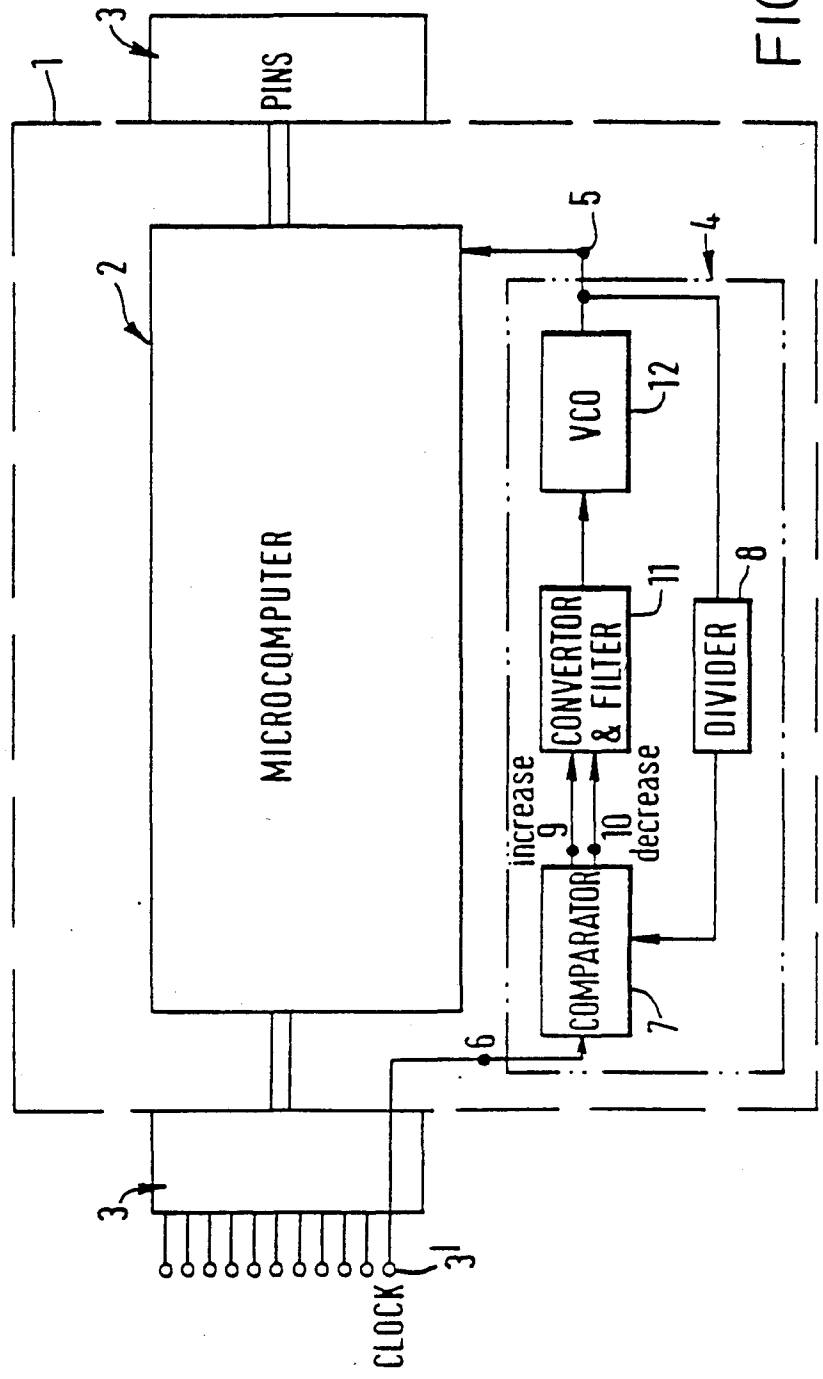
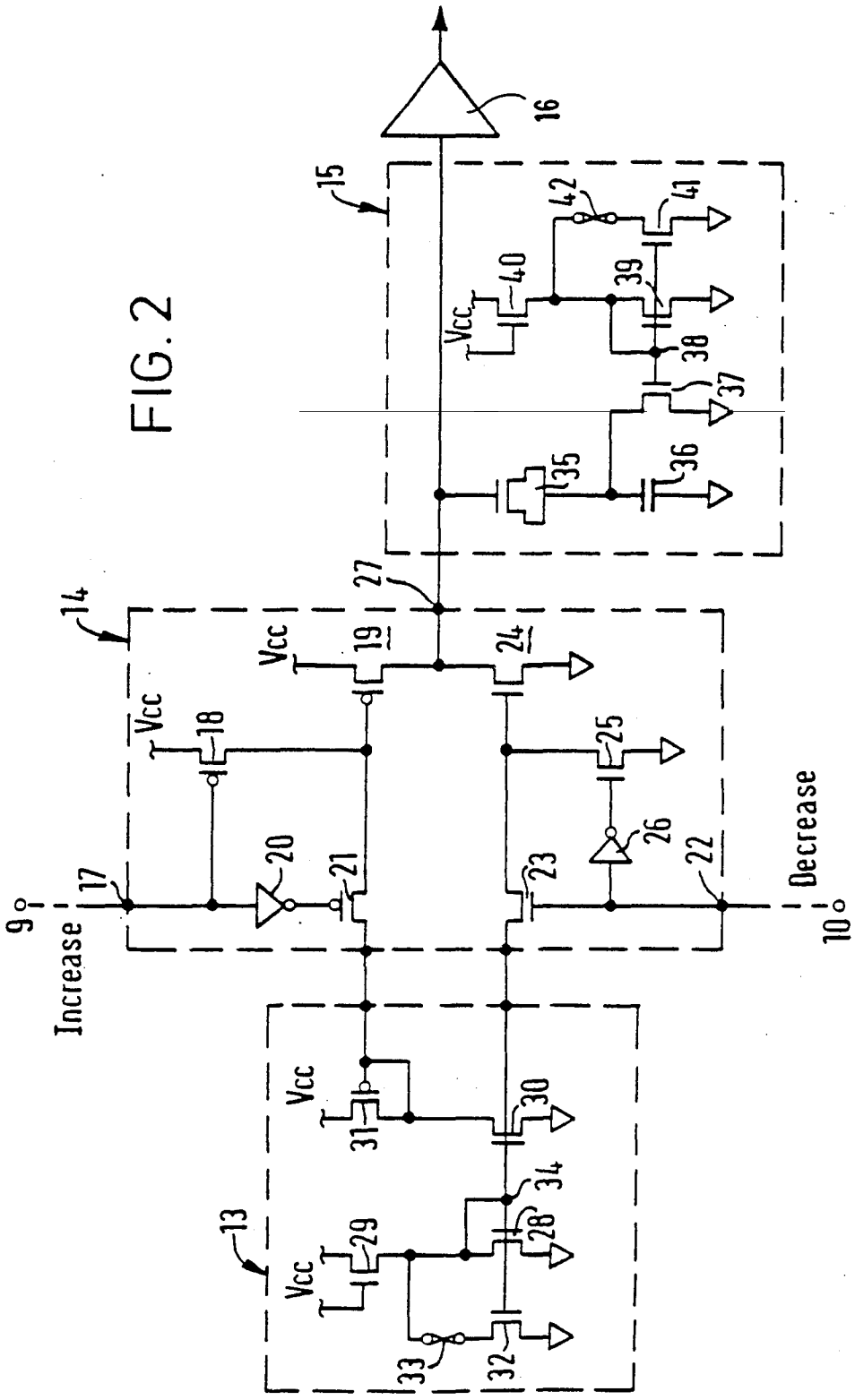

1
3
PINS
2
MICROCOMPUTER
5
4
VCO
12
CONVERTOR & FILTER
11
DIVIDER
8
increase
9
10
decrease
COMPARATOR
7
6
3
3'
CLOCK

FIG. 2


16
15
42
41
40
39
38
37
35
36
Vcc
27
14
19
24
18
25
26
22
17
20
21
23
9
10
Increase
Decrease
13
31
30
34
28
29
33
32

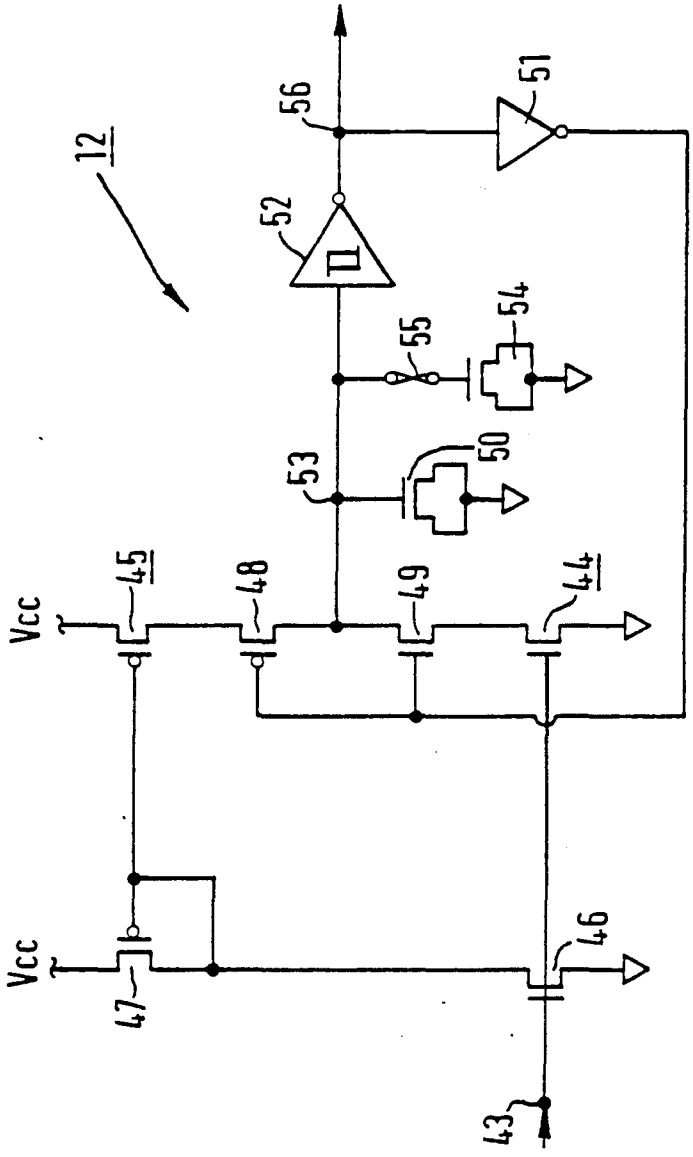


FIG. 3

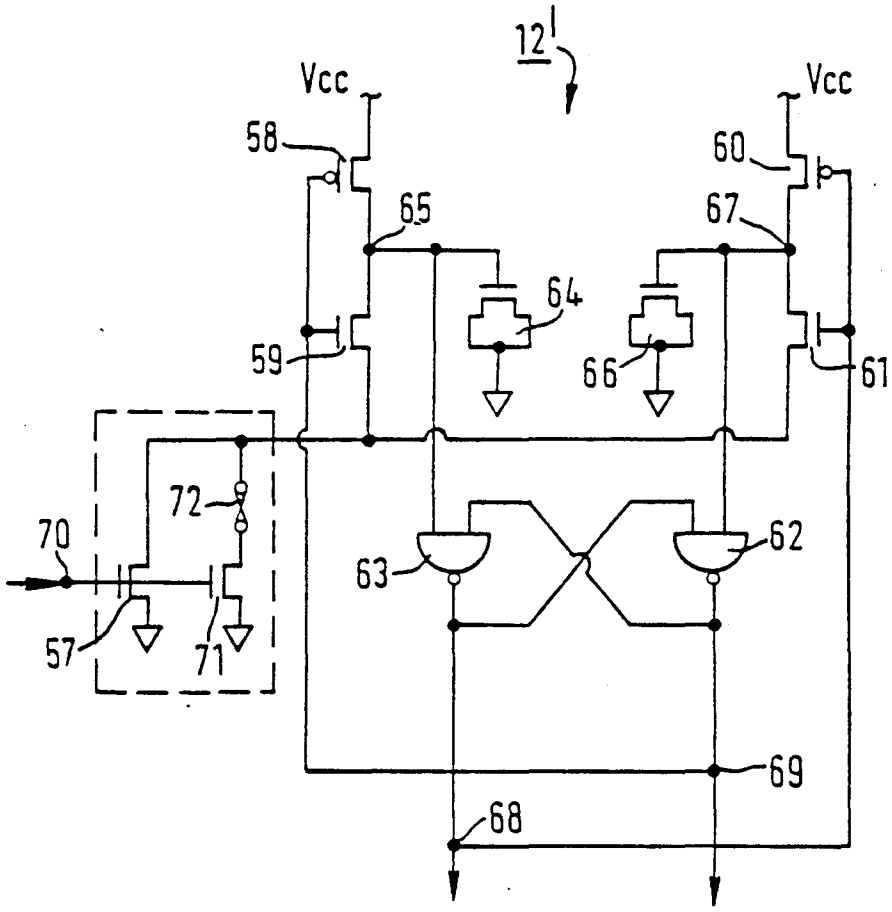


FIG. 4

INTEGRATED CIRCUIT PHASE LOCKED LOOP TIMING APPARATUS

The present invention relates to a timing apparatus for generating timing pulses.

For example, the timing pulses generated may be used for a microcomputer of the type described in our co-pending UK patent application No. 8233733 filed Nov. 26, 1982 or of the type described in our co-pending European patent application No. 83307078.2 filed Nov. 18, 1983.

The MOS technology processes used to manufacture microprocessors result in devices which are similar, but of varying performance. It is normal practice to measure the maximum operating speed of such devices after they have been manufactured, and it is found that the operating speed of the devices differ. The fast devices should be used with high frequency clock signals such that full advantage is taken of their potential to operate at high speeds, but the slower devices require a low frequency clock input. Thus, if the clock signals are to be matched to the operating speed of the manufactured devices it is currently necessary to provide an external clock of suitable speed once the performance of the microprocessor has been determined.

Furthermore, it is difficult to generate and distribute high frequency clock signals, and presently this imposes a real and practical limitation to the operating speed of current microprocessors and microcomputers.

Phase locked loops have been used for many years to construct frequency multipliers, and in recent times integrated circuit phase locked loops have been provided. However, the components of a phase locked loop are not easy to manufacture be existing integrated circuit manufacturing techniques such that existing integrated circuit phase locked loops require additional components external to the integrated circuit.

According to the present invention there is provided a timing apparatus including a control loop circuit and arranged upon receipt of a clock signal to produce a timing signal whose frequency is a multiple of that of said clock signal, said timing apparatus being formed on a single chip.

The present invention also extends to an integrated circuit timing apparatus comprising a phase locked loop arranged to produce an output timing signal whose frequency is a multiple of that of an input clock signal, wherein said phase locked loop comprises a voltage controlled oscillator and means for generating a voltage signal for controlling said oscillator, said generating means comprising one or more current sources.

According to a further aspect of the invention there is provided an integrated circuit device comprising a logic device connected to input and output pins, and a timing apparatus as defined above, an input of the timing apparatus being connected to one of the input pins for receipt of the clock signal, and an output of said timing apparatus being connected to said logic device to supply timing signals thereto.

Preferably, said logic device is a microcomputer.

The present invention also extends to a method of supplying timing signals to an integrated circuit logic device comprising applying a low frequency clock signal to an input of said integrated circuit, including in said integrated circuit a timing apparatus for receiving said clock signal and producing a timing signal having a frequency which is a multiple of that of said clock signal, and applying said high frequency timing frequency to said logic device.

Preferably, the operating speed of said logic device is determined and the frequency of the timing signal is matched to said operating speed.

The present invention also provides timing apparatus arranged to produce clock pulses, which timing apparatus includes a loop circuit incorporating a voltage controlled oscillator, the output signal being a multiple of the frequency of the input signal, said voltage controlled oscillator being responsive to the operation of one or more current sources, the operation of the current sources being adjustable to modify the output frequency.

The aforesaid modification of the current sources may be achieved by laser fusing techniques.

The aforesaid current sources may include integrated circuits and the modification of the current sources may be effected by a variety of techniques which make or break connections in said integrated circuits. These may incorporate laser fuses, electrically blown fuses, non-volatile storage elements or laser anti-fuses.

The invention includes a computer device, which may for example consist of a microcomputer, in combination with timing apparatus as aforesaid for generating clock pulses for use by the computing apparatus.

The invention also includes a network of computer devices in which clock pulses are produced by timing apparatus as aforesaid.

Embodiments of the present invention will hereinafter by described, by way of example, with reference to the accompanying drawings, in which:

FIG. **1** shows schematically an integrated circuit device including timing apparatus of the present invention;

FIG. **2** shows an embodiment of a convertor and filter circuit of the timing apparatus of FIG. **1**,

FIG. **3** shows a circuit diagram of one embodiment of a voltage controlled oscillator circuit of the timing apparatus of Figure **1**, and

FIG. **4** shows a further embodiment of a voltage controlled oscillator circuit of the timing apparatus.

FIG. **1** shows an integrated circuit device fabricated using complementary MOS technology on a single silicon chip **1**. The integrated circuit device includes a logic device **2** connected to input and output pins **3**.

In the embodiment illustrated, the logic device **2** is shown to be a microcomputer, and, for example, could be a microcomputer of the type described in our co-pending European Patent application No. 83307078.2 filed Nov. 18, 1983 which is fabricated on a single silicon chip.

However, the logic device **2** can be any circuit capable of performing logic operations which requires timing signals. Thus, the logic device **2** could be a processor, a central processing unit, an arithmetic logic unit and the like.

The integrated circuit device of FIG. **1** also includes timing apparatus, generally indicated by the reference numeral **4**, arranged to receive an external clock signal applied to one of the pins **3'** and to generate a timing signal at an output **5** for application to the logic device **2**.

The timing appartus **4** includes a control or closed loop circuit and is arranged to provide at its output **5** a timing signal whose frequency is a multiple of the frequency of the clock signal fed to its input **6** by way of the pin **3'**.

As is clear from FIG. 1, all of the components of the timing apparatus 4 are on the single silicon chip and the timing apparatus 4 has been designed such that it does not require any components external to the chip 1.

The basic structure of the control loop circuit of the timing apparatus 4 is apparent from FIG. 1 and it will be seen that it is constituted by a phase locked loop. The clock signal applied to the pin 3' is connected by way of the input 6 to a digital phase and frequency comparator 7 which is arranged to compare the input clock signal with a further signal fed back from the output 5 by way of a divider 8.

If the phase or frequency of the signal fed by the divider 8 to the comparator 7 differs from the input clock signal the comparator 7 is arranged to produce appropriate output signals. In this respect, if the frequency of the input signal from the divider 8 is lower than that of the clock signal the comparator 7 will produce an increase output signal on its output 9 to indicate that the frequency is to be increased. Similarly, if the frequency of the signal fed by the divider 8 to the comparator 7 is higher than that of the clock signal the comparator will produce a decrease output signal at its output 10 to signify that the frequency of the output signal has to be decreased.

The output signals from the comparator 7 on the outputs 9 and 10 are a series of pulses which are fed to a convertor and filter circuit 11 which is arranged to convert the output pulses from the comparator 7 into a voltage signal for controlling the frequency of oscillation of a voltage controlled oscillator circuit 12. In this respect, it is the amplitude of the voltage signal applied to the oscillator circuit 12 which determines the frequency of the oscillations and hence the frequency of the signal appearing at the output 5 of the timing apparatus 4.

As described above, the high frequency output signal appearing at the output of the voltage controlled oscillator 12 is fed back by way of the divider 8 to the phase comparator 7. The divider 8 is arranged to divide the frequency of the signal at its input by a predetermined integer N. It will thus be apparent that the phase locked loop will function to produce at its output 5 a signal whose frequency is N times the frequency of the clock signal applied to its input 6.

Generally, the comparator 7 will compare the frequency of its two input signals. However, when the phase locked loop has operated to make these frequencies substantially identical, the comparator 7 will compare the phases of the two input signals to accurately lock the loop.

Preferably, the divider 8 is programmable such that the value of the divider integer N may be varied as required. This can be done, for example, by providing connections in the divider circuit which can be made or broken as required. Thus, laser fuses, electrically blown fuses, non-volatile storage elements and/or laser anti-fuses could be provided in the divider circuit 8.

It is known to use a phase locked loop to construct a frequency multiplier in which the frequency of the output signal is a multiple of the frequency of the input signal and in this respect, the basic operation of the phase locked loop shown in FIG. 1 will be clear to anyone skilled in the art and is not further described herein.

For closed loop stability it can be shown that the Bode plot of the frequency response of the open loop should have a positive phase margin when the logarithm of the gain is zero. The frequency response of the open loop is dependent upon both the centre frequency of the voltage controlled oscillator circuit 12 and the transfer function of the convertor and filter circuit 11.

MOS manufacturing processes do not permit the physical properties of components of the integrated circuit to be sufficiently accurately controlled and thus using MOS technology it is not possible to determine in advance the centre frequency of the oscillations and the transfer function of the filter circuit. Thus, existing integrated circuit phase locked loops are provided with additional components external to the integrated circuit. Generally, these external components include filtering circuits and circuits for determining the centre frequency of the oscillator, these circuits being chosen to have characteristics which correspond to the measured responses of the integrated circuit once it has been fabricated.

The integrated circuit phase locked loop of the present invention has been designed such that all of its components can be manufactured using an MOS manufacturing process and such that external components are not required to provide closed loop stability.

Originally, the inventors designed the phase locked loop to include optional and alternative components connectible into the loop by way of fuses such that manufacturing variations could be compensated. Surprisingly, they found that the design of the convertor and filter circuit and of the voltage controlled oscillator means that in many cases trimming of the phase locked loop was not necessary. Accordingly, in many practical cases, it is only necessary to provide for variation of the divider integer N of the divider 8 such that the frequency of the output signal can be chosen as is required.

The convertor and filter circuit 1 of the phase locked loop is shown in FIG. 2 and is connected to receive both the increase output signal 9 and the decrease output signal 10 from the comparator 7. In this respect, each of the output signals from the comparator consists of a stream of pulses whose mark space ratio is proportional to the difference in frequency or phase identified by the comparator 7. The circuit 11 has the function of converting these streams of pulses into a DC voltage whose amplitude controls the voltage controlled oscillator 12. In addition, it is this circuit 11 which ensures the stability of the phase locked loop in that its transfer function is arranged to ensure that the loop has a positive phase margin at zero gain.

The circuit shown in FIG. 2 comprises a programmable current reference circuit 13, a pulse to voltage convertor circuit 14, a filter circuit 15, and an output buffer 16 for feeding the output signal to the voltage controlled oscillator circuit 12.

The increase signal from output 9 is fed to a first input 17 of the convertor 14 and is applied by way of a P channel transistor 18 to the gate of a further P channel transistor 19 which acts as a current source and whose source is connected to the voltage supply Vcc. The increase signal is also fed by way of an inverter 20 and a further P channel transistor 21 to the gate of the current source transistor 19. It will be appreciated that when negative going pulses of the increase signal are applied to the gate of the transistor 18, this transistor 18 will conduct and render the current source transistor 19 non-conductive. Positive going pulses of the increase signal when inverted by the inverter 20 and applied to the gate of the transistor 21 will cause the transistor 21 to conduct and apply negative pulses to the gate of the

transistor **19** which will thus be rendered conductive. The magnitude of the current flow from the current source transistor **19** will be determined by the magnitude of the voltage applied to its gate and thus by the current reference circuit **13** as is described below.

The decrease output signal from comparator output **10** is applied to an input terminal **22** of the convertor circuit **14** and then to the gate of an N channel transistor **23** whose source-drain path is connected to the gate of an N channel transistor **24** which is also arranged to act as a current source, and whose source is connected to ground. The gate of the current source transistor **24** is also connected to the source-drain path of a further N channel transistor **25** whose gate is connected by way of an inverter **26** to the input terminal **22**.

Negative going pulses applied to the input terminal **22** are inverted by inverter **26** such that the positive pulses applied to the gate of the transistor **25** render this transistor conductive and hence the current source transistor **24** non-conductive. The positive going pulses of the decrease signal will be effective to render the transistor **23** and hence the current source transistor **24** conductive and again the magnitude of the current flow will be determined by the voltage applied to the gate of the transistor **24**.

The current source transistor **19** will thus be controlled by the increase signal to produce positive sense current pulses at an output **27** whilst the current source transistor **24** will be controlled by the decrease signal to produce negative sense current pulses at the output **27**. It is required that the magnitude of the current produced at the output **27** by the transistor **19** in response to the application of a voltage of a predetermined magnitude at its gate be identical to that produced by the transistor **24** in response to the application of a voltage of the same predetermined magnitude at its gate. The magnitude of the current produced by each of the transistor current sources **19** and **24** is determined by way of the programmable current reference circuit **13** which utilizes current mirrors.

The programmable current reference circuit **13** includes an N channel current mirror provided by a transistor **28** whose width to length ratio is substantially the same as that of the current source transistor **24**. The gates of the transistors **24** and **28** are connected together. The gate **34** of the current mirror transistor **28** is also connected to its drain and by way of a further N channel transistor **29** to the voltage supply Vcc. The resistance of the transistor **29** determines the source-drain current of the transistor **28** and hence the voltage which appears on its gate **34**. The gate voltage of the current mirror transistor **28** acts as a reference voltage which is applied to the gate of the transistor **24** to determine the current flowing therethrough. In this instance, as the transistors **24** and **28** have the same width to length ratio, the currents flowing through the transistors **24** and **28** will be the same.

The reference voltage appearing at the gate **34** of the transistor **28** and determining the current through the current source transistor **24** is also applied to the gate of a further N channel transistor **30** whose source-drain path is connected by way of a P channel transistor **31** to the voltage source Vcc. The width to length ratio of the transistors **28** and **30** is the same such that the current flowing through the transistors **30** and **31** will be the same as that flowing in the transistor **24**.

The P channel transistor **31** is in fact a current mirror for the P channel current source transistor **19** of the

convertor circuit **14**. It will be seen that the gate of the P channel transistor **31** is connected to its drain such that the flow of current through the transistor **31** puts a voltage on its gate which is also applied to the gate of the transistor **19**, and as the width to length ratios of the transistors **19** and **31** are the same, the current flowing through the transistor **19** will have the same magnitude as that flowing through transistor **31**. Hence, it will be apparent that the reference circuit **13** is operative to generate a predetermined reference voltage which is arranged to ensure that both of the current source transistors **19** and **24** provide a current of equal magnitude.

Of course, the transistors **19** and **24**, acting as current sources, are controlled by the application of the increase and decrease signal pulses applied to the input terminals **17** and **22**.

The magnitude of the current output from the current source transistors **19** and **24** is determined by the value of the reference voltage and this in turn depends upon the width to length ratios of the transistors **28** and **29**. Clearly, the gains of the transistors **28** and **29** can be chosen as required and means can be provided for altering the gain if the CMOS circuit as manufactured does not provide the required circuit parameters.

Thus, in the embodiment illustrated in FIG. **2**, a further N channel transistor **32** is shown and its source-drain path is connected, by way of a programmable switch **33**, in series with the source-drain path of the transistor **29**. In the embodiment shown, this programmable switch is a normally closed fuse **33** which can be blown, for example, by laser. In the embodiment illustrated, with the fuse **33** normally closed, the gain exhibited by the transistor **28** is determined both by its width to length ratio and by that of the transistor **32**. Thus, the value of the reference voltage at gate **34** can be changed by blowing the fuse **33** to form an open circuit. If required, further transistors as **32** with appropriate fuse links as **33** can be provided.

The voltage convertor circuit **14** provides at its output **27** a plurality of positive and negative going current pulses whose magnitude is determined by the current reference circuit **13** but whose presence and frequency are controlled by the incoming increase signal pulses at input **17** and decrease signal pulses at input **22**. The convertor and filter circuit **11** incorporates the filter **15** at whose output a voltage signal for controlling the voltage controlled oscillator circuit **12** is provided.

The filter circuit **15** is a low pass lead/lag filter also incorporated by CMOS techniques in the integrated circuit. It will be seen that this filter circuit **15** includes a MOS capacitor **35** which is connected between the output **27** of the convertor and ground by way of a capacitor **36**. In addition, the MOS capacitor **35** is connected to ground by way of the source-drain path of a transistor **37**. The transistor **37** is an N channel transistor biased by way of the control voltage appearing on its gate **38** to operate as a resistor and thereby form with the MOS capacitor **35** an RC filter. The control voltage at the gate **38** is determined by way of a current mirror incorporating an N channel transistor **39** connected to Vcc by way of a further N channel transistor **40**. The control voltage at the gate **38** which determines that the transistor **37** functions as a resistor depends upon the width to length ratios of the transistors **39** and **40**.

Clearly, the characteristics of the filter circuit **15** can be altered as required by altering the gains of the transistors **39** and **40**. For example, and as illustrated, a further N channel transistor **41** can have its source-drain path

connected by way of a programmable switch such as a fuse **42**, to the source-drain path of the transistor **40**. It would be intended that the fuse **42** be normally closed upon manufacture such that the gain exhibited by the transistor **39** would be determined both by its width to length ratio and by that of the transistor **41**. Blowing of the fuse **42** would render it open circuit and alter the control voltage at gate **38**.

The voltage output signal from the filter circuit **15** is a DC voltage whose magnitude is determined by the mark space ratios of the input signals fed to the convertor **14** at inputs **17** and **22**. Thus, the application of an increase signal pulse causes an increase in the voltage output of the filter whereas the application of a decrease signal pulse causes the voltage to be decreased.

The output voltage from the filter circuit **15** is fed by way of a buffer circuit **16** which provides a low impedance drive circuit for the voltage controlled oscillator and also includes a filter to smooth out ripples in the output of the filter circuit **15**.

The frequency of oscillation of the frequency controlled oscillator **12** is determined by the magnitude of the voltage signal fed thereto as indicated earlier. A first embodiment of the voltage controlled oscillator circuit **12** is illustrated in FIG. **3**.

The voltage output from the buffer **16** is fed to an input terminal **43** of the voltage controlled oscillator circuit and is arranged to control the current flowing through an N channel transistor **44** acting as a current source and a P channel transistor **45** which also acts as a current source. The control voltage at input **43** is connected directly to the gate of the N channel transistor **44** such that it directly determines the current flowing through this transistor **44**. The same current is arranged to be generated in the P channel transistor **45** by the use of current mirrors. Thus, the control voltage at input terminal **43** is also applied to the gate of a further N channel transistor **46** having the same width to length ratio as the transistor **44** such that the same current is arranged to flow in both transistors **44** and **46**. The source-drain path of the transistor **46** is connected in series with the source-drain path of a P channel transistor **47** whose drain is connected to its gate. The gate voltage of the P channel transistor **47** is applied to the gate of the current source transistor **45** to induce a current therein. It will be appreciated that when a predetermined voltage is applied to the input **43**, both current source transistors **44** and **45** will produce a current of the same magnitude.

The P channel transistor **45** is connected by way of a further P channel transistor **48** to a node **53** connected to one terminal of a MOS capacitor **50**. Similarly, the current source transistor **44** is connected to the node **53** by way of an N channel transistor **49**. The transistors **48** and **49** are arranged to act as switches.

The gates of the two switching transistors **48** and **49** are each connected by way of an inverter **51** to the output of a Schmitt trigger **52**. The input of the Schmitt trigger **52** is also connected to the node **53**.

Let us assume initially that the transistor switch **48** is ON such that the current supplied by the transistor current source **45**, and determined by the magnitude of the voltage at input **43**, flows to charge the MOS capacitor **50**. The voltage on the gate of the switch **48** from the inverter **51** will be low and able to maintain the transistor **48** ON and at the same time will hold the transistor **49** OFF. The output from the Schmitt trigger **52** will be high and initially the input to the Schmitt

trigger **52** will be low. However, the current flowing into the capacitor **50** from the current source **45** will increase the voltage at the node **53** and eventually will attain a trigger voltage for the Schmitt trigger **52** such that the output state of the Schmitt trigger **52** will change from high to low. A high level voltage will then be applied by the inverter **51** to the gates of the transistors **49** and **48** switching the transistor **48** OFF and thereby curtailing the charging of the capacitor **50**. The transistor switch **49** will be switched ON such that the transistor **49** and the current source transistor **44** will provide a discharge path for the capacitor **50**. The magnitude of the discharge current through the transistor **44** will be determined by the magnitude of the voltage at the input terminal **43**. Of course, as the capacitor **50** discharges the voltage at the node **53** will fall and when it reaches the other trigger value for the Schmitt trigger **52**, the output of the Schmitt trigger will again change state. Thus, an oscillating output signal will be provided at the output **56** of the voltage controlled oscillator circuit and the oscillation will be sustained.

The frequency of the oscillation will depend upon the capacitance of the MOS capacior **50** and upon the value of the current flowing through the current sources **44** and **45** which is of course dependent upon the magnitude of the input voltage at input **43**. As the input voltage increases so does the magnitude of the current flow and hence the speed with which the capacitor is charged and discharged.

To make it possible for the oscillator circuit **12** to have the required centre frequency to meet the needs of the overall phase locked loop, one or more additional MOS capacitors as **54** may be provided as shown and connected to the node **53** by way of a respective programmable switch, such as a fuse **55**. Initially, the or each fuse **55** would be closed, but if trimming of the circuit was necessary one or more of the fuses could be blown to provide an open circuit and thereby disconnect the respective capacitor **54** from the node **53**. Clearly, this would vary the time constant of the capactivie circuit and hence vary the frequency of oscillations. Additionally, to enable variation of the current levels in the current sources **44** and **45**, it would be possible to connect additional transistors (not shown) in parallel with the current sources **44** and **45** such that the effective gains of these transistors could be varied. It is envisaged that any such transistors would be connected in circuit by way of programmable switches, such as fuses.

It is intended that the output of the oscillator circuit shown in FIG. **3** be used as a high frequency clock signal, for example for a processor or microcomputer. In these circumstances it is generally necessary to provide at least two clock signals of complementary phase which do not overlap. Thus, the output of the oscillator circuit shown in FIG. **3** could be applied by way of a two phase clock generator (not shown) to the microcomputer **2** (FIG. **1**).

FIG. **4** shows an alternative embodiment of a voltage controlled oscillator circuit **12'** which provides two oscillating output signals which are complementary in phase and which require only a minimum shaping before they can be applied to the microcomputer.

The voltage controlled oscillator circuit **12'** shown in FIG. **4** has an input terminal **70** to which the voltage output from the buffer **16** is applied. The circuit **12'** includes a voltage controlled current source in the form of an N channel transistor **57** whose gate is connected to

the input terminal 70. Thus, the current flowing in the transistor 57 is determined by the magnitude of the voltage applied to the input terminal 70. The source-drain path of the transistor 57 is connected in series with a first series connection of a P channel transistor 58 and an N channel transistor 59 and with a second series connection of a P channel transistor 60 and an N channel transistor 61. It will be appreciated that the current flowing through each pair of transistors 58, 59, and 60, 61 will be determined by that flowing through the N channel current source transistor 57.

The gates of the first pair of transistors 58 and 59 are connected together and to the output of a NAND gate 62. Similarly, the gates of the second pair of transistors 60 and 61 are connected together and to the output of a further NAND gate 63. A first input of each NAND gate is connected to a respective MOS capacitor. Thus, the first input of NAND gate 63 is connected to a node 65 connecting the drain of transistor 58 to the source of transistor 59, the node 65 also being connected to a MOS capacitor 64. The second input of the NAND gate 63 is connected to the output of the NAND gate 62.

Similarly, a first input to the NAND gate 62 is connected to a node 67 at which the transistors 60 and 61 are connected, the node 67 also being connected to a MOS capacitor 66. The second input to the NAND gate 62 is connected to the output of the NAND gate 63. It will also be seen that the output of the NAND gate 63 is connected to a first output terminal 68 whilst the output of the NAND gate 62 is connected to a second output terminal 69.

Consider initially that there is a low level voltage at the output of the NAND gate 62 which is applied to the second input of the NAND gate 63 and by way of the output 69 to the gates of the transistors 58 and 59. The P-channel transistor 58 will therefore conduct and begin to charge the capacitor 64. Initially there will be a low level voltage on the first input to the NAND gate 63.

The high level output of the NAND gate 63 is applied to the second input of the NAND gate 62 and by way of the output 68 to the transistors 60 and 61.

As the capacitor 64 is charged the first input to the NAND gate 63 will become high but the output of the NAND gate 63 will remain high.

The high output at the terminal 68 switches on the N channel transistor 61 and switches OFF the P channel transistor 60 such that the capacitor 66 is discharged by way of the transistor 61 and the current source transistor 57. A low going voltage is therefore applied to the first input to the NAND gate 62 whilst the high voltage is already applied to the second input. As the first input of NAND gate 62 goes from high to low its output switches from low to high such that the transistor 58 is switched OFF and the transistor 59 is switched ON such that discharging of the capacitor 64 is commenced by way of the current source transistor 57.

The high level output of the NAND gate 62 is fed to the second input of the NAND gate 63. As this NAND gate 63 also has a high applied to its first input, its output will go from high to low. The P channel transistor 60 will thereby be switched ON and the N channel transistor 61 will be rendered non-conductive such that charging of the capacitor 66 will be commenced. Of course, once the discharge of the capacitor 64 puts a low on the first input of the NAND gate 63 the output state thereof will change and the state of the NAND gate 62 will similarly be changed.

It will be seen that an oscillating signal will be generated on each of the outputs 68 and 69. The speed of the discharge of the capacitors 64 and 66 is determined by the magnitude of the current flow through the current source transistor 57 and hence upon the magnitude of the input voltage at input 70. Thus, the frequency of the oscillations at each output terminal 68 and 69 is determined by the magnitude of the input voltage.

The capacitor 64 is generally being charged as the capacitor 66 is being discharged and vice versa. Thus, the output signals at terminals 68 and 69 are substantially 180° out of phase. There may be some overlap between the leading edge of one output signal and the trailing edge of the other, but this can be removed if required by shaping one or both of the output waveforms.

The centre frequency of the oscillator 12' can be changed as previously by connecting one or more transistors, as 71 into the circuit by way of respective fuses, as 72.

It will be appreciated that initialisation of the oscillators 12 and 12' shown in FIGS. 3 and 4 may well be necessary. However, as initialisation techniques are well known, details thereof will not be described.

It will be seen from the description given above that the timing apparatus described including the phase locked loop is able to provide high frequency timing signals upon the application of a low frequency clock to the input thereof.

It thus becomes possible to supply a microcomputer incorporating apparatus on the same chip the timing as shown in FIG. 1. The user than needs only to connect the clock input pin 3' to a standard low frequency clock signal, at say 5 MHZ, to obtain operation of the microcomputer at high operating speeds. Thus, it would be envisaged that the timing apparatus would generate timing signals having a frequency, eg, of the order of 40–100 MHZ. Furthermore, the user could use the same low frequency standard clock for a number of or a network of such microcomputers, the individual timing apparatus associated with each microcomputer providing suitable high frequency timing signals for its microcomputer.

Of course, the timing apparatus of the invention is not limited to use with microcomputers, but can be used to provide timing signals for any logic device.

I claim:

1. An integrated circuit device comprising a logic device, a plurality of input pins connected to said logic device, a plurality of output pins connected to said logic device, and a timing apparatus for said logic device having an input connected to one of said input pins for receiving an input clock signal and an output connected to supply an output timing signal to said logic device, wherein both said logic device and said timing apparatus are completely formed on a common single chip, said timing apparatus comprising a phase locked loop arranged to produce said output timing signal whose frequency is a multiple of that of said received input clock signal, wherein said phase locked loop comprises:

comparator means having a first input to which said received input clock signal is applied, a second input, and two outputs on which comparison signals are provided;

a divider having an input connected to receive said output timing signal and an output connected to said second input of said comparator means, said divider being arranged to divide the frequency of

said output timing signal by a predetermined integer;

convertor and filter means connected to receive said comparison signals and arranged to generate a voltage signal whose magnitude is determined by said comparison signals; and

a voltage controlled oscillator arranged to be controlled by said voltage signal to produce said output timing signal at its output, the output of said voltage controlled oscillator being connected to said input of said divider, and wherein the output of said voltage controlled oscillator is also directly connected to said logic device to supply said output timing signal thereto.

2. An integrated circuit device according to claim 1 wherein said comparator means is a phase and frequency comparator and is arranged to produce first and second comparison output signals indicating a difference in either phase or frequency between the input clock signal and the divided output timing signal and the direction of this difference.

3. An integrated circuit device according to claim 2 wherein said convertor and filter means comprises at least one current source arranged to be controlled by said comparison signals and a current reference circuit arranged to determine the magnitude of the current produced by said current source.

4. An integrated circuit device according to claim 3 wherein said convertor and filter means comprises first and second current sources, said first current source being controlled by said first comparison signal, said second current source being controlled by said second comparison signal, each of said first and second current sources comprising a transistor and wherein said current reference circuit includes first and second current mirror transistors, each corresponding to a respective one of said first and second current source transistors, each current mirror transistor being arranged to determine the magnitude of the current produced by its corresponding current source transistor.

5. An integrated circuit device according to claim 4 wherein said current reference circuit is arranged to generate a predetermined reference voltage for determining the current flowing in each of the first and second current mirror transistors and hence in each of the first and second current source transistors.

6. An integrated circuit device according to claim 5 wherein said predetermined reference voltage is generated at a node connectible to the voltage supply by way of a circuit for determining said predetermined reference voltage, said circuit including a plurality of components connectible by programmable switches.

7. An integrated circuit device according to claim 6 wherein said programmable switches are fuses.

8. An integrated circuit device according to claim 1 wherein said convertor and filter means comprises a convertor coupled to receive said comparison signals and to produce a plurality of current pulses whose frequency is determined by said comparison signals, and a filter coupled to receive said current pulses and produce a dc output voltage whose magnitude is determined by said comparison signals, said filter having an input for receiving said current pulses, a MOS capacitor connected to said input, a transistor biased to operate as a resistor connected in series with said capacitor and to ground such that a series RC connection couples said input to ground, and an output connected to said capacitor.

9. An integrated circuit device comprising a logic device, a plurality of input pins connected to said logic device, a plurality of output pins connected to said logic device, and a timing apparatus for said logic device having an input connected to one of said input pins for receiving an input clock signal and an output connected to supply an output timing signal to said logic device, wherein both said logic device and said timing apparatus are completely formed on a common single chip, said timing apparatus comprising a phase locked loop arranged to produce said output timing signal whose frequency is a multiple of that of said received input clock signal, wherein said phase locked loop consists essentially of:

a comparator having a first input to which said received input clock signal is applied, a second input connected to the output of a divider arranged to divide the frequency of the output timing signal by a predetermined integer, and two outputs on which comparison signals are produced;

filter means coupled to receive current pulses derived from said comparison signals and to produce a dc output voltage whose magnitude is determined by said comparison signals; and

a voltage controlled oscillator arranged to be controlled by said dc output voltage to produce said output timing signal,

wherein said filter comprises an input for receiving said current pulses, a MOS capacitor connected to said input, a transistor biased to operate as a resistor connected in series with said capacitor and to ground such that a series RC connection couples said input to ground, and an output connected to said capacitor.

10. An integrated circuit device according to claim 9, wherein said filter means further comprises one or more transistor means connectible by way of programmable switches whereby the parameters of the filter may be varied.

11. An integrated circuit device according to claim 10, wherein said programmable switches comprise fuses.

12. An integrated circuit device according to claim 10, wherein said comparator is a phase and frequency comparator and is arranged to produce first and second comparison output signals indicating a difference in either phase or frequency between the input clock signal and the divided output timing signal and the direction of this difference.

13. An integrated circuit device according to claim 12, wherein said phase locked loop further includes a convertor arranged to receive said comparison signals and to produce a plurality of current pulses whose frequency is determined by said comparison signals, said filter means being coupled to receive said current pulses, and wherein said convertor comprises first and second current source transistors controlled by said comparison signals, and first and second current mirror transistors each corresponding to a respective one of said first and second current source transistors, each current mirror transistor being arranged to determine the magnitude of the current produced by its corresponding current source transistor.

14. An integrated circuit device according to claim 1 or 9 wherein said voltage controlled oscillator includes at least one capacitive circuit comprising a current source transistor coupled to a MOS capacitor.

15. An integrated circuit device comprising a logic device, a plurality of input pins connected to said logic device, a plurality of output pins connected to said logic device, and a timing apparatus for said logic device having an input connected to one of said input pins for receiving an input clock signal and an output connected to supply an output timing signal to said logic device, wherein both said logic device and said timing apparatus are completely formed on a common single chip, said timing apparatus comprising a phase locked loop arranged to produce said output timing signal whose frequency is a multiple of that of said received input clock signal, wherein said phase locked loop consists essentially of:

a comparator having a first input to which said received input clock signal is applied, a second input connected to the output of a divider arranged to divide the frequency of the output timing signal by a predetermined integer, and two outputs on which comparison signals are produced;

filter means coupled to receive pulses derived from said comparison signals and to produce a dc output voltage whose magnitude is determined by said comparison signals; and

a voltage controlled oscillator arranged to be controlled by said dc output signal to produce said output timing signal, wherein said voltage controlled oscillator comprises an input to receive said dc output voltage, an output, and switchable means for producing oscillations at a frequency determined by the magnitude of said output voltage, said voltage controlled oscillator further including at least one capacitive circuit comprising a current source transistor coupled to a MOS capacitor.

16. An integrated circuit device according to claim 15 further comprising means for varying the time constant of said capacitive circuit whereby the center frequency of said voltage controlled oscillator may be varied.

17. An integrated circuit device according to claim 16 wherein said means for varying the time constant of the capacitive circuit includes at least one further MOS capacitor connected to said capacitive circuit by way of programmable switches.

18. An integrated circuit device according to claim 17 wherein said means for varying the time constant of the capacitive circuit includes one or more transistor means connectible in parallel with said current source transistor by programmable switches.

19. An integrated circuit device according to claim 17 or 18, wherein said programmable switches are fuses.

20. An integrated circuit device according to claim 15 wherein said switchable means of the voltage controlled oscillator comprises two switching transistors, the current path of each of said swiitching transistors being connected to a node, and a Schmitt trigger having an input connected to said node and an output forming the output of said voltage controlled oscillator, the output of said Schmitt trigger also being coupled to the gates of said switching transistors, and wherein said MOS capacitor is connected to said node,

said voltage controlled oscillator further comprising two current source transistors, each being connected to a respective one of said switching transistors, and two current mirror transistors, each current mirror transistor being connected to the input of the voltage controlled oscillator and to a respective one of said current source transistors such that the current flowing in each current source transistor is determined by the magnitude of said dc output voltage.

21. An integrated circuit device according to claim 15, wherein the switchable means of the voltage controlled oscillator comprises:

first and second pairs of switching transistors, the current paths of the two transistors in each pair being connected together at a node, and

two NAND gates, each NAND gate having first and second inputs and an output, the first input of each NAND gate being connected to the said node between a respective one of said pairs of switching transistors, and the second input of

each NAND gate being connected to the output of the other NAND gate, the output of each NAND gate also being connected to the gates of the transistors of the pair of switching transistors other than the pair to which its first input is connected,

the voltage controlled oscillator further comprising two MOS capacitors, each MOS capacitor being connected to the node of a respective pair of switching transistors, said current source transistor being coupled to each of said MOS capacitors by way of the respective pair of switching transistors, said current source transistor being connected to the input of the voltage controlled oscillator and to said pairs of switching transistors such that the current flowing in said switching transistors is determined by the magnitude of said dc output voltage.

22. An integrated circuit device as claimed in claim 15, wherein said logic device is a microcomputer.

23. A method of supplying timing signals to an integrated circuit logic device employing a timing apparatus formed together with the logic device on a common single chip, the method comprising the steps of:

applying a low frequency clock signal to an input of said timing apparatus, the timing apparatus being arranged to generate a high frequency timing signal at its output having a frequency which is a multiple of that of said clock signal,

dividing the frequency of said high frequency timing signal by a predetermined integer,

comparing the divided frequency with the frequency of the clock signal,

generating an increase or a decrease comparison signal where the clock signal frequency is respectively greater than or less than said divided frequency,

generating a dc voltage whose magnitude is determined by said comparison signals, and

generating said high frequency timing signal at the output of a voltage controlled oscillator controlled by said dc voltage, wherein said high frequency timing signal at the output of said voltage controlled oscillator is connected directly to said logic device to form the timing signal therefor.

24. A method according to claim 23 further comprising determining the operating speed of said logic device, and selecting said predetermined integer by which said high frequency timing signal is divided such that the frequency of said high frequency timing signal is matched to the said operating speed.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/008,227	09/21/2006	6598148	0081-011D3C1X1	6167

40972 7590 02/12/2008

HENNEMAN & ASSOCIATES, PLC
714 W. MICHIGAN AVENUE
THREE RIVERS, MI 49093

EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 02/12/2008

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

DO NOT USE IN PALM PRINTER

(THIRD PARTY REQUESTER'S CORRESPONDENCE ADDRESS)

FOLEY AND LARDNER LLP
3000 K STREET NW
WASHINGTON, DC 20007

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/008,227*.

PATENT NO. *6598148*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Ex Parte Reexamination Interview Summary	Control No.	Patent Under Reexamination	
	90/008,227	6598148	
	Examiner	Art Unit	
	Joseph R. Pokrzywa	3992	

All participants (USPTO personnel, patent owner, patent owner's representative):

(1) *Joseph R. Pokrzywa*

(2) *Roland Foster; Sue Lao*

(3) *Larry Henneman*

(4) *Charles Moore*

Date of Interview: *12 February 2008*

Type: a)☐ Telephonic b)☐ Video Conference
c)☒ Personal (copy given to: 1)☐ patent owner 2)☒ patent owner's representative)

Exhibit shown or demonstration conducted: d)☒ Yes e)☐ No.
If Yes, brief description: *The patent owner's representative's e-mail message of the issues to be discussed at the interview*

Agreement with respect to the claims f)☐ was reached. g)☐ was not reached. h)☐ N/A.
Any other agreement(s) are set forth below under "Description of the general nature of what was agreed to..."

Claim(s) discussed: *4 and 8*.

Identification of prior art discussed: *Talbot (U.S. Pat. 4,689,581 and May (European Patent Publication EP 0 113 516)*.

Description of the general nature of what was agreed to if an agreement was reached, or any other comments:
See Continuation Sheet.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims patentable, if available, must be attached. Also, where no copy of the amendments that would render the claims patentable is available, a summary thereof must be attached.)

A FORMAL WRITTEN RESPONSE TO THE LAST OFFICE ACTION MUST INCLUDE PATENT OWNER'S STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. (See MPEP § 2281). IF A RESPONSE TO THE LAST OFFICE ACTION HAS ALREADY BEEN FILED, THEN PATENT OWNER IS GIVEN **ONE MONTH** FROM THIS INTERVIEW DATE TO PROVIDE THE MANDATORY STATEMENT OF THE SUBSTANCE OF THE INTERVIEW (37 CFR 1.560(b)). THE REQUIREMENT FOR PATENT OWNER'S STATEMENT CAN NOT BE WAIVED. **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).**

JOSEPH R POKRZYWA
PRIMARY EXAMINER
CRU - AU 3992

cc: Requester (if third party requester)

Examiner's signature, if required

Continuation Sheet (PTOL-474) **Reexam Control No. 90/008,227**

Continuation of Description of the general nature of what was agreed to if an agreement was reached, or any other comments:

Discussed differences in the prior art and the claimed invention. Particularly, the patent owner argued that the references failed to teach of the limitation requiring "said memory further occupying a majority of the total area of said single substrate". The patent owner further pointed out that the reference of May, noted above, describes that the memory can be the largest and densest component on the chip, but this is different than being the "majority of the total area",

Continuing, the patent owner further argued that the reference of Talbot does not teach of a "ring oscillator". The patent owner discussed features of a ring oscillator, such as being non-controllable, and being variable based on the environment. The patent owner argued that these features distinguish over what Talbot teaches. The examiner will reconsider the current rejection based on a forthcoming response, which will include arguments similar to what was discussed.

Joseph R. Pokrzywa
Primary Examiner
Central Reexamination Unit 3992

#15

PATENT

NANO-001/05US
N0765-2008

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on February 6, 1998.

Date: 2/6/98 By: Patricia K. Parry
Patricia K. Parry

2/20/98

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	Examiner: D. Eng
Charles H. Moore et al.	Art Unit: 2784
Serial No. 08/484,918	
Filed: June 7, 1995	AMENDMENT
For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK	Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Amendment is being submitted in response to the Office Action dated October 16, 1997 in the above-identified patent application.

IN THE CLAIMS

Please amend claims 19, 65, 73 and 78 as follows:

Sub 7

19(Three Times Amended). A microprocessor system, comprising a single integrated circuit including a central processing unit and [a] an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit.

Sub 72

65(Three Times Amended). In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:

providing [a] an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor; and

using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock.

Sub 73

73(Three Times Amended). A microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation.

Sub 74

78(Twice Amended). In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon [a] an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing [a] an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors; and

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way

E4

relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate.

REMARKS

Claims 19-21, 65-67 and 72-79 were rejected under 35 U.S.C. § 103 as unpatentable over Magar, U.S. Patent 4,503,500, in view of newly cited Pelgrom et al., U.S. Patent 4,627,082. In response, the independent claims have been rewritten to specify that the entire ring oscillator variable speed system clock, variable speed clock or oscillator be provided in the integrated circuit, in order to sharpen the distinction over the prior art. Because the prior art does not provide an entire ring oscillator variable speed system clock, variable speed clock or oscillator in the integrated circuit, in that the prior art circuits require an external crystal, the prior art fails to teach or suggest the invention as now claimed. This rejection is believed to be overcome by these changes to the claims and these remarks.

Shortly before this Office Action was mailed, Mr. George Shaw, the Assignee's technical representative, and the undersigned attorney had a phone interview with the Examiner regarding this and another of Assignee's cases. Technical distinctions of the present case over the Magar reference previously cited were discussed, as well as the benefits of the invention. Below is recited the pertinent points of that discussion, as well as rebuttal to the new Pelgrom reference.

First, the Examiner states "Pelgrom teaches that electronic components would exhibit same characteristics if they are manufactured by the same process technology", and applicant agrees that this is well known in the art. The Examiner states that, "Since Pelgrom's [Magar's?] microprocessor is made of electronic components, it would have obvious, from the teaching of Pelgrom, to a person of ordinary skill in the art to have the components of Magar' microprocessor and clock (oscillator) make of the same process for ensuring processing frequency of the cpu to track the clock rate in response to the parameter variations." Applicant agrees that the processing frequency capability of the CPU would track the clock rate capability of the clock generator, as this is controlled by the laws of physics on which the Pelgrom reference is based. However, there would be no "tracking" of the clock rate produced by the Magar clock generator, because the entire circuit is not provided on the integrated circuit. Magar's clock generator relies on an external crystal connected to terminals X1 and X2 to oscillate, as is conventional in microprocessor designs. It is not an entire oscillator in itself. And with the crystal, the clock rate generated is also conventional in that it is at a fixed, not a variable, frequency. The Magar clock is comparable in operation to the conventional crystal clock 434 depicted in Fig. 17 of the present application for controlling the I/O interface at a fixed rate frequency, and not at all like the clock on which the claims are based, as has been previously stated.

The Examiner also states that "applicants contend that Magar's clock is external to the IC." This is not the case. The "clock gen" part of the oscillator circuit is clearly on the IC, but not the crystal. Applicants note that the crystal is external, connected to X1 and X2, as Magar cites at column 15, lines 26-27,

"The chip 10 includes a clock generator 17 which has two external pins X1 and X2 to which a crystal (or external generator) is connected."

Thus while most of Magar's clock (generator) circuitry is on the IC, the entire oscillator, which because it requires an external crystal, is not.

"The Examiner further states that applicants imply a "correspondence" in application between Applicant's clock 434 and Magar's clock. This is not the case. Applicants only state that the two clocks are "of the same general type" or are "equivalent" at the circuit level, in that they both use an external crystal to fix the clock rate. They are both of conventional design and not the subject of the claims in the instant case. Clearly, either type could be used to drive a CPU, as Magar depicts the conventional case and Applicant depicts a unique design which provides a variable clock frequency or rate.

Applicant's prior comments apparently did not make clear the distinction between an oscillator and a clock as it applies to the Magar reference. As a self-contained on-chip circuit, Magar's clock gen is distinguished from an oscillator in at least that it lacks the crystal or external generator that it requires. Thus Magar's circuit is not an entirely on-chip oscillator as contemplated in the present case, it is only a clock.

As mentioned in Applicant's previous remarks, the term clock is sometimes used interchangeably with oscillator, even inappropriately, leading to confusion. And, adding to the confusion, in the instant case, 430 is both an oscillator and a clock in the conventional senses. It is an oscillator in that it oscillates without external components (unlike the Magar reference). An example of such an oscillator circuit which does not utililze external components is given in Fig. 18 of the present application. It is also a clock in Magar reference sense in that it produces the various required timing signals needed of the CPU. The signals PHASE 0, PHASE 1, PHASE 2, and PHASE 3 in Applicant's Fig 18 are synonymous with Q1, Q2, Q3, and Q4 depicted in Magar Fig. 2a. The essential difference is that the frequency or rate of the PHASE 0, PHASE 1, PHASE 2, and PHASE 3 signals is determined by the processing and/or operating parameters of the integrated circuit containing the Fig. 18 circuit, while the frequency or rate of the Q1, Q2, Q3, and Q4 signals depicted in Magar Fig. 2a are determined by the fixed frequency of the external crystal connected to the circuit portion outputting the Q1, Q2, Q3, and Q4 signals shown in Magar Fig. 2a.

To summarize, the Pelgrom reference teaches well known art as one of the fundamental principles on which IC are designed. If components did not vary in a similar manner circuit performance could not be predicted and ICs could not be designed. This does not negate

patentability in the present case because it is not the fundamental principle that is claimed but the combination in light of the fundamental principle of enumerated heretofore uncombined circuits to produce a result not obtained with the prior art that is the subject of the claims in the instant case. The Magar teaching is well known in the art as a conventional crystal controlled oscillator. It is specifically distinguished from the instant case in that it is both fixed-frequency (being crystal based) and requires an external crystal or external frequency generator.

Based on the above changes to the claims and remarks, the rejection under 35 USC § 103 is believed to be overcome. All of the claims in the application are believed to be patentable over the prior art. This application is believed to be in condition for allowance, and allowance is solicited.

Respectfully submitted,

COOLEY GODWARD LLP

Willis E. Higgins
Reg. No. 23,025

Five Palo Alto Square
Palo Alto, CA 94306-2155
Telephone: (650) 843-5145

NANO-001/05US
N0765-2008

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on July 3, 1997.

Date: 7/3/97 By: Patricia K. Parry
Patricia K. Parry

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	Examiner: D. Eng
Charles H. Moore et al.	Art Unit: 2315
Serial No. 08/484,918	
Filed: June 7, 1995	AMENDMENT
For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK	Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Amendment is being submitted in response to the Office Action dated April 3, 1997 in the above-identified patent application.

IN THE CLAIMS

Please amend claim 73 as follows:

73(Twice Amended). A microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and [including] being constructed of a second plurality of electronic devices, thus varying the [operating characteristics] processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of [transistors] electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said

integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation.

REMARKS

The above changes to the language of claim 73 clarify that claim and eliminate an inadvertent lack of antecedent basis problem in the former wording of the claim.

Claims 19-21, 65-67 and 72-79 were rejected under 35 U.S.C. § 103 as unpatentable over Magar, U.S. Patent 4,503,500. Shortly before issuing the Office Action, the Examiner had called to indicate that certain claims were allowable over the prior art, but when the undersigned attorney returned the Examiner's call, it was indicated that new prior art had been found and that a new action would be forthcoming. It is assumed that the Magar reference relied on is that new prior art. A review of the Magar reference shows that it is apparently no more pertinent than prior art acknowledged in the application, in that the clock disclosed in the Magar reference is in fact driven by a fixed frequency crystal, which is external to the Magar integrated circuit.

The clock gen circuit shown at the lower right hand edge of Fig. 2a in the Magar patent is of the same general type as shown at 434 in Fig. 17 of the present application, but depicted differently in that it shows the clock gen circuit portion which is on the semiconductor substrate, while Fig. 17 shows the external crystal at 434, connected to I/O interface 432 in the present invention. The crystal clock 434 is thus used in the invention for synchronizing I/O timing with the outside world, while the ring counter variable speed clock 430 also shown in Figure 17 is used for generating on-chip clock signals. The clock 430 is an example of the oscillator recited in the claims, the clock rate of which varies in the same way as a function of one or more device parameters associated with the integrated circuit substrate.

The definitive statement that the clock gen circuit in Fig. 2a in the Magar patent is equivalent to the "conventional crystal clock" 434 in Fig. 17 of the present application is at col. 15, lines 26-41 of Magar:

> "The chip 10 includes a clock generator 17 which has two external pins X1 and X2 to which a crystal (or external generator) is connected. The basic crystal frequency is up to 20 MHz and is represented by a clock 0 of Fig. 3a. This clock 0 has a period of 50 ns, minimum, and is used to generate for quarter-cycle clocks Q1, Q2, Q3 and Q4, seen in FIGS. 3b-3e, providing the basic internal timing for the microcomputer chip 10. A set of four quarter cycle clocks Q1 to Q4 defines one machine state of time of 200 ns., minimum; the states are referred to as S0, S1, S2 in FIG 3. The clock generator produces an output CLKOUT, Fig. 3f, on one of the control bus lines 13. CLKOUT has the same period as

Q1, but 50% duty cycle and beginning at the midpoint of Q1. This output is used for timing or synchronizing external components of the system of FIG. 1."

This description in Magar should be contrasted with the following detailed description of an embodiment of the present invention, as shown in Fig. 17, at explained at page 32, lines 3-29:

"Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor 50 provides a dual-clock scheme as shown in Figure 17, with the CPU 70 operating asynchronously to I/O interface 432 forming part of memory controller 118 (Figure 2) and the I/O interface 432 operating synchronously with the external world of memory and I/O devices. The CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor 50 for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface 432, speed of which is controlled by a conventional crystal clock 434. The interface 432 processes requests for memory accesses from the microprocessor 50 and acknowledges the presence of I/O data. The microprocessor 50 fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. By decoupling the variable speed of the CPU 70 from the fixed speed of the I/O interface 432, optimum performance can be achieved by each. Recoupling between the CPU 70 and the interface 432 is accomplished with handshake signals on lines 436, with data/addresses passing on bus 90, 136."

From these two quotations, it is clear that the element in Fig. 17 missing from Fig. 2a in Magar is the ring counter variable speed clock 430, and that Magar is merely representative of the "most microprocessors" acknowledged as prior art in the above description from the present application, which prior art microprocessors use a "conventional crystal clock." Because the variable speed clock is a primary point of departure from the prior art, independent claims 19, 65, 73 and 78 all recite a system including a variable speed clock or a method including using a variable speed clock. In light of the prior art, of which Magar is a good example, Applicants are entitled to claims of this scope. Dependent claims 20, 66, 74 and 79 further recite a second clock, exemplified by the crystal clock 434 in Fig. 17.

Contrary to the Examiner's assertion in the rejection that "one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock vary together due to manufacturing variation, operating voltage and temperature of the IC", one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock *do not* vary together due to manufacturing variation, operating voltage and temperature of the IC in the Magar microprocessor, as taught in the above quotation from the reference. This is simply because the Magar microprocessor clock is

frequency controlled by a crystal which is also external to the microprocessor. Crystals are by design fixed-frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The Magar microprocessor in no way contemplates a variable speed clock as claimed.

In making the rejection based on Magar, the examiner appears to be confusing the multiple uses and meanings of the technical term "clock." A clock is simply an electrical pulse relative to which events take place. Conventionally, a CPU is driven by a clock that is generated by an crystal. The crystal might be connected directly to two pins on the CPU, as in Magar, and be caused to oscillate by circuitry contained in the CPU with the aid of possibly other external components. Alternatively, the crystal may be contained in a package with the oscillation circuitry, the packaged component thus called an oscillator, and connected to one pin on the CPU as in Edwards et al., U.S. Patent 4,680,698.

While an oscillator may be a clock, a clock is not usually an oscillator. An oscillator must exist someplace in the circuit from which a periodic clock is derived. In both cases, the crystal (or the entire oscillator in the second case) is external to the CPU, and the output of the oscillator circuitry is a "clock." This clock is typically modified to produce additional required clock signals for the system. The many clock signals are sometimes created by circuitry called a "clock generator." For example, see Magar, Fig. 2a. The "clock gen" connects to a crystal at external pins X1 and X2 and generates clock signals for the system Q1, Q2, Q3, Q4 and CLKOUT. Other cited reference have similar examples, see Palmer, U.S. Patent 4,338,675, Fig. 1, item 24; Pohlman et al., U.S. Patent 4, 112,490 Fig. 1, item 22. All these systems operate at a frequency determined by the external crystal. The single, fixed, oscillation frequency of the crystal is determined by how the device is manufactured, i.e., how the crystal is cut and trimmed, and other factors. Crystals are used precisely for this purpose; they oscillate at a given frequency within a tolerance determined by their manufacture. Because of the cutting and trimming required, and that the crystal slice is typically suspended by two wires to allow it to freely oscillate, crystal oscillators have never, to Applicants' knowledge, been fabricated on a single silicon substrate with a CPU, for instance. Even if they were, as previously mentioned, crystals are by design fixed-frequency devices whose oscillation frequency is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The oscillation frequency of a crystal on the same substrate with the microprocessor would inherently not vary due to variations in manufacturing, operating voltage and temperature in the same way as the frequency capability of the microprocessor on the same underlying substrate, as claimed.

Note that the term clock can refer to many different signals since the definition is broad, and that it can also refer to the oscillator that is required to generate the clock. While a crystal-controlled oscillator typically operates at a single speed, the circuitry around the crystal may be

designed so that the output of the entire oscillator circuit can be varied. Many mechanisms can be used to control the output of a variable-frequency oscillator, including manual inputs, program-controlled inputs, temperature sensors, or other devices. Non-crystal controlled oscillators are also possible, and when they are designed as variable-frequency oscillators they are typically also controlled by manual inputs, program-controlled inputs, temperature sensors and other devices.

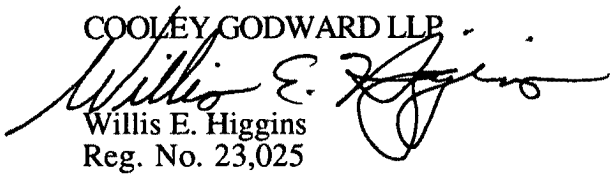
The present invention is unique in that it applies, and can only apply, in the circumstance where the oscillator or variable speed clock is fabricated on the same substrate as the driven device. The example given is a non-crystal controlled circuit, a ring oscillator. A ring oscillator will oscillate at a frequency determined by its fabrication and design and the operating environment. Thus in this example, the user designs the ring oscillator (clock) to oscillate at a frequency appropriate for the driven device when both the oscillator and the device are under specified fabrication and environmental parameters. Crucial to the present invention is that since both the oscillator or variable speed clock and driven device are on the same substrate, when the fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together. This differs from all cited references in that the oscillator or variable speed clock and the driven device are on the same substrate, and that the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so. Like the cited references, the driven device might additionally contain clock generation circuitry to produce variations on the clock output of the oscillator or variable speed clock for the other circuitry on the device.

The remaining Bennett et al., Brantingham, Pollack, Gruner et al.and Suzuki et al. references, cited but not applied in a rejection, have been reviewed and found not pertinent to the invention as claimed.

Based on the above remarks, the rejection under 35 USC § 103 is believed to be overcome. All of the claims in the application are believed to be patentable over the prior art. This application is believed to be in condition for allowance, and allowance is solicited.

Respectfully submitted,

COOLEY GODWARD LLP



Willis E. Higgins
Reg. No. 23,025

Five Palo Alto Square
Palo Alto, CA 94306-2155
Telephone: (415) 843-5145

clock speed varying in the same way as variations in the operating characteristics of the electronic devices making up the microprocessor. This allows the microprocessor to operate at its fastest safe operating speed, given its manufacturing process or changes in its operating temperature or voltage. In contrast, prior art microprocessor systems are given a rated speed based on possible worst case operating conditions and an external clock is used to drive them no faster than the rated speed. Under other than worst case operating conditions, the prior art microprocessors are actually capable of operating at a faster clock speed than their rated speed.

The above changes to the claims have been made to bring out the above distinction over the prior art more clearly. It is believed that they overcome the rejection of claims 19-21, 65-67 and 71-79 under 35 USC § 112, define statutory subject matter, i.e, a system implemented as a single integrated circuit having defined characteristics or a process, as well as distinguishing over the prior art of record.

In the rejection under 35 USC § 103, the Examiner contends that the Sheets reference "clearly indicates in lines 46-48 of column 2 that the system 100 shown in Figure 1 is fabricated *on a single chip* using MOS technology." Specific issue is taken with the inclusion of the italicized language in this characterization of the reference. Sheets does not say that the system 100 is on a single chip, only that it is implemented in MOS technology. At column 5, lines 15-17, a specific example of the Motorola 68000 microprocessor is given. That microprocessor is driven by an external clock that provides a clock signal to a designated pin of the microprocessor integrated circuit package. Applicants are aware of no prior art teaching or suggesting a variable speed oscillator in the same integrated circuit with a microprocessor and clocking the microprocessor with a clock speed that varies correspondingly with changes in operating characteristics of electronic devices making up the microprocessor, as a result of being in the same integrated circuit as the microprocessor, as claimed. Even if the Examiner is correct that the variable clock in Sheets is in the same integrated circuit as the microprocessor of system 100, that still does not give the claimed subject matter. In Sheets, a command input is required to change the clock speed. In the present invention, the clock speed varies correspondingly to variations in operating parameters of the electronic devices of the microprocessor because both the variable speed clock and the microprocessor are fabricated together in the same integrated circuit. No command input is necessary to change the clock frequency. The rejection under 35 USC § 103 is believed to be overcome.

PATENT

NANO-001/05US
N0765-2008

I hereby certify that this paper correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Date: 4/19/96 By: Felicia Walker

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	Examiner: D. Eng
Charles H. Moore et al.	Art Unit: 2315
Serial No. 08/484,918	
Filed: June 7, 1995	AMENDMENT
For: HIGH PERFORMANCE, LOW COST MICROPROCESSOR	Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Amendment is being submitted in response to the first Office Action in the above-identified patent application.

IN THE SPECIFICATION

At page 1, line 1, please change the title from "HIGH PERFORMANCE, LOW COST MICROPROCESSOR" to --HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK--.

110 JF 04/18/96 08484918 1 202 39.00 CK

21092053

[which comprises fabricating] providing a ring [counter] oscillator system clock having a plurality of transistors within the integrated circuit, said plurality of transistors having operating characteristics disposed to vary similarly to operating characteristics of transistors included within the microprocessor; [and the microprocessor each having a plurality of transistors having operating characteristics which vary in the same way with variations in their fabrication,] and

using the ring [counter] oscillator system clock for clocking the microprocessor, said central processing unit operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock.

66(Amended). The method of Claim 65 additionally comprising the steps of:

providing an input/output interface for the microprocessor integrated circuit, [and]

clocking the input/output interface with a second clock independent of the ring [counter] oscillator system clock, and

buffering information within said input/output interface received from said microprocessor integrated circuit.

Please add the following new claims 71-79:

71. The microprocessor system of claim 20 further including system memory coupled to said input/output interface, said system memory being synchronized to said second clock and operating synchronously with respect to said ring oscillator variable speed system clock.

72. The method of claim 65 further including the steps of:

transferring information to and from said microprocessor in synchrony with said ring oscillator system clock, and

buffering said information to facilitate transfer of said information to and from system memory synchronously with respect to said ring oscillator system clock.

73. A microprocessor system comprising:

a central processing unit disposed upon a substrate, said central processing unit operating at a processing frequency and including a first plurality of transistors;

an oscillator disposed upon said substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and including a second plurality of transistors designed such that operating characteristics of said first plurality and said second plurality of transistors vary in the same way as a function of parameter variation in one or more operational parameters associated with said substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation.//

74. The microprocessor system of claim 73 wherein said one or more parameters are included within the set consisting of: operating temperature of said substrate, operating voltage of said substrate, and fabrication process of said substrate.

75. The microprocessor system of claim 73 further comprising:

an input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, address and data with said central processing unit;

an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

76. The microprocessor system of claim 75 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.

77. The microprocessor system of claim 73 wherein said oscillator comprises a ring oscillator.

78. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon a substrate, said central processing unit including a first plurality of transistors and being operative at a processing frequency;

clocking said central processing unit at a clock rate using an oscillator disposed upon said substrate, said oscillator being provided so as to include a second plurality of transistors with said central processing unit being clocked by said oscillator at a variable frequency dependent upon variation in one or more operational parameters associated with said substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more operational parameters associated with said substrate.

79. The method of claim 78 further comprising the steps of:

connecting an input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, address and data between said input/output interface and said central processing unit;

clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

REMARKS

This amendment responds to the first office action. Claims 19-20 and 65-66 have been amended, and new claims 71-79 have been added.

The Examiner has requested that applicants update the status of the parent application. Applicants note that the parent application Serial No. 07/389,334 has issued as U.S. Pat. No. 5,440,749. Also pursuant to the Examiner's request, a new title and new abstract more aptly descriptive of the invention have been provided.

The Examiner has rejected claims 19-21 and 65-67 under 35 U.S.C. § 112 as being indefinite. With respect to the apparatus claims, the Examiner asserted that there exists no functional relationship and interconnection between the claimed components. Similarly, the Examiner asserted that a functional relationship does not exist between the steps of the method claims, and that it is unclear what the steps try to accomplish.

Applicants note that the present invention is directed to a microprocessor system including a central processing unit and a ring oscillator variable speed system clock connected thereto. In accordance with the claimed invention, the central processing unit and the ring oscillator variable speed system clock are provided in a single integrated circuit. This allows, for example, the central processing unit to track variations in the speed of the ring oscillator variable speed system clock, since the elements of each are disposed in the same integrated circuit. By this amendment the term "ring counter" has been replaced with "ring oscillator", in order to more particularly identify the ring oscillator (FIG. 18) incorporated within a preferred implementation of the microprocessor system of the invention.

Although applicants submit that the "functional relationship" between the claimed central processing unit and system clock connected thereto is inherently clear, the apparatus and method claims have been amended in an effort to accommodate the Examiner's concerns with respect to 35 U.S.C. §112. For example, claim 19 now recites a "functional relationship" in that it is made explicit that the ring oscillator variable speed system clock is disposed to clock the central processing unit. Moreover, the central processing unit and ring oscillator variable speed system clock are described as "each including a plurality of electronic devices of like type". This allows the central processing unit to operate at a

variable processing frequency which depends upon a variable speed of the ring oscillator variable speed system clock. See, for example, the specification at page 31, line 33 to page 32, line 1:

> By deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast. For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor 50 will operate slower than normal. Since the microprocessor 50 *ring oscillator clock 430 is made from the same transistors on the same die as the latches and gates*, it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.

Method claim 65 has been similarly amended, and now recites the step of:

> fabricating a ring oscillator system clock having a plurality of transistors, said plurality of transistors having operating characteristics disposed to vary similarly to operating characteristics of transistors included within the microprocessor ... .

The method claims thus now prescribe a technique for clocking a microprocessor using a ring oscillator system clock comprised of transistors having similar operating characteristics as those within the microprocessor. This advantageously allows the processing frequency of the microprocessor to track the clock rate of the ring oscillator system clock.

The Examiner has rejected claims 19 and 65 under 35 U.S.C. § 103 as being unpatentable over Sheets. The Examiner stated that Sheets teaches a microprocessor system having a microprocessor and a variable speed clock generator. Although admitting that Sheets does not disclose that his clock is implemented using a ring oscillator, the Examiner opined that a "counter is a basis component of [a] clock generator". It was further asserted that choosing the counter to be of the ring type is merely a matter of design choice.

Applicants again observe that the present invention is directed to a system and method for clocking a central processing unit disposed *within the same integrated circuit* as a ring oscillator variable speed system clock. This allows, for example, the central processing unit to track variations in the speed of the ring oscillator variable speed system clock, since the elements of each are disposed in the same integrated circuit. That is, the operational speed of the microprocessor and ring oscillator clock are designed to vary similarly as a function of variation in temperature, processing and other parameters affecting circuit performance.

The system of Sheets effects microprocessor clocking in a way which is entirely dissimilar from that of the present invention, and in fact teaches away from Applicants' clocking scheme. In particular, Sheets describes the use of discrete, commercially available microprocessor chips, e.g., the Motorola 68000 (col. 5, line 16), driven by a separate clock (VCO 12 of FIG. 1). As is well known, such microprocessor chips include terminals or pins, such as the CLK and INT terminals of microprocessor (FIG. 1), for receiving inputs from external devices like the VCO 12 and fixed oscillator 103. Because the VCO 12 is not integral with the microprocessor 101, Sheets has proposed a technique for adjusting the frequency of VCO 12 in accordance with a desired operating frequency of the microprocessor 101. Specifically, a digital word indicative of this desired operating frequency is written by microprocessor 101 to VCO 12 by way of data bus 104 as a means of adjusting clock frequency.

The present invention does not similarly rely upon provision of frequency control information to an external clock, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, since the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance. Sheets' system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.

Although the foregoing clearly indicates the existence of a patentable distinction between the system of Sheets and the present invention, claims 19 and 65 have nonetheless been amended to advance prosecution of the application. Specifically, claims 19 and 65 now explicitly recite that the ring oscillator and microprocessor are provided within the same integrated circuit. Moreover, these claims further state that the plurality of transistors included within the ring oscillator clock have operating characteristics which vary similarly to operating characteristics of transistors included within the microprocessor, thereby enabling the processing frequency of the microprocessor to track the speed of the ring oscillator clock:

> ...The CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process.
> (page 32, lines 10-13)

Neither of these aspects of the present invention are suggested by Sheets. As discussed above, Sheets describes the use of commercially available microprocessor chips, and depicts the microprocessor 101 as being coupled to a separate clock (i.e, VCO 12) by way of a data bus 104 and address bus 105. Moreover, the VCO 12 clearly is not comprised of transistors having operating characteristics disposed to vary similarly to those of transistors within the microprocessor 101. Rather, the VCO 12 is seen to be comprised of an LC oscillator (col. 3, line 58 and FIG. 6), which clearly is not adapted to mimic variation in the speed of transistors within the microprocessor 101. Accordingly, applicant respectfully submits that amended claims 19 and 65 are patentable over Sheets, and requests that the rejection thereof under 35 U.S.C. § 103 be withdrawn.

Since Schaire does not supplement the lack of teaching within Sheets with respect to amended claims 19 and 65, it is also respectfully submitted that pending claims 20-21 and 66-67 are patentable over Sheets in view of Schaire. Further with regard to pending claims 20 and 66, it is observed that Schaire provides no indication that bus interface unit 10 is clocked by a signal from a clock different from that used to clock the host microprocessor. That is, the origin of high-speed clock signal 230 (FIG. 1) provided to bus interface unit 10 does not appear to be described. Hence, Schaire fails to teach the claimed provision of separate, independent clock signals to an input/output interface buffer and microprocessor. Accordingly, applicant respectfully requests that the outstanding rejection of claims 20-21 and 66-67 under 35 U.S.C. § 103 be withdrawn.

By this amendment new claims 71-79 have also been added to more particularly identify the invention which appears to be available for protection. In this regard new claims 71-72 point out that information is transferred to and from the microprocessor in synchrony with the ring oscillator system clock, and that this information is buffered to facilitate transfer thereof to and from system memory synchronously with respect to the ring oscillator system clock. New claims 73-79 explicitly recite that the central processing unit and ring oscillator include first and second pluralities of transistors, respectively, and that the

operating characteristics of these transistors vary in the same way as a function of variation in operational parameters (e.g., operating temperature) of the substrate. This advantageously allows a processing frequency of the central processing unit to track a clock rate of the ring oscillator as a function of substrate parameter variation.

Accordingly, in view of the above remarks, it is submitted that this application is now ready for allowance. Early notice to this effect is solicited.

If in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned at (415) 843-5000.

Respectfully submitted,

COOLEY GODWARD CASTRO
HUDDLESON & TATUM

By: _____
Willis E. Higgins
Reg. No. 23,025

Cooley Godward Castro
Huddleson & Tatum
Five Palo Alto Square
3000 El Camino Real
Palo Alto, CA 94306-2155
(415) 843-5000

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address : COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
07/389,334	08/03/89	MOORE C	A50412WEH

EXAMINER
ENG, D

FLEHR, HOHBACH, TEST,
ALBRITTON & HERBERT
SUITE 3400
FOUR EMBARCADERO CENTER
SAN FRANCISCO, CA 94111

ART UNIT	PAPER NUMBER
2315	8

DATE MAILED: 12/31/92

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☒ Responsive to communication filed on 10/2/92 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), ____ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, Form PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 1, 3, 6-13, 16-30 and 32-70 are pending in the application.
   Of the above, claims 1, 12-13, 16-25, and 48-70 are withdrawn from consideration.
2. ☒ Claims 2, 4, 5, 14, 15 and 31 have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 3, 6-11, 26-30, 32-47 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable. ☐ not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed on _____, has been ☐ approved. ☐ disapproved (see explanation).
12. ☐ Acknowledgment is made of the claim for priority under U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____ ; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev. 9-89)

15. In the communication filed on October 2, 1992, applicants elect Group II with traverse. The claims are properly restricted for the reasons set forth in the last office action.

16. In the communication, applicants stated that claim 26 serves as a linking claim and that a complete examination of claim 26 will require consideration of the art for both groups. The examiner disagrees. In considering restriction, the claims are assumed to be patentable (MPEP 806.05 (a)). The art for Group I and II is separately claimed in claim 1 and 3. In other words, each of the Group I and II does not rely on the other for patentability. In examining claim 26, it does not require to consider the detail claimed in claim 2 which is in Group I. In examining claim 13, it does not require to consider all the details claimed in claim 36. In examining claim 16, it does not require to consider all the details claimed in claim 39. In examining claim 41, it does not require to consider all the details claimed in 21. In examining claim 2, it does not require to consider all the detail claimed in claim 6. In examining claim 24, it does not require to consider all the details claimed in claim 46. In examining claim 3, it does not require to consider the detail in claim 59-62.

17. In conclusion, the independent claims which respectively and solely claim the subject matter in a group is evidence that they do not rely on the detail claimed in the combination claims (one

of the dependent claims in the set of independent claim 26) for patentability. The restriction therefore is proper.

18. The remark in line 11-13 of page 2 of the October 2 communication is not understood. Claim 22 is neither in Group II nor Group X.

19. Claim 12 is inadvertently omitted in the last office action. The error is regretted. Claim 12 should be in Group II.

20. Claims 6, 10, 11, 26-30 and 31-37 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

21. With respect to claim 6, the components (means for storing a top item, means for storing a next item and the at least one stack register) of the first push down stack as recited do not appear to render the push down stack to operate as a stack. Note that a stack is such that an item propagated from one end of the stack to another via the stages in the stack. The stack as recited in the claim does not do that. Further, the claim fails to recite how the components of the stack are interconnected so as to form a stack having stages between the input and the output of the stack. The second push down stack has similar defects. Register file is not a stack.

22. Claim 6 further fails to recite how each of the means as recited functionally coacts with each other so as to achieve any

meaningful function or improvement. Although each of the means are recited to be interconnected, no meaningful coact is seen. For example, the means for storing top item of the first stack which is for providing a top item to ALU is recited for providing the same to another stack. The second stack as recited has nothing to do with arithmetic operation. It is not seen why it should receive a top item as the ALU. More example, the second stack is recited to be connected to the means for storing top item bidirectionally. However, the means for storing top item has not been recited for receiving anything from the second stack. It appears to the examiner that they should not be bidirectionally connected and controlled because the means for storing top item is part of another stack and it should receive items from the next stage of its own stack and not from another stack (the second stack).

23. Other claims (claims 27-29 and 37-38, for example) which recite stack have similar defects as claim 6.

24. In claims 10 and 33, it is not clear what is meant by "to provide a microloop in said instruction register". Note that an IR is commonly for storing instruction. Further, it is not seen how the supplying of control/reset signals to counters would provide a microloop in an instruction register.

25. Function of the counter as recited in claims 11 and 34 is not clear. It is not seen how the counter which is recited for

controlling supply of instructions can select variable width operand. Further, claims 11 fails to recite where the variables width operand is stored.

26. In claim 26, function of the multiplexing means is not clear. A multiplexer which is commonly for multiplexing is recited to provide different types of data on a bus. Where do the row addresses, column addresses and data come from and go to?

27. In claim 35, function of the means for fetching is not clear. A fetching means which is commonly for fetching is erroneously recited for assembly and storing instructions.

28. In claim 39, it is not clear what is meant by "different memory access timing for different sizes of DRAM". Is it referring to different storing capacity sizes, to different amount of instructions accessed at a time or to different physical sizes? Further with respect to claim 39, it is not seen how the sensing circuit and the driver circuit as recited can render the microprocessor to provide different sizes of DRAM.

29. Claim 41 is not understood. It is not clear what is meant by "ring counter -- to provide different clock speed -- depending on at least one of temperature, voltage and microprocessor fabrication process --". How does the clock response to the temperature, voltage and microprocessor fabrication process?

30. In claim 42, what is meant by "I/O interface -- to exchange -- signals -- with said I/O interface --"? What is

connected to the I/O interface and exchange with who? Claim 42 further fails to recite how the clock and the I/O interface functionally coact with each other so as to perform any meaningful operation.

31. Claims 44 and 45 fail to recite function of each of the elements recited therein and how they are functionally coact with each other such that desired result can be achieved.

32. Claims 37-38 are rejected under 35 USC 112 and objected to under 37 CFR 1.75 (b) as unduly multiplied.

33. Claims 37-38 are almost identical to parent claim 27-29.

34. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

35. Claims 3, 6-10, 26-30 and 32-33 are rejected under 35 U.S.C. § 103 as being unpatentable over Takahira.

36. See at least Figure 2 and the corresponding description in

the specification of Takahira. The drawing shows a data processing system having a CPU, memory, EEPROM, RAM, ROM, clock circuit, register file, status register, index register X and Y, program counter H and L for fetching instructions, ALU, accumulator, stacks and stack pointer, instruction register, instruction decoder and a bus. With respect to claim 3, Takahira does not specify how many instructions can be fetched per memory cycle.

One of ordinary skill in the art should readily recognize that, for the same machine, more instructions can be fetched if the memory cycle is extended longer. How long a memory cycle should be is merely a matter of design choice because it is dependent on the speed of the elements used and on the engineering design.

37. With respect to claim 7, one of ordinary skill in the art should readily recognize that for the same given amount of time more instructions can be fetched if the previous instruction is not a memory instruction because it is well known that a memory instruction takes longer time to executed.

38. With respect to claim 10, looping is well known in programming art. One of ordinary skill in the art should readily recognize that the processing system of Takahira as shown in Figure 2 is capable of looping because it also has program counters.

39. Claims 11 and 34 are rejected under 35 U.S.C. § 103 as being unpatentable over Takahira in view of Heath.

40. Takahira discloses claim combination set forth above. Takahira does not state whether his operand is of variable length. Heath shows such in lines 31 et seq. of column 5. It would have been obvious to make Takahira's operand variable length because it would be more flexible.

41. Claim 35 ~~is~~ and 12 are rejected under 35 U.S.C. § 103 as being unpatentable over Takahira and Heath in view of Bruinhorst.

42. Takahira and Heath disclose claim combination set forth above. Takahira does not state whether his program in PROM is transferred to RAM. Such is well known in the art as shown by Bruinhorst in lines 43 et seq. of column 15. It would have been obvious to load from PROM to RAM in Takahira as taught by Bruinhorst because it is more flexible in programming.

43. Claims 36, 37 and 38 are rejected under 35 U.S.C. § 103 as being unpatentable over Takahira, Heath, Bruinhorst further in view of Derchak.

44. Takahira, Heath and Bruinhorst disclose claim combination set forth above. Takahira does not show a DMA. DMA is well known in the art. Derchak shows such. It would have been obvious to a person of ordinary skill in the art to incorporate a DMA as taught by Derchak in Takahira because that would render Takahira's system more efficient.

45. Claims 39 and 40 are rejected under 35 U.S.C. § 103 as being unpatentable over Takahira, Heath, Bruinhorst, Derchak further in view of Kimoto.

46. Takahira does not state whether his microprocessor is capable of accessing the memory at a desired variable access time. Such is well known in the art as shown by Kimoto. It would have been obvious to a person of ordinary skill in the art to access the memory of Takahira as taught by Kimoto because the system of Takahira would run more efficiently.

47. Claims 41-45 are rejected under 35 U.S.C. § 103 as being unpatentable over Takahira, Heath, Bruinhorst, Derchak, Kimoto further in view of ~~Kimoto~~ Martin.

48. Takahira does not state whether his clock is of variable clock rate. Variable rate clock is well known in the art. ~~Kimoto~~ Martin shows such. (Fajcon) It would have been obvious to a person of ordinary skill in the art to incorporate a variable speed clock in Takahira's system if the circuits require.

49. With respect to claims 42-43, Takahira shows an I/O interface 13 in Figure 2.

50. Claims 46 and 47 are allowable if the 35 USC 112, second paragraph rejection is overcome.

51. Applicant's arguments with respect to claims 3, 6-11 and 26-30 and 32-45 have been considered but are deemed to be moot in view of the new grounds of rejection.

52. The prior art cited on July 10, 1992 has not been considered because the class and subclass information is missing.

Any inquiry concerning this communication should be directed to David Eng at telephone number (703) 308-1635.

DAVID Y. ENG
PRIMARY EXAMINER
ART UNIT 232

DE/kw
December 29, 1992

WHAT IS CLAIMED IS:

1. A microprocessor system, comprising a central processing unit, a dynamic random access memory, a bus connecting said central processing unit to said dynamic random access memory, and multiplexing means on said bus between said central processing unit and said dynamic random access memory, said multiplexing means being connected and configured to provide row addresses, column addresses and data on said bus.

2. The microprocessor system of Claim 1 in which said multiplexing means includes a plurality of latches for providing the row addresses to said dynamic random access memory.

3. A microprocessor system, comprising a central processing unit, a memory, a bus connecting said central processing unit to said memory, and means connected to said bus for fetching instructions for said central processing unit on said bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle.

4. The microprocessor system of Claim 3 in which said central processing unit includes an arithmetic logic unit and a first push down stack connected to said arithmetic logic unit, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit and means for storing a next item connected to a second input of said arithmetic logic unit, said arithmetic logic unit having an output connected to said means for storing a top item.

5. The microprocessor system of Claim 4 additionally comprising a second push down stack, said means for storing a top item being connected to provide an input to

said second push down stack.

6. The microprocessor system of Claim 5 in which said second push down stack comprises a register file and said means for storing a top item and said register file are bidirectionally connected.

7. The microprocessor system of Claim 3 additionally comprising means connected to said means for fetching multiple instructions for determining if multiple instructions fetched by said means for fetching multiple instructions require a memory access, said means for fetching multiple instructions fetching additional multiple instructions if the multiple instructions do not require a memory access.

8. The microprocessor system of Claim 3 in which said microprocessor system, including said memory, is contained in an integrated circuit, said memory is a dynamic random access memory, and said means for fetching multiple instructions includes a column latch for receiving the multiple instructions.

9. The microprocessor system of Claim 3 additionally comprising an instruction register for the multiple instructions connected to said means for fetching instructions, means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession, means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions, said counter being connected to said means for decoding to receive incrementing and reset control signals from said means

A-50412/WEH

for decoding, said means for decoding being configured to supply the reset control signal to said counter and to supply a control signal to said means for fetching instructions in response to a SKIP instruction in the multiple instructions.

10. The microprocessor system of Claim 9 additionally comprising a loop counter connected to receive a decrement control signal from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and the decrement control signal to said loop counter in response to a MICROLOOP instruction in the multiple instructions.

11. The microprocessor system of Claim 3 additionally comprising an instruction register for the multiple instructions connected to said means for fetching instructions, means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession, means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions, said counter being connected to said means for decoding to receive incrementing and reset control signals from said means for decoding, said means for decoding being configured to control said counter in response to an instruction utilizing a variable width operand, and means connected to said counter to select the variable width operand in response to said counter.

12. A microprocessor system, comprising a central processing unit, a dynamic random access memory, a bus connecting said central processing unit to said dynamic

random access memory, a programmable read only memory containing instructions connected to said bus, means connected to said bus for fetching instructions for said central processing unit on said bus, said means for fetching instructions including means for assembling a plurality of instructions from said programmable read only memory and storing the plurality of instructions in said dynamic random access memory.

13. A microprocessor system, comprising a central processing unit, a direct memory access processing unit, a memory, a bus connecting said central processing unit and said direct memory access processing unit to said memory, said memory containing instructions for said central processing unit and said direct memory access processing unit, said direct memory access processing unit including means for fetching instructions for said central processing unit on said bus and for fetching instructions for said direct memory access processing unit on said bus.

14. A microprocessor system comprising an arithmetic logic unit, a first push down stack connected to said arithmetic logic unit, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit and means for storing a next item connected to a second input of said arithmetic logic unit, said arithmetic logic unit having an output connected to said means for storing a top item, a register file, said means for storing a top item being connected to provide an input to said register file.

15. The microprocessor system of Claim 14 in which said register file comprises a second push down stack and said means for storing a top item and said register file are bidirectionally connected.

16. A data processing system, comprising a microprocessor including a sensing circuit and a driver circuit, a memory, and an output enable line connected between said memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level, said microprocessor being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

17. The data processing system of Claim 16 in which the predetermined electrical level is a predetermined voltage.

18. The data processing system of Claim 17 in which said memory is a dynamic random access memory.

19. A microprocessor system, comprising a central processing unit and a ring counter variable speed system clock connected to said central processing unit, said central processing unit and said ring counter variable speed system clock being provided in a single integrated circuit.

20. The microprocessor system of Claim 19 additionally comprising an input/output interface connected to exchange coupling control signals, addresses and data with said input/output interface, and a second clock independent of said ring counter variable speed system clock connected to said input/output interface.

21. The microprocessor system of Claim 20 in which said second clock is a fixed frequency clock.

22. A microprocessor system, comprising a central

processing unit, a memory, a bus connecting said central processing unit to said memory, said central processing unit including an arithmetic logic unit and a push down stack connected to said arithmetic logic unit, said push down stack including means for storing a top item connected to a first input of said arithmetic logic unit and means for storing a next item connected to a second input of said arithmetic logic unit, said arithmetic logic unit having an output connected to said means for storing a top item, said push down stack having a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit.

23. The microprocessor system of Claim 22 additionally comprising a first pointer connected to said first plurality of stack elements, a second pointer connected to said second plurality of stack elements, and a third pointer connected to said third plurality of stack elements, said central processing unit being connected to pop items from said first plurality of stack elements, said first stack pointer being connected to said second stack pointer to pop a first plurality of items from said second plurality of stack elements when said first plurality of stack elements are empty from successive pop operations by said central processing unit, said second stack pointer being connected to said third stack pointer to pop a second plurality of items from said third plurality of stack elements when said second plurality of stack elements are empty from successive pop operations by said central processing unit.

24. A microprocessor system, comprising a central processing unit, said central processing unit including an arithmetic logic unit, a first register connected to supply a first input to said arithmetic logic unit, a first shifter connected between an output of said arithmetic logic unit and said first register, a second register connected to receive a starting polynomial value, an output of said second register being connected to a second shifter, a least significant bit of said second register being connected to said arithmetic logic unit, a third register connected to supply feedback terms of a polynomial to said arithmetic logic unit, a down counter, for counting down a number corresponding to digits of a polynomial to be generated, connected to said arithmetic logic unit, said arithmetic logic unit being responsive to a polynomial instruction to carry out an exclusive OR of the contents of said first register with the contents of said third register if the least significant bit of said second register is a "ONE" and to pass the contents of said first register unaltered if the least significant bit of said second register is a "ZERO", until said down counter completes a count, the polynomial to be generated resulting in said first register.

25. A microprocessor system, comprising a central processing unit, said central processing unit including an arithmetic logic unit, a result register connected to supply a first input to said arithmetic logic unit, a first, left shifting shifter connected between an output of said arithmetic logic unit and said result register, a multiplier register connected to receive a multiplier in bit reversed form, an output of said multiplier register being connected to a second, right shifting shifter, a least significant bit of said second register being connected to said arithmetic logic unit, a third register connected to supply a multiplicand to said arithmetic

logic unit, a down counter, for counting down a number corresponding to one less than the number of digits of the multiplier, connected to said arithmetic logic unit, said arithmetic logic unit being responsive to a multiply instruction to add the contents of said result register with the contents of said third register when the least significant bit of said multiplier register is a "ONE" and to pass the contents of said result register unaltered when the least significant bit of said multiplier is a "ZERO", until said down counter completes a count, the product resulting in said first register.

26. A microprocessor system, comprising a central processing unit, a dynamic random access memory, a bus connecting said central processing unit to said dynamic random access memory, and multiplexing means on said bus between said central processing unit and said dynamic random access memory, said multiplexing means being connected and configured to provide row addresses, column addresses and data on said bus, and

means connected to said bus for fetching instructions for said central processing unit on said bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle.

27. The microprocessor system of Claim 26 in which said central processing unit includes an arithmetic logic unit and a first push down stack connected to said arithmetic logic unit, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit and means for storing a next item connected to a second input of said arithmetic logic unit, said arithmetic logic unit having an output connected to said means for storing a top item.

28. The microprocessor system of Claim 27

additionally comprising a second push down stack, said means for storing a top item being connected to provide an input to said second push down stack.

29. The microprocessor system of Claim 28 in which said second push down stack comprises a register file and said means for storing a top item and said register file are bidirectionally connected.

30. The microprocessor system of Claim 29 additionally comprising means connected to said means for fetching multiple instructions for determining if multiple instructions fetched by said means for fetching multiple instructions require a memory access, said means for fetching multiple instructions fetching additional multiple instructions if the multiple instructions do not require a memory access.

31. The microprocessor system of Claim 30 in which said microprocessor system, including said memory, is contained in an integrated circuit, said memory is a dynamic random access memory, and said means for fetching multiple instructions includes a column latch for receiving the multiple instructions.

32. The microprocessor system of Claim 30 additionally comprising an instruction register for the multiple instructions connected to said means for fetching instructions, means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession, means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions, said counter being

connected to said means for decoding to receive incrementing and reset control signals from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and to supply a control signal to said means for fetching instructions in response to a SKIP instruction in the multiple instructions.

33. The microprocessor system of Claim 32 additionally comprising a loop counter connected to receive a decrement control signal from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and the decrement control signal to said loop counter in response to a MICROLOOP instruction in the multiple instructions.

34. The microprocessor system of Claim 33 in which said means for decoding is configured to control said counter in response to an instruction utilizing a variable width operand, said microprocessor system additionally comprising means connected to said counter to select the variable width operand in response to said counter.

35. The microprocessor system of Claim 34 additionally comprising a programmable read only memory containing instructions connected to said bus, means connected to said bus for fetching instructions for said central processing unit on said bus, said means for fetching instructions including means for assembling a plurality of instructions from said programmable read only memory and storing the plurality of instructions in said dynamic random access memory.

36. The microprocessor system of Claim 35 additionally comprising a direct memory access processing unit, said bus connecting said direct memory access

processing unit to said dynamic random access memory, said dynamic random access memory containing instructions for said central processing unit and said direct memory access processing unit, said direct memory access processing unit including means for fetching instructions for said central processing unit on said bus and for fetching instructions for said direct memory access processing unit on said bus.

37. The microprocessor system of Claim 36 in which said central processing unit includes an arithmetic logic unit, a first push down stack connected to said arithmetic logic unit, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit and means for storing a next item connected to a second input of said arithmetic logic unit, said arithmetic logic unit having an output connected to said means for storing a top item, a register file, said means for storing a top item being connected to provide an input to said register file.

38. The microprocessor system of Claim 37 in which said register file comprises a second push down stack and said means for storing a top item and said register file are bidirectionally connected.

39. The microprocessor system of Claim 38 in which said microprocessor system includes a sensing circuit and a driver circuit, and an output enable line connected between said dynamic random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level, said microprocessor system being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

40. The microprocessor system of Claim 39 in which the predetermined electrical level is a predetermined voltage.

41. The microprocessor system of Claim 40 additionally comprising a ring counter variable speed system clock connected to said central processing unit, said central processing unit and said ring counter variable speed system clock being provided in a single integrated circuit.

42. The microprocessor system of Claim 41 additionally comprising an input/output interface connected to exchange coupling control signals, addresses and data with said input/output interface, and a second clock independent of said ring counter variable speed system clock connected to said input/output interface.

43. The microprocessor system of Claim 42 in which said second clock is a fixed frequency clock.

44. The microprocessor system of Claim 43 in which said first push down stack has a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit.

45. The microprocessor system of Claim 44 additionally comprising a first pointer connected to said first plurality of stack elements, a second pointer connected to said second plurality of stack elements, and a third pointer connected to said third plurality of stack

elements, said central processing unit being connected to pop items from said first plurality of stack elements, said first stack pointer being connected to said second stack pointer to pop a first plurality of items from said second plurality of stack elements when said first plurality of stack elements are empty from successive pop operations by said central processing unit, said second stack pointer being connected to said third stack pointer to pop a second plurality of items from said third plurality of stack elements when said second plurality of stack elements are empty from successive pop operations by said central processing unit.

SUB D7

46. The microprocessor system of Claim 45 additionally comprising a first register connected to supply a first input to said arithmetic logic unit, a first shifter connected between an output of said arithmetic logic unit and said first register, a second register connected to receive a starting polynomial value, an output of said second register being connected to a second shifter, a least significant bit of said second register being connected to said arithmetic logic unit, a third register connected to supply feedback terms of a polynomial to said arithmetic logic unit, a down counter, for counting down a number corresponding to digits of a polynomial to be generated, connected to said arithmetic logic unit, said arithmetic logic unit being responsive to a polynomial instruction to carry out an exclusive OR of the contents of said first register with the contents of said third register if the least significant bit of said second register is a "ONE" and to pass the contents of said first register unaltered if the least significant bit of said second register is a "ZERO", until said down counter completes a count, the polynomial to be generated resulting in said first register.

47. The microprocessor system of Claim 46 in which said first register is a result register, said first shifter is a left shifting shifter, said second register is a multiplier register connected to receive a multiplier in bit reversed form, said second shifter is a right shifting shifter, said third register is connected to supply a multiplicand to said arithmetic logic unit, said down counter is configured for counting down a number corresponding to one less than the number of digits of the multiplier, said arithmetic logic unit being responsive to a multiply instruction to add the contents of said result register with the contents of said third register, if the least significant bit of said second register is a "ONE" and to pass the contents of said first register unaltered if the least significant bit of said second register is a "ZERO" until said down counter completes a count, the product resulting in said first register.

48. A microprocessor, which comprises a main central processing unit and a separate direct memory access central processing unit in a single integrated circuit comprising said microprocessor, said main central processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus, said internal data bus being bidirectionally connected to a loop counter, said loop counter being connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register, said internal data bus being connected to a memory controller, to a Y register of a return push down stack, an X register and a program

counter, said Y register, X register and program counter providing outputs to an internal address bus, said internal address bus providing inputs to said memory controller and to an incrementer, said incrementer being connected to said internal data bus, said direct memory access central processing unit providing inputs to said memory controller, said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory.

49. The microprocessor of Claim 48 in which said memory controller includes a multiplexing means between said central processing unit and said address/data bus, said multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus.

50. The microprocessor of Claim 48 in which said memory controller includes means for fetching instructions for said central processing unit on said address/data bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle.

51. The microprocessor of Claim 50 additionally comprising means connected to said means for fetching instructions for determining if multiple instructions fetched by said means for fetching instructions require a memory access, said means for fetching instructions fetching additional multiple instructions if the multiple instructions do not require a memory access.

52. The microprocessor of Claim 50 in which said microprocessor and a dynamic random access memory are contained in a single integrated circuitand said means for fetching instructions includes a column latch for

receiving the multiple instructions.

53. The microprocessor of Claim 48 in which said microprocessor includes a sensing circuit and a driver circuit, and an output enable line for connection between the random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level, said microprocessor being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

54. The microprocessor of Claim 48 additionally comprising a ring counter variable speed system clock connected to said main central processing unit, said main central processing unit and said ring counter variable speed system clock being provided in a single integrated circuit.

55. The microprocessor of Claim 54 in which said memory controller includes an input/output interface connected to exchange coupling control signals, addresses and data with said main central processing unit, said microprocessor additionally including a second clock independent of said ring counter variable speed system clock connected to said input/output interface.

56. The microprocessor of Claim 48 in which said first push down stack has a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to

said single integrated circuit.

57. The microprocessor of Claim 56 additionally comprising a first pointer connected to said first plurality of stack elements, a second pointer connected to said second plurality of stack elements, and a third pointer connected to said third plurality of stack elements, said central processing unit being connected to pop items from said first plurality of stack elements, said first stack pointer being connected to said second stack pointer to pop a first plurality of items from said second plurality of stack elements when said first plurality of stack elements are empty from successive pop operations by said central processing unit, said second stack pointer being connected to said third stack pointer to pop a second plurality of items from said third plurality of stack elements when said second plurality of stack elements are empty from successive pop operations by said central processing unit.

58. In a microprocessor system, a method for fetching instructions, each having a first plurality of bits, from a memory, which comprises providing an instruction register having a second plurality of bits constituting a multiple of the first plurality of bits, fetching a first set of multiple sequential instructions in a single memory cycle, storing the multiple sequential instructions in the instruction register, determining if the multiple instructions require a memory access, and fetching a second set of multiple instructions during execution of the first set of multiple instructions if the first set of multiple instructions do not require access to the memory.

59. The method of Claim 58 in which a portion of the multiple sequential instructions are skipped in response

to a SKIP instruction.

60. The method of Claim 58 in which a portion of the multiple sequential instructions are repeated a predetermined number of times in response to a MICROLOOP instruction.

61. The method of Claim 58 additionally comprising the steps of storing an instruction utilizing a variable width operand and the variable width operand in said instruction register, determining if the instruction utilizes a variable width operand, and selecting the width of the operand for output from said instruction register in response to the instruction using the variable width operand.

62. The method of Claim 58 additionally comprising the steps of storing a plurality of instructions in a read only memory, fetching selected instructions from the plurality of instructions, assembling the multiple sequential instructions, and storing the multiple sequential instructions in a random access memory prior to fetching the multiple sequential instructions.

63. In a microprocessor connected to a memory by an output enable line, a method for determining when an enable signal can be sent to said memory, which comprises sensing a predetermined electrical level on said output enable line, and providing the enabling signal on said output line in response to the predetermined electrical level.

64. The method of Claim 63 in which the predetermined electrical level is a voltage.

65. In a microprocessor integrated circuit, a method

for clocking the microprocessor, which comprises fabricating a ring counter system clock and the microprocessor each having a plurality of transistors having operating characteristics which vary in the same way with variations in their fabrication, and using the ring counter system clock for clocking the microprocessor.

66. The method of Claim 65 additionally comprising the steps of providing an input/output interface for the microprocessor integrated circuit and clocking the input/output interface with a second clock independent of the ring counter system clock.

67. The method of Claim 66 in which the second clock is a fixed frequency clock.

68. In a microprocessor system, a method for operating a push down stack, which comprises providing a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, the first and second plurality of stack elements being provided in a single integrated circuit with the microprocessor, providing a third plurality of stack elements configured as a random access memory external to the single integrated circuit, storing items in the push down stack, popping up to a first plurality of items from the first plurality of stack elements without accessing the second plurality of stack elements, popping a first plurality of items from the second plurality of stack elements when the first plurality of stack elements are empty, popping up to the second plurality of items from the second plurality of stack elements without accessing the third plurality of stack elements, and popping a second plurality of items from the third plurality of stack elements when the second plurality of stack elements are empty.

69. A method for generating a polynomial, which comprises providing a starting polynomial value, right shifting feedback terms for the polynomial, determining if a least significant bit of the starting polynomial value is a "ONE" or a "ZERO", performing an exclusive OR of the shifted feedback terms for the polynomial with the feedback terms for the polynomial if the least significant bit of the starting polynomial is a "ONE", right shifting the shifted feedback terms for the polynomial if the least significant bit of the the starting polynomial is a "ZERO", and repeating the above operations a total number of times equal to the number of digits of the polynomial to be generated.

70. A method of multiplying, which comprises providing a multiplier, a multiplicand and a "ZERO", determining if a least significant bit of the multiplier is a "ONE" or a "ZERO", adding the multiplicand and the "ZERO" and shifting the sum left if the least significant bit of the multiplicand is a "ONE", storing the "ZERO" if the least significant bit of the the starting polynomial is a "ZERO", to give a partial result, shifting the multiplier right to give a right shifted multiplier, and repeating the above operations, using the right shifted multiplier in place of the multiplier and the partial result in place of the given "ZERO" after the first time the operations are performed, and shifting the sum of the partial result and the multiplicand or the passed through partial result left to carry out the operations a total number of times equal to one less than the number of digits in the multiplier, to give a desired product.

Add B13 Add C3

Rewrite claims 1, 3, 6, 8, 10, 12, 13, 16, 19, 22, 23, 26, 27, 28, 34, 39, 41, 44, 45, 52, 53, 54, 58, 62, 63, 65, 68, 69 and 70 as follows:

1(Amended). ~~A microprocessor system, comprising a central processing~~ unit, a dynamic random access memory, a bus connecting said central processing unit to said dynamic random access memory, and multiplexing means on said bus between said central processing unit and said dynamic random access memory, said multiplexing means being connected and configured to provide multiplexed row ~~addresses, column addresses and data on said bus.~~

3(Amended). A microprocessor system, comprising a central processing unit, a memory, a bus connecting said central processing unit to said memory, and means connected to said bus for fetching instructions for said central processing unit on said bus from said memory, said means for fetching instructions being configured and connected to fetch multiple sequential instructions in parallel during a single memory cycle.

6(Amended). The microprocessor system of Claim [5] 3 in which said central processing unit includes an arithmetic logic unit and a first push down stack connected to said arithmetic logic unit, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input, means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input, and at least one stack register connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack, said arithmetic logic unit having an output connected to said means for storing a top item, a second push down stack, said means for storing a top item being connected to provide an input to said second push down stack and a control means connected between said means for storing a top item and said second push down stack for controlling provision of the input to said second push down stack, said second push down stack comprises a register file and said means for storing a top item and said register file are bidirectionally connected.

8(Amended). The microprocessor system of Claim 5 in which said microprocessor system, including said memory, is contained in an integrated circuit, said memory is a dynamic random access main memory, and said means for fetching multiple instructions includes a column latch for receiving the multiple instructions.

10(Amended). The microprocessor system of Claim 9 additionally comprising a loop counter connected to receive a decrement control signal from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and the decrement control signal to said loop counter in response to a MICROLOOP instruction in the multiple instructions to provide a microloop in said instruction register.

12(Amended). A microprocessor system, comprising a central processing unit, a dynamic random access memory, a bus connecting said central processing unit to said dynamic random access memory, a programmable read only memory containing instructions connected to said bus, means connected to said bus for fetching instructions for said central processing unit on said bus from said programmable read only memory, said means for fetching instructions including means for assembling a plurality of instructions from said programmable read only memory and storing the plurality of instructions in said dynamic random access memory, said means for fetching instructions being configured to configure said bus dynamically as unmultiplexed data and address lines during reading of the plurality of instructions from said programmable read only memory and to a multiplexed bus for row addresses, column addresses and data during transfer of the plurality of instructions to said dynamic random access memory.

13(Amended). A microprocessor system, comprising a central processing unit, a direct memory access processing unit, a memory, a bus connecting said central processing unit and said direct memory access processing unit to said memory, said memory containing instructions for said central processing unit and said direct memory access processing unit, said direct memory access processing unit including means for fetching instructions for said central processing unit from

said memory on said bus, supplying the instructions for said central processing unit to said central processing unit, [and] for fetching instructions for said direct memory access processing unit from said memory on said bus and for supplying the instructions for said direct memory access processing unit to said direct memory access processing unit.

16(Amended). A data processing system configured to provide different memory access timing for different amounts of memory connected in said data processing system, comprising a microprocessor including a sensing circuit and a driver circuit, a memory, and an output enable line connected between said memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level after a memory read operation, said microprocessor being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

19(Amended). A microprocessor system which operates at a variable clock speed, comprising a central processing unit and a ring counter variable speed system clock connected to said central processing unit, said central processing unit and said ring counter variable speed system clock being provided in a single integrated circuit, said ring counter variable speed system clock being configured to provide different clock speeds to said central processing unit, depending on at least one of temperature, voltage and microprocessor fabrication process.

22(Amended). A microprocessor system, comprising a central processing unit, a memory, a bus connecting said central processing unit to said memory, said central processing unit including an arithmetic logic unit and a push down stack connected to said arithmetic logic unit, said push down stack including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input and means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input, and at least one stack register connected to said means for storing a next item to receive the

next item from said means for storing a next item when pushed down in said push down stack, said arithmetic logic unit having an output connected to said means for storing a top item, said push down stack having a first plurality of stack registers having stack memory elements configured as latches, a second plurality of stack registers having stack memory elements configured as a random access memory, said first and second plurality of stack [elements] registers and said central processing unit being provided in a single integrated circuit, and a third plurality of stack registers having stack memory elements configured as a random access memory external to said single integrated circuit.

23(Amended). The microprocessor system of Claim 22 additionally comprising a first pointer connected to said first plurality of stack [elements] registers, a second pointer connected to said second plurality of stack [elements] registers, and a third pointer connected to said third plurality of stack [elements] registers, said central processing unit being connected to pop items from said first plurality of stack [elements] registers, said first stack pointer being connected to said second stack pointer to pop a first plurality of items from said second plurality of stack [elements] registers when said first plurality of stack [elements] registers are empty from successive pop operations by said central processing unit, said second stack pointer being connected to said third stack pointer to pop a second plurality of items from said third plurality of stack [elements] registers when said second plurality of stack [elements] registers are empty from successive pop operations by said central processing unit.

26(Amended). A microprocessor system, comprising a central processing unit, a dynamic random access memory, a bus connecting said central processing unit to said dynamic random access memory, and multiplexing means on said bus between said central processing unit and said dynamic random access memory, said multiplexing means being connected and configured to provide multiplexed row addresses, column addresses and data on said bus, and

means connected to said bus for fetching instructions for said central processing unit on said bus from said memory, said means for fetching instructions

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address : COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.

EXAMINER

ART UNIT | PAPER NUMBER

4

DATE MAILED

COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☒ Responsive to communication filed on 6/8/92 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire ____ month(s), 30 days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of informal Patent Application, Form PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 1, 3, 6-13, 16-30 and 32-70 are pending in the application.

   Of the above, claims _____ are withdrawn from consideration.

2. ☒ Claims 2, 4, 5, 14, 15 and 31 have been cancelled.

3. ☐ Claims _____ are allowed.

4. ☐ Claims _____ are rejected.

5. ☐ Claims _____ are objected to.

6. ☒ Claims 1, 3, 6-13, 16-30 & 32-70 are subject to restriction or election requirement.

7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.

8. ☐ Formal drawings are required in response to this Office action.

9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable. ☐ not acceptable (see explanation or Notice re Patent Drawing, PTO-948).

10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).

11. ☐ The proposed drawing correction, filed on _____, has been ☐ approved. ☐ disapproved (see explanation).

12. ☐ Acknowledgment is made of the claim for priority under U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____ ; filed on _____

13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev. 9-89)

15. Claims 2, 4, 5, 14, 15 and 31 have been cancelled. The active claims are 1, 3, 6-13, 16-30 and 32-70.

16. Restriction to one of the following inventions is required under 35 U.S.C. § 121:

I. Claims 1 and 2, drawn to microprocessor system having a multiplex bus, classified in Class 395, subclass 325.

II. Claims 3, 6-11, 26-30 and 32-47, drawn to a processor system having means for fetching multiple instructions in parallel during a single maching cycle, classified in Class 395, subclass 775.

17. III. Claim13, drawn to a microprocessor system having a DMA for fetching instruction for a CPU and itself, classified in Class 395, subclass 725.

18. IV. Claims 16-18 and 63-64, drawn to a processing system configured to provide different memory access time for different amounts of memory, classified in Class 395, subclass 425.

19. V. Claims, 19-21 and 65-67, drawn to method and appartus which operates at a varible clock speed, classified in Class 395, subclass 550.

20. VI. Claims 22-23, drawn to a CPU having stacks and pointers, classified in Class 395, subclass 800.

21. VII. Claims 24-25 and 69-70, drawn to a processing system for processing polynominal instruction, classified in Class 395, subclass 800.

22. VIII. Claims 48-57, drawn to a microprocessor architecture, classified in Class 395, subclass 800.

23. IX. Claims 58-62, drawn to method for prefetching, classified in Class 395, subclass 375.

24. X. Claim 68, drawn to method for operating a stack, classified in Class 395, subclass 800.

25. The inventions are distinct, each from the other because of the following reasons:

26. Inventions I to IX and X are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations. (M.P.E.P. § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the combination (claim 26, AB_{br}) as claimed does not set forth the details [the multiplex bus in claim 12, the DMA in claim 13, the variable acess time memory in claim 16, the variable clock speed in claim 19, the stack in claim 22, the polynominal instruction processor in claim 24, the microprocessor architecture in claim 48, the prefetching in claim 58 and the method for operating a stock in claim 68, B_{sp}] of the subcombination as separately claimed. The subcombination has separate utility such as each of

the inventions do not require the other inventions for operation.

27. Because these inventions are distinct for the reasons given above and the search required for each of the inventions is not required for each other groups restriction for examination purposes as indicated is proper.

28. Applicant is advised that the response to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed.

29. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 C.F.R. § 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently-filed petition under 37 C.F.R. § 1.48(b) and by the fee required under 37 C.F.R. § 1.17(h).

Any inquiry concerning this communication should be directed to Examiner David Eng at telephone number (703) 308-~~0754~~ 1635.

DE/ss
August 21, 1992

DAVID Y. ENG
PRIMARY EXAMINER
ART UNIT 232

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Moore, et al.
U.S. Patent No.:	5,530,890
Issue Date:	June 25, 1995
Serial No.:	08/480,206
Filing Date:	June 7, 1995
Title:	High performance, low cost microprocessor

Mail Stop Ex Parte Reexam
Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR EX PARTE REEXAMINATION UNDER 35 U.S.C. § 302 AND 37 C.F.R. § 1.510

Reexamination under 35 U.S.C. § 302 and 37 C.F.R. § 1.510 is requested for all claims (i.e., claims 1-10) of U.S. Patent No. 5,530,890 (the '890 patent), which issued on June 25, 1996 to Moore, et al.

CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. EV741503103US

January 16, 2009
Date of Deposit

(Id. pg. 111)

MacGregor shows the MC68020 as including a plurality of on-chip Clock Generator circuits. *(Id., pg. 108, Figure 1)* The Clock Generator circuits are used to provide clocking signals to the various components of the MC68020. The MC68020 is capable of operating at clock frequencies of 16 MHz to 24 MHz. *(Id. pg. 117)* MacGregor also teaches a multiplexer included in the MC68020. The multiplexer sits between the internal 32-bit data/address bus and an external data/address bus. The multiplexer is used to transfer data to and from 8-, 16-, and 32-bit bus ports. *(Id., pg. 107)*

The instruction cache of the MC68020 is a 256-byte-on-chip instruction cache which is used to obtain a significant increase in performance by reducing the number of fetches required to external memory. The reduced bus utilization by the MC68020 also increases system performance by providing more bus bandwidth for other bus masters such as DMA devices. The cache interface to the processor data paths allows complete overlap of instruction fetches with data operand accesses, and thus provides a significant increase in performance. A hit in the instruction cache allows for concurrent instruction and data fetches to take place. *(Id., pg. 107)*

The '890 patent teaches the same architecture and functionality described above in connection with the MacGregor reference. In the Summary of the Invention, the '890 patent describes a microprocessor which includes a first push down stack connected to an arithmetic logic unit. *(Appendix A., 3:4-6)* The first push down stack is described as being capable of providing inputs to the ALU and receiving an output from the ALU. In a second embodiment, the microprocessor is described as including a second stack configured as a random access memory. In this embodiment, the microprocessor includes first and second stack pointers for pushing and popping items from the push down stacks. *(Id., 3:55-66)* The '890 patent teaches a direct memory access controller and states that "conventional microprocessors provide direct memory accesses (DMA) for system peripheral units through DMA controllers, which may be located on the microprocessor integrated circuit" *(Id., 1:52-55)* The '890 patent further teaches means for fetching multiple instructions from a dynamic random access memory. The multiple instructions are then stored in an instruction register. The instruction register is connected to means for supplying the multiple instructions in succession from the instruction register. *(Id., 2:34-51)* The multiple instructions can be fetched in a single instruction cycle via a 32-bit

internal data bus. *(Id., 7:50-55)* One embodiment of the '890 patent teaches an internal oscillator fabricated on the same chip as the rest of the microprocessor. The internal oscillator provides clocking signals to various components of the microprocessor. *(Id., 17:20-36)* The '890 patent further teaches multiplexing means "configured to provide row addresses, column addresses and data on the bus." *(Id., 2:8-12)*

This is the same architecture taught in the MacGregor reference. In both the MacGregor reference and the '890 patent preferred embodiment, a microprocessor includes a 32-bit data/address bus, direct memory access means, two stacks, two stack pointers, a CPU, an ALU, multiplexing means for addressing memory, means for fetching multiple instructions in a single instruction fetch, and an on-chip clock generation circuit.

2. According to the Patent Owner's Assertions, One Skilled in the Art Would Understand McGregor to Disclose a Push Down Stack As Recited in the Claims

The Patent Owner has sent numerous communications to third parties in an attempt to solicit licenses under the '890 and '749 patents. The communications generally include claim charts stamped "confidential" that purport to show the correspondence between the third party processor systems and the claims of the '890 and '749 patents. Requester understands that scores of substantially similar claim charts have been sent to various companies throughout the semiconductor and other industries. The Office is encouraged to request these materials from the Patent Owner under Rule 105.[1]

---

[1] Requester submits that the Office is empowered to request this information under Rule 105, which provides in pertinent part:

> (a) (1) In the course of examining or treating a matter in a pending or abandoned application filed under 35 U.S.C. 111 or 371 (including a reissue application), in a patent, or in a reexamination proceeding, the examiner or other Office employee may require the submission, from individuals identified under § 1.56(c), or any assignee, of such information as may be reasonably necessary to properly examine or treat the matter, for example:
>
> . . .
>
> (viii) Technical information known to applicant. Technical information known to applicant concerning the related art, the disclosure, the claimed subject matter, other factual information pertinent to patentability, or concerning the accuracy of the examiner's stated interpretation of such items.

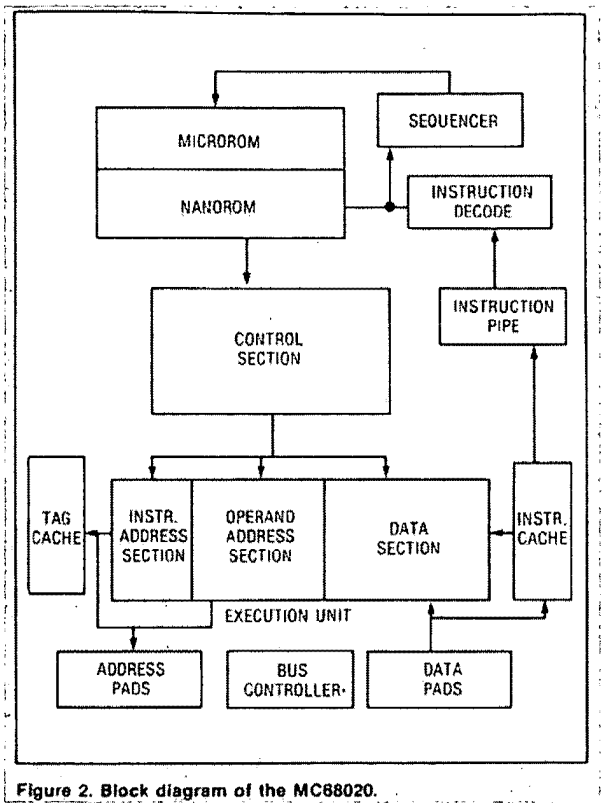
The assertions of infringement made by the Patent Owner explicitly contain a technical assessment of what architecture would necessarily be present in certain systems that include stack pointers. Requestor respectfully submits that this information is clearly "factual information pertinent to patentability." The Office is accordingly urged to request that the Patent Owner produce claim charts and other materials submitted to third parties sufficient to demonstrate the technical and claim construction positions taken by the Patent Owner.

In the claim charts the Patent Owner repeatedly asserts that the mere presence of a stack pointer "confirms the existence of a push down stack" as recited in the claims of the '890 patent. The Patent Owner argues that evidence of a stack pointer is sufficient to demonstrate the existence of an ALU that is coupled to the top register in a push down stack wherein the top two registers of the push down stack provide inputs to the ALU.

Turning to the MacGregor reference, if one accepts the Patent Owner's argument then the system disclosed in MacGregor must contain a push down stack as recited in the claims of the '890 patent. Figure 1 of MacGregor *(p. 104)* shows a User Stack Pointer (A7) that is capable of storing and supplying operands to the ALU through the general purpose register file. The registers in the general purpose register file can act as top item and next item registers. Figure 2 of MacGregor *(p. 104)* similarly shows Interrupt and Master stack pointers. According to the Patent Owner, these stack pointers are indicative of the presence of a push down stack which meets the limitations recited in the claims of the '890 patent.

3. Claim Chart Demonstrating that MacGregor Anticipates Claims 1-5 and Renders Obvious Claims 6-10 of the '890 Patent

The following claim chart demonstrates in detail the correspondence between the elements in claims 1-10 and the MacGregor reference. The MacGregor reference *(Appendix D)* anticipates claims 1-5 of the '890 patent and in combination with other references renders obvious the remaining claims (i.e. claims 6-10).

Claim of the '890 patent	D. MacGregor et al. The Motorola MC68020, IEEE Micro, Vol. 4, issue 4, August 1984, pp.103-118
1. A microprocessor, which comprises a main central processing unit and	The Motorola MC68020 is a microprocessor system for processing instructions. MacGregor, p. 101: "The MC68020 represents the first successful extension of a 16-bit microprocessor into the 32-bit world" Fig. 2, p. 109:  Figure 2. Block diagram of the MC68020.
a separate direct memory access central processing unit in a single integrated circuit comprising said microprocessor,	MacGregor teaches that the bus of the MC68020 may optionally be coupled to a DMA device. (p. 107: "The reduced bus utilization by the MC68020 also increases system performance by providing more bus bandwidth for other bus masters such as DMA devices.") At the time of filing, DMA devices were conventionally on the same chip as the central processing unit. *(See, e.g., US Patent Nos. 4,783,764 (4:51-5:52); 4,989,113; (3:58-4:12); 4,558,176 (Col 15, Table II & 60:60-61:9); 4,885,785 (8:60-63, 10:3-8); 4,984,176 (18:41-43)).* Accordingly, one skilled in the art would have understood McGregor to teach the optional use of an on-chip DMA unit in connection with the disclosed central processing unit. Alternatively, Requestor submits that the DMA controllers were conventionally placed on the same chip as of the '890 patent's priority date and thus this feature would have been considered obvious by one skilled in the art. For example, United States Patent no. 4,783,764 to Tsuchiya et al. describes a Direct Memory Access controller on a single integrated circuit with a CPU that can be used with the MC68020. Tsuchiya teaches a processor which includes a CPU and a "mode exchange circuit 9" all on one chip. The

item register and a next item register, connected to provide inputs to said arithmetic unit (see Figs. 1 and 2 on page 104). The additional passages regarding the system described in MacGregor, pointed out in the Request for Reexamination in the claim chart on pages 11 though 15, are hereby incorporated by reference from the request for reexamination for their explanation of the teaching provided in MacGregor, which was not present in the prosecution of the application which became the '890 Patent. Further, there is a substantial likelihood that a reasonable examiner would consider this teaching important in deciding whether or not the claims are patentable. Accordingly, MacGregor raises a substantial new question of patentability as to independent claim 1, which question has not been decided in a previous examination of the '890 Patent. Further, because MacGregor is seen to raise an SNQ with respect to independent claim 1, the reference of MacGregor is additionally seen to raise an SNQ with respect to claims 2-10, which are each directly or indirectly dependent on claim 1, and which include each of the limitations of independent claim 1 by virtue of their dependency.

11. Continuing, with respect to the proposed SNQ#3, noted above, it is also agreed that the May reference in view of Tsuchiya raise a substantial new question of patentability as to independent claim 1 of the '890 Patent. The May reference describes a microprocessor (see Fig. 1) having an arithmetic logic unit connected to a push down stack register (see Fig. 2, A, B, and C registers). Further, as pointed out by the Third Party Requester, Tsuchiya describes a microprocessor further including a separate direct memory access central processing unit (see col. 4, line 51-col. 5, line 52). Thus, the combination, as proposed by the Third Party Requestor, would appear to teach the limitation that requires a microprocessor having the claimed

5. However, upon review of the references submitted in the Request for Reexamination, the examiner notes that the reference of the "Transputer Reference Manual", published by Inmos Ltd., 1988 (hereafter the "Transputer Manual"), is seen to describe an on-chip DMA controller. Thus, a rejection of independent claim 1 follows that utilizes the May'948 Patent, which incorporates by reference the reference of U.S. Patent Number 4,680,698, issued to Edwards *et al.* (hereafter the "Edwards'698 Patent"), and further in view of the "Transputer Reference Manual", published by Inmos Ltd., 1988 (hereafter the "Transputer Manual").

6. Further, also upon review of the references cited in the Request for Reexamination on page 11 (as well as pages 26 and 27) that teach of on-chip DMA controllers, the examiner notes that the reference of U.S. Patent 4,989,113, issued to Hull, Jr. *et al.* can be interpreted as teaching the other features that are required by the current claim language. Thus an additional rejection follows which utilizes this reference, and is discussed more fully below.

74(Amended). The microprocessor system of claim 73 wherein said one or more operational parameters [are included within the set consisting of:] include operating temperature of said substrate[,] or operating voltage of said substrate[, and fabrication process of said substrate].

78(Amended). In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon [a] an integrated circuit substrate, said central processing unit [including] being constructed of a first plurality of transistors and being operative at a processing frequency;

providing a variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors; and

clocking said central processing unit at a clock rate using [an oscillator, disposed upon said substrate, said oscillator being provided so as include a second plurality of transistors] variable speed clock with said central processing unit being clocked by said [oscillator] variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate.

Cancel claim 71.

REMARKS

Appreciation is expressed for the courteous and helpful telephone interview granted by the Examiner on January 7 and 8, 1997, with the undersigned attorney and Mr. George Shaw, representing the assignee of the application. The above changes to the claims are based on the discussion in the interview. Proposed changes to claims 19, 65 and 73 were sent by facsmile to the Examiner on January 7 to facilitate the further discussion on January 8. On January 8, the Examiner agreed that these changes merited further consideration of the application and appeared to overcome the prior art of record. The following remarks in part summarize the discussion in the interview and respond to specific points in the Final Rejection.

In the interview, the fact that operating characteristics of electronic devices in an integrated circuit will track one another depending on variations in the manufacturing process used to make the integrated circuit was discussed. This fact is described at page 31, line 1 through page 32, line 1 of this application, in the context of the microprocessor system of this invention. This fact is utilized in the present invention to provide a variable speed clock for the microprocessor, with the

clock speed varying in the same way as variations in the operating characteristics of the electronic devices making up the microprocessor. This allows the microprocessor to operate at its fastest safe operating speed, given its manufacturing process or changes in its operating temperature or voltage. In contrast, prior art microprocessor systems are given a rated speed based on possible worst case operating conditions and an external clock is used to drive them no faster than the rated speed. Under other than worst case operating conditions, the prior art microprocessors are actually capable of operating at a faster clock speed than their rated speed.

The above changes to the claims have been made to bring out the above distinction over the prior art more clearly. It is believed that they overcome the rejection of claims 19-21, 65-67 and 71-79 under 35 USC § 112, define statutory subject matter, i.e, a system implemented as a single integrated circuit having defined characteristics or a process, as well as distinguishing over the prior art of record.

In the rejection under 35 USC § 103, the Examiner contends that the Sheets reference "clearly indicates in lines 46-48 of column 2 that the system 100 shown in Figure 1 is fabricated *on a single chip* using MOS technology." Specific issue is taken with the inclusion of the italicized language in this characterization of the reference. Sheets does not say that the system 100 is on a single chip, only that it is implemented in MOS technology. At column 5, lines 15-17, a specific example of the Motorola 68000 microprocessor is given. That microprocessor is driven by an external clock that provides a clock signal to a designated pin of the microprocessor integrated circuit package. Applicants are aware of no prior art teaching or suggesting a variable speed oscillator in the same integrated circuit with a microprocessor and clocking the microprocessor with a clock speed that varies correspondingly with changes in operating characteristics of electronic devices making up the microprocessor, as a result of being in the same integrated circuit as the microprocessor, as claimed. Even if the Examiner is correct that the variable clock in Sheets is in the same integrated circuit as the microprocessor of system 100, that still does not give the claimed subject matter. In Sheets, a command input is required to change the clock speed. In the present invention, the clock speed varies correspondingly to variations in operating parameters of the electronic devices of the microprocessor because both the variable speed clock and the microprocessor are fabricated together in the same integrated circuit. No command input is necessary to change the clock frequency. The rejection under 35 USC § 103 is believed to be overcome.

Cir. 2006). This case presents a particularly compelling case for summary judgment because there is no material disagreement between TPL and HTC (or their respective experts) about how the accused HTC products operate. The facts required to establish entitlement to summary judgment were readily admitted or acknowledged by TPL's own expert. The Federal Circuit has repeatedly emphasized that such a case is particularly suited to summary judgment. *See, e.g., MyMail, Ltd. v. Am. Online, Inc.*, 476 F.3d 1372, 1378 (Fed. Cir. 2007).

IV. HTC DOES NOT INFRINGE THE '336 PATENT

The purported "problem" that the '336 patent was attempting to solve is reflected in at least two express limitations in every asserted claim: (1) the "entire" clock limitations and (2) the requirement that the speed of the clock or oscillator clocking the CPU be "varying" with the PVT parameters. Both of these limitations go to the core of the purported problem addressed by the '336 patent. TPL cannot show that the accused HTC products satisfy either of these claim limitations, literally or under the doctrine of equivalents.

The reason HTC does not infringe is straightforward: HTC's accused products did not adopt the "solution" described in the '336 patent. Those products, if anything, embrace the purported "problem" the '336 patent sought to solve. HTC's accused products, like the prior art, use a fixed speed clock that relies on an external crystal. And like the prior art, those products generate a stable and fixed clock signal frequency that exhibits only minimal variation based on a wide range of PVT parameters—the direct opposite of the system described in the '336 patent.

In summary, the HTC accused products, much like the prior art, rely on a fixed-frequency, crystal-based clocking system that intentionally excludes the purported benefit of varying frequency based on PVT parameters.

A. The Accused HTC Products Do Not Satisfy the "Entire" Limitations

Every independent claim of the '336 patent recites an "entire" ring oscillator, oscillator, or variable speed clock disposed on the same substrate as the CPU. These "entire" terms fall into the following three groups:

- "an entire ring oscillator variable speed system clock in said single integrated circuit" (claims 1, 11);

- "an entire oscillator disposed upon said integrated circuit substrate" (claims 6, 13); and
- "an entire variable speed system clock disposed upon said integrated circuit substrate" (claims 10, 16).

To convince the examiner to allow their claims over invalidating prior art, as explained below, the applicants repeatedly and unambiguously told the PTO that their allegedly inventive microprocessor system did not rely on any external crystal or frequency generator of a fixed speed, and that their internal clock or oscillator speed is variable. Those clear statements and disclaimers must be reflected in the construction of the three "entire" terms. And because the only infringement theory proffered for those limitations relies on an interpretation that was expressly disclaimed, the Court should grant summary judgment of non-infringement.

1. The "Entire" Limitations Should Be Construed To Exclude Reliance on a Control Signal or an External Crystal/Clock Generator To Generate a Clock Signal

The first step in any infringement analysis is to construe the disputed language of the asserted claim. *Freedman Seating Co. v. Am. Seating Co.*, 420 F.3d 1350, 1356-57 (Fed. Cir. 2005). Judge Ware construed only one of the "entire" terms prior to his retirement. As the Federal Circuit has observed, "district courts may engage in a rolling claim construction, in which the court revisits and alters its interpretation of the claim terms as its understanding of the technology evolves." *Pressure Prods. Med. Supplies, Inc. v. Greatbatch Ltd.*, 599 F.3d 1308, 1316 (Fed. Cir. 2010). This Court should now address all three "entire" limitations together and, as explained below, should adopt the construction adopted by Judge Gildea for all three terms.[3] Because the construction of the "entire" limitations is fundamental to the question of infringement, the Court should resolve this issue now. *See O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008) ("When the parties present a fundamental dispute regarding the scope of a claim term, it is the court's duty to resolve it.").

[3] Although HTC believes that this Court should apply Judge Gildea's consistent constructions across all three "entire" terms, as explained in Part IV.A.2, below, summary judgment of non-infringement of claims 10 and 16 would also be warranted under Judge Ware's construction of the single "entire" term that he construed from those claims.

HTC has proposed a set of consistent and parallel constructions of the three "entire" terms as set forth below:

Claim Term from the '336 Patent	HTC's Proposed Construction (Also Adopted by Judge Gildea)
an entire ring oscillator variable speed system clock in said single integrated circuit (claims 1, 11)	a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an external crystal/ clock generator to generate a clock signal
"an entire oscillator disposed upon said integrated circuit substrate" (claims 6, 13)	an oscillator that is located entirely on the same semiconductor substrate as the central processing unit and does not rely on a control signal or an external crystal/ clock generator to generate a clock signal
"an entire variable speed system clock disposed upon said integrated circuit substrate" (claims 10, 16)	a variable speed clock that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an external crystal/ clock generator to generate a clock signal

The key component of HTC's proposal is that each of the "entire ring oscillator," "entire oscillator," and "entire variable speed system clock" does not "rely on a control signal or an external crystal/ clock generator to generate a clock signal." This requirement captures the clear disclaimers made by the applicants during the prosecution of the '336 patent and is consistent with the specification's teachings and its criticisms of the prior art. This issue goes to the heart of this case as every accused '336 product includes an off-chip, fixed speed crystal that controls the frequency of the alleged on-chip clock or oscillator. Because the applicants clearly and unambiguously disclaimed on-chip oscillators and clocks that rely on external off-chip crystals and off-chip clock generators, HTC's proposed constructions should be adopted.

a. The Specification Describes the Importance of a Variable Speed Clock that Does Not Rely on an External Crystal or External Frequency Generator

One of the key features recited in the claims is the requirement that the "entire" variable speed clock or oscillator be located on the same integrated circuit substrate as the CPU that it clocks. The specification makes clear that, as a consequence of locating both the variable speed clock or oscillator and the CPU on the same substrate, the speed of such clock or oscillator will

vary based on the PVT (process, voltage, and temperature) parameters to which the integrated circuit is then subjected. ('336, 16:59-60, 65-67, 17:5-10, 19-22.) Performance of the CPU is thereby allegedly optimized such that the "CPU **70** will always execute at the maximum frequency possible, but never too fast." ('336, 16:67-17:2.)

In doing so, the specification describes an alleged improvement over the prior art solution of clocking a CPU with a fixed clock whose frequency is controlled by an external fixed speed crystal or clock generator. As the specification explains, this fixed speed clock is always set at a frequency well below the maximum theoretical frequency at which the CPU can operate under optimal PVT parameters because, by definition, a fixed speed clock cannot vary its speed with the PVT parameters. ('336, 16:44-53.) This setting is necessary to account for times when the CPU is operating under the worst-case PVT parameters. (*Id.*) But according to the '336 patent, setting the frequency at this lower level is inefficient. (*Id.*)

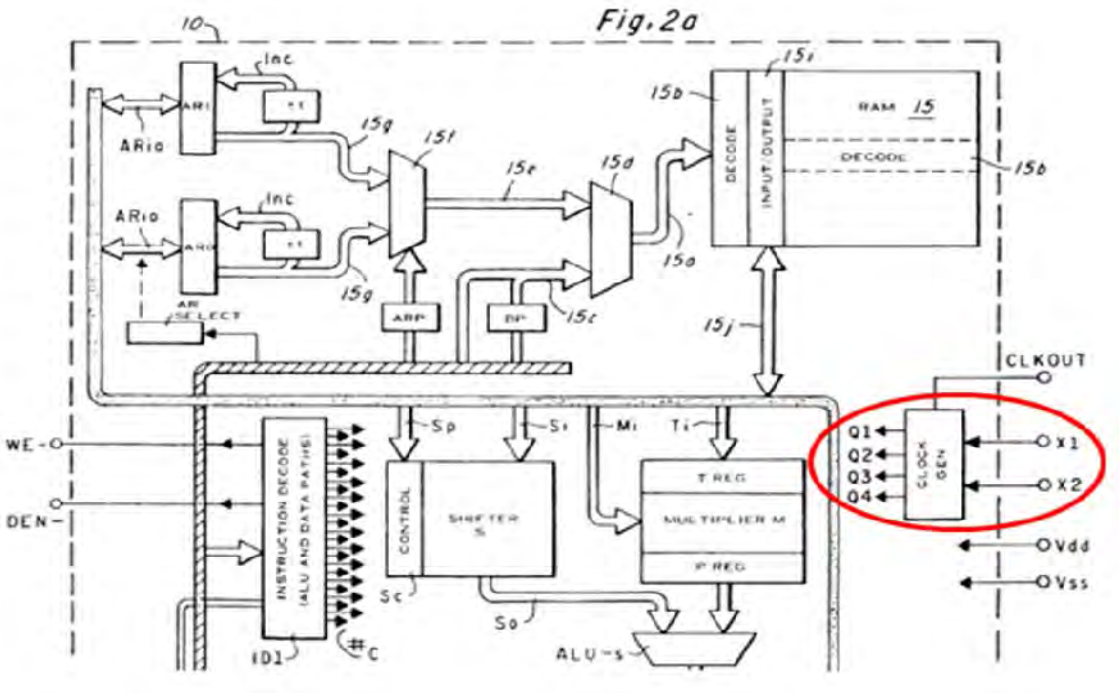
The claimed invention thus seeks to overcome this alleged inefficiency by fabricating the CPU and its clock entirely on the same substrate so that the PVT parameters affect both the CPU and the clock in the same way, without the CPU clock being controlled by an external fixed speed clock source. (*Id.* at 16:44-17:10, 19-22.) As a result, the CPU and clock's respective frequencies automatically vary in response to changes in the PVT parameters. (*Id.*)

b. The Applicants Repeatedly Disclaimed Reliance on External Crystals and External Frequency Generators

During the original prosecution of the '336 patent, the applicants repeatedly distinguished their purported invention from the prior art on the basis that their on-chip clock and on-chip oscillator do not rely on an external crystal or an external frequency generator. In doing so, the applicants clearly and unambiguously disclaimed any clock or oscillator, even though fabricated on the same substrate as the CPU, that relies on an external crystal or frequency generator.

Specifically, during the original prosecution, the PTO issued a non-final rejection based on U.S. Patent No. 4,503,500 to Magar ("Magar"), Fig. 2a of which is reproduced below. (Chen Decl. Ex. 5 ('336 prosecution history, Apr. 3, 1997 rejection) (TPL85300002433-34).) In his rejection, the examiner asserted that the "CLOCK GEN" (clock generator) circuitry in Fig. 2a of

Magar was fabricated on the same microprocessor substrate 10 as the CPU, as required by the claims. (*Id.* at 2 (TPL85300002434).) *See* Magar, Fig. 2a reproduced below (red circle added).



In response, the applicants attempted to distinguish Magar on the basis that an external off-chip crystal (connected to the X1 and X2 inputs in the figure above) drove the clock in Magar:

> A review of the Magar reference shows that it is apparently no more pertinent than prior art acknowledged in the application, in that ***the clock disclosed in the Magar reference is in fact driven by a fixed frequency crystal, which is external to the Magar integrated circuit.***

(Chen Decl. Ex. 6 ('336 prosecution history, July 7, 1997 Amendment) at 2 (emphasis added) (TPL85300002426).) The applicants further emphasized the difference between the claimed variable speed clock and Magar's clock generator's reliance on the frequency of an external crystal:

> Contrary to the Examiner's assertion in the rejection that 'one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock vary together due to manufacturing variation, operating voltage and temperature of the IC [integrated circuit],' one of ordinary skill in the art should readily recognize that the speed of the CPU and clock ***do not*** vary together due to manufacturing variation, operating voltage, and temperature of the IC in the Magar processor . . . ***This is simply because the Magar microprocessor clock is frequency controlled by a crystal which is also external to the microprocessor. Crystals are by design fixed frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating***

> ***voltage and temperature. The Magar microprocessor in no way contemplates a variable speed clock as claimed.***

(*Id*. at 3-4 (second emphasis added) (TPL85300002427-28).) Through these exchanges, the applicants unambiguously disclaimed clocks and oscillators that rely on an external crystal for frequency control.

The PTO subsequently issued a second rejection based on Magar. In response, the applicants amended their claims to explicitly require that ***the entire*** oscillator/clock be on the same integrated circuit substrate as the CPU.[4] (Chen Decl. Ex. 7 ('336 prosecution history, Feb. 10, 1998 Amendment) at 1-2 (TPL85300002399-400).) Along with this amendment, the applicants again tried to distinguish Magar from the claimed invention, arguing that Magar's clock generator could not operate properly without the use of an external component such as a crystal. In doing so, the applicants directed the examiner to Magar's disclosure at 15:26-27, which states that "chip 10 includes a clock generator 17 which has two external pins X1 and X2 to which a crystal (or external generator) is connected." (*Id.* at 4 (TPL85300002402).) The applicants then, consistent with their earlier statements, further distinguished an external crystal by stating:

> [W]hile most of Magar's clock (generator) circuitry is on the IC, ***the entire oscillator, which because it requires an external crystal, is not***.

(*Id*. at 4 (emphasis added) (TPL85300002402).) The applicants reinforced their disclaimers by identifying "the essential difference" between Magar's fixed-frequency clock and the variable speed clock of the '336 patent—that Magar's clock relies on an external crystal while the frequency of the '336 clock (in Figure 18) is determined by PVT parameters:

> The signals PHASE 0, PHASE 1, PHASE 2 and PHASE 3 in Applicants' Fig. 18 are synonymous with Q1, Q2, Q3 and Q4 depicted in Magar Fig. 2a. The ***essential difference*** is that the ***frequency or rate of the PHASE 0, PHASE 1, PHASE 2 and PHASE 3 signals is determined by the processing and/or***

---

[4] Then pending claim 19 was amended to recite "an entire ring oscillator variable speed system clock in said single integrated circuit," claim 73 was amended to recite "an entire oscillator disposed upon said integrated circuit substrate," and claim 78 was amended to recite "an entire variable speed clock disposed upon said integrated circuit substrate." (Chen Decl. Ex. 7 ('336 prosecution history, Feb. 10, 1998 Amendment) at 1-2.)

> ***operating parameters of the integrated circuit*** containing the Fig. 18 circuit, ***while the frequency or rate of the Q1, Q2, Q3 and Q4 signals depicted in Magar Fig. 2a are determined by the fixed frequency of the external crystal*** connected to the circuit portion outputting the Q1, Q2, Q3 and Q4 signals shown in Magar Fig. 2a.

(*Id.* (emphasis added).) The applicants concluded their argument about Magar by specifically distinguishing their claimed system from an external crystal used for frequency control or oscillation:

> The Magar teaching . . . is specifically distinguished from the instant case in that it is both fixed frequency (being crystal based) and ***requires an external crystal or external frequency generator***.

(*Id.* at 5 (emphasis added) (TPL85300002403).)

The applicants' statements to the PTO made clear that the alleged invention requires an "entire" on-chip clock or "entire" oscillator that does not rely on an external crystal or external frequency generator. Magar's clock generator was repeatedly distinguished as not disclosing the claimed "entire" clock because Magar's clock generator relies on an external crystal or external frequency generator. The claimed "entire" clocks and "entire" oscillators cannot therefore be construed to encompass reliance on an external crystal or external frequency generator. *See Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319, 1325 (Fed. Cir. 2002) ("Explicit arguments made during prosecution to overcome prior art can lead to a narrow claim interpretation because '[t]he public has a right to rely on such definitive statements made during prosecution.'"); *Am. Piledriving Equip. v. Geoquip, Inc.*, 637 F.3d 1324, 1336 (Fed. Cir. 2011) ("[A]n applicant's argument that a prior art reference is distinguishable on a particular ground can serve as a disclaimer of claim scope even if the applicant distinguishes the reference on other grounds as well.").[5]

---

[5] The patentee's disclaimers are also consistent with testimony from the named inventors describing their alleged invention. Although inventor testimony is not part of the intrinsic record, it may be used to "provide background information, including explanation of the problems that existed at the time the invention was made and the inventor's solution to these problems." *Voice Techs. Group, Inc. v. VMC Sys., Inc.*, 164 F.3d 605, 615-16 (Fed. Cir. 1999). In this case, inventor Charles Moore testified that the variable speed clock of the alleged invention would not be connected, directly or indirectly, to a crystal oscillator. (Chen Decl. Ex. 8 (Moore E.D. Tex. Depo.) at 23:15-17 (TPL8531710898).) The other named inventor, Russell Fish, III, agreed. (Chen Decl. Ex. 4 (Fish ITC Depo.) at 201:2-9.) Mr. Fish also testified that the presence of inputs into the variable speed clock or oscillator would indicate a system that did not include the '336 clock. (*Id.* at 83:14-84:12.)

c. The Applicants Also Repeatedly Disclaimed Reliance on Control Signals To Control the Clock

In addition to disclaiming reliance on an external crystal or clock generator, the applicants also disclaimed reliance on control signals to control the clock or oscillator. The first of these disclaimers occurred in response to the examiner's rejection of the claims in light of U.S. Patent No. 4,670,837 to Sheets ("Sheets"). In attempting to overcome Sheets, the applicants distinguished microprocessors that rely on frequency control information from an external source:

> ***The present invention does not similarly rely upon provision of frequency control information to an external clock***, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit ***obviates the need for provision of the type of frequency control information described by Sheets . . . Sheets' system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention***.

(Chen Decl. Ex. 9 ('336 prosecution history, Apr. 15, 1996 Amendment) at 8 (emphasis added) (TPL85300002473).) In response to a subsequent rejection based on Sheets, the applicants went even further and disclaimed the use of controlled oscillators altogether, regardless of whether the control is on-chip or not:

> Even if the examiner is correct that the variable clock in Sheets is in the same integrated circuit as the microprocessor of system **100,** ***that still does not give the claimed subject matter.*** In Sheets, a command input is required to change the clock speed.

(Chen Decl. Ex. 10 ('336 prosecution history, January 8, 1997 Amendment) at 4 (emphasis added) (TPL85300002449).)

Simply having a CPU clock on the chip was not enough, according to the applicants, to meet the claimed invention because controlling the on-chip ring oscillator's speed using a command signal "does not give the claimed subject matter." (*Id.*) Indeed, in response to a subsequent rejection based on Magar, the applicants left no doubt that, unlike "all cited references," the on-chip clock or on-chip oscillator of their purported invention is completely free of inputs and extra components:

> Crucial to the present invention is that . . . when the fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together. ***This differs from all cited references in that . . . the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so.***

(Chen Decl. Ex. 6 ('336 prosecution history, July 7, 1997 Amendment) at 5 (emphasis added) (TPL85300002429).) This prosecution statement confirms the applicants' clear disclaimer of any reliance on input control signals. Accordingly, HTC's proposed constructions include the requirement that the clock or oscillator "does not rely on . . . a control signal to generate a clock signal," and should be adopted.

d. HTC's and Judge Gildea's Construction Is Consistent with the Previous Construction by Judge Ward and TPL's Positions in this Litigation

Judge Gildea is not the only judge who has found that the applicants disclaimed an on-chip clock that relies on a control signal or an external crystal or clock generator to generate a clock signal.[6] The '336 patent was also the subject of prior litigation in the Eastern District of Texas before Judge Ward. *See Tech. Props. Ltd. v. Matsushita Elec. Indus. Co., Ltd.*, 514 F. Supp. 2d 916 (E.D. Tex. 2007). Judge Ward construed an "entire ring oscillator variable speed system clock in said single integrated circuit" of claim 1 as "a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not directly rely on a command input control signal or an external crystal/clock generator to generate a clock signal." *Id.* at 926. Judge Ward explained: "The Court agrees with the defendants that the applicant disclaimed the use of an input control signal and an external crystal/clock generator to generate a clock signal." *Id.* (emphasis added).[7]

---

[6] The ITC Staff Attorney Whitney Winston, a graduate from the Massachusetts Institute of Technology, in this parallel ITC investigation also agrees that HTC's proposed constructions "accurately capture the patentee's clear disclaimer." (Chen Decl. Ex. 11 (02/08/2013 OUII Opening Markman Brief) at 9.)

[7] Judge Ward's construction largely mirrors the construction adopted by Judge Gildea and proposed by HTC. The only differences are that Judge Gildea did not include certain language from Judge Ward's construction ("*directly* rely upon," "*command input* control signal"). Accordingly, while Judge Ward's prior claim construction correctly recognized the applicant's disclaimers regarding reliance on an external crystal/clock generator or control signal, the

TPL itself acknowledged this disclaimer by repeatedly urging this Court to adopt Judge Ward's construction—in at least three claim construction briefs filed with this Court. (*See* Doc. No. 228 at 18 (12/09/2010 TPL Claim Construction Brief); Doc. No. 258 at 18 (02/11/2011 TPL Claim Construction Brief); Doc. No. 339 at 19 (12/23/2011 TPL Claim Construction Brief).) During the ITC case, however, TPL retreated from its long-standing position and sought a different construction. (Chen Decl. Ex. 3 (04/18/2013 Public ITC Order) at 20.)

2. The HTC Accused Products Do Not Meet the "Entire" Limitations as a Matter of Law

After the relevant claim language has been construed, the second step in an infringement analysis is to compare the accused product with the claim as construed by the Court. *See Freedman Seating Co.*, 420 F.3d at 1357. TPL can present no evidence to raise a genuine issue of material fact as to whether the accused HTC products rely on an external crystal or clock to generate a clock signal for the CPU. As shown below, there can be no infringement because the accused HTC products operate in precisely the same manner as the prior art distinguished during prosecution—they rely on an external crystal or clock to generate a clock signal.

According to TPL's expert, the on-chip clock that TPL contends meets the "entire" limitations on all of the accused HTC products is based on a structure known as a "phase-locked loop" ("PLL"). TPL contends that the PLLs in the accused HTC products include either a voltage-controlled oscillator ("VCO") or a current-controlled oscillator ("ICO"). (*See* Chen Decl. Ex. 12 (Oklobdzija 07/13/2013 Depo.) at 56:13-57:23.) These VCOs or ICOs, according to TPL's expert, "directly clock the CPU." (*Id.* at 57:5-9.)

The problem with TPL's infringement theory, however, is that the oscillators in the accused products indisputably rely on an external crystal or clock generator to clock the CPU. Similar to a "cruise control" in an automobile that maintains a constant speed, the PLLs and their VCOs and ICOs in the accused HTC products maintain a stable CPU frequency. (Declaration of

---

"directly" and "command input" qualifiers in that construction should not be adopted here because there is no support for that specific language from the intrinsic record.

Thomas A. Gafford ("Gafford Decl.") Ex. 1 (Gafford 07/02/2013 Non-Infringement Rep.), ¶ 149.) The PLLs accomplish this stability by relying on an input signal from an external signal, known as a "reference" signal, that provides a fixed and stable frequency. (Chen Decl. Ex. 12 (Oklobdzija 07/13/2013 Depo.) at 57:10-15, 57:24-58:18; Chen Decl. Ex. 14 (Oklobdzija 06/04/2013 Infringement Rep.), ¶ 91 ("That other reference frequency is usually produced externally to the chip and that oscillator is encapsulated in a noise free, temperature and voltage controlled environment assuring the frequency stability of the reference signal.").)

All of the PLLs in the HTC accused products receive this external "reference" signal, according to TPL's expert, from either an external crystal or an external clock generator. (*See* Chen Decl. Ex. 12 (Oklobdzija 07/13/2013 Depo.) at 58:14-18.) In the words of TPL's expert, "they all must have a reference. That's essential part of PLL." (*Id*.; *see also id*. at 59:3-7 ("[I]t's the nature of PLL that must receive a reference. Now, that reference can be either an external clock generator or external crystal. In both cases the reference is external.").)

This "reference" signal directly controls the frequency of the on-chip oscillator. In particular, the PLL circuitry on the chip takes the external reference signal and "multiplies" it by a constant value to obtain a higher frequency. (Chen Decl. Ex. 14 (Oklobdzija 06/04/2013 Infringement Rep.), ¶ 91.) For example, in the accused Qualcomm MSM7x30 chip, a PLL clocks the CPU at a fixed speed of 768 MHz. The PLL circuitry on the chip obtains this frequency by taking the reference frequency from the external crystal—19.2 MHz—and multiplying it by 40. A PLL maintains this fixed frequency by constantly comparing the frequency of the oscillator to the crystal frequency, and correcting the oscillator frequency such that it remains a constant multiple of the reference frequency supplied by the crystal. (Gafford Decl. Ex. 1 (Gafford 07/02/2013 Non-Infringement Rep.), ¶ 40*; see also* Chen Decl. Ex. 14 (Oklobdzija 06/04/2013 Infringement Rep.), ¶ 122 ("The reference clock provides the timing reference used by the PLL. The PLL uses this reference to calibrate its own ring oscillator VCO, which generates the clock signal.").) The frequency of the on-chip clock in the accused HTC products, therefore, directly depends on the frequency of the external crystal.

HTC's expert, Mr. Gafford, was also able to empirically confirm that the accused HTC products rely on an external crystal/clock generator. (Gafford Decl. Ex. 1 (Gafford 07/02/2013 Non-Infringement Rep..), ¶¶ 110-15, 203-09.) He ran a series of tests on certain HTC accused products in which he was able to increase or decrease the reference frequency and measure its effect on the frequency produced by the PLL. (*Id.*) His testing showed a linear relationship between the reference frequency and the frequency of the on-chip PLL—if you increase the frequency of the reference signal, for example, the frequency of the on-chip PLL increases. (*Id.* ¶¶ 204-09.) And if you decrease the frequency of the reference signal, the frequency of the on-chip PLL decreases in direct response. (*Id.*) TPL's expert testified that he was "not surprised" with Mr. Gafford's results. (*See* Chen Decl. Ex. 12 (Oklobdzija 07/13/2013 Depo.) at 126:12-127:7.) Nor should he have been surprised because "in general it's true if we have a PLL as we have described that depends on the reference[, a]nd so if the reference is affected, then the output frequency will be affected as well." (*Id.* at 84:17-22). And these results were not surprising given that the accused phones were *designed* to maintain a fixed and stable frequency based on the crystal reference.

Non-infringement would also be warranted even if the Court applied Judge Ware's construction of "an entire variable speed system clock" as to claims 10 and 16, which he construed as "a variable speed clock that is located ***entirely*** on the same semiconductor substrate as the central processing unit." (Doc. No. 364, at 19 (emphasis added).) As explained previously, the PLL and the external crystal are inextricably intertwined components of the clocking mechanism for the CPU. Because it is undisputed that the crystal is not on the same semiconductor substrate as the accused oscillator, TPL cannot show that the clock is located entirely on the same substrate as required under Judge Ware's construction. As the applicants emphasized in discussing the "entire" terms in the '336 patent during the original prosecution, "while most of Magar's clock (generator) circuitry is on the IC, the entire oscillator, which because it requires an external crystal, is not." (Chen Decl. Ex. 7 ('336 prosecution history, Feb. 10, 1998 Amendment) at 4 (emphasis added) (TPL85300002402).)

A finding of non-infringement, as noted previously, is entirely consistent with the prosecution history in which the applicant argued that Magar was "distinguished from the instant case in that it is both fixed frequency (being crystal based) and ***requires an external crystal or external frequency generator***." (*Id.* at 5 (TPL85300002403).) "Claims may not be construed one way in order to obtain their allowance and in a different way against accused infringers." *Southwall Techs., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995). For all of these reasons, therefore, TPL cannot establish infringement of the '336 patent, literally or under the doctrine of equivalents, as a matter of law.

B. <u>The Accused HTC Products Also Do Not Satisfy the "Varying" Limitations as a Matter of Law</u>

The accused HTC products do not infringe for another reason that is separate from the "entire" limitations discussed above. Each independent claim of the '336 patent requires that the variable speed clock or oscillator be "varying" based on the PVT parameters as follows:

Claim Term from the '336 Patent (in Underlining with Surrounding Language)
"a processing frequency capability of said central processing unit and ***<u>a speed of said</u>*** ring oscillator variable speed system ***<u>clock varying</u>*** together ***<u>due to said manufacturing variations and due to at least operating voltage and temperature</u>*** of said single integrated circuit" (claims 1, 11)
"***<u>varying</u>*** the processing frequency of said first plurality of electronic devices and ***<u>the clock rate</u>*** of said second plurality of electronic devices in the same way ***<u>as a function of parameter variation in one or more fabrication or operational parameters</u>*** associated with said integrated circuit substrate" (claims 6, 13)
"said processing frequency and ***<u>said clock rate varying</u>*** in the same way ***<u>relative to said variation in said one or more fabrication or operational parameters</u>*** associated with said integrated circuit substrate" (claims 10, 16)

As shown in the chart above, the requirement may be stated in slightly different language in the independent claims, but the underlying requirement is the same—the speed or clock rate of the claimed variable speed clock or oscillator must be "varying" with the PVT parameters.

Summary judgment is appropriate because TPL has offered no evidence whatsoever to show that the claimed "clock" or "oscillator" is "varying" with the PVT parameters as recited in

PATENT

NANO-001/05US
N0765-2008

I hereby certify that this paper correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Date: 4/19/96 By: Felicia Walker

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Charles H. Moore et al.

Serial No. 08/484,918

Filed: June 7, 1995

For: HIGH PERFORMANCE, LOW COST MICROPROCESSOR

Examiner: D. Eng

Art Unit: 2315

AMENDMENT

Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Amendment is being submitted in response to the first Office Action in the above-identified patent application.

IN THE SPECIFICATION

At page 1, line 1, please change the title from "HIGH PERFORMANCE, LOW COST MICROPROCESSOR" to --HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK--.

110 JF 04/18/96 08484918 1 202 39.00 CK

21092053

Please rewrite the Abstract as follows:

--A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.--

IN THE CLAIMS

Please amend claims 19-20 and 65-66 as follows:

19(Amended). A microprocessor system, comprising a single integrated circuit including a central processing unit and a ring [counter] oscillator variable speed system clock connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring [counter] oscillator variable speed system clock [being provided in a single integrated circuit] each including a plurality of electronic devices of like type, said central processing unit operating at a variable processing frequency dependent upon a variable speed of said ring oscillator variable speed system clock.

20(Amended). The microprocessor system of Claim 19 additionally comprising an input/output interface connected to exchange coupling control signals, address and data with said [input/output interface] central processing unit, and a second clock independent of said ring [counter] oscillator variable speed system clock connected to said input/output interface.

65(Amended). In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:

Case5:08-cv-00882-PSG Document457-16 Filed07/16/13 Page24 of 111

[which comprises fabricating] providing a ring [counter] oscillator system clock having a plurality of transistors within the integrated circuit, said plurality of transistors having operating characteristics disposed to vary similarly to operating characteristics of transistors included within the microprocessor; [and the microprocessor each having a plurality of transistors having operating characteristics which vary in the same way with variations in their fabrication,] and

using the ring [counter] oscillator system clock for clocking the microprocessor, said central processing unit operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock.

B3

66(Amended). The method of Claim 65 additionally comprising the steps of:

providing an input/output interface for the microprocessor integrated circuit, [and]

clocking the input/output interface with a second clock independent of the ring [counter] oscillator system clock, and

buffering information within said input/output interface received from said microprocessor integrated circuit.

Please add the following new claims 71-79:

71. The microprocessor system of claim 20 further including system memory coupled to said input/output interface, said system memory being synchronized to said second clock and operating synchronously with respect to said ring oscillator variable speed system clock.

B4 Sub C3

72. The method of claim 65 further including the steps of:

transferring information to and from said microprocessor in synchrony with said ring oscillator system clock, and

buffering said information to facilitate transfer of said information to and from system memory synchronously with respect to said ring oscillator system clock.

73. A microprocessor system comprising:

21092053

a central processing unit disposed upon a substrate, said central processing unit operating at a processing frequency and including a first plurality of transistors;

an oscillator disposed upon said substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and including a second plurality of transistors designed such that operating characteristics of said first plurality and said second plurality of transistors vary in the same way as a function of parameter variation in one or more operational parameters associated with said substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation.//

74. The microprocessor system of claim 73 wherein said one or more parameters are included within the set consisting of: operating temperature of said substrate, operating voltage of said substrate, and fabrication process of said substrate.

75. The microprocessor system of claim 73 further comprising:

an input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, address and data with said central processing unit;

an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

~~76~~. The microprocessor system of claim ~~75~~ wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.

~~77~~. The microprocessor system of claim ~~73~~ wherein said oscillator comprises a ring oscillator.

78. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon a substrate, said central processing unit including a first plurality of transistors and being operative at a processing frequency;

clocking said central processing unit at a clock rate using an oscillator disposed upon said substrate, said oscillator being provided so as to include a second plurality of transistors with said central processing unit being clocked by said oscillator at a variable frequency dependent upon variation in one or more operational parameters associated with said substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more operational parameters associated with said substrate.

79. The method of claim 78 further comprising the steps of:

connecting an input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, address and data between said input/output interface and said central processing unit;

clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

REMARKS

This amendment responds to the first office action. Claims 19-20 and 65-66 have been amended, and new claims 71-79 have been added.

The Examiner has requested that applicants update the status of the parent application. Applicants note that the parent application Serial No. 07/389,334 has issued as U.S. Pat. No. 5,440,749. Also pursuant to the Examiner's request, a new title and new abstract more aptly descriptive of the invention have been provided.

The Examiner has rejected claims 19-21 and 65-67 under 35 U.S.C. § 112 as being indefinite. With respect to the apparatus claims, the Examiner asserted that there exists no functional relationship and interconnection between the claimed components. Similarly, the Examiner asserted that a functional relationship does not exist between the steps of the method claims, and that it is unclear what the steps try to accomplish.

Applicants note that the present invention is directed to a microprocessor system including a central processing unit and a ring oscillator variable speed system clock connected thereto. In accordance with the claimed invention, the central processing unit and the ring oscillator variable speed system clock are provided in a single integrated circuit. This allows, for example, the central processing unit to track variations in the speed of the ring oscillator variable speed system clock, since the elements of each are disposed in the same integrated circuit. By this amendment the term "ring counter" has been replaced with "ring oscillator", in order to more particularly identify the ring oscillator (FIG. 18) incorporated within a preferred implementation of the microprocessor system of the invention.

Although applicants submit that the "functional relationship" between the claimed central processing unit and system clock connected thereto is inherently clear, the apparatus and method claims have been amended in an effort to accommodate the Examiner's concerns with respect to 35 U.S.C. §112. For example, claim 19 now recites a "functional relationship" in that it is made explicit that the ring oscillator variable speed system clock is disposed to clock the central processing unit. Moreover, the central processing unit and ring oscillator variable speed system clock are described as "each including a plurality of electronic devices of like type". This allows the central processing unit to operate at a

variable processing frequency which depends upon a variable speed of the ring oscillator variable speed system clock. See, for example, the specification at page 31, line 33 to page 32, line 1:

> By deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast. For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor 50 will operate slower than normal. Since the microprocessor 50 *ring oscillator clock 430 is made from the same transistors on the same die as the latches and gates*, it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.

Method claim 65 has been similarly amended, and now recites the step of:

> fabricating a ring oscillator system clock having a plurality of transistors, said plurality of transistors having operating characteristics disposed to vary similarly to operating characteristics of transistors included within the microprocessor ... .

The method claims thus now prescribe a technique for clocking a microprocessor using a ring oscillator system clock comprised of transistors having similar operating characteristics as those within the microprocessor. This advantageously allows the processing frequency of the microprocessor to track the clock rate of the ring oscillator system clock.

The Examiner has rejected claims 19 and 65 under 35 U.S.C. § 103 as being unpatentable over Sheets. The Examiner stated that Sheets teaches a microprocessor system having a microprocessor and a variable speed clock generator. Although admitting that Sheets does not disclose that his clock is implemented using a ring oscillator, the Examiner opined that a "counter is a basis component of [a] clock generator". It was further asserted that choosing the counter to be of the ring type is merely a matter of design choice.

Applicants again observe that the present invention is directed to a system and method for clocking a central processing unit disposed *within the same integrated circuit* as a ring oscillator variable speed system clock. This allows, for example, the central processing unit to track variations in the speed of the ring oscillator variable speed system clock, since the elements of each are disposed in the same integrated circuit. That is, the operational speed of the microprocessor and ring oscillator clock are designed to vary similarly as a function of variation in temperature, processing and other parameters affecting circuit performance.

The system of Sheets effects microprocessor clocking in a way which is entirely dissimilar from that of the present invention, and in fact teaches away from Applicants' clocking scheme. In particular, Sheets describes the use of discrete, commercially available microprocessor chips, e.g., the Motorola 68000 (col. 5, line 16), driven by a separate clock (VCO 12 of FIG. 1). As is well known, such microprocessor chips include terminals or pins, such as the CLK and INT terminals of microprocessor (FIG. 1), for receiving inputs from external devices like the VCO 12 and fixed oscillator 103. Because the VCO 12 is not integral with the microprocessor 101, Sheets has proposed a technique for adjusting the frequency of VCO 12 in accordance with a desired operating frequency of the microprocessor 101. Specifically, a digital word indicative of this desired operating frequency is written by microprocessor 101 to VCO 12 by way of data bus 104 as a means of adjusting clock frequency.

The present invention does not similarly rely upon provision of frequency control information to an external clock, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, since the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance. Sheets' system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.

Although the foregoing clearly indicates the existence of a patentable distinction between the system of Sheets and the present invention, claims 19 and 65 have nonetheless been amended to advance prosecution of the application. Specifically, claims 19 and 65 now explicitly recite that the ring oscillator and microprocessor are provided within the same integrated circuit. Moreover, these claims further state that the plurality of transistors included within the ring oscillator clock have operating characteristics which vary similarly to operating characteristics of transistors included within the microprocessor, thereby enabling the processing frequency of the microprocessor to track the speed of the ring oscillator clock:

> ...The CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process.
> (page 32, lines 10-13)

Neither of these aspects of the present invention are suggested by Sheets. As discussed above, Sheets describes the use of commercially available microprocessor chips, and depicts the microprocessor 101 as being coupled to a separate clock (i.e, VCO 12) by way of a data bus 104 and address bus 105. Moreover, the VCO 12 clearly is not comprised of transistors having operating characteristics disposed to vary similarly to those of transistors within the microprocessor 101. Rather, the VCO 12 is seen to be comprised of an LC oscillator (col. 3, line 58 and FIG. 6), which clearly is not adapted to mimic variation in the speed of transistors within the microprocessor 101. Accordingly, applicant respectfully submits that amended claims 19 and 65 are patentable over Sheets, and requests that the rejection thereof under 35 U.S.C. § 103 be withdrawn.

Since Schaire does not supplement the lack of teaching within Sheets with respect to amended claims 19 and 65, it is also respectfully submitted that pending claims 20-21 and 66-67 are patentable over Sheets in view of Schaire. Further with regard to pending claims 20 and 66, it is observed that Schaire provides no indication that bus interface unit 10 is clocked by a signal from a clock different from that used to clock the host microprocessor. That is, the origin of high-speed clock signal 230 (FIG. 1) provided to bus interface unit 10 does not appear to be described. Hence, Schaire fails to teach the claimed provision of separate, independent clock signals to an input/output interface buffer and microprocessor. Accordingly, applicant respectfully requests that the outstanding rejection of claims 20-21 and 66-67 under 35 U.S.C. § 103 be withdrawn.

By this amendment new claims 71-79 have also been added to more particularly identify the invention which appears to be available for protection. In this regard new claims 71-72 point out that information is transferred to and from the microprocessor in synchrony with the ring oscillator system clock, and that this information is buffered to facilitate transfer thereof to and from system memory synchronously with respect to the ring oscillator system clock. New claims 73-79 explicitly recite that the central processing unit and ring oscillator include first and second pluralities of transistors, respectively, and that the

operating characteristics of these transistors vary in the same way as a function of variation in operational parameters (e.g., operating temperature) of the substrate. This advantageously allows a processing frequency of the central processing unit to track a clock rate of the ring oscillator as a function of substrate parameter variation.

Accordingly, in view of the above remarks, it is submitted that this application is now ready for allowance. Early notice to this effect is solicited.

If in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned at (415) 843-5000.

Respectfully submitted,

COOLEY GODWARD CASTRO
HUDDLESON & TATUM

By: _____
Willis E. Higgins
Reg. No. 23,025

Cooley Godward Castro
Huddleson & Tatum
Five Palo Alto Square
3000 El Camino Real
Palo Alto, CA 94306-2155
(415) 843-5000

01/13/97

PATENT

NANO-001/05US
N0765-2008

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on January 8, 1997.

Date: 1-8-97 By: Patricia K. Carey

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Charles H. Moore et al.

Serial No. 08/484,918

Filed: June 7, 1995

For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

Examiner: D. Eng

Art Unit: 2315

AMENDMENT

Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Amendment is being submitted in response to the Final Rejection dated July 8, 1996 in the above-identified patent application.

IN THE CLAIMS

Please amend claims 19, 65, 66, 71, 72, 73, 74 and 78 as follows:

19(Twice Amended). A microprocessor system, comprising a single integrated circuit including a central processing unit and a ring oscillator variable speed system clock connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices [of like type] correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit [operating at a variable processing frequency dependent upon a variable speed of] and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said integrated circuit.

65(Twice Amended). In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:

providing a ring oscillator system clock [having a plurality] constructed of [transistors] electronic devices within the integrated circuit, said [plurality of transistors] electronic devices having operating characteristics [disposed to] which will, because said ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary [similarly to] together with operating characteristics of [transistors] electronic devices included within the microprocessor; and

using the ring oscillator system clock for clocking the microprocessor, said [central processing unit] microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock.

66(Twice Amended). The method of Claim 65 additionally comprising the steps of:

providing an input/output interface for the microprocessor integrated circuit, and

clocking the input/output interface with a second clock independent of the ring oscillator system clock[, and

buffering information within said input/output interface received from said microprocessor integrated circuit].

72(Amended). The method of claim 65 further including the [steps] step of:

transferring information to and from said microprocessor in synchrony with said ring oscillator system clock[, and

buffering said information to facilitate transfer of said information to and from system memory synchronously with respect to said ring oscillator system clock].

73(Amended). A microprocessor system comprising:

a central processing unit disposed upon [a] an integrated circuit substrate, said central processing unit operating at a processing frequency and [including] constructed of a first plurality of [transistors] electronic devices;

an oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and including a second plurality of [transistors] electronic devices, thus varying the [designed such that] operating characteristics of said first plurality and said second plurality of transistors [vary] in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation.

74(Amended). The microprocessor system of claim 73 wherein said one or more operational parameters [are included within the set consisting of:] include operating temperature of said substrate[,] or operating voltage of said substrate[, and fabrication process of said substrate].

78(Amended). In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon [a] an integrated circuit substrate, said central processing unit [including] being constructed of a first plurality of transistors and being operative at a processing frequency;

providing a variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors; and

clocking said central processing unit at a clock rate using [an oscillator, disposed upon said substrate, said oscillator being provided so as include a second plurality of transistors] variable speed clock with said central processing unit being clocked by said [oscillator] variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate.

Cancel claim 71.

REMARKS

Appreciation is expressed for the courteous and helpful telephone interview granted by the Examiner on January 7 and 8, 1997, with the undersigned attorney and Mr. George Shaw, representing the assignee of the application. The above changes to the claims are based on the discussion in the interview. Proposed changes to claims 19, 65 and 73 were sent by facsmile to the Examiner on January 7 to facilitate the further discussion on January 8. On January 8, the Examiner agreed that these changes merited further consideration of the application and appeared to overcome the prior art of record. The following remarks in part summarize the discussion in the interview and respond to specific points in the Final Rejection.

In the interview, the fact that operating characteristics of electronic devices in an integrated circuit will track one another depending on variations in the manufacturing process used to make the integrated circuit was discussed. This fact is described at page 31, line 1 through page 32, line 1 of this application, in the context of the microprocessor system of this invention. This fact is utilized in the present invention to provide a variable speed clock for the microprocessor, with the

clock speed varying in the same way as variations in the operating characteristics of the electronic devices making up the microprocessor. This allows the microprocessor to operate at its fastest safe operating speed, given its manufacturing process or changes in its operating temperature or voltage. In contrast, prior art microprocessor systems are given a rated speed based on possible worst case operating conditions and an external clock is used to drive them no faster than the rated speed. Under other than worst case operating conditions, the prior art microprocessors are actually capable of operating at a faster clock speed than their rated speed.

The above changes to the claims have been made to bring out the above distinction over the prior art more clearly. It is believed that they overcome the rejection of claims 19-21, 65-67 and 71-79 under 35 USC § 112, define statutory subject matter, i.e, a system implemented as a single integrated circuit having defined characteristics or a process, as well as distinguishing over the prior art of record.

In the rejection under 35 USC § 103, the Examiner contends that the Sheets reference "clearly indicates in lines 46-48 of column 2 that the system 100 shown in Figure 1 is fabricated *on a single chip* using MOS technology." Specific issue is taken with the inclusion of the italicized language in this characterization of the reference. Sheets does not say that the system 100 is on a single chip, only that it is implemented in MOS technology. At column 5, lines 15-17, a specific example of the Motorola 68000 microprocessor is given. That microprocessor is driven by an external clock that provides a clock signal to a designated pin of the microprocessor integrated circuit package. Applicants are aware of no prior art teaching or suggesting a variable speed oscillator in the same integrated circuit with a microprocessor and clocking the microprocessor with a clock speed that varies correspondingly with changes in operating characteristics of electronic devices making up the microprocessor, as a result of being in the same integrated circuit as the microprocessor, as claimed. Even if the Examiner is correct that the variable clock in Sheets is in the same integrated circuit as the microprocessor of system 100, that still does not give the claimed subject matter. In Sheets, a command input is required to change the clock speed. In the present invention, the clock speed varies correspondingly to variations in operating parameters of the electronic devices of the microprocessor because both the variable speed clock and the microprocessor are fabricated together in the same integrated circuit. No command input is necessary to change the clock frequency. The rejection under 35 USC § 103 is believed to be overcome.

All of the claims in the application are believed to be patentable over the prior art. This application is believed to be in condition for allowance, and allowance is solicited.

Respectfully submitted,

COOLEY GODWARD LLP

Willis E. Higgins
Reg. No. 23,025

Five Palo Alto Square
Palo Alto, CA 94306-2155
Telephone: (415) 843-5145

United States Patent [19]

Magar

[11] **Patent Number: 4,503,500**

[45] **Date of Patent: Mar. 5, 1985**

[54] **MICROCOMPUTER WITH BUS INTERCHANGE MODULE**

[75] Inventor: **Surendar S. Magar**, Houston, Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **619,650**

[22] Filed: **Jun. 15, 1984**

Related U.S. Application Data

[63] Continuation of Ser. No. 347,860, Feb. 11, 1982.

[51] **Int. Cl.**[3] **G06F 3/00**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** 364/200, 900

[56] **References Cited**

U.S. PATENT DOCUMENTS

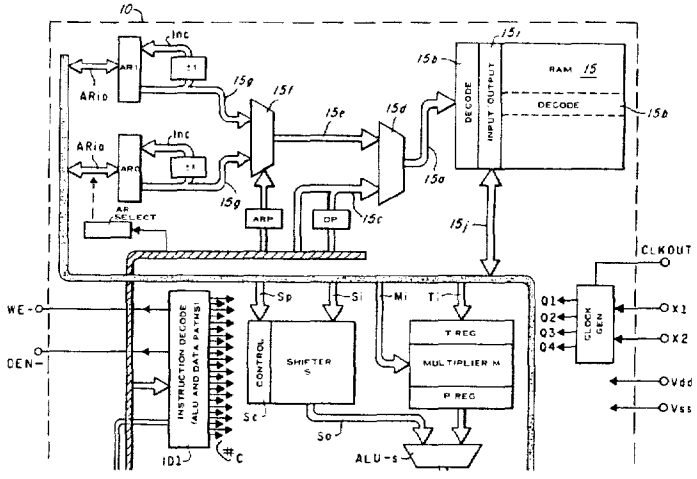
4,309,754	1/1982	Dinwiddie, Jr.	364/200
4,339,793	7/1982	Marenin	364/200
4,348,743	9/1982	Dozier	364/900
4,378,589	3/1983	Finnegan et al.	364/200

Primary Examiner—Gareth D. Shaw
Assistant Examiner—Ronni S. Malamud
Attorney, Agent, or Firm—John G. Graham

[57] **ABSTRACT**

A system for real-time digital signal processing employs a single-chip microcomputer device having separate on-chip program ROM and data RAM, with separate address and data paths for program and data. An external program address bus allows off-chip program fetch in an expansion mode, with the opcode returned by an external data bus. A bus interchange module allows transfer between the separate internal program and data busses in special circumstances. The internal busses are 16-bit, while the ALU and accumulator are 32-bit. A multiplier circuit produces a single state 16×16 multiply function separate from the ALU, with 32-bit output to the ALU. One input to the ALU passes through a 0-to-15 bit shifter with sign extension.

9 Claims, 15 Drawing Figures



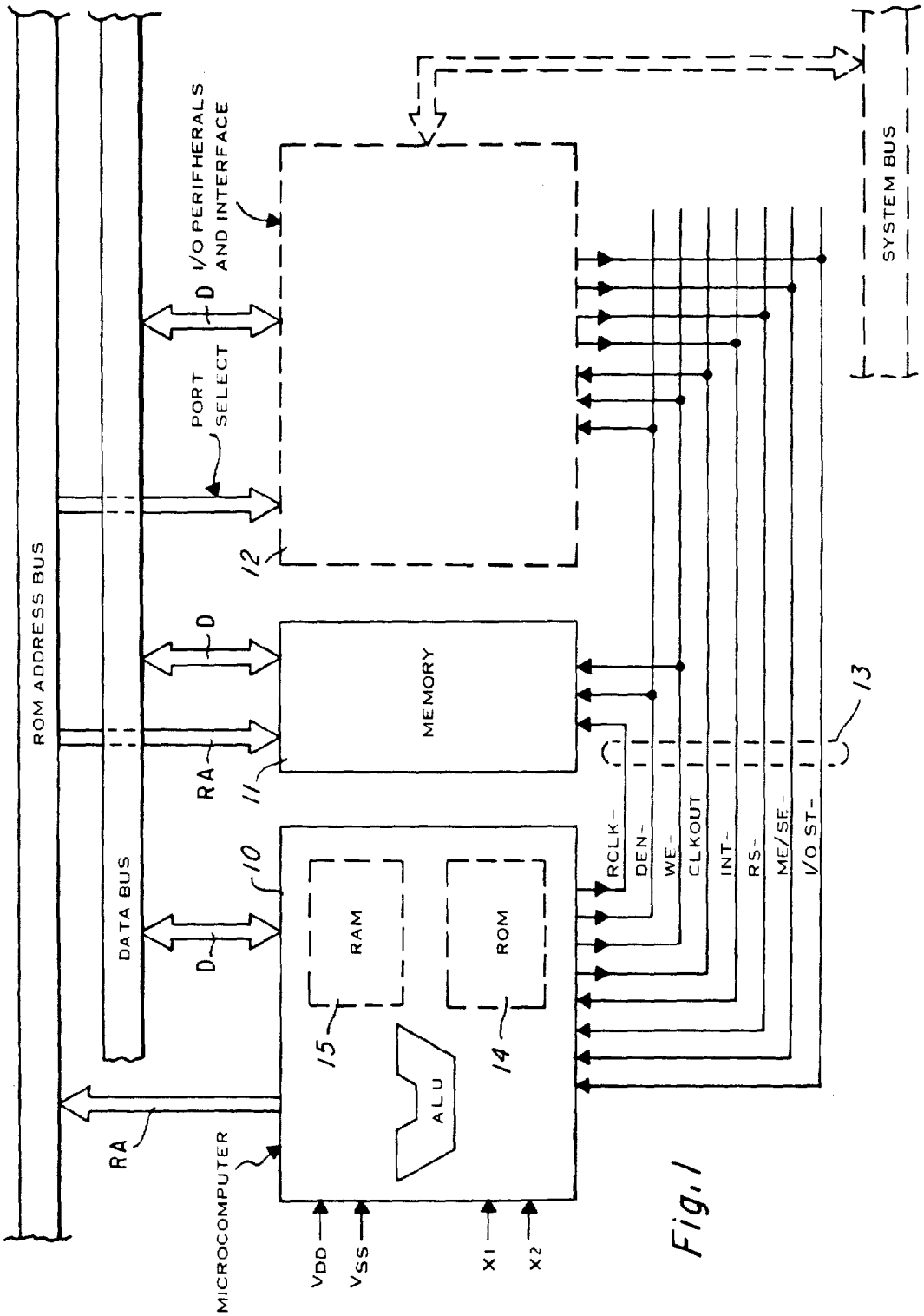
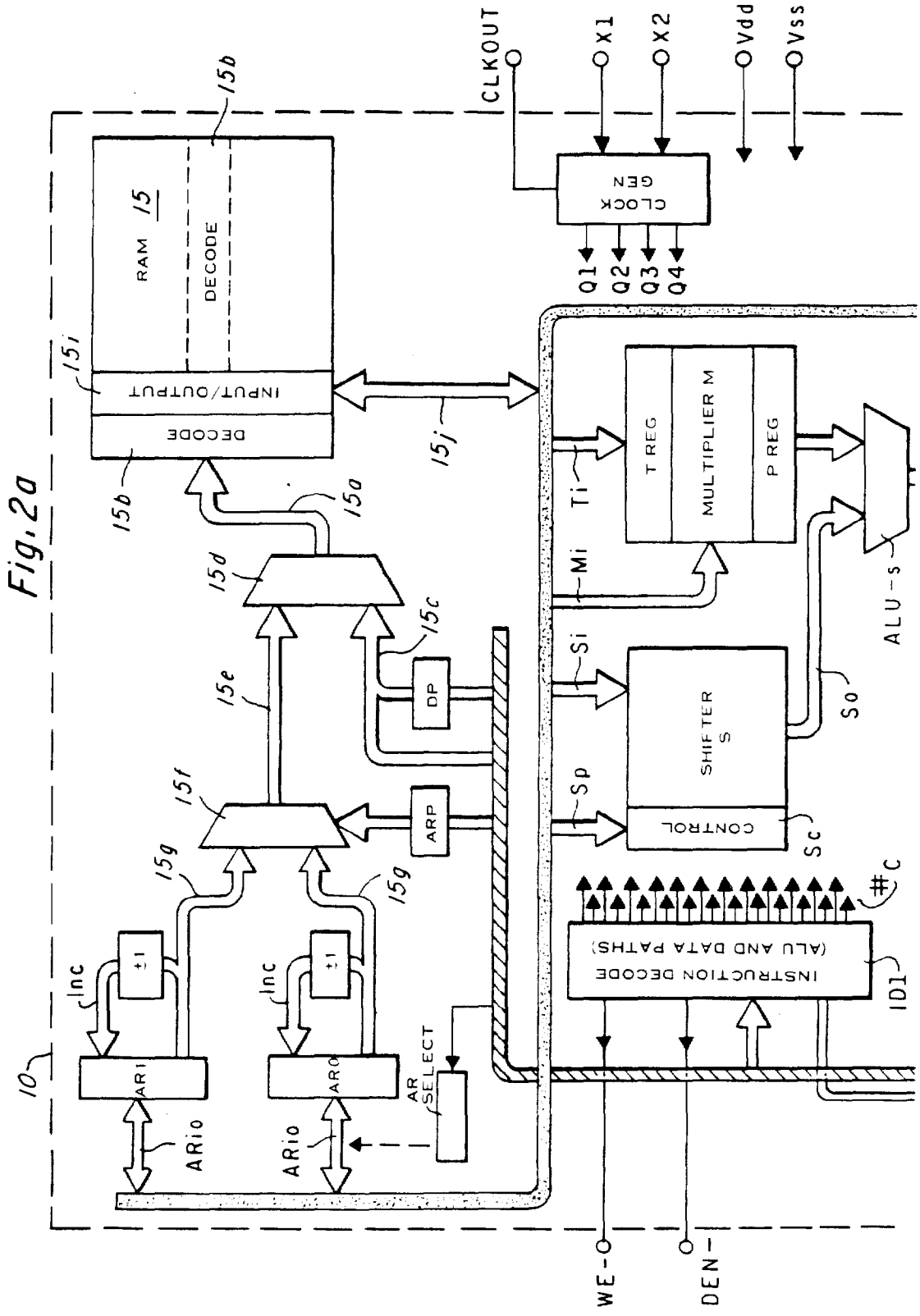

ROM ADDRESS BUS
DATA BUS
MICROCOMPUTER
I/O PERIFHERALS AND INTERFACE
PORT SELECT
SYSTEM BUS
MEMORY
RAM
ROM
ALU
RA
D
RCLK-
DEN-
WE-
CLKOUT
INT-
RS-
ME/SE-
I/O ST-
VDD
VSS
X1
X2
10
11
12
13
14
15

Fig. 1

Fig. 2a


CLKOUT
X1
X2
Vdd
Vss
CLOCK GEN
Q1
Q2
Q3
Q4
15b
RAM 15
DECODE
15i
INPUT/OUTPUT
DECODE
15j
15b
15a
15d
15c
15e
DP
15f
ARP
15g
15g
T REG
MULTIPLIER M
P REG
Ti
Mi
ALU-s
Si
SHIFTER S
So
Sp
CONTROL
Sc
#C
INSTRUCTION DECODE (ALU AND DATA PATHS)
ID1
INC
±1
INC
±1
10
AR1
AR0
AR SELECT
ARio
ARio
WE-
DEN-

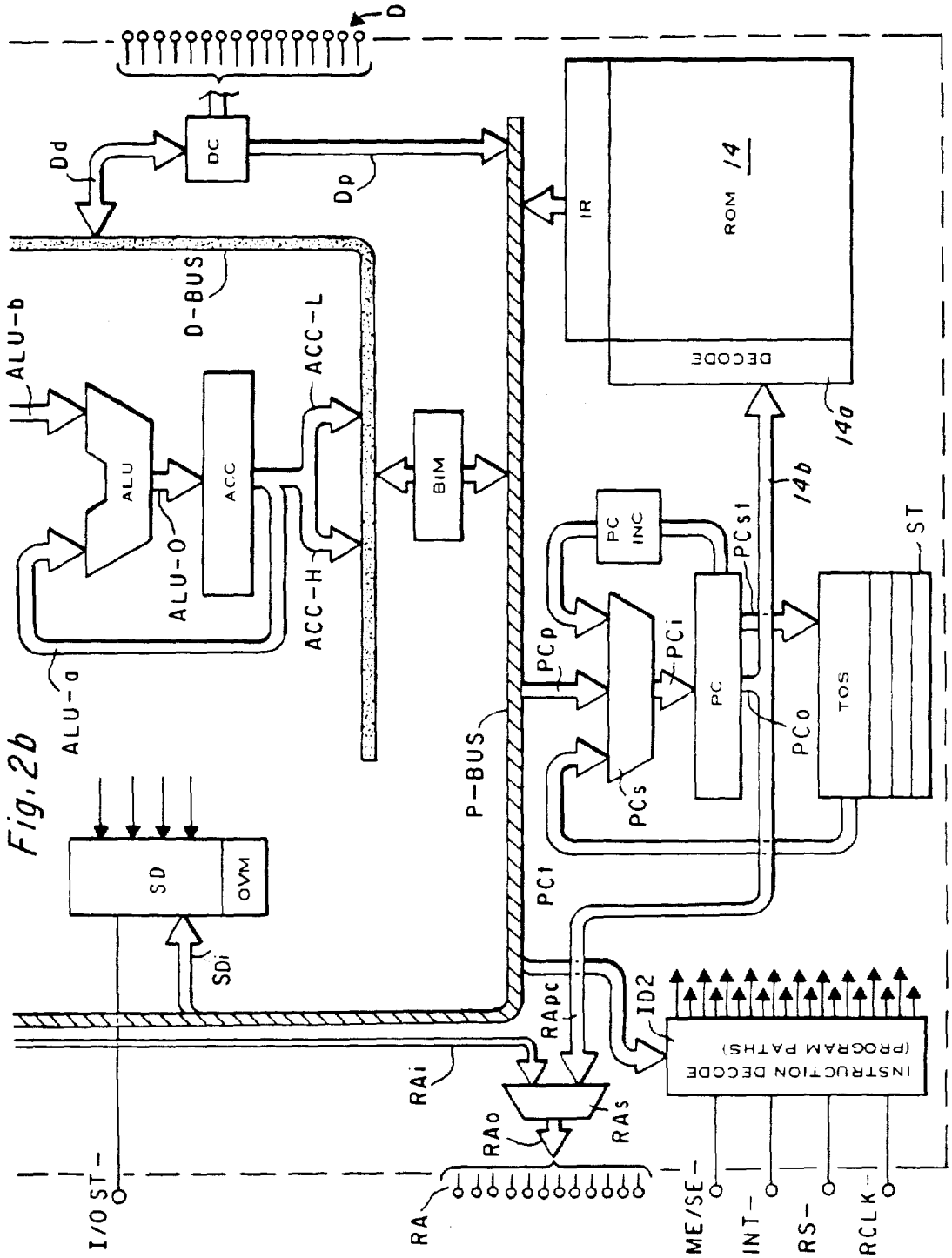

D
Dd
DC
Dp
IR
ROM 14
DECODE
140
D-BUS
ALU-b
ACC-L
ALU
ACC
BIM
ALU-0
ACC-H
ALU-a
14b
PC INC
PCs1
ST
PCp
PCi
PC
PCo
TOS
PCs
P-BUS
PC1
SD
OVM
SDi
RApc
ID2
INSTRUCTION DECODE
(PROGRAM PATHS)
RAi
RAo
RAs
I/O ST-
RA
ME/SE-
INT-
RS-
RCLK-

Fig. 2b

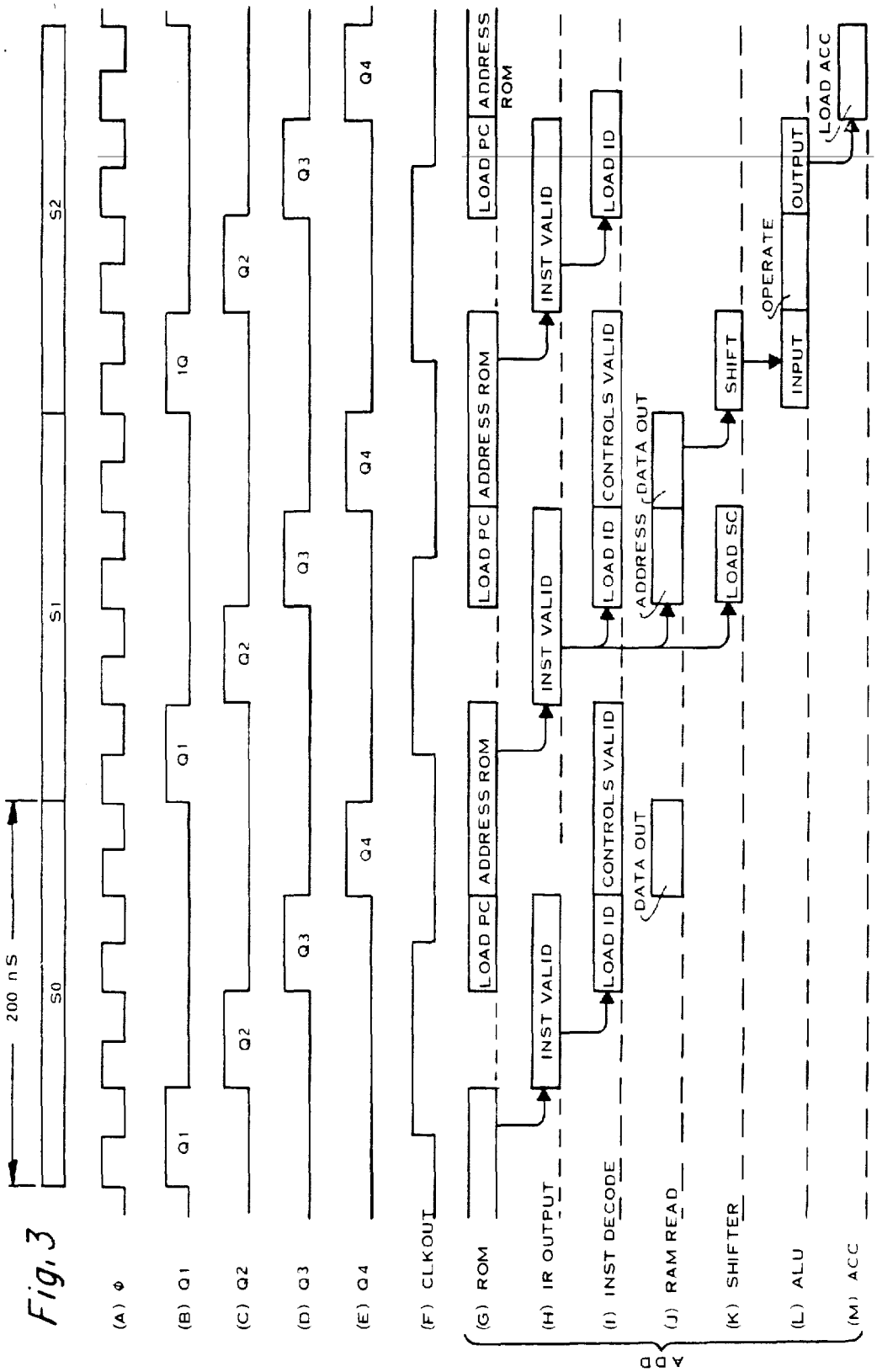

200 nS
S0
S1
S2
(A) Φ
(B) Q1
(C) Q2
(D) Q3
(E) Q4
(F) CLKOUT
(G) ROM
(H) IR OUTPUT
(I) INST DECODE
(J) RAM READ
(K) SHIFTER
(L) ALU
(M) ACC
LOAD PC
ADDRESS ROM
INST VALID
LOAD ID
CONTROLS VALID
DATA OUT
ADDRESS
LOAD SC
SHIFT
OPERATE
INPUT
OUTPUT
LOAD ACC

Fig. 3

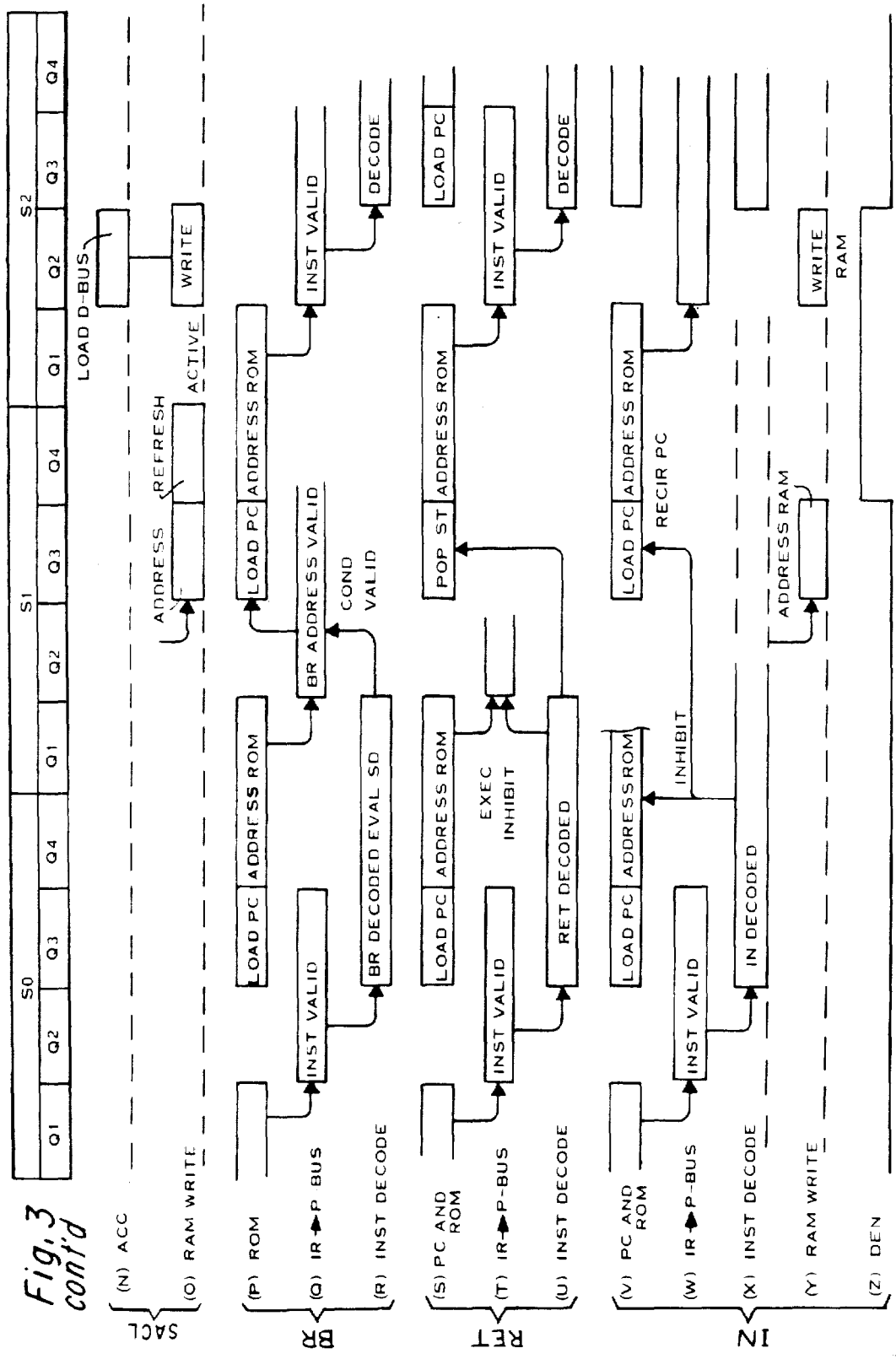


Fig. 3 cont'd
S0
S1
S2
Q1
Q2
Q3
Q4
(N) ACC
(O) RAM WRITE
SACL
LOAD D-BUS
WRITE
ADDRESS
REFRESH
ACTIVE
(P) ROM
(Q) IR→P BUS
(R) INST DECODE
BR
LOAD PC
ADDRESS ROM
INST VALID
BR DECODED EVAL SD
BR ADDRESS VALID
COND VALID
DECODE
(S) PC AND ROM
(T) IR→P-BUS
(U) INST DECODE
RET
POP ST
EXEC INHIBIT
RET DECODED
(V) PC AND ROM
(W) IR→P-BUS
(X) INST DECODE
IN
RECIR PC
INHIBIT
IN DECODED
ADDRESS RAM
(Y) RAM WRITE
RAM
(Z) DEN

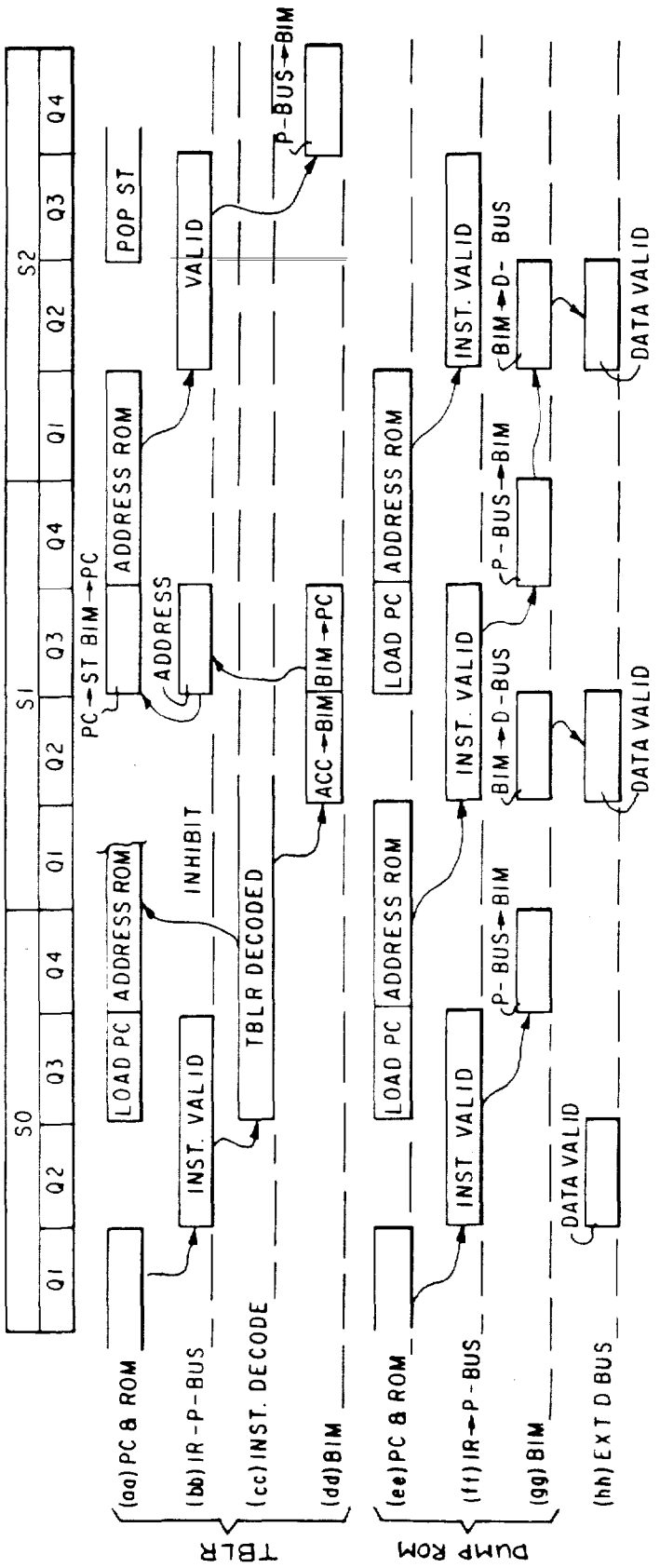

S0
S1
S2
Q1
Q2
Q3
Q4
(aa) PC & ROM
(bb) IR-P-BUS
(cc) INST. DECODE
(dd) BIM
TBLR
LOAD PC
ADDRESS ROM
INST. VALID
TBLR DECODED
INHIBIT
PC→ST BIM→PC
ADDRESS
ACC→BIM BIM→PC
POP ST
VALID
P-BUS→BIM
(ee) PC & ROM
(ff) IR→P-BUS
(gg) BIM
(hh) EXT D BUS
DUMP ROM
BIM→D-BUS
P-BUS→BIM
DATA VALID
INST. VALID
BIM→D- BUS

Fig. 3 (cont'd)

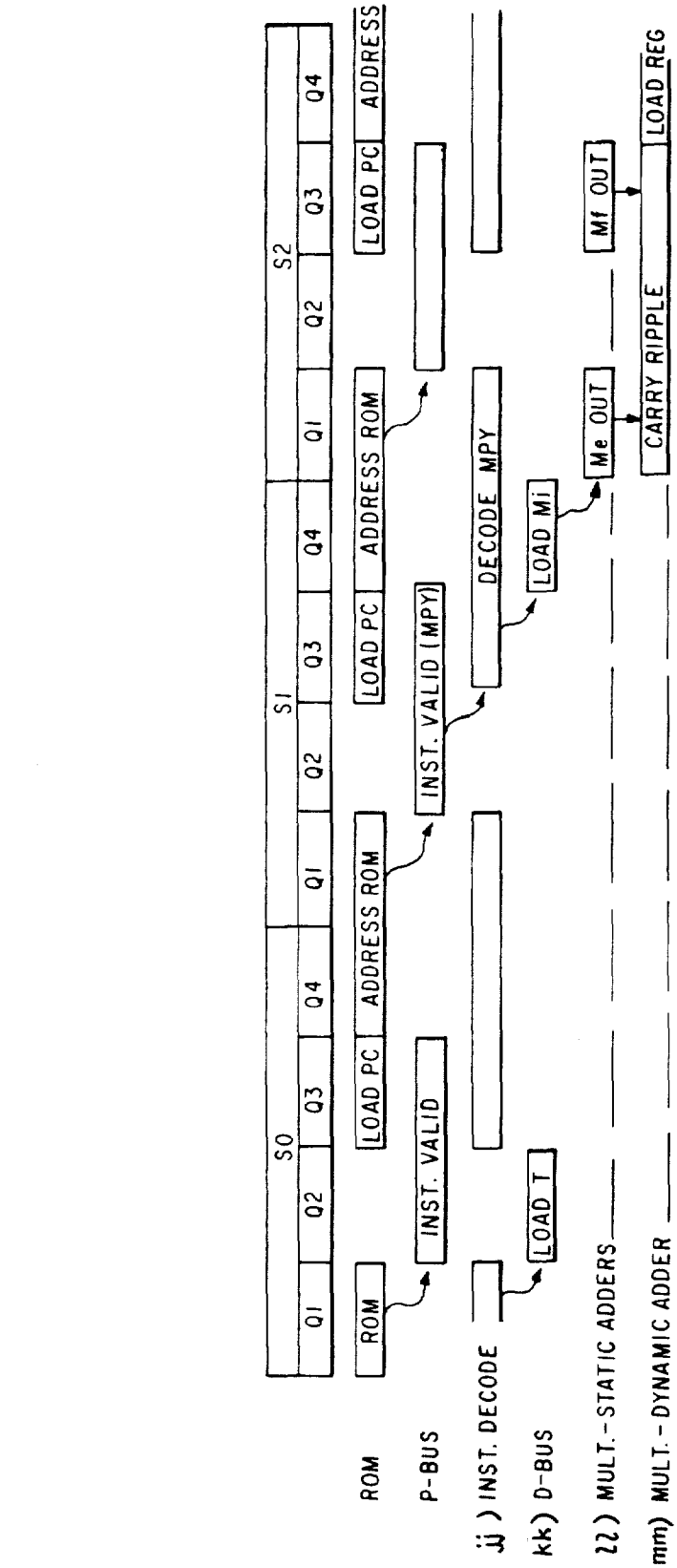


Fig. 3(cont'd) MULTIPLY INSTRUCTION

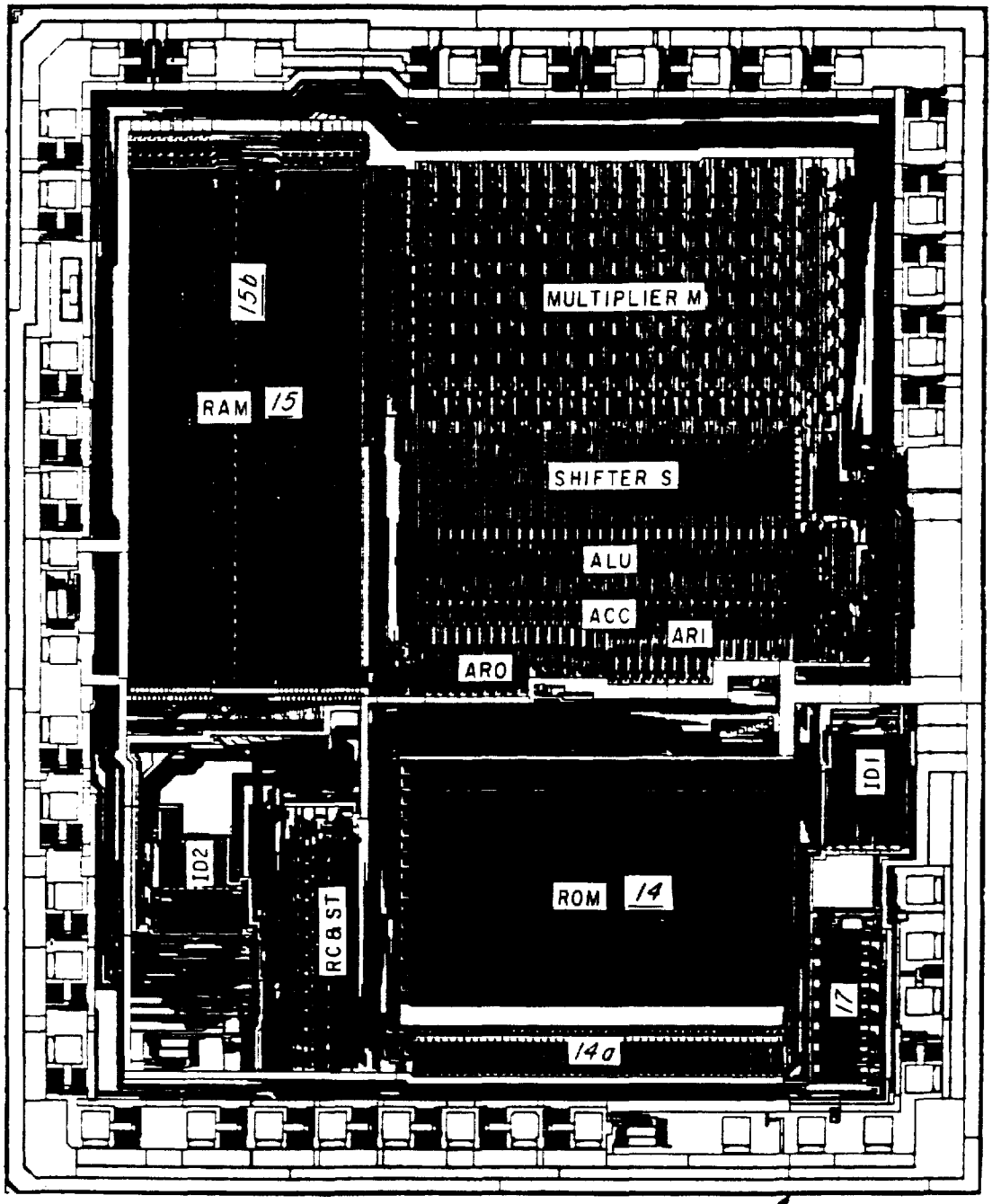

15b
MULTIPLIER M
RAM
15
SHIFTER S
ALU
ACC
ARI
ARO
ID1
ID2
RC & ST
ROM
14
17
14a
10

Fig. 4

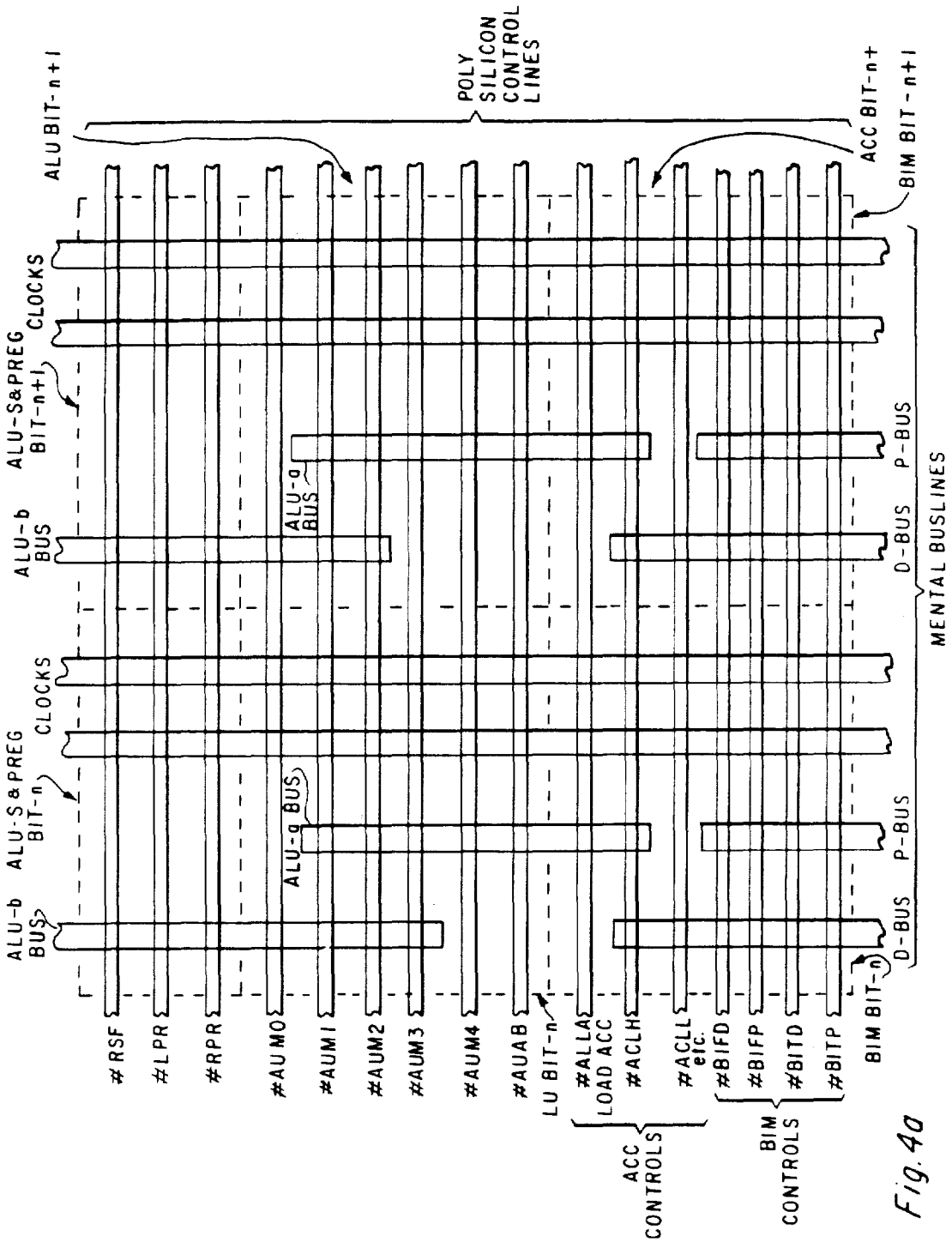

POLY SILICON CONTROL LINES
ALU BIT-n+1
ACC BIT-n+1
BIM BIT-n+1
ALU-S&PREG CLOCKS
ALU-S&PREG BIT-n+1
ALU-b BUS
ALU-g BUS
D-BUS
P-BUS
MENTAL BUSLINES
ALU-S&PREG CLOCKS
ALU-S&PREG BIT-n
ALU-b BUS
ALU-g BUS
D-BUS
P-BUS
BIM BIT-n
LU BIT-n
#RSF
#LPR
#RPR
#AUMO
#AUM1
#AUM2
#AUM3
#AUM4
#AUAB
#ALLA LOAD ACC
#ACLH
#ACLL etc.
#BIFD
#BIFP
#BITD
#BITP
ACC CONTROLS
BIM CONTROLS

Fig. 4a

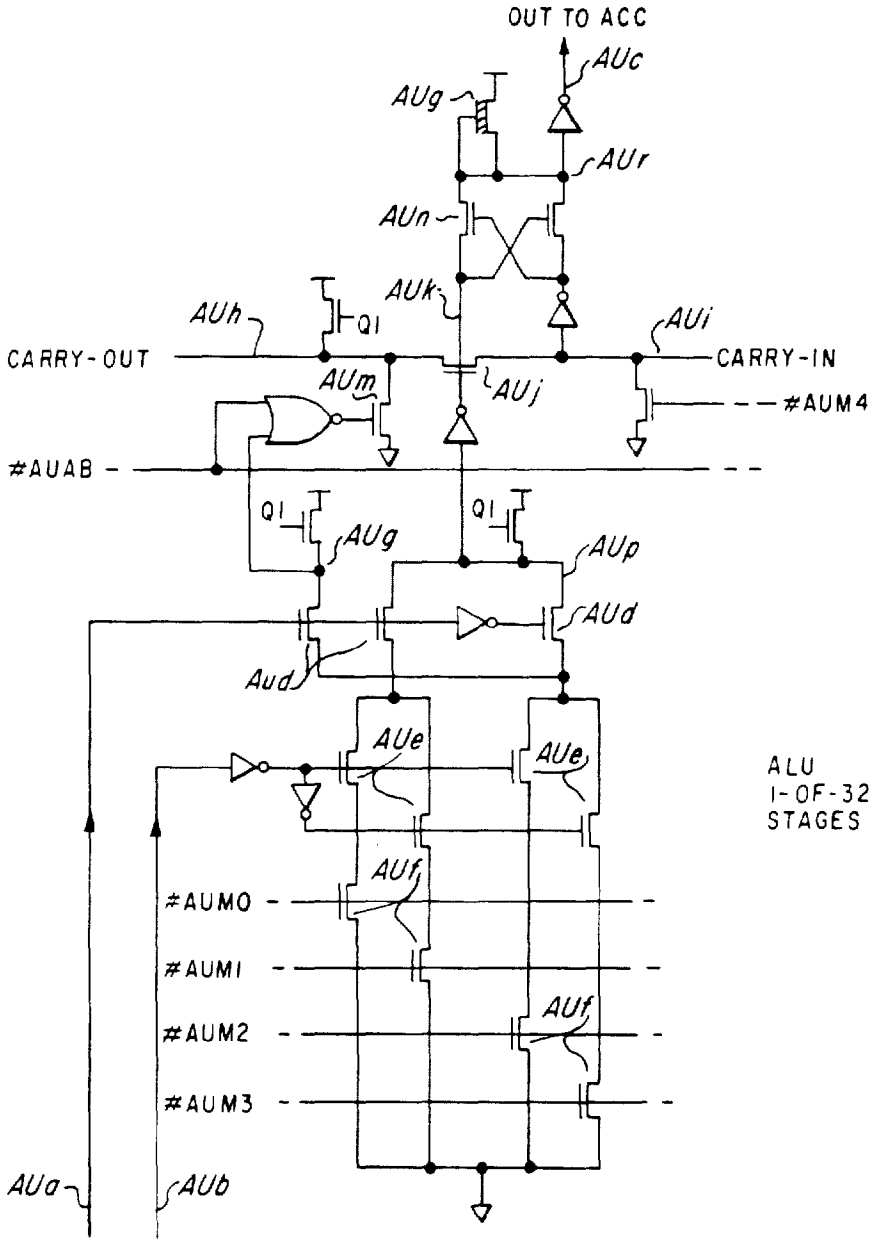

OUT TO ACC
AUc
AUg
AUr
AUn
AUk
AUh
Q1
AUi
CARRY-OUT
CARRY-IN
AUm
AUj
#AUM4
#AUAB
Q1
Q1
AUg
AUp
AUd
AUd
AUe
AUe
ALU
1-OF-32
STAGES
AUf
#AUMO
#AUMI
AUf
#AUM2
#AUM3
AUa
AUb

Fig. 5a

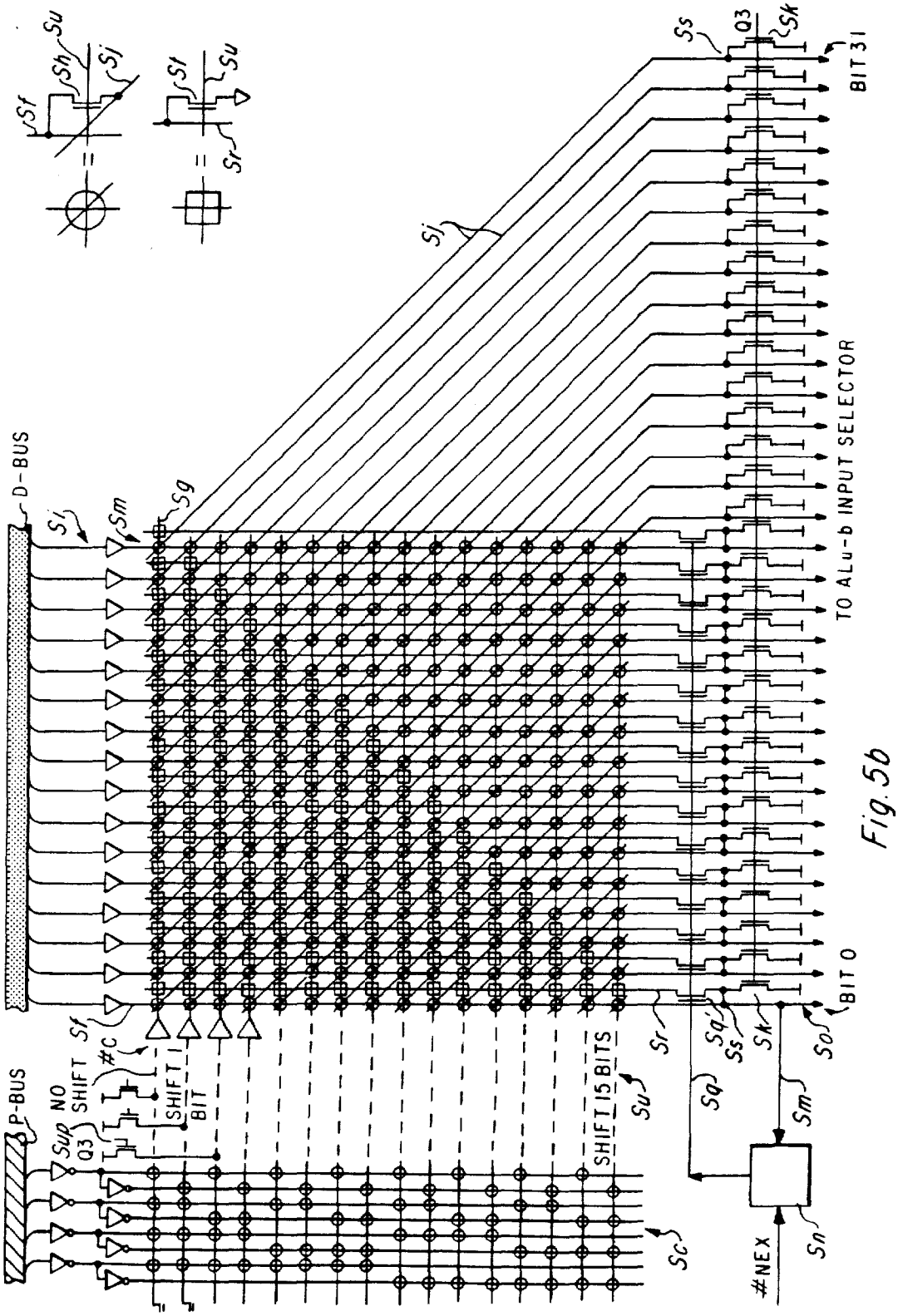

Su
Sh
Sj
Sf
Si
Su
Sr
Ss
Q3
Sk
BIT 31
Sj
D-BUS
Si
Sm
Sg
TO ALu-b INPUT SELECTOR
Sf
#C
SHIFT
NO SHIFT
Sup
Q3
P-BUS
SHIFT 1 BIT
SHIFT 15 BITS
Su
Sr
Sq'
Ss
Sk
So
BIT 0
Sq
Sm
Sc
#NEX
Sn

Fig. 5b

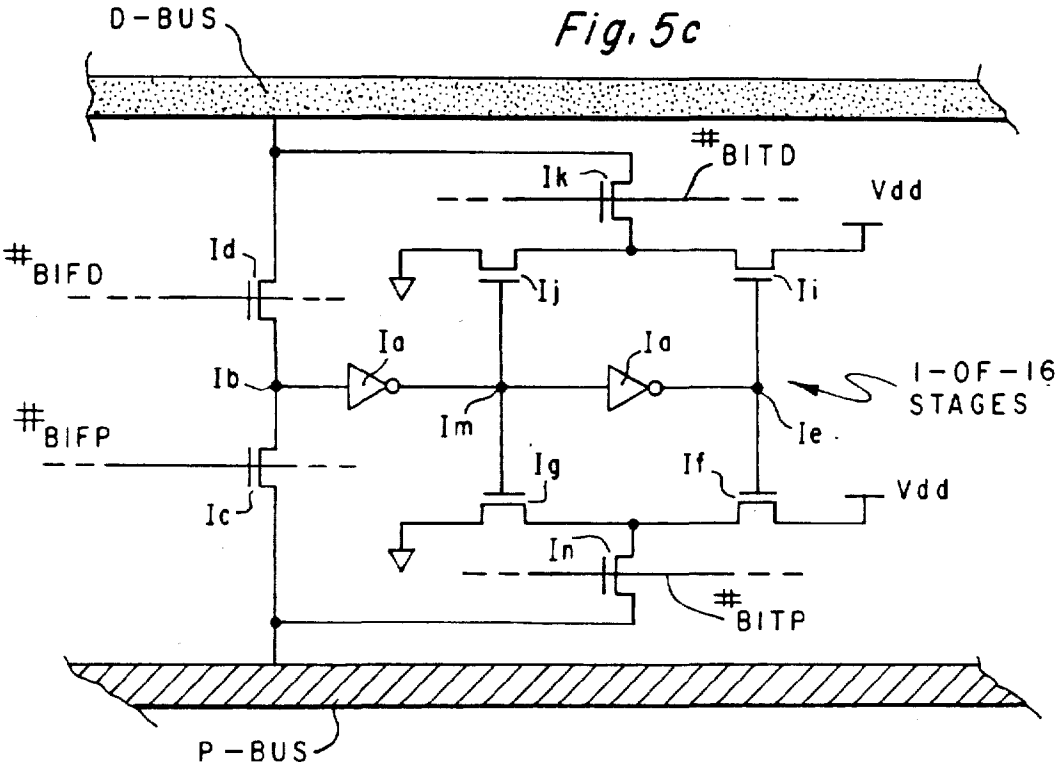

D-BUS
#BITD
Ik
Vdd
#BIFD
Id
Ij
Ii
Ia
Ia
Ib
I-OF-16
STAGES
#BIFP
Im
Ie
Ig
If
Vdd
Ic
In
#BITP
P-BUS

Fig. 5c

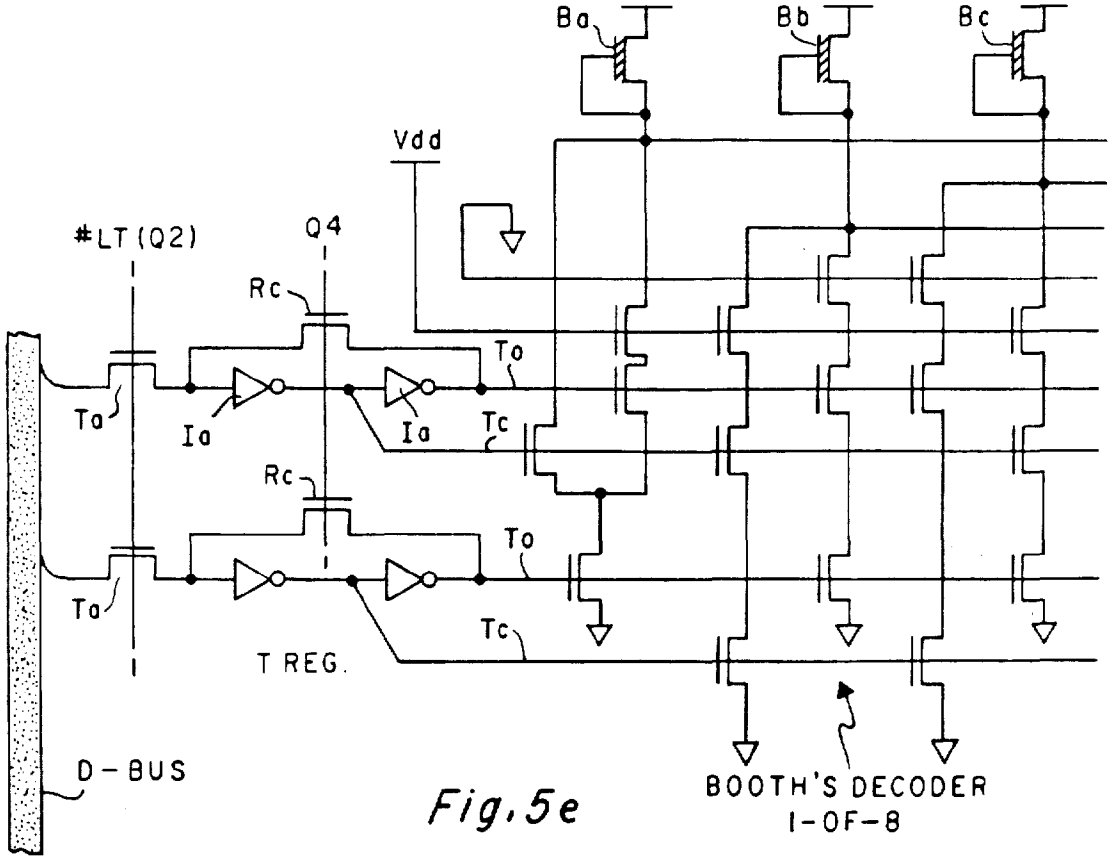

Ba
Bb
Bc
Vdd
#LT(Q2)
Q4
Rc
To
To
Ia
Ia
Tc
Rc
To
To
Tc
T REG.
D-BUS
BOOTH'S DECODER
I-OF-8

Fig. 5e

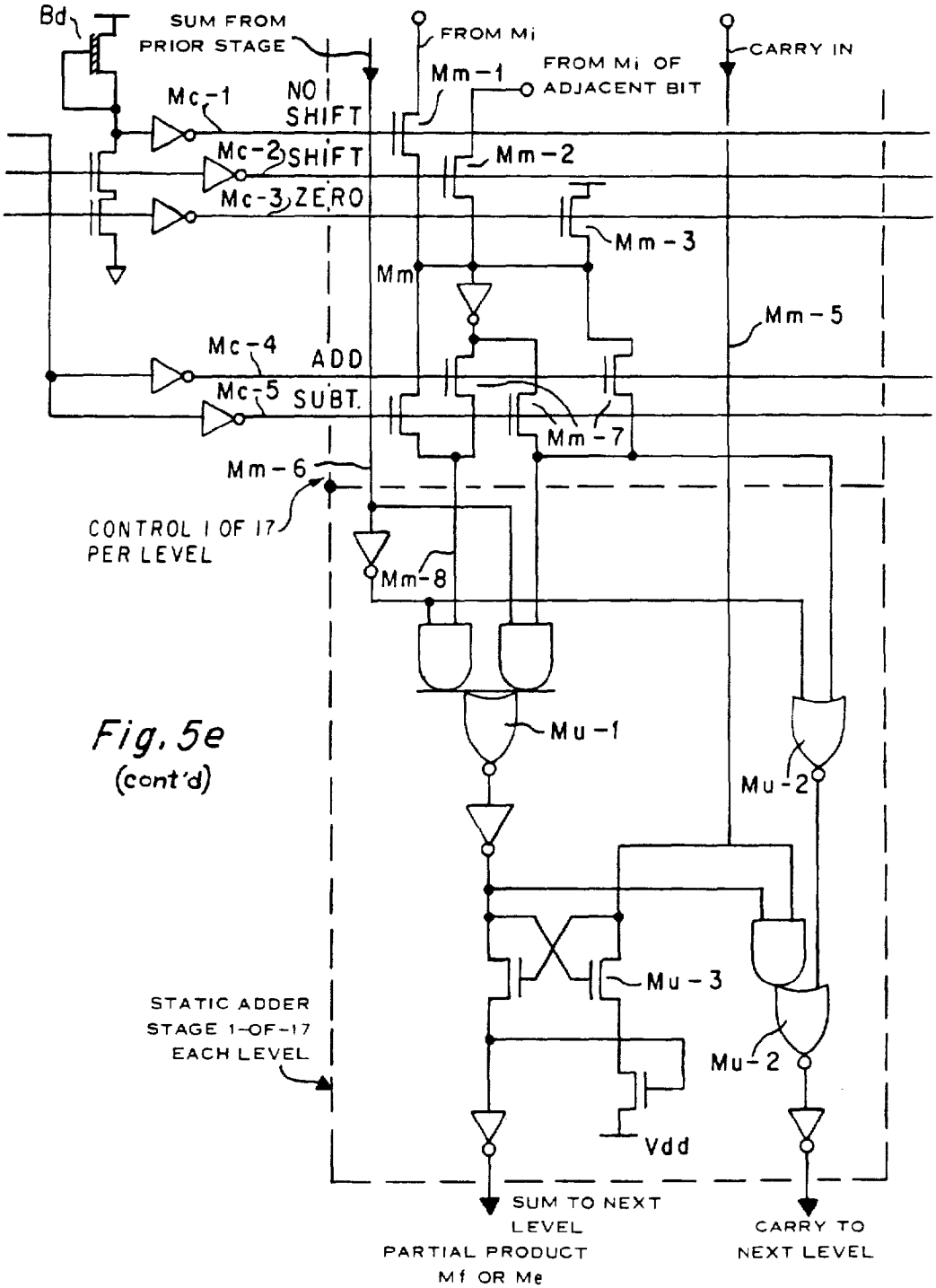
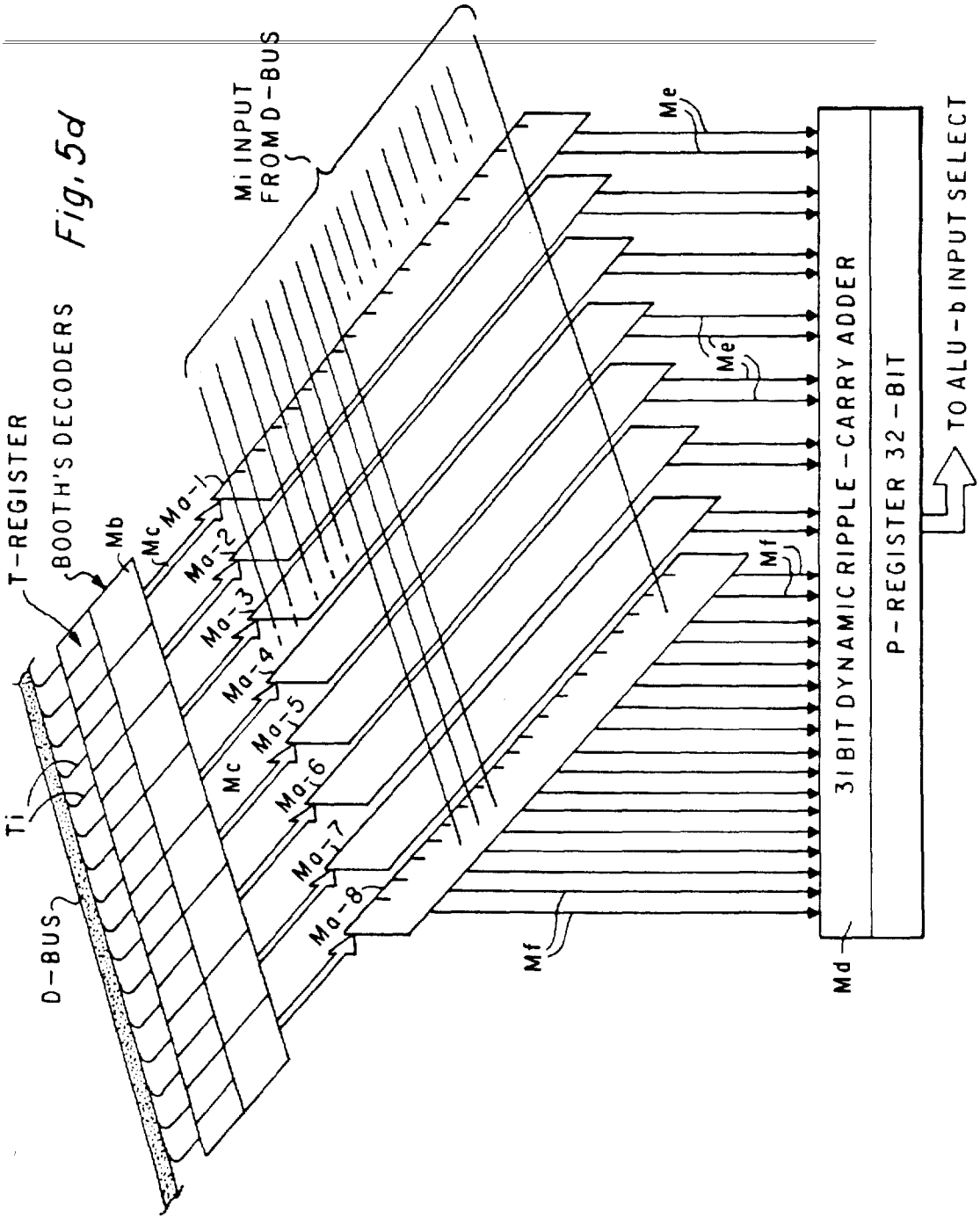

Bd
SUM FROM PRIOR STAGE
FROM Mi
FROM Mi OF ADJACENT BIT
CARRY IN
Mm-1
Mc-1
NO SHIFT
Mc-2 SHIFT
Mc-3 ZERO
Mm-2
Mm-3
Mm
Mm-5
Mc-4
ADD
Mc-5 SUBT.
Mm-7
Mm-6
CONTROL 1 OF 17 PER LEVEL
Mm-8
Mu-1
Mu-2
Mu-3
Mu-2
STATIC ADDER STAGE 1-OF-17 EACH LEVEL
Vdd
SUM TO NEXT LEVEL PARTIAL PRODUCT Mf OR Me
CARRY TO NEXT LEVEL

Fig. 5e
(cont'd)


Fig, 5d
Mi INPUT FROM D-BUS
Me
Me
T-REGISTER
BOOTH'S DECODERS
Mb
Mc Ma-1
Ma-2
Ma-3
Ma-4
Mc Ma-5
Ma-6
Ma-7
Ma-8
Mf
Mf
31 BIT DYNAMIC RIPPLE-CARRY ADDER
P-REGISTER 32-BIT
TO ALU-b INPUT SELECT
Ti
D-BUS
Md

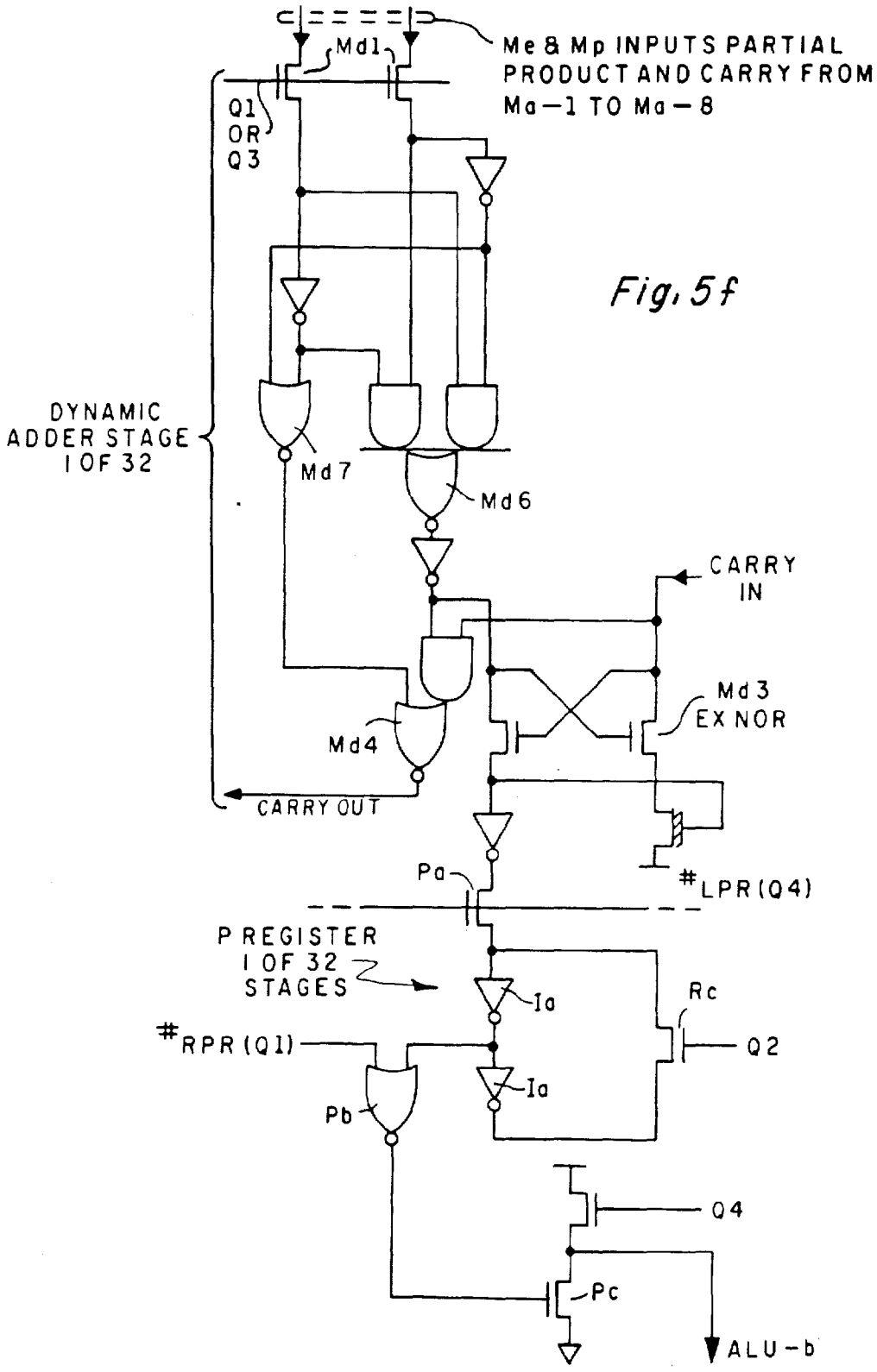

Me & Mp INPUTS PARTIAL PRODUCT AND CARRY FROM Ma−1 TO Ma−8
Md1
Q1 OR Q3
DYNAMIC ADDER STAGE 1 OF 32
Md7
Md6
CARRY IN
Md3 EX NOR
Md4
CARRY OUT
Pa
#LPR(Q4)
P REGISTER 1 OF 32 STAGES
Ia
Rc
#RPR(Q1)
Q2
Ia
Pb
Q4
Pc
ALU−b

Fig. 5f

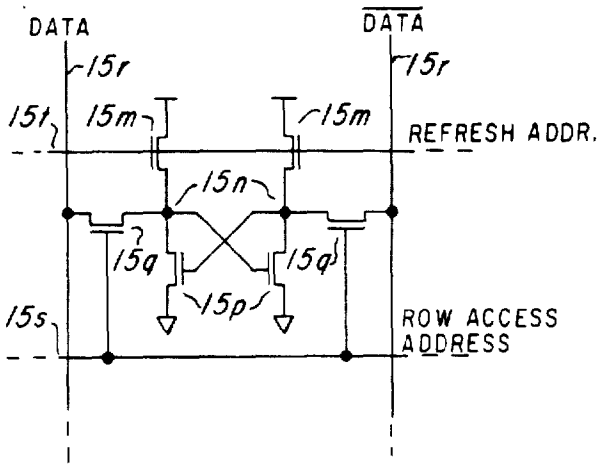

DATA
DATA
15r
15r
15t
15m
15m
REFRESH ADDR.
15n
15q
15q
15p
15s
ROW ACCESS ADDRESS

Fig. 5g

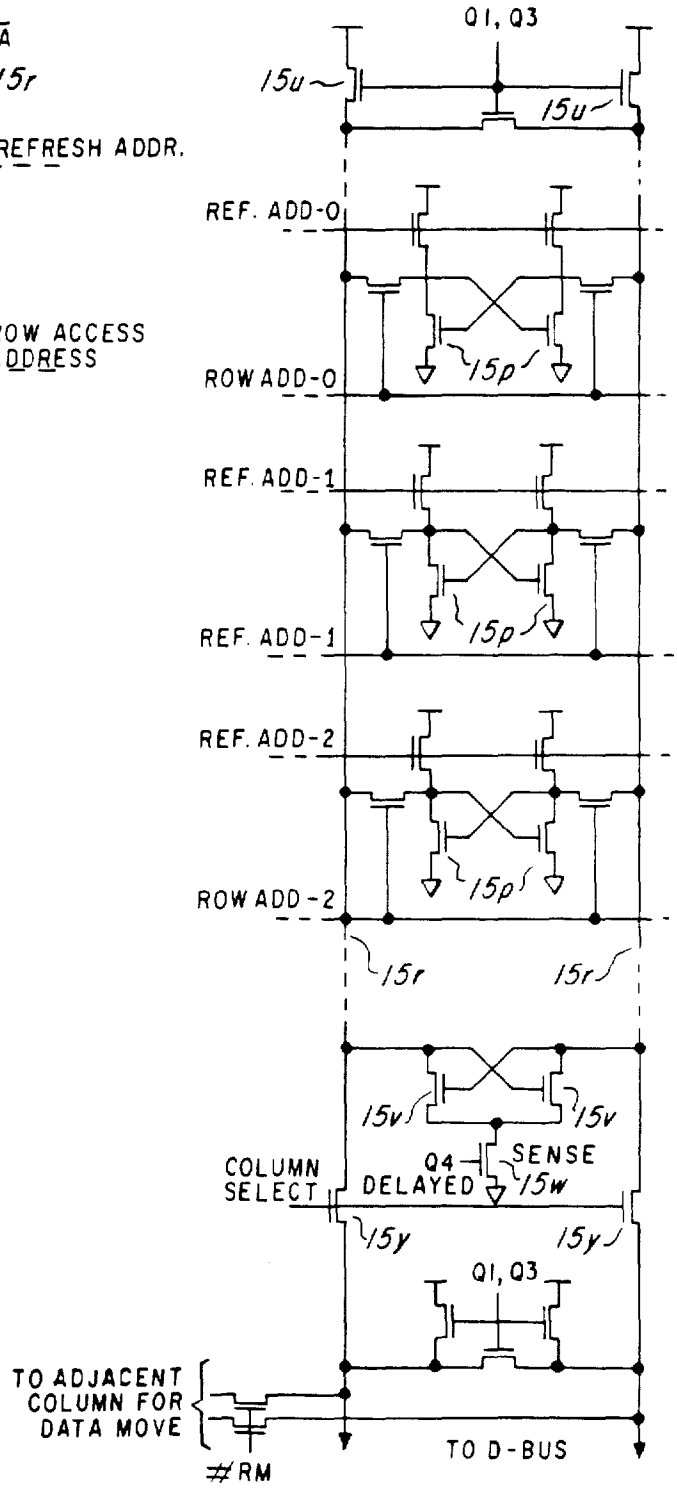

Q1, Q3
15u
15u
REF. ADD-0
15p
ROW ADD-0
REF. ADD-1
15p
REF. ADD-1
REF. ADD-2
15p
ROW ADD-2
15r
15r
15v
15v
COLUMN SELECT
Q4 DELAYED
SENSE
15w
15y
15y
Q1, Q3
TO ADJACENT COLUMN FOR DATA MOVE
#RM
TO D-BUS

Fig. 5h

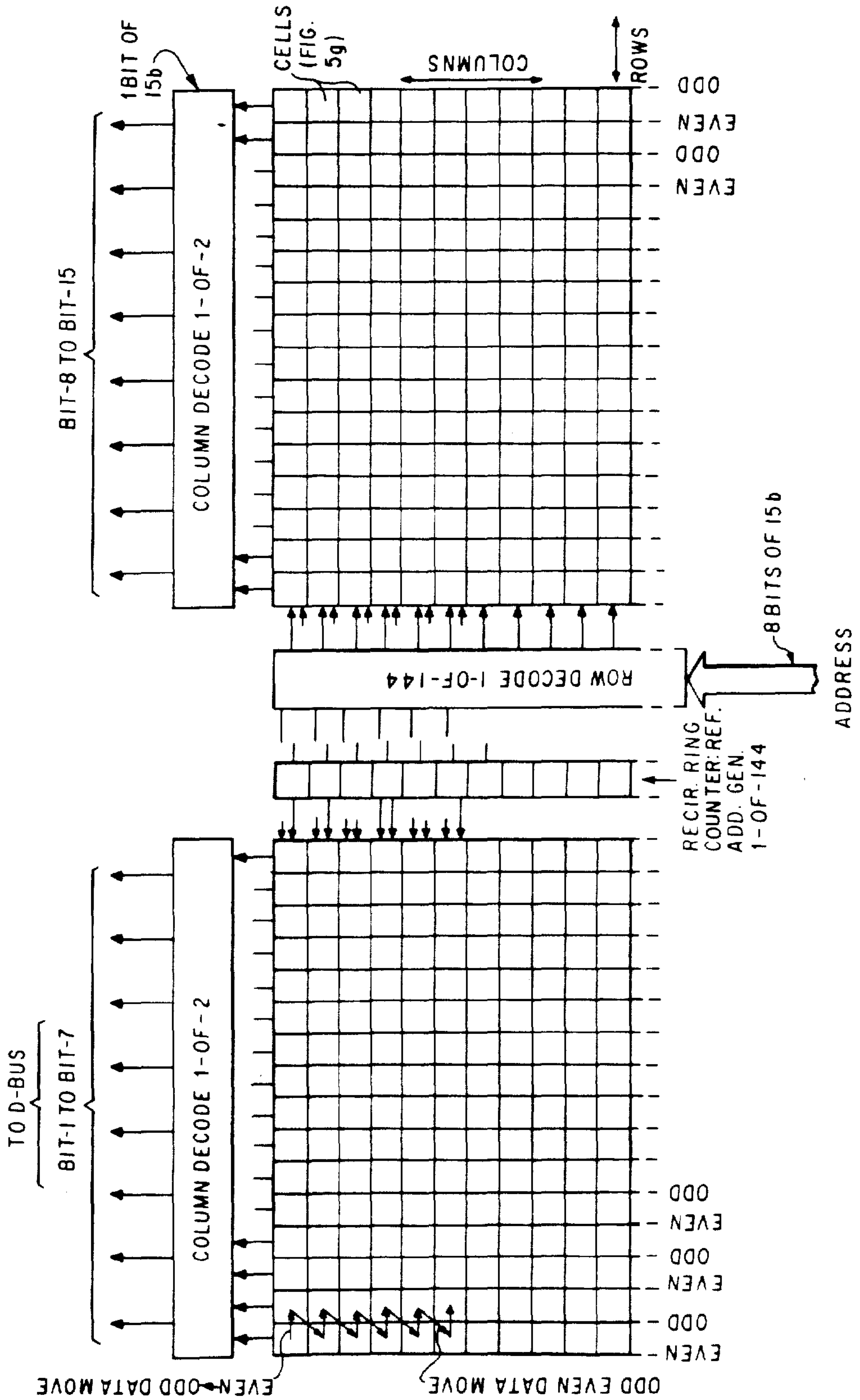

1BIT OF 15b
CELLS (FIG. 5g)
COLUMNS
ROWS
ODD
EVEN
BIT-8 TO BIT-15
COLUMN DECODE 1-OF-2
ROW DECODE 1-OF-144
8 BITS OF 15b
ADDRESS
RECIR. RING COUNTER: REF. ADD. GEN. 1-OF-144
TO D-BUS
BIT-1 TO BIT-7
EVEN→ODD DATA MOVE
ODD EVEN DATA MOVE

Fig. 5i

MICROCOMPUTER WITH BUS INTERCHANGE MODULE

This is a continuation of application Ser. No. 347,860, filed Feb. 11, 1982.

BACKGROUND OF THE INVENTION

This invention relates to integrated semiconductor devices and systems, and more particularly to a high-speed, miniaturized, electronic digital signal processing system in single-chip microcomputer form.

A microprocessor device is a central processing unit or CPU for a digital processor which is usually contained in a single semiconductor integrated circuit or "chip" fabricated by "MOS/LSI" technology, as shown in U.S. Pat. No. 3,757,306 issued to Gary W. Boone and assigned to Texas Instruments. The Boone patent shows a single-chip 8-bit CPU including a parallel ALU, registers for data and addresses, an instruction register and a control decoder, all interconnected using the Von Neuman architecture and employing a bidirectional parallel bus for data, address and instructions. U.S. Pat. No. 4,074,351, issued to Gary W. Boone and Michael J. Cochran, assigned to Texas Instruments, shows a single-chip "microcomputer" type device which contains a 4-bit parallel ALU and its control circuitry, with on-chip ROM for program storage and on-chip RAM for data storage, constructed in the Harvard architecture. The term microprocessor usually refers to a device employing external memory for program and data storage, while the term microcomputer refers to a device with on-chip ROM and RAM for program and data storage; the terms are also used interchangably, however, and are not intended as restrictive as to this invention.

Subsequent to 1971 when U.S. Pat. Nos. 3,757,306 and 4,074,351 were originally filed, many improvements have been made in microprocessors and microcomputers to increase the speed and capability of these devices and reduce the cost of manufacture, providing more circuitry and functions in less space, i.e., smaller chip size. Improved VLSI semiconductor processing and photolithographic techniques allow narrower line widths and higher resolution, providing added circuit density and higher speed, but circuit and system improvements also contribute to the goals of increased performance with smaller chip size. Some of these improvements in microcomputers are disclosed in the following U.S. Patents, all assigned to Texas Instruments: U.S. Pat. No. 3,991,305 issued to Edward R. Caudel and Joseph H. Raymond Jr.; U.S. Pat. No. 4,156,927 issued to David J. McElroy and Graham S. Tubbs; U.S. Pat. No. 3,934,233 issued to R. J. Fisher and G. D. Rogers; U.S. Pat. No. 3,921,142 issued to J. D. Bryant and G. A. Hartsell; U.S. Pat. No. 3,900,722 issued to M. J. Cochran and C. P. Grant; U.S. Pat. No. 3,932,846 issued to C. W. Brixely et al; U.S. Pat. No. 3,939,335 issued to G. L. Brantingham, L. H. Phillips and L. T. Novak; U.S. Pat. No. 4,125,901 issued to S. P. Hamilton, L. L. Miles, et al; U.S. Pat. No. 4,158,432 issued to M. G. VanBavel; U.S. Pat. No. 3,757,308 and U.S. Pat. No. 3,984,816. The devices described in these patents have been of the Harvard architecture and of the 4-bit type, particularly adapted for calculator or controller applications.

Additional examples of microprocessor and microcomputer devices in the evolutation of this technology are described in publications. In Electronics, Sept. 25, 1972, pp. 31–32, a 4-bit P-channel MOS microcomputer with on-chip ROM and RAM is shown which is similar to U.S. Pat. No. 3,991,305. Two of the most widely used 8-bit microprocessors like that of U.S. Pat. No. 3,757,306 are described in Electronics, Apr. 18, 1974 at pp. 88–95 (the Motorola 6800) and pp. 95–100 (the Intel 8080). A microcomputer version of the 6800 is described in Electronics, Feb. 2, 1978 at pp. 95–103. Likewise, a single-chip microcomputer version of the 8080 is shown in Electronics, Nov. 25, 1976 at pp. 99–105. Another single-chip microcomputer, the Mostek 3872, is shown in Electronics, May 11, 1978, at p. 105–110 and an improved version of the 6800 is disclosed in ELectronics, Sept. 17, 1979 at pp. 122–125. Sixteen-bit microprocessors based on minicomputer instruction sets evolved such as the part number TMS9900 described in a book entitled "9900 Family Systems Design", published in 1978 by Texas Instruments Incorporated, P.O. Box 1443, M/S 6404, Houston, Tex. 77001, Library of Congress Catalog No. 78-058005. The 8086, a 16-bit microprocessor evolving from the 8080, is described in Electronics, Feb. 16, 1978, pp. 99–104, while a 16-bit microprocessor identified as the 68000 (based on the 6800) is described in Electronic Design, Sept. 1, 1978 at pp. 100–107, and in IEEE Computer, Vol. 12. No. 2, pp. 43–52 (1979).

These prior 8-bit and 16-bit microprocessors and microcomputers have been general-purpose processors of the Von Neuman architecture with multiplexed address/data busses, and usually have been microcoded as described in U.S. patent application Ser. No. 209,915, filed Nov. 24, 1980 by Guttag, McDonough and Laws (now U.S. Pat. No. 4,402,043, or Ser. No. 253,624, filed Apr. 13, 1981, by Hayn, McDonough and Bellay, both assigned to Texas Instruments, and at pp. 28–34, IEEE Spectrum, March 1979, by McKevitt and Bayliss, or Proceedings 11th Annual Microprogramming Workshop, December, 1979 by Stintter and Tredenick. Microcoding, originally described by Wilkes in 1951, employs a control ROM to store microinstruction sequences entered by instruction words; the programmer works in a higher level machine code, so the number of assembly language code statements is supposedly reduced, and thus programming cost is reduced.

In contrast, a special-purpose high-speed microcomputer device according to the embodiment of the invention described herein departs from these contemporary microprocessor devices in several major respects in order to achieve substantial speed and performance advantages. This device is a non-microcoded processor of modified Harvard architecture.

It is the principal object of this invention to provide improved features of a microcomputer device and system, particularly one adapted for real-time digital signal processing. Another object is to provide a high-speed microcomputer of enhanced capabilities.

SUMMARY OF THE INVENTION

In accordance with one embodiment, features of the invention are included in a system for real-time digital signal processing employing a single-chip microcomputer device having separate on-chip program ROM and data RAM, with separate address and data paths for program and data. An external program address bus allows off-chip program fetch in an expansion mode, with the opcode returned by an external data bus. A bus interchange module allows transfer between the sepa-

rate internal program and data busses in special circumstances. The internal busses are 16-bit, while the ALU and accumulator are 32-bit. A multiplier circuit produces a single state 16×16 multiply function separate from the ALU, with 32-bit output to the ALU. One input to the ALU passes through a 0-to-15 bit shifter with sign extension.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as other features and advantages thereof, will be best understood by reference to the detailed description which follows, read in conjunction with the accompanying drawings, wherein;

FIG. **1** is an electrical diagram in block form of a microcomputer system employing features of the invention;

FIG. **2** is an electrical diagram in block form of an MOS/LSI microcomputer device (including a CPU or central processor unit) employed in the system of FIG. **1** and utilizing features of the invention;

FIGS. **3***a*–**3***mm* are timing diagrams showing voltage or event vs. time in the operation of the microcomputer of FIG. **2**;

FIGS. **4** and **4***a* are greatly enlarged plan views of a semiconductor chip containing the microcomputer of FIG. **2**, showing the physical layout of the various parts of the device;

FIGS. **5***a*–**5***i* are electrical schematic diagram of particular circuits in the microcomputer device of FIG. **2**.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENT

Microprocessor System

The microcomputer device to be described herein is primarily used for signal processing, but concepts thereof may be used in processor devices of various configurations, and these devices may be used in many different systems; in one embodiment the microcomputer is used in a system shown in generalized form in FIG. **1**. The system may be, for example, a voice communication system, a speech analysis system, a small "personal" or "home" computer, a single-board general purpose microcomputer, a word processing system, a computer terminal having local processing capability with display and typewriter keyboard, or any one of many applications of various types. The system includes a single-chip MOS/LSI central processing unit or microcomputer **10** which will be described in detail, along with a program or data memory **11** and input/output or I/O devices **12**. Usually the I/O devices **12** for the typical system include analog-to-digital and/or digital-to-analog converters, a modem, a keyboard, a CRT display, a disc drive, etc. Often the I/O **12** includes coupling to a general purpose processor; that is the microcomputer **10** is an attached processor in a larger system with interface via the I/O **12**. The microcomputer **10**, program data memory **11** and I/O **12** communicate with one another by two multibit, parallel address and data busses, D and RA, along with a control bus **13**. The microcomputer **10** has suitable supply voltage and crystal-input terminals; for example, the device employs a single +5 V Vcc supply and ground or Vss, and a crystal is connected to terminals X1 and X2 of the device **10** to control certain system timing. The microcomputer **10** is a very high speed device with a crystal input of 20 MHZ, providing an instruction execution rate of five million per second, in one embodiment.

The microcomputer device **10** is a general purpose microcomputer specifically aimed at serving a large class of serial signal processing problems such as digital filtering, signal handling for telecommunications modems (modulation, demodulation), data compression for linear predictive code (LPC) speech signals, fast Fourier transforms, and in general for virtually all computation intensive analog system functions, including detection, signal generation, mixing, phase tracking, angle measurement, feedback control, clock recovery, correlation, convolution, etc. It is suitable for applications which have computational requirements similar to those for control and signal processing, such as coordinate transformation, solution of linear differential equations with constant coefficients, averaging, etc. The device **10** is usually interfaced via I/O **12** to a general purpose processor such as a 99000, an 8600 or a 68000, to construct processing systems as will be explained.

It is understood that, even though described in the context of a microcomputer in the preferred embodiment, with an on-chip program ROM **14** and data RAM **15**, nevertheless, some concepts of the invention may be used in a single-chip microprocessor with all off-chip program memory and/or data memory instead of the on-chip memory illustrated. Indeed, modes of operation are provided which disable the on-chip memory. Also, a microcomputer is shown having two separate external program address and data busses instead of the multiplexed, bidirectional busses which are now common, but some features herein disclosed are applicable where busses are multiplexed. The advantage of separating the busses and separating program and data memory space is speed.

In general terms, the system of FIG. **1** functions in the following manner: the microcomputer **10** fetches an instruction word internally by accessing the ROM **14** or externally by sending out an address on the ROM address bus RA to the memory **11** (and RCLK-on control bus **13**). If external, the instruction word is received back via the data bus D from the addressed location in the memory **11**. This instruction is executed in the next machine cycle (of length of 200 ns defined by a 20 MHz clock or crystal X1, X2) while a new instruction is being fetched; execution of an instruction may include accessing the on-chip RAM **15** for an operand, or writing a result into data RAM **15**, and an arithmetic or logic operation in ALU.

In the example to be described in detail, a 12-bit instruction address applied internally to ROM **14** or externally to the RA bus directly addresses 2^{12} or 4K words of program instruction or constants in ROM **14** and memory **11**. When reading from memory **11**, a DEN– (data bus enable bar) command is asserted on control bus **13**. It is also possible to write into the memory **11**, and for this purpose a WE– (write enable bar) command is asserted by the device **10** on one of the control bus lines **13**; the memory **11** may contain read/write memory devices in some or all of the address space, so the WE– command permits a write function.

The I/O devices **12** are addressed as ports; this interface to external devices **12** is accomplished using the address and data busses RA and D and control bus **13**, but the I/O devices **12** do not occupy locations in the logical address space like the memory **11**. This is in contrast to conventional memory-mapped I/O.

Data input/output via I/O or peripherals **12** employs a 3-bit field from the bus RA to select one of eight 16-bit ports in peripheral circuitry **12**. The selected 16-bit port is then accessed for read or write via the bus D. This operation uses one of the two instructions IN or OUT, on the control bus **13**, WE− is active for write or OUT, or DEN− is active for read or IN. A ROM clock RCLK− is active on control bus **13** on every machine cycle except when either DEN− or WE− is active; that is, the memory **11** is activated by RCLK− for possible instruction word access from off-chip in each machine cycle, but if accessing peripheral **12** using DEN− or WE− then the RCLK− does not occur.

A reset signal RS− on the control bus **13** clears the program counter and address bus RA (resets to zero), sets the data bus D in a high impedance state, and the memory controls DEN−, WE− and RCLK− in an inactive (high) state. All address and temporary data registers within the microcomputer **10** are cleared by a reset routine in the ROM **14**, but the internal RAM is not cleared. In this manner, the peripheral circuitry **12** (such as a main processor) can assert control, or initiate a start-up or power-on sequence.

An interrupt signal INT− on the control bus **13** causes the microcomputer **10** to halt execution (saving the current ROM address) and go to an interrupt vector address, unless interrupts are masked by the program.

The ME/SE− line in the control bus **13** defines the memory expansion mode or systems emulator mode for the microcomputer **10**. When this pin is held high (at +Vcc), the microcomputer executes from on-chip ROM and off-chip memory **11**, but when low (Vss) the chip is in the systems emulator mode and execution is only from the memory **11** which is PROM, EPROM or RAM so the program can be easily changed.

The Microcomputer Chip

The internal architecture of the microcomputer **10** is shown in a detailed block diagram in FIG. **2**. This device is a single-chip semiconductor integrated circuit mounted in a standard dual-in-line package or a chip carrier. Sixteen pins or terminals of the package are needed for the 16-bit data bus D, twelve to sixteen are used for the address bus RA (depending upon memory size) and the remaining terminals are used for the power supply Vcc and Vss, the crystal X**1**, X**2**, and the control bus **13**.

In addition to the program and data memory **14** and **15**, the microcomputer **10** contains a central processing unit or CPU for the system of FIG. **1**, and this CPU includes a 32-bit arithmetic logic unit or ALU, a 32-bit accumulator Acc to hold operands and results, multiplier M separate from the ALU, a shifter S which is one input to the ALU, status or flag decode SD, and an instruction decoder ID**1** which receives part of the current instruction word and generates the control bits for the CPU and data memory portions of the device **10**.

The program memory **14** has associated with it a program counter PC to hold the instruction address used to access the ROM **14** or sent out on bus RA to the memory **11**, an instruction register IR to receive the instruction word from ROM **14**, a stack ST to save program memory addresses, and an instruction decoder ID**2** which receives part of the current instruction word and generates control bits for the program memory portion of the microcomputer.

Associated with the data memory **15** are two auxiliary address registers AR**0** and AR**1** for the data memory **15**, a page register ARP to select between the registers AR**0** and AR**1** as the data memory address, and a data page buffer DP to hold certain bits of the data memory address.

The CPU is oriented around two internal busses, a 12-bit program bus (P-Bus) and a 16-bit data bus (D-Bus). Program access and data access can thus occur simultaneously, and the address spaces are separate. A bus interchange module BIM permits loading the program counter PC from Acc, for example, or accessing ROM **14** for constants via P-Bus, BIM and D-Bus.

The two major requirements for a signal processing microcomputer are high speed arithmetic and flexibility. Performance is achieved by using separate, principally on-chip program and data memories **14** and **15**, a large single accumulator Acc and a parallel multiplier M. A special purpose operation, data move, is defined within the data memory **15** which further enhances the performance in convolution operations. Flexibility has been achieved by defining an instruction set as will be described with reference to Table A, incorporating memory expansion and a single lever of interrupt.

The device can be configured with, for example, less than 2K or 2^{11} words of on-chip program memory **14** and the architecture allows for memory expansion up to 4K or 2^{12} words by the addition of external program memory in the memory **11**. In addition, a separate mode allows the device **10** to be configured as a system emulation device; in this "system emulator" mode, the entire 4K memory space is external and the ROM **14** is not used.

The CPU

The arithmetic logic unit or ALU consists of thirty-two parallel stages, each separate stage performing an arithmetic or logic function on its two input bits and producing a one-bit output and carry/borrow. The ALU has two 32-bit data inputs ALU-a and ALU-b, and a 32-bit data output ALU-o to accumulator Acc. The ALU-a input is always from the accumulator Acc and the ALU-b input is always either from the shifter S or from a 32-bit product register P in the multiplier M. The particular function performed on data passing through the ALU is defined by the current instruction word in IR which is applied by the program bus P-Bus to an instruction decoder ID**1**. The source of the ALU-b input is defined by an input select circuit ALU-s which selects from these two alternatives, based upon the contents of the current instruction word, i.e., the outputs #C of the decoder ID**1**. The shifter S receives a 16-bit input Si from D-Bus and produces a 32-bit output So which is the input Si shifted from zero to fifteen places to the left. Left-shifted data is zero-filled, i.e., all right-hand bit positions are filled with zeros when data is shifted out to the left. A unique feature is that the high-order bit is sign extended during shift operations. The ALU operates in twos-complement. The shifter S includes a shift control Sc loaded with a four-bit value from P-Bus via lines Sp so an arithmetic instruction can directly define the number of bits shifted in the path from D-Bus to the ALU-b input.

In this description, the LSB is considered to be on the right and the MSB on the left, so left-shift is toward more significant bits. Bit-**0** is the MSB and bit-**15** is the LSB. Data is always in signed 2's complement in this architecture.

The multiplier M is a 16×16 multiplier using carry feed-forward, constructed in partly dynamic and partly

static logic, to implement Booth's algorithm. One input to the multiplier M is the T register which is a 16-bit register for temporary storage of the multiplicand received from D-Bus via lines Ti. The other 16-bit input is via lines Mi from the D-Bus; this multiplier input may be from the data memory **15** or may be a 13-bit multiply-immediate value derived directly from the instruction word (loaded right-justified and sign-extended).

The ALU always receives the contents of the accumulator Acc as its ALU-a input, and always stores its output in Acc, i.e., Acc is always the destination and the primary operand. The unit will add, subtract and perform the logic operations of And, Or and Exclusive Or. The logic operation results are between the lower half of Acc (bits **16–31**) and a 16-bit value from the data memory **15**. Due to passing the data memory value through the shifter S (with zero shift), the operand for the logical operation result of the MSBs (bits **0–15**) is zero. The final 32-bit result reaching the accumulator is thus in two parts: Bits **0–15** will be Acc bits **0–15** Anded (or Or'ed, etc) with zero; bits **16–31** of the result will be Acc bits **16–31** Anded (etc.) with the data memory value. The accumulator Acc output, in addition to the 32-bit ALU-a input, includes high and low 16-bit outputs Acc-H (bits **0–15**) and Acc-L (bits **16–31**); separate instructions "store accumulator high" SACH and SACL "store accumulator low" are provided for storing high and low-order Acc bits in the data memory **15**.

The status decoder SD monitors the Acc whenever an instruction which updates Acc is executed. Four bits of SD are OV, L, G and Z. Accumulator overflow (or underflow) is indicated by the OV bit, Acc contents less than zero is indicated by the L bit, Acc greater than zero indicated by the G bit, and Acc equal zero indicated by the Z bit. Upon interrupt the OV bit is saved in an overflow flag register, but the other bits are available only up to the time the next accumulator instruction is executed.

The accumulator overflow mode is a single-bit mode register OVM (included in SD), directly under program control, to allow for saturated results in signal processing computations. When the overflow mode OVM is reset, overflow results are loaded via ALU-o into the accumulator Acc from the ALU without modification. When the overflow mode is set, overflow results are set to the largest, or smallest, representable value of the ALU and loaded into the accumulator Acc. The largest or smallest value is determined by the sign of the overflow bit. This allows a saturated Acc result in signal processing applications, modeling the saturation process of analog signals.

A separate status bit in SD monitors the condition of the currently used auxiliary register AR0 or AR1 and detects the all-zero condition of the least significant nine bits of the current auxiliary register (i.e. loop counter portion). This bit is used for a branch instruction conditioned on non-zero for the auxiliary register (BARNZ), "branch on auxiliary register non-zero."

The input/output status bit (I/O ST−) is an external pin which is part of the control bus **13** and provides "branch on I/O zero" instruction (BIOZ) to interrogate the condition of peripheral circuits **12**. A zero level on the I/O ST− pin will cause a branch when sampled by the BIOZ instruction.

The bus interchange module BIM exchanges the low-order twelve bits of the 16-bit value on the D-Bus with the twelve bits on the P-Bus. This operation is not available to the programmer as an instruction, but instead is needed as an inherent operation in instructions such as table look up (TBLR A).

PROGRAM MEMORY ADDRESSING

The program memory **14** is a ROM which is partitioned to produce a 16-bit output to instruction register IR, and this ROM employs a decoder **14***a* which selects one 16-bit instruction word based on an 11-bit or 12-bit address on input lines **14***b*. In the example embodiment, the ROM **14** contains less than 2K words, so an 11-bit address can be used, but the on-chip program memory could be expanded to 4K with a 12-bit address. The circuit of the ROM **14** is especially adapted for fast access as will be explained. The address input **14***b* is received from the program counter PC which is a 12-bit register containing the address of the instruction following the one being executed. That is, at the time when the control bits #C are valid at the outputs of the instruction decoders ID1 and ID2 for one instruction, PC contains the address of the next instruction; an address in PC goes into decoder **14***a* and the next instruction is read from ROM **14** into IR, and the program counter PC is incremented via PCinc in preparation for another instruction fetch. That is, PC is self incrementing under control of a #C control bit from ID2. The output PCo from the program counter PC is also applied via lines RApc and selector RAs (and output buffers not shown) to the external RA bus via output lines RAo and twelve output pins of the microcomputer device. The RA bus (RA0 through RA11) contains the PC output via RApc when the selector RAs is in one mode, or contains the input RAi when executing I/O instructions IN and OUT. Whenever the address in PC is above the highest address in ROM **14**, off-chip program addressing to memory **11** is assumed; however, the device is designed to operate principally with the on-chip ROM, so for many uses of the device off-chip fetches for program instructions would never be needed. The program counter PC may be loaded via input PCi and selector PCs from the P-Bus for branch or call instructions, or loaded from the accumulator Acc via Acc-L, D-Bus, BIM, P-Bus, PCp and PCi in a "call accumulator" CALLA instruction.

The register stack ST is used for saving the contents of PC during subroutine and interrupt calls. In the illustrated embodiment, the stack ST contains four 12-bit registers constructed as a first-in, last-out push-down stack, although a larger or smaller number of registers could be used. The current contents of PC are saved by "pushing" onto the top-of-stack register TOS via lines PCst. Succesive CALL instructions will keep pushing the current contents of PC onto TOS as the prior contents are shifted down, so up to four nested subroutines can be accomodated A subroutine is terminated by execution of a return instruction RET which "pops" the stack, returning the contents of TOS to PC via lines PCt, selector PCs and input PCi, allowing the program to continue from the point it had reached prior to the last call or interrupt. When TOS is popped, the addresses in lower registers of ST move up one position. Each subroutine, initiated by a call instruction or an interrupt, must be terminated by a RET instruction.

In an example embodiment, the ROM **14** contains 1536 words, so the remainder of the 4K program address space, 2560 words, is off-chip in the memory **11**. When the memory expansion control pin ME/SE− is high, at logic 1, the device interprets any program address in PC in the 0-to-1535 range as being an on-chip

address for the ROM **14**, and any address in the 1536–4095 range as being an off-chip address so that the PC contents are sent out via RApc and RAo to the RA bus. An output strobe RCLK— generated by the decoder ID2 for every machine state enables the external memory **11** (except when IN or OUT instructions are being executed). When off-chip program memory **11** is accessed, the instruction word read from memory **11** is applied to the external bus D and thus to the internal P-Bus via input/output control DC and lines Dp; this is a 16-bit instruction and, like the output of ROM **14** via IR, it is loaded into decoders ID1 and ID2 for execution, or loaded into PC via PCp, or otherwise used just as an on-chip instruction fetch.

When the ME/SE— pin is at zero the device enters the system emulator mode wherein the entire 4K program address space is off-chip, so all PC addresses are applied to the RA bus via RApc and RAo. This mode is necessary when a user is developing systems or programs, prior to arriving at a final version of code for the ROM **14**. That is, the microcomputer **10** can operate with no code permanently programmed into the ROM so that new programs (stored in RAM or EPROM in the memory **11**) can be tested and debugged, then when the final code is established the chips **10** are produced in large volume with this code mask-programmed into the ROM **14**.

In either mode, the first two program addresses 0000 and 0001 are used for the reset function. When the reset pin RS— is brought low, an address of all zeros is forced into the program counter PC, as will be explained. Also, the third address is reserved for an interrupt vector; when the INT— pin is brought low, an address of 0002 is forced into PC to begin an interrupt routine.

DATA MEMORY ADDRESSING

The data memory **15** in the example embodiment contains 144 16-bit words, and so an 8-bit address is needed on address input **15***a* to the RAM address decoder **15***b*. However, the RAM **15** may be constructed with up to 512 words, requiring a 9-bit address, so the addressing arrangement will be described in terms of address bits which are unused in some embodiments. Each 128 word block of the RAM **15** is considered to be a page, so a 7-bit address field in an instruction word from program memory **14** on P-Bus via input **15***c* is used to directly address up to 128 words of data memory **15**. Two auxiliary registers AR0 and AR1 are employed in the example embodiment; however, up to eight of these 16-bit registers may be used, with the particular one currently being used as the source of the address for the RAM **15** being defined by the auxiliary register pointer ARP. With two registers AR0 and AR1, the pointer ARP is only one bit, but for an embodiment with eight auxiliary registers the pointer ARP is a 3-bit register. The 16-bit auxiliary registers AR0 and AR1 are under control of store, load or modify auxiliary register instructions SAR, LAR, and MAR as will be described. Nine-bit addresses from the low-order parts of the auxiliary registers may be applied to the address input **15***a* via selector **15***d*, , lines **15***e*, selector **15***f* and lines **15***g*. When one of the auxiliary registers is to be the source of the RAM address, the selector **15***d* uses the value on lines **15***e* as the address input **15***a*, whereas if the P-Bus is to be the source of the RAM address the selector **15***d* uses a 7-bit address from input **15***c* and a 1-bit (expandable to 3-bit or 4-bit) page address from the data page register DP. The selector **15***f* is controlled by the pointer ARP which is loaded from P-Bus as defined by an instruction. The auxiliary registers are used for indirect addressing wherein an instruction need not contain a complete address for RAM **15** but instead merely specifies that an auxiliary register is to be used for this address; such instructions can also specify increment or decrement for the auxiliary register selected, in which case the nine LSBs of AR0 or AR1 are changed by +1 or −1 via paths Inc. The auxiliary registers may be thus used as loop counters. The auxiliary registers are accessed by the D-Bus vis lines ARio so these registers may be used as miscellaneous working registers, or may be initially loaded to begin a loop count.

The data memory **15** is accessed via the D-Bus and an input/output circuit **15***i*, via lines **15***j*. Construction of the data memory is such that a data move wholly within the RAM **15** is permitted, according to an important feature of the microcomputer **10**. Under instruction control, the data at one address can be moved to the next higher location in one machine cycle without using the ALU or D-Bus. Thus during an add, for example, the accessed data can be also moved to the next higher address. INPUT/OUTPUT FUNCTIONS

Input and output of data from the microcomputer chip **10** uses the data bus D and two of the lines of the control bus **13**, these being data enable bar (DE—) and write enable bar (WE—). Two instructions, IN and OUT, are employed for the data input and output functions. The external data bus D is coupled to the internal data bus D-Bus by the input/output control and data buffers DC. The output buffers in D1 are tri-state, so the output to data bus D is always placed in a high impedence state except when IN or OUT is being executed; to this end, one of the controls #C from the instruction decode ID1 sets the output buffers in high impdence state whenever IN or OUT is not decoded. When the instruction IN is present, the control DC activates sixteen input buffers, so the external data bus D is coupled to the internal D-Bus via DC and lines Dd for data input. When the OUT instruction is decoded, a control #C from ID1 activates output buffers in DC so the internal D-Bus is coupled via Dd and DC to the external bus D.

Execution of an IN instruction will also generate a data enable DEN— strobe on line **13***a* from ID1, and will couple the D-Bus to the RAM **15** via **15***i* and **15***j*, so the data from external will be entered into on-chip data memory. The intended uses of the microcomputer as a signal processor require hundreds or thousands of accesses to RAM **15** for every off-chip reference. That is, a value will be fetched from off-chip then convolution or like operations performed using this new value and other data in the RAM **15**, so thousands of instruction executions will transpire before another off-chip reference is needed. For this reason, the architecture favors internal data manipulation over off-chip data access.

Execution of an OUT instruction causes generation of an off-chip write enable WE— strobe on line **13***b* from ID1 and outputs data from RAM **15** via **15***i* and **15***j*, D-Bus, lines Dd and buffer DC to the external bus D. Referring to FIG. **1**, this data may be written into one of the ports (selected by the 3-bit RAi value) in the peripherals **12**.

Implicit in both the IN and OUT instructions is a 3-bit port address on lines RAi from ID1. This address is multiplexed onto the three LSBs (RA9–RA11) of the external address bus RA via selector RAs. Up to eight

peripherals may thus be addressed. The remaining high order bits of the RA bus outputs are held at logic zero during these instructions.

THE INSTRUCTION SET

The microcomputer **10** of FIGS. **1** and **2** executes the instruction set of Table A. The Table shows in the first column in mneumonic or assembly language name of each instruction used in writing source code, followed in the second column by the object code in binary which is the form the code appears in the ROM **14** and in the instruction register IR. This binary code is decoded in ID**1** and ID**2** to generate all of the controls #C to execute the desired operation by accessing various busses and registers and setting the functions of the ALU. The Table also gives the number of cycles or machine states employed by the microcomputer in executing the instruction; note that all instructions except branches, calls, table look-up and input/output are executed in one state time. The microcomputer is not microcoded; the standard ALU instructions are executed in one state. The Table also shows the number of instruction words needed to execute each instruction; it is important to note that only branches and call direct require two instruction words. The right-hand column is a brief description of the operation for each instruction.

Most of the instructions of Table A show the low-order eight bits (bits **8–15**) as "IAAAAAAA", which is the direct or indirect RAM **15** address for one operand. If the "I" bit, bit-**8**, is 0, the direct addressing mode is used, so the "A" field of the instruction word, bits **9–15**, is employed as a direct address connected from IR through P-Bus, lines **15***c* and selector **15***d* to address input **15***a*. In this direct addressing mode, the auxiliary registers AR**0**–AR**1** are not used.

For the instructions containing "IAAAAAA", the indirect addressing mode is specified by a 1 in the I field, bit-**8**, of these instructions. The input address on lines **15***a* for the RAM **15** will in this case be obtained from one of the auxiliary registers AR**0** or AR**1**, and bit **15** will select which one. If bit-**15** is 0, AR**0** is used; if bit-**15** is 1, AR**1** is used. Thus bit-**15** coupled from IR via P-Bus controls the selector **15***f* (and can be loaded into the ARP register). Since the number of auxiliary registers is expandable to eight, bits **13–15** of these indirect-address instructions are reserved for use with a 3-bit selector **15***f* and ARP register to define one-of-eight in the indirect addressing mode. Bit-**10** to bit-**12** are controls in indirect addressing: bit-**10** causes the addressed auxiliary register to be incremented if 1, or no change if 0; bit-**11** causes the addressed AR to be decremented if 1 or no change if 0; bit-**12** if 0 causes bit-**15** to be loaded into ARP after execution of the current instruction, or if 1 leaves the ARP unchanged.

The shift code SSSS used in many instructions of Table A is a four-bit field loaded into shift control Sc via Sp to define the number of spaces (zero to fifteen) that the data coming from the RAM **15** via D-bus is left shifted as it passes through the shifter S on the way to the ALU-b input.

Although not material to the structure described herein, assembly language formats using the instruction set of Table A employ "A" to designate direct addressing and "@" to designate indirect. Thus, "ADD S,A" means add contents of memory location defined by the A field of the instruction word. "ADD A@" means add using contents of the data memory location addressed by the auxiliary register AR**0** or AR**1** selected by the existing contents of ARP. ADD S@+ means add using current contents of ARP to define AR then increment this auxiliary register for loop counting. ADD S@ is the same as previous except decrement by 1. ADD S@,AR is same as previous except ARP is loaded with the value of bit-**15** to define a new auxiliary register for subsequent operations.

The descriptions given in the right-hand column of Table A assume direct addressing. For indirect addressing, the above explanation applies.

The ADD instruction thus adds the 16-bit contents of RAM **15** (at location OAAAAAAA for direct, or the contents at the locations in RAM **15** selected by the chosen AR if indirect), shifted SSSS spaces left, to the 32-bit contents of the Acc, and stores the result in the Acc. ADDH does the same except only the high-order half of Acc is the source of one operand and destination of the result, and no shift is performed.

The subtract instructions SUB and SUBH subtract the addressed RAM **15** data from the accumulator and store the result in Acc, but are otherwise the same as add. The load instruction LAC loads Acc with the 16-bit data addressed by IAAAAAAA which is left-shifted by SSSS bits. Only ADD, SUB and LAC specify a shift.

There are four instructions associated with the auxiliary registers: SAR, LAR, LARK and MAR. Store auxiliary register SAR causes the contents of one of the auxiliary registers defined by RRR to be stored in the memory location IAAAAAAA; the load AR instruction LAR is the reverse of SAR. With the LARK instruction a constant K from IR (bits **8–15**) is loaded into the AR defined by RRR; this 8-bit constant K is right-justified and MSBs set to zero in the 16-bit auxiliary register. The modify auxiliary instruction MAR causes one auxiliary register to be modified by bits-**10** to **12** as above, but no add or memory **15** access is implemented. The MAR code is operative only in the indirect mode, I=1; in direct mode this instruction results in no-op.

The input/output instructions are written in assembly language as "IN PA, A" or "OUT PA, A", where PA is the 3-bit port address PPP output on bits **9–11** of the RA bus (generated from the decoder ID**1** and coupled via lines RAi). IN enables DEN− and disables RCLK−, while OUT enables WE− and disables RCLK−. The peripheral devices **12** decode RA**9**–RA**11** to select one of eight 16-bit ports or locations for read or write via the bus D. These instructions use two machine states so that the data input pins of bus D are free on the second state to allow external fetch of the next instruction from memory **11** instead of ROM **14**.

The store accumulator instructions SACL and SACH, written as "SACL X,A" in assembly, cause the low or high order bits of Acc to be left-shifted XXX places and stored in the data memory **15** at the location defined direct or indirect by IAAAAAAA. The X field is not fully implemented in the example embodiment; for SACL only X=0 is allowed and for SACH only X=0, X=1 and X=4 are allowed. This shift is implemented in the accumulator circuitry itself rather than in the shifter S.

The arithmetic and logic instructions without shift code are ADDH, ADDS, SUBH, SUBS, SUBC, ZALH, ZALS, EXOR, AND, OR and LACK. These are all written as ADDH A, for example, in assembly language. ADDH causes the 16-bit data from the defined location in RAM **15** to be added to the high-order

half of Acc and stored in the high-order half of Acc; actually the data from RAM **15** is left shifted sixteen bits in shifter S as it goes from D-Bus to the ALU-b input. The ADDS instruction means that the sign extension is suppressed in the shifter S; the data from RAM **15** defined by A is treated as a 16-bit positive number instead of a signed 2's complement integer. SUBH and SUBS correspond to ADDH and ADDS except subtract is performed in the ALU.

The conditional subtract instruction SUBC is used in divide operations. The contents of the defined location in RAM **15** are subtracted from the contents of Acc and left-shifted fifteen bits, producing an ALU output ALU-o which, if equal to zero is left-shifted by one bit and a +1 is added, with the result stored in Acc. If the ALU output is not equal to zero then it is left-shifted by one-bit and stored in Acc (the +1 is not added). SUBC is a two-cycle instruction that assumes the accumulator is not used in the following instruction. If the following operation involves Acc then a NO OP instruction should be inserted after SUBC.

The "xero accumulator load high" instruction ZALH fetches the 16-bit word at the addressed location in the RAM and loads it into the high-order half of Acc (bits **0–15**); the Acc has been zeroed, so the low-order bits **16–31** reamin zero. The shifter S is in the data path from D-Bus via ALU to Acc, so a 16-bit shift is performed in ZALH to move the data to the high-order half. The ZALS instruction fetches a word from RAM and loads it into the low-order half of the zeroed Acc, with sign extension suppressed in the shifter S.

The logic operations EXOR, AND and OR are performed in 32-bit format, even though the operand fetched is sixteen bits. For EXOR, the high-order half of Acc is Exclusive Or'ed with zeros, concatenated with Exclusive Or of the fetched data with the low-order half of Acc, both halves of the result being stored in Acc. The same applies to OR and AND.

The load accumulator instruction LACK causes an 8-bit constant contained in the eight LSB's of the instruction word to be loaded into the eight LSB's of Acc, right justified; the upper twenty-four bits of Acc are zeroed. To accomplish this operation, the instruction word on P-Bus from IR (after ID1 and ID2 are loaded, of course), is coupled to the D-Bus by BIM, and thence to the ALU-b via shifter S (with no shift). The ALU performs "pass ALU-b" or add zeros to b, leaving the constant in Acc.

The data shift or data move instruction DSHT causes the contents of the defined location in the RAM **15** to be moved to the defined location plus one. This is accomplished internal to the RAM **15** without using the ALU or data bus D-Bus. The operation cannot cross a page boundry, however.

The "load T" instructions are used to set up multiply operations. LT causes the T register to be loaded from RAM **15** with the value defined by IAAAAAAA. The "load T with data move" instruction LTD employs an operation like DSHT in the RAM; the T register is loaded with the contents of the RAM **15** location defined by IAAAAAAA, then this same value is shifted to location IAAAAAAA+1, and also the contents of Acc is added in ALU to the contents of the P register with the result going to Acc. The LTA instruction is the same as LTD but without data move; the T register is loaded from RAM **15** and the P register is added to Acc, with result to Acc.

The multiply instruction MPY causes the 16-bit contents of T register to be multiplied in multiplier M (not using ALU) by the value from RAM **15** on the input Mi from D-Bus, with the 32-bit result going to the P register. The "multiply constant" instruction MPYK causes the 16-bit contents of T register to be multiplied by a 13-bit constant C from the opcode in IR; the 32-bit result stays in P register. For MPYK, the constant is connected from IR to Mi via P-Bus, BIM and D-Bus.

The "load data page" instructions LDPK and LDP cause the data page register DP to be loaded with up to eight bits from the opcode itself or from the defined location in RAM **15**. In the embodiment shown, the DP register is only one bit, but in other embodiments with a larger RAM **15** the DP register contains up to eight bits. The page address remains the same until a new load page instruction occurs.

The load status and store status instructions LST and SST are used in call subroutine or interrupts to save the contents of the status circuits SD, or restore status SD. These instructions are used instead of hard wired circuits for performing this function.

The disable and enable interrupt instructions DINT and EINT are used to mask or unmask the interrupt capability, i.e., these instructions reset or set a latch which determines whether or not the microcomputer **10** responds to the INT− pin.

An absolute value instruction ABS functions to assure that the accumulator contains only an absolute valve, i.e., if Acc is less than zero, the absolute value of Acc is loaded into Acc, but if Acc is greater than zero there is no change. Similarly, the zero accumulator instruction ZAC clears Acc.

The overflow mode instructions RAMV and SAMV cause the overflow mode latch OVM in the status decode SD to be set to 1 or reset to 0. When set, the ALU output is set to its maximum or minimum before loading into Acc upon overflow. This simulates the effect of saturating an amplifier in an analog circuit, and is useful in signal processing.

Three P register instructions PAC, HPAC and SPAC are used in manipulating data after a multiply MPY or MPYK. PAC loads the accumulator with the contents of the P register by passing the 32-bit data through the ALU without performing any operation to modify the data; actually the ALU-a input is zeroed and an ADD is executed. The APAC instruction adds the contents of the P register to the contents of Acc, with the result going to Acc. Similarly, the SPAC subtracts the contents of P register from Acc, result to Acc.

The subroutine instructions are CALL, CALLA and RET. CALL is a two-word instruction; the first word is the opcode and the second is the absolute address of the first instruction in the subroutine. When CALL is decoded in ID2, PC is incremented to fetch the next instruction word which is the address, then the incremented contents of PC are pushed to stack ST. The subroutine ends in return RET which causes the address on TOS to be popped and loaded into PC. To save status, SST must be used before CALL, and LST inserted after RET. The CALLA instruction is unique for a Harvard architecture machine; this uses the contents of Acc as the subroutine address rather than using the next location addressed by PC+1. The low-order bits of Acc are transferred via Acc-L and BIM to the P-Bus and thus via PCp to the program counter PC. The incremented PC is saved in CALLA by pushing to ST just as in a CALL.

The table look up instructions TBLR and TBLW also employ the Acc as an address source. These instructions require three states to execute. The RAM **15** location defined by IAAAAAAA is transferred via D-Bus and BIM to P-Bus, and thus via PCp to PC, from whence this address is applied via RApc to the external RA bus, or to ROM **14**.

The branch instructions all require two words, the first being the opcode and the second at PC+1 being the address. The low-order bits **8–15** of the opcodes are unused. Unconditional branch B loads the word at PC+1 into PC as the next address. BARNZ is conditional upon whether or not a loop counter, one of the auxiliary registers defined by ARP, is not-zero. BV causes a branch if the overflow bit OV in the status decode SD is a 1. BIOZ causes a branch if the IO bit from I/O ST− is a 1 in the status decoder SD. The six instructions BLZ, BLEZ, BGZ, BGEZ, BNZ and BZ are all dependent upon the defined condition in SD reflecting the condition in Acc.

SYSTEM TIMING

Referring to FIGS. *3a–3ii*, the timing of the system of FIG. **1** and the CPU chip of FIG. **2** is illustrated in a sequence of voltage vs. time waveforms or event vs. time diagrams. The chip **10** includes a clock generator **17** which has two external pins X1 and X2 to which a crystal (or external generator) is connected. The basic crystal frequency is up to 20 MHz and is represented by a clock **0** of FIG. *3a*. This clock **0** has a period of 50 ns, minimum, and is used to generate four quarter-cycle clocks Q1, Q2, Q3 and Q4 seen in FIGS. *3b–3e*, providing the basic internal timing for the microcomputer chip **10**. A set of four quarter cycle clocks Q1 to Q4 defines one machine state time of 200 ns, minimum; the states are referred to as S0, S1, S2, in FIG. **3**. The clock generator **17** produces an output CLKOUT, FIG. *3f*, on one of the control bus lines **13**. CLKOUT has the same period as Q1, but 50% duty cycle and beginning at the midpoint of Q1. This output is used for timing or synchronizing external elements of the system of FIG. **1**.

Internally, the microcomputer **10** executes one instruction per state time for most types of instructions, so five million instructions per second are executed. Of course, some instructions such as input/output, branch, call or table look-up require two or three state times. Assuming a sequence of single-state instructions such as add, load, store, etc., a new address is loaded into PC during each Q3 as seen in FIG. *3g*, then the ROM **14** is addressed during Q4 and Q1 so an instruction word output is produced from IR onto P-Bus starting in the next Q2 and continuing through Q3, as seen in FIG. *3h*. The ROM **14** access time is thus about 100 ns. If an external instruction fetch from memory **11** is used, the same access time applies. The instruction decoders ID1 and ID2 receive the instruction word from P-Bus during Q3 as seen in FIG. *3i*, and most of the decoder outputs #C are valid during Q1, although some fast controls are available in Q4. For direct addressing of the RAM, the address on bit-**9** to bit-**15** of P-Bus is immediately gated into the RAM decoder **15***b* when P-Bus becomes valid, but in either direct or indirect the RAM address is valid by the beginning of Q3 as seen in FIG. *3j*. For RAM read, the data output via **15***j* to D-Bus is valid on Q4, FIG. *3j*, and this data passes through the shifter S, FIG. *3k*, and is available as an ALU input during Q1, FIG. *3l*. The ALU controls #C are valid in Q2 and ALU output ALU-o is available during Q3. The accumulator Acc is loaded from ALU in Q4, FIG. *3m*.

It is thus seen that an ADD instruction, for example, for which fetch began at Q3 of the S0 state in FIGS. *3a–3m*, will be completed, i.e., the result loaded into Acc, in Q4 of state S2. There is substantial overlap of instruction execution. A new instruction fetch begins during Q3 of each state time, so execution of two more instructions have begun before one is finished.

Not shown in FIGS. *3a–3m* is the write-RAM function. The RAM **15** is always written into during Q2. Addressing the RAM is always during Q3, however. Thus, an instruction such as "store accumulator low" SACL is illustrated in FIGS. *3n* and *3o*. The RAM address is received from the instruction register via P-Bus on Q3 of S1 (assuming the SACL instruction was fetched beginning at Q3 of S0), and the write will not occur until Q2 of state S2. During the read slot, Q4 of S1, a refresh occurs for the addressed row of the RAM, then the same address stays until Q2 of state S2 for the write. The D-Bus is loaded from Acc during this same Q2, see FIG. *3n*.

If the accumulator must perform the saturate function in the overflow mode, i.e., OVM set to **1**, this will be performed after the load accumulator function of FIGS. *3m*. That is, for the ADD instruction of FIGS. *3a–3m*, the Acc is saturated during Q1 if the next state S3, so that when the accumulator is accessed by the following instruction it will be available to load the D-Bus on Q2.

When an instruction uses the data move function within the RAM **15**, the move operation occurs during Q1 as illustrated in FIG. *3o*. Also, if the increment loop counter function is performed for the auxiliary registers AR0 or AR1, the increment (or decrement) is executed in Q1. The T register, auxiliary registers AR0 or AR1, ARP latch, DP register and stack ST registers are each loaded during Q2 of any state time if these functions are included in the current instruction.

The bus interchange module BIM always executes a transfer from D-Bus to P-Bus beginning in Q2, if this function is defined by the instruction. The transfer from P-Bus to D-Bus by BIM is begun during Q4. The D-Bus is precharged on Q3 of every cycle, so no data can carry over on D-Bus through Q3 of any state, nor can data be loaded to or from D-Bus during Q3.

The program counter PC is incremented by the PCinc path during Q3 of each state time. That is, the load PC function of FIG. *3g* is the incremented value just generated.

Execution of a branch instruction is illustrated in FIGS. *3p–3r*. If the instruction loaded into the decoders ID1 and ID2 during Q3 of state S0 is a branch, the status decode SD bits from the previous instruction are valid during Q1 of S1 so the decision of branch or not is made at this point. Meanwhile, of course, another instruction fetch has begun so if the branch condition is met the instruction delivered to P-Bus during Q2 of S1 is used as the next address; if the condition is not met, however, this instruction is discarded. Assuming the condition is met, the branch address is loaded from IR via P-Bus to PC during Q3 of S1, and the new instruction delivered to IR and P-Bus in Q2 of S2 then decoded and executed beginning at Q3 of S2, FIG. *3r*.

A CALL instruction is executed in the same time sequence as a branch, seen in FIGS. *3p–3r*, except no SD evaluation is needed, and PC+1 is pushed to stack ST during Q3 of S1.

A return instruction RET is a two cycle instruction as illustrated in FIGS. 3*s*–3*u*. If the instruction loaded into the decoders ID1 and ID2 during Q3 of state S0 is RET, the instruction fetch which began with PC+1 and load PC in Q3 of S) is discarded and a pop stack function is performed in Q3 of S1 so the next instruction fetch is to the return address. The instruction fetched during Q4 of S1 is then decoded and executed beginning at Q3 of S2.

Input (or output) instructions are executed in two cycles as illustrated in FIGS. 3*v*–3*x*. Assume the opcode loaded into the decoder ID2 in Q3 of S0 is IN. The instruction fetched beginning at Q3 of S0 is not used; execution is inhibited by the decode of IN. The contents of PC at Q3 of S1 are saved until Q3 of S2 for the next instruction fetch; that is, PC is recirculated back to PC by the increment path, but no increment is performed. The controls #C produced from decode of IN are available for two states. The RAM address is loaded from P-Bus on Q3 of S1, seen in FIG. 3*y*, and the data input reaches D-Bus on Q4 of S1 and is written into RAM 15 during Q2 of S2. The DEN− control is active from Q4 of S1 through Q2 of S2 for the IN function. An OUT instruction is executed like IN except the RAM 15 is read during Q4 of S1 and the WE− control is active instead of DEN−.

A table look up instruction is executed as shown in FIGS. 3*aa*–3*cc*. The TBLR opcode is decoded beginning at Q3 of S0 and causes the Acc to be loaded via D-Bus to BIM in Q2 of S1, then PC is loaded via P-Bus from BIM in Q3 of S1 so the content of Acc is used as the next instruction fetch address. Meanwhile, execution of the instruction fetched beginning at Q3 of S0 is inhibited by preventing a ROM read control #RR from loading IR with the ROM 14 output, at Q2 of S1. The incremented contents of PC from Q3 of S0 are pushed to ST during Q3 of S1, then popped at Q3 of S2 as the next instruction address. The data fetched from ROM 14 (or memory 11) using the address from Acc during Q4/S1 to Q1/S2 is loaded onto P-Bus during Q2 of S2 where it remains until Q4 of S2 at which time the BIM accepts the data from P-Bus and then transfers it to D-Bus on Q2 of S3, the next state. The destination address for RAM 15 loaded into decoder 15*b* from P-Bus by Q3 of S1 and remains for two states, so the RAM write occurring at Q2 of S3 will use the RAM address defined in the original TBLR opcode.

One of the problems inherent in manufacturing microcomputer devices is that of testing the parts to determine whether or not all of the elements are functional. In many microcomputers, the instruction words read from the internal ROM are not available on external busses and so the ROM cannot be checked in any way other than by executing all possible functions, which can be lengthy. The device of FIG. 2 allows the ROM 14 to be read out one word at a time using the interchange module as illustrated in FIGS. 3*ee*–3*hh*. A test mode, not part of the instruction set of Table A, is entered by holding the I/O ST− pin at above Vdd, for example 10V, and holding RS− low, producing an input to the decoders ID1 and ID2 causing a ROM output function in which the ROM 14 is accessed every cycle and PC incremented as seen in FIG. 3*ee*. The P-Bus receives the ROM output, FIG. 3*ff*, but the opcodes are not loaded into the decoders ID1, ID2. Instead, the BIM accepts the opcodes from P-Bus on Q4 of each cycle and transfers to D-Bus on the next Q2, as seen in FIG. 3*hh*.

THE CHIP LAYOUT

In FIG. 4, the microcomputer 10 of FIGS. 1 and 2 is illustrated in chip layout form. This is a top view of an MOS/LSI chip which is about 150 mils on a side. A major part of the area of the chip 10 is occupied by the memory including the ROM 14 and RAM 15 with their address decoders, and by the 16×16 multiplier M. The ROM 14 has associated with it an X address decoder 14X and a separate Y address decoder 14*y* for instruction word output; twelve address bits are used to define one of up to 4096 16-bit words in the ROM 14, although in this example only 1536 are on-chip.

The RAM 15 has an X address decoder 15*b*–*x* which selects 1-of-72 row lines, and a Y address decoder 15*b*–*y* and sense amplifiers 15*s* which select 1-of-2 column lines, so only eight bits are needed for the RAM select in this embodiment (eight bits could accomodate a 256 byte RAM).

The busses RA and D have twelve or sixteen bonding pads on the chip (total of twenty-eight) for connection to external, and the areas of the chip around these bonding pads seen in FIG. 4 are occupied by the buffers used for the ports. It will be noted that the RA bus is only used for output, so only output buffers are needed for this port, while the D-Bus requires tri-state output buffers as well as input buffers.

The multiplier M, shifter S, ALU, accumulator Acc and auxiliary registers AR0, AR1 on the chip 10 of FIG. 4 comprise a 32-bit wide "strip" which is an array of rows (parallel to control lines #C) and columns (parallel to metal bus lines such as D-Bus and P-Bus and ALU and register bits) containing all of the 16-bit and 32-bit registers, ALU bits, and the like circuitry associated with the D-Bus and related control lines #C. As set forth in U.S. Pat. No. 4,402,044 issued to McDonough and Guttag, assigned to Texas Instruments, an important feature is that the 32-bit ALU and its associated 32-bit Acc registers, the two 16-bit AR registers, the shifter S, and the bus interchange BIM as described above are laid out on the MOS/LSI chip 10 in a regular strip pattern as seen in FIG. 4. Other circuitry connected to the D-Bus and the ALU-b input and having controls #C shared by sixteen or thirty-two bits may also be in the strip, such as AR and BIM. The Acc and the ALU each contain thirty-two bits or stages which are laid out in a regular pattern like memory cells, the bits arrayed and aligned horizontally and vertically as seen in FIG. 4. D-Bus and P-Bus of FIG. 2 are each sixteen parallel metal strips on top of the cells of the ALU and registers, and all of the dozens of control lines #C are horizontal polysilicon lines typically used as the control gates for transistors in the ALU and its associated registers and like circuitry. This layout arrangement is advantageous because the multiplier ALU and registers, and perpendicular control lines #C and metal busses fit in an array with virtually none of the wasted space used merely for routing conductors in conventional contruction of microprocessors. Metal bus lines such as P-Bus and D-Bus and control lines #C are in large part routed over functional regions or cells of the chip in the strip rather than over unused silicon, and many 90 degree turns are produced inherently at functional cells rather than in conductor routing. In the prior devices, the controls, the registers, the ALU, etc. where islands of circuitry connected by busses or conductors. The enlarged view of FIG. 4*a* shows a small part of the strip, two-bits wide, illustrating the metal bus

lines and the polysilicon control lines #C for an N-channel silicon gate MOS device made generally by a single-level polysilicon process according to U.S. Pat. No. 4,055,444, assigned to Texas Instruments. Various contacts (not shown) would be made within each register bit or stage from metal to silicon or to polysilicon. It is significant to note that many of the connecting lines from registers to busses illustrated in FIG. **2** are not physically lines or elongated conductors at all but instead are merely metal-to-silicon or metal-to-poly contact areas along the metal bus lines of FIG. **4***a*. That is, routing of 16-bit or 32-bit sets of parallel conductors is minimized by the strip feature, and the size of the chip **10** is reduced. All busses are not needed in any one part of the strip, and thus the pitch or maximum width of cells of the strip is minimized since the the metal-to-metal spacing is a critical limiting factor in bit density.

The internal program of the microcomputer **10** may be modified at the gate level mask in making the chip. The macro code or program in the ROM **14** is defined by a single mask in the manufacturing process as set forth for example in U.S. Pat. Nos. 3,541,543, 4,208,726 or 4,230,504, assigned to Texas Instruments. By rewriting this user or macrocode, keeping the instruction set defined by ID1 and ID2 the same, a wide variety of different functions and operations are available.

ARITHMETIC LOGIC UNIT

A detailed schematic diagram of one bit of the 32-bit ALU is shown in FIG. **5***a*. The ALU operates under control of six of the #C commands from the instruction decode ID1, these commands being labelled #AUM-0–#AUM4 (valid on Q2) and #AUAB (valid on Q1). The ALU-a input, inverted, is on line AUa and the ALU-b input inverted, is on line AUb, both being valid on Q1, one from Acc and the other from the shifter S or P register. The ALU output is at line AUc, valid on Q4, representing one of the inverted 32-bit parallel output ALU-o to Acc. Table B shows the function produced by operation of the ALU for various combinations of the six #C commands. This ALU is generally the same as U.S. Pat. No. 4,422,143, issued to Karl M. Guttag, assigned to Texas Instruments. Propagate and generate nodes AUp and AUg are precharged on Q1 and conditionally discharged by transistors AUd controlled by the ALU-a input, transistor AUe controlled by the ALU-b input and its complement, and transistors AUf controlled by the #AUM0–#AUM3 commands, according to the functions of Table B. A carry-out node AUh and a carry-in node AUi for each bit are coupled by a propagate-carry transistor AUj controlled by a line AUk which is the propagate node AUp inverted. The carry-out node AUh is precharged on Q1 and conditionally discharged via transistor AUm which is controlled by a NOR gate having the generate node AUg as one input and the absolute value command #AUAB as the other, so if #AUAB is 1 the transistor AUm is off and carry-out bar is always 1, meaning no carry or absolute value. If #AUAB is 0, the generate signal on AUg controls. The inverted propagate signal on AUk is one input to an Exclusive Nor circuit AUn with static load AUq; the inverted carry-in bar of line AUi is the other input to the Exclusive NOR, resulting in an output AUr which inverted is the ALU output AUc. The carry-in bar node AUi is made unconditionally 0 when control #AUM4 is high for logic functions OR, AND and EXOR, so this input to circuit AUn is unconditionally 1, but for ADD, SUB, etc., the control #AUM4 is 0 and the carry-in from the node AUu of the next low-order bit of the ALU controls.

THE SHIFTER S

Referring to FIG. **5***b*, the shifter S includes a 16-bit input Si, a shift matrix Sm, a shift controller Sc, and a 32-bit output So going to the ALU-b input. The input Si is connected to receive the D-Bus at all times and to drive lines Sf in the matrix Sm through high level buffers. If no shift is to be performed, a line Sg is high, turning on all sixteen of the transistors Sh for this line, so the 16-bit data on lines Sf will appear on the sixteen right-most output lines So via diagonal lines Sj. All of the lines Sf are precharged on Q3 via thirty-two transistors Sk then conditionally discharged by the input Si. The sign bit is extended by detecting the MSB bit-0 of the input Si by the line Sm. A gate Sn also receives a #NEX not extend command from ID1 (one of the controls #C) to kill the sign extension for certain instructions of Table A. Based on the incoming sign bit Sm and #NEX, the gate Sn generates an extend command on line Sq to transistors Sq'. The transistors Sq' in series with lines Sr conditionally discharge the nodes Ss on lines Sf through transistors St. The control Sc is a 1-of-16 decoder or selector which receives the bits 4–7 of the instruction word from the P-Bus on 4-bit input Sp during Q3 and activates one of the sixteen lines Su; the lines Su are precharged in Q3 via transistors Sup and conditionally discharged during Q4 via transistors Sud and Sc'. The controls for the shifter S consist of the 4-bit value on Sp (the SSSS field of the ADD instruction, for example) defining the number of positions of left shift, and controls on lines #C for negating sign extension, etc. Since the data is usually in two's complement, the sign bit is extended to all bits to the left of the most significant data bit. The sign bit is 0 for positive and 1 for negative. If the shift is to be seven bits, for example, the seventh line Su stays high on Q4 and all others go low. This turns on all transistors Sh and St in the seventh row and all other transistors Sh and St are off. The 16-bit data coming in on lines Si thus moved via transistors Sh and lines Sj to a position on lines So seven bits to the left of the zero shift (right-most) position, and zero-filled to the right due to the prcharge Sk. To the left, the sign bit will stay 0 is the bit-0 is low, but if bit-0 is 1 then Sq is high, transistors Sq are on, allowing all bits to the left to discharge.

BUS INTERCHANGE MODULE

The bus interchange module BIM, shown in detail in FIG. **5***c*, consists of sixteen identical stages, only one of which is illustrated. Each stage has two clocked inverters Ia, with no feedback loop since data is not held in BIM longer than about half a state time. Input node Ib is connected to the respective bit of P-Bus via one of sixteen transistors Ic driven by a control bit #BIFP valid on Q4. The D-Bus is connected to the input node Ib via transistors Id driven by the control bit #BIFD (Bus Interchange From D) from decoder ID1 valid on Q2. The output node Ie is connected to the P-Bus by a push-pull stage including transistors If and Ig, and a transistor Ih driven by a control bit #TP, valid during Q2 and Q3. Likewise, output node Ie is coupled to the D-Bus via a push-pull stage having driver transistors Ii and Ij, and a transistor Ik driven by a control bit #BITD valid on Q2 and Q4. The transistors Ig and Ij are driven by node Im at the output of the first inverter Ia, providing a push-pull output. Data is transferred

from D-Bus to nodes Ib, Im, Ie on Q2, and then from these nodes to P-Bus on Q4. Similarly, data is transferred from P-Bus to nodes Ib, Im, Ie on Q4, and then from these nodes to D-Bus on Q4 on the next Q2.

THE MULTIPLIER

Referring to FIG. 5*d*, a schematic representation of the multiplier M and its T and P registers is shown, and corresponding detailed circuit diagrams are shown in FIGS. 5*e*, 5*f*. The 16-bit output of the T register is applied to a set of eight Booth's decoders Mb which produce eight sets of outputs Mc, each set including five functions: shift or no shift, and add, subtract or zero. A set of eight banks of 17-it static carry-feed-forward adders Ma-1 to Ma-8 receive the Mc inputs when the T register is loaded, and so a significant part of the multiplication function is initiated before the MPY instruction is executed. The adders Ma-1 to Ma-8 are static in that no clock Q1–Q4 is needed to cause them to operate. Each stage of each level or bank includes a control section Mm responsive to the decoder outputs Me, and the control section feeds an adder. Level Ma-2 uses half adders and levels Mc-3 to Mc-8 use full adders. The first level Mc-1 does not need an adder because there is no partial product from the prior stage, so it has only the control section. When the MPY instruction is decoded, on Q4 the second operand is applied to the static adders from D-Bus by 16-bit input Mi. As each level of the eight levels of adders Ma-1 to Ma-8 calculates the sum, the partial product is fed forward via lines Mf to the next higher level, except for the two LSBs of each level which are fed to the dynamic adders Md via lines Me. When the static adder array settles, the 17-bit output Mg from the level Ma-8 plus the seven lower level 2-bit LSB outputs Me, is applied to a carry-ripple adder MD(31-stages) to perform the final carry evaluation, producing a 31-bit product in two's complement notation. The 31-bits are sign extended to obtain a 32-bit product in the product register P.

Booth's 2-bits algorithm reduces the number of adder stages to about half the number otherwise required. When performing multiply in the classic pencil and paper method, the right or LS digit of one operand is multiplied by the other operand to produce a partial product, then the next digit is multiplied to produce another partial product which is shifted one digit with respect to the first. Booth's algorithm gave a method of multiplying in binary which allowed two bits to be treated each time, instead of one. Thus, level Ma-1 multiplies the two LSBs of T reg times all bits of D-Bus, producing a partial product Me and Mf. The second level Ma-2 multiplies the next two bits of T reg to D-Bus, adds the partial product Mf from Ma-1, and generates a new partial product Mf and two more bits Me because this operation shifts two bits each level.

In FIG. 5*e*, one of the eight decoders Mb is shown, along with two bits of the T register. The T register stage consists of two inverters Ia with a recirculate transistor Rc clocked in Q4. The stage is loaded via transistor Ta by a #LT command from ID1 occurring on Q2 during an LT instruction. The outputs of two stages of the T register and complements are applied by lines To and Tc to one Booth decoder Mb. The decoder consists of four logic circuits, each having a static load Ba, Bb, Bc or Bd and a pattern of transistors Be with the lines To and Tc applied to the gates. Two of the terms have 1 or 0 fixed in the gates by lines Bf. Outputs Mc-1 and Mc-2 represent no-shift and shift commands and come from the logic stages Be and Bd. Outputs Mc-4 and Mc-5 are true and complement outputs from load Ba of the first of the logic circuits, and these represent add and subtract commands. The output Me-3 from Bb is the zero command.

The first level Ma-1 of the static adders is simpler than the higher levels in that only the D-Bus input Mi and the inputs Mc are involved, with no partial product. Two stages of this first level are seen in FIG. 5*g*, along with two of the seventeen stages of level Ma-2 and level Ma-3. The control sections Mm are all the same on all levels. Note that no elements are clocked.

The decoders Mb and control sections Mm with controls Mc define the Booth's two-bits at a time algorithm which reduces circuitry and increases speed by a factor of two. When two bits are interrogated successively, the only operations required are add, subtract, do nothing or shift by one bit. Considering the input from T as one operand, and from D-Bus as the other, the following table describes the function

Ti + 1	Ti	(Ti − 1)	Function	Partial Product
0	0	(0)	Do nothing	K + O
0	0	(1)	Add D	K + D
0	1	(0)	Add D	K + D
0	1	(1)	Shift D & Add	K + 2D
1	0	(0)	Shift D & Add	K − 2D
1	0	(1)	Subtract D	K − D
1	1	(0)	Subtract D	K − D
1	1	(1)	Do nothing	K + O

An example of multiplication using Booth's two bit algorithm is as follows:

D = 001101 (= 13 decimal)
T = 100111(0) (= −25 decimal)

	Ti+1	Ti	(Ti−1)	
000000000000	1	1	(0)	→ K − D
1111111(10011)	0	1	(1)	→ K + 2D
000(001101)0	1	0	(0)	→ K − 2D
1(110011)0				
111010111011				

(= −325 decimal)

In the control sections Mm the inputs Mi from the D-Bus are controlled by a transistor Mm-1 and control Mc-1, not shift. The Mi input for the adjacent bit is gated in by transistor Mm-2 and the Mc-2 shift command, providing the "2D" function as just described. The zero is provided by transistor Mm-3 and zero control Mc-3 which results in mode Mm-4 being connected to Vcc (zero in two's complement). The carry-in from

the prior stage is on line Mm-5, and the partial product from the prior stage is on line Mm-6. The add or subtract control is provided by transistors Mm-7 controlled by the Mc-4 and Mc-5 add and subtract commands. The full adder includes logic gate Mn-1 receiving the outputs of the control section, as well as gates Mn-2 and the exclusive Nor Mn-3, producing a sum on line Mn-4 and a carry on line Mn-5. Speed is increased by using carry feed forward instead of carry ripple on the same level. Level Ma-1 has no partial product or sum Mm-6 from the prior stage, nor carry-in Mn-5, so the adder is not needed, only the control, producing a sum (a difference) at mode Mn-8 and no carry. The second level Ma-2 is a half adder since no carry feed forward is received from Ma-1.

One of the adder stages of the 31-stage ripple-through carry adder is shown in FIG. 5*f*, along with one stage of the P register. The adder stage receives two inputs Me, gated on Q1 or Q3 by transistors Md1. The six LSBs of adder Md have their inputs gated in on Q1 because the static array levels Ma-1, Ma-2 and Ma-3 will have settled and outputs Me will be valid at this point, so the add and ripple through in Md can begin, although the outputs Mf are not yet valid. Thus, the more significant bits are gated on Q3 at transistors Md1. A carry input Md2 from the next lower-significant stage is applied to one input of an exclusive NOR circuit Md3, and to a carrry output gate Md4 which produces a carry output Md5 to the next higher stage. A propagate term is generated from the inputs Me and the carry-in by logic gate Md6, and a carry generate term by a logic gate Md7 with Md4. The same output Md8 is connected by line Md9 to the input of the P register stage, gated by #LPR (load P Reg) from ID1 on Q4 by transistor Pa. The P register stage consists of pair of inverters Ia and recirculate transistor Rc gated on Q2. The output is applied to the ALU-b input on Q1 by gate Pb with #NRPR (not read P Reg) from ID1 as one input, along with an inverter Pc. Transistor Pd precharges the ALU-b input on Q4.

The timing of the multiplier operation is illustrated in FIGS. 3*jj* to 3*mm*. On Q2 of So, the register is loaded and outputs Mc from the Booth's decoder become valid. The Mi inputs from D-Bus are valid at Q4 of S1, assuming the MPY instruction is valid in decoder ID1 at Q3 of S1. The lower bits of the dynamic adder Md are loaded with Me on Q1 of S2, via Md1, and the carry begins to ripple through the lower of the 31-bits, then this continues in Q3 of S2 through the output Mf of the upper levels, so P register is loaded on Q4 of S2 via Pa, where the data remains until loaded to ALU-b on Q1 of a succeeding cycle.

THE RAM

The cell used in the RAM 15 is a pseudo-static 6-transistor cell as seen in FIG. 5*g*. This cell differs from the traditional 6-transistor static cell in that refresh transistors 15*m* are used in place of polysilicon resisters or depletion transistors used as load impedences. The implanted resistors or depletion devices are larger and interpose process complexities. The storage nodes 15*n* are connected through cross-coupled driver transistors 15*p* to ground; one transistor 15*p* is on and the other off, storing a 1 or 0. Read or write is through access transistors 15*q* to data and data bar lines 15*r*, with gates of the transistors 15*q* driven by a row address line 15*s*. Refresh is accomplished when the refresh line 15*t* is pulsed high allowing the node 15*n* which is at 1 to be charged back up to a level near Vdd, while the 0 node 15*n* will conduct the pulse of current to ground through the on transistor 15*p*. The row address on 15*s* is delayed slightly from the refresh line 15*t* so that both won't begin at the same time. In the timing sequence of the FIGS. 3*a*–3*e*, particularly FIGS. 3*j* and 3*o*, the cell of FIG. 5*j* is read in Q4 of any cycle, or written into on Q2.

Referring to FIG. 5*k*, several of the cells of FIG. 5*g* are shown in a column. The data and data bar lines 15*r* are precharged to Vdd-Vt on Q1 and Q3 by transistors 15*u*. The refresh address on lines 15*t*-0, 15*t*-1 and 15*t*-2, etc., occur in sequence, one-at-a-time, generated by a ring counter; for example, if the RAM 15 is partitioned in 64 rows, then a 64 bit ring counter generates one refresh address bit each state time, refreshing the entire array once each 64 states. The refresh pulse occurs on a line 15*t* during Q3, while transistors 15*u* precharge and equallize the data and data bar lines. A row address on a line 15*s* might begin to come up to 1 during the later part of Q3 since read access is in Q4, so the sizes of the transistors are such that nodes 15*n* will not be both forced to Vdd-Vt when transistors 15*m* and 15*q* are all turned on. The on transistor in the pair 15*p* will hold the 0 node lower than the 1 node. After the refresh pulse on 15*t* goes low, for a cell addressed for both read and refresh in Q3, the delayed Q3 address line stays high momentarily to assure that the zero-going line 15*r* will discharge at least slightly through 15*q* and 15*p* for the 0 side. Then a bistable sense circuit including cross-coupled transistors 15*v* is activated by transistor 15*w* having Q4 on its gate (delayed slightly to make sure Q3 has gone to zero). This flips the data and data bar lines to full logic level, after which the column access transistors 15*y* are activated for the addressed column and data can be read out onto the D-bus. Internal shift is implemented by lines 15*x* connecting nodes 15*z* to adjacent column lines 15*r* via transistors 15*z* activated by a RAM move command #RM from decoder ID1, occuring on Q4. The data is held until Q2 of the next cycle (after Q1 precharge of all data and data bar lines 15*r*) before being applied to the adjacent column for this move operation. Meanwhile, the row address may be incremented by 1; i.e., the next higher line 15*t*-1, etc., goes high so on Q2 the data is written into the next higher location.

The sixteen bits of the RAM 15 are arranged as seen in FIG. 5*i*, with column lines (data and data bar lines) 15*r* running vertical and row lines 15*s* horizontal. The RAM is only 32-columns wide, so the column select 15*y* is merely one-of-two, even or odd. There are in this embodiment 144 row lines 15*s*. The LSB of the address 15*b* to the RAM is the column address, even or odd. To implement the data move operation, on even columns the LSB of the address buffer is complemented, but for odd columns the LSB of the address buffer is complemented and also the row decoder output on line 15*s* is incremented.

TABLE A

THE INSTRUCTION SET

Source Code	Object Code-Binary	No. of Cycles	No. of Words	DESCRIPTION
ADD	0000SSSSIAAAAAAA	1	1	Add word at RAM address A (shifted S places to left) to Acc; Result to Acc
SUB	0001SSSSIAAAAAAA	1	1	Subtract word at address A (shifted S places to left) from ACC; Result to Acc
LAC	0010SSSSIAAAAAAA	1	1	Load Acc with word at address A (shifted S places to left)
SAR	00110RRRIAAAAAAA	1	1	Store contents of Aux Reg number R at location defined by A
LAR	00111RRRIAAAAAAA	1	1	Load Aux Reg R with value at location A
IN	01000PPPIAAAAAAA	2	1	Input value on external data bus, store in A
OUT	01001PPPIAAAAAAA	2	1	Output value at address A to ext data bus
SACL	01010XXXIAAAAAAA	1	1	Store low order Acc bits in location A, shifted X places left
SACH	01011XXXIAAAAAAA	1	1	Store high order Acc bits in location A, shifted X places left
ADDH	01100000IAAAAAAA	1	1	Add value at address A to high order Acc bits; result to Acc; no shift
ADDS	01100001IAAAAAAA	1	1	Add Acc to value at address A sign extension suppressed
SUBH	01100101IAAAAAAA	1	1	Subtract value at address A from high order Acc bits; result to Acc; no shift
SUBS	01100AAIAAAAAAA	1	1	Subtract with sign extension suppressed
SUBC	01100100IAAAAAAA	2	1	Conditional subtract for divide; left shift ALu output and conditional +1
ZALH	01100101IAAAAAAA	1	1	Zero Accumulator and Load High under half of Acc with addressed data
ZALS	01100110IAAAAAAA	1	1	Zero Accumulator and Load with sign Extension Suppressed
TBLR	01100111IAAAAAAA	3	1	Table Read; read data from program memory using Acc as address; store in RAM
MAR	01101000IAAAAAAA	1	1	Modify Auxiliary Registers
DSHT	01101001IAAAAAAA	1	1	Data Shift; value defined by A shifted to A+1
LT	01101010IAAAAAAA	1	1	Load T Reg with value defined by A
LTD	01101011IAAAAAAA	1	1	Load T Reg with value A; shift A to A+1; Acc+Preg Acc
LTA	01101100IAAAAAAA	1	1	Load T Reg with value defined by A; Acc+Preg Acc
MPY	01101101IAAAAAAA	1	1	Multiply T times value defined by A, result to P Reg
LDPK	01101110DDDDDDDD	1	1	Load page reg for data memory with 8-bit constant D
LDP	01101111IAAAAAAA	1	1	Load DP reg with value whose address is at A
LARK	01110RRRDDDDDDDD	1	1	Load Auxiliary Register R with 8-bit constant D; MSB's Zero
EXOR	01111000IAAAAAAA	1	1	Exclusive OR Acc with value defined by A; result to LSBs of Acc; zero MSB's
AND	01111001IAAAAAAA	1	1	AND LSB's of Acc with value defined by A; result to LSB's of Acc; (zero)-(MSB's)
OR	01111010IAAAAAAA	1	1	OR LSB's of Acc with value defined by A; result to Acc; (zero)-(MSB's of Acc)
LST	01111011IAAAAAAA	1	1	Load Status with 16-bit value found at location A in RAM
SST	01111100IAAAAAAA	1	1	Store Status in location defined by 8-bit address A in RAM
TBLW	01111101IAAAAAAA	3	1	Table Write; write the value at Ram address to program memory address in Acc
LACK	01111110DDDDDDDD	1	1	Load Accumulator with 8-bit constant from instruction word
NOOP	0111111110000000	1	1	No-operation
DINT	0111111110000000	1	1	Disenable Interrupt-masks interrupt input INT
EINT	0111111110000010	1	1	Enable Interrupt-unmasks interrupt input INT
ABS	0111111110001000	1	1	Absolute Value operation; if Acc 0, Acc Acc; else Acc Acc
ZAC	0111111110001001	1	1	Clear Accumulator; zeros Acc
RAMV	0111111110001010	1	1	Reset Overflow Mode
SAMV	0111111110001011	1	1	Set Overflow Mode
CALLA	0111111100001100	2	1	Call subroutine indirect
RET	0111111110001101	2	1	Return from Subroutine
PAC	0111111110001110	1	1	Load accumulator with contents of P Reg
APAC	0111111110001111	1	1	Add accumulator to contents of P Reg; Result to Acc
SPAC	0111111110010000	1	1	Subtract contents of P reg from Accumulator; Result to Acc
MPYK	100CCCCCCCCCCCCC	1	1	Multiply by constant C
BARNZ	11110100XXXXXXXX	2	2	Branch if Loop Counter Not Zero, to location defined PC+1
BV	11110101XXXXXXXX	2	2	Branch if Overflow Bit in ST is 1
BIOZ	11110110XXXXXXXX	2	2	Branch if IO Bit in ST (from IO pin) is 1
CALL	11111000XXXXXXXX	2	2	Call Subroutine
B	11111001XXXXXXXX	2	2	Unconditional Branch to location W at PC+1
BLZ	11111010XXXXXXXX	2	2	Branch if Acc is less than zero
BLEZ	11111011XXXXXXXX	2	2	Branch if Acc is less than or equal to zero
BGZ	11111100XXXXXXXX	2	2	Branch if Acc is greater than zero
BGEZ	11111101XXXXXXXX	2	2	Branch if Acc is greater than or equal to zero
BNZ	11111110XXXXXXXX	2	2	Branch if Acc is not zero
BZ	11111111XXXXXXXX	2	2	Branch if Acc is equal to zero

TABLE B

ALU FUNCTIONS

	Control Code						Propagate Node	Generate Node	Output
	#AUM0	#AUM1	#AUM2	#AUM3	#AUM4	#AUMB			
Add	0	1	1	0	0	0	A+B	AB	$A+B+C_{in}$
Subtract	1	0	0	1	0	0	A+B	AB	$A+B+C_{in}$
Load Acc	0	1	0	1	1	0	B	X	B+1=B
Exclusive Or	1	0	0	1	1	0	A+B	X	A+B+1=A+B
Or	1	0	0	1	1	0	AB (=A+B)	X	A+B+1=A+B
And	0	1	1	1	1	0	A+AB	X	(A+AB)+1=A+B=A
Abs. Value	0	0	1	1	0	1	A	0	$A-C_{in}$

What is claimed is:

1. A microcomputer formed in a single integrated circuit comprising:

an arithmetic/logic unit having data input and data output;

a data memory having an address input and having data input/output means;

data bus means coupled to the data input and data output of the arithmetic/logic unit and coupled to the data input/output means of the data memory, the data bus means transferring multi-bit data;

a program memory having an address input and having an instruction output, the program memory storing instruction words;

program address means having an input and including incrementing means; said program address means having an output connected to said address input of the program memory means;

control means for generating controls in response to instruction words; the controls defining operation of the arithmetic/logic unit, transfer of multi-bit data to and from the data bus means, and operation of said program address means;

program bus means coupling said instruction output to an input of said control means, and to said input of said program address means, the program bus means transferring multi-bit information;

timing means for establishing repetitive operating cycles wherein during one of said operating cycles multi-bit data is transferred from the data memory to the data input of the arithmetic/logic unit via said data bus means, the program address means applies an address to the address input of the program memory, and the control means receives an instruction word from the instruction output via said program bus means;

bus interchange means within said integrated circuit and coupled to said data bus means and to said program bus means for

(a) transferring said multi-bit data from the data bus means to the program bus means and for transferring said multi-bit data from the program bus means to said input of said program address means, both during one of said operating cycles, and

(b) transferring said multibit information from said instruction output of said program memory to said program bus means and transferring said multibit information from said program bus means to said data bus means, both during one of said operating cycles,

(c) all said transferring being in response to controls received from said control means generated from a single one of said instruction words.

2. A device according to claim 1 wherein:

after transferring said multi-bit data and multi-bit information in response to said single one of said instruction words via said bus interchange means,

multi-bit information from the program bus means is valid on said data bus means during one part of said one of said operating cycles and

multi-bit data from the data bus means is valid on said program bus means during another part of a different one of said operating cycles.

3. A device according to claim 2 wherein the bus interchange means receives said multi-bit data from the data bus means only during said one part for transfer to the program bus means, and receives said multi-bit information from the program bus means during said another part for transfer to the data bus means.

4. A device according to claim 1 wherein the data output of the arithmetic/logic unit is coupled to an accumulator and an output of the accumulator is coupled to the data bus means.

5. A device according to claim 4 wherein an output of the accumulator is coupled to a data input of the arithmetic/logic unit.

6. A microcomputer formed in a single integrated circuit comprising:

an arithmetic/logic unit having data input and data output;

a data memory having an address input and having data input/output means;

data bus means coupled to the data input and data output of the arithmetic/logic unit and coupled to the data input/output means of the data memory, the data bus means transferring multi-bit data;

a program memory having an address input and having an instruction output, the program memory storing instruction words;

program address means having an input and including incrementing means; said program address having an output connected to said address input of the program memory means;

program bus means separate from the data bus means and coupled to said instruction output and to said input of said program address means, the program bus means transferring multi-bit information;

control means having an input coupled to receive instruction words from said program bus means, said control means generating sets of controls in response to the instruction words; the sets of controls defining operation of the arithmetic/logic unit, transfer of multi-bit data to and from the data bus means, transfer of multibit information to and from the program bus means, and operation of said program address means;

timing means for establishing repetitive operating cycles wherein during one of said operating cycle multi-bit data is transferred from the data memory to the data input of the arithmetic/logic unit via said data bus means, the program address means applies an address to the address input of the program memory, and the control means receives an instruction word from the instruction output via said program bus means;

bus interchange means within said integrated circuit and coupled to said data bus means and to said program bus means, the bus interchange means including:

(a) means for transferring said multi-bit data from the data bus means to the program bus means and for transferring said multi-bit information from the program bus means to said data bus means,

(b) said means for transferring and said control means operating in response to one of said instructions words to transfer multi-bit data from the data bus means via said bus interchannge means to said input of the program address means, in one of said operating cycles,

(c) said means for transferring and said control means operating in response to a given instruction word to transfer multi-bit information from said instruction output of said program memory via said bus interchange means to said data bus means, in one of said operating cycles.

7. A microcomputer according to claim 6 wherein said one instruction word is the same as said given instruction word.

8. A microcomputer according to claim 6 including address and data bus means external to said integrated circuit and coupled to said address bus means and to said data bus means, and program and data memory means external to said integrated circuit coupled to said address and data bus means.

9. A microcomputer according to claim 8 wherein said address and data bus means external to the integrated circuit include an address bus and a data bus.

* * * * *

United States Patent [19]

Sheets

[11] **Patent Number: 4,670,837**

[45] **Date of Patent: Jun. 2, 1987**

[54] **ELECTRICAL SYSTEM HAVING VARIABLE-FREQUENCY CLOCK**

[75] Inventor: **Laurence L. Sheets**, St. Charles, Ill.

[73] Assignees: **American Telephone and Telegraph Company; AT&T Bell Laboratories**, both of Murray Hill, N.J.

[21] Appl. No.: **624,469**

[22] Filed: **Jun. 25, 1984**

[51] **Int. Cl.**[4] **H03K 5/04**

[52] **U.S. Cl.** **364/200**; 328/38.1

[58] **Field of Search** 364/200, 900; 328/62, 328/38; 365/222

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,453,601	7/1969	Bogert et al.	364/200
3,656,123	4/1972	Carnevale et al.	340/172.5
3,775,696	11/1973	Garth	331/57
3,922,526	11/1975	Cochran	235/152
4,037,090	7/1977	Raymond, Jr.	364/200
4,191,998	3/1980	Carmody	364/200
4,241,418	12/1980	Stanley	364/900
4,331,924	5/1982	Elliot et al.	328/38
4,414,637	11/1983	Stanley	364/569
4,438,490	3/1984	Wilder, Jr.	364/200
4,447,870	5/1984	Tague et al.	364/200
4,463,440	7/1984	Nishiura et al.	364/900

FOREIGN PATENT DOCUMENTS

0098653	6/1983	European Pat. Off. .
2248170	4/1974	Fed. Rep. of Germany .

Primary Examiner—Gareth D. Shaw
Assistant Examiner—Randy W. Lacasse
Attorney, Agent, or Firm—Ross T. Watland

[57] **ABSTRACT**

The microprocessor unit of a system implemented using metal-oxide-silicon (MOS) technology, is driven by a variable-frequency clock. The microprocessor controls the clock frequency based on the present rate of required microprocessor activity. By driving the microprocessor unit at a lower clock frequency when such activity rate is low, the energy dissipated by the microprocessor unit is reduced due to the MOS power-frequency characteristic.

7 Claims, 6 Drawing Figures

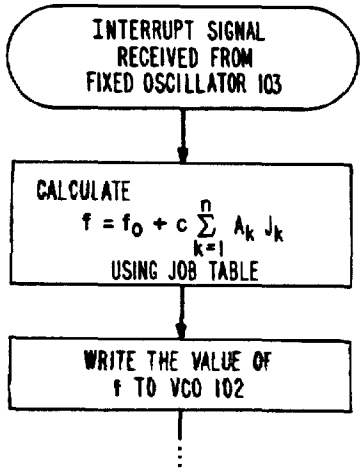


FIG. 1

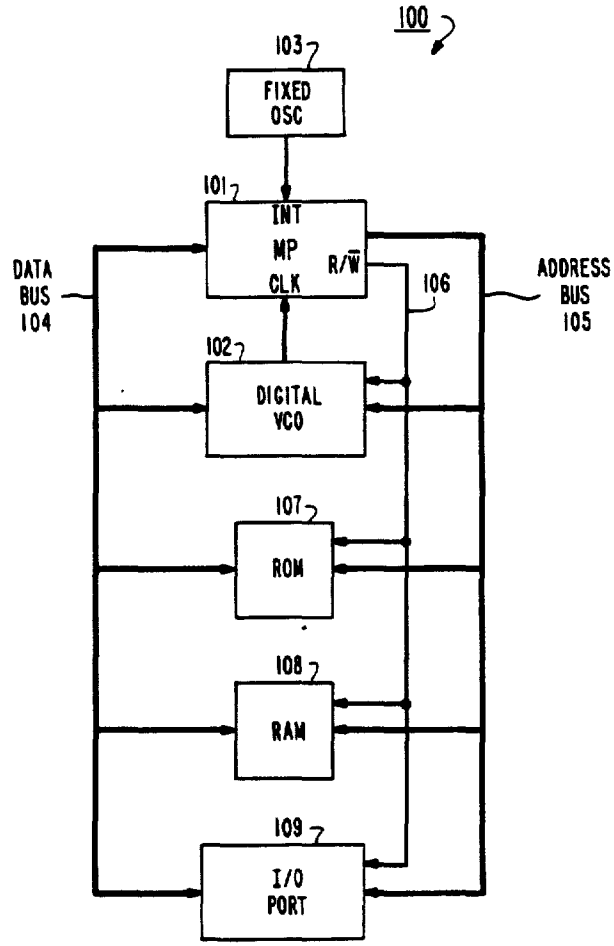

100
103
FIXED OSC
101
INT
MP
CLK
R/W
106
DATA BUS 104
ADDRESS BUS 105
102
DIGITAL VCO
107
ROM
108
RAM
109
I/O PORT

FIG. 2

JOB TABLE

JOB TYPE	NO. OF JOBS TO BE DONE
1	J_1
2	J_2
.	.
.	.
.	.
.	.
.	.
.	.
.	.
n	J_n

FIG. 3

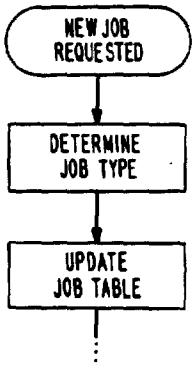


FIG. 4

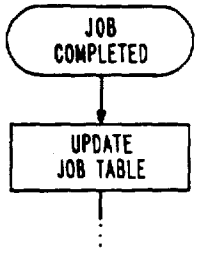
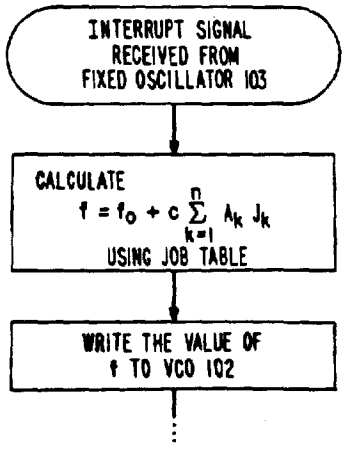


FIG. 5



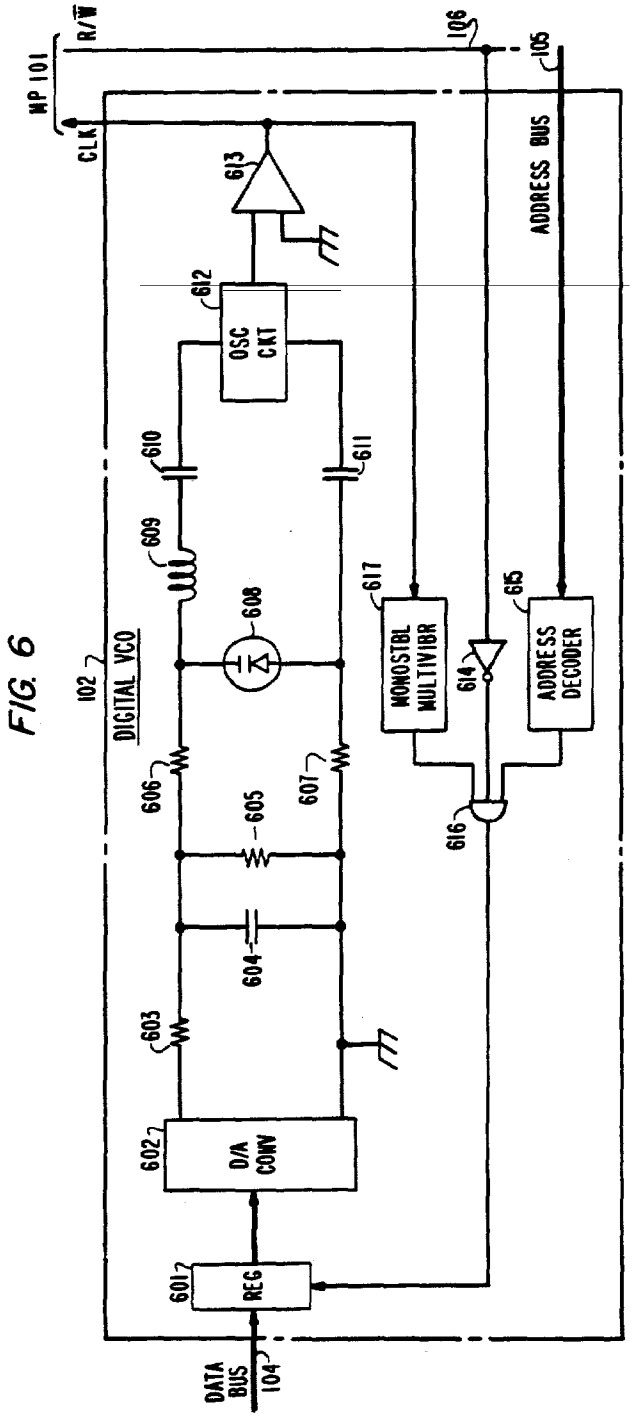

R/W
106
105
MP 101
CLK
ADDRESS BUS
613
612
OSC CKT
610
611
609
608
617
615
MONOSTBL MULTIVIBR
ADDRESS DECODER
614
102
DIGITAL VCO
606
607
605
616
604
603
602
D/A CONV
601
REG
DATA BUS
104

FIG. 6

ELECTRICAL SYSTEM HAVING VARIABLE-FREQUENCY CLOCK

TECHNICAL FIELD

This invention relates to clocked, electrical systems, and, more particularly, to microprocessor-based systems implemented using metal-oxide-silicon (MOS) technology.

BACKGROUND OF THE INVENTION

One very important aspect of the continuing evolution of silicon technology is the proliferation of microprocessors throughout our society. Because of the significant reductions in their size and cost, such processors can be economically used in many applications where the use of computers could not otherwise be justified. Even in applications where larger computers, e.g., minicomputers, have traditionally been used, the advantages of distributed processing have been obtained by using a number of microprocessors to perform the functions previously performed by a single larger processor. For example, many of the control functions previously performed by the central control unit in stored program controlled switching systems are being performed in more modern systems by a number of microprocessors which are distributed toward the system periphery and which communicate with each other to control system operation.

One countervailing factor to weigh against the established advantages of distributed processing is the large amount of power typically required to keep such distributed control processors continuously energized. This factor will become even more important as the cost of energy continues to increase. The power dissipation of microprocessors also becomes important when they are used in portable, battery-powered personal computers. In these applications and others, the ma9nitude of power required to operate microprocessor-based systems is a problem which diminishes the otherwise overall attractiveness of such systems.

SUMMARY OF THE INVENTION

The aforementioned problem is advantageously solved and a technical advance is achieved in accordance with the principles of the invention in both an electrical system driven by a variable-frequency clock and an associated system operation method which reduce the magnitude of energy required by the electrical system by determining the processing load presented to the system and then reducing the clock frequency at which the system is driven, during times when the processing load is reduced. The amount of the saving is dependent on the power-frequency characteristic associated with the particular technology with which the electrical system is implemented.

BRIEF DESCRIPTION OF THE DRAWING

A more complete understanding of the present invention may be obtained from a consideration of the following description when read in conjunction with the drawing in which:

FIG. **1** is a block diagram of a microprocessor-based system illustrating the principles of the present invention;

FIGS. **2** through **5** are diagrams illustrating a method of monitoring the processing load and computing the required clock frequency to reduce the magnitude of energy required by the system of FIG. **1**; and

FIG. **6** is a circuit diagram of a digital, voltage-controlled oscillator included in the system of FIG. **1**.

DETAILED DESCRIPTION

FIG. **1** is a block diagram of an exemplary microprocessor-based system **100** illustrating the principles of the present invention. The system is controlled by a microprocessor **101** which communicates with associated devices via a data bus **104** and an address bus **105**. For example, microprocessor **101** reads information from a read only memory (ROM) **107** via data bus **104** by transmitting a logic one signal from a control terminal R/$\overline{W}$ via a conductor **106** and transmitting on address bus **105**, an address defining both ROM **107** and the particular location of ROM **107** to be read. ROM **107** is typically used to store information such as programs to be executed by microprocessor **101** or fixed data. Microprocessor **101** reads information in like manner from a random access memory (RAM) **108**, used to store variable data, or from an input/output (I/O) port **109**, used to interface with various external devices (not shown), e.g., devices being operated under the control of microprocessor **101**. In addition, microprocessor **101** also writes information via data bus **104** to RAM **108** or I/O port **109** by transmitting a logic zero signal from control terminal R/$\overline{W}$ on conductor **106** and transmitting the appropriate address on address bus **105**.

The portion of system **100** described thus far is well known. Various other control or status signals are typically conveyed between microprocessor **101** and its associated devices to achieve correct system operation. However, since such signals are not relevant to the present invention and tend to vary depending upon the particular family of devices used in a given implementation, they are not further described herein. Microprocessor **101** and its associated devices are energized by means of a DC power source (not shown), e.g., a battery or, alternatively, a DC power supply driven from a commercial AC source. The present invention is directed to reducing the amount of energy drawn by system **100** from such a DC source. In addition to energy savings, an enhancement of long-term system reliability is also obtained.

Microprocessor-based systems such as system **100** are typically implemented using metal-oxide-silicon (MOS) technology. The magnitude of power consumed by a MOS device at a given voltage is substantially directly proportional to the frequency at which the device is operated. In the case of microprocessor **101**, which is a relatively complex MOS device, the duration of each execution cycle is defined by the signal received at a CLK terminal. In accordance with the present exemplary embodiment of the invention, a digital, voltage-controlled oscillator (VCO) **102** transmits the cycle-defining clock signal. Upon determining the amount of processing required at any given time, microprocessor **101** computes an operating frequency that is sufficient to meet the offered processing load. Microprocessor **101**, which communicates with VCO **102** via data bus **104**, address bus **105** and conductor **106** in the same manner as with RAM **108** or I/O port **109**, writes a digital word defined by the computed frequency via data bus **104** to VCO **102**. VCO **102** gradually adjusts the frequency of the clock signal transmitted to microprocessor **101** to the computed frequency in response to the digital word. Reducing the clock frequency reduces

the power consumed by microprocessor **101** and, by reducing the required access rate to the associated devices, i.e., ROM **107**, RAM **108**, and I/O port **109**, also reduces the power consumed by those devices. The power reduction is substantially directly proportional to the reduction of the clock frequency. For example, a frequency reduction from 20 megahertz to 10 megahertz will result in a saving of approximately 50%.

In system **100**, the timing of real-time events is controlled by microprocessor **101** in response to interrupt signals received at an INT terminal from a fixed-frequency oscillator **103**. For example, microprocessor **101** repeats the process of computing the required frequency based on the processing load and writing a digital word to digital VCO **102** at regular intervals as defined by the interrupt signals from fixed oscillator **103**.

In the present embodiment, microprocessor **101** determines its processing load to control the VCO **102** clock frequency at any given time by using a linear regression. All possible processing jobs expected for microprocessor **101** in a particular application, are categorized according to complexity, i.e., the number of execution cycles required for completion, into n job types, where n is a positive integer greater than one. Associated with each job type is a predetermined weighting factor A_k which defines the complexity of that job type with respect to other job types. Microprocessor **101** maintains a job table (FIG. **2**) in RAM **108**. The job table lists for each job type the number, J_k, of jobs of that type presently required. As shown in FIG. **3**, when each processing job is requested, the associated job type is determined and the job table is updated by incrementing J_k by one. Jobs may be requested in a number of ways. For example, certain jobs may be required at regular intervals as defined by the interrupt signals from fixed oscillator **103**. Other jobs may be requested in response to information received from external devices and read via I/O port **109**. After each processing job is completed, the job table is updated by decrementing J_k by one for the associated job type (FIG. **4**). Thus the job table in RAM **108** is kept current at all times. As shown in FIG. **5**, each time that microprocessor **101** receives an interrupt signal from fixed oscillator **103**, microprocessor **101** reads each of the J_k values in the job table and computes the required clock frequency, f, according to

$$f = f_0 + c \sum_{k=1}^{n} A_k J_k,$$

where f_o is the lowest desired frequency and c is an appropriate scale factor. (Alternatively, the A_k weighting factors could be properly scaled to eliminate the need for the scale factor c.) A digital word defined by the computed value of f is then written to VCO **102**.

In the present embodiment, di9ital VCO **102** is implemented as an LC oscillator (FIG. **6**). When microprocessor **101** computes a new clock frequency, it transmits a digital word defined by that frequency via data bus **104** to a register **601**. Microprocessor **101** also transmits an address on address bus **105** to an address decoder **615**. Address decoder **615** responds to the particular address defining VCO **102** by transmitting a logic one signal to an AND gate **616**. Microprocessor **101** transmits a logic zero signal on conductor **106** from its $R/\overline{W}$ terminal to an inverter **614**, which in turn transmits a logic one signal to AND gate **616**. When a monostable multivibrator **617** transmits a logic one signal to a third input terminal of AND gate **616**, AND gate **616** responds by transmitting a logic one signal to register **601** which then stores the digital word from data bus **104**. A D/A converter **602** generates an analog control voltage in response to the digital word in register **601**. The analog control voltage is filtered by a low-pass filter comprised of resistors **603** and **605** and a capacitor **604**, the values of which determine a filter time constant such that the control voltage transmitted varies slowly with respect to the minimum required clock frequency. The resistor **605** is connected across capacitor **604** as a discharging means. The control voltage is then applied via a pair of decoupling resistors **606** and **607** to a varicap diode **608**, having a capacitance that varies from 25 to 100 picofarads with applied voltage. The combination of the variable capacitance of the varicap diode **608** and the inductance of an inductor **609**, e.g., 2.5 microhenries, is coupled via a pair of coupling capacitors **610** and **611** to an oscillator circuit **612**. Oscillator circuit **612**, which is implemented in the present embodiment as an amplifier circuit, transmits a sinusoidal signal at the frequency determined by the combination of varicap diode **608** and inductor **609**. The sinusoidal signal transmitted by circuit **612** is applied to one input terminal of comparator **613**, which has its other input terminal 9rounded. Accordingly, comparator **613** transmits a square wave at the determined frequency. The square wave is transmitted to both the CLK terminal of microprocessor **101** to define its execution cycle and to monostable multivibrator **617** which responds by transmitting a logic one signal to AND gate **616** as described above. Monostable multivibrator **617** transmits a pulse of predetermined duration on the leading edge of the square wave generated by comparator **613** and is included to assure that each data word on data bus **104** is stable before AND gate transmits a logic one signal to store that data word in register **601**.

In this embodiment, the relationship between the clock frequency computed by microprocessor **101** and the digital word transmitted to VCO **102** is predetermined based on the characteristic of VCO **102**. Accordingly, when microprocessor **101** computes a given clock frequency, it transmits a digital word to VCO **102** according to the predetermined relationship such that VCO **102** generates the given clock frequency in response to that digital word.

It is to be understood that the above-described embodiment is merely illustrative of the principles of the present invention and that other embodiments may be devised by those skilled in the art without departing from the spirit and scope of the invention. For example, the LC oscillator implementation of digital VCO **102** may be replaced by a switched RC oscillator where resistors of differing resistance are switched in and out of the circuit to vary the frequency in response to the digital words received by the D/A converter. Rather than computing the frequency based on the processing backlog, the activity on data bus **104** and address bus **105** could be monitored and then used as a basis for determining the required frequency. Instead of using a continuously variable-frequency clock, selections can be made from a small number of discrete frequencies. For example, in a battery-powered personal computer with an operating system which includes a sleep state, the microprocessor CPU could be operated at a low frequency sufficient to keep any dynamic logic re-

freshed, e.g., 500 kilohertz, when the operating system is in the sleep state, and the frequency could then be increased to a nominal operating frequency, e.g., 10 megahertz, when wakeup occurs. In some applications, the desired clock frequency could be determined based on historical activity records rather than in real time. For example, the operating frequency of the distributed microprocessors used for control in a telephone switching system could be adjusted based on calling patterns observed during different times of the day or during different days of the week as a way of reducing the energy requirements of the system. It is to be recognized that any of a number of microprocessor families can be advantageously used in such systems. One specific example is the Motorola 68000 microprocessor and its associated devices. Furthermore, the invention is applicable to clocked, electrical systems other than microprocessor-based systems where power consumption is a function of clock frequency as, for example, in gate arrays.

What is claimed is:

1. In an electrical system driven by a variable-frequency clock to perform processing jobs, a method of operating said system under control of a processor to increase efficiency in power consumption comprising:

determining the processing load of said system based on all requested but uncompleted processing jobs and

adjusting the frequency of said clock basewd on the determined processing load, where each of said processing jobs is one of n types, n being a positive integer greater than one, said method further comprising

maintaining data that define a number, J_K, of jobs of type K for each integer K from one through n, to be performed by said system,

wherein said determining step further comprises reading said data and

wherein said adjusting step further comprises adjusting the frequency, f, of said clock according to

$$f = f_0 + C \sum_{K=1} A_K J_K,$$

wehrein f0 is a minimum frequency, A_K is a weighting factor associated with jobs of type K, and C is a predetermined scale factor.

2. A method in accordance with claim 1 further comprising

repeating at regular intevals said determining step and said adjusting step.

3. A method in accordance with claim 1 wherein said maintianing step further comprises

incrementing said number, J_k, by one as each job of type k is requested and

decremeting said number, J_k, by one as each job of type k is completed.

4. An electrical system comprising:

variable-frequency clock means for transmitting a clock signal of variable frequency,

electrical means for performing processing jobs at an operating frequency defined by the frequency of said clock signal, said electrical means comprising a processor

means for repetitively determining the processing load of said electrical means based on all requested but uncompleted processing jobs and

means coupled to said variable-frequency clock means for adjusting the frequency of said clock signal basedon the processing load determined by said determining means, wherein

each of said processing jobs is one of n types, n being a positive integer greater than one, said system further comprises

means for maintaining data that define a number, J_K, of jobs of type K, for each integer K from one through n, to be performed by said system,

wherein said determining means further comprises means for reading said data

wherein said adjusting means further comprises means for calculating an operating frequency, f, according to

$$f = f_0 + C \sum_{K=1} A_K J_K,$$

wherein f_0 is a minimum frequency, A_K is a weighting factor associated with jobs of type K, and C is a predetermined scale factor and

means for transmitting a digital word defined by said calculated operating frequency, f, to said variable-frequency clock means,

wherein said variable-frequency clock means is responsive to said digital word for generating said clock signal at said calculating operating frequency, f.

5. An electrical system in accordance with claim 4 wherein said variable-frequency clock means further comprises

converter means for generating an analog control voltage in response to said digital word and

oscillator means coupled to said converter means for generating said clock signal at a frequncy defined by said analog control voltage.

6. An electrical system in accordance with claim 5 further comprising

low-pass filter means interposed between said converter means and said oscillato means for filtering said analog control voltage.

7. An electrical system in accordance with claim 4 wherein said electrical means is implemented in metal-oxide-silicon technology.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 4,670,837

DATED : June 2, 1987

INVENTOR(S) : Laurence L. Sheets

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

IN THE CLAIMS

Column 5, line 30, "basewd" should be "based",
Column 5, line 47, "wehrein" should be "where",
Column 5, line 52, "intevals" should be "intervals",
Column 5, line 56, "maintianing" should be "maintaining";
Column 6, line 1, "decremeting" should be "decrementing",
Column 6, line 15, "basedon" should be "based on",
Column 6, line 48, "frequncy" should be "frequency",
Column 6, line 53, "oscillato" should be "oscillator".

Signed and Sealed this

Seventeenth Day of July, 1990

Attest:

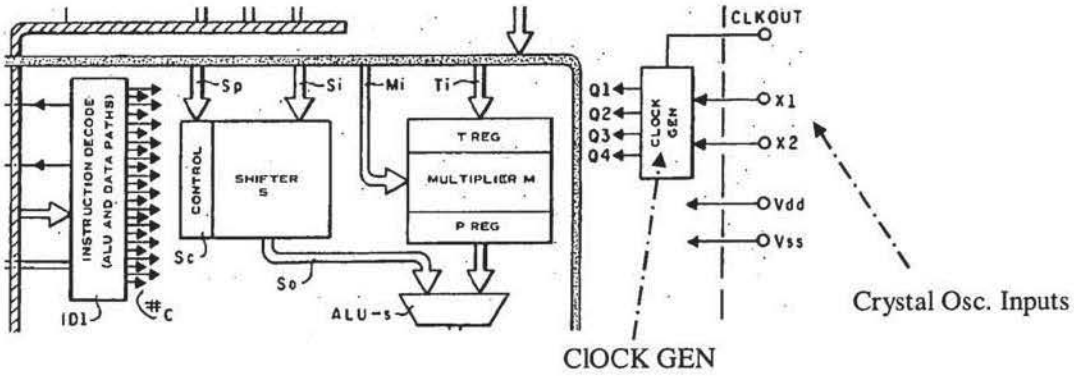
Attesting Officer

HARRY F. MANBECK, JR.

Commissioner of Patents and Trademarks

> Crucial to the present invention is that since both the oscillator or variable speed clock and driven device are on the same substrate, when the fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together. This differs from all cited references in that the oscillator or variable speed clock and the driven device are on the same substrate.... [Exhibit 10, p. 5] (emphasis added).

The Office was not able to rebut such statements during original prosecution, which were true only in the limited vacuum of the "cited prior art". The reference before the Examiner that most closely approximated the "on-chip ring oscillator" or "variable speed system clock" was the Magar patent, (U.S. Pat. No. 4,503,500, Exhibit 11). The Magar patent described an off-chip crystal oscillator, with on-chip clock generation circuitry. The pertinent portions of Fig. 2A from the Magar patent are shown below, with dashed arrows added by the Requester to indicate particular features:



Magar shows "CLOCK GEN" circuitry on the right-hand side of Fig. 2A that is on a single substrate with the CPU. The CLOCK GEN circuitry, however, has crystal oscillator inputs X1 and X2. This leads to the supposition that CLOCK GEN is not a resonator itself, but rather circuitry that amplifies, filters or otherwise prepares the crystal resonator output for use as

a CPU clock. Since the crystal resonator of Magar was off-chip, the Applicants were able to assert:

> one of ordinary skill in the art should readily recognize the speed of the CPU and the clock *do not* vary together due to manufacturing variation, operating voltage and temperature of the IC in the Magar microprocessor, as taught in the above quotation from the reference. This is simply because the Magar microprocessor clock is frequency-controlled by a crystal which is also external to the microprocessor. Crystals are by design fixed-frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The Magar microprocessor in no way contemplates the variable speed clock as claimed. (emphasis in original) [Amendment of July 3, 1997, Exhibit 10, p. 3-4]

If the Office had had access to the best prior art, it could have quickly met this argument with a better rejection. In fact, by 1980, the use of on-chip ring oscillators to clock integrated circuits was *undergraduate textbook knowledge*, appearing in Mead & Conway (Exhibit 18). In Chapter 7, the Mead & Conway textbook discusses integrated circuit clocks, stating that they are most easily constructed using on-chip ring oscillators, and that the frequency of the ring oscillators will vary with ambient conditions and process technology:

> Process variation in integrated circuit fabrication does not allow accurate resonant networks to be fabricated by usual means, but it is perfectly feasible, indeed essential for self-contained VLSI systems, to generate clock signals on the chip….[T]he role of the clock in a synchronous system is to connect sequence and time….A *model* of the temporal behavior of the systems being clocked is built into the clock generator or in the choice of times for the various timers. The easiest way to build these timers is as chains of inverters. The propagation delay time of such a chain will of course vary with τ, according to the way in which the fabrication process, aging, temperature and power voltage affect τ. However, these variations only make the inverter chain a better model of the system being clocked than a fixed timer would be….Clocks that employ these delays as timers are all elaborations

COOLEY LLP
HEIDI L. KEEFE (178960) (hkeefe@cooley.com)
MARK R. WEINSTEIN (193043) (mweinstein@cooley.com)
KYLE D. CHEN (239501) (kyle.chen@cooley.com)
Five Palo Alto Square, 4th Floor
3000 El Camino Real
Palo Alto, California 94306-2155
Telephone: (650) 843-5000
Facsimile: (650) 857-0663

Attorneys for Plaintiffs
HTC CORPORATION and
HTC AMERICA, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION and HTC AMERICA, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED,

Defendants.

Case No. 5:08-cv-00882 PSG

[Related to Case No. 5:08-cv-00877 PSG]

PLAINTIFFS' NOTICE OF MOTION AND MOTION FOR PARTIAL SUMMARY JUDGMENT OF (1) NON-INFRINGEMENT OF U.S. PATENT NOS. 5,530,890 AND 5,809,336; AND (2) NO WILLFUL INFRINGEMENT OF U.S. PATENT NO. 5,530,890

Date: August 13, 2013
Time: 10:00 a.m.
Place: Courtroom 5, 4th Floor
Judge: Hon. Paul S. Grewal

Complaint Filed: February 8, 2008
Trial Date: September 23, 2013

NOTICE OF MOTION AND MOTION

PLEASE TAKE NOTICE that Plaintiffs HTC Corporation and HTC America, Inc. (collectively "Plaintiffs" or "HTC") move, pursuant to Federal Rule of Civil Procedure 56, for partial summary judgment (1) of non-infringement for any alleged infringement of U.S. Patent Nos. 5,530,890 (the "'890 patent") occurring prior to March 1, 2011; (2) of non-infringement for any alleged infringement of U.S. Patent No. 5,809,336 (the "'336 patent") occurring prior to December 15, 2009; and (3) of no willful infringement of the '890 patent.

This Motion is filed pursuant to the briefing schedule established by the Court's order of July 3, 2013, as amended on July 12, 2013. (Doc. Nos. 452, 456.) This Motion is based on the Memorandum of Points and Authorities set forth below, the accompanying declaration of Mark R. Weinstein ("Weinstein Decl.") submitted herewith, and such other matters as may be presented at the hearing on HTC's motion and allowed by the Court.

MEMORANDUM OF POINTS AND AUTHORITIES

I. INTRODUCTION

The '890 and '336 patents-in-suit were involved in *ex parte* reexaminations that resulted in the addition of new claims and the cancellation of or narrowing amendments to each independent claim. Under the doctrine of absolute intervening rights in 35 U.S.C. § 307(b), Defendants Technology Properties Ltd., Patriot Scientific Corp., and Alliacense Ltd. (collectively "TPL") cannot recover damages for alleged infringement of a patent that was narrowed in reexamination prior to the issuance of the reexamination certificate. In this case, a substantial portion of the damages TPL seeks from HTC under the '890 patent and the '336 patent is based on sales of accused HTC products that took place prior to issuance dates of these reexamination certificates. HTC is therefore entitled to judgment as a matter of law that TPL cannot recover damages with respect to the '890 or '336 patent prior to those dates.

HTC also seeks summary judgment against HTC's claim of willful infringement under the '890 patent.[1] As shown below, TPL has presented no evidence to satisfy either the subjective or

[1] This motion addresses TPL's willful infringement contentions as to the '890 patent and not the

the objective prong of the willful infringement standard under *Seagate*, and as such, summary judgment is appropriate.

II. ARGUMENT

A. HTC Is Entitled to Partial Summary Judgment of Non-Infringement Under the Absolute Intervening Rights Doctrine

Under 35 U.S.C. § 307(b), a patent owner may not recover, prior to the issuance of the reexamination certificate, for any alleged infringement of a patent whose scope was substantively changed in reexamination. "Unless a claim granted or confirmed upon reexamination is ***identical to an original claim***, the patent can not be enforced against infringing activity that occurred before issuance of the reexamination certificate." *Bloom Engineering Co., Inc. v. North American Mfg. Co., Inc.*, 129 F.3d 1247, 1250 (Fed. Cir. 1997) (emphasis added). "'Identical' does not mean verbatim, but means at most without substantive change." *Id.* Because all asserted claims of the '890 patent and the '336 patent underwent "substantive change" during reexamination, TPL cannot recover damages prior to the issuance of the reexamination certificate for each patent.

1. No Recovery Under the '890 Patent Prior to March 1, 2011

The '890 patent issued on June 25, 1996 with 10 originally-issued claims, with claim 1 being the sole independent claim. (Weinstein Decl. Ex. 1.) On January 19, 2009, an *ex parte* reexamination request was filed against the '890 patent. More than two years later, on March 1, 2011, the Patent Office issued an *ex parte* reexamination certificate canceling claims 1-4 and adding new claims 11-20. (Weinstein Decl. Ex. 2.) In the present case, TPL is only asserting claims 11, 12, 13, 17 and 19 of the '890 against HTC – all of which were added during the reexamination and are substantively different from the original claims.

In particular, TPL added claim 11 during the reexamination by copying the language from claim 1 but adding a critical new limitation to overcome the prior art. Claim 11 as issued from the

---

'336 patent. This is because HTC is filing, concurrently herewith, a separate motion for summary judgment of full non-infringement as to the '336 patent. That motion also alternatively argues that TPL has no evidence of willful infringement as to the '336 patent. As such, alleged willful infringement as to the '336 patent is not discussed in this motion.

reexamination reads (with the new limitation shown in bold underlining):

> 11. (New) A microprocessor, which comprises a main central processing unit and a separate direct memory access central processing unit in a single integrated circuit comprising said microprocessor, said main central processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus, said internal data bus being bidirectionally connected to a loop counter, said loop counter being connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register, **said stack pointer pointing into said first push down stack**, said internal data bus being connected to a memory controller, to a Y register of a return push down stack, an X register and a program counter, said Y register, X register and program counter providing outputs to an internal address bus, said internal address bus providing inputs to said memory controller and to an incrementer, said incrementer being connected to said internal data bus, said direct memory access central processing unit providing inputs to said memory controller, said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory.

(Weinstein Decl. Ex. 2 (Reexamination Certificate), Claim 11.)

As shown above, TPL added the limitation, "**said stack pointer pointing to said first push down stack**," to claim 11. Neither claim 1, nor any other originally-issued claim of the '890 patent, recited that limitation. The reexamination file history confirms that this limitation was not only substantively narrowing, but critical to overcoming the prior art.

The addition of claim 11 came in response to a Final Rejection in which the Examiner rejected claim 1 (and other claims) based on a number of prior art references. TPL responded by adding new claims 11-20 and making various arguments about its original claims. In adding the new claims, TPL explained:

> Claims 11-20 are new. Claim 11 is independent. Claims 12-20 depend from claim 11. The new claims are substantially similar to claims 1-10 except that Claim 11 includes language that Examiner Pokrzywa has indicated overcomes all of the current language. In particular, Claim 11 recites (in part) "said stack pointer pointing into said first push down stack," clarifying the association of the stack pointer and the first push down stack.

(Weinstein Decl., Ex. 3, (06/29/2010 Applicant Response and Amendents), at 20.)

The Examiner subsequently relied on this additional language, "said stack pointer pointing

to said push down stack," to draw clear distinctions between original claim 1 and new claim 11. He issued an Advisory Action on August 12, 2010 maintaining the rejection of claim 1 but indicating that claim 11 would be confirmed. (*See* Weinstein Decl. Ex. 4 (08/12/2010 Advisory Action).) He observed that unlike newly-added claim 11, "the current language of claim 1 does not require that a stack pointer **points to the push-down stack** … Thus, there is no function claimed for the 'stack pointer', only that a stack pointer is bidirectionally connected to an internal bus." (*Id.* at 5 (bold in original).)

The Examiner subsequently conducted a telephone interview with TPL's representative in which TPL authorized an examiner's amendment cancelling claim 1. (*See* Weinstein Decl. Ex. 5 (11/03/2010 Notice of Intent to Issue Reexamination Certificate), at 2.) In that same amendment, the Examiner found claim 11 patentable over the prior art, stressing the importance of the new claim limitation:

> The closest prior art of record, being the May '948 reference does teach of using a push down stack. However, the May '948 reference does not expressly describe a stack pointer that points "into said first push down stack". With this feature, which was added in the Patent Owner's amendment dated 6/29/2010, claim 11 is deemed patentable.

(*Id.* at 8.) This reexamination record leaves no doubt that the limitation added during the reexamination, "said stack pointer pointing to said push down stack," substantively changed the scope of the claims. The Reexamination Certificate for the '890 patent issued on March 1, 2011, and as such, TPL cannot recover damages for any alleged infringement prior to that date.

As noted previously, the only claims asserted by TPL in this litigation are claim 11 and four additional claims that depend from claim 11 (*i.e.* claims 12, 13, 17 and 19). Because claim 11 was a substantively narrower replacement to independent claim 1, and all other asserted claims depend from claim 11, all claims asserted against HTC are subject to absolute intervening rights under 35 U.S.C. § 307(b). TPL therefore cannot as a matter of law recover damages for any alleged infringement of the '890 patent occurring prior to March 1, 2011.

2. No Recovery Under the '336 Patent Prior to December 15, 2009

The reexamination story with respect to the '336 patent is similar to that of the '890 patent

discussed above. (Weinstein Decl. Ex. 6.) The '336 patent issued September 15, 1998 with 10 originally-issued claims, with claims 1, 3, 6, and 10 being independent claims. Between October 2006 and January 2007, a series of *ex parte* reexamination requests were filed against the '336 patent. More than three years later, on December 15, 2009, the Patent Office issued an *ex parte* reexamination certificate. (Weinstein Decl. Ex. 7.) With respect to the independent claims, the certificate reflected the cancellation of independent claim 3, amendments to independent claims 1, 6, and 10, and the addition of new independent claims 11, 13 and 16. (*Id.*) In the present case, TPL is asserting independent claims 1, 6, 10, 11, 13 and 16 of the '336 against HTC – all of which were either substantially narrowed or newly-added during the reexamination. As explained below, all of these claims reflect significant substantive changes in scope such that TPL cannot recover damages for any alleged infringement occurring prior to December 15, 2009.

In particular, with respect to original independent claims 1, 6 and 10, TPL amended them to add new limitations relating to the origin of the clock signal for the second or external clock. The amendments to these three claims are reflected in bold underline below:

> 1. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, **wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock**.
>
> 6. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices; an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the

clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and an **off-chip** external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and **wherein a clock signal from said off-chip external clock originates from a source other than said oscillator**.

10. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of: providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency; providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors; clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate; connecting an on-chip input/output interface between said central processing unit and an **off-chip** external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and clocking said input/output interface using an **off-chip** external clock wherein said **off-chip** external clock is operative at a frequency independent of a clock frequency of said variable speed clock **and wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock**.

(Weinstein Decl. Ex. 7 ('336 Reexamination Certificate), Claims 1, 6, 10.)

As shown above, the reexamination narrowed claim 1 by adding "wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock," and added similar limitations to claims 6 and 10. These limitations were not recited in any original claim of the '336 patent. Claims 6 and 10, as shown above, reflected further amendments requiring that certain recited components be "off-chip."

These amendments narrowed the scope of the claims and were the sole basis in the Examiner's stated reasons for allowing these claims over the prior art. In his reasons for

allowability, the Examiner expressly relied on these new features. With respect to independent claim 1 as amended, for example, the Examiner wrote:

> Claim 1: Entry of the examiner's amendment produces claim 1, which recites:
>
> *"a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock."*
>
> None of the references to Kato Ledzius et al, Ikeda et al and McDermott et al incorporate these recited features, either alone or in combination. Additionally, these features are not present in the remaining prior art of record. Accordingly, claim 1 is determined to be allowable.

(Weinstein Decl. Ex. 8 (Notice of Intent to Issue Reexamination Certificate), at 9.) The Examiner made substantially the same finding with respect to independent claims 6 and 10, in both cases relying exclusively on the new limitations added during the reexamination. (*Id.* at 9-10.)

As to new independent claims 11, 13, and 16, they were based on originally-issued claims 1, 6, and 10, respectively, but included new "wherein" limitations to the end of each claim. Claim 11, for example, was based on the language of claim 1 but added a limitation at the end, "**wherein said central processing unit operates asynchronously to said input/output interface**." (*Id.* at 10.) Similar language was incorporated into claims 13 and 16. (*Id.* at 11-12.)

As with the amendments to claims 1, 6, and 10 discussed above, the Examiner expressly relied on the "wherein" limitations in new claims 11, 13 and 16 in allowing those claims. With respect to independent claim 11, for example, the Examiner wrote:

> Claim 11: Entry of the examiner's amendment produces claim 11, which recites:
>
> *"a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein said central processing unit operates asynchronously to said input/output interface."*
>
> None of the references to Kato Ledzius et al, Ikeda et al and McDermott et al incorporate these recited features, either alone or in combination. Additionally, these features are not present in the remaining prior art of record. Accordingly, claim 11 is determined to be allowable.

(*Id.* at 10.) The Examiner made substantially the same finding with respect to independent claims 13 and 16, in both cases relying exclusively on the new limitations. (*Id.* at 11-12.)

As with the '890 patent discussed above, the '336 reexamination record leaves no doubt that limitations were added during the reexamination substantively changing the scope of each asserted independent claim, in order to overcome prior art. The Reexamination Certificate for the '336 patent issued on December 15, 2009, and as such, TPL cannot recover damages for any alleged infringement prior to that date. *See* 35 U.S.C. § 307(b).

B. HTC Is Entitled to Partial Summary Judgment of No Willful Infringement of the '890 Patent

The Court should dispose of TPL's willful infringement claim on summary judgment because TPL has presented no evidence to support this claim. The Federal Circuit has held that a showing of willful infringement requires that the plaintiff establish by clear and convincing evidence (1) that the accused infringer "acted despite an objectively high likelihood that its actions constituted infringement of a valid patent," and (2) that this objectively defined risk "was either known or so obvious that it should have been known to the accused infringer." *In re Seagate Tech., LLC*, 497 F.3d 1360, 1371 (Fed. Cir. 2007) (*en banc*).

TPL cannot establish either prong because it has come forward with no evidence whatsoever of willful infringement. HTC propounded an interrogatory specifically asking TPL to identify its evidence and the complete factual basis for its allegation of willful infringement against HTC. (*See* Weinstein Decl. Ex. 9 (TPL's Response to HTC Interrogatory No. 9) at 22.) TPL's response included a parade of groundless objections but provided no substantive response. (*Id.*) TPL never supplemented its response to this interrogatory, and fact discovery closed long ago.

Moreover, the evidence affirmatively establishes that TPL could not establish willful infringement even if it had responded to HTC's interrogatory. Under the objective prong of the willful infringement analysis, "a patentee must show by clear and convincing evidence that the infringer acted despite an objectively high likelihood that its actions constituted infringement of a valid patent." *In re Seagate Tech., LLC*, 497 F.3d at 1371. "The state of mind of the accused infringer is not relevant to this objective inquiry." *Id.* This objective determination entails an

assessment of the reasonableness of the accused infringer's defenses, such as its defenses to infringement. *See Bard Peripheral Vascular, Inc. v. W.L. Gore & Assocs., Inc.*, 682 F.3d 1003, 1006 (Fed. Cir. 2012). The Federal Circuit has made clear that this objective prong presents a legal question suitable for summary judgment. "When a defense or noninfringement theory asserted by an infringer is purely legal (*e.g.*, claim construction), the objective recklessness of such a theory is a purely legal question to be determined by the judge." *Id.* at 1007. Even in those instances when the objective prong turns on factual issues, "the judge remains the final arbiter of whether the defense was reasonable, even when the underlying fact question is sent to a jury." *Id.*

The reexamination of the '890 patent, detailed above, underscores HTC's reasonable reliance on its invalidity defense. The Patent Office granted a request to reexamine the '890 patent only upon a finding that the prior art cited in the request demonstrated "a substantial new question of patentability." 35 U.S.C. § 303(a). The Patent Office not only found a substantial new question of patentability, but as explained above, the Examiner repeatedly rejected the claims and allowed them only after TPL made narrowing amendments affecting every claim. The reexamination certificate had the effect of chopping off years of damages and restricting TPL's recovery substantially. Although the reexamination ultimately resulted in claims being confirmed, the length of the reexamination and the extent to which it weakened the '890 patent underscore the reasonableness of HTC's invalidity defenses and the lack of objective recklessness.

TPL also cannot establish the subjective prong of the willful infringement test. Under the subjective prong, "the patentee must also demonstrate that this objectively-defined risk (determined by the record developed in the infringement proceeding) was either known or so obvious that it should have been known to the accused infringer." *Seagate*, 497 F.3d at 1371. With respect to the '890 patent, there can be no claim of willful infringement because there is no evidence that HTC was placed on notice of this patent prior to TPL's filing of a countersuit against HTC on that patent. HTC did not list the '890 patent in its declaratory judgment complaint. (Doc. No. 1.) TPL has presented no evidence that HTC learned of the '890 patent or any claim of infringement before TPL countersued for infringement, which occurred after the filing of HTC's declaratory judgment complaint in the present action.

"To willfully infringe a *patent*, the patent must exist and one must have knowledge of it." *State Indus., Inc. v. A.O. Smith Corp.*, 751 F.2d 1226, 1236 (Fed. Cir. 1985) (emphasis in original); *see also Am. Original Corp. v. Jenkins Food Corp.*, 774 F.2d 459, 465 (Fed. Cir. 1985) (accused infringer's alleged awareness of pending patent application insufficient to show willfulness because "[t]o willfully infringe *a patent*, the patent must exist.") (quoting *State Indus., Inc.*, 751 F.2d at 1236) (emphasis in *State Indus.*). *Seagate* also makes clear that "a willfulness claim asserted in the original complaint must necessarily be grounded exclusively in the accused infringer's pre-filing conduct." 497 F.3d at 1374. TPL has offered no evidence of any pre-suit notice of alleged infringement by HTC of the '890 patent.

Nor can TPL base a claim of willful infringement on any alleged HTC conduct subsequent to the filing of the Complaint. The Federal Circuit held in *Seagate* that "[a] patentee who does not attempt to stop an accused infringer's activities [by moving for a preliminary injunction] should not be allowed to accrue enhanced damages based solely on the infringer's post-filing conduct." 497 F.3d at 1374. TPL never sought a preliminary injunction with respect to the '890 patent, and it cannot identify any unusual circumstances that could justify an allegation of willful infringement based on any post-filing conduct. Summary judgment against TPL's willful infringement claim is therefore warranted.

III. CONCLUSION

For the foregoing reasons, HTC respectfully requests that the Court grant its motion for partial summary judgment of non-infringement with respect to the '890 and '336 patents. With respect to the '890 patent, HTC respectfully requests that the Court grant summary judgment of non-infringement as to any alleged infringement occurring prior to March 1, 2011. As to the '336 patent, HTC respectfully requests that the Court grant summary judgment of non-infringement as to any alleged infringement occurring prior to December 15, 2009. Finally, HTC respectfully requests that the Court grant summary judgment of no willful infringement of the '890 patent.

Dated: July 16, 2013

Respectfully submitted,

COOLEY LLP
HEIDI L. KEEFE
MARK R. WEINSTEIN
KYLE D. CHEN

By: */s/ Mark R. Weinstein*

Attorneys for Plaintiffs
HTC CORPORATION and
HTC AMERICA, INC.

1153475 v2/HN

Please amend the claims as follows:

1. (Original) A microprocessor, which comprises a main central processing unit and a separate direct memory access central processing unit in a single integrated circuit comprising said microprocessor, said main central processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus, said internal data bus being bidirectionally connected to a loop counter, said loop counter being connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register, said internal data bus being connected to a memory controller, to a Y register of a return push down stack, an X register and a program counter, said Y register, X register and program counter providing outputs to an internal address bus, said internal address bus providing inputs to said memory controller and to an incrementer, said incrementer being connected to said internal data bus, said direct memory access central processing unit providing inputs to said memory controller, said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory.

2. (Original) The microprocessor of claim 1 in which said memory controller includes a multiplexing means between said central processing unit and said address/data bus, said multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus.

3. (Original) The microprocessor of claim 1 in which said memory controller includes means for fetching instructions for said central processing unit on said address/data bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle.

4. (Original) The microprocessor of claim 3 additionally comprising means connected to said means for fetching instructions for determining if multiple instructions fetched by said means for

fetching instructions require a memory access, said means for fetching instructions fetching additional multiple instructions if the multiple instructions do not require a memory access.

5. (Original) The microprocessor of claim 3 in which said microprocessor and a dynamic random access memory are contained in a single integrated circuit and said means for fetching instructions includes a column latch for receiving the multiple instructions.

6. (Original) The microprocessor of claim 1 in which said microprocessor includes a sensing circuit and a driver circuit, and an output enable line for connection between the random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level, said microprocessor being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

7. (Original) The microprocessor of claim 1 additionally comprising a ring oscillator variable speed system clock connected to said main central processing unit, said main central processing unit and said ring oscillator variable speed system clock being provided in a single integrated circuit.

8. (Original) The microprocessor of claim 7 in which said memory controller includes an input/output interface connected to exchange coupling control signals, addresses and data with said main central processing unit, said microprocessor additionally including a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.

9. (Original) The microprocessor of claim 1 in which said first push down stack has a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit.

10. (Original) The microprocessor of claim 9 additionally comprising a first pointer connected to said first plurality of stack elements, a second pointer connected to said second plurality of stack elements, and a third pointer connected to said third plurality of stack elements, said central processing unit being connected to pop items from said first plurality of stack elements, said first stack pointer being connected to said second stack pointer to pop a first plurality of items from said second plurality of stack elements when said first plurality of stack elements are empty from successive pop operations by said central processing unit, said second stack pointer being connected to said third stack pointer to pop a second plurality of items from said third plurality of stack elements when said second plurality of stack elements are empty from successive pop operations by said central processing unit.

11. (New) A microprocessor, which comprises a main central processing unit and a separate direct memory access central processing unit in a single integrated circuit comprising said microprocessor, said main central processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus, said internal data bus being bidirectionally connected to a loop counter, said loop counter being connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register, said stack pointer pointing into said first push down stack, said internal data bus being connected to a memory controller, to a Y register of a return push down stack, an X register and a program counter, said Y register, X register and program counter providing outputs to an internal address bus, said internal address bus providing inputs to said memory controller and to an incrementer, said incrementer being connected to said internal data bus, said direct memory access central processing unit providing inputs to said memory controller, said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory.

12. (New) The microprocessor of claim 11 in which said memory controller includes a multiplexing means between said central processing unit and said address/data bus, said

multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus.

13. (New) The microprocessor of claim 11 in which said memory controller includes means for fetching instructions for said central processing unit on said address/data bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle.

14. (New) The microprocessor of claim 13 additionally comprising means connected to said means for fetching instructions for determining if multiple instructions fetched by said means for fetching instructions require a memory access, said means for fetching instructions fetching additional multiple instructions if the multiple instructions do not require a memory access.

15. (New) The microprocessor of claim 13 in which said microprocessor and a dynamic random access memory are contained in a single integrated circuit and said means for fetching instructions includes a column latch for receiving the multiple instructions.

16. (New) The microprocessor of claim 11 in which said microprocessor includes a sensing circuit and a driver circuit, and an output enable line for connection between the random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level, said microprocessor being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

17. (New) The microprocessor of claim 11 additionally comprising a ring oscillator variable speed system clock connected to said main central processing unit, said main central processing unit and said ring oscillator variable speed system clock being provided in a single integrated circuit.

18. (New) The microprocessor of claim 17 in which said memory controller includes an input/output interface connected to exchange coupling control signals, addresses and data with

said main central processing unit, said microprocessor additionally including a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.

19. (New) The microprocessor of claim 11 in which said first push down stack has a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit.

20. (New) The microprocessor of claim 19 additionally comprising a first pointer connected to said first plurality of stack elements, a second pointer connected to said second plurality of stack elements, and a third pointer connected to said third plurality of stack elements, said central processing unit being connected to pop items from said first plurality of stack elements, said first stack pointer being connected to said second stack pointer to pop a first plurality of items from said second plurality of stack elements when said first plurality of stack elements are empty from successive pop operations by said central processing unit, said second stack pointer being connected to said third stack pointer to pop a second plurality of items from said third plurality of stack elements when said second plurality of stack elements are empty from successive pop operations by said central processing unit.

Patent Owner's Interview Summary

An in-person interview was conducted at the U.S. Patent Office on June 16, 2010. The participants were Examiner Joseph Pokrzywa, Examiner Sue Lao, and Patent Owner's Attorney Larry Henneman.

The interview started with a review of the operation of a push-down stack. Mr. Henneman explained how data items are pushed onto and popped off of a stack. Then, an example logic operation using 4 data items was demonstrated. (a OR (b AND c AND d)) The demonstration appeared to be helpful to both examiners.

Next, the "broadest reasonable interpretation" standard was discussed. Mr. Henneman pointed out that any interpretation must be consistent with the specification.

Then, the interpretation of the claim term "push down stack" was discussed. Mr. Henneman pointed out that the specification clearly set forth the push-pop operation of a push down stack. Col. 24, Lines 9-16 describes the push-pop operation. Col. 30 discloses severalregister operations using push and/or pop in conjunction with the parameter stack. Col. 31 discloses several logic and several math operations using push and pop in conjunction with the parameter stack.

Mr. Henneman pointed out that the Hull, Jr. reference did not disclose a stack, but rather a collection of registers that did not operate as a stack. Mr. Henneman then asserted that it would be inconsistent with the specification to interpret the "push down stack" of Claim 1 to read on the registers 50 of Hull, Jr. Examiner Pokrzywa seemed to agree and, indicated that he would reconsider this issue.

Next, the issue of whether any of the Transputer references disclosed a stack pointer was discussed. Mr. Henneman pointed out that the hard-wired stack of May (Registers A, B, and C) did not require a pointer, because the top of the stack (Register A) was always in the same location. Mr. Henneman further pointed out that the "stack pointer" was defined in Patent

Owner's specification, at Col. 21, Line 51, as a pointer into the parameter stack. In contrast, the instruction pointer of May (cited by the examiner as the stack pointer) pointed to instructions of a process.

Mr. Henneman asked how the instruction pointer of May could be characterized as a stack pointer. Examiner Pokrzywa responded that the stack pointer of Claim 1 was not explicitly associated with the first push down stack of Claim 1. Therefore, he concluded that if the instruction pointer of May pointed to any position in any stack, then the instruction pointer could be considered a stack pointer. Mr. Henneman objected that a stack pointer operates to indicate/track the location of a particular position (e.g., top item) within a stack. The Examiner stated that under the *broadest reasonable interpretation* standard, any address that pointed to a stack could be considereda stack pointer. Mr. Henneman disagreed.

It was suggested to amend Claim 1 to clearly associate the stack pointer with the first push down stack. Mr. Henneman indicated that Patent Owners would be very reluctant to amend Claim 1 without agreement that the amendment would be sufficient to overcome the rejections. Examiner Pokrzywa agreed that he would consider whether a proposed amendment would overcome the rejections, before such an amendment was filed.

Subsequently, Examiner Pokrzywa agreed that such an amendment would overcome the current rejections.

Patent Owners thank Examiner Pokrzywa and Examiner Lao for extending the interview and for the constructive nature of the interview.

App. Serial No.: 90/009,388
Atty. Docket No.: 0081-011D1X1

Examiner's Interview Summary

Discussed the terms "push down stack" and "stack pointer". First, with respect to the "push down stack", the Patent Owner discussed the differences between a push down stack and what is shown in Hull. Upon a subsequent response, the examiner will reconsider the rejection to claim 1 as being anticipated by Hull, Jr. based on the Patent Owner's discussion of the "push down stack". However, the examiner noted that the reference of May is seen to teach of a push dwn stack.

Continuing, with respect to the "stack pointer" the Patent Owner argues that the "stack pointer" points to the push down stack and the return stack pointer points to the return push down stack. The Patent Owner continued discussing that the reference of May does not point to the push down stack. However, similar to the Response to Arguments in the previous Office Action, the current claim language does not require this relationship of the stack pointer to the push down stack.

The Patent Owner suggested possibly amending the claim to clarify this point, which the examiner would consider. With that, the Patent Owner may propose a subsequent amendment, whereby the examiner expressed that the cited prior art references would need to be reviewed before any decision as to overcoming the current rejection.

Examiner interview summary, mailed June 16, 2010, at 2

App. Serial No.: 90/009,388
Atty. Docket No.: 0081-011D1X1

REMARKS

These remarks are in response to the Office Action dated April 29, 2009, which has a shortened statutory period for response set to expire June 29, 2010. No extension of time is necessary.

Claims

Claims 1-20 are currently pending in the above-identified reexamination application. Claims 1-10 remain as issued. New Claims 11-20 are added. Claims 1-8 are finally rejected over prior art. Claims 9 and 10 are indicated to be patentable and/or confirmed.

Reconsideration of the prior art rejections of Claims 1-8 is requested. Favorable consideration of new Claims 11-20 is also respectfully requested.

Rejections Under 35 U.S.C. §102

Claims 1-6 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent Number 4,989,113 (Hull, Jr. et al.) (hereinafter "Hull"). Patent Owners respectfully traverse.

Claim 1 recites (in part): "a first push down stack." However, Hull does not disclose a first push down stack. Rather, Hull discloses a plurality of registers 50 (50a-h) that do not operate as a push down stack. The registers have no push-pop relationship to each other.The registers have no push-pop relationship with any other data structure.

Moreover, even under the *broadest reasonable interpretation* standard, it would be improper to interpret the registers 50 of Hull, by themselves, as a push down stack, because that interpretation would be inconsistent with Patent Owners' specification.The specificationdisclosesa top item register and a next item register connected to provide inputs to the ALU. SeeFigs. 1 and 13. But these two registers alone cannot operate as a push down stack.

In the specification,the Top of Stack and Next Item registers are functionally (push/pop) associated with theparameter stack 74. This push down stack operates in a push-pop relationship

with the Top of Stack and Next Item registers. See, e.g. Figs. 13 and 21. The push-pop relationship is facilitated by a "stack pointer," defined in the specification[1] as a pointer into the parameter stack[2]. "Parameter stack" is also defined in the specification[3]. The parameter stack is the push down stack used for math and logic operations in cooperation with the Top of Stack and Next Itemregisters[4]. The math and logic instructions pop operands from the parameter stack and push results back onto the parameter stack. Col. 21, lines 29-32.

The parameter stack is illustrated in Fig. 2 as element 74, in Fig. 13 as element 74 and in Fig. 21 as elements 450, 452 and 454 which the text states substitutes for the parameter stack 74. See, col. 11, line 32-33for Fig. 2; col. 14, lines 32-33for Fig. 13; and col. 18, lines 13-45for Fig. 21. The parameter stack is also denominated as a "push down stack" in, for example, the abstract, at col. 3, lines 6-10; at col. 3, lines 36-44; at col. 6, lines 21-22.

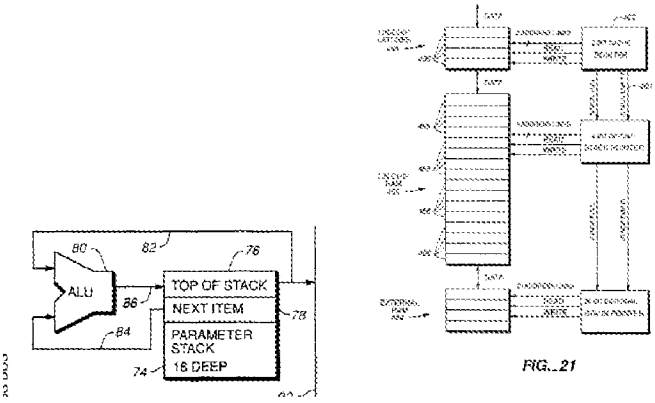


FIG._21

Because Hull does not disclose "a first push down stack", as recited in Claim 1, Hull does not anticipate Claim 1. Therefore, patent Owners respectfully request reconsideration and withdrawal of the rejection of Claim 1 under 35 U.S.C. §102. Claims 2-6 depend, either directly or indirectly, from Claim 1 and are, therefore, distinguishable over Hull for at least the same reasons as Claim 1.

[1] Col. 21, line 51
[2] Id.
[3] Col. 21, lines 5-15 and 30-32
[4] Id.

In addition, for the reasons set forth in Patent Owners' prior response, Patent Owners respectfully assert that Hull fails to disclose "a stack pointer", as recited in Claim 1. Those reasons are incorporated herein by reference. Independent Claim 1, and dependent Claims 2-6 are, therefore, distinguishable over Hull for these additional reasons.

Rejections under 35 U.S.C. §103

Claims 1-4 are rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent Number 4,758,948 (May '948), which incorporates by reference U.S. Patent Number 4,680,698 (Edwards '698), further in view of the "Transputer Reference Manual," (the Transputer Manual). Collectively, these references are referred to hereinafter as the "Transputer references."

Patent Owners respectfully traverse.

In order to establish a prima facie case of obviousness, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. M.P.E.P. §2143.

Claim 1 recites (in part) "a stack pointer." However the cited references fail to disclose "a stack pointer" in combination with the other elements of Claim 1.

Patent Owners' previous response pointed out that the Transputer references fail to disclose a stack pointer. Those arguments are incorporated herein by reference in their entirety.

The final office action advances two main responses to Patent Owners' prior arguments. First, the final office action asserts that the IPTR 50 of May '948 can be seen as pointing to the stack of the A, B, and C registers because it "is shown as being bidirectionally connected to the stack registers A, B, and C." Second, the final office action asserts that IPTR S 65 of May '948 is a pointer to a register stack. Moreover, these arguments are advanced in view of the broadest reasonable interpretation standard and the Examiner's position that Claim 1 does not expressly require that the stack pointer be associated with the first pushdown stack. Patent Owners acknowledge, but do not necessarily agree with, this interpretation of Claim 1.

IPTR 50 of May '948 is not a stack pointer

Patent Owners respectfully submit that the instruction pointer of May '948(IPTR 50) does not "point" to the stack registers A, B and C by virtue of being bidirectionally connected thereto or because it loads the contents of A during a general call. Rather, IPTR 50 holds the memory address of the next instruction to be executed and thus points to the location in memory of that next instruction, as stated by May '948. It is not a stack pointer to the stack (A, B, C) of May '948. Indeed, IPTR 50 is not a pointer to any stack.

Patent Owners respectfully, but vehemently, object to any interpretation that equates "bidirectionally connected" with "pointing," as unreasonable. Such an interpretation strips the term "pointer" of any real meaning. Under the proposed interpretation, every element of May '948 that is coupled to X bus, Z bus, and/or bidirectional data bus 31 would have to be considered a pointer. This demonstrates the unreasonableness of interpreting "pointing" as "bidirectionally connected."

IPTR 50 of May '948, like the program counter 130 of US '890, holds the address of the next instruction to be executed.

IPTR REG	A register 50 which holds the instruction pointer (IPTR) of any process indicated by register 51

May'948 at col. 8, lines 10-12

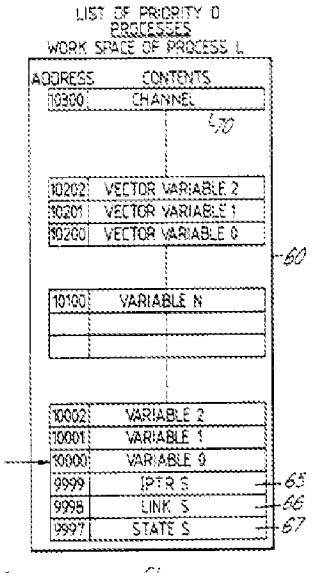
It is clear that IPTR 50 is the program counter of May. For at least this reason, IPTR 50 cannot be interpreted as the claimed stack pointer.

IPTR S 65 of May '948 is not a stack pointer

The final office action also indentified IPTR S 65 as a stack pointer. IPTR S 65, however, is simply the "program counter" address of a process awaiting execution. It is stored in

a predefined location in a workspace containing essential information for the waiting process. When a process is activated, the contents of IPTR S 65 is loaded into IPTR 50.

In more detail, May describes a multi-processor. When May switches from one process to another, it loads a number of registers from a workspace associated with the process being given control. Each workspace, e.g., workspace L below, includes a number of variables, a machine state 67, a link 66 to the next workspace in a queue of workspaces, and an instruction pointer IPTR S 65 that points to the next instruction for that process. See Fig. 3, below. When a process, such as L, is activated, the computer loads the computer's program counter IPTR 50 with the contents of IPTR S 65.



May '948, Fig. 3, excerpt

See, e.g., May'948 at column 8, lines 10-12; column 35, lines 16-24; and column 35, lines 44-46. Just like US '890's program counter 130, May's instruction pointer IPTR 50 (S 65) points to instructions in memory. Neither IPTR 50 nor IPTR S 65 point to anythingthat could be considered a stack.

The Transputer's process queues are not stacks

The Transputer References, including May '948, operate with two sequential lists of process workspaces identified in May as queues.[5] See, e.g., May at col. 35, lines 23-26. There are two queues of these workspaces because the Transputer has two process priorities. One queue is associated with priority 0. A second is associated with priority 1. Col. 36, lines 10-32. A WPTR register 51 points to the workspace for the current process. Queue pointers,FPTR 53 and BPTR 52, point respectively to the front and end of a queue of waiting process workspaces. Each of the queue elements includes a pointer, Link S 66, thatpoints to the next queue element.

WPTR REG	A register 51 for holding the workspace pointer (WPTR) of the current process or an interrupted process.
BPTR REG	A register 52 holding the workspace pointer of a process at the end of a list of priority 1 processes awaiting execution.
FPTR REG	A register 53 holding the workspace pointer of a process at the front of a list of priority 1 processes awaiting execution.

Col. 8, lines 12-18.

As described by May and as well known in the art, process queues operate sequentially, on a first-in, first-out basis. See, e.g., http://en.wikipedia.org/wiki/FIFO. When processing of one element completes, control is passed to the next sequential element in the queue.

However, the examiner has cited both IPTR S 65 and LINK S 66 as stack pointers, the latter for the "return stack element." See, final action at page 9. It follows that the examiner cites May's process queues as stacks. However, they are not stacks within the meaning of US '890 or within the understanding of the meaning of stack to one of ordinary skill in the art.

[5] A sequential list of processes is known in the art as a FIFO queue. See, e.g., http://en.wikipedia.org/wiki/FIFO for a description of FIFO queues. The same distinction was known to the art in 1989, the year of filing of the instant application. See, e.g., Brandenburg, Franz-Josef, Analogies of PAL and COPY, page 61, Fundamentals of Computation Theory (Berlin, Heidelberg, New York: Springer-Verlag, 1981) at page 62.:

As is well known in the art, stacks are data structures that operate in a LIFO manner, last-in, first out. See the linked Wikipedia page. http://en.wikipedia.org/wiki/LIFO_(computing). See also, Flynn, Roger R., *An Introduction to Information Science* (New York: Marcel Dekker, Inc., 1987) at page 758:

> to handling multiple entries is a stack. A stack is simply a series of locations (say an array) in which items are "pushed onto the stack" when we want to store them, and "popped off" when we want to retrieve them. The items are "pushed on" so that they go one on top of the other, then popped off in reverse order, much as the plates in a cafeteria or pancakes on a plate. Because of the reverse removal, the stack is sometimes referred to as a last-in-first-out or LIFO data structure. (Queues or lines, as in a grocery store, are first-in-first-out or FIFO.) For our example, we would use the stack to remember the parents.

ROGER R. FLYNN, AN INTRODUCTION TO INFORMATION SCIENCE758 (1987)

Google Books Link

As therein described, when something is added to a stack, it pushes the rest of the items down. When something is removed, i.e., popped from the stack, all the rest of the items pop up. Access to a stack is at the location indicated by a stack pointer, unless the stack has a fixed top as shown in May, where the rest of the stack has a push-pop relationship with the fixed top of stack (i.e., data is physically transferred up and down in the registers).

A stack pointer, as is commonly understood in the art, is the address (or a storage element that contains the address) of a stack element(also known as a "node"), generally the most recent item (also known as the top of the stack). See, e.g., http://www.yourdictionary.com/computer/stack-pointer; or http://dictionary.die.net/stack%20pointer. While these links are to current dictionaries, the historical understanding of those skilled in the art at the time of filing of the US '890 in 1989 is consistent. For example, the discussion of "stack pointer" from Information Representation and Manipulation in a Computer pg. 76 , E.S. Page, L.B Wilson, 2d Edition 1978 Cambridge University Press is reproduced below.

Moving a large number of nodes in storage every stack operation is very inefficient. Instead a stack would be implemented in a computer by using a stack pointer T which points to the top node of the stack and moving the pointer instead of all the nodes of the stack. If the stack is empty, the stack pointer T = 0. The stack pointer advances when we place an item on the stack and retreats when we take the top item off the stack. This

E.S. PAGE & L.B. WILSON, INFORMATION REPRESENTATION AND MANIPULATION IN A COMPUTER 76 (2d ed. 1978)

Google Books link

US'890 has both queues and stacks. When it uses the term "queue," it refers exclusively to a queue of instructions, which are executed sequentially. See, e.g. US '890 at col. 7, line 49, col. 12, lines 28-43 and line 56. When it refers to stacks, it refers exclusively and only to LIFO"push down stacks." See, e.g., col. 21 at line13. The stacks of US'890 are described throughout as "push down stacks." The term push down stack is unambiguously linked to the concept of LIFO. Push down stacks ARE LIFO stacks and are not anything else.

Further, the description of stack operations at col. 24, lines 9-15expressly states that the stacks operate by push and pop functionality.

For math and logic operations, the microprocessor 50 exploits the inherent advantage of a stack by designating the source operand(s) as the top stack item and the next stack item. The math or logic operation is performed, the operands are popped from the stack, and the result is pushed back on the stack. The result is a very efficient utilization of instruc-

Col. 24, lines 9-15

The specification further states that US'890's math and logic operations always use stack operations.

A stack has the advantage of faster operation compared to on-chip registers by avoiding the necessity to select source and destination registers. (A math or logic operation always uses the top two stack items as source and the top of stack as destination.) The stack's disadvantage is that it makes

Col. 14, lines 55-59

Moreover, consistent with the specification, claim 1 of US'890 defines each stack as a push down stack: "first push down stack" and "return push down stack." A push down stack is a LIFO stack. It is not a FIFO queue. Both the claim language and the specification is consistent in this regard.

For all these reasons, the process queues of May are not stacks. Therefore, the associated pointers to the process queues of May are not, for this reason, "stack" pointers and cannot be the claimed "stack pointer" of Claim 1.

However, May'948 does have a push down stack embodied in registers A, B and C. However, these registers are internally connected in a push pop relationship. They do not require and do not have an associated stack pointer. In fact, a stack pointer would interfere with the operation of such a stack making it non operational, because operands are pushed onto the stack only through the A register. Any stack pointer allowing an operand to be pushed onto the stack through a different element would render the May '948 stack non operational. So, not only does May '948 not have a stack pointer, it cannot have a stack pointer associated with its stack.

Still, the final action suggests that IPTR S 65 is a "stack pointer" because IPTR 50 is bidirectionally connected to the registers and because a call operation includes the following operation:

```
general call
def:                    SEQ
                          Oreg[Pri] := IptrReg[Pri]
                          IptrReg[Pri] := Areg[Pri]
                          Areg[Pri] := Oreg[Pri]
purpose:                to perform a procedure call, with
                        a new instruction pointer in Areg
```

May'948, col. 27, lines 36-46

What this instruction does, among other things, is load IPTR 50 with the contents of the A register (using the O register as a temporary register). The A register had previously been loaded with the address of a called subroutine, aka, procedure. At the same time, the current IPTR contents are loaded into A register for use by the called subroutine.

However, merely being connected to or loading the contents of the "A register" is far different from "pointing" to the stack. US'890, and indeed the cited references and those of ordinary skill in the art, all use "pointer" in the same way: A pointer is something that contains the address of the thing to which the pointer points. See, e.g., http://en.wikipedia.org/wiki/Pointer_(computing):
"In computer science, a pointer is a programming language data type whose value refers directly to (or "points to") another value stored elsewhere in the computer memory using its address."
See also, *The Essentials of Data Structures I*, *supra*("a pointer is merely an address to a node").

This is the very way the term is used in US'890. The term consistently is used to describe a storage element, such as a latch or register, the contents of which address a memory location or a particular register. See e.g., the definition of program counter at column 21 lines 21-26. See also the discussion of the program counter at column 27, line 63 to column 28 line 2,

> "PROGRAM COUNTER -- a 30 bit memory pointer normally used to point to four-byte instruction groups. ...When used as [a] memory pointer, the PC is also incremented after each operation."

For the foregoing reasons, Patent Owners respectfully assert that any pointers disclosed in the Transputer references fail to point to any stack and cannot, therefore, be considered stack pointers. Moreover, the Transputer references fail to disclose any pointers to the stack registers A, B, and C. Therefore, the Transputer references fail to disclose a stack pointer.

Because the cited references fail to disclose a "stack pointer", as recited in Claim 1, no prima facie case of obviousness is established with respect to Claim 1. Patent owners, therefore, respectfully request reconsideration and withdrawal of the rejection of Claim 1 under 35 U.S.C.

§103 over the Transputer references. Claims 2-4 depend, either directly or indirectly, from Claim 1 and are, therefore, distinguishable over the cited references for at least the same reasons as Claim 1.

Claims 7 and 8

Claims 7 and 8 are rejected under 35 U.S.C. § 103 as being unpatentable over Hull in view of U.S. Patent Number 4,766,567 (Kato).

Patent Owners respectfully traverse.

Claims 7 and 8 depend, either directly or indirectly, from Claim 1 and, therefore, include all of the limitations of Claim 1. As indicated above, Hull fails to disclose a "first push down stack," as recited in Claim 1. It does not appear to Patent Owners, and the Examiner has not asserted, that Kato discloses a "first push down stack." Because the combined references fail to teach or suggest all of the limitations of Claim 1 and dependent Claims 7 and 8, no prima facie case of obviousness is established with respect to Claim 7 or Claim 8. Therefore, Patent Owners respectfully request withdrawal of the rejections of Claim 7 and Claim 8 under 35 U.S.C. §103.

For the foregoing reasons, Patent Owners respectfully request reconsideration and review of all rejections under 35 U.S.C. §103.

New Claims 11-20

Claims 11-20 are new. Claim 11 is independent. Claims 12-20 depend from claim 11. The new claims are substantially similar to claims 1-10, except that Claim 11 includes language that Examiner Pokrzywa has indicated overcomes all of the current rejections. In particular, Claim 11 recites (in part) "said stack pointer pointing into said first push down stack,"clarifying the association of the stack pointer and the first push down stack.

Support for new Claims 11-20 is provided at least by issued Claims 1-10, Fig. 2, and Col. 21, Line 51 of the specification, which defines the stack pointer as a pointer into the parameter stack, which, as discussed above, is also denominated the push down stack.

No new matter is added.

App. Serial No.: 90/009,388
Atty. Docket No.: 0081-011D1X1

For all of the foregoing reasons, Patent Owners believe Claims 1-8 (Examiner has confirmed the patentability of Claims 9 and 10) are in condition for confirmation of patentability. For the same reasons, new claims 11-20 are patentable. Should the Examiner undertake any action other than confirmation of Claims 1-8, and 11-20, or if the Examiner has any questions or suggestions for expediting the prosecution of this reexamination application, the Examiner is requested to contact Patent Owners' attorney at (269) 279-8820.

Respectfully submitted,

June 29, 2010

Date:_____

/Larry E. Henneman, Jr./

_____

Larry E. Henneman, Jr., Reg. No. 41,063
Attorney for Patent Owners
Henneman& Associates, PLC
70 N. Main St.
Three Rivers, MI 49093

CERTIFICATE OF FACSIMILE TRANSMISSION (37 CFR 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being electronically filed or transmitted via facsimile, on the date shown below, to: MS Ex Parte Reexamination, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, at (571) 273-8300.

June 29, 2010

Date:_____

/Larry E. Henneman, Jr./

_____

Larry E. Henneman, Jr.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

DO NOT USE IN PALM PRINTER

(THIRD PARTY REQUESTER'S CORRESPONDENCE ADDRESS)

FISH & RICHARDSON, PC
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/009,388*.

PATENT NO. *5530890*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Ex Parte Reexamination Advisory Action Before the Filing of an Appeal Brief	**Control No.** 90/009,388	**Patent Under Reexamination** 5530890	
	Examiner JOSEPH R. POKRZYWA	**Art Unit** 3992	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

THE PROPOSED RESPONSE FILED *29 June 2010* FAILS TO OVERCOME ALL OF THE REJECTIONS IN THE FINAL REJECTION MAILED *29 April 2010*.

1. ☐ Unless a timely appeal is filed, or other appropriate action by the patent owner is taken to overcome all of the outstanding rejection(s), this prosecution of the present *ex parte* reexamination proceeding WILL BE TERMINATED and a Notice of Intent to Issue *Ex Parte* Reexamination Certificate will be mailed in due course. Any finally rejected claims, or claims objected to, will be CANCELLED.

   THE PERIOD FOR RESPONSE IS EXTENDED TO RUN _____ MONTHS FROM THE MAILING DATE OF THE FINAL REJECTION. Extensions of time are governed by 37 CFR 1.550(c).

NOTICE OF APPEAL

2. ☒ An Appeal Brief is due two months from the date of the Notice of Appeal filed on *29 July 2010* to avoid dismissal of the appeal. See 37 CFR 41.37(a). Extensions of time are governed by 37 CFR 1.550(c). See 37 CFR 41.37(e).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final action, but prior to the date of filing a brief, will not be entered because:
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the proceeding in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____ (See 37 CFR 1.116 and 41.33(a)).
4. ☒ Patent owner's proposed response filed *29 June 2010* has overcome the following rejection(s): *see attached Detailed Action*
5. ☒ The proposed new or amended claim(s) *11-20* would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
6. ☒ For purposes of appeal, the proposed amendment(s) a)☐ will not be entered, or b)☒ will be entered and an explanation of how the new or amended claim(s) would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) patentable and/or confirmed: *5-20*
   Claim(s) objected to: _____
   Claim(s) rejected: *1-4*
   Claim(s) not subject to reexamination: _____

AFFIDAVIT OR OTHER EVIDENCE

7. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because patent owner failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
8. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence fails to overcome all rejections under appeal and/or appellant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
9. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

10. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.
11. ☒ Note the attached Information Disclosure Statement(s), PTO/SB/08, Paper No(s) *7/16/2010 & 7/8*.
12. ☐ Other:_____.

cc: Requester (if third party requester)

DETAILED ACTION

Response to Amendment

1. The Patent Owner submitted an after-final amendment 6/29/2010. A Notice of Appeal was filed 7/29/2010. With this, the Patent Owner's amendment dated 6/29/2010 has been entered and made of record.

2. Briefly, claims 1-10 of U.S. Patent Number 5,530,890 (hereafter "the '890 Patent") originally issued on June 25, 1996. In the after-final amendment dated 6/29/2010, the Patent Owner added claims 11-20, whereby new independent claim 11 adds the limitation of "said stack pointer pointing into said first push down stack" to the text of what appear in original claim 1, and new dependent claims 12-20 directly correspond to original dependent claims 2-10.

3. Continuing, in the final Office action dated 4/29/2010, dependent claims 9 and 10 of the '890 Patent were indicated as being patentable, while claims 1-8 of the '890 Patent were rejected in the following manner:

Claims 1-6 stands rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Number 4,989,113, issued to Hull, Jr. *et al.* (hereafter "Hull, Jr.");

Claims 1-4 stands rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Number 4,758,948, issued to May *et al.* (hereafter "May'948"), which incorporates by reference the reference of U.S. Patent Number 4,680,698, issued to

Edwards *et al.* (hereafter Edwards'698"), further in view of the "Transputer Reference Manual", published by Inmos Ltd., 1988 (hereafter the "Transputer Manual"); and

Claims 7 and 8 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Hull, Jr. in view of Kato *et al.* (U.S. Patent Number 4,766,567, hereafter "Kato").

4. With the filing of the Notice of Appeal dated 7/29/2010, new claims 11-20 have been entered, and as discussed below, are believed to be patentable. Further, as also discussed below, the rejection of claims 1-6 as being anticipated by Hull, Jr., and the rejection of claims 7 and 8 as being unpatentable over Hull, Jr. in view of Kato have been withdrawn, as the Patent Owner's arguments submitted 6/29/2010 are persuasive. However, the rejection of claims 1-4 as being unpatentable over May'948, which incorporates by reference the reference of Edwards'698, further in view of the Transputer Manual, remains, as the examiner believes that these references are still seen to teach the features of independent claim 1 and dependent claims 2-4, as currently worded.

Response to Arguments

5. Patent Owner's arguments, on pages 10-12, filed 6/29/2010, with respect to the rejection of claims 1-6, as being anticipated by Hull, Jr., have been fully considered and are persuasive. Specifically, upon reconsideration, the Hull, Jr. reference is unclear if the plurality of registers 50 (50a-h), seen in Fig. 2, is actually the claimed "first push-down stack". While the examiner still believes that registers 50 are shown as a "stack", as discussed by the Patent Owner on pages 10-12, there is not a description within Hull, Jr. the expressly describes a "push-down stack". Therefore, the rejection of claims 1-6 as being anticipated by Hull, Jr. has been withdrawn.

6. Continuing, for the same reasons discussed above, with respect to the rejection of dependent claims 7 and 8, under 35 U.S.C. 103 as being unpatentable over Hull, Jr. in view of Kato, as noted above, the rejection of these claims is withdrawn. Upon reconsideration, the primary reference of Hull, Jr. is unclear if the plurality of registers 50 (50a-h), seen in Fig. 2, is actually the claimed "first push-down stack". Kato is not seen to remedy this shortfall. Therefore, the rejection of claims 7 and 8 as being unpatentable over Hull, Jr. in view of Kato has been withdrawn.

7. Continuing, with respect to the rejection of claims 1-4, cited as being unpatentable over May'948, which incorporates by reference Edwards '698, further in view of the Transputer Manual, the Patent Owner's arguments filed 6/29/2010 have been fully considered but they are not persuasive.

8. Particularly, on page 13, the Patent Owner argues that the May '948 Patent does not teach of a "stack pointer", whereby "the instruction pointer of May '948 (IPTR 50) does not 'point' to the stack registers A, B, C by virtue of being bidirectionally connected thereto or because it loads contents of A during a general call.....IPTR 50...is not a stack pointer to the stack (A,B,C) of May '948." However, with this, the examiner notes that the current language of claim 1 does not require that a stack pointer **points to the push-down stack**. Currently claim 1 requires "...said internal data bus being bidirectionally connected to a stack pointer, return stack pointer mode register, and instruction register..." Thus, there is no function claimed for the "stack pointer", only that a stack pointer is bidirectionally connected to an internal bus. With this, the interpretation noted in the final Office action dated 4/29/2010 of the IPTR 50, which is described in the May'948 Patent as being a pointer, which is utilized by the stack, can be reasonably considered as a "stack pointer".

9. Recall that claims are given their broadest reasonable interpretation, consistent with the specification. Specifically, MPEP 2111 [R-5], states, in part:

> During patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification." >The Federal Circuit's en banc decision in *Phillips v. AWH Corp.*, 415 F.3d 1303, 75 USPQ2d 1321 (Fed. Cir. 2005) expressly recognized that the USPTO employs the "broadest reasonable interpretation" standard:
>
> > The Patent and Trademark Office ("PTO") determines the scope of claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." In re Am. Acad. of Sci. Tech. Ctr., 367 F.3d 1359, 1364[, 70 USPQ2d 1827] (Fed. Cir. 2004). Indeed, the rules of the PTO require that application claims must "conform to the invention

> as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description." 37 CFR 1.75(d)(1).

10. Thus, in reviewing the reference of May '948, as stated in col. 35, lines 12-32, May '948 states "The instruction pointer (IPTR) of any process in the list is stored in the IPTR location 65 of its workspace as shown in FIG. 3." Continuing, as described in the final Office action dated 4/29/2010, in viewing Fig. 2, May '948 illustrates the IPTR 50 is shown as being bidirectionally connected to the stack registers A, B, and C. With this, the instruction pointer IPTR of May '948 can be seen as pointing to the stack of the A, B, and C registers. This is also described in May '948 on col. 27, lines 36-42, which states that a purpose of the particular register manipulation is "to perform a procedure call, with a new instruction pointer in Areg". With this, the instruction pointer is utilized by the Areg, being the top of the push-down stack, as described in May '948 on col. 8, lines 44-56. Therefore, the examiner believes that the IPTR 50 can be reasonably interpreted as being the "stack pointer".

11. However, the examiner will further discuss a separate interpretation of the "stack pointer", as a different pointer described in the May '948 reference appears to function similarly to the definitions provided by the Patent Owner on pages 15-19 of the "stack pointer". Particularly, on page 16, the Patent Owner defines a "stack pointer" as "the address (or a storage element that contains the address) of a stack element (also known as a "node")...", or on page 19 as "A pointer is something that contains the address of the thing to which the pointer points....a

pointer is a programming language data type whose value refers directly to (or "points to") another value stored elsewhere in the computer memory using its address". With this, the May'948 reference discloses the WPTR, stored in the WPTR REG 51, whereby in col. 6, lines 52-63, May '948 states "A workspace pointer WPTR is used to point to a set location for the process workspace." Continuing, on col. 9, lines 25-42, May '948 states "The address of the first local variable of the workspace is indicated by the workspace pointer (WPTR)."

12. Continuing, on col. 44, line 67-col. 45, line 4, May'948 states "According to lines 5 and 6 this is tested to see if it is -1 and if so the contents of the A register are written to the memory location indicated by the WPTR REG and the A register has the value machine TRUE indicating that this is the selected process." Thus, the workspace pointer WPTR is clearly a "stack pointer", as the May'948 expressly states that the WPTR is "the address (or a storage element that contains the address) of a stack element", whereby the WPTR is the address to where the element from the A register, being part of the stack, is stored.

13. Therefore, the rejection of claims 1-4, as cited in the final Office action dated 4/29/2010, under 35 U.S.C. 103(a) as being unpatentable over May '948, expressly incorporating Edwards '698 Patent, further in view of the Transputer Manual, is maintained.

14. With respect to new claims 11-20, whereby new independent claim 11 includes the features of "said stack pointer pointing into said first push down stack", the examiner notes that this claim is believed to be patentable, as the pointers described in the May '948 reference are not particularly seen to point "into said stack pointer". As noted above, on col. 44, line 67-col. 45, line 4, May'948 states "According to lines 5 and 6 this is tested to see if it is -1 and if so the contents of the A register are written to the memory location indicated by the WPTR REG and the A register has the value machine TRUE indicating that this is the selected process." With this, the stack pointer WPTR points to a memory location for the top register A of the push-down stack. But the WPTR is not seen to point into the push-down stack. Similarly, the IPTR is not seen to point "into the push-down stack". The secondary references of Edwards '698 and the Transputer Manual are also not seen to expressly describe this feature. Thus, with this feature, claim 11 would be rendered patentable over the cited prior art of May'948, Edwards'698, and the Transputer Manual.

Information Disclosure Statement

15. The references listed in the Information Disclosure Statement submitted on 7/16/2010 and 7/8/2010 have been received and entered into the record.

16. Continuing, the examiner notes that the numerous Office actions from related U.S. Patent Applications and the numerous Court documents submitted in the above noted Information Disclosure Statements have been received, and considered, but are not proper to be listed on an Information Disclosure Statement, as the documents are not proper be printed on the face of a Reexamination Certificate, once issued. Thus, these citations have been indicated as having a line through the citation in the Information Disclosure Statement.

17. Further, the examiner notes that MPEP 2256, under the heading "Prior Art Patents and Printed Publications Reviewed by Examiner in Reexamination" states, in part:

> Where patents, publications, and other such items of information are submitted by a party (patent owner or requester) in compliance with the requirements of the rules, **the requisite degree of consideration to be given to such information will be normally limited by the degree to which the party filing the information citation has explained the content and relevance of the information**. The initials of the examiner placed adjacent to the citations on the form PTO/SB/08A and 08B or its equivalent, without an indication to the contrary in the record, do not signify that the information has been considered by the examiner any further than to the extent noted above. [Emphasis added.]

18. Additionally, MPEP 609.05(b) states:

> The information contained in information disclosure statements which comply with both the content requirements of 37 CFR 1.98 and the requirements, based on the time of filing the statement, of 37 CFR 1.97 will be considered by the examiner. Consideration by the examiner of the information submitted in an IDS means that **the examiner will consider the documents in the same manner as other documents in Office search files are considered by the examiner while conducting a search of the**

> **prior art in a proper field of search**. The initials of the examiner placed adjacent to the citations on the ** PTO/SB/08A and 08B or its equivalent mean that the information has been considered by the examiner to the extent noted above. [Emphasis added.]

19. With this, the examiner notes that the prior art references listed in the Information Disclosure Statements submitted on 7/16/2010 and 7/8/2010 have been considered by the examiner to at least the "degree to which the party filing the information citation has explained the content and relevance of the information", and in "the same manner as other documents in Office search files are considered by the examiner while conducting a search of the prior art in a proper field of search" (see attached PTO/SB/08A's).

Conclusion

20. **All** correspondence relating to this ex parte reexamination proceeding should be directed:

By Mail to: Mail Stop *Ex Parte* Reexam
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand: Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Registered users of EFS-Web may alternatively submit such correspondence via the electronic filing system EFS-Web, at https://sportal.uspto.gov/authenticate/authenticateuserlocalepf.html. EFS-Web offers the benefit of quick submission to the particular area of the Office that needs to act on the correspondence. Also, EFS-Web submissions are "soft scanned" (i.e., electronically uploaded) directly into the official file for the reexamination proceeding, which offers parties the opportunity to review the content of their submissions after the "soft scanning" process is complete.

Any inquiry concerning this communication should be directed to Joseph R. Pokrzywa at telephone number 571-272-7410.

Signed:

Joseph R Pokrzywa
Primary Patent Examiner
Central Reexamination Unit 3992
(571) 272-7410

Conferees: /r.g.f./
ESK

Notice of Intent to Issue Ex Parte Reexamination Certificate	Control No.	Patent Under Reexamination	
	90/009,388	5530890	
	Examiner	Art Unit	
	JOSEPH R. POKRZYWA	3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ Prosecution on the merits is (or remains) closed in this *ex parte* reexamination proceeding. This proceeding is subject to reopening at the initiative of the Office or upon petition. *Cf.* 37 CFR 1.313(a). A Certificate will be issued in view of
   - (a) ☐ Patent owner's communication(s) filed: _____.
   - (b) ☐ Patent owner's late response filed: _____.
   - (c) ☐ Patent owner's failure to file an appropriate response to the Office action mailed: _____.
   - (d) ☐ Patent owner's failure to timely file an Appeal Brief (37 CFR 41.31).
   - (e) ☒ Other: *Telephone Interview dated 9/22/2010*.

   Status of *Ex Parte* Reexamination:
   - (f) Change in the Specification: ☐ Yes ☒ No
   - (g) Change in the Drawing(s): ☐ Yes ☒ No
   - (h) Status of the Claim(s):
     - (1) Patent claim(s) confirmed: *5-10*.
     - (2) Patent claim(s) amended (including dependent on amended claim(s)): _____
     - (3) Patent claim(s) canceled: *1-4*.
     - (4) Newly presented claim(s) patentable: 11-20.
     - (5) Newly presented canceled claims: _____.
     - (6) Patent claim(s) ☐ previously ☐ currently disclaimed: _____
     - (7) Patent claim(s) not subject to reexamination: _____.

2. ☒ Note the attached statement of reasons for patentability and/or confirmation. Any comments considered necessary by patent owner regarding reasons for patentability and/or confirmation must be submitted promptly to avoid processing delays. Such submission(s) should be labeled: "Comments On Statement of Reasons for Patentability and/or Confirmation."

3. ☐ Note attached NOTICE OF REFERENCES CITED (PTO-892).

4. ☒ Note attached LIST OF REFERENCES CITED (PTO/SB/08 or PTO/SB/08 substitute).

5. ☐ The drawing correction request filed on _____ is: ☐ approved ☐ disapproved.

6. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the certified copies have
   - ☐ been received.
   - ☐ not been received.
   - ☐ been filed in Application No. _____.
   - ☐ been filed in reexamination Control No. _____.
   - ☐ been received by the International Bureau in PCT Application No. _____.

   * Certified copies not received: _____.

7. ☒ Note attached Examiner's Amendment.

8. ☐ Note attached Interview Summary (PTO-474).

9. ☐ Other: _____.

cc: Requester (if third party requester)

DETAILED ACTION

Response to Telephone Interview

1. The Patent Owner authorized an Examiner's Amendment, appearing below, which cancels claims 1-4, being the current claims that stand rejected in the Final Office action dated 4/29/2010, and discussed in the Advisory Action dated 8/12/2010.

Summary of Issues

2. Briefly, original claims 1-10 of U.S. Patent Number 5,530,890 (hereafter "the '890 Patent") issued on June 25, 1996. In the after-final amendment dated 6/29/2010, which has been entered, and made of record, the Patent Owner added claims 11-20, whereby new independent claim 11 adds the limitation of "said stack pointer pointing into said first push down stack" to the text of what appears in original claim 1, and new dependent claims 12-20 directly correspond to original dependent claims 2-10. Thus, presently, the current pending claims of the '890 Patent are claims 1-20.

Regarding ***claim 11***, in the examiner's opinion, it would not have been obvious to one of ordinary skill in the art to have the microprocessor additionally comprising the features of "a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit,...said internal bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register, said stack pointer pointing into said first push down stack,..." The closest prior art of record, being the May'948 reference does teach of using a push down stack. However, the May'948 reference does not expressly describe a stack pointer that points "into said first push down stack". With this feature, which was added in the Patent Owner's amendment dated 6/29/2010, claim 11 is deemed patentable.

Any comments considered necessary by PATENT OWNER regarding the above statement must be submitted promptly to avoid processing delays. Such submission by the patent owner should be labeled: "Comments on Statement of Reasons for Patentability and/or Confirmation" and will be placed in the reexamination file.

Underwater Devices Inc. v. Morrison-Knudsen Co., Inc., 717 F.2d 1380, 1389 (Fed. Cir. 1983). "Failure to plead an affirmative defense is a waiver of that defense." *Id.*

Moreover, HTC waited roughly four years before raising this defense in its motion for partial summary judgment. Because both parties have been litigating this case for several years, allowing HTC to raise this affirmative defense for the first time on summary judgment would not only violate Rule 8(c), but also unfairly prejudice TPL. HTC's motion for partial summary judgment should be denied for this reason alone.

B. HTC's Intervening Rights Defense Fails Because the Scope of the Reexamined Claims of the '890 and '336 Patents Are "Substantively Identical" to Their Original Counterparts.

1. Reexamination claim 11 of the '890 patent is substantively identical to original claim 1.

Claim 11 of the reexamined patent is substantially identical in scope to original claim 1 because the only change in language provides explicit clarification of a preexisting implicit limitation. As HTC concedes, "TPL added claim 11 during the reexamination by ***copying the language from claim 1***" and the only difference is the is the addition of the phrase, "said stack pointer pointing to said first push down stack." Motion at 2 (emphasis added). As evidenced by the prosecution history, this amendment was added only for the sake of clarification and did not result in any substantive change.[4]

During reexamination, it was noted that the original specification of the'890 patent clearly described a *stack* pointer pointing into the parameter stack and that the prior art reference at issue clearly described an *instruction* pointer pointing into the *instructions* of a process.[5] However,

---

[4] Indeed, the PTO granted *ex parte* reexamination *inter alia* because "the specific allowable features of claims 1-10 of the '890 Patent in the original prosecution [were] unclear." *See* Declaration of Tanya Wei in support of Defendants' Opposition to HTC's Motion for Partial Summary Judgment ("Wei Decl."), Ex. A (April 8, 2009 Order Granting Request for *Ex Parte* Reexamination of U.S. Patent No. 5,530,890) at 6.

[5] *See, e.g.*, Dkt. No. 458-3 (June 29, 2010 Response to Office Action) at 13 ("Patent Owners respectfully submit that the instruction pointer of May '948(IPTR 50) does not 'point' to the stack registers A, B and C by virtue of being bidirectionally connected thereto or because it loads the contents of A during a general call. Rather, IPTR 50 holds the memory address of the

there were no rejections made to the claims with the prior art of record, nor were any of the cited prior art in the record expressly discussed. Thus, the specific allowable features of claims 1-10 of the '890 Patent in the original prosecution are unclear.

Discussion of Substantial New Question of Patentability

9. First, the examiner notes that MPEP 2240 [R-5] states, in part:

> 37 CFR 1.515. Determination of the request for ex parte reexamination.
>
> (a) Within three months following the filing date of a request for an *ex parte* reexamination, an examiner will consider the request and determine whether or not a substantial new question of patentability **affecting any claim of the patent** is raised by the request and the prior art cited therein, with or without consideration of other patents or printed publications. The examiner 's determination will be based on the claims in effect at the time of the determination, will become a part of the official file of the patent, and will be mailed to the patent owner at the address as provided for in § 1.33(c) and to the person requesting reexamination. [Emphasis added.]

10. With this, with respect to the first proposed SNQ noted above, it is agreed that the consideration of MacGregor raises a substantial new question of patentability as to independent claim 1 of the '890 Patent. The reference of MacGregor appears to teach of a microprocessor having similar architecture as that required in claim 1 of the '890 Patent, being what was noted as allowable over the prior art of record in the original prosecution of the '890 Patent. Particularly, MacGregor is seen as teaching of a microprocessor (MC68020, see Fig. 1 on page 108 and Fig. 2 on page 109) having a main central processing unit having an arithmetic unit (included in "three arithmetic units", see page 101, col. 2), a first push down stack with a top

set the frequency of the devices on the chip, the PVT parameters affect the frequency of those devices. In fact, the use of a PLL is an acknowledgement that PVT factors will affect the components on the chip, because a PLL is used to increase the oscillator frequency if the oscillator begins to slow down or decrease the oscillator frequency if the oscillator begins to speed up.

53. All components on microprocessors are subject to process variations (also referred to as manufacturing or fabrication variations) at the time they are manufactured or fabricated. This is because all transistors on a chip are similarly affected by process variations introduced at the time of fabrication. Those process variations affect the performance of the transistors on the chip throughout the lifetime of the chip. This is recognized in the industry, and a standard practice called "binning" is used to group the chips based on their performance as a result of these process variations, as I explained in my opening expert report.

54. Because the on-chip oscillator in the accused product drives the CPU by generating a clock signal at a particular clock rate or frequency, the CPU's processing frequency will track the clock rate.

55. As I explained in my expert report, PLLs attempt to set the frequency of an on-chip oscillator, but are only able to set that frequency to within a range. This range is referred to as a "dead band," because within the band the PLL is not able to adjust the frequency of the on-chip oscillator. Within the dead band, variations in frequency are due to PVT parameters, and not any control of the PLL circuitry.

Scope of Reexam Claims for '890 and '336 Patents

56. I have also reviewed HTC's Motion for Partial Summary Judgment of (1) Noninfringement of U.S. Patent Nos. 5,530,890 and 5,809,336; and (2) Willful Infringement of U.S. Patent No. 5,530,890. For the reasons explained below and laid out in my Report, I disagree with HTC's basis for noninfringement. HTC's motion is based on a misunderstanding of the differences between an instruction pointer, a stack pointer, a return stack pointer, a first push down stack, and a return push down stack are and their possible functions.

57. In my experience, an instruction pointer (*i.e.*, instruction address register, or

program counter) points to the location in the instruction memory of the next instruction to be fetched and executed. As such, it is under program control (*i.e.*, controlled by the processor) and is not modifiable by the user. Thus, it does not fit the definition of a stack. One of ordinary skill in the art would understand that instructions are kept in the instruction memory, which is randomly accessible, and ***not*** located in a stack. To avoid any potential problems in program execution, any modification of the instructions is forbidden. For example, in U.S. Patent No. 4,758,948 to May cited in the prosecution history of the '890 patent describes a multi-processor which loads a number of registers from a workspace associated with the process being given control as well as an instruction pointer IPTR S 65 that points to the next instruction for that process, not to the stack pointer.

58. The claims of the '890 patent describe two stacks (a first push down stack and a return push down stack) each having its own purpose. The first stack (the first push down stack) is used to store parameters and data that are being operated upon. The second stack (the return push down stack) is used for storing return addresses when the program jumps into subroutine calls. Each stack pointer associated with a particular stack and constitutes an integral part of the stack. Interchanging the stacks (or content of the stacks) is not permitted because that would create an unpredictable and unmanageable situation, which would cause the program to crash. Thus, if the stack pointers of the '890 patent were interchanged, *i.e.*, if the stack pointer did not point into the first push down stack, but instead pointed into the return push down stack, the same undesirable situation would occur. In my opinion, the term "stack pointer" was interpreted in an overly broad manner during the reexamination of the '890 patent by going beyond what a person of ordinary skill in the art would understand to be a stack pointer. Reexamined claim 11 clarified this situation by stating what is obvious to someone of the ordinary skill in the art – that stack pointers can only point to the stack with which they are associated.

59. I also disagree with HTC's basis for noninfringement of the'336 patent because it ignores the original claims, written description, and prosecution history of the '336 patent. For the reasons explained below and laid out in my Report, it is my further opinion that nothing in the

A7125; A7152; A7161-A7163; A7199-A7200
REMOVED DUE TO CONFIDENTIAL MATERIAL

COOLEY LLP
HEIDI L. KEEFE (178960) (hkeefe@cooley.com)
RONALD S. LEMIEUX (120822) (rlemieux@cooley.com)
MARK R. WEINSTEIN (193043) (mweinstein@cooley.com)
KYLE D. CHEN (239501) (kyle.chen@cooley.com)
Five Palo Alto Square, 4th Floor
3000 El Camino Real
Palo Alto, California 94306-2155
Telephone: (650) 843-5000
Facsimile: (650) 857-0663

Attorneys for Plaintiffs
HTC CORPORATION AND HTC AMERICA, INC.

[See signature page for additional counsel]

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION, HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00882 PSG **JOINT REQUEST TO DISMISS ALL CLAIMS RELATING TO U.S. PATENT NO. 5,530,890 UNDER F.R.C.P. 41(a)(2)** **[PROPOSED] ORDER THEREON** The Honorable Paul S. Grewal

WHEREAS plaintiffs HTC Corporation and HTC America, Inc. (collectively "HTC") filed a First Amended Complaint seeking a declaratory judgment that HTC does not infringe any valid and enforceable claim of U.S. Patent No. 5,530,890 (the "'890 patent");

WHEREAS defendants Technology Properties Limited, Patriot Scientific Corporation, and Alliacense Limited (collectively "Defendants") filed an Answer and Counterclaim denying HTC's averment that HTC did not infringe any valid and enforceable claim of the '890 patents,

and asserting a counterclaim of infringement regarding the '890 patent;

WHEREAS the '890 patent was subject to *ex parte* reexamination with a reexamination certificate issuing on March 1, 2011;

WHEREAS on September 17, 2013, the Court issued an order granting-in-part HTC's motion for summary judgment based on the intervening rights doctrine, concluding that "any claims of infringement before the date of the issuance of the reexamination certificate [of the '890 patent] must be precluded" (Dkt. No. 585, at 20:17-18) ("Summary Judgment Order");

WHEREAS the HTC products accused of infringing of the '890 patent did not generate revenue in the United States in 2011 or thereafter;

WHEREAS based on the Summary Judgment Order and the HTC products accused of infringing the '890 patent in the present action, Defendants cannot establish entitlement to damages under any claim of the '890 patent under 35 U.S.C. § 284;

WHEREAS Defendants respectfully believe that the Summary Judgment Order is erroneous with respect to intervening rights on the '890 patent, and reserve their right to seek review by the U.S. Court of Appeals for the Federal Circuit after entry of final judgment in this action;

WHEREAS in order to conserve judicial resources and streamline these proceedings, and without prejudice to the rights of any party to appeal all or part of the Summary Judgment Order or any other order for which an appeal is permissible, the parties respectfully request that the Court order, as follows:

1. Because Defendants cannot establish entitlement to damages in the present action based on the Summary Judgment Order, the Court hereby **DISMISSES** the Fifth Claim for Relief in HTC's First Amended Complaint (seeking a declaration that HTC does not infringe any valid and enforceable claim of the '890 patent), and Count IV of Defendants' Answer and Counterclaim (alleging infringement of the '890 patent), subject to the conditions of this Order.

2. This Order shall not affect any other claim or counterclaim asserted in the present

action, and shall not impair any rights of Defendants or HTC to challenge on appeal any pretrial ruling by the Court for which an appeal is permissible including, without limitation, any challenge to the Summary Judgment Order's application of the intervening rights doctrine.

3. In the event the Federal Circuit reverses the Summary Judgment Order with respect to application of the intervening rights doctrine to the '890 patent, HTC's declaratory judgment claim and Defendants' counterclaim under the '890 patent will be reinstated and proceed unaffected by the dismissal provided in this Order.

4. The provisions of this Order shall be incorporated into any final judgment entered in this action.

Respectfully Requested,

Dated: September 18, 2013

COOLEY LLP

By: */s/ Mark R. Weinstein*

Heidi L. Keefe, Esq.
hkeefe@cooley.com
Ron Lemieux
rlemieux@cooley.com
Mark R. Weinstein, Esq.
mweinstein@cooley.com
Cooley LLP
3000 El Camino Real
Five Palo Alto Square, 4th Floor
Palo Alto, California 94306
Phone: (650) 843-5000
Fax: (650) 857-0663

ATTORNEYS FOR PLAINTIFFS HTC CORPORATION AND HTC AMERICA, INC.

By: */s/ James C. Otteson*

James C. Otteson, State Bar No. 157781
jim@agilityiplaw.com
Thomas T. Carmack, State Bar No. 229324
tom@agilityiplaw.com
Philip W. Marsh, State Bar No. 276383
phil@agilityiplaw.com

Attorneys for Defendants
TECHNOLOGY PROPERTIES LIMITED
and ALLIACENSE LIMITED

KIRBY NOONAN LACE & HOGE

By: */s/ Charles T. Hoge*
Charles T. Hoge, State Bar No. 110696
choge@knlh.com

Attorneys for Defendant
PATRIOT SCIENTIFIC CORPORATION

FILER'S ATTESTATION

Pursuant to Civil Local Rule 5.1(i)(3), the undersigned attests that James C. Otteson and Charles T. Hoge have concurred in the filing of this Joint Request to Dismiss All Claims Relating to U.S. Patent No. 5,530,890 Under F.R.C.P. 41(a)(2).

Dated: September 18, 2013

COOLEY LLP

By: */s/ Mark R. Weinstein*

IT IS SO ORDERED.

Dated: _____

_____
Honorable Paul S. Grewal
United States Magistrate Judge

1172697 v1/HN

COOLEY LLP
HEIDI L. KEEFE (178960) (hkeefe@cooley.com)
RONALD S. LEMIEUX (120822) (rlemieux@cooley.com)
MARK R. WEINSTEIN (193043) (mweinstein@cooley.com)
KYLE D. CHEN (239501) (kyle.chen@cooley.com)
Five Palo Alto Square, 4th Floor
3000 El Camino Real
Palo Alto, California 94306-2155
Telephone: (650) 843-5000
Facsimile: (650) 857-0663

Attorneys for Plaintiffs
HTC CORPORATION AND HTC AMERICA, INC.

[See signature page for additional counsel]

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION, HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00882 PSG **JOINT REQUEST TO DISMISS ALL CLAIMS RELATING TO U.S. PATENT NO. 5,530,890 UNDER F.R.C.P. 41(a)(2)** ~~**[PROPOSED]**~~ **ORDER THEREON** The Honorable Paul S. Grewal

WHEREAS plaintiffs HTC Corporation and HTC America, Inc. (collectively "HTC") filed a First Amended Complaint seeking a declaratory judgment that HTC does not infringe any valid and enforceable claim of U.S. Patent No. 5,530,890 (the "'890 patent");

WHEREAS defendants Technology Properties Limited, Patriot Scientific Corporation, and Alliacense Limited (collectively "Defendants") filed an Answer and Counterclaim denying HTC's averment that HTC did not infringe any valid and enforceable claim of the '890 patents,

and asserting a counterclaim of infringement regarding the '890 patent;

WHEREAS the '890 patent was subject to *ex parte* reexamination with a reexamination certificate issuing on March 1, 2011;

WHEREAS on September 17, 2013, the Court issued an order granting-in-part HTC's motion for summary judgment based on the intervening rights doctrine, concluding that "any claims of infringement before the date of the issuance of the reexamination certificate [of the '890 patent] must be precluded" (Dkt. No. 585, at 20:17-18) ("Summary Judgment Order");

WHEREAS the HTC products accused of infringing of the '890 patent did not generate revenue in the United States in 2011 or thereafter;

WHEREAS based on the Summary Judgment Order and the HTC products accused of infringing the '890 patent in the present action, Defendants cannot establish entitlement to damages under any claim of the '890 patent under 35 U.S.C. § 284;

WHEREAS Defendants respectfully believe that the Summary Judgment Order is erroneous with respect to intervening rights on the '890 patent, and reserve their right to seek review by the U.S. Court of Appeals for the Federal Circuit after entry of final judgment in this action;

WHEREAS in order to conserve judicial resources and streamline these proceedings, and without prejudice to the rights of any party to appeal all or part of the Summary Judgment Order or any other order for which an appeal is permissible, the parties respectfully request that the Court order, as follows:

1. Because Defendants cannot establish entitlement to damages in the present action based on the Summary Judgment Order, the Court hereby **DISMISSES** the Fifth Claim for Relief in HTC's First Amended Complaint (seeking a declaration that HTC does not infringe any valid and enforceable claim of the '890 patent), and Count IV of Defendants' Answer and Counterclaim (alleging infringement of the '890 patent), subject to the conditions of this Order.

2. This Order shall not affect any other claim or counterclaim asserted in the present

action, and shall not impair any rights of Defendants or HTC to challenge on appeal any pretrial ruling by the Court for which an appeal is permissible including, without limitation, any challenge to the Summary Judgment Order's application of the intervening rights doctrine.

3. In the event the Federal Circuit reverses the Summary Judgment Order with respect to application of the intervening rights doctrine to the '890 patent, HTC's declaratory judgment claim and Defendants' counterclaim under the '890 patent will be reinstated and proceed unaffected by the dismissal provided in this Order.

4. The provisions of this Order shall be incorporated into any final judgment entered in this action.

Respectfully Requested,

Dated: September 18, 2013

COOLEY LLP

By: */s/ Mark R. Weinstein*

Heidi L. Keefe, Esq.
hkeefe@cooley.com
Ron Lemieux
rlemieux@cooley.com
Mark R. Weinstein, Esq.
mweinstein@cooley.com
Cooley LLP
3000 El Camino Real
Five Palo Alto Square, 4th Floor
Palo Alto, California 94306
Phone: (650) 843-5000
Fax: (650) 857-0663

ATTORNEYS FOR PLAINTIFFS HTC CORPORATION AND HTC AMERICA, INC.

By: */s/ James C. Otteson*

James C. Otteson, State Bar No. 157781
jim@agilityiplaw.com
Thomas T. Carmack, State Bar No. 229324
tom@agilityiplaw.com
Philip W. Marsh, State Bar No. 276383
phil@agilityiplaw.com

Attorneys for Defendants
TECHNOLOGY PROPERTIES LIMITED
and ALLIACENSE LIMITED

KIRBY NOONAN LACE & HOGE

By: */s/ Charles T. Hoge*
Charles T. Hoge, State Bar No. 110696
choge@knlh.com

Attorneys for Defendant
PATRIOT SCIENTIFIC CORPORATION

FILER'S ATTESTATION

Pursuant to Civil Local Rule 5.1(i)(3), the undersigned attests that James C. Otteson and Charles T. Hoge have concurred in the filing of this Joint Request to Dismiss All Claims Relating to U.S. Patent No. 5,530,890 Under F.R.C.P. 41(a)(2).

Dated: September 18, 2013

COOLEY LLP

By: */s/ Mark R. Weinstein*

IT IS SO ORDERED.

Dated: September 19, 2013

Honorable Paul S. Grewal
United States Magistrate Judge

1172697 v1/HN

COOLEY LLP
HEIDI L. KEEFE (178960) (hkeefe@cooley.com)
MARK R. WEINSTEIN (193043) (mweinstein@cooley.com)
RONALD S. LEMIEUX (120822) (rlemieux@cooley.com)
KYLE D. CHEN (239501) (kyle.chen@cooley.com)
Five Palo Alto Square, 4th Floor
3000 El Camino Real
Palo Alto, California 94306-2155
Telephone: (650) 843-5000
Facsimile: (650) 857-0663

STEPHEN R. SMITH (*pro hac vice*) (stephen.smith@cooley.com)
One Freedom Square
Reston Town Center
11951 Freedom Drive
Reston, VA 20190-5656
Telephone: (703) 456-8000
Facsimile: (703) 456-8100

Attorneys for Plaintiffs
HTC CORPORATION and
HTC AMERICA, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION and HTC AMERICA, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED,

Defendants.

Case No. 5:08-cv-00882 PSG

[Related to Case No. 5:08-CV-00877 PSG]

EMERGENCY MOTION FOR ADDENDUM TO JURY INSTRUCTIONS

Complaint Filed: February 8, 2008
Trial Date: September 23, 2013

Date: September 20, 2013
Time: 9:30 a.m.
Place: Courtroom 5, 4th Floor
Judge: Hon. Paul S. Grewal

NOTICE OF MOTION AND MOTION

PLEASE TAKE NOTICE that Plaintiffs HTC Corporation and HTC America, Inc. (collectively "Plaintiffs") move, on an emergency basis, pursuant to Civil Local Rules 6-3 and 7-11, this Court to add an addendum to the Joint Proposed Jury Instructions to reflect the Court's recent findings in its Order on Summary Judgment of Non-Infringement of the '336 Patent.

This Motion is based on the Memorandum of Points and Authorities set forth below, the accompanying Declaration of Kyle Chen, and such other matters as may be presented at the hearing on Plaintiffs' motion and allowed by the Court.

Plaintiffs notified Defendants' counsel on September 18, 2013, that Plaintiffs intended to file this motion and asked for a prompt response on whether Defendants opposed. Defendants and Plaintiffs were not able to reach a resolution.

MEMORANDUM OF POINTS AND AUTHORITIES

In light of the Court's Order (Dkt. No. 585) granting-in-part HTC's Motion for Summary Judgment of Non-Infringement of the '336 Patent and finding that the patentee disclaimed certain claim scope (*id*. at 11), Plaintiffs HTC Corporation and HTC America, Inc. ask the Court to add the following addendum to the Joint Proposed Jury Instructions (Dkt. No. 513). This addendum would add the following paragraph immediately before current paragraph no. 1 at line 15 of page 44 of those instructions:

> The terms "entire ring oscillator variable speed system clock" (in claims 1 and 11), "entire oscillator" (in claims 6 and 13), and "entire variable speed clock" (in claims 10 and 16) are not satisfied by an accused system that uses any external clock to generate a signal.
>
> An accused product can only infringe the '336 patent if that product contains an on-chip oscillator or clock that is (a) self-generating and (b) does not rely on an input control to determine its frequency.

///

///

///

///

///

Dated: September 18, 2013

Respectfully submitted,

COOLEY LLP
HEIDI L. KEEFE
MARK R. WEINSTEIN
RONALD S. LEMIEUX
STEPHEN R. SMITH
KYLE D. CHEN

By: */s/ Kyle D. Chen*

Attorneys for HTC CORPORATION and HTC AMERICA, INC.

397916

COOLEY LLP
HEIDI L. KEEFE (178960) (hkeefe@cooley.com)
MARK R. WEINSTEIN (193043) (mweinstein@cooley.com)
RONALD S. LEMIEUX (120822) (rlemieux@cooley.com)
KYLE D. CHEN (239501) (kyle.chen@cooley.com)
Five Palo Alto Square, 4th Floor
3000 El Camino Real
Palo Alto, California 94306-2155
Telephone: (650) 843-5000
Facsimile: (650) 857-0663

STEPHEN R. SMITH (*pro hac vice*) (stephen.smith@cooley.com)
One Freedom Square
Reston Town Center
11951 Freedom Drive
Reston, VA 20190-5656
Telephone: (703) 456-8000
Facsimile: (703) 456-8100

Attorneys for Plaintiffs
HTC CORPORATION and
HTC AMERICA, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION and HTC AMERICA, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED,

Defendants.

Case No. 5:08-cv-00882 PSG

[Related to Case No. 5:08-CV-00877 PSG]

REPLY IN SUPPORT OF EMERGENCY MOTION FOR ADDENDUM TO JURY INSTRUCTIONS

Complaint Filed: February 8, 2008
Trial Date: September 23, 2013

Date: September 20, 2013
Time: 9:30 a.m.
Place: Courtroom 5, 4th Floor
Judge: Hon. Paul S. Grewal

To assist the Court in locating the intrinsic records of the '336 patent when considering HTC's Emergency Motion for Addendum to Jury Instructions (Dkt. 590), the following citations to the docket are brought to the Court's attention:

1. **Regarding the Magar Reference:**

"[T]he Magar microprocessor clock is **frequency controlled** by a crystal which is also external to the microprocessor. … The Magar microprocessor in no way contemplates a variable speed clock as claimed." Dkt. No. 457-13, Ex. 6 to Chen Decl. iso MSJ, 7/7/1997 Amendment at 3-4 (TPL853_00002427-28) (emphasis added).

"The Magar teaching is well known in the art as a conventional **crystal controlled oscillator**. It is specifically distinguished from the instant case in that it is **both fixed frequency (being crystal based) and requires an external crystal or external frequency generator**." Dkt. No. 457-14, Ex. 7 to Chen Decl. iso MSJ, 2/10/1998 Amendment at 5 (TPL853_00002403) (emphasis added).

"**[W]hile most of Magar's clock (generator) circuitry is on the IC**, the entire oscillator, which because it requires an external crystal, is not." *Id.* at 4 (TPL853_00002402) (emphasis added).

2. **Regarding the Sheets Reference:**

"Even if the examiner is correct that **the variable clock in Sheets is in the same integrated circuit as the microprocessor of system 100**, that still does not give the claimed subject matter. In Sheets, **a command input is required to change the clock speed**." Dkt. No. 457-17, Ex. 10 to Chen Decl. iso MSJ, 1/8/1997 Amendment at 4) (TPL853_00002449) (emphasis added).

///

///

Dated: September 20, 2013

Respectfully submitted,

COOLEY LLP
HEIDI L. KEEFE
MARK R. WEINSTEIN
RONALD S. LEMIEUX
STEPHEN R. SMITH
KYLE D. CHEN

By: */s/ Kyle D. Chen*

Attorneys for HTC CORPORATION and HTC AMERICA, INC.

1173380 v1/HN

OBJECTIVE PRONG.

WE'RE NOT DISPUTING THAT THE DECISION OF A PRIOR TRIBUNAL CAN BE RELEVANT, BUT THE POINT IS IT'S NOT IN THIS CASE BECAUSE OF THE DIFFERENT CLAIM CONSTRUCTION. THE CONSTRUCTION OF THE ENTIRE LIMITATION AS ONE EXAMPLE CERTAINLY IS DIFFERENT THAN IN THIS CASE.

AND I THINK BECAUSE WE NOW HAVE AN I.D. THAT'S SUBJECT, POTENTIALLY SUBJECT TO DE NOVO REVIEW, THE FACT OF THE I.D. MAKES THIS MORE CONFUSING TO THE JURY RATHER THAN LESS CONFUSING.

THE COURT: ALL RIGHT. MR. LEMIEUX, DO YOU WANT TO OFFER ANY LAST COMMENTS?

MR. LEMIEUX: WELL, ON CLAIM CONSTRUCTION, YOUR HONOR, I WOULD POINT OUT THAT ITS TERM, THE VARYING TERM, THERE IS NO DIFFERENCE BETWEEN WHAT THIS COURT IS GOING TO USE AND WHAT WAS USED IN THE ITC.

SO, YES, IN A THEORETICAL SENSE, THE FACT THAT THERE IS ANOTHER TRIBUNAL OUT THERE THAT HAS FOUND NO INFRINGEMENT AND THE JURY CAN SAY, "HM, THEY FOUND NO INFRINGEMENT, SO WHY SHOULD WE?"

BUT WE SHOULDN'T BE FORCED TO PUT ALL OF OUR EGGS IN ONE BASKET, EITHER, AND SAY "YOU SHOULD BELIEVE US ON NON-INFRINGEMENT BECAUSE THERE IS OBJECTIVE EVIDENCE THAT OUR POSITION," AND THAT'S ALL THIS IS GOING TO, JUST FOR WILLFULNESS, "OUR POSITION WAS NOT UNREASONABLE, AND THIS IS

DIRECT EVIDENCE, OBJECTIVE EVIDENCE OF THE REASONABLENESS OF OUR POSITION."

AND WITHOUT BEING ABLE TO PUT THAT SAME EVIDENCE IN THERE, WE'RE BASICALLY BEING PRECLUDED FROM BEING ABLE TO ATTACK THAT PART OF THEIR CHARGE.

THE COURT: ALL RIGHT. WELL, LET ME MAKE THIS ONE EASY. I'M GOING TO DENY THE MOTION FOR RECONSIDERATION. I'M PERSUADED MY ORIGINAL REASONING WAS CORRECT.

OBVIOUSLY THERE WILL BE OPPORTUNITIES TO ADDRESS THAT IN FURTHER TRIBUNALS.

LET'S MOVE ON TO THE NEXT MOTION.

MR. LEMIEUX: ABSOLUTELY, YOUR HONOR. I'M SURE YOU CAN APPRECIATE OUR NEED TO MAKE A RECORD ON THAT PARTICULAR ISSUE.

THE COURT: I APPRECIATE THAT.

GO AHEAD.

MR. LEMIEUX: ON THE NEXT ONE, YOUR HONOR, THIS IS REALLY -- THEY'RE THE ONES WHO ARE TRYING TO REARGUE EVERYTHING WITH REGARD TO CLAIM CONSTRUCTION FROM THIS COURT.

IN THE SUMMARY JUDGMENT MOTIONS, WE ASKED THIS COURT TO MAKE CERTAIN CLAIM CONSTRUCTIONS THAT HAD NOT BEEN REACHED YET IN THIS CASE, AND THE COURT, IN CONSIDERING BOTH PARTIES' ANALYSIS OF THESE ISSUES, DID REACH CERTAIN CONSIDERATIONS.

THEY KEEP TRYING TO BRING UP THIS ISSUE THAT WE'RE TALKING ABOUT FREQUENCY, WHICH IS NOT THE SAME AS GENERATE, AND WE

SHOULD REALLY BE CHIDED FOR MAKING THAT ARGUMENT.

THE FACT OF THE MATTER IS, IN THE DISCLAIMERS THAT THE COURT ITSELF CITED AND FOUND AS CLEAR DISCLAIMERS, THE LANGUAGE THAT'S IN THE PROSECUTION HISTORY IS "THE MAGAR MICROPROCESSOR CLOCK IS FREQUENCY CONTROLLED BY A CRYSTAL WHICH IS ALSO EXTERNAL TO THE MICROPROCESSOR. THE MAGAR MICROPROCESSOR IN NO WAY CONTEMPLATES A VARIABLE SPEED CLOCK AS CLAIMED."

IT ALSO GOES ON TO STATE, "THE MAGAR TEACHING IS SPECIFICALLY DISTINGUISHED FROM THE INSTANT CASE IN THAT IT IS BOTH FIXED FREQUENCY BEING CRYSTAL-BASED AND REQUIRES AN EXTERNAL CRYSTAL OR EXTERNAL FREQUENCY GENERATOR."

NOW, THE COURT LOOKED AT THAT -- WE ARGUED THIS EXTENSIVELY IN THE SUMMARY JUDGMENT MOTION -- AND FOUND THERE WAS A DISCLAIMER AND FOUND THAT THERE WAS AN ISSUE OF FACT AS TO WHETHER OR NOT, GIVEN ALL OF THAT, THERE WAS THIS FREE RUNNING OSCILLATOR THAT DIDN'T RELY ON ANY EXTERNAL CONTROL SIGNALS.

WE UNDERSTAND THE ISSUE OF FACT THAT THE COURT HAS IDENTIFIED HERE.

BUT IN TERMS OF FOLLOWING AND GIVING GUIDANCE TO THE JURY HERE IN TERMS OF CLAIM CONSTRUCTION AS TO HOW THEY'RE TO EVALUATE THIS EVIDENCE, ALL WE DID WAS SIMPLY TAKE THE COURT'S TERMINOLOGY AND TRY TO FASHION THAT INTO THE JURY INSTRUCTION THEN AS PART OF THE CLAIM CONSTRUCTION CHARGE THAT THE COURT WILL GIVE THE JURY.

THE COURT: SO MR. LEMIEUX, I TAKE IT YOUR CONCERN IS

LESS WITH THE PARTICULAR VERBIAGE I ADOPT TO EXPRESS THAT OR MAKE THAT EXPLANATION TO THE JURY. YOU JUST WANT THE JURY TO UNDERSTAND, AS A MATTER OF LAW, THAT THE TERM ONLY HAS THAT GIVEN SCOPE?

MR. LEMIEUX: THAT'S RIGHT.

THE COURT: OKAY.

MR. LEMIEUX: THIS WAS PART OF -- THIS WAS PART OF THE MOTION, YOUR HONOR. SO YOU FOUND ON THAT, YOU JUST FOUND ANOTHER ISSUE OF FACT THAT PRECLUDED YOU FROM GRANTING SUMMARY JUDGMENT.

BUT THE CONSTRUCTION JUST SAYS THE COURT'S GOING TO GIVE AN INSTRUCTION TO THE JURY ON CLAIM CONSTRUCTION AND OTHER ISSUES.

WE BELIEVE THIS IS NECESSARY AS WELL SO THAT THEY UNDERSTAND AND CAN PUT INTO CONTEXT THE EVIDENCE THEY'RE GOING TO HEAR.

THE COURT: AND AS I RECALL, YOU ALL PRESENTED THIS ISSUE IN THE FORM OF A SUMMARY JUDGMENT MOTION AFTER YOU TALKED AND AGREED THAT RATHER THAN BREAKING THIS UP INTO TWO MOTIONS, A CLAIM CONSTRUCTION MOTION, OR FURTHER CLAIM CONSTRUCTION MOTION, AND ANY OTHER, YOU JUST DECIDED IT WOULD BE MORE EFFICIENT.

MR. LEMIEUX: THAT'S RIGHT. AS PART OF THE SUMMARY JUDGMENT, YOU WOULDN'T REQUIRE THE COURT TO ENGAGE IN A CERTAIN AMOUNT OF CLAIM CONSTRUCTION TO BE ABLE TO DO IT, AND THAT'S WHY THEY WERE BOTH BROUGHT IN THE SAME MOTIONS.

THE COURT: ALL RIGHT.

MR. OTTENSON, YOU'RE UP.

MR. OTTESON: YOUR HONOR, I GUESS I'M A LITTLE CONFUSED ABOUT WHERE WE'RE AT. WE HAVE A CLAIM CONSTRUCTION --

THE COURT: DAY BEFORE TRIAL, U.S. DISTRICT COURT, SAN JOSE, CALIFORNIA.

(LAUGHTER.)

MR. OTTESON: UNITED STATES OF AMERICA.

THE COURT: THAT'S RIGHT.

MR. OTTESON: PLANET EARTH.

OKAY. WE HAVE A CLAIM CONSTRUCTION AND THE CLAIM CONSTRUCTION IS THAT THE -- AN ENTIRE OSCILLATOR IS AN OSCILLATOR THAT IS ENTIRELY ON THE SAME SEMICONDUCTOR SUBSTRATE AS A CPU.

NOW, WHAT THEY'RE TRYING TO DO WITH THE COURT'S ORDER IS, I THINK, MAKE THIS VERY CONFUSING FOR THE JURY AND THEY WANT TO -- THEY WANT TO INCORPORATE INTO JURY INSTRUCTIONS THIS VERY SERIOUS AMBIGUITY AND TRY TO CONFUSE AGAIN THE ISSUES OF GENERATING A CLOCK SIGNAL AND REGULATING OR ADJUSTING THE FREQUENCY OF A CLOCK SIGNAL AND THEY'RE TRYING TO EQUATE THE TWO AND CONFUSE THEM.

NOW, MAGAR AND SHEETS SIMPLY DON'T SUPPORT THAT. YOU KNOW, THEY KEEP RAISING MAGAR. THE EXTERNAL CRYSTAL IN MAGAR -- AND I ACTUALLY HAVE SOME SLIDES AND I KNOW THAT YOU HAVE, YOU HAVE PEOPLE HERE AND SO, YOU KNOW, I'M ASSUMING THAT YOU WON'T

INDULGE ME IN SHOWING YOU THESE -- BUT IF YOU LOOK AT THE MAGAR REFERENCE, FIGURE 2, 2A, YOU CAN SEE THE X1 AND X2 TERMINALS THAT ARE CONNECTED TO AN EXTERNAL OSCILLATOR. THAT IS WHAT PROVIDES THE CPU CLOCK. OKAY? THAT IS NOT THE INVENTION.

HOWEVER, IF YOU LOOK AT FIGURE 17 OF THE '336 PATENT, YOU CAN SEE OVER ON THE RIGHT THERE'S AN EXTERNAL OSCILLATOR THAT PROVIDES A CLOCK SIGNAL TO THE I/O INTERFACE, AND THAT'S DECOUPLED FROM THE ON-CHIP RING OSCILLATOR. SO IT'S VERY DIFFERENT.

WHAT WAS -- WHAT WAS DISCLAIMED WITH RESPECT TO MAGAR WAS THE USE OF AN EXTERNAL CRYSTAL TO GENERATE THE CLOCK SIGNAL FOR THE CPU.

THE COURT: AND THAT STATEMENT IS REMARKABLY CONSISTENT WITH WHAT I SAID ON PAGE 11 OF MY ORDER, SO WHAT WOULD BE THE PROBLEM, IF YOU AND I TEND TO AGREE WITH THAT POINT, WITH LETTING THE JURY IN ON THAT INSIGHT?

MR. OTTESON: WELL, I GUESS I'M A LITTLE CONCERNED HERE. THERE'S A DIFFERENCE BETWEEN DETERMINING FREQUENCY AND GENERATING A CLOCK SIGNAL, AND IT'S A FUNDAMENTAL DIFFERENCE.

A CLOCK SIGNAL IS A SERIES OF PULSES OVER TIME, AS YOU KNOW.

NOW, THE FREQUENCY OF THAT CLOCK SIGNAL CAN CHANGE DEPENDING ON CONDITIONS, AND THAT'S WHAT THE '336 PATENT SAYS.

THE FREQUENCY IS A CHARACTERISTIC OF THE CLOCK SIGNAL. IT IS NOT THE SAME THING AS THE CLOCK SIGNAL.

SO LET ME BE AS CLEAR AS I CAN ON THIS. IF THE JURY IS INSTRUCTED THAT AN EXTERNAL CLOCK, WHICH IS USED AS A REFERENCE FREQUENCY FOR A PLL -- IT IS NOT PROVIDING THE CLOCK SIGNAL FOR THE CPU, IT'S A REFERENCE FREQUENCY -- THAT CLOCK SIGNAL IS BEING PROVIDED BY A RING OSCILLATOR IN THE PLL.

BUT IF THE COURT INSTRUCTS THE JURY THAT AN EXTERNAL CRYSTAL CAN'T BE USED AS A REFERENCE TO HELP REGULATE OR ADJUST OR DETERMINE THE FREQUENCY, THEN WE SHOULD HAVE JUDGMENT TAKEN AGAINST US, OKAY? BECAUSE WE ACKNOWLEDGE THAT ALL OF THE ACCUSED PRODUCTS HAVE PLL'S THAT HAVE CIRCUITRY THAT REGULATES OR ADJUSTS THE FREQUENCY OF THE CLOCK SIGNAL. THEY DO NOT GENERATE THE CLOCK SIGNAL.

THE CLOCK SIGNAL, WHICH IS A HUNDRED TIMES FASTER -- I MEAN, I'M NOT KIDDING. IT'S TWO ORDERS OF MAGNITUDE FASTER THAN THAT REFERENCE -- THAT EXTERNAL REFERENCE CRYSTAL, THE CLOCK SIGNAL IS GENERATED BY THE RING OSCILLATOR IN THE PLL.

AND SO IF WE CAN'T -- IF THEY DON'T INFRINGE AND THE COURT INSTRUCTS THE JURY THAT THEY DON'T INFRINGE BECAUSE AN EXTERNAL CRYSTAL IS USED TO DETERMINE THE FREQUENCY OR SET THE FREQUENCY OR CONTROL THE FREQUENCY --

THE COURT: THEN WE SHOULD ALL JUST GO HOME AND YOU SHOULD GO TO WASHINGTON RIGHT AWAY, RIGHT?

MR. OTTESON: THAT'S WHAT I'M SAYING.

THE COURT: YEAH, I GET THAT. SO TELL ME --

MR. OTTESON: WE SHOULD HAVE JUDGMENT TAKEN AGAINST

US AND THEN WE CAN TAKE OUR APPEAL. AND THAT -- YOU KNOW, OBVIOUSLY I DON'T WANT THAT, BUT I JUST DON'T WANT TO WASTE THE COURT'S TIME OR THE PARTIES' TIME.

THE COURT: NO, I UNDERSTAND. SO IF I WERE SIMPLY TO INSTRUCT THE JURY THAT THE DISPUTED LIMITATIONS EXCLUDE ANY EXTERNAL CLOCK THAT IS USED TO GENERATE A SIGNAL, WOULD YOU HAVE ANY PROBLEM WITH THAT?

MR. OTTESON: WELL, USED TO GENERATE THE CLOCK SIGNAL FOR THE CPU.

THE COURT: YEAH.

MR. OTTESON: BECAUSE THAT WAS A DISCLAIMER IN MAGAR. IT WASN'T -- MAGAR HAD NOTHING TO DO WITH PLL'S. IT HAD NOTHING TO DO WITH USING THAT EXTERNAL CLOCK AS A REFERENCE. THAT EXTERNAL CLOCK ACTUALLY GENERATED THE CLOCK SIGNAL FOR THE CPU.

BUT MAGAR HAD NOTHING TO DO WITH THE DISCLAIMER THAT THE EXTERNAL CLOCK WAS GOING TO BE USED TO -- AS A REFERENCE IN A PLL TO ADJUST THE FREQUENCY. IT WAS ACTUALLY GENERATING THE CLOCK SIGNAL.

SO IF YOUR HONOR WANTED TO CONSTRUCT OR CONSTRUE "ENTIRE OSCILLATOR" SO THAT YOU CAN'T USE AN EXTERNAL REFERENCE CRYSTAL TO GENERATE THE CPU'S CLOCK SIGNAL, THAT'S ENTIRELY DIFFERENT FROM SAYING THAT YOU CAN'T USE THE EXTERNAL CRYSTAL TO ADJUST OR MANIPULATE THE FREQUENCY OF THE CLOCK SIGNAL.

THE COURT: SO IT EXCLUDES THE EXTERNAL CLOCK YOU USE

TO GENERATE THE SIGNAL. NOTHING MORE, NOTHING LESS?

MR. OTTESON: RIGHT, RIGHT.

THE COURT: SO YOU DON'T HAVE A PROBLEM WITH THAT?

MR. OTTESON: NO, BECAUSE WE WIN. WE WIN ON THAT. I MEAN, WE -- WE CAN SHOW THE JURY THAT THE CLOCK SIGNAL THAT'S USED TO CLOCK THE CPU IS GENERATED BY THE RING OSCILLATOR.

AGAIN, I DON'T THINK -- I DON'T REALLY THINK THAT'S A -- YEAH, I MEAN --

THE COURT: OKAY. LET ME STOP YOU THERE.

AND I'LL ASK YOU, MR. LEMIEUX, IF I INSTRUCTED THE JURY THAT ENTIRE OSCILLATOR EXCLUDES ANY EXTERNAL CLOCK USED TO GENERATE A SIGNAL, ARE WE DONE HERE? WE'RE NOT DONE, BUT ARE WE DONE WITH THIS ISSUE?

MR. LEMIEUX: WE WOULDN'T BE, YOUR HONOR, BECAUSE THE DISCLAIMER GOES BEYOND THAT. THE DISCLAIMER DOES SPECIFICALLY MENTION FREQUENCY, AND AS I POINTED OUT IN TWO EARLIER POINTS, AND I CAN SHOW -- HERE'S THE MAGAR REFERENCE, YOUR HONOR. HERE'S THE EXTERNAL CRYSTAL AND IT'S GOING INTO SOMETHING CALLED A CLOCK GENERATOR.

IT'S NOT GENERATING THE SIGNAL AS MR. OTTESON JUST TRIED TO POINT OUT TO YOU. IT'S ACTUALLY PROVIDING A REFERENCE SIGNAL TO A CLOCK GENERATOR WHO'S PROVIDING THAT SIGNAL THEN FOR THE REST OF THE BUS.

THE LANGUAGE IN THE PROSECUTION HISTORY IS VERY CLEAR. THEY SPECIFICALLY DISCLAIM ON FREQUENCY, AS WELL AS ON THIS

IDEA OF GENERATING CLOCK SIGNAL.

AND THE ABILITY TO USE EXTERNAL CONTROLS TO CONTROL THE FREQUENCY, I AGREE WITH MR. OTTESON, WE SHOULD WIN. BASED ON THESE CLEAR DISCLAIMERS, WE SHOULD JUST TAKE THIS TO THE FEDERAL CIRCUIT BECAUSE BY THESE DISCLAIMERS WE SHOULD WIN AND WE SHOULD JUST GO TO WASHINGTON. THAT PART OF IT I DO AGREE WITH.

MR. OTTESON: THE PROBLEM I GUESS WE HAVE --

IF YOU DON'T MIND, I'LL JUST TAKE THIS FOR A SECOND.

MR. LEMIEUX: SURE.

MR. OTTESON: -- IS THAT REALLY AN UNDERSTANDING OF MAGAR.

NOW, WE TALKED ABOUT THIS EXTENSIVELY IN OUR BRIEFING AND HE'S SAYING, WELL, THIS GOES INTO A CLOCK GEN CIRCUIT AND THAT GENERATES THE CLOCK FOR THE SIGNAL. FALSE. THAT IS NOT TRUE.

NOW, IF YOU -- AND I HAVE SLIDES AND WE CAN LOOK AT THIS, BUT I CAN POINT TO YOU IN MAGAR, ALL THIS CLOCK GENERATOR BOX HAS IN IT IS DIVIDERS, OKAY? SO THE CLOCK, THE CLOCK THAT IS BEING GENERATED FOR THE CPU COMES FROM THAT CRYSTAL AND IT'S JUST DIVIDED DOWN.

SO THAT'S THE PROBLEM I HAVE, YOU KNOW, WITH OUR, YOU KNOW, THE MANY REPEATED ARGUMENTS WE'VE HAD ABOUT MAGAR IS HOW THEY MISCONSTRUE IT. THAT CLOCK GEN BOX IS A MISNOMER. IT IS NOT GENERATING A CLOCK SIGNAL.

IT'S GOT -- AND THERE'S -- IN THE SPECIFICATION -- IN FACT,

I CAN TELL YOU EXACTLY WHERE IT IS IN THE MAGAR SPECIFICATION. IT'S COLUMN 15, AND IT'S THE PARAGRAPH RIGHT UNDER THE LABEL "SYSTEM TIMING" IN COLUMN 15 OF THE MAGAR REFERENCE. IT SAYS, "THE CHIP INCLUDES A CLOCK GENERATOR 17 WHICH HAS TWO EXTERNAL PINS X1 AND X2 TO WHICH A CRYSTAL OR AN EXTERNAL GENERATOR IS CONNECTED. THE BASIC CLOCK, CRYSTAL FREQUENCY IS UP TO 20 AND IS REPRESENTED BY A CLOCK 0, FIGURE 3A," ET CETERA.

"THE CLOCK 0 HAS A PERIOD OF 50 NANOSECONDS MINIMUM AND IS USED TO GENERATE FOUR QUARTER CYCLE CLOCKS, Q1, Q2, Q3, AND Q4."

THAT CLOCK GEN BOX IS JUST DIVIDERS TO CREATE QUARTER CYCLE CLOCKS.

BUT THE CLOCK SIGNAL ITSELF, THE OSCILLATING SIGNAL, IS DRIVEN BY, CREATED BY, GENERATED BY THE EXTERNAL CRYSTAL. THAT'S COMPLETELY DIFFERENT THAN THE '336 INVENTION.

IN FACT, THIS -- YOU KNOW, FIGURE 2A OF MAGAR, THAT IS THE PRIOR ART. THAT IS THE PRIOR ART. THAT'S AN EXTERNAL CRYSTAL THAT IS DRIVING THE CPU CLOCK.

AND THAT'S WHY I DON'T THINK IT'S FAIR AND IT'S NOT RIGHT AND IT'S A MISCHARACTERIZATION OF THE FILE HISTORY TO SAY THAT YOU CAN'T USE -- YOU CAN'T USE AN EXTERNAL CRYSTAL FOR ANY PURPOSE AT ALL, LIKE ADJUSTING A CLOCK SIGNAL LIKE YOU WOULD USE THAT AS AN EXTERNAL REFERENCE IN A PLL. IT'S VERY DIFFERENT, YOUR HONOR. IT'S VERY DIFFERENT.

THE COURT: MR. LEMIEUX, YOU WANT TO RESPOND? AND

THEN I'LL MOVE ON.

MR. LEMIEUX: CERTAINLY, YOUR HONOR.

WE'RE TALKING HERE ABOUT DISCLAIMER FOR CLAIM SCOPE. THE DISCLAIMER IS GOVERNED BY THE WORDS ACTUALLY USED BY THE PATENT APPLICANT, AND THE WORDS USED BY THE PATENT APPLICANT ARE "THE MAGAR MICROPROCESSOR CLOCK IS FREQUENCY CONTROLLED BY A CRYSTAL," FREQUENCY CONTROLLED BY A CRYSTAL, "WHICH IS ALSO EXTERNAL TO THE MICROPROCESSORS." OKAY? SO IT IS FREQUENCY CONTROLLED BY A CRYSTAL EXTERNAL TO THE MICROPROCESSOR.

THE MAGAR MICROPROCESSOR CONTEMPLATES -- IN NO WAY CONTEMPLATES THE VARIABLE SPEED CLOCK AS CLAIMED. OKAY.

"THE MAGAR TEACHING IS SPECIFICALLY DISTINGUISHED FROM THE INSTANT CASE IN THAT IT IS BOTH FIXED FREQUENCY BEING CRYSTAL-BASED," AGAIN, THE CRYSTAL IS CONTROLLING THE FREQUENCY, "AND REQUIRES AN EXTERNAL CRYSTAL OR EXTERNAL FREQUENCY GENERATOR."

THESE ARE THE WORDS OF THE PATENT APPLICANT ITSELF WHEN IT'S SEEKING THE ISSUANCE OF THIS PATENT.

IT ALSO WENT ON TO SAY "IN SHEETS, A COMMAND INPUT IS REQUIRED TO CHANGE THE CLOCK SPEED," AND THAT'S HOW THEY DIFFERENTIATE SHEETS.

AGAIN, IT'S THE CRYSTAL BEING USED TO CONTROL THE FREQUENCY. IT'S NOT JUST THIS IDEA OF GENERATION. IT'S ALSO THE IDEA OF THE EXTERNAL CRYSTAL BEING USED TO CONTROL THE FREQUENCY OF THE CLOCK GENERATOR.

THAT HAS TO BE PART OF THE CONSTRUCTION GIVEN TO THE JURY. IT IS -- HE JUST WANTS TO GIVE PART, WHAT HE BELIEVES TO BE PART OF THE CONSTRUCTION BECAUSE HE THINKS HE CAN THEN EDGE HIS WAY AROUND THAT.

BUT THAT'S NOT WHAT THE PATENT APPLICANT SAID IN ITS DISCLAIMERS TO THE PTO.

THE COURT: ALL RIGHT.

MR. OTTESON: AND WHAT THE APPLICANT SAID WAS IN THE CONTEXT OF THE PRIOR ART.

JUDGE, YOU KNOW THAT A DISCLAIMER HAS TO BE A CLEAR DISAVOWAL. THAT HAS TO BE TAKEN IN THE CONTEXT OF WHAT THE PRIOR ART REFERENCE IS, WHICH IS EXACTLY THE KIND OF PRIOR ART THAT WAS DESCRIBED IN THE '336 PATENT ITSELF.

AND YOU EVEN HAVE AN EXAMPLE OF THAT ON THE RIGHT SIDE OF FIGURE 17 OF '336 WHERE YOU HAVE AN EXTERNAL CRYSTAL THAT'S DRIVING AND PROVIDING A FIXED FREQUENCY CLOCK SIGNAL FOR THE I/O INTERFACE.

BUT THERE'S NOTHING IN MAGAR ABOUT AN ON-CHIP OSCILLATOR. THERE'S NOTHING IN SHEETS ABOUT AN ON-CHIP OSCILLATOR. THEY'RE VERY DIFFERENT.

THE COURT: ALL RIGHT. WELL, I GUESS I HAVE MORE READING TO DO OVER LUNCH. I'M GOING TO READ MAGAR AND SHEETS. I'LL GET YOU AN ORDER OUT THIS AFTERNOON. WE'LL GET THIS DECIDED.

MR. LEMIEUX: SURE. AND I'LL POINT OUT THAT THIS CAN

BE FOUND IN TPL 85300002426 AND IN 2403, THESE SPECIFIC REFERENCES MADE BY THE APPLICANT DURING THE PROSECUTION HISTORY.

SO I AGREE, IT IS AN ISSUE OF CLAIM DISCLAIMER HERE, YOUR HONOR. YOUR HONOR FOUND A DISCLAIMER AND IT'S A QUESTION OF HOW FAR DOES IT GO. THIS IS THE EXACT LANGUAGE USED BY THE APPLICANT.

THE COURT: ALL RIGHT. I HAVE IT. I'LL TAKE IT FROM HERE AND GET AN ORDER OUT SHORTLY.

MR. OTTESON: THANK YOU, YOUR HONOR.

MR. LEMIEUX: THANK YOU, YOUR HONOR.

THE COURT: IF I COULD, BEFORE I LET YOU ALL GO, I DID WANT TO JUST REVIEW SOME HOUSEKEEPING MATTERS FOR MONDAY'S PROCEEDINGS.

WE ARE NOW DOWN TO TWO PARTIES AND SO I WANTED TO REVISIT OR RETURN TO THE QUESTION OF WHAT HOURS ARE APPROPRIATE FOR THE TRIAL AND WHAT WITNESSES AND SO FORTH ARE GOING TO CONSUME WHATEVER BUDGET IS SET.

I WILL START THE BIDDING BY OFFERING MY SUGGESTION AS TO WHAT HOUR LIMITS ARE APPROPRIATE NOW THAT WE HAVE TWO PARTIES RATHER THAN THREE.

IT OCCURS TO ME, AS I LOOK AT THE RECORD HERE, THAT THIS CASE COULD BE TRIED AS FOLLOWS: ONE HOUR EACH FOR OPENING STATEMENTS; ONE HOUR EACH FOR CLOSING ARGUMENTS; AND 15 HOURS EACH FOR DIRECT AND CROSS-EXAMINATION IN TOTO. THAT'S MY BEST

Volume II of II, Pages A7451 to A9317

Nos. 2014-1076, -1317

United States Court of Appeals for the Federal Circuit

HTC CORPORATION and HTC AMERICA, INC.,

Plaintiffs-Cross-Appellants,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED,

Defendants-Appellants.

Appeals from the United States District Court for the Northern District of California in Case No. 5:08-cv-00882-PSG, United States Magistrate Judge Paul S. Grewal

CORRECTED NON-CONFIDENTIAL JOINT APPENDIX

James C. Otteson
Thomas T. Carmack
Philip W. Marsh
AGILITY IP LAW, LLP
149 Commonwealth Dr.
Menlo Park, CA 94025
(650) 227-4800

Attorneys for Defendants-Appellants Technology Properties Limited, Patriot Scientific Corporation and Alliacense Limited

Heidi L. Keefe
Mark R. Weinstein
Kyle D. Chen
COOLEY LLP
3175 Hanover Street
Palo Alto, CA 94306-2155
(650) 843-5000

Stephen R. Smith
COOLEY LLP
One Freedom Square
Reston Town Center
11951 Freedom Drive
Reston, VA 20190-5656
(703) 456-8000

Attorneys for Plaintiffs-Cross-Appellants HTC Corporation and HTC America, Inc.

October 8, 2014

TABLE OF CONTENTS

CONFIDENTIAL MATERIAL OMITTED

Pages A7125, A7152, A7161-A7163, and A7199-A7200 have been omitted from this non-confidential version of the Joint Appendix. The material on those pages was designated by HTC as confidential under the protective order dated April 21, 2010. They contain the damages expert's opinion based on confidential financial information.

Pages A9041, and A9054 have been omitted from this non-confidential version of the Joint Appendix. The material on those pages was designated by HTC as confidential under the protective order dated April 21, 2010. They contain HTC's confidential technical information.

Pages A9043-A9045, A9050-A9052, A9065-A9066, A9072-A9073, and A9316-A9317 have been omitted from this non-confidential version of the Joint Appendix. The material on those pages was designated by Qualcomm as confidential under the protective orders dated April 21, 2010 and May 17, 2011. They contain Qualcomm's confidential technical information.

Pages A9056-A9058, and A9068-A9069 have been omitted from this non-confidential version of the Joint Appendix. The material on those pages was designated by Texas Instruments as confidential under the protective order dated April 21, 2010. They contain Texas Instruments' confidential technical information.

SOME KIND OF PROCESSING ON A FUNCTION, WHEN IT SENDS IT OFF, THEN IT WANTS TO SEND IT OFF THE CHIP TO EXTERNAL MEMORY, THAT'S TRUE.

BUT MOST MICROPROCESSORS ACTUALLY ALSO HAVE MEMORY ON THE CHIP, SO IF YOU LOOK AT THIS ONE IN PARTICULAR, THESE AREAS THAT LOOK VERY UNIFORM ARE VERY LIKELY MEMORY THAT'S ON THE CHIP.

SO THE MICROPROCESSOR HAS DIFFERENT PARTS. IT'S GOT, YOU KNOW, THESE MEMORY MODULES, IT'S GOT THE INPUT/OUTPUT INTERFACE WE TALKED ABOUT FOR GETTING STUFF ON AND OFF THE CHIP.

AND THEN THE MOST IMPORTANT PART OF THE MICROPROCESSOR, THE BRAIN OF THE MICROPROCESSOR IF YOU WILL, IS CALLED THE CPU OR A CENTRAL PROCESSING UNIT, AND I DON'T KNOW EXACTLY WHERE THAT IS, BUT IT'S SOMEWHERE IN HERE, AND IT DOES ALL OF THE EXECUTIONS OF INSTRUCTIONS AND MANIPULATION OF DATA.

SO JUST LIKE THE MICROPROCESSOR CHIP IS THE BRAIN OF YOUR PHONE, THE CPU, OR THE CENTRAL PROCESSING UNIT INSIDE OF THE MICROPROCESSOR IS THE BRAIN OF THE MICROPROCESSOR.

SO IT DOES ALL KINDS OF FUNCTIONS THAT HELP YOU DO THE THINGS THAT YOU WANT TO DO WITH YOUR PHONE, LIKE WE TALKED ABOUT, USING THE INTERNET BROWSER, MAKE PHONE CALLS, E-MAIL, TEXTING, PLAY GAMES, ET CETERA.

AND WHAT'S REALLY IMPORTANT TO UNDERSTAND ABOUT HOW THE MICROPROCESSOR DOES ALL OF THOSE THINGS IS THAT TIMING IS CRITICAL BECAUSE THE MICROPROCESSOR AND THE DIFFERENT PARTS OF

IT HAVE TO KNOW WHEN THINGS ARE GOING TO BE DONE AND WHAT ORDER THEY'RE DONE IN.

SO IN ORDER TO ACHIEVE THAT TIMING SO THAT THE CHIP KNOWS WHEN TO DO THINGS AND WHAT ORDER TO DO THEM IN, THAT REQUIRES SOMETHING THAT WE CALL A CLOCK, OR A CLOCK SIGNAL, AND THAT'S REALLY WHERE NOW WE'RE STARTING TO GET TO CHUCK MOORE'S INVENTION.

SO WHAT IS A CLOCK OR A CLOCK SIGNAL IN THE CONTEXT OF A MICROPROCESSOR? IT'S ACTUALLY A MUCH SIMPLER, STRAIGHTFORWARD CONCEPT THAN YOU MIGHT THINK. FOR A MICROPROCESSOR, A CLOCK IS JUST SOMETHING, A DEVICE THAT SENDS A TIMING SIGNAL TO THE CPU AND OTHER PARTS OF THE MICROPROCESSOR TO PROVIDE TIMING.

IT'S ACTUALLY VERY SIMILAR TO THE TICK, TOCK, TICK, TOCK OF A NORMAL CLOCK THAT WE'RE ALL FAMILIAR WITH. OR IF YOU HAVE A DIGITAL WATCH, FOR EXAMPLE, LIKE THIS ONE, WHERE THIS IS SHOWING 1:00 O'CLOCK, ONE SECOND, TWO SECONDS, WE SEE TIME GOING BY, AND A CLOCK SIGNAL IS VERY SIMILAR TO THAT IN A MICROPROCESSOR EXCEPT YOU SEE HERE A CLOCK SIGNAL IN A MICROPROCESSOR IS REPRESENTED BY THE SQUARE WAVE, AND BASICALLY EVERY TIME THERE'S AN EDGE OF THE SQUARE WAVE THAT GETS TO A CERTAIN POINT, THAT'S AN INDICATION THAT AN INSTRUCTION SHOULD BE EXECUTED, SO THAT WAY THE CLOCK HELPS CONTROL THE TIMING FOR THE MICROPROCESSOR SO THAT IT KNOWS WHAT TO DO, WHEN TO DO IT, AND WHAT ORDER TO DO IT IN.

SO THE CLOCK IS VERY IMPORTANT TO COORDINATE THE FUNCTIONS

OF THE MICROPROCESSOR CHIP, AND FOR THAT MATTER, TO ALSO COORDINATE THE FUNCTIONS OF THE MICROPROCESSOR CHIP WITH ALL OF THESE OTHER THINGS IN THE PHONE ON THE PRINTED CIRCUIT BOARD, BECAUSE JUST LIKE THE FUNCTIONS OF THE MICROPROCESSOR HAVE TO BE COORDINATED WITH THE TIMING SIGNAL, THE TIMING SIGNAL ALSO HAS TO BE USED TO COMMUNICATE WITH THINGS OUTSIDE OF THE CHIP, LIKE CAMERA, MEMORY, ET CETERA.

SO THAT'S AN IMPORTANT CONCEPT, HOW IMPORTANT CLOCK SIGNALS ARE FOR THE TIMING OF A MICROPROCESSOR TO MAKE SURE IT EXECUTES THINGS IN THE RIGHT ORDER AND AT THE RIGHT TIME.

NOW, ANOTHER THING THAT'S IMPORTANT TO UNDERSTAND ABOUT CLOCK SIGNALS IS A VERY IMPORTANT CHARACTERISTIC OF THEM IS HOW FAST THEY ARE, BECAUSE THERE ARE SOME FAST CLOCKS AND SOME SLOW CLOCKS, AND WHEN WE TALK ABOUT THE SPEED OF A CLOCK, THERE'S A SPECIAL WORD THAT WE USE TO REFER TO THAT AND THAT'S FREQUENCY.

SO AS I'M SURE YOU CAN APPRECIATE, IF A MICROPROCESSOR HAS A FASTER CLOCK SIGNAL WITH A HIGHER FREQUENCY, IT CAN ACTUALLY DO MORE WORK IN A SHORTER AMOUNT OF TIME.

IF IT HAS A LOWER SPEED CLOCK SIGNAL WITH A LOWER FREQUENCY OR A SLOWER SPEED, IT CAN'T DO AS MUCH WORK IN THE SAME AMOUNT OF TIME BECAUSE IT EXECUTES INSTRUCTIONS WITH EVERY, WITH EVERY CLICK OF THE CLOCK SIGNAL, EVERY TICK, TOCK.

SO I'M SURE, YOU KNOW, MANY OF US REMEMBER IN HIGH SCHOOL WHEN WE LEARNED ABOUT SIGN WAVES, AND THAT'S REALLY A VERY SIMILAR CONCEPT OF THESE SQUARE WAVES HERE EXCEPT THAT THEY'RE

SQUARE INSTEAD OF BEING WAVY LINE A SIGN WAVE.

SO CLOCK SIGNALS IN A COMPUTER -- LET ME TALK TO YOU ABOUT HOW THEY'RE REPRESENTED NORMALLY.

SO IN A COMPUTER, EVERYTHING IS DONE NORMALLY WITH 1'S AND 0'S, AND A LOT OF TIMES THAT'S KEPT TRACK OF WITH A VOLTAGE.

SO IF YOU LOOK AT THIS CLOCK SIGNAL AND WE JUST KEEP IT ON THE SCREEN HERE FOR A MINUTE, THE LOW PART OF THIS SQUARE WAVE IS PROBABLY REPRESENTED BY A LOW VOLTAGE LIKE 0 VOLTS, AND THE TOP PART OF THE SQUARE WAVE IS PROBABLY REPRESENTED IN A COMPUTER BY A HIGHER VOLTAGE, LIKE 1 VOLT.

SO BASICALLY -- IF WE COULD RUN THE ANIMATION AGAIN, BILL, PLEASE? THANK YOU.

YOU'VE GOT THIS ALTERNATING HIGH/LOW SIGNAL, AND IN A COMPUTER, AGAIN, IT WOULD BE HIGH, LOW, HIGH, LOW, MEANING A HIGH VOLTAGE, LOW VOLTAGE. OR 1, 0, 1, 0, WHICH IS HOW COMPUTERS DO EVERYTHING BASICALLY. THEY STORE INFORMATION IN 1'S AND 0'S.

THAT'S HOW THE CLOCKS ARE, TOO. SO THIS -- LET'S RUN THIS ONE MORE TIME JUST SO THAT WE CAN LOOK AT THE FREQUENCY CHANGE AGAIN.

LIKE WE TALKED ABOUT, THERE ARE ALSO DIFFERENT -- IT'S POSSIBLE TO HAVE A DIFFERENT FREQUENCY FOR A CLOCK. SO IF YOU LOOK AT THIS ONE IN PARTICULAR, THIS IS KIND OF A SLOW FREQUENCY, WHICH MEANS THAT THESE SQUARE WAVES ARE BIGGER, THEY'RE FATTER, IT TAKES LONGER FOR THEM TO GO BY THE DOTTED

WOODSIDE.

Q. SO ARE YOU THEN AN INVENTOR OF THE '336 PATENT?

A. THAT'S RIGHT.

Q. AND WERE THE -- WERE THERE ANY CO-INVENTORS THAT YOU HAD ON THE '336?

A. RUSSELL FISH WAS THE CO-INVENTOR.

Q. NOW, LET ME ASK YOU THIS: IS THE '336 PATENT PART OF A GROUP OR WHAT WE MIGHT CALL A PORTFOLIO OF PATENTS?

A. YES, IT IS.

Q. AND WHAT IS -- WHAT IS THAT CALLED?

A. THAT'S TERMED MMP PORTFOLIO, THE MOORE MICROPROCESSOR PATENT PORTFOLIO.

Q. AND HOW DOES THE '336 PATENT FIT INTO THE MMP PORTFOLIO?

A. I THINK THAT PORTFOLIO HAS ABOUT SEVEN PATENTS. WE APPLIED FOR A PATENT, AS IT INDICATES THERE, IN AUGUST OF 1989 AND THE PATENT OFFICE CAME BACK WITH AN OFFICE ACTION SAYING WE SHOULD BREAK IT UP INTO MULTIPLE PATENTS BECAUSE THERE WERE SO MANY IDEAS PRESENTED IN IT.

Q. OKAY. SO WHAT'S THE RELATIONSHIP BETWEEN THE '336 PATENT, THEN, AND THE ORIGINAL PATENT APPLICATION THAT YOU FILED BACK IN AUGUST OF 1989?

A. IT IS A PORTION OF THE ORIGINAL PATENT THAT DEALT WITH THE COMPUTER CLOCK.

Q. OKAY. SO HOW WOULD YOU GENERALLY DESCRIBE YOUR INVENTION IN THE '336 PATENT?

A. THE INVENTION IS THAT I PUT A RING OSCILLATOR ON THE SAME CHIP AS THE MICROPROCESSOR TO ACT AS A COMPUTER CLOCK; AND A SECOND CLOCK TO, TO INTERFACE WITH THE I/O INTERFACE.

IN OTHER WORDS, I -- INSTEAD OF ONE CLOCK, AS MOST COMPUTERS HAD, I HAD TWO CLOCKS THAT WERE INDEPENDENT.

Q. AND THE RING OSCILLATOR, WHICH PORTION OF THE MICROPROCESSOR WAS THE RING OSCILLATOR USED TO CLOCK?

A. IT CLOCKED THE CPU.

Q. WHAT IS A CPU?

A. IT'S THE CONTROLLING ELEMENT OF THE MICROPROCESSOR IN THE SAME SENSE AS THE MICROPROCESSOR IS THE CONTROLLING ELEMENT OF A COMPUTER.

Q. AND YOU MENTIONED THE TERM "CLOCK."

WHAT IS A CLOCK IN THE CONTEXT OF COMPUTERS?

A. A CLOCK IS A PERIODIC SIGNAL THAT IS USED TO DETERMINE WHEN AN INSTRUCTION BEGINS AND WHEN IT ENDS.

Q. NOW, I THINK YOU ALSO MENTIONED THE TERM "INPUT/OUTPUT INTERFACE."

WHAT IS AN INPUT/OUTPUT INTERFACE?

A. IT IS USED, FOR INSTANCE, TO COMMUNICATE WITH MEMORY. MEMORY REQUIRES PRECISE TIMING SIGNALS WHICH WOULD BE INAPPROPRIATE FOR A RING OSCILLATOR TO GENERATE, SO THEY WOULD BE GENERATED BY A CRYSTAL CLOCK.

LIKEWISE IF YOU HAVE AN ETHERNET CONNECTION THAT REQUIRES A VERY PRECISE TIMING SIGNALS, OR A USB REQUIRES TIMING

SIGNALS. ALL THESE PERIPHERAL DEVICES REQUIRE THEIR OWN TIMING.

Q. OKAY. MAYBE WE CAN GO TO FIGURE 17 OF THE '336 PATENT AND YOU CAN TALK TO US ABOUT SOME OF THESE THINGS.

ACTUALLY, FIGURE 17, I THINK, IS REPRODUCED ON THE FRONT PAGE, BUT -- YEAH, LET'S JUST BLOW THAT UP.

SO MAYBE YOU CAN USE THIS DIAGRAM, MR. MOORE, WHICH IS ON THE COVER OF THE '336 PATENT TO TALK ABOUT SOME OF THE THINGS YOU WERE JUST TALKING ABOUT WITH RESPECT TO YOUR INVENTION.

A. YES. THERE IS THE RING OSCILLATOR WHICH GENERATES A TIMING SIGNAL THAT IS PASSED TO THE CPU.

THEN THERE'S A SECOND CLOCK, THE CRYSTAL CLOCK, WHICH GENERATES A MORE -- A CONSTANT, A STEADY TIMING SIGNAL TO THE I/O INTERFACE.

AND THAT IS -- THAT IS AN APPROPRIATE FREQUENCY FOR THE EXTERNAL MEMORY BUS, FOR OTHER PERIPHERALS WHICH ARE DRIVEN BY THE COMPUTER.

Q. OKAY. VERY GOOD.

COULD YOU PLEASE TALK TO US ABOUT WHAT IN THIS DIAGRAM THAT WE SEE ON THE COVER PAGE OF THE '336 PATENT, WHICH OF THESE COMPONENTS ARE ACTUALLY ON THE MICROPROCESSOR ITSELF?

A. EVERYTHING EXCEPT THE CRYSTAL CLOCK.

Q. OKAY. SO THE RING OSCILLATOR, THE CPU, AND THE I/O INTERFACE, ARE THOSE ALL ON THE SILICON CHIP?

A. YES, THEY ARE.

A. THEY WERE ASSURED THE RIGHT TO MANUFACTURE THE CHIP AFTER WE PROVED THAT THE PROTOTYPES WERE SUCCESSFUL.

Q. AND DID -- WHERE WERE OKI'S SEMICONDUCTOR MANUFACTURING FACILITIES?

A. THEY WERE IN JAPAN.

Q. DID OKI EVENTUALLY FABRICATE OR MANUFACTURE THE CHIP?

A. THEY MADE ABOUT 20 PROTOTYPES FOR US IN THE -- OVER WINTER OF 1989.

Q. OKAY. SO LET'S TALK ABOUT THE SHBOOM CHIP. WHAT WAS SIGNIFICANT, FROM YOUR PERSPECTIVE, ABOUT THE DESIGN OF THE SHBOOM PROCESSOR?

A. FIRST, THAT IT WOULD RUN FORTH INSTRUCTIONS VERY EFFICIENTLY. IN RETROSPECT, IT USED VERY LITTLE ENERGY TO DO SO. THE CHIP RAN COOL, EVEN THOUGH IT WAS RUNNING VERY FAST. AND IT RAN VERY FAST.

Q. SO WHEN YOU SAY SHBOOM "RAN VERY FAST," MAYBE YOU COULD EXPLAIN FOR US WHAT YOU MEAN BY THAT.

A. I HADN'T -- INSTEAD OF USING A CRYSTAL TO CLOCK THE CHIP, I USED AN ON-CHIP RING OSCILLATOR, WHICH COULD RUN MUCH FASTER THAN A CRYSTAL, AND WAS VERY SUCCESSFUL IN THAT PARTICULAR APPLICATION.

Q. WELL, LET ME -- LET ME BACK UP JUST A LITTLE BIT THEN.

AT THE TIME IN THE 1998, '89 -- I'M SORRY -- 1988/'89 TIMEFRAME, HOW WERE COMMERCIAL PROCESSORS CLOCKED? WHERE DID THEY GET THEIR CLOCK PROCESSORS FROM TO YOUR KNOWLEDGE?

A. ALMOST ALL COMPUTERS HAD A CRYSTAL OSCILLATOR, A SEPARATE OFF-CHIP DEVICE THAT WOULD GENERATE A CLOCK SIGNAL FOR THEM.

Q. ALL RIGHT. LET'S TAKE A LOOK AT DDX-51, PLEASE.

AND EXPLAIN TO US WHAT YOU'RE TALKING ABOUT MAYBE USING THIS DEMONSTRATIVE HERE.

A. YES. SO IN THE LOWER LEFT-HAND CORNER IS A CRYSTAL OSCILLATOR. IT'S IN A METAL CONTAINER SO THAT -- TO SHIELD THE REST OF THE CIRCUITRY FROM STRAY RADIATION GENERATED BY THE OSCILLATOR.

AND IT SENDS A CLOCK SIGNAL TO THE MICROPROCESSOR CHIP. IT COMES IN ON ONE OF THE PINS IN ORDER TO GENERATE TIMING SIGNALS FOR THE CPU.

Q. SO JUST TO BE CLEAR, IS THIS HOW SHBOOM WAS CLOCKED OR IS THIS AN EXAMPLE OF HOW MICROPROCESSORS WERE CLOCKED BEFORE SHBOOM?

A. NO. SHBOOM DID NOT NEED THIS DEVICE TO CLOCK THE CPU. IT HAD AN ON-CHIP CLOCK.

Q. OKAY. LET'S TALK A LITTLE BIT MORE ABOUT CRYSTAL OSCILLATORS BEFORE WE GET TO HOW YOU DID IT WITH SHBOOM. DID CRYSTAL OSCILLATORS HAVE ANY ADVANTAGES THAT MADE THEM APPEALING TO CHIP DESIGNERS AT THE TIME?

A. THEY WOULD PRODUCE -- THEY WOULD ACCURATELY PRODUCE A FIXED FREQUENCY.

Q. AND DID -- OR DO CRYSTAL OSCILLATORS STILL HAVE ANY DISADVANTAGES THAT YOU CAN THINK OF?

A. THE DISADVANTAGES ARE THAT THEY PRODUCE A FIXED FREQUENCY. THEY ALSO USE A FAIR AMOUNT OF ENERGY TO PRODUCE THAT.

Q. LET'S TAKE A LOOK AT DDX-52, IF WE COULD, PLEASE. SO -- MAYBE YOU COULD LOOK AT THE SLIDE AND EXPLAIN TO THE JURY WHAT WE'RE LOOKING AT HERE.

A. THERE IS A BEAUTIFUL EXAMPLE OF A QUARTZ CRYSTAL, I DON'T KNOW THAT THE ONES THEY USED IN CRYSTAL OSCILLATORS LOOK THAT WAY. THEY'RE PROBABLY MORE SQUARE. BUT THOSE CRYSTALS ARE CUT OR DICED INTO CAREFULLY SIZED PIECES THAT WILL VIBRATE AT A PARTICULAR FREQUENCY, IT'S A MECHANICAL VIBRATION.

AND THEN THEY'RE PACKAGED IN, IN METAL PACKAGES BOTH FOR SHIELDING AND PROTECTION AND GIVEN POWER SO THAT THEY OSCILLATE.

Q. OKAY. AND IN TERMS OF THEIR FREQUENCY OF OSCILLATION, THE CLOCK SIGNAL THEY GENERATE, HOW FAST DO THEY TYPICALLY GO?

IF WE GO BACK TO 1989, HOW FAST DID THESE CRYSTAL OSCILLATORS TYPICALLY GO?

A. WELL, THEY WOULD START AROUND 32 KILOHERTZ, WHICH WAS A FREQUENCY USED IN WATCHES AND TIMEPIECES, AND THEY WOULD GO AS HIGH AS MAYBE 50 MEGAHERTZ, WHICH WAS A THOUSAND TIMES FASTER, FOR ELECTRONIC APPLICATIONS.

Q. SO FOR A -- I THINK YOU SAID FOR A QUARTZ CRYSTAL WATCH, YOU SAID THE CRYSTAL OSCILLATOR WOULD OSCILLATE AT 32 KILOHERTZ?

A. THAT'S RIGHT.

INSTEAD OF SEVEN?

A. THE RING OSCILLATOR WOULD, WOULD RUN AROUND FASTER -- EACH INVERTER ADDS A CERTAIN FIXED DELAY -- AND THAT WOULD HAVE BEEN TOO FAST FOR THE DECODING I HAD TO DO IN THE CPU.

Q. OKAY. SO LET'S GO AHEAD AND GO BACK TO DDX-56 AGAIN, AND GO AHEAD AND CONTINUE EXPLAINING WHAT WE'RE LOOKING AT HERE IF YOU WOULD, PLEASE.

A. NOW, THE I/O INTERFACE WAS CLOCKED WITH A 32 MEGAHERTZ CRYSTAL, AND THE MAIN OUTPUT OF THE I/O INTERFACE WAS CONTROL SIGNALS GOING TO MEMORY. SO THOSE FREQUENCIES WERE DETERMINED BY THE DEVICES THAT I WANTED TO DRIVE OFF-CHIP.

THAT HAD ALMOST NOTHING TO DO WITH THE SPEED OF THE CPU, AND SO I DECIDED TO RUN THAT AS FAST AS I COULD.

AT THE TIME, AND EVEN STILL TODAY, YOU GET BROWNIE POINTS FOR RUNNING YOUR COMPUTER FAST, EVEN IF IT'S NOT NECESSARY.

Q. OKAY. SO --

A. AND I WANTED TO HAVE A STUNNINGLY FAST MICROPROCESSOR.

Q. VERY GOOD. THANK YOU.

NOW, I SEE THAT THE NUMBERS THAT WE'RE VARYING BETWEEN HERE ON THE LEFT ARE 50, 70, AND 100. IS THERE SOME REASON YOU CHOSE TO PUT THOSE IN THIS PARTICULAR ANIMATION, DDX-56?

A. 100 IS THE FREQUENCY THAT I HOPED THE CPU WOULD RUN AT; 70 IS THE FREQUENCY -- 70 MEGAHERTZ IS THE FREQUENCY IT ACTUALLY RAN AT; AND 50 IS SORT OF THE LOWER LIMIT OF WHAT YOU MIGHT ACHIEVE AT LOW VOLTAGE.

Q. SO -- OKAY. SO THEN JUST -- SO YOUR CHIP WAS NOT ABLE TO RUN AT 100 MEGAHERTZ; IS THAT RIGHT?
A. THE SIMULATION SAID IT WOULD, BUT THE SIMULATOR WAS WRONG.
Q. OKAY. SO THE ACTUAL SPEED IT RAN AT, UNDER THE BEST CONDITIONS, WAS WHAT?
A. UNDER THE ONLY CONDITIONS I MEASURED IT WAS 70 MEGAHERTZ.
Q. OKAY. NOW, WHAT'S THE SIGNIFICANCE OF THIS LIGHT BULB OVER HERE WITH THE DIMMER SWITCH (INDICATING)? WHAT'S THAT SUPPOSED TO CONVEY?
A. WHEN YOU DIM A LIGHT BULB, YOU REDUCE THE FREQUENCY YOU SEND TO IT. SO IT'S JUST SUGGESTIVE OF THE FACT THAT THE LOW FREQUENCIES, IT RUNS LOWER THAN -- AT LOW VOLTAGES IT RUNS SLOWER THAN AT HIGH VOLTAGES.
Q. SO I'M SORRY, JUST TO MAKE SURE WE'RE CLEAR ON THE RECORD, WHEN YOU MOVE THE DIMMER SWITCH DOWN, YOU REDUCE WHAT?
A. REDUCE THE VOLTAGE AND REDUCE THE FREQUENCY.
Q. OKAY. AND SO THE FREQUENCY YOU'RE TALKING ABOUT IS THE CLOCK SPEED ON THE CHIP?
A. RIGHT. IT'S THE RING OSCILLATOR SPEED BASICALLY WHICH CONTROLS THE CPU.
Q. OKAY. VERY GOOD.
SO IF -- OH, I WAS ALSO GOING TO ASK YOU, WHAT'S THE SIGNIFICANCE OF THIS SPEED OVER HERE, 32 MEGAHERTZ? WHY DID YOU CHOOSE TO PUT THAT ON THIS PARTICULAR SLIDE?
A. I DON'T REMEMBER. THAT'S THE FREQUENCY OF THE CRYSTAL

WHICH I USED ON THE DEMO BOARD AND IT WAS APPROPRIATE FOR THE MEMORY.

IT WAS ALSO APPROPRIATE FOR GENERATING VIDEO SIGNALS, WHICH WAS BASICALLY WHAT I WAS DOING.

Q. OKAY. AND JUST TO BE CLEAR, I DON'T WANT TO CONFUSE ANYBODY, THIS -- THIS 32 IS NOT IN FIGURE 17 IN THE PATENT? THAT'S ACTUALLY SOMETHING THAT WAS ADDED TO ILLUSTRATE THIS?

A. THAT'S RIGHT. THE -- THAT WAS DETERMINED EMPIRICALLY.

Q. OKAY. AND YOU SAY THAT 32 MEGAHERTZ SPEED WAS THE SPEED OF -- YOU MENTIONED SOME KIND OF BOARD OR SOMETHING.

A. WE MADE A DEMONSTRATION BOARD WITH A SHBOOM CHIP ON IT AND SOME MEMORY AND SOME OTHER CIRCUITRY AND THAT WAS THE CRYSTAL THAT WE USED ON THAT BOARD.

Q. OKAY. SO THE CRYSTAL YOU USED ON THE BOARD WAS 32 MEGAHERTZ AND THAT WAS USED TO CLOCK THE I/O INTERFACE OF SHBOOM?

A. RIGHT.

Q. OKAY. SO -- LET'S SEE. LET'S TAKE A LOOK NOW AT FIGURE -- I MEAN DDX-57 AND TALK A LITTLE BIT MORE ABOUT RING OSCILLATORS.

SO WHAT ARE WE LOOKING AT HERE IN DDX-57, MR. MOORE?

A. HERE WE SHOW THAT A RING OSCILLATOR REQUIRES A POWER SUPPLY. IN THIS CASE IT WAS A 5 VOLT POWER SUPPLY. YOU APPLY 5 VOLTS TO THE TRANSISTORS IN THESE INVERTERS AND THE INVERTER WILL RUN.

FALLING EDGE, LIKE GOING FROM 1 TO 0 IS THE ONE THAT CLOCKS THE SYSTEM, BUT THAT'S IRRELEVANT.

JUST WHAT I NEED YOU TO REMEMBER IS THAT THAT ONE TRANSITION, ONE TRANSITION, 0 TO 1, WHICH YOU SEE EVERY PERIOD, OKAY, IS WHAT GIVES THE PROCESSOR STOP AND GO.

SO IT OPERATES IN LOCK STEPS. JUST LIKE MR. SMITH WAS PRESSING THE RUN, PAUSE BUTTON, RUN AND PAUSE BUTTON TO GO FROM STEP TO STEP TO STEP, THIS IS WHAT CLOCK DOES. IT DIRECTS THOSE OPERATIONS.

SO THE OPERATIONS IN A MICROPROCESSOR IS VERY SIMPLE, THEY GO JUST FOR ONE STEP, AND THE CLOCK IS THE ONE THAT GIVES THAT SIGNAL, THE GO SIGNAL.

Q. SO DOCTOR, I WANT TO ASK YOU, YOU MENTIONED THAT BY PERFORMING BILLIONS OF CALCULATIONS PER SECOND, YOU CAN PERFORM VERY COMPLEX, COMPLEX OPERATIONS.

WHAT I'M CURIOUS ABOUT IS, DOES THE SPEED OF THE CLOCK SIGNAL MATTER AT ALL?

A. YES.

MR. SMITH, CAN YOU CONTINUE RUNNING IT JUST FOR ILLUSTRATION?

YES, BECAUSE -- OKAY. THIS CLOCK TELLS A CPU WHEN TO START AND END THOSE STEPS, WHEN TO START.

SO THE SPEED OF THE CLOCK DETERMINES HOW FAST THESE OPERATIONS ARE BEING PERFORMED. SO LET'S SAY IF I CAN RUN, HYPOTHETICALLY I CAN RUN THAT PROCESSOR AT ONE SECOND, JUST AS

I SAID, STOP, GO, STOP, GO, OR I CAN RUN IT AS FAST AS ONE BILLION OF THOSE PER SECOND.

SO A CLOCK IS THE ONE THAT DIRECTS THE SPEED, OR DETERMINES THE SPEED, OR THE PROCESSING FREQUENCY IN FANCIER TERMS, OF THE MICROPROCESSOR.

SO HOW FAST -- SO JUST LIKE IF YOU HAVE A PERSON WHICH IS WALKING AND YOU DELAY, OKAY, GO, STOP, OKAY, SO ONE STEP AT A TIME, OKAY, YOU CAN, BY GIVING THOSE INSTRUCTIONS, DETERMINE HOW FAST THIS PERSON WILL MOVE.

Q. SO I HEARD YOU MENTION THE WORD "FREQUENCY." CAN YOU EXPLAIN TO THE JURY WHAT THAT MEANS IN TERMS OF THIS CLOCK SIGNAL THAT WE SAW UP HERE?

A. OKAY. FREQUENCY -- OKAY. IN GENERAL, I MEAN, FREQUENCY IS GENERAL TERM, RIGHT? FREQUENCY MEANS HOW OFTEN SOMETHING CHANGES, YOU KNOW? YOU CAN HAVE A FREQUENCY OF ONCE A WEEK, THAT YOUR GARBAGE COMES ON MONDAY. THAT'S THEIR FREQUENCY, ONCE A WEEK FOR SEVEN DAYS.

GENERALLY IN TECHNICAL TERM, WE DEFINE FREQUENCY IN HERTZ. 1 HERTZ MEANS IT CHANGES ONE PER SECOND. 2 HERTZ MEANS CHANGE TWICE PER SECOND. 1 MEGAHERTZ MEANS IT CHANGES ONE MILLION TIMES PER SECOND. 1 GIGAHERTZ MEANS ONE BILLION TIMES PER SECOND.

Q. SO I NOTICE IN THIS ANIMATION WHEN WE RAN THE CLOCK SIGNAL THAT THE SQUARE WAVES GOT SMALLER AND CLOSER TOGETHER. DOES THAT HAVE ANYTHING TO DO WITH THIS CONCEPT OF FREQUENCY?

A. YES. IT'S RUNNING FASTER.
Q. SO AT THE END IT'S RUNNING FASTER. IS THAT A FASTER FREQUENCY?
A. CORRECT.
Q. AND WHAT ABOUT -- WE'VE HEARD THE TERM "CLOCK RATE" MENTIONED BEFORE. WHAT DOES THAT MEAN?
A. THAT IS ANOTHER MORE COLLOQUIAL TERM TO SAY CLOCK FREQUENCY, OR FREQUENCY OF THE CLOCK. A RATE MEANS HOW, HOW FAST IT CHANGES.
Q. AND SO JUST TO BE TOTALLY CLEAR, FOR THE PURPOSES OF THIS CASE, WHAT DOES IT MEAN WHEN THE CLOCK RATE GETS FASTER? WHAT DOES THAT MEAN FOR THE CPU PROCESSING FREQUENCY?
A. IT RUNS FASTER.
Q. THANK YOU.
LET'S TURN TO THE NEXT SLIDE, DDX-110, AND WHAT ARE YOU SHOWING IN THIS SLIDE?
A. OKAY. WHAT WE ARE SHOWING IN THIS SLIDE IS AN ILLUSTRATION OF A PROCESSOR WHICH IS RECEIVING THAT CLOCK SIGNAL FROM AN EXTERNAL CLOCK.
NOW, BY PASSING THAT LITTLE PIECE OF BOARD, YOU'VE SEEN THAT LITTLE, LITTLE ENCAPSULATED LITTLE BOX WHERE THE CRYSTAL IS (INDICATING). THE BOX CONTAINS USUALLY MORE THAN JUST A CRYSTAL. THERE'S AN OSCILLATOR CIRCUIT WHICH MAKES THIS CRYSTAL OSCILLATE, AND IT PRODUCES A SIGNAL WHICH IS A SQUARE WAVE, BASICALLY, THAT COMES TO THE PIN OF THE CHIP, GETS ON THE

CHIP, AND IS DISTRIBUTED THROUGHOUT THE CHIP.

SO THIS CRYSTAL HERE IS CLOCKING THIS CHIP IN THIS PARTICULAR CASE (INDICATING).

Q. AND SO JUST TO BE PERFECTLY CLEAR, WHAT'S THE BLUE SQUIGGLY LINE IN THIS FIGURE (INDICATING)?

A. THAT IS A CLOCK SIGNAL.

Q. AND WHAT'S THE SIGNIFICANCE OF THE TITLE OF THIS SLIDE, IF ANY?

A. WHAT WE ARE ILLUSTRATING AND WHAT I THINK MR. MOORE DESCRIBED HERE BEFORE THE PATENT, THE MAJORITY -- AT THAT TIME THE COMPUTERS WERE CLOCKED BY AN EXTERNAL CLOCK, THE CLOCK WHICH WAS ON THE P.C. BOARD, PROVIDING THAT CLOCK SIGNAL TO THE CPU (INDICATING).

AND FOR THOSE OLDER PEOPLE, LIKE ME, WE REMEMBER THAT THE FIRST P.C. WAS RUNNING FROM 4.7 MEGAHERTZ CRYSTAL AND THE LATER A.T. WAS RUNNING AT 8, AND WE COULD KIND OF WIGGLE AND REPLACE IT AND JUST OVER CLOCK IT TO 10 MEGAHERTZ, YOU KNOW, BY, BY CHANGING THE FREQUENCY OF THAT CLOCK. YOU CAN HAVE YOUR IBM P.C. TO RUN FASTER EXACTLY THAN WHAT THEY DESIGNED IT FOR. THEY DID NOT RECOMMEND IT AND LIKE IT, BUT YOU COULD DO IT.

Q. THANK YOU. LET'S TALK A LITTLE BIT MORE ABOUT THE CRYSTAL. SO YOU SAID IT'S A CRYSTAL. WHY DO WE CALL IT A CRYSTAL?

A. THE ANSWER IS BECAUSE IT IS A CRYSTAL, OKAY.

Q. ASK A STUPID QUESTION, I GUESS.

A. YEAH.

Q. CAN YOU EXPLAIN, WHY DO WE USE A CRYSTAL?

A. SORRY. JUST LET ME EXPLAIN IT, OKAY?

WHAT IS SHOWN HERE IS A CRYSTAL, QUARTZ CRYSTAL (INDICATING).

NOW, THIS QUARTZ CRYSTAL HAS WHAT IS CALLED A PIEZOELECTRIC EFFECT, IT'S A GREEK WORD. PIEZOELECTRIC IS A PROPERTY THAT IF YOU TAKE ANY SLICE OF THIS CRYSTAL AND PUT IT BETWEEN TWO ELECTRODES, IF YOU SQUEEZE THOSE ELECTRODES WITH YOUR FINGERS, YOU SQUEEZE THEM, THERE WILL BE VOLTAGE HERE THAT WILL SHOW UP (INDICATING).

ALSO, IF YOU APPLY A VOLTAGE, THIS CRYSTAL WILL EITHER EXPAND OR SHRINK.

SO IF YOU APPLY ALTERNATING VOLTAGE HERE (INDICATING), THE CRYSTAL WILL MECHANICALLY VIBRATE, OKAY?

AND THEN IF YOU HIT THE RIGHT FREQUENCY, JUST LIKE THE TUNING FORK -- I HOPE YOU ARE FAMILIAR WITH THE TUNING OF A PIANO -- YOU CAN HIT IT, IT RESONATES AT A FREQUENCY WHICH IS DETERMINED BASICALLY BY THE LENGTH OF THOSE FORKS. SO IT HAS ITS OWN FREQUENCY.

SO IF I APPLY AN ALTERNATING VOLTAGE HERE TO A CRYSTAL AND I HIT ITS RESONATING FREQUENCY, I CAN MAKE IT OSCILLATE. BASICALLY I WILL RECEIVE THAT SIGNAL BACK AND I WILL AMPLIFY IT. I WILL AMPLIFY THAT, WHAT I GET, AND I WILL GET IT INTO OSCILLATION.

NOW, LET ME JUST FINISH THIS.

NOW, YOU ADJUST THAT OSCILLATION BY HOW THIN THAT CRYSTAL IS, AND AS I SAID, WHEN I WAS 12 YEARS OLD, I OPENED IT APART AND THEN YOU WOULD SAND IT BASICALLY BY, BY SANDING IT ON A VERY FINE PAPER (INDICATING). YOU CAN MAKE A TINY SLICE AND YOU CAN CHANGE THE FREQUENCY BECAUSE WE HAD TO ADJUST THE FREQUENCY TO GO IN A CERTAIN RANGE, WHICH I DIDN'T HAVE APPROPRIATE CRYSTAL FOR, FOR EXAMPLE.

SO, NOW, THIS FREQUENCY OF OSCILLATION, WHEN YOU BUILD A CRYSTAL, IT'S VERY STABLE.

Q. SO LET ME ASK YOU THIS: YOU MENTIONED OSCILLATION AND OSCILLATING AND OSCILLATORS. WHAT DOES THAT MEAN? WHAT DOES IT MEAN TO OSCILLATE IN THIS CONTEXT?

A. TO OSCILLATE MEANS TO CHANGE PERIODICALLY THE OUTPUT OF THE SIGNAL. SO THE OUTPUT OF, LIKE, THE OSCILLATOR -- WELL, ACTUALLY LET ME GET BACK. YOU'RE ASKING THE DEFINITION OF WHAT DOES IT MEAN TO OSCILLATE.

I WOULD DEFINE IT AS TO PERIODICALLY CHANGE A PROPERTY.

Q. SO THAT'S SIMILAR TO THE VIBRATION OF THE FORK? IT'S VIBRATING BACK AND FORTH? THAT'S AN OSCILLATION?

A. IT CHANGES THE DISTANCE, RIGHT, AND THAT IS AN OSCILLATION. AS A RESULT, YOU HEAR THE SOUND SIGNAL.

BUT THAT MECHANICAL VIBRATION IS WHAT DEFINES THE OSCILLATION.

Q. AND WHAT'S THE SIGNIFICANCE OF THE TEXT AT THE BOTTOM OF

DDX-111?

A. OH. IF YOU GO ON THE PREVIOUS SLIDE, FOR EXAMPLE, PROBABLY GOOD TO USE THAT, YEAH, SO THE ONE -- CRYSTALS WERE GREAT, AND STILL THEY'RE GREAT AND THEY'RE USED. AS A MATTER OF FACT, YOUR WATCH, THEY HAVE A CRYSTAL RUNNING IT 32768 HERTZ TO CREATE PRECISE SECOND. THEY'RE ALL BASED ON CRYSTAL.

BUT WE CAN MAKE THIS FREQUENCY AS HIGH AS YOU CAN THIN IT, AND BY SANDING A CRYSTAL, YOU BREAK IT EVENTUALLY. IT BECOMES SO THIN THAT YOU REACH THE MAXIMUM FREQUENCY.

SO THE FREQUENCY IS WE CAN FABRICATE, AND TODAY THEY'RE VERY SMALL, OKAY. IT REACHES ITS LIMIT, BASICALLY. AND THAT LIMIT IS I WOULD SAY ABOUT 50 MEGAHERTZ, THOUGH I'VE SEEN, LIKE, OKAY POSSIBLY TO PRODUCE HUNDRED. BUT THIS IS ABOUT IT, OKAY? SO THAT'S THE END OF THE FREQUENCY THAT YOU CAN PRODUCE WITH A CRYSTAL.

SO AS THE PROCESSOR SPEED, AS YOU KNOW, SO-CALLED MOORE'S LAW HAVE DOUBLED EVERY TWO YEARS, EVERY GENERATION SINCE ACTUALLY MOORE INVENTED MICROPROCESSOR. ACTUALLY, IT WASN'T HIM, I BELIEVE. THAT FREQUENCY, LET'S SAY AT THE OLD TIME WHEN WE HAD A.T., IT WAS 10 MEGAHERTZ AND 3 MEGAHERTZ, AND NOW WE CANNOT CLOCK WITH A CRYSTAL ANYMORE BECAUSE THE FREQUENCY NOW IS MUCH HIGHER.

SO THAT'S ONE.

THE TWO IS YOU CANNOT INTEGRATE IT ON THE CHIP BECAUSE THIS CHIP, AS YOU'VE SEEN, IS SILICON AND THIS IS QUARTZ. THEY

DON'T MIX.

AND THIS IS RELATIVELY LARGE PIECE TO PUT ON.

SO IT BECAME NOT POSSIBLE TO INTEGRATE, I MEAN TO CLOCK THIS WAY ANYMORE.

AND THE '336 MOVED THE OSCILLATOR ON THE CHIP, AND THAT OSCILLATOR IS FABRICATED ON THE CHIP THE SAME WAY AS THE REST OF THE PROCESSOR IS FABRICATED OF THE SAME TRANSISTORS. IT WILL BEHAVE THE SAME WAY. IT WILL BE SUBJECTED TO THE SAME CONDITIONS BECAUSE IT'S ON THE SAME SPOT, BASICALLY, IN THE SAME HOUSE HERE AND IT WILL BEHAVE THE SAME (INDICATING).

Q. EXCELLENT. I WANT TO MAKE SURE THAT ONE THING IS CLEAR THAT MIGHT HAVE GOTTEN CONFUSED THERE. I HEARD YOU MENTION MOORE'S LAW, AND WE'VE HAD AN INVENTOR NAMED CHARLES MOORE.

I JUST WANT TO MAKE SURE, WE'RE TALKING ABOUT TWO DIFFERENT MOORES, RIGHT?

A. I'M TALKING ABOUT GORDON MOORE, YEAH.

Q. OKAY. I JUST WANT TO MAKE SURE THAT THAT'S CLEAR.

OKAY. SO LET'S MOVE ON TO DDX-112, AND I THINK YOU PREPARED AN ANIMATION HERE. I WANT TO ASK YOU WHAT YOU'RE TRYING TO SHOW US IN THIS ANIMATION.

A. OKAY. WHAT I'M TRYING TO SHOW IS TO DIFFERENTIATE WITH A SCENARIO -- HOLD ON, PLEASE -- WHEN WE HAD THE PROCESSOR, MICROPROCESSOR BEING CLOCKED WITH A FIXED CRYSTAL, OKAY?

AND SO THIS IS JUST LIKE WE HAVE A CAR, WHICH OBVIOUSLY CAN RUN FAST, WE CHOSE A FERRARI, THAT'S THAT RIGHT HERE

(INDICATING), BUT WE HAVE SET THE ENGINE SPEED TO 25 MILES PER HOUR BECAUSE WE DON'T WANT TO GET ANY TICKETS AND WE KNOW IT'S GOING TO GO THROUGH THE SCHOOL ZONE. SO IT'S FIXED AT 25 MEGAHERTZ.

SO NOW YOU CAN RUN IT, MR. SMITH.

Q. SO THE 25 MILES AN HOUR, WHAT DOES THAT REPRESENT?

A. THAT'S THE SPEED AT WHICH THIS FERRARI HAS BEEN FIXED TO RUN, AND EVEN THOUGH IT ENTERED THE FREEWAY, IT CAN RUN FASTER, IT'S NOT GOING TO GO FASTER THAN 25 ON THE SPEED DIAL HERE (INDICATING).

Q. AND SO WHY DID YOU LABEL THIS SLIDE "CPU CLOCK SPEED BEFORE THE '336 PATENT"?

A. WELL, IF WE GO TWO SLIDES BACK, RIGHT, WHEN WE HAD THAT CRYSTAL, SO WE HAVE A FIXED CRYSTAL, AND LET'S SAY WE TOOK THE MAXIMUM POSSIBLE, LET'S SAY TODAY 50 MEGAHERTZ CLOCKING THAT, THAT CHIP. IT CANNOT RUN FASTER THAN 50 MEGAHERTZ, EVEN THOUGH TECHNOLOGY TODAY WILL ALLOW IT TO RUN 4 GIGAHERTZ.

Q. JUST LIKE THE FERRARI IS ABLE TO GO FASTER? IS THAT YOUR POINT?

A. JUST LIKE FERRARI.

Q. OKAY. LET'S MOVE ON TO DDX-113, AND I WANT TO ASK YOU, WHAT ARE YOU SHOWING US HERE IN THIS SLIDE?

A. SO THIS IS A QUOTE FROM THE '336 PATENT. IT SAYS THAT "THE RING OSCILLATOR IS USEFUL AS A SYSTEM CLOCK BECAUSE ITS PERFORMANCE TRACKS THE PARAMETERS WHICH SIMILARLY AFFECT ALL

OTHER TRANSISTORS ON THE SAME SILICON DIE."

BASICALLY WHAT IT SAYS, THIS CLOCK IS ON THE SAME PLACE AS THE REST, MADE OUT OF THE SAME THING AS THE REST, AND IT WILL BE AFFECTED THE SAME WAY AS THE REST OF THE CHIP.

Q. THANK YOU. LET'S TAKE A LOOK AT A DIFFERENT ANIMATION IN DDX-114 THAT YOU HAVE LABELED "CPU CLOCK SPEED AFTER THE '336 PATENT." WHAT ARE YOU TRYING TO SHOW US HERE?

A. NOW WE HAVE, PLEASE NOTICE, THIS IS A RED FERRARI, OKAY, AND THIS ONE IS ALLOWED TO CHANGE SPEED AND ADAPT TO THE CONDITIONS OF THE ROAD.

SO LET'S RUN IT.

Q. SO THE SPEED LIMIT WENT TO 75 AND THE CAR WENT FASTER?

A. RIGHT. I GUESS THE DRIVER DOESN'T WANT TO GET A TICKET, SO HE'S KIND OF OBSERVING THE LIMIT, WHICH I WOULDN'T IF I HAD RED FERRARI.

Q. AND APPARENTLY HE'S IN MONTANA, SO THE SPEED LIMIT IS NOW 100.

A. THAT'S A GOOD STATE, MONTANA, YEAH.

Q. AND HE'S ABLE TO GO 100. SO THAT IS ON A SLIDE ENTITLED "CPU CLOCK SPEED AFTER THE '336 PATENT." HOW DOES THAT RELATE TO THE '336 PATENT?

A. SO WHAT '336 DID BY PUTTING THAT CLOCK ON THE CHIP ALLOWED IT TO RUN AS FAST AS THE PROCESSOR CAN RUN. ACTUALLY IT ALLOWS IT TO CHANGE THE SPEED SO YOU CAN ADAPT. YOU CAN RUN IT BASICALLY AT THE SPEED, AT THE SPEED YOU WANT.

OR FABRICATION VARIATIONS?

A. YES, IT DOES. WHAT '336 SAYS BASICALLY, BY PUTTING THE OSCILLATOR ON THE SAME DIE AS THE CPU, THE PROCESS IS GOING TO IN EFFECT BE EQUAL. SO THOSE THAT HAVE, THAT RESULT IN A FASTER PROCESSOR WILL ALSO HAVE FASTER CLOCK, AND THOSE THAT RESULT IN A SLOWER PROCESSOR WILL HAVE A SLOWER CLOCK.

SO WHAT THE PATENT SAYS, THEY WILL VARY TOGETHER DUE TO MANUFACTURING AND MANUFACTURING VARIATIONS.

Q. SO I SEE HERE ON DDX-117 THERE'S A SELECTION FROM EXHIBIT 245 OF THE PATENT. WHAT DOES THIS TELL US?

A. OKAY. LET ME TRY TO SIMPLIFY THE PATENT LANGUAGE. IT'S ALWAYS DIFFICULT TO READ.

BUT THIS BASICALLY SAYS IF THE FABRICATION PROCESS ON A PARTICULAR CHIP RESULTS IN SLOW TRANSISTORS, EVERYTHING ON THE CHIP WILL OPERATE SLOWER, MEANING THE CPU AND THE RING OSCILLATOR THAT CLOCKS IT WILL OPERATE SLOWER.

WHY? BECAUSE THEY'RE MADE OF THE SAME TRANSISTORS AND THEY'RE AFFECTED IN THE SAME WAY. THAT'S BASICALLY -- YOU KNOW, WHEN YOU TRANSLATE THIS LEGAL LANGUAGE INTO NORMAL LANGUAGE, THAT'S WHAT IT SAYS.

Q. AND IS THAT TRUE FOR EVERY CHIP?

A. YES, THAT IS TRUE FOR EVERY CHIP.

Q. WHAT IF YOU TRY VERY HARD TO DESIGN CHIPS SO THAT THEY'RE EXACTLY THE SAME? WILL YOU GUARANTEE THAT THEY'LL RUN THE SAME SPEED?

A. IF I HAVE A WAFER AND I TRY TO HAVE ALL THE CHIPS THE SAME ON THE WAFER, I CAN'T.

Q. WHY IS THAT?

A. BECAUSE THE MANUFACTURING PROCESS DOES NOT ALLOW ME TO CONTROL THINGS TO SUCH A DEGREE THAT I CAN MAKE THEM PRECISELY THE SAME.

Q. AND EARLIER YOU MENTIONED THE TERM "TRANSISTORS." AT A VERY HIGH LEVEL, WHAT IS A TRANSISTOR?

A. BASICALLY -- THIS IS A GREAT QUESTION, ACTUALLY. IN A DIGITAL WORLD, THE TRANSISTOR IS LIKE A SWITCH, SO IT IS ON OR OFF (INDICATING).

AND WE CAN MAKE DEVICES OUT OF THOSE SWITCHES. SO, FOR EXAMPLE, WHEN YOU SEE THAT INVERTER (INDICATING), WHICH YOU HAVE SEEN IN THE OPENING STATEMENT, IT'S LIKE A STAIRCASE SWITCH. YOU KNOW, YOU TURN IT WITH THE LIGHT BULB IS GOING IN THE OPPOSITE DIRECTIONS, BASICALLY BECAUSE IT CONNECTS EITHER UP OR DOWN.

SO IT HAS TWO TRANSISTORS WHICH ARE OPPOSITE, OKAY. SO THE OUTPUT IS CONDUCTED EITHER DOWN TO GROUND OR IT'S CONNECTED UP TO THE VOLTAGE BASED ON WHAT THE INPUT IS.

AND YOU DO THE OPPOSITE FUNCTION IN THE INVERTER.

SO BASICALLY THEY ARE -- THEY OPERATE AS SWITCHES, FAST SWITCHES IN A DIGITAL WORLD BECAUSE WE ALSO DEAL WITH 0'S AND 1'S, SO WE DON'T CARE FOR ANYTHING IN BETWEEN.

Q. ARE THEY A MECHANICAL SWITCH, LIKE A LIGHT SWITCH?

A. NO, NO. THEY'RE ELECTRIC SWITCH.
Q. SO THEY'RE ELECTRONIC DEVICES?
A. THEY'RE ELECTRONIC DEVICES, YES.
Q. ON A MODERN MICROPROCESSOR, WHAT COMPONENTS ARE MADE UP OF TRANSISTORS, IF ANY?
A. EVERYTHING IS MADE OUT OF TRANSISTORS. THAT'S A BASIC BLOCK. THAT IS LIKE A BRICK AND YOU WILL BUILD WITH IT AND LARGER STRUCTURES.
BUT BASIC, BASIC BLOCK IS TRANSISTOR. A BASIC -- AND ACTUALLY, THERE'S NOTHING MORE COMPLICATED THAT WE BUILD THAN TRANSISTOR. WE BUILD COMPLICATED THINGS OUT OF TRANSISTORS.
Q. SO WE'VE TALKED A LITTLE BIT BEFORE ABOUT A CPU AND A RING OSCILLATOR. IS THE CPU MADE OUT OF TRANSISTORS?
A. YES, ENTIRELY.
Q. IS THE RING OSCILLATOR MADE OUT OF TRANSISTORS?
A. YES.
Q. LET'S TALK A LITTLE BIT ABOUT RING OSCILLATORS. ON DDX-118, YOU HAVE AN ANIMATION HERE. COULD YOU PLEASE EXPLAIN WHAT THIS -- BEFORE WE DO THAT, I SEE THIS SAYS FIG 18. WHERE IS THIS FIGURE FROM?
A. THIS FIGURE IS TAKEN FROM THE '336 PATENT.
Q. OKAY. AND --
(DISCUSSION OFF THE RECORD BETWEEN DEFENDANTS' COUNSEL.)
BY MR. MARSH:
Q. LET'S GO AHEAD AND QUICKLY GO THROUGH THIS. LET'S RUN THE

ANIMATION, PLEASE BILL.

A. I WOULD -- LET ME EXPLAIN BEFORE THE ANIMATION. I HOPE I CAN EXPLAIN BETTER THAN IT WAS IN THE OPENING STATEMENT.

SO WHAT THE RING OSCILLATOR IS, OKAY, SO HERE YOU HAVE A SIGNAL WHICH IS 0. AS I EXPLAINED, THIS INVERTER WILL MAKE THE OPPOSITE, WHICH IS 1. THIS ONE IS GOING TO MAKE THE OPPOSITE, WHICH IS 0.

SO WE STARTED WITH 0. REMEMBER THAT. WE STARTED WITH 0, OKAY? THIS IS 0. MAKE 1, MAKE 0, MAKE 1, 0, 1, 0, 1.

NOW, THIS 1 IS CONNECTED BACK TO THIS INPUT, SO IT CHANGES THE 0 TO 1, WHICH WILL CHANGE THIS TO 0, TO 1, 0, 1, 0, 1, 0.

NOW, THAT 0 IS CONNECTED TO THE INPUT AND IT WILL MAKE THE CHANGE AGAIN. OKAY?

AND AS I SAID, THIS INVERTER HAS CERTAIN DELAY. IT DOESN'T HAPPEN INSTANTANEOUSLY. JUST LIKE AFTER TEN PICOSECONDS, LET'S SAY, IT WILL SWITCH.

Q. SO PICOSECONDS IS A VERY SHORT TIME?

A. VERY SHORT, LINE 10 TO THE MINUS 12, OKAY?

SO YOU HAVE A SITUATION HERE WHERE THIS IS ALWAYS CHASING EACH OTHER. THIS INPUT IS ALWAYS CHASING STABILITY BECAUSE THAT 0 GETS CHANGED TO 1, THAT 1 WILL CHANGE TO 0, THE 0 GET CHANGED TO 1, THAT 1 GETS CHANGED TO 0, ET CETERA, ET CETERA.

NOW, THE ANALOGY I HAVE FOR THAT IS, AND I'M SURE WE HAVE SEEN IT, IT'S LIKE WHEN YOU HAVE A DOG CHASING ITS TAIL, OKAY? AND IT'S RUNNING IN CIRCLE, SO BECAUSE, YOU KNOW, THE MOMENT A

Q. AND IS THAT THE CLOCK SIGNAL THAT IT USES TO THEN DECIDE WHEN TO START AND STOP TO DO ITS OPERATIONS?

A. EXACTLY. THAT'S THE START AND STOP OF ALL THE OPERATIONS THAT THE CPU PERFORMS AS WE ILLUSTRATED BEFORE.

Q. AND WHAT'S THIS BIG BLACK PORTION OF THE RECTANGLE THAT WE SEE ON THIS SLIDE?

A. THAT IS LET'S SAY ILLUSTRATING THE PACKAGE, OKAY? THIS IS THE PACKAGE AND THE CHIP IS, IS ENCAPSULATED INTO THIS PACKAGE.

Q. SO THAT WHERE THE -- WHERE ARE THE RING OSCILLATOR AND THE CPU LOCATED EXACTLY WITH RESPECT TO THE PROCESSOR?

A. ON THE SAME CHIP.

Q. NOW, I THINK -- ONE OF OUR JURORS ASKED A QUESTION ABOUT CLOCKING THE RING OSCILLATOR, OR THE SPEED OF THE RING OSCILLATOR IN THE CPU, SO I WANT TO JUST MAKE SURE THAT WE'VE GOT THIS PERFECTLY CLEAR.

IF THE RING OSCILLATOR HAS A SPEED OF 80 MEGAHERTZ, IF THAT'S ITS CLOCK RATE, WHAT WOULD BE THE PROCESSING FREQUENCY OF THE CPU?

A. IT WOULD BE -- AS YOU SEE, THEY ARE CONNECTED. IF YOU HAVE 80 MEGAHERTZ HERE, LIKE THAT GOES HERE AND YOU HAVE 80 MEGAHERTZ IN THE CPU, SO CPU IS OPERATING AT 80 MEGAHERTZ (INDICATING).

SO IT'S EXACTLY THE SAME.

Q. AND WHAT WOULD HAPPEN IF YOU CHANGED THE CLOCK RATE OF THE RING OSCILLATOR TO 100 MEGAHERTZ?

A. THEN THIS IS WIGGLING AT 100 (INDICATING), GOES IN AT 100, AND THE CPU IS OPERATING AT 100 MEGAHERTZ.

Q. SO THAT WOULD BE -- THE CPU PROCESSING FREQUENCY WOULD BE 100 MEGAHERTZ.

SO THE SAME TRUE AT 2 GIGAHERTZ? IF WE GO REALLY FAST AT 2 GIGAHERTZ FROM THE CLOCK OSCILLATOR --

A. IT IS TRUE AT ANY FREQUENCY. WHY? BECAUSE THEY'RE CONNECTED.

THIS IS JUST LIKE IF I GRAB MR. MARSH'S HAND AND I START SHAKING IT AT LIKE 2 HERTZ FREQUENCY, HE'S SHAKING AT TWO HERTZ (INDICATING).

IF I GO AT TEN HERTZ, HE'S SHAKING AT TEN HERTZ (INDICATING). THOSE TWO ARE CONNECTED.

SO IF THIS ONE IS PRODUCING THE OUTPUT OF THE OSCILLATOR AT 2 GIGAHERTZ, IT IS DISTRIBUTED AT 2 GIGAHERTZ.

Q. NOW, IF, IN PRACTICE, I WANTED TO CHANGE THE FREQUENCY THAT THE RING OSCILLATOR IS OPERATING AT, WHAT COULD I DO? HOW WOULD THAT BE IMPLEMENTED IN A MODERN MICROPROCESSOR?

A. OKAY. WHAT I CAN DO IS I CAN LOOK AT -- I CAN CHANGE THE RING OSCILLATOR. SO IF I RAISE THE VOLTAGE OF THE RING OSCILLATOR OR LOWER THE VOLTAGE -- OR IF I FIND A SPOT, LET'S SAY I LIMIT THE CURRENT THAT GOES THROUGH THIS RING OSCILLATOR, OR WHAT IS KNOWN, THE TERM IS LIKE CURRENT STARVING, OKAY, IF I STARVE IT FROM CURRENT, IT'LL SLOW DOWN.

SO IF I DON'T ALLOW THEM TO DRAW AS MUCH CURRENT AS THEY

WANT, THEY WILL SLOW DOWN. SO I CAN DO THAT CURRENT STARVING BY VOLTAGE OR BY CURRENT, BASICALLY, SO I CAN ADJUST THE FREQUENCY.

SO LET'S SAY IT'S DESIGNED TO BE 2 GIGAHERTZ. YOU SAY THAT'S TOO FAST, I DON'T WANT IT 2. WELL, I WILL STARVE IT UNTIL IT IS 1 GIGAHERTZ.

Q. AND IS THERE ANY ELECTRONIC CIRCUITRY THAT YOU COULD USE TO CHANGE THE VOLTAGE OF THE RING OSCILLATOR, TO CHANGE ITS SPEED?

A. THAT IS WHAT PLL DOES. AND I THINK WE'LL EXPLAIN IT LATER.

Q. WELL, LET'S TAKE A LOOK AT THE NEXT SLIDE, DDX-120. WHAT ARE THESE COMPONENTS?

A. THOSE ARE THE COMPONENTS OF THE PLL, AND I WILL EXPLAIN HOW PLL DOES IT.

THE OUTPUT OF THIS FILTER IS ACTUALLY THAT VOLTAGE OF CURRENT WHICH WILL START IT AND MAKE IT RUN AT THE FREQUENCY THAT THIS CURRENT DETERMINES (INDICATING).

SO WHATEVER COMES OUT OF HERE, THE VOLTAGE OR CURRENT, THE CURRENT STARTS THE RING OSCILLATOR, WILL MAKE IT RUN FASTER OR SLOWER (INDICATING).

AND REMEMBER, THIS IS A VOLTAGE THAT COMES OUT HERE (INDICATING). THIS IS NOT THE CLOCK. THIS IS THE VOLTAGE THAT CONTROLS THIS. OKAY?

Q. SO I SEE YOU'RE STILL USING, IN THIS SLIDE, DDX-121, YOU

STILL HAVE A RING OSCILLATOR.

A. YES.

Q. WHAT IS THE RING OSCILLATOR DOING IN THIS SLIDE?

A. THE RING OSCILLATOR IS HAPPILY CLOCKING THE CPU.

Q. OKAY.

A. OKAY. AND SO I HAVE A FREQUENCY DIVIDER.

AS MR. HAROUN FROM TI EXPLAINED, THE FREQUENCY CAN BE DIVIDED.

AND HE ALSO SAID AT ONE POINT IT CANNOT BE MULTIPLIED, WHICH I AGREE. THE CIRCUIT THAT MULTIPLIES THE FREQUENCY IS YET TO BE INVENTED, OKAY?

WE CAN DIVIDE IT. HOW DO WE DIVIDE IT? WE PASS IT THROUGH A DEVICE THAT WOULD JUST CHANGE EVERY OTHER CLOCK, AND THEN WE PASS THAT THROUGH A DEVICE THAT CHANGES EVERY OTHER CLOCK AND SO FORTH. SO WE DIVIDE BY 2 OR DIVIDE IT BY 4 AND WE CAN DIVIDE IT FURTHER.

SO THAT SIGNAL GOES TO THE FREQUENCY DIVIDER HERE (INDICATING).

WE MAY CHOSE NOT TO HAVE A DIVIDER. IF WE WANT TO KIND OF REGENERATE THE CLOCK, WE HAVE A SIGNAL THAT COULD COME IN HERE AND PHASE DETECTOR.

THE PHASE DETECTOR COMPARES THIS DIVIDED SIGNAL. SO LET'S SAY THIS IS RUNNING AT 1 GIGAHERTZ AND WE DIVIDE IT 100 TIMES. USUALLY THE NUMBER IS A BINARY NUMBER, SO IT'LL BE 64, 128, 256, 512, 1024, ONE OF THOSE. NOT -- 100 DOESN'T FIT IN THAT

RANGE, BUT LET'S SAY WE DIVIDE IT BY 100 JUST FOR SIMPLICITY.

AND SO I GET 10 MEGAHERTZ HERE. THIS 10 MEGAHERTZ I WILL COMPARE WITH SOME REFERENCE SIGNAL. AND WHY ARE WE DOING THAT IS BECAUSE WHAT I'M BUILDING HERE IS LIKE A CRUISE CONTROL FOR THAT FERRARI, SO I AM COMPARING THE SPEED AT WHICH FERRARI IS RUNNING TO SOME VALUE FOR WHICH I WANT TO SET IT TO RUN, OKAY?

AND LET'S SAY THIS VALUE IS MUCH LOWER, SO I CAN TO DIVIDE IT IN THIS CASE, BUT I DON'T HAVE TO.

SO I HAVE TO PUT SOME REFERENCE. LET'S SAY IF I SAY, OKAY, I WANT TO -- I WANT TO SET THAT CAR TO RUN AT 65, I HAVE TO HAVE SOMETHING THAT POINTS TO 65 SO WHEN THE SPEEDOMETER COMES TO 65, I WILL LOCK INTO 65. SO I HAVE TO HAVE REFERENCE. I CANNOT JUST SAY, "OKAY, RUN AT 65." IT DOESN'T KNOW.

Q. SO I THINK WE HEARD -- WE'VE HEARD DISCUSSION OF A REFERENCE BEFORE. WE HEARD MENTION OF A METRONOME. WHAT DOES A PLL USE FOR ITS REFERENCE?

A. A PLL USES EXTERNAL QUARTZ OSCILLATOR, NOT NECESSARILY, OKAY?

WHAT PLL -- WHAT WE WANT TO USE HERE IS SOME STABLE REFERENCE.

NOW, STABLE DEPENDS HOW STABLE YOU WANT IT TO BE.

Q. SO WHY DON'T WE TAKE A LOOK AT DDX-122 WHERE I THINK YOU'VE ILLUSTRATED THE IDEA OF USING A REFERENCE HERE.

WHAT DOES THAT SLIDE SHOW US?

A. OKAY. SO THIS SLIDE SHOWS NOW WE HAVE CONNECTED THE

POINTS, AND LET'S START FROM HERE.

I HAVE THIS ONE RUNNING AT 10 -- AT 1 GIGAHERTZ, DIVIDED BY 100, FOR EXAMPLE, BECAUSE THIS REFERENCE IS 10 MEGAHERTZ (INDICATING).

BASICALLY WHAT I WANT IS THIS FREQUENCY AND THIS TO BE THE SAME (INDICATING). WHY? BECAUSE I AM COMPARING THEM.

WELL, IF I AM DIVIDING THIS BY 100, I HAVE TO RUN THIS 100 TIMES FASTER, OKAY, THAN THE REFERENCE. AND WHY? BECAUSE I DON'T HAVE A FASTER REFERENCE THAN 10 MEGAHERTZ FOR EXAMPLE IN THIS CASE. THAT'S THE FASTEST I CAN HAVE.

IF I HAVE A STABLE REFERENCE AT 1 GIGAHERTZ, I WOULD NOT DIVIDE AT ALL. I WOULD JUST FEED IN, COMPARE WITH THAT ONE, AND, AND USE THAT 1 GIGAHERTZ REFERENCE TO RUN THE RING OSCILLATOR AT 1 GIGAHERTZ.

AND WE DO THAT OFTEN WHEN WE DO, LIKE, REGENERATION OF THE CLOCK. WHEN I HAVE A MULTIPLE PROCESSOR, MULTIPLE CHIPS AS MR. MOORE SAID, AND I DISTRIBUTE THE CLOCK, I WANT TO RESYNCHRONIZE SO EVERY CHIP IS THE SAME.

Q. SO I FORGOT TO ASK YOU SOMETHING ON THE PREVIOUS SLIDE THAT I WANT TO ASK YOU ABOUT, WHICH IS I SEE SEVERAL COMPONENTS HERE, AND I -- THERE ARE NO CONNECTIONS ON DDX-121.

DO ALL OF THOSE COMPONENTS RECEIVE POWER?

A. YES.

Q. DESPITE -- DESPITE NOT SEEING ANY CONNECTIONS ON HERE?

A. YES. EVERYTHING RECEIVES POWER AND WE DON'T PUT THAT ON

THE SCHEMATICS BECAUSE IT WOULD BE REDUNDANT. OKAY. PUT IT POWER HERE, POWER HERE, POWER HERE, OVER THERE AT EVERY POINT (INDICATING). SO IT'S AN ASSUMPTION.

Q. OKAY. SO TURNING BACK NOW TO THIS FIGURE, NOW I SEE THAT THE GREEN ARROW AND THE RING OSCILLATOR ARE STILL THERE. WHAT ARE THE RING OSCILLATOR -- WHAT IS THE RING OSCILLATOR DOING IN THIS SLIDE, DDX-122?

A. THE RING OSCILLATOR IS CLOCKING THE CPU, AND AS I SAID HERE, AT 1 GIGAHERTZ.

NOW, LET ME GO AND EXPLAIN IT FURTHER. SO WHAT I WANT TO EXPLAIN IS THOSE TWO FREQUENCIES HAVE TO BE THE SAME, THOSE TWO ARE THE SAME, BECAUSE THIS IS MY REFERENCE (INDICATING). THIS IS MY 65 (INDICATING).

SO JUST LIKE YOU WANT TO SET YOUR FERRARI TO 130 AND YOU DIVIDE THE SPEED OF A FERRARI TWICE, SO HALF, AND YOU COMPARE 65, OKAY?

WELL, WHEN 65 -- WHEN IT COMES TO THIS POINT, THE 65, THIS IS RUNNING AT 130 ACTUALLY, BUT THAT'S WHY YOU DIVIDE IT (INDICATING). OKAY? SO THESE TWO FREQUENCIES ARE THE SAME (INDICATING).

NOW, IF THIS FREQUENCY START DRIFTING, IT'S BECOMING FASTER OR SLOWER, THIS COMPARATOR WHICH COMPARES THEM, THEY'RE BOTH 10 MEGAHERTZ HERE AND LOOK AT THEM AND SEE IF THEY ARE EQUAL (INDICATING).

IF IT SEES INEQUALITY, THEY'RE NOT THE SAME, IT CREATES A

SIGNAL HERE WHICH GETS FILTERED OUT BECAUSE WE DON'T WANT TO CHANGE IT TOO RAPIDLY --

Q. LET ME STOP YOU THERE. YOU SAID YOU HAVE A SIGNAL HERE. THERE'S A BLACK ARROW (INDICATING). WHAT IS THE BLACK ARROW COMING FROM THE PHASE DETECTOR?

A. IT IS A VOLTAGE, BUT IT'S KIND OF A PULSATING VOLTAGE BASED ON THE AVERAGE.

Q. IS THAT A CLOCK SIGNAL, THE BLACK ARROW?

A. NO.

Q. OKAY.

A. IT'S A PULSATING VOLTAGE WHICH IS WHAT IS CALLED THE ERROR, THE ERROR VOLTAGE. THE ARROW IS IF THOSE TWO SIGNALS ARE NOT RUNNING THE SAME, I HAVE AN ERROR.

NOW, THIS ERROR FILTER (INDICATING), IT SMOOTHED IT AND WILL, WILL YANK THIS RING OSCILLATOR, MOVE IT UP OR DOWN DEPENDING ON THE ERROR (INDICATING), SAY, OKAY, YOU'RE RUNNING TOO FAST, SLOW DOWN, AND IT SLOWS IT DOWN UNTIL THOSE TWO MATCH (INDICATING).

Q. SO LET ME MAKE SURE I UNDERSTAND SOMETHING VERY IMPORTANT FOR THIS CASE. THIS SIGNAL HERE, THIS LAST BLACK ARROW GOING FROM THE FILTER TO THE RING OSCILLATOR, WHAT IS THAT (INDICATING)?

A. THAT IS VOLTAGE.

Q. AND YOU SAID IT'S A SMOOTHED VOLTAGE. WHAT DO YOU MEAN BY THAT?

A. IT IS A SMOOTH VOLTAGE BECAUSE WE HAVE THE ERROR VOLTAGE HERE AND IT GETS SMOOTHED, FILTERED, BECAUSE WE DON'T WANT TO JERK THAT RING OSCILLATOR TOO FAST, OR TOO MUCH, YOU KNOW, BECAUSE IT'LL BE JITTERY (INDICATING).

SO WE SMOOTH THAT VOLTAGE SO IT WILL KIND OF GENTLY PUSH IT BACK OR PUSH IT FORWARD GENTLY, OKAY? THAT'S WHAT YOU WANT TO DO. WE WANT TO BE GENTLE PEOPLE.

OKAY. SO TO ADJUST IT GENTLY, SAY, HEY, YOU'RE RUNNING TOO FAST, SLOW DOWN A LITTLE BIT. OKAY?

AND, WELL, IT SLOWS TOO MUCH. SAY, WELL, I CAN SEE THE DIFFERENCE HERE. WELL, PRODUCE THE VOLTAGE AND SAY, OKAY, NOW GO A LITTLE FASTER.

SO THIS -- WHAT PLL DOES IS BASICALLY LIKE A CRUISE CONTROL, COMPARES THIS SPEED TO SOME REFERENCE POINT AND ADJUSTS THE SPEED OF THE RING OSCILLATOR TO WITHIN THAT REFERENCE.

SO LET'S SAY THIS IS A CRUISE CONTROL AND THIS IS A 65 MILE AN HOUR SPEED. MY REFERENCE IS 1 MILE AN HOUR HERE (INDICATING). I DIVIDED THAT BY 65, I HAVE 1 MILE HERE, I'M COMPARING THEM, THEY'RE EQUAL, THAT'S FINE.

THIS ONE DOUBLES THE SPEED, JUMPS TO 130. I DIVIDED THIS IS 2 MILE AN HOUR, THIS IS 1 MILE AN HOUR SPEED HERE COMPARED (INDICATING), SAY, OH, YOU'RE GOING TOO FAST, PRODUCE THE ERROR VOLTAGE, THAT VOLTAGE TELLS IT TO SLOW DOWN UNTIL IT GETS TO 65 (INDICATING).

NOW THEY'RE EQUAL, NOW THERE'S NO ERROR, THERE'S NO ADJUSTMENT.

Q. LET ME TURN TO DDX-123 WHERE I THINK YOU'VE ILLUSTRATED HERE A MATHEMATICAL EQUATION. WHAT DOES THIS TELL US?

A. WELL, THIS JUST INSTEAD OF 1 GIGAHERTZ, WHICH I USED, USES 2 GIGAHERTZ. SO LET'S SAY THIS IS 20 MEGAHERTZ REFERENCE. IF I HAVE A REFERENCE OF 20, I HAVE TO DIVIDE THAT UNTIL I GET 20 HERE, OKAY, TO BE EQUAL, BECAUSE I'M COMPARING TWO THINGS THAT ARE EQUAL.

Q. AND WHAT COMPONENT DOES THAT DIVISION?

A. THE FREQUENCY DIVIDER.

NOW, WHY DO I HAVE TO DIVIDE IT? AS I SAID, BECAUSE THE EXTERNAL REFERENCE, I COULD PHYSICALLY HAVE IT MUCH SLOWER, MUCH SLOWER THAN THE ONE.

IF I HAVE A 2 GIGAHERTZ, A GOOD 2 GIGAHERTZ STABLE FREQUENCY HERE, I WOULD NOT NEED TO DIVIDE. I JUST DIVIDE -- I JUST COMPARE THEM DIRECTLY.

BUT BECAUSE THIS REFERENCE IS SLOWER, I HAVE TO DIVIDE IT TO MATCH.

NOW, LET ME JUST SAY SOMETHING ELSE ABOUT WHAT I HEARD DURING THE OTHER TESTIMONY WHEN THE SECRET FORMULAS WERE SHOWN HERE, OKAY?

YOU CAN BASICALLY -- I CAN DIVIDE, I CAN DO DIVIDER HERE, TOO (INDICATING), AND I HAVE A DIVIDER OVER HERE AND I CAN HAVE SOME RELATIONSHIP (INDICATING).

OKAY. THIS IS WHAT THE SECRET FORMULAS ARE (INDICATING), WHICH YOU CAN FIND IN EVERY TEXTBOOK, BY THE WAY.

WHAT THE ESSENCE IS, THIS FREQUENCY AND THIS HAVE TO BE THE SAME (INDICATING).

SO YOU CREATE A RELATIONSHIP IN WHICH THOSE TWO MATCH SO THEY CAN BE COMPARED, BECAUSE I CANNOT COMPARE IF I DIVIDE THIS BY 200 AND I GET 10 MEGAHERTZ HERE AND 20 MEGAHERTZ HERE, THEY'RE NOT THE SAME (INDICATING). THEY'RE OBVIOUSLY NOT THE SAME. I HAVE TO BRING THEM TO THE SAME SO I CAN SEE THE DRIFTS.

SO IF I DIVIDE THIS ONE BY 10, FOR EXAMPLE, THEN I WOULD HAVE IN THAT SECRET FORMULA (INDICATING). I WOULD HAVE -- LET ME SEE.

NO. IF I DIVIDE IT BY 2, THEN I WOULD DIVIDE THIS BY 2 (INDICATING).

SO THIS WAS A FACTOR N IN THE SECRET FORMULA AND THIS IS THE FACTOR M IN THE SECRET FORMULA, SO YOU GET M DIVIDED BY N.

OR I CAN CONVERT IT AND MAKE IT MULTIPLY BY 1 OR M OVER N AND THEN HE PLAYED THIS MATHEMATIC TO TRY TO PROVE YOU ALMOST EVERYTHING.

BUT BASICALLY JUST REMEMBER, THIS AND THIS ARE EQUAL (INDICATING).

Q. SO I WANT TO MAKE SURE I DIDN'T GET LOST IN THE MATH THERE. YOU'RE SAYING THAT IT'S POSSIBLE TO REWRITE THIS AS A MULTIPLICATION? IS THAT WHAT YOU MEAN?

A. YES. I CAN MULTIPLY THIS BY 1 OVER 100 AND I WOULD SAY (INDICATING), OH, THIS MULTIPLIES.

WELL, WHEN YOU MULTIPLY SOMETHING WITH 1 OVER 100, IT'S GOING TO DIVIDE BY 100.

Q. SO WHY DON'T YOU WRITE IT THAT WAY HERE IN DDX-123?

A. WHY DID I?

Q. WHY DID YOU NOT WRITE IT AS A MULTIPLICATION PROBLEM IN DDX-123?

A. BECAUSE I'M NOT TRYING TO CONFUSE ANYONE HERE. THAT'S WHY. THAT'S NORMAL WAY YOU WRITE IT.

Q. AND LET ME ASK YOU THIS --

A. IF I'M TRYING TO, TO CONTORT THIS SO IT LOOKS LIKE IT'S MULTIPLICATION, I WOULD MULTIPLY THIS BY 1 OVER 100.

Q. SO LET ME -- LET ME MAKE SURE I UNDERSTAND. MULTIPLICATION IS EASIER FOR ME. WHY NOT JUST TAKE THIS 20 MEGAHERTZ SIGNAL FROM THE CRYSTAL AND MULTIPLY IT BY 100 TO GET YOUR 2 GIGAHERTZ? WHY WOULDN'T I JUST DO THAT?

A. BECAUSE THERE IS NO CIRCUIT LIKE THAT THAT CAN MULTIPLY. YOU CAN DIVIDE. YOU CAN DIVIDE THE FREQUENCY. BUT WE CANNOT MULTIPLY. THERE IS NO CIRCUIT LIKE THAT, AND I THINK MR. HAROUN ADMITTED THAT.

SO I HAVE 20 MEGAHERTZ. THE ONLY WAY I CAN MAKE -- THAT I CAN CREATE OR I CAN CONTROL THE HIGHER FREQUENCY HERE IS BY, BY USING THE PLL.

Q. WHAT ABOUT THIS: WHY WOULDN'T I JUST GO OUT AND GET A 2

GIGAHERTZ CRYSTAL CLOCK?

A. NUMBER ONE, IF YOU CAN FIND ONE, OKAY, THAT WOULD BE GREAT. BUT YOU CAN'T.

NUMBER TWO, LET'S SAY I DON'T -- IT DOESN'T HAVE TO BE A CRYSTAL, OKAY? IT COULD BE A REFERENCE.

AND AS FAR AS -- IN MY RADIO HOBBIES, IF I WANT A REAL STABLE REFERENCE, WE TAKE THE SIGNAL FROM THE GPS FROM THE SATELLITE WHICH IS REALLY STABLE TO 1 HERTZ, AND I WILL FEED THAT AS A REFERENCE, FOR EXAMPLE.

BUT LET'S SAY SOMEHOW I HAVE A STABLE 2 GIGAHERTZ REFERENCE HERE. IT IS ALSO HARD TO PUSH IT THROUGH THIS PIN ON THE CHIP (INDICATING) BECAUSE THOSE ARE VERY HIGH FREQUENCIES AND, AND IT IS NOT EASY AND IT CONSUMES POWER.

AND, FOR EXAMPLE, YOU KNOW, ONE THING THAT A DDR MEMORIES THAT YOU'RE BUYING FOR YOUR P.C.'S, THEY RUN AT -- I THINK THE HIGHEST THEY MAKE IS 1033 GIGAHERTZ, BUT THIS IS A DDR, DOUBLE CLOCK, MEANING THAT THE REAL FREQUENCY IS ABOUT 500 MEGAHERTZ.

AND THEY HAVE HEAT SYNCH, AS YOU KNOW, WHEN YOU PUT IT IN YOUR PROCESSOR OR YOUR COMPUTER OR WHATEVER.

SO IT'S NOT EASY TO PUSH THE HIGH FREQUENCY ON THE CHIP DIRECTLY.

Q. SO LET ME ASK YOU THIS: I WANT TO MAKE SURE THAT I UNDERSTAND BECAUSE THIS IS A VERY IMPORTANT ISSUE FOR THIS CASE.

ON THIS FIGURE, DDX-123, WHAT COMPONENT GENERATES THE

CLOCK SIGNAL THAT CLOCKS THE CPU?

A. I HOPE I WAS CLEAR IN EXPLAINING THE RING OSCILLATOR AND HOW A RING OSCILLATOR GENERATES THE SIGNAL AND I HOPE THE JURY UNDERSTANDS IT'S LIKE A DOG CHASING THE TAIL, OKAY. THAT'S THOSE 0'S AND 1'S ARE CHASING EACH OTHER. THIS IS THIS PIECE HERE, WHICH IS DIRECTLY CONNECTED TO THE CPU AND CLOCKS THE CPU (INDICATING).

Q. DOES THE -- DOES THE CRYSTAL OFF OF THE CHIP HAVE ANY ROLE IN GENERATING THE CLOCK SIGNAL?

A. NO.

Q. THAT CLOCKS THE CPU?

A. THAT'S WHY I ASKED YOU TO MOVE A COUPLE OF SLIDES BACK, AND IF YOU WANT, YOU CAN DO IT AGAIN.

LET'S MOVE TO THE RING OSCILLATOR SLIDE.

Q. WELL, RATHER THAN GOING BACK, I JUST WANT TO MAKE SURE THAT I UNDERSTAND. YOU SAID THAT THE RING OSCILLATOR GENERATES THE CLOCK. DOES THE RING OSCILLATOR RELY ON THE CRYSTAL TO GENERATE THE CLOCK SIGNAL THAT CLOCKS THE CPU?

A. NO. THE RING OSCILLATOR GENERATES THE CLOCK REGARDLESS, AND IT WILL CONTINUE TO GENERATE THE CLOCK EVEN WHEN YOU DISCONNECT THIS, THIS CRYSTAL.

Q. DOES ANY ON-CHIP COMPONENT RELY ON THE OFF-CHIP CRYSTAL TO GENERATE A CLOCK SIGNAL?

A. NO. CLOCK SIGNAL -- THIS CRYSTAL IS A REFERENCE (INDICATING).

Q. AND YOU WERE HERE -- I THINK YOU MENTIONED BEFORE YOU HEARD THE TESTIMONY FROM DR. HAROUN OF TI; RIGHT?
A. RIGHT.
Q. AND IS TEXAS INSTRUMENTS A PARTY TO THIS LITIGATION?
A. YES, IT IS.
Q. ARE THEY -- ARE THEY ONE OF THE PARTIES IN THE LITIGATION?
A. I DON'T KNOW IF THEY ARE PARTIES, BUT THEIR PROCESSOR IS BEING USED.
Q. AND DR. HAROUN -- WAS WHAT YOU JUST SAID -- DID DR. HAROUN SAY ANYTHING INCONSISTENT WITH WHAT YOU JUST TOLD US ABOUT GENERATING THE CLOCK SIGNAL?
A. YES. THERE ARE AT LEAST TWO INCONSISTENCIES WITH WHAT HE SAID.

ONE, HE WAS TRYING TO SAY HOW THIS CLOCK GOES AND CLOCKS THE CPU, AND THEN -- BUT IN THE WAY HE SAID, WELL, THE FIRST ONE GOES THROUGH AND THEN IT CONTINUES HUNDRED TIMES AND THEN THE FIRST ONE GOES THROUGH AND CONTINUES HUNDRED TIMES.

WHERE? MY QUESTION WAS, WHERE? HOW DOES IT GO? WHERE IS THE PATH? IT STOPS RIGHT HERE (INDICATING).

AND HERE IS THE VOLTAGE (INDICATING). YOU DON'T SEE THE CLOCK CONNECTION GOING TO THE CPU AT ALL.

SO THAT JUST DOESN'T FIT THE PRINCIPLES OF HOW A PLL OPERATES SIMPLY. AND IT'S IN EVERY TEXTBOOK.

Q. AND WHEN YOU SAID IT STOPS RIGHT HERE (INDICATING), WHAT DID YOU MEAN?

A. BECAUSE THIS IS -- THIS IS A CLOCK SIGNAL, OKAY? IT GOES LIKE THIS, OKAY (INDICATING). IT COMES HERE (INDICATING), IT IS COMPARED WITH THAT ONE (INDICATING).

WHAT COMES OUT IS VOLTAGE, AND THAT VOLTAGE IS SMOOTH THAT COMES OUT OF HERE (INDICATING).

THERE'S NO CONNECTION WHERE THAT CLOCK CAN GO AND JUMP OVER AND GO TO THE CPU. THERE ISN'T.

Q. WHAT WOULD HAPPEN TO THE RING OSCILLATOR IF YOU DISCONNECTED THE CRYSTAL?

A. IF YOU DISCONNECT, IT WILL RUN AT THE FREQUENCY AT WHICH IT WILL RUN WITHOUT THIS CURRENT STARVING REGULATION MAKING IT, SOMETHING THAT IS IN THERE.

AS A MATTER OF FACT, IF YOU LOOK AT THE SPECS OF THE QUALCOMM CHIP, THEY SAY IF VARYING OSCILLATOR RUNS FROM 200 TO 1.4 GIGAHERTZ, FOR EXAMPLE, MEANING OKAY, IF YOU DISCONNECT, WE'LL RUN AT 200.

Q. SO THE RING OSCILLATOR WILL STILL RUN IF YOU DISCONNECT THE CRYSTAL?

A. YES, BECAUSE CRYSTAL IS NOT ESSENTIAL TO GENERATE THE CLOCK. CRYSTAL IS NOT NEEDED TO GENERATE THE CLOCK. IT GENERATES THE CLOCK BY ITSELF. GENERATION OF THE CLOCK MEANS PRODUCING THE SIGNAL OF THE ALTERNATING OUTPUT.

Q. YOU MENTIONED QUALCOMM. LET'S TAKE A LOOK AT A QUALCOMM PLL IN DDX-124. WHAT IS THIS FIGURE SHOWING US?

A. OKAY. WHAT THIS FIGURE SHOWS IS A PLL. IT MAY LOOK

COMPLICATED, BUT REALLY IT ISN'T, OKAY, AND I WILL WALK YOU THROUGH.

IT HAS -- ACTUALLY IT'S TWO PLL'S IN ONE KIND OF. IT HAS TWO RING OSCILLATORS (INDICATING), AND --

Q. LET ME STOP YOU THERE. THE RING OSCILLATORS, YOU'RE POINTING TO THE BLUE BOXES HERE (INDICATING)?

A. THE BLUE BOX WHICH SHOWS THOSE INVERTERS WHICH LOOK NICE, RIGHT, ARE ARRANGING IN THE ODD NUMBER, 1, 2, 3, 4, 5, OKAY. THE TWO OF THEM (INDICATING).

SO THIS IS WHAT PRODUCES THE CLOCK, THAT GENERATES THE CLOCK (INDICATING); THIS IS CONNECTED TO THE PLL OUT (INDICATING); THIS GOES TO THE PROCESSOR OF --

Q. WHAT IS THE PLL OUT?

A. PLL OUT IS THE CLOCK THAT CLOCKS THE PROCESSOR. SO THIS, IN THIS CASE, IS CONNECTED AND CLOCKS THE PROCESSOR, OKAY (INDICATING)?

HERE IS THE REGULATION, OKAY? THIS PART IS ADJUSTING IT (INDICATING).

AND THE OTHER THING MR. HAROUN KEPT SAYING IS IT'S A DIGITAL PLL.

AND DON'T GET CONFUSED. WHAT DIGITAL MEANS, IT HAS THIS REGULATION WHICH IS A DIGITAL SIGNAL, BUT WHAT HE CONVENIENTLY FORGET TO MENTION, IT GOES TO DIGITAL THROUGH ANALOG CONVERTER WHICH CONVERTS THAT TO VOLTAGE OR CURRENT.

SO BASICALLY WHAT REGULATES THIS IS VOLTAGE AND CURRENT,

SAME THING.

Q. WHERE IS THE DIGITAL TO ANALOG CONVERTER HERE?

A. IT SAYS DAC. DAC MEANS DIGITAL TO ANALOG CONVERTER, THE COMPONENT HERE (INDICATING).

SO THIS OUTPUT OPERATION TO EXTEND THE DIGITAL SIGNAL TO DAC, THIS DAC JUST MAKES THE PLAIN VOLTAGE OUT (INDICATING), THIS VOLTAGE WHICH COMES FROM HERE (INDICATING), AND PRODUCES THIS VOLTAGE WHICH WILL SMOOTHLY MOVE THIS ONE IN THE RANGE WE WANT IT TO OSCILLATE (INDICATING).

NOW, LET ME GO BACK JUST ONE SECOND. THIS IS A DIVIDER (INDICATING), AND THIS IS A COMPARATOR (INDICATING). THIS IS WHAT IS CALLED A PHASE DETECTOR (INDICATING).

HERE IS THE REFERENCE (INDICATING). THIS REFERENCE IS COMPARED WITH THE DIVIDED SIGNAL HERE, AND WHAT IT DOES IS, YOU CAN SEE THE SWITCHES, IT EITHER MOVES THIS VOLTAGE UP OR DOWN.

THESE CAPACITORS HAVE BEEN CHARGED AND THEY FILTER THAT VOLTAGE SO IT'S NOT JUMPING UP AND DOWN, SO IT'S SMOOTH, THAT VOLTAGE, OKAY, WHEN CONNECTED.

AND IN CASE THIS IS DISCONNECTED, BUT WHEN CONNECTED, IT'S CONVERTED INTO A CURRENT, SOME WITH WHAT DIGITAL PLL DOES, OR DIGITAL OUTPUT, SAME THING, VOLTAGE, AND IT WILL ADJUST THIS VCO, VOLTAGE CONTROL OSCILLATOR, RING OSCILLATOR.

Q. SO IN THIS FIGURE, DDX-124 FROM EXHIBIT 407, WHAT IS POWERING THE RING OSCILLATOR THAT'S GENERATING THE CLOCK SIGNAL PLL OUT?

A. WHAT IS POWERING? IT'S A POWER SUPPLY THAT IS CONNECTED.
Q. AND CAN YOU SHOW US WHERE THE POWER SUPPLY IS CONNECTED TO THE RING OSCILLATOR?
A. AS I SAID, EVERYTHING RECEIVES POWER SUPPLY, BUT IT'S NOT CONNECTED. IT'S REDUNDANT AND ASSUMED AND WE ALL KNOW WE HAVE TO CONNECT IT TO POWER IN ORDER TO WORK.
Q. IN THIS FIGURE, YOU MENTIONED THAT TCXO IS A REFERENCE. IS THAT REFERENCE AFFECTING THE RING OSCILLATOR THAT GENERATED PLL OUT IN ANY WAY?
A. IN THIS PARTICULAR FIGURE, WHICH COMES FROM QUALCOMM, OKAY, YOU SEE THAT THIS CURRENT, VOLTAGE TO CURRENT THROUGH INVERTER, IS CONNECTED TO A FIXED VOLTAGE. THIS FIXED VOLTAGE PRODUCES A CURRENT, THIS ONE IS DISCONNECTED (INDICATING), WHICH WILL SET THAT TO CERTAIN FREQUENCY. SO THIS ONE IS RUNNING AT THAT FREQUENCY, OKAY (INDICATING).

AND WHAT I DO IS ACTUALLY -- WHY THEY HAVE THIS, THEY'RE PREPARING, SETTING UP THIS ONE TO RUN AT A CERTAIN FREQUENCY, AND IT'S RUNNING WITHOUT BEING IN PLL, BASICALLY (INDICATING). IT'S DISCONNECTED FROM A PLL. AND THIS IS DISCONNECTED (INDICATING). THIS IS DISCONNECTED (INDICATING). THIS IS DISCONNECTED (INDICATING).

IT'S RUNNING BY ITSELF IN THE PLL. IT'S GENERATING THE CLOCK SIGNAL. ONCE THEY SET IT IN THE RANGE THEY WANT, THEY WILL SWITCH TO IT.

OR THEY WILL SWITCH TO ANOTHER ONE. THERE ARE TWO PLL'S

WAY THEY ARE PRODUCED.

NOW, BINNING TAKES ADVANTAGE OF THESE VARIATIONS THAT THEY VARY TOGETHER AND IT PUTS THEM IN THE PROPER BINS.

Q. SO LET'S TAKE A LOOK AT THE ANIMATION HERE ON DDX-128, AND CAN YOU TELL US WHAT DOES THIS SLIDE SHOW?

A. WELL, WHAT WE HAVE IN THIS ANIMATION, WE HAVE, YOU KNOW, THE ONE FROM THE SLOWER BINS RUNS SLOWER, THE ONE FROM THE FASTER BIN WILL RUN FASTER WHEN YOU, YOU KNOW, USE THAT CHIP.

AND THEN WE HAVE THE I/O INTERFACE RUNNING AT A FIXED SPEED DETERMINED BY THE EXTERNAL CLOCK INDEPENDENT OF THE FIRST CLOCK.

Q. NOW, DOES BINNING AFFECT ANY OF THE COMPONENTS ON THE CHIP ILLUSTRATED HERE IN DDX-128?

A. IT DOES IN THE WAY THAT THE FASTER BIN HAS FASTER CHIPS OR FASTER COMPONENTS AND SLOWER BIN HAS SLOWER COMPONENTS.

Q. SO WHICH COMPONENTS ON THE CHIP ARE AFFECTED BY INNING?

A. THE TRANSISTORS, AS I SAID, THE BUILDING BLOCKS.

Q. AND THOSE ARE THE BUILDING BLOCKS ON WHICH COMPONENT?

A. EVERYTHING IS BUILT FROM EVERYTHING FROM TRANSISTORS, SO RING OSCILLATOR IS BUILT FROM TRANSISTORS, THE CPU IS BUILT FROM TRANSISTORS, REGISTER FILE IS BUILT FROM TRANSISTORS, LATCHES ARE BUILT FROM TRANSISTORS.

SO IF TRANSISTORS ARE FASTER, ALL OF THE ABOVE ARE FASTER. IF TRANSISTORS ARE SLOWER, THEY ARE SLOWER.

Q. SO I WANT TO ASK YOU THIS: WE TALKED ABOUT A PLL EARLIER.

IS THERE A GOOD ANALOGY TO EXPLAIN A PLL AND WHAT IT DOES? ARE YOU AWARE OF A GOOD COMPARISON?

A. WELL, YOU KNOW, I THINK WE USED CRUISE CONTROL AS AN ANALOGY, AND --

Q. SO LET'S TAKE A LOOK AT DDX-131. WHAT IS SHOWN HERE?

A. WELL, I THINK MY OPPONENTS USED THE ANALOGY OF CRUISE CONTROL, BUT I THINK I CAME TO THAT REALLY AT THE FIRST DEPOSITION. I WAS DRIVING THROUGH TEXAS AND, YOU KNOW, TEXAS IS HILLY, AND I ALREADY HAD ONE BIG SPEEDING TICKET IN TEXAS, SO I SET IT ON CRUISE CONTROL AND I WAS VERY NERVOUS. I MEAN, WHEN THE CAR GOES DOWNHILL.

BUT THE CRUISE CONTROL VARIES BY, YOU KNOW, SOME FIVE, SEVEN MILES, OKAY? AND I SET IT RIGHT KIND OF ABOVE THE SPEED LIMIT, JUST I KNOW THEY WILL NOT STOP ME FOR THAT, SO A FEW MORE MILES, IT'S ALL GOOD.

AND I USE THIS ANALOGY. SO YOU CAN SET, SET YOUR REFERENCE, WHICH IS HOW I SET MY REFERENCE.

BUT YOUR, YOUR SPEED WILL VARY DEPENDING ON THE CONDITIONS.

Q. AND SO GOING UP A HILL, HOW DOES THAT RELATE, IF AT ALL, TO A PLL?

A. WELL, THE CRUISE CONTROL WILL STILL -- YOU KNOW, EVEN THOUGH -- IT'LL KICK -- YOUR CAR WILL SLOW DOWN, BUT THE CRUISE CONTROL WILL KICK IT UP TO RUN FASTER, SO YOU WILL SEE YOUR ENGINE REVVING.

Q. OKAY. AND WHEN YOU'RE ON THE FLAT GROUND, WHAT HAPPENS?
A. WHEN YOU'RE ON THE FLAT, LET'S SAY IF THERE ARE NO OTHER PARAMETERS AFFECTING IT, LIKE IT DOESN'T START RAINING OR WIND, IT WILL RUN RELATIVELY SMOOTH.
Q. AND WHAT ABOUT DOWNHILL?
A. WHEN YOU'RE DOWNHILL, YOU HAVE TO WATCH, OKAY, I MEAN, BECAUSE IT'LL SPEED UP.
Q. HOW DOES THAT RELATE TO A PLL, IF AT ALL?
A. WELL, THE PLL IS A REGULATOR, JUST LIKE CRUISE CONTROL. SO A PLL COMPARES THE SPEED OF THE RING OSCILLATOR TO THE REFERENCE, AND WHEN IT SEES THAT IT IS RUNNING FAST, IT WILL SLOW IT DOWN BY VOLTAGE. CURRENT STARVE IT AND IT'LL SLOW DOWN BECAUSE IT'LL BE STARVED, OKAY?

WHEN IT NEEDS IT TO SPEED UP, WHEN IT SEES THAT IT'S LAGGING BEHIND BY PHASE COMPARATOR -- WHAT A PHASE COMPARATOR DOES, IT WILL GIVE MORE JUICE TO RUN UP, JUST LIKE I THINK CRUISE CONTROL DOES WITH YOUR CAR ENGINE.

Q. DOES THE CRUISE CONTROL GENERATE THE POWER FOR THE CAR?
A. NO. YOUR -- YOU KNOW, YOUR ENGINE GENERATES THE POWER FOR YOUR CAR, NOT THE CRUISE CONTROL.
Q. OKAY. I WANT TO MOVE ON FOR A MINUTE AND TALK ABOUT THE PATENT AT ISSUE IN THIS CASE, THE '336 PATENT.

ARE YOU FAMILIAR WITH THIS PATENT? IT'S SHOWN HERE IN DDX-138.
A. YES, I'M QUITE FAMILIAR WITH THIS PATENT.

Q. AND AS PART OF YOUR WORK IN THIS CASE, HAVE YOU REVIEWED THIS PATENT?

A. YES, I HAVE REVIEWED THIS PATENT MANY TIMES.

Q. AND DID -- SIR, DO YOU HAVE AN OPINION ABOUT THE QUALITY OF THIS PATENT AT ALL?

A. THAT'S A LOADED QUESTION. GENERALLY -- I'M A TECHNICAL EXPERT. I AM SUPPOSED TO BE INDEPENDENT AND I AM TRYING MY BEST NOT TO HAVE OPINION.

NOW, AS FAR AS THIS PATENT IS CONCERNED, AS FAR AS THE PATENT --

MR. SMITH: YOUR HONOR, I HATE TO INTERRUPT THE WITNESS. HE JUST SAID HE'S A TECHNICAL EXPERT. HE'S NOT A LEGAL EXPERT, SO IF HE'S GOING TO OFFER AN OPINION ON ANYTHING LEGAL, IT'S BEYOND THE BOUNDS.

THE COURT: MR. MARSH, DO YOU WANT TO RESPOND?

MR. MARSH: LET ME REFRAME THE QUESTION IF I MAY, YOUR HONOR.

THE COURT: OKAY. YOU MAY WITHDRAW THE QUESTION AND FORM ANOTHER QUESTION.

MR. MARSH: THANK YOU.

THE COURT: THE OBJECTION IS SUSTAINED. GO AHEAD.

BY MR. MARSH:

Q. DR. OKLOBDZIJA, DO YOU HAVE AN OPINION ABOUT THE TECHNICAL ASPECTS OF THIS PATENT AND THE QUALITY OF THOSE -- THE TECHNICAL DESCRIPTION IN THE PATENT AND THE TECHNOLOGY THAT IT

DESCRIBES?

A. I WOULD SAY IT'S A WIDE REACHING PATENT AND DESCRIBES THE TECHNOLOGY, MICROPROCESSOR TECHNOLOGY WHICH IS, AGAIN, WIDELY USED.

Q. WHEN YOU SAY "WIDELY USED," WHAT DO YOU MEAN BY THAT?

A. EVERYTHING HAS MICROPROCESSOR TODAY ALMOST.

Q. ARE THERE ANY MICROPROCESSORS THAT DON'T USE THE TECHNOLOGY IN THE '336 PATENT?

MR. SMITH: I'M GOING TO OBJECT, YOUR HONOR. IT'S WELL OUTSIDE HIS OPINION. HE'S NEVER OFFERED ON OPINION ON ALL MICROPROCESSORS.

THE COURT: MR. MARSH, YOU WANT TO RESPOND?

MR. MARSH: YES. DR. OKLOBDZIJA IS AN EXPERT IN MICROPROCESSOR DESIGN AND DIGITAL CLOCKING AND I THINK IT'S -- HE'S IN THE BEST POSITION TO EXPLAIN TO US WHAT THE STATE OF THE INDUSTRY IS AS TO MICROPROCESSORS.

THE COURT: IF I MIGHT SUGGEST, PERHAPS THIS WOULD BE AN EXCELLENT TIME TO TAKE OUR BREAK FOR THE AFTERNOON. WE CAN ADDRESS THIS WHILE THE JURY IS OUT.

WITH THAT, LADIES AND GENTLEMEN OF THE JURY, IT IS TIME FOR OUR AFTERNOON BREAK. DON'T DISCUSS THE CASE WHILE WE'RE OUT ON BREAK.

WE'LL SEE YOU BACK HERE IN ABOUT 10 OR 15 MINUTES.

(JURY OUT AT 2:42 P.M.)

THE COURT: ALL RIGHT. MR. SMITH, I BELIEVE YOU WERE

GOING TO REPLY.

MR. SMITH: YES, YOUR HONOR. I'M VERY -- I'M VERY CONCERNED RIGHT NOW. YOUR HONOR SPECIFICALLY -- A COUPLE POINTS. YOUR HONOR SPECIFICALLY WARNED US THE OTHER DAY AFTER MR. OTTESON COMPLAINED ABOUT CHARACTERIZATIONS OF THE PATENT AND NOW HE'S OFFERING GENERALIZATIONS ABOUT HOW THE TECHNOLOGY OF THE PATENT AND THE QUALITY OF THE PATENT, UNMOORED TO ANYTHING IN THE PATENT. SO THAT'S THE FIRST OBJECTION, AND I THINK IT MAY WARRANT A LIMITING INSTRUCTION.

AND NUMBER TWO, YOUR HONOR, FOR THIS EXPERT AND FOR MR. MARSH TO TRY TO ELICIT TESTIMONY THAT, EFFECTIVELY, EVERY MICROPROCESSOR THAT'S OUT THERE TODAY USES THE '336 PATENT, YOUR HONOR, WE NEED A LIMITING INSTRUCTION ON THAT.

WE'RE, WE'RE WAY OVER -- WE'RE WAY BEYOND THE BOUNDS AT THIS POINT. I MEAN, HE WAS GOING TO TESTIFY THAT EVERYTHING OPERATES WITH -- THAT WORKS WITH A MICROPROCESSOR USES THE '336 PATENT.

THE WITNESS: I WAS NOT GOING TO SAY THAT.

THE COURT: DR. OKLOBDZIJA -- DR. OKLOBDZIJA, IF I CAN ASK YOU TO REFRAIN FROM PARTICIPATING. I NEED TO FOCUS.

THE WITNESS: I WOULD NOT SAY THAT.

THE COURT: SIR, WITH ALL RESPECT, I NEED TO FOCUS ON THE LAWYERS FOR THIS CONVERSATION.

MR. SMITH: CERTAINLY IT WAS IMPLICIT WITH THE QUESTION.

BRING THE JURY IN, PLEASE.

THE CLERK: YES, YOUR HONOR.

THE COURT: THANK YOU.

(JURY IN AT 3:10 P.M.)

THE COURT: MEMBERS OF THE JURY, BEFORE WE BROKE, WE WERE HEARING TESTIMONY FROM DR. OKLOBDZIJA.

DR. OKLOBDZIJA, WOULD YOU RESUME YOUR PLACE ON THE WITNESS STAND? I WILL REMIND YOU YET AGAIN, SIR, THAT YOU REMAIN UNDER OATH.

THE WITNESS: YES, YOUR HONOR.

THE COURT: MR. MARSH, WHENEVER YOU'RE READY, YOU MAY RESUME YOUR EXAMINATION.

MR. MARSH: THANK YOU, YOUR HONOR.

Q. DR. O, BEFORE THE BREAK WE WERE TALKING ABOUT THE '336 PATENT. ARE YOU AWARE THAT THE '336 PATENT IS PART OF A PORTFOLIO OF PATENTS?

A. YES, I AM.

Q. AND WHAT PORTFOLIO IS THAT, SIR?

A. IT IS CALLED MMP PORTFOLIO.

Q. AND WHAT DOES MMP MEAN?

A. THE MOORE MICROPROCESSOR PATENT PORTFOLIO.

Q. AND DO YOU HAVE AN OPINION, SIR, AS TO THE RELATIVE VALUE OF THE '336 PATENT IN THAT PORTFOLIO?

I'M SORRY. LET ME ASK A DIFFERENT QUESTION FIRST.

DID YOU ANALYZE ANY OF THE OTHER PATENTS IN THE MMP

PORTFOLIO?

A. YES, I DID. I REVIEWED ALL OF THEM.

Q. AND DO YOU HAVE AN OPINION, SIR, AS TO THE RELATIVE VALUE OF THE '336 PATENT IN THE MMP PORTFOLIO?

A. YES. I THINK IT'S THE MOST VALUABLE OF ALL OF THE PATENTS.

Q. THANK YOU. I WANT TO TURN NOW TO DDX --

A. I WANT TO QUALIFY. IT'S MOST APPLICABLE. IT'S HARD TO VALUE A PATENT. I THINK IT'S -- SO I WON'T GET INTO THAT.

Q. OKAY. THANK YOU. LET'S TURN TO DDX-139. SO WHAT ARE YOU SHOWING US HERE ON THIS SLIDE, DR. O?

A. WHAT WE'RE SHOWING ARE THE CLAIMS OF THOSE, OF '336 PATENT WHICH HAVE BEEN ASSERTED AGAINST HTC CURRENTLY.

Q. AND I SEE -- WELL, LET ME BACK UP. WHAT ARE CLAIMS IN THE PATENT, JUST GENERALLY?

A. OKAY. THE CLAIMS ARE THE MOST IMPORTANT PART OF THE PATENT. THEY -- THEY DESCRIBE THE SCOPE OF THE PATENT. THEY DESCRIBE WHAT IT IS THAT THE PATENT IS CLAIMING THAT THE PATENT HAS INVENTED. THAT IS SUMMARIZED IN THE CLAIMS AND THAT IS THE RELEVANT PART.

AND WHEN -- AS AN EXPERT, WHEN I EXAMINE THE PATENT, I LOOK AT THE CLAIMS.

Q. AND I SEE HERE THAT YOU LIST TWO INDEPENDENT CLAIMS, INDEPENDENT CLAIM 6 AND INDEPENDENT CLAIM 13.

WHAT IS AN INDEPENDENT CLAIM?

A. AN INDEPENDENT CLAIM IS A CLAIM THAT CAN STAND BY ITSELF. SO -- YES.

Q. AND SO YOU ALSO LIST SOME DEPENDENT CLAIMS. WHAT ARE DEPENDENT CLAIMS?

A. DEPENDENT CLAIMS ARE THE CLAIMS THAT DEPEND ON THE OTHER CLAIMS, SO IN THIS CASE CLAIM 6 IS INDEPENDENT AND CLAIM 7 AND 9 DEPEND ON 6.

SO IF, FOR EXAMPLE, IN THE PATENT RE-EXAMINATIONS -- AND THIS, THIS HAD MANY -- IF THE EXAMINER WOULD FIND CLAIM 6 INVALID AND STRIKE IT, THEN THERE GOES 7 AND 9.

Q. SO I DON'T WANT TO FOCUS ON VALIDITY RIGHT NOW. THE PATENT'S PRESUMED VALID, YOU UNDERSTAND?

A. YES, I -- I AM AWARE THAT THE PATENT WENT THROUGH TWO RE-EXAMINATIONS. THERE WAS SIX REQUESTS, FOUR WERE GRANTED, THOSE FOUR WERE COMBINED INTO TWO, AND THERE WERE 600 REFERENCES THAT WERE ASSERTED AND THEY WERE EXAMINED AND THE PATENT STILL STANDS.

AND IN MY LONG HISTORY, I THINK I STARTED BY -- I DON'T KNOW IF I READ THE 600 REFERENCES, BUT I READ A LARGE PORTION OF THEM.

Q. THANK YOU. LET'S FOCUS ON INFRINGEMENT OF THESE CLAIMS THAT ARE LISTED HERE IN DDX-139. AND IN DDX-140, YOU HAVE WHAT YOU SAY IS A DIAGRAM OF CLAIMS 6 AND 13.

CAN YOU EXPLAIN WHAT THIS IS?

A. YES. IN THE DIAGRAM, I'M TRYING TO SIMPLIFY IT AND

PRESENT IT TO THE COURT IN A WAY THAT AN ORDINARY PERSON CAN UNDERSTAND. IT'S LIKE WHAT ARE THOSE CLAIMS 6 AND 13 ABOUT BASICALLY.

Q. SO THIS IS AN ILLUSTRATION OF THE ELEMENTS IN THE CLAIMS?

A. RIGHT. IT SAYS WE HAVE A SINGLE CHIP WHICH CONTAINS ONE CLOCK, FIRST CLOCK (INDICATING); THE CLOCK CPU (INDICATING); IT CONTAINS THE I/O INTERFACE CONNECTED BY A BUS WHICH HAS CONTROL, ADDRESS, AND DATA (INDICATING); AND THERE IS A SECOND CLOCK WHICH IS EXTERNAL TO THE CHIP (INDICATING), TO THE SILICON, CONNECTED TO THE MEMORY BUS.

Q. OKAY. LET'S TAKE A LOOK AT THE ACTUAL CLAIM LANGUAGE OF THE FIRST CLAIM LIST OF INDEPENDENT CLAIM 6.

(DISCUSSION OFF THE RECORD BETWEEN DEFENDANTS' COUNSEL.)

BY MR. MARSH:

Q. WHAT'S SHOWN HERE IN DDX-142?

A. THIS EXHIBIT SHOWS CLAIM 6.

NOW, IF YOU START READING THIS CLAIM 6, I THINK YOU GET A HEADACHE. I MEAN, SO I TRIED TO BREAK IT INTO BASICALLY LANGUAGE THAT, YOU KNOW, ONE CAN HANDLE, DIGEST AND UNDERSTAND, TO SIMPLIFY IT, TO BREAK IT INTO WHAT IS CALLED ELEMENTS.

OKAY. THIS CLAIM CLAIMS ELEMENTS A, B, C, AND D.

Q. IS THAT WHAT YOU'RE SHOWING BY THE COLORS HERE ON DDX-143?

A. RIGHT. IN ORDER TO ACHIEVE THAT, I COLORED IT.

SO THIS IS ELEMENT A (INDICATING); ELEMENT B (INDICATING); ELEMENT C (INDICATING); ELEMENT D (INDICATING).

AND THIS CLAIM 6 CONSISTS -- YOU CAN BREAK IT INTO FOUR ELEMENTS.

Q. AND SO WHAT ARE YOU SHOWING HERE ON DDX-144?

A. OKAY. SO ON -- I'M SHOWING THOSE FOUR ELEMENTS AND BASICALLY SUMMARIZING IN A FEW WORDS WHAT THEY ARE ABOUT.

AND IF YOU CAN GO BACK ONE SLIDE, PLEASE.

FOR EXAMPLE, IF YOU READ THIS, A CENTRAL PROCESSING UNIT WHICH IS ON AN INTEGRATED CIRCUIT SUBSTRATE, OPERATING A PROCESSING FREQUENCY, MADE OF A FIRST PLURALITY OF TRANSISTORS, THE OSCILLATOR, ENTIRE, NOT JUST PARTIAL, ALSO AN INTEGRATED CIRCUIT WHICH IS CONNECTED TO THE CENTRAL PROCESSING UNIT, CLOCKING IT, MADE OF THE SECOND VARIETY OF A DEVICE, MEANING ALSO TRANSISTORS.

OKAY. SO I SUMMARIZED THAT -- IF YOU CAN GO ON THE NEXT SLIDE -- BASICALLY WHEN IT SAYS IS IT'S A CPU AND THE FIRST CLOCK ARE ON THE SAME IC.

Q. AND IC HERE IS?

A. INTEGRATED CIRCUIT.

Q. AND I SAW THE WORD "SUBSTRATE." WHAT DOES THAT MEAN?

A. A SUBSTRATE IS -- I WOULD SAY MORE ACCURATE TERM FOR THAT IS SILICON DIE OR PIECE OF SILICON. AS I SAID, IT'S ETCHED ON THAT AND THE REST IS CALLED SUBSTRATE. SO IT IS ON THE SAME IC, INTEGRATED CIRCUIT, OR THE SAME CHIP, ON THE SAME DIE TO USE THE PLAIN LANGUAGE.

Q. SO IN YOUR MIND, THOSE TERMS ARE SYNONYMOUS?

A. YES.

Q. OKAY. SO I WANT TO -- I WANT TO UNDERSTAND EACH OF THESE ELEMENTS. LET'S START FIRST WITH THE FIRST ELEMENT, ELEMENT A AS SHOWN HERE ON DDX-145.

NOW, CAN YOU TELL ME WHAT'S -- WHAT IS ELEMENT A?

A. RIGHT. I JUST WENT THROUGH THAT, AND BASICALLY I READ THIS AND, YOU KNOW, YOU CAN SUMMARIZE IT, OKAY, THAT THE FIRST CLOCK -- THIS DIED.

THE FIRST CLOCK AND THE CPU HAVE TO BE ON THE SAME INTEGRATED CIRCUIT.

Q. AND THE INTEGRATED CIRCUIT HERE IS WHERE?

A. THE BOUNDARY IS THIS SQUARE BOUNDARY (INDICATING).

AND WHY IS THAT SO? SO THAT THEY ARE BUILT ON THE SAME TRANSISTORS AND THEY ARE EQUALLY EXPOSED TO THE SAME PARAMETERS, PROCESS, AND OPERATING CONDITIONS. THAT'S BASICALLY WHY THIS ELEMENT IS REQUIRED. THEY ARE BOTH ON THE IC.

Q. SPEAKING OF THAT, LET'S TURN TO DDX-146. WHAT ARE YOU SHOWING ON THIS SLIDE?

A. THIS SLIDE IS THE SECOND ELEMENT OF THE CLAIM, WHICH REQUIRES THAT THEY VARY TOGETHER, OKAY?

SO IT READS THAT VARYING THE PROCESSING FREQUENCY OF THE FIRST TRANSISTORS AT A CLOCK RATE OF -- THANK YOU VERY MUCH. I -- THIS DOESN'T WORK -- AND THE SECOND PLURALITY OF THE ELECTRONIC DEVICES, THEY VARY THE SAME WAY AS THE FUNCTIONAL

PARAMETER VARIATIONS IN ONE OR MORE FABRICATION OR OPERATIONAL PARAMETERS ASSOCIATED WITH INTEGRATED CIRCUIT ENABLING THE PROCESSING FREQUENCY TO TRACK CLOCK RATE IN RESPONSE TO PARAMETER VARIATIONS.

BASICALLY WHAT IT'S SAYING, LOOK, THEY'RE MADE OUT OF SAME TRANSISTORS. THEY ARE THE SAME. SO IF I HEAT UP THE CHIP, ALL OF THEM WILL SLOW DOWN. IF I ELEVATE THE VOLTAGE, ALL OF THEM WILL SPEED UP.

IN OTHER WORDS, IT'S NOT GOING TO HAPPEN WHEN ONE GOES IN ONE DIRECTION AND ONE GOES IN THE OPPOSITE DIRECTION. THEY GO TOGETHER.

BUT IT DOESN'T SAY FOR HOW MUCH. I MEAN, BUT JUST -- WHAT IT REQUIRES IS THAT THEY, THEY ARE SUBJECTED TO SAME CONDITIONS IN THE SAME PLACE SO THEY WILL VARY IN THE SAME WAY.

Q. AND WHY DID YOU THEN COLOR IN THE IC OR THE CHIP?

A. IT -- IT'S A COLOR CODING, SO WHEN YOU SEE ORANGE, YOU KNOW WE ARE TALKING ABOUT THE ELEMENT OF VARYING TOGETHER.

Q. AND I SAID "IC OR CHIP." ARE THOSE THE SAME THING?

A. YES. INTEGRATED CIRCUIT, OR, YOU KNOW, COLLOQUIALLY WE USE THE TERM "CHIP." I EXPLAINED WHY. IT'S JUST CHIPPED OFF FROM THE WAFER.

I THINK WE'RE LOSING SOME PRECISION. I THINK THE COURT HAS CONSTRUCTED THE TERM WHAT INTEGRATED CIRCUIT MEANS, AND DEFINED IT PRECISELY BASICALLY.

AND I HAVE -- IN MY CHEAT SHEET I HAVE THE CLAIM

CONSTRUCTION.

Q. AND DID YOU APPLY THE COURT'S CLAIM CONSTRUCTIONS?

A. YES. AS A MATTER OF FACT, THIS IS WHY I HAVE A CHEAT SHEET HERE, AND I'LL PULL IT OUT.

AND SO WE'RE TALKING ABOUT WHICH --

Q. WHAT IS THE DOCUMENT THAT YOU HAVE, DR. O? CAN YOU JUST IDENTIFY IT?

A. WHAT I HAVE IS CLAIM TERMS CONSTRUCTED BY THE COURT. SO THE COURT HAS -- SO THAT WE DON'T TALK ABOUT DIFFERENT THINGS. LIKE WHEN I SAY MR. SMITH, I MEAN MR. BILL SMITH, OKAY? SO WE KNOW -- OR WHEN YOU SAY, YOU KNOW, DR. O, IT'S NOT MR. JIM OTTESON. IT'S ME.

SO THE COURT DEFINES THOSE TERMS, WHAT THE MEANING IS.

AND --

Q. WHY DON'T WE MOVE ON TO THE NEXT ELEMENT --

A. YEAH.

Q. -- WHICH IS ELEMENT C SHOWN IN DDX-147. WHAT IS THIS ELEMENT?

A. THIS ELEMENT SAYS THAT IN ADDITION, IT HAS TO HAVE AN I/O INTERFACE. SO THE I/O INTERFACE IS INPUT/OUTPUT INTERFACE, SOMETHING THAT TALKS TO THINGS OR COMMUNICATES WITH THINGS OUTSIDE OF THE CHIP.

Q. AND IN DDX-148, YOU SHOW ELEMENT D. WHAT IS THAT?

A. AND IN THAT ELEMENT D, IT SAYS THAT IT HAS TO HAVE AN INDEPENDENT SECOND CLOCK. IT HAS TO HAVE -- THIS I/O INTERFACE

CONTROLLING THAT 3-STAGE CURRENT CONTROL OSCILLATOR AS THEY, AS THEY STATE IT HERE IN THE FIGURE, ACTUALLY.

Q. AND SO, AGAIN, THIS IS A DIGITAL PLL. IS THAT THE SAME THING AS A DPLL?

A. YES. IT ALL OPERATES ON THE SAME PRINCIPLES AS THE ANALOG EXCEPT YOU DIGITIZE THAT CONTROL WHICH CONTROLS THE FEEDBACK.

Q. WHAT IS SHOWN IN DDX-185?

A. HERE IS THAT 3-STAGE RING OSCILLATOR AND --

Q. CAN YOU POINT OUT THE STAGES, PLEASE.

A. ONE, TWO, THREE (INDICATING).

NOW, THIS GOES POSITIVE TO POSITIVE, SO THERE IS INVERSION HERE (INDICATING).

AND IT SHOWS IT'S A DIFFERENTIAL, DIFFERENTIAL STAGE. SO YOU HAVE DIFFERENTIAL -- INPUT COMES IN BOTH POLARITIES AND THE OUTPUT COMES OUT ALSO IN BOTH POLARITIES.

Q. SO CAN YOU EXPLAIN, IF WE STARTED ON THE UPPER LEFT-HAND LEAD WITH A 0, HOW DOES THIS WORK?

A. LET'S SEE. IF I START WITH 0 AND, AND THAT I WILL COME BACK, I WILL COME FROM HERE AND WILL END UP AS 1 AND THAT 1 WILL COME IN HERE AND CHANGE (INDICATING).

SO IT GOES BASICALLY LIKE THIS, LIKE AN 8, LIKE NUMBER 8 (INDICATING).

Q. OKAY. THANK YOU. NOW, WHAT'S SHOWN ON DDX-186?

A. IT IS THE CHIP MICRO PHOTOGRAPH. BASICALLY THEY FABRICATED THAT CHIP AND THEY TOOK A PICTURE, AND THIS IS THE

PART OF THE PAPER WHICH WAS PUBLISHED IN ISSC 2000 AND, MAYBE THAT'S A --

BILL, COULD YOU PLEASE BLOW UP THIS PORTION HERE?

Q. YOU MIGHT BE ABLE TO SEE IT ON YOUR SCREEN THERE.

A. OH, YEAH. IT'S 2004.

Q. THANK YOU. OKAY. WHAT'S SHOWN ON THE NEXT SLIDE, DDX-187 HERE?

A. SO IT SHOWS THE SAMSUNG PRODUCT, WHICH IS THE SAMSUNG CHIP 32442A. THIS WOULD BE THE BOUNDARY OF THE CHIP (INDICATING). IT HAS THE ARM PROCESSOR RIGHT HERE (INDICATING). AND IT HAS MPLL WHICH CONTAINS THE RING OSCILLATOR (INDICATING).

Q. OKAY. AND TURNING TO DDX-188, I SEE A BOX LABELED "VCO." WHAT DOES THAT MEAN?

A. THAT IS A VOLTAGE CONTROL OSCILLATOR WHICH IS USED IN SAMSUNG PLL.

Q. OKAY. AND WHAT'S THAT VCO USED FOR?

A. IT IS USED TO CLOCK A -- THE COMPONENTS, THE PROCESSING, THE CPU ON THE CHIP.

Q. GREAT. SO LET'S SUM UP ON ELEMENT A.

YOU ANALYZED THE HTC PRODUCTS CONTAINING QUALCOMM, TI, AND SAMSUNG CHIPS, AND DID YOU DETERMINE WHETHER OR NOT THEY HAVE AN ENTIRE OSCILLATOR AND CPU THAT'S MADE OF ELECTRONIC DEVICES AND ON THE SAME INTEGRATED CIRCUIT?

A. YES. I MEAN, THE FIRST STATEMENT, THAT THEY'RE MADE OUT OF THE SAME TRANSISTORS, THAT'S A GIVEN. WE KNOW THAT

EVERYTHING THAT IS FABRICATED IS FABRICATED FROM THE SAME TRANSISTORS, AND SO THEY MEET THAT ALL ACROSS.

Q. OKAY. AND DID YOU DETERMINE WHETHER OR NOT THE ENTIRE OSCILLATOR IS CONNECTED TO AND CLOCKS THE CPU AS REQUIRED BY THE CLAIM LANGUAGE?

A. YES. WE HAVE FOUND AND IDENTIFIED THE OSCILLATORS WHICH ARE USED TO CLOCK A CPU AND THEY'RE CONNECTED TO THE CPU.

Q. OKAY. NOW, THERE'S A DOTTED LINE HERE. WHAT DOES THAT DOTTED LINE TELL US?

A. IS -- ABOVE THAT IS CLAIM 6 APPLY, AND BELOW IS CLAIM 13 WHICH HAS THAT ADDITIONAL ELEMENT THAT THAT OSCILLATOR HAS TO BE A RING OSCILLATOR.

Q. WELL, I THINK WE'VE GOT SOME CLAIMS LISTED THERE, CLAIMS 9 AND 15?

A. RIGHT, DEPENDENT CLAIMS, RIGHT.

Q. SO THIS, ABOVE THE LINE, IS CLAIM -- IS INDEPENDENT CLAIMS 6 AND 13; IS THAT RIGHT?

A. THAT'S RIGHT, YES. THAT'S CORRECT.

Q. OKAY.

A. I -- WE MIX IT IN THIS SLIDE. IT'S DIFFERENT.

Q. SO IN YOUR OPINION, DO THE HTC PRODUCTS MEET ELEMENT A OF CLAIMS 6 AND 13?

A. YES, IT DOES.

Q. OKAY. AND THEN AS FAR AS THE DEPENDENT CLAIMS WHICH REQUIRE THAT THE ENTIRE OSCILLATOR IS A RING OSCILLATOR, DO THE

HTC PRODUCTS MEET THAT LIMITATION AS WELL?

A. YES, IT DOES. WE HAVE FOUND THEM.

Q. AND THAT'S FOR DEPENDENT CLAIMS 9 AND 15; CORRECT?

A. THAT APPLIES TO 9 AND 15.

Q. OKAY. SO BACK TO OUR BIG CHART. HAVE YOU FORMED AN OPINION, THEN, AS TO WHETHER OR NOT EACH OF THESE PRODUCTS MEETS ELEMENT A, EACH OF THE HTC PRODUCTS IN THIS CASE MEETS ELEMENT A?

A. YES, WE'VE FOUND THAT THEY MEET.

Q. OKAY.

A. SO THE CHECK MARK GOES ON THIS FIRST ROW.

Q. GREAT. LET'S MOVE ON TO ELEMENT B. ELEMENT B IS THE VARYING TOGETHER ONE.

DO YOU RECOGNIZE THE BOOK SHOWN IN DDX-196?

A. YES, I DO.

Q. AND WHAT IS THIS BOX?

A. THIS IS A BOOK WHICH CONTAINS ARTICLES ON HIGH PERFORMANCE MICROPROCESSOR CIRCUIT DESIGN EDITED BY DR. CHANDRAKASAN THAT WE MENTIONED.

Q. AND THIS IS THE SAME BOOK THAT I HELD UP EARLIER IN WHICH YOU PUBLISHED A CHAPTER?

A. THE VERY SAME ONE.

Q. OKAY. PUBLISHED BY IEEE PRESS; RIGHT?

A. YES.

Q. WHAT ARE YOU SHOWING IN DDX-197?

OR REFERENCES IT DURING HIS OR HER TESTIMONY, THAT'S ADEQUATE TO THE TASK AND SO YOU CAN THEN MOVE IT INTO EVIDENCE AT A BREAK OR WHATEVER IT'S CONVENIENT. OR YOU CAN DO IT DURING YOUR TIME. I DON'T PARTICULARLY CARE.

MR. MARSH: THANK YOU VERY MUCH.

AND JUST TO BE CLEAR, REFERENCING IT, BY REFERENCING THE DOCUMENT CITED IN THE SLIDE IS SUFFICIENT IN YOUR VIEW?

THE COURT: AS LONG AS HE TALKS ABOUT IT, CERTAINLY.

MR. MARSH: THANK YOU VERY MUCH.

THE COURT: ALL RIGHT. ANY OTHER ISSUES?

MR. RIVERA, DO YOU KNOW, ARE THE JURORS ALL HERE?

THE CLERK: YES, YOUR HONOR.

THE COURT: OKAY. LET'S BRING THE JURY BACK IN.

(JURY IN AT 9:22 A.M.)

THE COURT: LADIES AND GENTLEMEN OF THE JURY, GOOD MORNING. WELCOME BACK. I HOPE YOU HAD A GOOD EVENING.

YOU WILL RECALL THAT BEFORE WE BROKE FOR THE DAY YESTERDAY, WE WERE HEARING TESTIMONY FROM DR. OKLOBDZIJA.

I BELIEVE DR. OKLOBDZIJA IS IN THE FRONT ROW.

SIR, IF YOU WOULD RETURN TO THE WITNESS STAND.

DR. OKLOBDZIJA, AS YOU APPROACH THE WITNESS STAND --

THE WITNESS: GOOD MORNING, YOUR HONOR.

THE COURT: GOOD MORNING, SIR. I WILL REMIND YOU THAT YOU REMAIN UNDER OATH.

THE WITNESS: YES, THANK YOU, YOUR HONOR.

(VOJIN OKLOBDZIJA, DEFENDANTS' WITNESS, WAS PREVIOUSLY SWORN.)

THE COURT: MR. MARSH, YOU MAY RESUME YOUR EXAMINATION.

MR. MARSH: THANK YOU, YOUR HONOR.

DIRECT EXAMINATION (RESUMED)

Q. GOOD MORNING, DR. OKLOBDZIJA. WELCOME BACK.

A. GOOD MORNING, MR. MARSH.

Q. BEFORE WE GET STARTED, I WANTED TO JUST RECAP WHERE WE WERE.

YESTERDAY YOU TESTIFIED THAT IT WAS YOUR OPINION THAT THE HTC PRODUCTS AT ISSUE IN THIS CASE MET ELEMENT A OF THE CLAIMS, AND WHEN WE STOPPED YESTERDAY WE WERE DISCUSSING ELEMENT B.

AND YOU HAD SHOWN US THIS SLIDE ABOUT THE CHANDRAKASAN REFERENCE, THE TEXTBOOK, AND YOU HAD SHOWN US INFORMATION ABOUT THE QUALCOMM PRODUCTS IN THE HTC -- OR THE QUALCOMM CHIPS IN THE HTC PRODUCTS THAT YOU ANALYZED, AND YOU HAD SHOWN US INFORMATION ABOUT THE TI CHIPS IN THE HTC PRODUCTS THAT YOU ANALYZED, AND WE HAD JUST FINISHED DISCUSSING INFORMATION ABOUT THE SAMSUNG CHIPS HERE ON EXHIBIT, OR HERE ON DDX-209 THAT YOU HAD ANALYZED.

DO YOU RECALL THAT?

A. YES.

Q. OKAY. NOW, BASED ON THE INFORMATION THAT YOU HAVE ANALYZED, HAVE YOU FORMED AN OPINION AS TO WHETHER THE HTC PRODUCTS AT ISSUE HAVE A CPU PROCESSING FREQUENCY THAT TRACKS

AND VARIES IN THE SAME WAY AS THE ENTIRE OSCILLATOR CLOCK RATE?

A. YES, THEY HAVE THE RING OSCILLATOR.

Q. AND HAVE YOU FORMED AN OPINION AS TO WHETHER OR NOT THE HTC PRODUCTS THE ISSUE IN THIS CASE, WHETHER THE VARYING THAT OCCURS IS SOMETHING THAT OCCURS AS A FUNCTION OF OR IN RESPONSE TO PARAMETER VARIATION IN FABRICATION OR OPERATIONAL PARAMETERS?

A. YES, THAT'S TRUE FOR THE MAJORITY OF THE CHIPS.

Q. AND I SAID "OR," BUT I MEAN ARE BOTH TRUE? IS IT TRUE THAT THEY VARY BOTH AS A FUNCTION OF AND IN RESPONSE TO THOSE PARAMETER VARIATIONS?

A. YES. THEY VARY IN RESPONSE TO FABRICATION AND/OR OPERATIONAL PARAMETERS.

Q. THANK YOU. AND SO I SEE WE'VE REACHED A DOTTED LINE AGAIN. IS THERE ANY SIGNIFICANCE IN THAT?

A. YES, BECAUSE THAT IS -- NOW WE'RE CROSSING INTO CLAIM 13 AND DEPENDENT CLAIMS 7 AND 14.

Q. OKAY. SO I THINK CLAIMS 6 AND 13 ARE THE TWO ROWS ABOVE; IS THAT RIGHT?

A. THAT IS CORRECT.

Q. OKAY. AND CLAIMS, DEPENDENT CLAIMS 7 AND 14 THEN HAVE ADDITIONAL LANGUAGE THAT SAYS THE OPERATIONAL PARAMETERS INCLUDE TEMPERATURE OR VOLTAGE.

DID YOU REACH A DETERMINATION AS TO WHETHER THE HTC PRODUCTS IN THIS CASE HAVE AN OPERATIONAL PARAMETER THAT

INCLUDES EITHER TEMPERATURE OR VOLTAGE?

A. YES, I DID. WE WENT THROUGH IT YESTERDAY.

Q. AND WHAT WAS YOUR -- WHAT WAS YOUR DETERMINATION?

A. THEY DO MEET.

Q. OKAY. SO NOW GOING BACK TO OUR MASTER CHART HERE AND THINKING ABOUT ELEMENT B, THE VARYING ELEMENT OF THE CLAIMS, DID YOU -- HAVE YOU FORMED AN OPINION, SIR, AS TO WHETHER OR NOT THE HTC PRODUCTS IN THIS CASE MEET ELEMENT B OF THE CLAIMS?

A. YES, I DID.

Q. OKAY. AND THAT APPLIES FOR BOTH CLAIMS 6 AND 13?

A. THAT IS CORRECT.

Q. OKAY. GREAT. LET'S TALK ABOUT THE ON-CHIP I/O INTERFACE NEXT.

WHAT ARE YOU SHOWING HERE IN DDX-218?

A. FIRST OF ALL, I SHOULD SAY THERE ARE MANY I/O INTERFACES THAT THE MODERN PHONE HAS, AND OUT OF THOSE -- FIRST OF ALL, THERE'S AN INTERFACE, I/O INTERFACE TO THE RADIO PART BECAUSE THE PHONE IS CONNECTED TO THE RADIO NETWORK IN ORDER TO BE, TO RECEIVE EITHER PHONE SIGNALS OR SIGNALS FROM THE INTERNET BASICALLY. IT ALL GOES THROUGH THE INTERNET.

Q. AND DR. O, CAN YOU EXPLAIN TO ME, WHAT IS I/O AGAIN JUST SO THAT I'VE GOT THAT CORRECT.

A. INPUT/OUTPUT. SO THAT PROCESSOR COMMUNICATES WITH THE SURROUNDING ENVIRONMENT THROUGH INPUT/OUTPUT INTERFACE.

SO OUT OF MANY, WE HAVE SINGLED HERE TWO OF THEM, AND

SHARPEN THOSE DISPUTES FOR EVERYBODY. ALL RIGHT?

A. THAT'S FAIR. I -- THAT'S FAIR.

Q. NOW, CAN WE GO TO THE PATENT?

AND, DR. OKLOBDZIJA, YOU KNOW THAT THIS PATENT WAS FILED IN 1989; RIGHT?

A. THAT IS CORRECT.

Q. AND WE'VE HEARD A LOT OF TALK DURING THE WEEK ABOUT PLL'S OR PHASE LOCK LOOPS; RIGHT?

A. THAT IS CORRECT.

Q. AND PLL'S WERE WELL-KNOWN SINCE THE 1970S; RIGHT?

A. YOU SAID 19 --

Q. '70S?

A. I BELIEVE 1930.

Q. OKAY, 1930. FAIR ENOUGH.

AND CRYSTALS TO CLOCK CPU'S WERE KNOWN BEFORE THE PATENT; RIGHT?

A. THAT IS CORRECT.

Q. AND RING OSCILLATORS WERE KNOWN BEFORE THE PATENT; CORRECT?

A. THAT IS CORRECT.

Q. NOW, THE FRONT, OR THE TITLE OF THE PATENT ITSELF -- CAN WE PULL THAT UP, JIM? IT STATES "HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK." RIGHT?

A. THAT IS CORRECT.

Q. AND YOU WOULD AGREE WITH ME THAT AT THE TIME THIS PATENT

WAS FILED, AND EVEN TODAY, DESIGNERS OF MICROPROCESSORS ARE -- HAVE TO CONFRONT CERTAIN OPERATIONAL PARAMETERS; RIGHT?

A. THAT IS CORRECT.

Q. RIGHT. AND SOMETIMES YOU'VE HEARD THEM REFERRED TO NUMEROUS TIMES AS PROCESS, VOLTAGE, AND TEMPERATURE, FOR EXAMPLE; RIGHT?

A. YES, ALWAYS.

Q. AND PEOPLE REFER TO THEM AS PVT; RIGHT?

A. YES.

Q. AND WOULD THAT BE FINE TO REFER TO THEM AS PVT? WOULD YOU BE OKAY WITH THAT?

A. THAT IS FINE.

Q. NOW, IF WE COULD GO TO COLUMN 16, LINES 48 TO 53 OF THE PATENT, AND BEGINNING WITH TRADITIONAL, SO THE PATENT EXPLAINS THAT TO DEAL WITH THESE PARAMETERS, "TRADITIONAL CPU DESIGNS ARE DONE SO THAT WITH THE WORSE CASE OF THE THREE PARAMETERS," WHICH THE THREE PARAMETERS ARE PROCESS, VOLTAGE AND TEMPERATURE; RIGHT?

A. THAT'S CORRECT, THAT'S THE WORSE CASE CORNER.

Q. RIGHT. "THE CIRCUIT WILL FUNCTION AT THE RATED CLOCK SPEED." I READ THAT RIGHT; RIGHT?

A. THE FIRST AND --

Q. THAT PORTION OF THE PATENT; CORRECT?

A. I READ THIS PORTION OF THE PATENT, YES.

Q. AND YOU AGREE WITH IT?

A. YEAH.
Q. OKAY. AND THE PATENT SAYS THAT THE RESULT ARE DESIGNS THAT MUST BE CLOCKED A FACTOR, AND IT SHOULD, OR TWO SLOWER THAN THEIR MAXIMUM THEORETICAL PERFORMANCE, SO THEY WILL OPERATE PROPERLY IN WORSE CASE CONDITIONS; RIGHT?
A. ABOUT THAT TIME THAT, YOU KNOW, '89 TIMEFRAME --
Q. RIGHT.
A. -- ROUGHLY, YOU HAVE TO LEAVE A SAFETY MARGIN, WHICH I BELIEVE WAS ONE OF THE QUESTIONS THE JURORS ASKED. YOU HAVE TO LEAVE A SAFETY MARGIN, AND I THINK THEY ASKED HOW BIG THE SAFETY MARGIN IS. LET'S SAY PUT IT IN THE MIDDLE, GO TO HALF, AND LEAVE YOURSELF SOME LEEWAY FOR THE WORSE CASES.
Q. WELL, DOCTOR, A FACTOR OF 2 IS 50 PERCENT; CORRECT?
A. YEAH.
Q. OKAY. SO LET'S GO TO FIGURE 17 OF THE PATENT. IF WE CAN BRING IT DOWN.
JIM, IF I COULD HAVE THE ELMO.
NOW, WE'VE SEEN THIS QUITE A BIT, RIGHT, IN THIS CASE? THIS IS FROM MY --
CAN YOU SIZE THAT, JIM? OKAY, THANKS. THAT'S GOOD. THAT'S GOOD. THANK YOU.
NOW, DOCTOR, YOU SAW THIS IN MY OPENING STATEMENT; CORRECT.
A. MANY TIMES.
Q. OKAY. AND I'VE PUT ON A DOTTED LINE AROUND CERTAIN OF

Q. OKAY. SO LET ME PUT IT UP ON THE ELMO. AND THAT'S THE CONSTRUCTION, RIGHT, DOCTOR, THE ENTIRE OSCILLATOR THAT WE JUST SAW IN THE CLAIM IS PROPERLY UNDERSTOOD TO EXCLUDE ANY EXTERNAL CLOCK USED TO GENERATE THE SIGNAL USED TO CLOCK THE CPU; RIGHT?

A. EXCLUDE ANY EXTERNAL CLOCK -- YES, THAT'S CORRECT.

Q. AND YOU APPLIED THAT CLAIM CONSTRUCTION IN OFFERING YOUR OPINION; CORRECT?

A. I DO, ABSOLUTELY.

Q. RIGHT. NOW, WE'RE ALL BOUND BY THIS CONSTRUCTION? WE ALL HAVE TO USE IT?

A. THAT -- THOSE ARE THE RULES OF THE GAME.

Q. THE RULES OF THE GAME, OKAY. AND I WANT TO WALK THROUGH THE RULES OF THE GAME WITH YOU IN A LITTLE BIT OF DETAIL.

NOW, IT SAYS, "PROPERLY UNDERSTOOD TO EXCLUDE ANY EXTERNAL CLOCK," AND YOU WOULD AGREE WITH ME, DOCTOR, THAT AN EXTERNAL CLOCK MEANS IT'S OFF THE CHIP; RIGHT?

A. I ABSOLUTELY AGREE WITH YOU, MR. SMITH.

Q. YOU AGREE -- I'M SORRY?

A. ABSOLUTELY I AGREE.

Q. OKAY. THANK YOU.

SO -- AND YOU WOULD AGREE WITH ME THAT IF THERE'S AN OFF-CHIP CLOCK THAT'S USED TO GENERATE THE SIGNAL THAT CLOCKS THE CPU, THEN THERE'S NO INFRINGEMENT; RIGHT?

A. THEN THE ELEMENT 13 -- WELL, THE ELEMENT A IS NOT SATISFIED AND THAT WILL KNOCK BOTH OF THEM OUT.

Q. BECAUSE YOU HAVE TO HAVE ALL OF THE ELEMENTS TO INFRINGE; RIGHT?

A. THAT IS -- IF I'M BEING A GOOD LAW STUDENT, I THINK THAT'S HOW I UNDERSTAND IT.

Q. OKAY. NOW, LET'S GO -- LET'S GO RIGHT TO THE ACCUSED PHONES AND SEE IF WE CAN SEE WHERE WE DISAGREE ON THE CLAIM CONSTRUCTION. LET'S GO RIGHT TO THE HEART OF THE MATTER.

A. RIGHT TO THE HEART, THAT'S RIGHT.

Q. NOW, SOME OF THE -- WE CAN DROP THAT, JIM.

SOME OF THE HTC PHONES USE A QUALCOMM CHIP; RIGHT?

A. YES, SOME.

Q. AND SOME USE A TEXAS INSTRUMENTS CHIP?

A. CORRECT.

Q. AND OTHERS, THE REMAINDER, USE THE SAMSUNG CHIPS; RIGHT?

A. THAT IS CORRECT.

Q. AND FOR PURPOSES OF YOUR INFRINGEMENT ANALYSIS, THEY GENERALLY WORK THE SAME WAY; CORRECT?

A. THAT IS CORRECT.

Q. OKAY. AND SO YOU WOULD AGREE WITH ME, DOCTOR, THAT ALL OF THE ACCUSED HTC PHONES THAT YOU LOOKED AT, WHATEVER THE MANUFACTURER OF THE CHIP, ALL HAD A PLL IN THEM; RIGHT?

A. THAT IS CORRECT.

Q. AND I WANT TO PUT YOUR DIAGRAM UP.

IF WE CAN GET THE ELMO AGAIN, JIM. THANK YOU.

AND YOU REMEMBER THIS -- YOU PREPARED THIS SLIDE; RIGHT?

A. YES.
Q. AND IN ALL OF THE HTC PHONES THAT HAVE THE -- AND ALL OF THEM HAVE PLL, AND THE PLL SENDS OUT A CLOCK THAT CLOCKS THE CPU (INDICATING); CORRECT?
A. THAT IS CORRECT.
Q. AND ALL THE HTC PHONES HAVE AN EXTERNAL REFERENCE (INDICATING); RIGHT?
A. THAT IS CORRECT.
Q. AND THEY'RE ALL DIRECTLY OR INDIRECTLY BASED ON A CRYSTAL; RIGHT?
A. AS WE HAVE SEEN IT, RIGHT.
Q. RIGHT. COULD BE DIRECTLY FROM A CRYSTAL OR IT COULD BE FROM A CLOCK GENERATOR THAT HAS A CRYSTAL; RIGHT?
A. SOMETHING STABLE.
Q. OKAY. BUT THEY ALL COME FROM A CRYSTAL ONE WAY OR THE OTHER; RIGHT?
A. LET'S SAY YES. I MEAN, NOT NECESSARILY, BUT SOMETHING STABLE, STABLE REFERENCE, AND CRYSTAL IS USUALLY STABLE REFERENCE.
Q. SO THIS IS A STABLE REFERENCE (INDICATING). ALL THE PHONES USE A STABLE REFERENCE INTO THE PLL; CORRECT?
A. THAT IS CORRECT.
Q. AND COULD YOU CALL THAT A FIXED REFERENCE?
A. I WOULD CALL IT STABLE.
Q. STABLE. BECAUSE NOTHING IS PERFECT; CORRECT?

A. THAT IS CORRECT.
Q. OKAY. NOW -- AND THIS IS -- THIS IS EXTERNAL, RIGHT, DOCTOR?
A. THAT IS EXTERNAL.
Q. OKAY. AND ALL THE HTC PHONES THAT YOU LOOKED AT -- AND, YOUR HONOR, MAY I APPROACH THE SCREEN?
THE COURT: YOU MAY, MR. SMITH.
MR. SMITH: THANK YOU.
Q. -- THEY ALL CONTAIN EITHER A RING OSCILLATOR OR AN OSCILLATOR IN A PLL; CORRECT?
A. THAT IS CORRECT.
Q. AND YOUR POINT, DOCTOR, IF I UNDERSTOOD YOUR TESTIMONY CORRECTLY, WAS THAT IT'S THE RING OSCILLATOR OR THE OSCILLATOR THAT, APPLYING THE JUDGE'S CLAIM LANGUAGE, IS USED TO GENERATE THE CLOCK SIGNAL; CORRECT?
A. THAT IS CORRECT. IT IS CONNECTED TO THE CPU, IT GENERATES THAT CLOCK SIGNAL AS I EXPLAINED TO THE COURT, AND THAT IS THE CLOCK GENERATOR.
Q. SO THE ANSWER IS YOU'RE POINTING TO THE RING OSCILLATOR OR THE OSCILLATOR AND SAYING THAT THAT'S USED TO GENERATE THAT CLOCK?
A. THAT IS CORRECT.
Q. RIGHT. AND YOUR POINT IS THAT EVEN THOUGH THERE'S A CRYSTAL OR AN EXTERNAL REFERENCE THAT GOES INTO THE PLL --
A. RIGHT.

Q. -- THIS IS NOT USED TO GENERATE THE CLOCK SIGNAL OVER HERE (INDICATING); RIGHT?
A. THAT IS CORRECT.
Q. THAT'S YOUR OPINION?
A. IT IS NOT USED TO GENERATE.
Q. RIGHT. TO?
A. TO GENERATE. IT IS USED TO BE A REFERENCE. IT IS USED TO ADJUST, BUT IT IS NOT USED TO GENERATE.
Q. WE'LL GET THERE, DOCTOR. TRUST ME. BUT I JUST WANT TO MAKE SURE WE KNOW WHERE THE DISPUTE IS. OKAY?
SO YOUR POINT IS IT'S THE RING OSCILLATOR OR OSCILLATOR ALONE THAT GENERATES THIS CLOCK SIGNAL; CORRECT?
A. AS I HAVE DEMONSTRATED HERE IN COURT.
Q. RIGHT. BUT I JUST WANT TO MAKE SURE WE'RE ON THE SAME PAGE.
A. YES.
Q. OKAY, GOOD. NOW, YOU'LL AT LEAST AGREE WITH ME, DOCTOR, THAT THIS EXTERNAL REFERENCE RIGHT HERE IS AN ESSENTIAL PART OF THE, OF ALL THE PLL'S IN THE HTC PHONES (INDICATING); RIGHT?
A. I AGREE WITH YOU THAT IF WE ARE TALKING ABOUT PLL, PLL NEEDS TO HAVE A REFERENCE. SO IT IS -- LIKE IF WE ARE -- IF I AM TEACHING PLL, OKAY, I'LL HAVE TO INCLUDE THE REFERENCE.
Q. RIGHT. SO YOUR POINT IS YOU CAN'T HAVE A -- YOU CAN'T HAVE A PLL WITHOUT A CRYSTAL?
A. WITHOUT A REFERENCE, YES, CORRECT.

Q. OKAY. AND TYPICALLY THE REFERENCE IS A CRYSTAL; CORRECT?
A. YES, LET'S SAY A CRYSTAL.
Q. A STABLE, EXTERNAL REFERENCE; CORRECT?
A. YES, RIGHT.
Q. OKAY. NOW --
YOUR HONOR, MAY I APPROACH AGAIN?
THE COURT: YOU MAY.
MR. SMITH: THANK YOU.
Q. NOW, THIS STABLE REFERENCE HAS A RELATIONSHIP TO THE CLOCK SIGNAL IN ALL THE HTC PHONES THAT YOU LOOKED AT (INDICATING); CORRECT?
A. IT IS USED TO ADJUST THE FREQUENCY GENERATED BY THE RING OSCILLATOR, SO IT HAS SOME RELATIONSHIP WITH IT.
Q. AND I THINK -- AND IT'S A -- IT'S A FORMULA; RIGHT?
A. YOU CAN PUT IT THIS WAY. AS I EXPLAINED TO THE COURT, BASICALLY IF I CAN POINT, THIS FREQUENCY AND THIS FREQUENCY HAVE TO BE EQUAL (INDICATING).
Q. BUT IT'S A FORMULA?
A. HOWEVER YOU COME TO THAT, YEAH, YOU CAN MAKE A FORMULA OUT OF IT, BUT BASICALLY DIVIDING THE RING OSCILLATOR TO BE EQUAL, OR EVEN IF THERE IS -- IF YOU WANT THIS ONE TO RUN EXACTLY EQUAL FREQUENCY OF THIS ONE, THEN YOU HAVE TO DIVIDE IT.
Q. WELL, DOCTOR, YOU CALL THIS, THIS RELATIONSHIP, I THINK YOU WERE SMILING WHEN YOU SAID IT, BUT YOU CALLED IT THE SECRET FORMULA; RIGHT?

A. BECAUSE --
Q. BUT THAT'S WHAT YOU SAID, SIR; RIGHT?
A. IT'S A COMMON SENSE.
Q. NO, NO. I DIDN'T --
A. THIS IS EQUAL TO THAT, SO YOU CAN DERIVE THAT RELATIONSHIP AND IT'S A TEXTBOOK.
Q. WELL, DOCTOR, I PROMISE YOU, WE WILL GET TO THE FORMULA.
A. OKAY.
Q. BUT I WANT TO JUST ASK SOME SIMPLE QUESTIONS SO WE'RE ROLLING ON THE SAME PAGE.
A. ALL RIGHT.
Q. YOU CALLED THIS RELATIONSHIP BETWEEN THE EXTERNAL REFERENCE AND THIS CLOCK SIGNAL (INDICATING), YOU REFERRED TO IT AS THE SECRET FORMULA; RIGHT? YES?
A. I USED THE TERM BECAUSE IT IS IN EVERY TEXTBOOK, SO I WAS SURPRISED IT'S SECRET.
Q. RIGHT. BUT THE FORMULA FOR THE RELATIONSHIP BETWEEN THIS EXTERNAL CRYSTAL, EXTERNAL REFERENCE AND THE CLOCK SIGNALS IS IN EVERY TEXTBOOK? THAT'S YOUR POINT; RIGHT?
A. AND EVERY TEXTBOOK ON PLL WILL TELL YOU THAT THIS, YOU KNOW, IS RELATED TO THAT ONE AND IT'S RELATED BY WHATEVER DIVIDE FACTOR IT IS, AND IF YOU PUT A DIVIDE FACTOR OVER THERE, YOU KNOW, ET CETERA, WHICH MEANS WHAT MR. HAROUN WAS TRYING TO DIVIDE HERE --
Q. RIGHT.

A. -- NOT VERY SUCCESSFULLY.
Q. IF WE CAN TAKE DOWN -- AND YOU DISAGREED WITH DR. HAROUN; CORRECT?
A. I DIDN'T HAVE A PRIVILEGE TO SEE THAT FORMULA AND --
Q. JUST IN GENERAL YOU DISAGREE?
A. AND I WONDER IF THAT WOULD BE ANYTHING DIFFERENT THAN WHAT'S IN THE TEXTBOOKS.
Q. OKAY. IF WE COULD TAKE DOWN THE ELMO AND PUT UP EXHIBIT 3027. AND LET'S -- WE'VE LOOKED AT A LOT OF SLIDES AND ANIMATIONS IN THIS CASE, DOCTOR, BUT I WANT TO LOOK AT AN ACTUAL DATA SHEET FOR ONE OF THE QUALCOMM CHIPS THAT'S USED IN AN ACTUAL ACCUSED HTC PHONE. RIGHT?
A. YEAH.
Q. AND THIS IS A PLL (INDICATING)?
A. THAT IS A PLL.
Q. AND IT'S FOR 45 NANOMETER MOBILE CPU'S; CORRECT?
A. CORRECT.
Q. AND THE 45 NANOMETER, NM, REFERS TO THE SIZE OF THE CHIP; CORRECT?
A. IT IS FABRICATION TECHNOLOGY, WHICH MEANS THAT MINIMAL TRANSISTOR FEATURE SIZE IS 45 NANOMETER.
Q. IT REFERS TO THE PHOTOLITHOGRAPHY PROCESS TO GET TO THE 45 NANOMETERS; CORRECT?
A. YES, CORRECT.
Q. OKAY. NOW, THIS DATA SHEET IS CONFIDENTIAL --

OH, CAN WE GO DARK ON THE OUTSIDE, PLEASE? OKAY, GREAT.

-- IT'S QUALCOMM CONFIDENTIAL AND PROPRIETARY INFORMATION; CORRECT?

A. THAT IS CORRECT.

Q. AND THEY SHARE IT WITH THEIR CUSTOMERS SUCH AS HTC; CORRECT?

A. THEY SHARE IT WITH HTC.

Q. AND THIS TYPE OF DATA SHEET IS SHARED WITH, TYPICALLY, HTC ENGINEERS; RIGHT?

A. THAT IS CORRECT.

Q. OKAY. THIS IS NOT FOR MASS PUBLICATION?

A. THAT IS CORRECT.

Q. YOU HAVE TO HAVE A -- YOU'VE GOT TO BE PRETTY TECHNICAL TO READ THESE, DOCTOR; RIGHT?

A. THAT IS CORRECT.

Q. OKAY. AND LET'S TAKE A LOOK AT FIGURE 2.1, IF WE COULD, JIM, WHICH IS ON PAGE 9.

DOCTOR, THAT SHOULD BE RIGHT IN FRONT OF YOU.

A. YES.

Q. AND IF WE COULD BLOW UP THIS PLL CORE (INDICATING).

NOW, THIS IS A BLOCK DIAGRAM OF A PLL (INDICATING); CORRECT?

A. YES. AND I THINK I SHOWED THE VERY SAME ONE HERE.

Q. OR VERY SIMILAR; RIGHT?

A. NO. THE SAME ONE WAS IN MY PRESENTATION.

Q. OKAY. NOW, THIS TCXO, DOCTOR, DO YOU SEE THAT?
A. YES.
Q. THAT'S A TEMPERATURE CONTROLLED CRYSTAL OSCILLATOR; RIGHT?
A. AS I EXPLAINED, YES.
Q. AND THAT INCLUDES A CRYSTAL; RIGHT?
A. THAT'S A STABLE REFERENCE.
Q. STABLE REFERENCE. AND THAT STABLE REFERENCE IS OFF CHIP; CORRECT?
A. THAT IS CORRECT. THAT'S IN THE LITTLE SHINY BOX WHICH I HAVE SHOWN.
Q. OKAY. AND THE PLL OUT OF THE QUALCOMM CHIP SENDS THE FREQUENCY OF THAT CLOCK TO THE CPU; CORRECT?
A. THAT IS CORRECT.
Q. ALL RIGHT. AND SOMETIMES THAT'S REFERRED TO, AS YOU KNOW, CLOCK OUT OR PLL OUT; RIGHT?
A. THAT IS CORRECT.
Q. THERE'S NOT ONE STANDARD WAY YOU CAN REFER TO THAT PLL OUT; RIGHT?
A. YES.
Q. OKAY. NOW, IF WE LOOK AT PAGE 29 OF EXHIBIT 3027, AND WE CAN BLOW UP THE FIRST PART HERE, IT SAYS "OPERATION" AT THE TOP. JIM, IF WE COULD PULL THAT DOWN JUST A LITTLE BIT. IT SAYS "OPERATION" RIGHT HERE (INDICATING).
AND 5.1 STATES "OUTPUT FREQUENCIES," CORRECT; DOCTOR.
A. YES, THAT'S CORRECT.

Q. AND IT STATES THAT "THE PLL OUTPUT FREQUENCY IS GIVEN BY" -- AND THE PLL OUTPUT CLOCK IS WHAT WE JUST SAW IN FIGURE 2; RIGHT?

A. YES.

Q. OKAY. AND NOW -- AND HERE'S THE SECRET FORMULA, F CLOCK EQUALS FTCXO, AND THIS IS TIMES L TIMES 2; RIGHT? DID I READ THAT RIGHT?

A. YES.

Q. THOSE LITTLE ASTERISKS, THEY'RE THE MULTIPLICATIONS --

A. YES.

Q. -- IN THIS FORMULA?

A. YES, BECAUSE YOU HAVE -- BECAUSE YOU HAVE DIVIDED THE CLOCK BY L AND YOU DIVIDED IT AGAIN BY 2, SO YOU HAVE TO MULTIPLY TO GET THAT.

Q. AND THAT TCXO WE SAW WAS FROM FIGURE 2; RIGHT?

A. YES.

Q. AND THAT'S THE EXTERNAL REFERENCE?

A. THAT'S THE EXTERNAL REFERENCE.

Q. AND THAT'S FIXED, OR A STABLE REFERENCE?

A. THAT IS A STABLE REFERENCE.

Q. OKAY. AND NOW IF WE GO DOWN TO THE TEXT, IT STATES, THE VALID OUTPUT FREQUENCIES, RIGHT HERE (INDICATING), WITH A 19.2 MEGAHERTZ REFERENCE ARE LISTED IN TABLE 5.1. CORRECT? THAT'S WHAT IT SAYS?

A. YES.

Q. AND TABLE 5.1 IS NOT HERE, AND WE'LL GET TO THAT IN A MOMENT, BUT THIS 19.2 MEGAHERTZ IS REFERRING TO THE TCXO; CORRECT?

A. THAT IS CORRECT.

Q. AND THAT'S WHAT'S THE FREQUENCY THAT'S COMING INTO THE PLL?

A. YES, THAT'S CORRECT.

Q. THAT'S THE STABLE REFERENCE SIGNAL?

A. THAT'S THE REFERENCE THAT COMES FROM THE SHINY LITTLE HOUSING ON THE CHIP.

Q. OKAY. NOW, LET'S WALK THROUGH THIS FORMULA, DOCTOR.

MAY I APPROACH AGAIN, YOUR HONOR?

THE COURT: YOU MAY.

BY MR. SMITH:

Q. ON THIS TABLE 5-1 SAYS "PLL OUTPUT CLOCK FREQUENCIES WITH 19.2 MEGAHERTZ REFERENCE"?

A. CORRECT.

Q. AND AGAIN, THE 19.2 MEGAHERTZ REFERENCE IS REALLY THE TCXO UP THERE (INDICATING); RIGHT?

A. RIGHT.

Q. AND THIS INPUT FREQUENCY ON THE LEFT-HAND SIDE, IT'S ALWAYS 19.2; RIGHT?

A. THAT IS CORRECT.

Q. AND WHY IT'S CALLED INPUT FREQUENCY, IT'S ACTUALLY INPUTTED INTO THE PLL FROM OFF CHIP?

A. IT IS A REFERENCE, REFERENCE INPUT.
Q. FROM OFF CHIP?
A. FROM OFF CHIP.
Q. OKAY. AND THEN THE WAY THIS WORKS IS L IS REFERRED TO IN THE FORMULA UP HERE (INDICATING); CORRECT?
A. YEAH, THAT'S A DIVIDE FACTOR. THIS IS HOW MUCH THEY DIVIDE THE VCO FREQUENCY.
Q. OKAY. AND THEN THE WAY YOU SET L IS THROUGH THESE BINARY VALUES; CORRECT?
A. THAT IS THE BINARY 10.
Q. THAT'S 10, RIGHT THERE (INDICATING).
AND THIS IS A BINARY NUMBER 11 AND SO FORTH (INDICATING); CORRECT?
A. THAT IS CORRECT.
Q. OKAY. AND THEN WHEN WE SEE THE OUTPUT FREQUENCY, THIS IS WHAT COMES OUT OF THE PLL (INDICATING); CORRECT?
A. THAT IS -- YES, THAT IS THE FREQUENCY OF THE RING OSCILLATOR.
Q. OKAY. THIS -- THIS FREQUENCY IS OUTPUTTED FROM THE PLL; CORRECT?
A. FROM THE -- YES, FROM THE RING OSCILLATOR.
Q. WELL, COMING OUT OF THE PLL IS THIS FREQUENCY (INDICATING); RIGHT?
A. BECAUSE PLL IS SURROUNDING RING OSCILLATOR.
Q. NO, I UNDERSTAND. I'M JUST ASKING YOU, IT COMES OUT OF

THE PLL, THOUGH; RIGHT?

A. IT COMES OUT OF -- IT CORRECTLY COMES OUT OF THE RING OSCILLATOR.

BUT IF YOU PUT A BOX AROUND IT AND CALL IT PLL, THEN IT COMES OUT OF THE PLL.

Q. OKAY. AND THE WAY YOU GET THERE, DOCTOR, AND LET ME -- LET'S MOVE BACK A LITTLE BIT.

SO THE USER, LIKE HTC, WOULD GET TO DECIDE WHAT FREQUENCY THEY WANT TO COME OUT OF THAT PLL; RIGHT?

A. THAT IS CORRECT.

Q. THAT'S THE PURPOSE OF A PLL? YOU CAN STABILIZE OR FIX THE DIFFERENT FREQUENCIES?

A. TO ADJUST THE FREQUENCY OF THE RING OSCILLATOR WILL BE WITH RESPECT TO REFERENCE -- JUST LIKE YOUR CRUISE CONTROL. SO THIS IS WHERE YOU'RE SETTING YOUR CRUISE CONTROL (INDICATING).

Q. SO YOU CAN SET THESE VALUES DIFFERENTLY DEPENDING UPON WHAT YOU WANT TO ACHIEVE IN THE PHONE; CORRECT?

A. THAT IS CORRECT.

Q. OKAY. NOW, THE WAY THIS WORKS -- LET'S GO THROUGH THE FIRST ONE. HERE WE HAVE THE REFERENCE SIGNAL COMING IN, RIGHT, 19.2?

A. YES.

Q. AND IT'S MULTIPLIED BY L, TIMES 10, RIGHT? AND THEN IT'S MULTIPLIED BY 2 AGAIN. SO 19.2 TIMES L, WHICH IS 10, TIMES 2, GIVES YOU THE 384; CORRECT?

A. OKAY. LET ME JUST EXPLAIN.
Q. NO, NO. CAN YOU JUST ANSWER MY QUESTION, DOCTOR? DID I DO THE MATH RIGHT?
A. YOU HAVE -- BECAUSE YOU DIVIDED. YOU DIVIDED IT BY 2. YOU DIVIDED -- YOU DIVIDED THE 384 BY 10, YOU GET 38, YOU DIVIDE IT BY 2, YOU GET 19.2 SO YOU CAN COMPARE THOSE TWO REFERENCES.
THE PLL DOESN'T MULTIPLY. IT DIVIDES.
Q. SO, DOCTOR, YOU'RE DISAGREEING WITH THIS QUALCOMM DOCUMENT; CORRECT?
A. WHAT THEY HAVE PRESENTED --
Q. NO. DOCTOR, CAN YOU JUST ANSWER MY QUESTION?
A. THERE IS A RELATIONSHIP BETWEEN --
MR. SMITH: YOUR HONOR --
THE WITNESS: -- BETWEEN THE CLOCK AND THE REFERENCE, BUT THAT DOES NOT DESCRIBE HOW PLL WORKS. IT JUST TELLS YOU, IF YOU SET THAT ON 10, THIS IS WHAT YOU'RE GOING TO GET OUT.
THE COURT: MR. SMITH, DO YOU WISH TO RAISE AN OBJECTION OR MAKE A REQUEST?
MR. SMITH: I DON'T WANT TO BE ARGUMENTATIVE, YOUR HONOR. I JUST ASKED A VERY SIMPLE QUESTION AND I WOULD INSTRUCT THE WITNESS NOT TO --
THE COURT: YOU'RE ASKING ME TO GIVE THE WITNESS AN INSTRUCTION TO THE WITNESS?
MR. SMITH: YES.

THE COURT: MR. MARSH?

MR. MARSH: YOUR HONOR, WE WOULD JUST ASK THAT THE WITNESS BE PERMITTED TO ANSWER WITHOUT INTERRUPTION.

THE COURT: OKAY. SO LET ME JUST REITERATE SOME GROUND RULES.

DR. OKLOBDZIJA, YOU, LIKE ALL WITNESSES, MUST ANSWER A QUESTION PUT TO YOU IN CROSS-EXAMINATION WITH A "YES" OR "NO" OR "I DON'T KNOW," ASSUMING THE QUESTION ASKS FOR THAT TYPE OF RESPONSE.

MR. MARSH WILL GIVE YOU AN OPPORTUNITY TO CLARIFY ANY CONCERNS YOU MAY HAVE IN HIS REDIRECT.

AS FOR LETTING THE WITNESS ANSWER THE QUESTION, THAT'S A FAIR REQUEST AS WELL.

MR. OKLOBDZIJA, I'M SURE IF YOU ANSWER THE QUESTION, HE WILL GIVE YOU A FULL OPPORTUNITY TO GIVE YOUR ANSWER.

BUT LET'S PROCEED ON THOSE LINES SO WE DON'T WASTE THE JURY'S TIME.

MR. SMITH: THANK YOU, YOUR HONOR.

THE COURT: MR. SMITH, GO AHEAD.

MR. MARSH: THANK YOU, YOUR HONOR.

BY MR. SMITH:

Q. SO, DR. OKLOBDZIJA, YOU WOULD AGREE WITH ME, 19.2 TIMES 10 TIMES 2 EQUALS 384; CORRECT?

A. THAT IS THE BASIC MATH.

Q. THAT'S THE BASIC MATH THAT'S IN THIS DOCUMENT; CORRECT?

A. THAT THEY PUT IN A DOCUMENT TO, TO TELL PEOPLE HOW CAN THEY GET THE REFERENCE FREQUENCY OR HOW CAN THEY HAVE THE OUTPUT FREQUENCY WITH RESPECT TO THE REFERENCE, WHICH IS 19.2.

Q. OKAY. AND IT'S ALL BASED UPON THIS FORMULA (INDICATING); CORRECT?

A. THIS FORMULA SHOWS THE RELATIONSHIP TO IT.

Q. OKAY. WE CAN TAKE THAT ONE DOWN. THANK YOU, DOCTOR.

NOW, DR. OKLOBDZIJA, ONE OF THE -- LET'S SWITCH GEARS. LET ME TELL YOU WE'RE GOING TO SWITCH GEARS. WE'RE OFF THE SECRET FORMULA. LET'S TALK ABOUT BINNING.

A. ALL RIGHT.

Q. ALL RIGHT. NOW, BINNING HAS BEEN AROUND FOR A LONG TIME; RIGHT?

A. NOT FOR SUCH A LONG TIME. I BELIEVE THAT, YOU KNOW, THE FIRST HALF OF THE TECHNOLOGY LIFE THERE WAS NO BINNING. IT CAME LATER WHEN VARIATIONS INCREASED.

Q. IT WAS THERE BY THE EARLY '80S; RIGHT?

A. FOR SOME HIGH SPECIALTY PARTS.

Q. OKAY. AND IF WE CAN GO BACK TO THE ELMO, AND JUST SO WE CAN ORIENT OURSELVES, WHEN YOU PUT UP -- I PUT UP CLAIM 16, OR 13, I BELIEVE, AND WE HAD THE PINK OR PURPLE VARYING TOGETHER, THAT'S THE SECOND ELEMENT, RIGHT?

A. ELEMENT B.

Q. ELEMENT B. SO WE'VE MOVED ON FROM ELEMENT A. NOW WE'RE ON ELEMENT B; RIGHT?

A. THAT'S CORRECT.
Q. NOW, BINNING, YOU SAID BINNING IS ONE OF THE REASONS WHY YOU BELIEVE THAT THE VARYING TOGETHER ELEMENT WAS INFRINGED; CORRECT?
A. WELL, BECAUSE THEY VARY TOGETHER WHEN YOU PUT THEM IN THE FAST BIN, THEY'RE FAST TOGETHER. WHEN YOU PUT THEM IN THE SLOW BIN, THEY'RE SLOW TOGETHER.
Q. SO YOU, YOU SAY THE HTC PHONES INFRINGE THE VARYING TOGETHER LIMITATION BECAUSE OF BINNING; CORRECT?
A. THAT IS CORRECT.
Q. OKAY. NOW, LET'S GO THROUGH THE PROCESS OF BINNING IN A LITTLE BIT OF DETAIL. OKAY?
A. ALL RIGHT.
Q. THE CHIPS ARE BASICALLY SORTED BY SPEED CAPABILITY.
YOUR HONOR, MAY I APPROACH AGAIN?
THE COURT: YOU MAY, MR. SMITH.
MR. SMITH: THANK YOU.
Q. BY SPEED; RIGHT? 800 MEGAHERTZ, 1.0 GIGAHERTZ, AND THIS LOOKS LIKE 1.3 GIGAHERTZ; CORRECT?
A. YEAH. THAT'S ILLUSTRATION.
Q. AND SO THE CHIPS -- AND THE SPEED WE'RE TALKING ABOUT IS CAPABILITY; RIGHT?
A. WHEN YOU BIN, IT'S THE ACTUAL SPEED.
Q. WELL, YOU COULD SET THE SPEED LOWER THAN 800 MEGAHERTZ; CORRECT?

THE COURT: ANY OBJECTION TO INCLUDING THOSE IN THE RECORD?

MR. MARSH: NO OBJECTION, ASSUMING THEY'RE NOT SUBSTANTIVE EVIDENCE.

THE COURT: OKAY. THEY WILL NOT BE MOVED INTO EVIDENCE. THEY'RE SIMPLY INCLUDED IN THE RECORD AS REQUESTED BY MR. SMITH.

ALL RIGHT. LET'S BRING THE JURY BACK IN.

(JURY IN AT 3:15 P.M.)

THE COURT: MEMBERS OF THE JURY, BEFORE WE BROKE, WE WERE HEARING TESTIMONY FROM DR. PROWSE.

MR. LANSKY, YOU MAY RESUME YOUR EXAMINATION.

MR. LANSKY: THANK YOU, YOUR HONOR. WELCOME BACK, EVERYONE.

COULD WE GET THE SLIDES BACK UP. GREAT, THANK YOU.

Q. SO DR. PROWSE, WE SPOKE A LITTLE BIT ABOUT THESE GEORGIA-PACIFIC FACTORS. DID YOU CONSIDER ALL OF THOSE FACTORS IN MAKING YOUR ANALYSIS?

A. YES, I DID. I DID CONSIDER ALL OF THEM. SOME OF THEM DIDN'T HAVE MUCH, IF ANY, IMPACT ON THE ANALYSIS, THOUGH.

Q. OKAY. BEFORE WE GET INTO ALL OF THOSE GEORGIA-PACIFIC FACTORS WERE, LET'S NOT VARY.

CAN YOU TELL US WHAT YOUR ULTIMATE CONCLUSION WAS AS A RESULT OF A HYPOTHETICAL NEGOTIATION BETWEEN TPL AND HTC?

A. YES, AND I'VE PREPARED A SLIDE. OBVIOUSLY WE'RE NOW ON

THE BOTTOM LINE, HOW MUCH IS THE TOTAL ROYALTY AFTER APPLYING A ROYALTY RATE TO A ROYALTY BASE TO COME UP WITH A LUMP SUM, AND IN MY OPINION, A PERCENTAGE ROYALTY OF .125 PERCENT WOULD ADEQUATELY COMPENSATE TPL FOR USE OF THE '336 PATENT. SO THAT'S MY ROYALTY RATE.

AND YOU CAN SEE THE CALCULATION I DO AT THE BOTTOM THERE TAKING THE ROYALTY BASE AND -- OF ALMOST $8 BILLION, MULTIPLYING THAT BY THE .125 PERCENT RATE GETS A ROYALTY AMOUNT OF $9.985 MILLION, IN OTHER WORDS, JUST A LITTLE UNDER $10 MILLION.

NOW, YOU'LL SEE I HAVE A DEDUCTION THERE OF 5 PERCENT. I'LL TALK ABOUT THAT A LITTLE BIT LATER IN DETAIL, BUT THAT HAS TO DO WITH A PATENT THAT WAS FORMERLY IN THE CASE THAT IS NO LONGER IN THE CASE, DEDUCTING FOR THAT.

SO AFTER I DEDUCT FOR THAT, MY TOTAL DAMAGES AMOUNT FOR INFRINGEMENT OF THE '336 PATENT IS $9,486,266, OR APPROXIMATELY $9.5 MILLION.

Q. THANK YOU. AND NOW THAT WE'VE HEARD YOUR OPINION ON THE ROYALTY THAT HTC OWES, LET'S DIG A LITTLE DEEPER INTO HOW YOU GOT THERE.

SO THERE WERE A LOT OF WORDS ON THE SCREEN WHEN WE HAD THE GEORGIA-PACIFIC FACTORS UP THERE. IS THERE AN EASIER WAY TO LOOK AT THOSE?

A. YES, THERE IS, AND I'VE SORT OF SHORTENED THE WORDS AND I'VE BUCKETED THE DIFFERENT FACTORS INTO DIFFERENT AREAS, OR

DIFFERENT TOPICS.

SO THERE'S A GROUP OF FACTORS 1, 2, 3, 4, AND 7 THAT HAVE TO DO WITH LICENSING, LICENSING PRACTICES, RATES RECEIVED FROM LICENSING THE PATENT-IN-SUIT, THAT'S THE LICENSING BUCKET.

THERE'S A FINANCIAL/BUSINESS BUCKET WHICH HAS -- WHICH IS FACTORS 5, 6, 8, 12, AND 13, WHICH HAVE TO DO WITH FINANCIAL AND ECONOMIC FACTORS RELATING TO THE PRODUCT THAT PRACTICES THE PATENT GENERALLY.

THEN THERE'S A GROUP OF TECHNICAL, MORE TECHNICAL FACTORS THAT COVER THE BENEFITS OF THE PATENTED FEATURE IN THE PRODUCT, AND THOSE ARE FACTORS 9, 10, AND 11.

FINALLY, THERE ARE TWO MORE GENERAL FACTORS, THE OPINION OF QUALIFIED EXPERTS AND 15, THE ONE WE'VE ALREADY TALKED ABOUT, THE HYPOTHETICAL NEGOTIATION BETWEEN THE LICENSOR, TPL, AND THE LICENSEE, HTC.

Q. SO LET'S TRY TO STREAMLINE THIS EVEN MORE. ARE THERE ANY FACTORS THAT YOU FOUND TO BE MORE RELEVANT THAN THE OTHER FACTORS IN YOUR ANALYSIS?

A. YES. AND I'VE BOLDED THOSE FACTORS THAT ARE THE MOST IMPORTANT AND THAT WE'LL SPEND THE MOST TIME TALKING ABOUT.

YOU'LL SEE TWO FACTORS IN THE LICENSING BUCKET; TWO IN THE FINANCIAL/BUSINESS BUCKET; THREE IN THE TECHNICAL BUCKET; AND THE TWO FINAL ONES IN THE GENERAL BUCKET.

Q. SO LET'S JUST JUMP RIGHT IN. CAN YOU WALK US THROUGH THE FACTORS IN THE LICENSING BUCKET?

B-U-N-D-E-S-P-O-S-T; LAST WORD, B-E-R-L-I-N.

THE REPORTER: THANK YOU.

THE WITNESS: THAT'S A MOUTHFUL, I KNOW.

BY MS. KEEFE:

Q. IS THERE A TRANS -- I'M NOT EVEN GOING TO TRY. IS THERE A TRANSLATION FOR THE SCHOOL?

A. IT'S THE ENGINEERING SCHOOL OF THE GERMAN BUNDESPOST, WHICH IS THE PTT OR THE POST -- HOW DO YOU CALL IT -- KIND OF LIKE U.S. POSTAL. THEY OWNED THE TELECOMMUNICATIONS PIECE BACK IN THE DAY BEFORE IT WAS PRIVATIZED AS THE TELECOM, WHICH ALSO OWNS T-MOBILE HERE IN THE U.S.

Q. SO THE --

A. SO IT WAS -- THEY HAD THEIR OWN ENGINEERING SCHOOL AND I DECIDED TO GO THERE.

Q. SO JUST SO I UNDERSTAND, THE SCHOOL ACTUALLY IS SPECIFICALLY AFFILIATED WITH TELECOMMUNICATIONS; IS THAT RIGHT?

A. IT'S A PURE BRED TELECOMMUNICATIONS SCHOOL. IT WAS ACTUALLY THE SCHOOL. IT'S MERGED WITH A DIFFERENT SCHOOL SINCE THE REUNIFICATION IN 1990, BUT IT WAS A PURE BRED TELECOM SCHOOL THAT JUST SPIT OUT ENGINEERS, NOTHING ELSE.

Q. AND WHY DID YOU CHOOSE THAT SCHOOL?

A. YOU KNOW, IT WAS A SCHOOL THAT WAS KNOWN FOR A VERY NO NONSENSE ENGINEERING CURRICULUM. IT WAS AN OPPORTUNITY TO GET THROUGH ENGINEERING SCHOOL WITHIN THREE YEARS, WHICH I APPRECIATED BECAUSE I WANTED TO GET TO WORK FAIRLY QUICKLY.

AND I JUST -- I JUST LIKED THE CURRICULUM AND JUMPED ON IT.

Q. AND WHY DID YOU CHOOSE TELECOMMUNICATIONS?

A. YOU KNOW, IT'S -- I WAS -- I WAS LOOKING AT TWO DIFFERENT, VERY DIFFERENT THINGS. I WAS LOOKING AT ARTISTRY OR ENGINEERING. IT MIGHT SOUND STRANGE. THE GOOD THING NOW IS THAT ARTISTRY IS A BETTER HOBBY THAN ENGINEERING WOULD PROBABLY BE.

I LIKED ENGINEERING BECAUSE IT WAS TECHNICALLY A HIGHLY INTERESTING FIELD AND ENGINEERING IS VERY APPLICABLE, MORE APPLICABLE THAN I THOUGHT PHYSICS WOULD HAVE BEEN.

SO -- AND I LIKE TELECOMMUNICATION BECAUSE I WAS INTERESTED IN RADIO FREQUENCY TECHNOLOGIES.

Q. SO THE JURY HAS BEEN HEARING A NUMBER OF TECHNICAL TERMS AND I JUST WANT TO ASK IF YOU HAPPEN TO KNOW WHAT THOSE TECHNICAL TERMS ARE.

A. SURE.

Q. HAVE YOU HEARD OF A PLL?

A. PHASE LOCK LOOP, YES. IT'S ESSENTIALLY A NUMBER OF COMPONENTS THAT CREATE A FIXED CLOCK FOR A SYSTEM, USUALLY SOMETHING YOU LEARN IN ENGINEERING SCHOOL SECOND, THIRD SEMESTER.

Q. AND HAVE YOU HEARD OF THE TERM "CRYSTAL CLOCK," OR "CRYSTAL OSCILLATOR"?

A. YEAH. CRYSTAL OSCILLATOR IS A COMPONENT THAT YOU PUT A

VOLTAGE ON THE COMPONENT AND THEN IT STARTS OSCILLATING AT A FIXED FREQUENCY. IT'S ALSO PART OF A PLL. IT FEEDS A PLL AND MAKES SURE THAT THE PLL HAS A REFERENCE SIGNAL.

Q. HAVE YOU HEARD OF THE TERM "RING OSCILLATOR"?

A. YEAH. RING OSCILLATORS ARE USED TO CREATE HIGHER FREQUENCY CLOCKS BECAUSE OSCILLATORS -- CRYSTALS CAN ALSO ONLY CREATE CLOCKS UP TO A CERTAIN LEVEL, SO RING OSCILLATORS ARE USED TO CREATE HIGHER FREQUENCY CLOCKS AND THEY'RE USUALLY USED ON CHIPS.

Q. SO LET'S GO BACK TO YOUR WORK AT HTC. YOU SAID YOU WERE THE VICE-PRESIDENT OF PRODUCT AND OPERATION. THERE WAS A PRODUCT MANAGEMENT PIECE, AND AN OPERATIONS PIECE; CORRECT?

A. YES.

Q. HOW LONG HAVE YOU BEEN AT HTC?

A. I JOINED HTC IN NOVEMBER 2009, SO ABOUT FOUR YEARS NOW.

Q. HAS YOUR JOB ALWAYS BEEN ROUGHLY THE SAME AS IT IS NOW?

A. THERE WERE A FEW MODIFICATIONS. I STARTED OUT AS THE V-P OF PRODUCT AND PLANNING, AND THEN FOR ABOUT A YEAR I WAS RUNNING THE BUSINESS. I WAS THE INTERIM PRESIDENT OF HTC NORTH AMERICA. MY BOSS HAD MOVED UP TO A GLOBAL ROLE AND I WAS ASKED TO STEP IN UNTIL WE HAD FOUND A, A SUCCESSOR FOR MY BOSS. I DID THAT FOR ABOUT A YEAR.

AND AFTER THAT I TOOK THE OPERATIONS PIECE ON TOP OF WHAT I DID AT THE VERY BEGINNING.

Q. BEFORE YOU JOINED HTC, WHERE DID YOU WORK?

A. I WORKED AT FLEXTRONICS OUT OF MILPITAS HERE IN THE BAY AREA. I WAS RUNNING THEIR WHAT WE CALL ODM BUSINESS, ORIGINAL DESIGN AND MANUFACTURING BUSINESS. IT'S ESSENTIALLY A BUSINESS WHERE YOU DESIGN AND MANUFACTURE SOMETHING AND SOMEBODY ELSE PUTS THEIR NAME ON IT. WE DESIGNED PHONES FOR SONY ERICSSON, FOR RIM BLACKBERRY, FOR NOKIA, FOR LG, AND A FEW OTHERS.

AND I WAS IN CHARGE OF THAT BUSINESS FOR FLEXTRONICS RUNNING THEIR DESIGN AND MANUFACTURING.

Q. AND BEFORE FLEXTRONICS, WHERE DID YOU WORK?

A. I WAS AT SIEMENS. THAT'S A LARGE GERMAN COMPANY WHO MAKES EVERYTHING. I WAS PART OF THEIR PHONE BUSINESS RUNNING PRODUCT MANAGEMENT AND ENGINEERING FOR SIEMENS IN MY LAST JOB.

Q. AND SO --

A. AND A NUMBER OF OTHER JOBS.

Q. SO HOW DID YOU GET FROM SIEMENS AND FLEXTRONICS TO HTC?

A. IT'S ACTUALLY INTERESTING IF YOU THINK ABOUT IT BECAUSE WHILE I WAS AT SIEMENS, I LAUNCHED MY FIRST HTC PRODUCT, WHICH IS PROBABLY -- YEAH, THAT'S EXACTLY THE THING THAT YOU HAVE IN YOUR HAND. THE CODE NAME FOR THIS THING WAS BLUE ANGEL. IT WAS A DEVICE THAT --

MS. KEEFE: MAY I APPROACH, YOUR HONOR, SO THAT HE CAN SHOW THE JURY?

THE COURT: YOU MAY, YES.

THE WITNESS: IT'S A DEVICE THAT HTC HAD DEVELOPED IN 2001, AND THE PROBLEM FOR HTC AT THAT POINT WAS THEY DIDN'T

A. OF COURSE.
Q. AND AT A HIGH LEVEL, WHAT IS THE PURPOSE OF A PHASE LOCK LOOP?
A. PHASE LOCK LOOP IS USED TO PROVIDE A FIXED TARGET FREQUENCY CLOCK SIGNAL.
Q. AND GENERALLY HOW IS THAT ACHIEVED?
A. IN THE QUALCOMM FAMILY OF CHIPS, BASICALLY THERE'S A FIXED REFERENCE INPUT CLOCK THAT COMES TO A BOX, PHASE LOCK LOOP. THERE ARE ELEMENTS THAT GO INTO IT, WE CALL THEM L, M, N, DIFFERENT PARAMETERS, AND THE OUTPUT FREQUENCY OF THE PHASE LOCK LOOP WOULD BE A MATHEMATICAL FORMULA OF THOSE ELEMENTS MULTIPLIED BY THE INPUT REFERENCE CLOCK FREQUENCY.
Q. MR. DENA, DO YOU MIND DRAWING A LITTLE BIT ABOUT WHAT YOU JUST TESTIFIED TO?
A. SURE.
Q. AND SHOW US HOW THIS WORKS?
YOUR HONOR, MAY HE HAVE PERMISSION AND CAN I APPROACH?
THE COURT: YOU MAY. GO AHEAD.
MR. SMITH: THANK YOU, YOUR HONOR.
Q. YOU MAY HAVE TO COME THIS WAY SO HIS HONOR AND THE JURY CAN SEE.
A. OKAY.
THE COURT: MR. MARSH, IF YOU NEED TO ADJUST YOUR PLACE, YOU PLAY.
MR. MARSH: THANK YOU, YOUR HONOR.

BY MR. SMITH:

Q. AND IF YOU DON'T MIND SKETCHING OUT FOR US, AT A HIGH LEVEL -- I UNDERSTAND IT'S A LITTLE BIT MORE COMPLICATED -- BUT AT A HIGH LEVEL WHAT YOU'VE JUST TALKED ABOUT.

A. SO THERE'S THE, THE VERY FIRST ELEMENT IS A FIXED INPUT CLOCK FREQUENCY (INDICATING).

Q. WHAT IS THAT?

A. IT'S COMING FROM AN EXTERNAL CHIP CRYSTAL, WE CALL IT TCXO. IT STANDS FOR TEMPERATURE COMPENSATED CRYSTAL OSCILLATOR.

Q. OKAY.

A. THE BOX I'M DRAWING IS BASICALLY THE PLL SYSTEM ITSELF (INDICATING).

Q. SO MR. DENA, IS THE TCXO PART OF THE CHIP?

A. NO. THE CRYSTAL RESIDES OUTSIDE THE CHIP.

Q. OKAY. PLEASE CONTINUE.

A. THERE ARE WHAT WE CALL REGISTERS THAT ARE 32 BIT WIDE, AND THEY'RE BASICALLY REPRESENTING THE BINARY VALUE OF THE NUMBER. SO FOR COURT PURPOSES, WE CAN IMAGINE THESE ARE JUST L, M, AND N, OR A SERIES OF NUMBERS (INDICATING).

Q. HOLD ON, MR. DENA. LET ME SEE IF WE CAN GET A BETTER VIEW HERE.

EXCUSE ME. THANK YOU.

A. AND THEN BASICALLY OF THE PLL OUTPUT, WHICH ESSENTIALLY IS THE CLOCK THAT WE USE FOR THE REST OF THE CHIP (INDICATING).

SO THIS SYSTEM THAT I'VE SHOWN IS THE SOURCE OF ALL CLOCKS ON THE CHIPS, AND WE HAVE MULTIPLE OF THESE DEPENDING ON THE CHIP, AND IN SOME CHIPS YOU HAVE FOUR, SOME CHIPS YOU HAVE FIVE, SEVEN, SIX, DEPENDING ON THE CHIP APPLICATION.

NOW, IN THIS PARTICULAR CASE -- SO ON THE REFERENCE INPUT FREQUENCY, THE REFERENCE INPUT HAS A FREQUENCY ASSOCIATED WITH IT (INDICATING), AND THEN YOU HAVE THE CLOCK OUTPUT THAT HAS A FREQUENCY ASSOCIATED WITH IT (INDICATING).

IN A NUTSHELL, PLL USE THAT FORMULA TO CREATE A FREQUENCY A LOT LARGER IN MAGNITUDE THAN THE INPUT FREQUENCY THAT IT RECEIVES, AND THAT FORMULA BASICALLY IS DICTATED IN THIS -- IN THIS PARTICULAR CASE I'M SHOWING THE CLOCK FREQUENCY, WHICH MEANS THE OUTPUT FREQUENCY, L PLUS M OVER N MULTIPLIED BY THE INPUT FREQUENCY (INDICATING).

SO YOU CAN IMAGINE IF YOU WANTED TO MULTIPLY THE FREQUENCY OF THE PLL TO BE TEN TIMES, 10.25 TIMES THE INPUT FREQUENCY, YOU PUT 10 FOR L AND YOU PUT 1 OVER 4 FOR M AND N, AND THAT BASICALLY DOES THE JOB (INDICATING).

OF COURSE YOU HAVE TO GO THROUGH THE PERIOD OF WAITING FOR THE PLL TO LOCK UNTIL THE STEADY OUTPUT IS ACHIEVED, AND THEN FROM THEN ON, THE TARGET, THE OUTPUT FREQUENCY IS ALWAYS CONSTANT.

Q. IS THERE ANY SIGNIFICANCE FOR THE OUTPUT SIGNAL TO BE CONSTANT?

A. IT'S CRITICAL FOR THE CHIP PERFORMANCE.

THEY WERE POWERED UP WITHOUT THE EXTERNAL CLOCK CONNECTED?

"THE WITNESS: RING OSCILLATORS ON THEIR OWN REALLY HAVE LITTLE SIGNIFICANCE. RING OSCILLATORS ARE ONE OF THE COMPONENTS THAT BUILD THE PLL SYSTEM TOGETHER, INCLUDING THEIR INPUT REFERENCE CLOCK.

IF THEY ARE POWERED UP, RING OSCILLATOR COULD BE RUNNING. IT'S ON A STABLE CIRCUIT BY NATURE."

HE DID SAY THAT, DIDN'T HE?

A. YEAH. I HAVE NO IDEA WHAT HE MEANS BY STABLE THERE, OTHER THAN PERHAPS THEY'RE STABLE IN THE SENSE THAT YOU CAN RELY ON THEM OSCILLATING WHEN YOU PROVIDE POWER.

Q. BUT AT LEAST YOU DO AGREE THAT HE SAID THAT WHEN YOU WEREN'T HERE ON FRIDAY?

A. I READ IT AND I'M AWARE THAT HE SAID IT AND HE WENT ON TO SAY SOME THINGS THAT -- WELL, I'M SURE MY COUNSEL WILL BRING SOMETHING UP IF THERE'S ANYTHING PERTINENT THAT HE ALSO SAID.

Q. I'M SURE HE WILL.

NOW, YOU WOULD ALSO AGREE THAT THE VCO, IN OTHER WORDS, THE RING OSCILLATOR, THAT IT IS THE VCO IN THE RING OSCILLATOR THAT GENERATES THE CLOCK SIGNAL FOR THE CPU; RIGHT?

A. IT GENERATES IT USING THE EXTERNAL CRYSTAL, BUT IT DOES GENERATE IT. THAT'S WHERE THE 2 GIGAHERTZ COMES FROM.

Q. OKAY. SO YOU'RE SAYING THAT THE RING OSCILLATOR GENERATES THE 2 GIGAHERTZ SIGNAL THAT CLOCKS A CPU; CORRECT?

A. THAT'S NOT ALL THE WORDS I SAID AND I'M NOT GOING TO

INSIST ON READING THE ENTIRE CLAIM AND THE ENTIRE JUDGE'S CONSTRUCTION. OTHERWISE WE DON'T KNOW WHAT THE HECK WE'RE TALKING ABOUT HERE.

Q. WELL, LET'S SEE WHAT YOU SAID IN YOUR EXPERT REPORT. LET'S TAKE A LOOK AT THAT, BECAUSE IN YOUR EXPERT REPORT, YOU SAID THE SELECTED ICO PROVIDES THE PLL OUTPUT SIGNAL THAT IS USED AS A CLOCK SIGNAL.

DO YOU DISAGREE WITH THAT?

A. NO, I DO NOT.

Q. THANK YOU.

NOW LET'S TAKE A LOOK -- GO BACK TO DDX-38, PLEASE.

TAKE A LOOK AT THE EQUATION AT THE BOTTOM. DO YOU AGREE WITH THAT MATH? IS THAT RIGHT?

A. YES, THAT MATH ACCURATELY DESCRIBES THE OPERATION OF THIS EXAMPLE HYPOTHETICAL --

Q. SO YOU'VE GOT -- I'M SORRY.

A. -- HYPOTHETICAL PLL.

Q. OKAY. SO YOU'VE GOT A 2.0 GIGAHERTZ CLOCK SIGNAL GENERATED BY THE RING OSCILLATOR THAT'S CLOCKING THE CPU, AND YOU DIVIDE BY 100, AND THAT'S WHAT THIS CIRCUITRY ACTUALLY DOES; CORRECT?

A. YES.

Q. TO GET A 20 MEGAHERTZ SIGNAL SO THAT YOU CAN DO EDGE MATCHING WITH THE EXTERNAL REFERENCE CRYSTAL SIGNAL IN THE PHASE DETECTOR; CORRECT?

A. YES. THAT FORMULA GETS CAUSE AND EFFECT BACKWARDS, BUT THAT IS THE RIGHT RELATIONSHIP.

Q. WELL, IT GETS CAUSE AND EFFECT BACKWARDS? IS THAT WHAT YOU SAID?

A. YES, I DID.

Q. WELL, IT DOESN'T GET WHAT THE ACTUAL MAP IS AND THE DIRECTION OF THESE SIGNALS BACKWARDS, DOES IT? BECAUSE THAT'S WITH ACTUALLY HAPPENS; RIGHT?

A. NO. AS A MATTER OF FACT, WHAT ACTUALLY HAPPENS IS THE -- IF WE TAKE MR. DENA'S TESTIMONY THAT WHEN YOU POWER ON THE RING OSCILLATOR, IT WILL WORK AT SOME FREQUENCY, IT'S CERTAINLY NOT THE ONE WE DESIRED -- THAT WITH THE MICROPROCESSOR DESIGNER DESIRES FOR THIS SYSTEM.

WHAT HAPPENS IS THE -- WHATEVER THAT RANDOM FREQUENCY IS IS BEING FED INTO THE PHASE DETECTOR ALONG WITH THE 20 MEGAHERTZ REFERENCE, ALONG WITH THE PROGRAMMING OF THE FREQUENCY DIVIDER AND THAT GENERATES AN ERROR SIGNAL --

Q. YEAH, I WAS TALKING --

A. -- SO THAT THE OUTPUT FREQUENCY THEN RESPONDS TO THE ERROR.

AND IT'S MORE ACCURATE TO SAY THAT 2 GIGAHERTZ EQUALS 20 TIMES 100 THAN IT IS TO SAY -- JUST IN TERMS OF THE SENSE OF THE CIRCUIT THAN IT IS TO WRITE IT THE WAY YOU HAVE.

Q. OKAY. YOU'RE SAYING SOMETHING ENTIRELY DIFFERENT.

ALL I'M SAYING IS THAT THIS VERY FAST 2.0 GIGAHERTZ CLOCK

SIGNAL, THE DIRECTION THAT THAT IS FED IS THIS WAY THROUGH THE FREQUENCY DIVIDER AND IT'S DIVIDED (INDICATING), IT DOESN'T GO THE OTHER WAY, IT'S NOT MULTIPLIED BECAUSE NO CIRCUIT CAN DO THAT (INDICATING), IT'S FED THROUGH THE FREQUENCY DIVIDER IN THIS DIRECTION OF THE ARROWS (INDICATING); CORRECT?

A. HOW MUCH OF WHAT YOU JUST SAID WAS A QUESTION FOR ME? BECAUSE I DISAGREE WITH SEVERAL THINGS YOU SAID.

Q. TELL ME THIS, SIR: THIS FAST 2.0 GIGAHERTZ FREQUENCY IS FED THIS WAY IN THIS DIRECTION THROUGH THE FREQUENCY DIVIDER AND IS DIVIDED DOWN TO 20 MEGAHERTZ AND FED TO THE PHASE DETECTOR (INDICATING). CORRECT?

A. YES.

Q. THANK YOU.

NOW LET ME ASK YOU A COUPLE OF QUESTIONS ABOUT THE MICROPROCESSOR CHIPS IN THE ACCUSED HTC PRODUCTS. THOSE PRODUCTS WOULD WORK JUST FINE IF YOU PULLED THE RING OSCILLATOR OUT OF THE PLL, WOULDN'T THEY?

A. THE RING?

Q. YEAH, THE RING OSCILLATOR.

A. THE RING? JUST FINE? NO, NONE OF THAT STATEMENT IS TRUE.

Q. OH. OH. SO THE PRODUCTS WOULDN'T WORK IF YOU PULLED THE RING OSCILLATOR OUT?

A. THEY WOULD WORK, BUT NOWHERE NEAR THEIR SPECIFICATION BECAUSE THEY NEED THE RING TO MULTIPLY THE REFERENCE TO GO THE SPEED THAT THEY'RE -- THAT PRODUCES THE STATED PERFORMANCE THAT

PEOPLE PAY MONEY FOR.

Q. TIME OUT ON THAT.

THIS RING OSCILLATOR DOESN'T MULTIPLY THE REFERENCE. WE JUST TALKED ABOUT HOW THE MATH GOES AND IT GOES THIS WAY (INDICATING); RIGHT?

A. YOU AND I ARE GOING TO HAVE TO DISAGREE ABOUT THE MATH. I GAVE YOU MY TESTIMONY ABOUT THE MATH AND I GAVE YOU MY TESTIMONY ABOUT CAUSE AND EFFECT.

Q. AND YOU ALSO TOLD ME THAT THE FREQUENCY DIVIDER DIVIDES THIS FAST SIGNAL AND FEEDS THE PHASE DETECTOR (INDICATING); RIGHT?

A. YES, IT DOES.

Q. THANK YOU.

NOW, EVEN THOUGH ALL OF THE ACCUSED PRODUCTS USE A RING OSCILLATOR TO GENERATE THAT VERY FAST FREQUENCY AT 500 MEGAHERTZ, 1 TO 2 GIGAHERTZ, WHATEVER IT IS, THE PRODUCTS DON'T REALLY NEED TO RUN THAT FAST TO OPERATE, DO THEY?

A. TO OPERATE AS THEY'RE SPECIFIED TO OPERATE, NO. THEY TYPICALLY DON'T RUN FULL SPEED.

Q. SO, LIKE, FOR EXAMPLE, IF WE PUT A DIFFERENT CHIP IN MY PHONE THAT DIDN'T HAVE A RING OSCILLATOR, WOULD IT -- WOULD IT BE ABLE TO ALLOW ME TO SURF THE INTERNET AND PLAY 3-D GAMES AND RECEIVE AND SEND E-MAIL AND TAKE PHOTOS AND SEND THEM AND ALL THAT?

A. YOU'RE TALKING ABOUT REDESIGNING THE PHONE AND YOU STOPPED

THAN THAT.

Q. WELL, YOU LIVE IN LAS VEGAS, RIGHT?

A. I DO.

Q. YOU'VE GOT SOME WIDE OPEN SPACES THERE WHERE YOU COULD GO FAST?

A. THE HIGHEST LEGAL LIMIT IS 75, SO I GUESS I'VE JUST ADMITTED TO INFRINGING A SPEED LAW ON THE RECORD HERE.

Q. NO WORRIES. WE WILL NOT REPORT YOU.

A. ALL RIGHT. GOOD.

Q. NOW, HAVE YOU EVER HAD THE EXPERIENCE OF DRIVING YOUR CAR, WHETHER IT WAS YOUR PRIUS OR SOME PREVIOUS CAR, ON A WINDING MOUNTAIN ROAD WHERE YOU GOT STUCK BEHIND A MOTOR HOME?

A. YES, AND THEN SOMETIMES I'VE BEEN THAT MOTOR HOME.

Q. SO YOU'VE GOT A MOTOR HOME, TOO?

A. WELL, A TRAILER.

Q. OKAY. VERY GOOD.

SO IF YOU CAN IMAGINE THIS EXAMPLE, ASSUME YOU'RE STUCK BEHIND A MOTOR HOME GOING 50 MILES AN HOUR AND IT'S A NARROW, TWO LANE ROAD, THERE'S NOT AN OPPORTUNITY FOR YOU TO PASS, YOU'VE GOT A DOUBLE YELLOW LINE, AND YOU'RE GETTING KIND OF FRUSTRATED STUCK BACK THERE IN YOUR PRIUS OR MAYBE -- WE'LL JUST PLAY FOR A MINUTE AND IMAGINE YOU'RE DRIVING A CAMARO. HOW ABOUT THAT?

A. WHY DON'T WE IMAGINE MY WONDERFUL OLD V8 ALFA?

Q. OKAY. VERY GOOD. SO AN ALFA THAT HAD A V8.

SO YOU'RE DRIVING YOUR ALFA WITH A V8, YOU'RE STUCK BEHIND THIS MOTOR HOME GOING 50 MILES AN HOUR. LET ME ASK YOU THIS: AT THAT POINT, WHICH VEHICLE IS GENERATING THE POWER FOR YOUR CAR? YOUR ALFA? OR THE MOTOR HOME?

A. MY ALFA IS GENERATING THE POWER FOR THAT CAR.

Q. NOW, THAT'S BECAUSE YOUR ALFA HAS A V8 ENGINE THAT'S GENERATING THE POWER TO MAKE IT GO 50; RIGHT?

A. YES.

Q. AND IN FACT, THAT MOTOR HOME IS NOT BEING USED TO GENERATE POWER FOR YOUR ALFA, EITHER, IS IT?

A. IT'S NOT BEING -- IT'S CERTAINLY NOT BEING USED TO GENERATE THE POWER.

IT IS, HOWEVER, BEING USED TO GENERATE THE SIGNAL THAT TELLS ME HOW MUCH POWER I WANT TO GENERATE.

Q. YEAH. IT IS LIMITING HOW FAST YOU CAN GO; RIGHT?

A. IT'S -- I WOULD SAY IT'S MORE THAN LIMITING. I'M GOING AS FAST AS IT WILL GO. IF IT SHOWS DOWN, I'LL GO THAT SPEED.

BUT I'M -- THE SPEED AT WHICH MY CAR IS GOING IS USING THE TRAILER AS A REFERENCE IN THAT SCENARIO.

Q. SO LET'S IMAGINE WE HAVE A VERY CALM AND CONSISTENT MOTOR HOME DRIVER WHO ALWAYS DRIVES AT 50 MILES AN HOUR AND YOU'RE STUCK BEHIND HIM.

THE MOTOR HOME IS NOT BEING USED TO GENERATE THE POWER OF YOUR ALFA, IS IT? IT IS LIMITING THE SPEED OF YOUR ALFA, BUT IT IS NOT BEING USED TO GENERATE THE SPEED OF YOUR ALFA; RIGHT?

A. YOU KNOW, IN THAT ANALOGY -- BECAUSE WE AREN'T TALKING ABOUT APPLES AND ORANGES HERE, WE ARE TALKING ABOUT THIS CASE AND WHETHER THE ANALOGY IS APT OR NOT IS IMPORTANT HERE, THE MOTOR HOME IS BEING USED -- IT IS BEING USED TO GENERATE THE POWER BECAUSE I AM CONTROLLING THE AMOUNT OF POWER I GET OUT OF MY ENGINE IN RESPONSE TO THE MOTOR HOME, WHICH IS REGULATING THE SPEED AT WHICH I'M GOING, JUST LIKE THE EXTERNAL REFERENCE.

Q. WELL, IT'S CERTAINLY LIMITING HOW FAST YOU CAN GO. BUT YOU'RE SAYING THAT MOTOR HOME IS GENERATING THE POWER IN YOUR ALFA'S ENGINE?

A. I DIDN'T SAY THAT.

Q. I THINK YOU DID SAY THAT.

A. ABSOLUTELY NOT.

Q. THERE ARE LIMITS FOR ALL ANALOGIES. I THINK WE'VE MADE OUR POINT THERE.

LET'S TAKE A LOOK AT THE CLAIM LANGUAGE OF THE '336 PATENT. LET'S TAKE A LOOK AT -- FIRST OF ALL, LET'S LOOK AT CLAIM 1. CLAIM 1 OF THE '336 PATENT. YEAH, GO AHEAD.

MR. LEMIEUX: YOUR HONOR?

THE COURT: YES, MR. LEMIEUX?

MR. LEMIEUX: CLAIM 1 ISN'T ASSERTED IN THIS CASE, SO I'M NOT SURE WHAT THE RELEVANCE OF THIS LINE OF QUESTIONING WOULD BE.

THE COURT: ALL RIGHT. I'LL GIVE MR. OTTESON SOME LEEWAY. WE'LL SEE WHERE THIS GOES.

INSTRUCTIONS, INSTRUCTED THE JURY ON WHICH CLAIMS ARE INCLUDED.

THE COURT: OKAY. MR. WEINSTEIN, DO YOU WANT TO RESPOND?

MR. WEINSTEIN: YES, YOUR HONOR. THERE'S ACTUALLY A FEW MORE AS WELL THAT WE IDENTIFIED.

THE COURT: OKAY.

MR. WEINSTEIN: ITEM NUMBER 2 APPEARS TO BE APPLICABLE ONLY TO CLAIMS 10 AND 16; ITEM 7, APPLICABLE TO CLAIMS 1 AND 10 ONLY; ITEM 10, THERE ARE A NUMBER OF THEM THAT WERE SORT OF GROUPED TOGETHER. THE ONLY ONE THAT IS APPLICABLE IS THE LAST ONE, VARYING THE SAME WAY. THE OTHER ONES BEFORE THE SEMICOLON THERE ARE APPLICABLE TO OTHER UNASSERTED CLAIMS.

ON NUMBER 13 AND 16, WE AGREE THOSE ARE NOT RECITED IN ANY OF THE ASSERTED CLAIMS.

IN ADDITION, I DO NOT BELIEVE MR. CARMACK MENTIONED IT, BUT I THINK 20 IS ANOTHER ONE THAT IS NOT --

THE COURT: I THINK HE DID. IT SOUNDS LIKE YOU'RE IN AGREEMENT ON THAT.

MR. WEINSTEIN: OKAY. NUMBER 26 IS DUPLICATIVE OF 21.

AND ACTUALLY, IT'S NOT -- THE CLAIM LANGUAGE DOESN'T SAY CPU, IT SAYS CENTRAL PROCESSING UNIT, SO 21 IS THE APPROPRIATE ONE. 26 CAN GO.

THE COURT: OKAY. WITH THAT, IT SEEMS AS IF YOU ALL ARE IN AGREEMENT THAT IF THE TERMS ARE USED EXCLUSIVELY IN A

CLAIM WHICH IS NO LONGER AT ISSUE IN THIS CASE, THE WISE COURSE HERE IS TO GET RID OF IT, AND I'M HAPPY TO DEFER TO YOUR JUDGMENT ON THAT.

ON THAT BASIS, I'M GOING TO DELETE FROM THIS INSTRUCTION WHAT IS PRESENTLY NUMBERED AS 2, 7, 11, 13, 16, 19, 20, 22, 25, AND 26.

WITH RESPECT TO WHAT IS PRESENTLY NUMBERED AS 10, I WILL EXCISE THE LANGUAGE "VARYING TOGETHER; VARY TOGETHER; VARYING IN THE SAME WAY."

OKAY?

MR. CARMACK: THANK YOU, YOUR HONOR.

THE COURT: ALL RIGHT. LET'S TURN TO PAGE 28, WHICH IS INFRINGEMENT. ANY OBJECTIONS?

MR. WEINSTEIN: YOUR HONOR, BEFORE WE MOVE ON.

THE COURT: OH, YES.

MR. WEINSTEIN: I JUST WANT TO MAKE SURE, WE UNDERSTAND YOU -- WE HAD EXTENSIVE ARGUMENT ABOUT THE ENTIRE OSCILLATOR TERM. WE HAD A HEARING PRIOR TO THE TRIAL AND I JUST WANTED TO MAKE SURE THAT THE OBJECTIONS THAT WE HAD REGARDING THE TWO SENTENCES THAT WE WANTED ARE STILL PRESERVED.

THE COURT: THEY ARE PRESERVED, ABSOLUTELY.

MR. CARMACK: AND OURS TOO, YOUR HONOR; CORRECT?

THE COURT: AND YOURSELF ARE ALSO PRESERVED.

MR. CARMACK: ALL RIGHT.

THE COURT: ALL RIGHT. PAGE 28, I BELIEVE THERE WERE

NO OBJECTIONS TO INFRINGEMENT. IS THAT CORRECT?

MR. CARMACK: CORRECT FOR DEFENDANTS.

THE COURT: AND FOR HTC?

MR. WEINSTEIN: THAT'S CORRECT.

THE COURT: PAYMENT 29, DIRECT INFRINGEMENT. ANY OBJECTIONS?

MR. CARMACK: NONE FROM DEFENDANTS.

MR. WEINSTEIN: NONE FROM DEFENDANTS.

THE COURT: PAGE 30, LITERAL INFRINGEMENT. ANY OBJECTIONS?

MR. CARMACK: NONE FROM THE DEFENDANTS.

MR. WEINSTEIN: JUST ONE, YOUR HONOR. THE SECOND PARAGRAPH, THE OBJECTION WE HAVE TO THE SECOND PARAGRAPH ON COMPRISING IS WE THINK IT'S ARGUABLY INTENDED IN CONTENTION WITH YOUR INSTRUCTION FOR THE ENTIRE OSCILLATOR, WHICH IS THE ENTIRE OSCILLATOR EXCLUDED ANY EXTERNAL CLOCK USED TO GENERATE THE SIGNAL USED TO CLOCK THE CPU.

WE'D ASK THAT TO BE REMOVED ONLY BECAUSE WE THINK THAT COULD INVITE SORT OF A MISLEADING ARGUMENT THAT, AN ATTEMPT TO REREAD WHAT THE EXTERNAL OSCILLATOR INSTRUCTION ACTUALLY SAYS.

THE COURT: DOES THE -- DO THE -- DOES THE CLAIM ENTIRE OSCILLATOR OR ANY OF THE VARIANTS THAT WE'VE TALKED ABOUT APPEAR IN ANY ASSERTED CLAIM WHICH ALSO INCLUDES SOME PRICING? IN OTHER WORDS, IS THE POTENTIAL FOR THIS OVERLAP BETWEEN THE TWO? I THINK THAT'S TRUE, BUT --

THAT IS SELECTED AT ANY GIVEN TIME, THAT IS USED TO THEN CLOCK THE CPU.

IN ADDITION, IN THE PLL, AS YOU KNOW, IT GOES DOWN TO THIS DIVIDE THAT DIVIDED THAT VERY, VERY FAST, HIGH FREQUENCY CLOCK SIGNAL DOWN TO, IN THE QUALCOMM CHIPS, 19.2 MEGAHERTZ (INDICATING).

WHY? BECAUSE THAT'S THE FREQUENCY OF THE TCXO (INDICATING), THE EXTERNAL REFERENCE CRYSTAL.

AND THE REASON THEY WANT THEM TO BE THE SAME FREQUENCY IS BECAUSE THEY THEN WANT TO MATCH UP THOSE SQUARE WAVES, THEY WANT TO MATCH UP THE EDGES OF THE SQUARE WAVES HERE IN THE PHASE DETECTOR (INDICATING).

AND THEN WHAT HAPPENS? THEN WHAT DOES THE PLL DO WITH THAT CLOCK SIGNAL? WELL, WHAT HAPPENS NEXT IS IT MAKES LITTLE ADJUSTMENTS WITH THE CHARGE PUMP AND IT STORES CORRECTION CHARGES HERE (INDICATING).

NOW, DO WE HAVE THAT 19.2 MEGAHERTZ CLOCK SIGNAL SQUARE WAVE CONTINUING THROUGH TO THE RING OSCILLATORS (INDICATING)? NO. NO WAY. THAT CLOCK SIGNAL FROM THE EXTERNAL REFERENCE IS NOT USED TO GENERATE THE CLOCK SIGNAL OF THE RING OSCILLATORS. IT STOPS.

WHAT GENERATES THE CLOCK SIGNAL FOR THESE CLOCK -- FOR THESE RING OSCILLATORS IS POWER, AND THEY'VE GOT THAT, ALL FOUR OF THEM HAVE THAT ALL THE TIME, EVEN THE ONES THAT AREN'T SELECTED TO BE IN THE PLL AT ANY GIVEN TIME. THEY'RE ALWAYS

GENERATING A CLOCK SIGNAL.

NOW, LET'S TAKE A LOOK AT DDX-24 IF WE COULD, PLEASE, AND WE CAN TURN THE BACK SCREEN BACK ON.

AGAIN, THIS ILLUSTRATES THE POINT I WAS MAKING EARLIER. AS WE'VE DISCUSSED, EACH OF THESE INVERTERS HAS POWER, AND IT GETS IT FROM THE CHIP'S MAIN POWER SUPPLY.

NOW, IS THERE EXTRA VOLTAGE OR CURRENT THAT IS SUPPLIED TO TRY TO REGULATE OR ADJUST THE SPEED? YES.

BUT THAT IS NOT GENERATING THE CLOCK SIGNALS.

SO THERE IS A DIFFERENCE, VERY IMPORTANT DIFFERENCE BETWEEN GENERATING A CLOCK SIGNAL, WHICH THAT HAPPENS BECAUSE THE RING OSCILLATORS HAVE POWER, THERE'S A BIG DIFFERENCE BETWEEN THAT AND REGULATING OR LIMITING THE FREQUENCY OF THAT CLOCK SIGNAL, BECAUSE FREQUENCY AND CLOCK SIGNAL ARE NOT THE SAME. FREQUENCY IS A CHARACTERISTIC OF A CLOCK SIGNAL.

THAT IS WHAT THE CRYSTAL IS USED FOR. THE CRYSTAL IS USED TO LIMIT OR REGULATE THE SPEED OF THE CLOCK SIGNAL THAT IS GENERATED BY THE RING OSCILLATOR.

NOW, WE TALKED ABOUT MR. DENA, THAT HE TESTIFIED THAT IN THE QUALCOMM CHIPS THEY'RE ALL POWERED AND THEY OSCILLATE AND GENERATE A CLOCK SIGNAL ON THEIR OWN. THEY DON'T NEED AN EXTERNAL REFERENCE CLOCK TO GENERATE A CLOCK SIGNAL.

SO, AGAIN, WHAT THAT EXTERNAL REFERENCE CRYSTAL IS USED FOR -- ARE WE DARK ON THE BACK SCREEN? SORRY. -- AGAIN, WHAT THAT EXTERNAL REFERENCE CRYSTAL IS USED FOR, IT IS USED AS A

REFERENCE. IT IS A COMPARATOR. A COMPARISON IS MADE BETWEEN THIS (INDICATING) AND THAT HERE (INDICATING).

AND THAT COMPARISON IS USED TO ADJUST THE SPEED, BUT NOT GENERATE THE CLOCK SIGNAL FROM THE RING OSCILLATOR.

NOW, YESTERDAY I DISCUSSED --

LET'S TAKE THAT DOWN. THANK YOU.

YESTERDAY I DISCUSSED AN ANALOGY WITH MR. GAFFORD TO ILLUSTRATE WHAT THE CRYSTAL IS USED FOR, AND WE'RE GOING TO PUT UP A GRAPHIC HERE TO ILLUSTRATE THAT. THAT WAS IT. YEAH, THAT'S IT.

THIS IS DDX-401. AS YOU CAN SEE, THERE IS A SPORTS CAR THAT IS TRAPPED GOING UP A HILL BEHIND AN RV, OR A MOTOR HOME, GOING UP A HILL, SOLID YELLOW LINE, CAN'T PASS. THE RV IS GOING, SAY, 50 MILES AN HOUR AND THAT SPORTS CAR WANTS TO GO FASTER THAN THAT.

SO IS THE RV LIMITING THE SPEED OF THE SPORTS CAR? YES. IT'S LIMITING THE SPEED OF THE SPORTS CAR.

BUT IS THE RV AND THE ENGINE IN THAT MOTOR HOME, IS THAT USED TO GENERATE THE CLOCK SIGNAL, OR THE ENGINE POWER FOR THE SPORTS CAR? NO WAY. NO WAY. THE SPORTS CAR HAS ITS OWN ENGINE, GENERATES ITS OWN POWER.

SO WHAT THE RV IS DOING IS LIMITING THE SPEED THAT THE SPORTS CAR CAN GO, BUT IT'S NOT USED TO GENERATE THE POWER FOR THAT SPORTS CAR.

AND INITIALLY YESTERDAY, AT LEAST INITIALLY, MR. GAFFORD

AGREED WITH ME THAT THE MOTOR HOME WAS NOT GENERATING THE POWER FOR HIS SPORTS CAR WHEN HE WAS STUCK BEHIND IT, AND THAT -- AND HE ALSO AGREED INITIALLY THAT THE MOTOR HOME WAS NOT BEING USED TO GENERATE THE POWER FOR THE SPORTS CAR.

LET'S LOOK AT WHAT HE SAID.

OH, NO. WE NEED TO GO TO THE TESTIMONY, BILL. DO YOU HAVE THAT? THIS IS AT 1382, 1 THROUGH 14.

OKAY. SO I SAID, "SO YOU'RE DRIVING YOUR ALFA, YOU'RE STUCK BEHIND THIS MOTOR HOME GOING 50. AT THAT POINT, WHICH VEHICLE IS GENERATING THE POWER FOR YOUR CAR? YOUR ALFA? OR THE MOTOR HOME?"

HE SAYS, "MY ALFA IS GENERATING THE POWER FOR THAT CAR."

AND THEN I COME DOWN HERE AND I SAY, HEY, "IN FACT, THAT MOTOR HOME IS NOT BEING USED TO GENERATE POWER FOR ALFA, EITHER, IS IT?"

HE SAYS, "IT'S NOT BEING -- IT'S CERTAINLY NOT BEING USED TO GENERATE THE POWER. IT IS, HOWEVER, BEING USED TO GENERATE THE SIGNAL THAT TELLS ME HOW MUCH POWER I WANT TO GENERATE."

YEAH, THAT'S RIGHT. THAT MOTOR HOME IS NOT BEING USED TO GENERATE THE POWER FOR HIS CAR, BUT IT IS A CUE TO HIM. SO IT DOES LIMIT HIS SPEED.

BUT, AGAIN, HE DECIDED HE DIDN'T REALLY LIKE THE WAY THE QUESTIONS WERE GOING, SO LET'S SEE WHAT HE SAID ON THE NEXT PAGE AT 1382:20 TO 1383:13.

SO HE SAID -- TAKE THE BACK ONE FIRST THERE, YEAH. "SO

THE COURT: MR. RIVERA, WOULD YOU PLEASE BRING THE JURY BACK IN?

THE CLERK: YES, YOUR HONOR.

(JURY IN AT 3:17 P.M.)

THE COURT: MEMBERS OF THE JURY, IT'S NOW TIME FOR CLOSING ARGUMENT BY HTC.

MS. KEEFE, YOU MAY PROCEED.

MS. KEEFE: THANK YOU, YOUR HONOR.

(MS. KEEFE GAVE HER CLOSING ARGUMENT ON BEHALF OF THE PLAINTIFFS.)

MS. KEEFE: AND THANK YOU, LADIES AND GENTLEMEN.

I ASKED YOU IN THE VERY BEGINNING, I THINK I EVEN ASKED YOU ALL THE WAY BACK WHEN WE WERE FIRST TALKING TO YOU ABOUT WHETHER OR NOT YOU WERE GOING TO BE ON THIS JURY, TO WAIT UNTIL YOU HEARD THE REST OF STORY AND GIVE ME A CHANCE TO TELL MY PART.

AND SO THANK YOU SO MUCH FOR DOING JUST AND FOR LETTING ME NOW TELL THE REST OF THE STORY AND REALLY REMIND YOU OF THE EVIDENCE THAT CAME IN HERE, THE EVIDENCE THAT CAME IN THROUGH OUR WITNESSES.

I WAS ACCUSED A LITTLE WHILE OF AGO OF BEING PART OF A TEAM THAT DIDN'T REALLY USE THE CLAIM, DIDN'T REALLY USE THE JUDGE'S CLAIM CONSTRUCTION, SO LET'S START THERE. LET'S START RIGHT THERE, BECAUSE HTC DOES NOT INFRINGE THESE CLAIMS AS CONSTRUED BY THE COURT.

CAN WE ACTUALLY JUST START WITH THE SLIDES, PLEASE?

SO THE FIRST THING I DID WAS TOOK THE LANGUAGE FROM THE CLAIM, THIS IS THE CLAIM THAT YOU'RE GOING TO BE ASKED TO SEE WHETHER OR NOT WE INFRINGE, AND WE ARE GOING TO FOCUS ON TWO LIMITATIONS, AND THE LIMITATIONS ARE JUST BITS AND PARTS OF THAT CLAIM ITSELF.

AND THE TWO LIMITATIONS THAT WE'RE GOING TO FOCUS ON ARE RIGHT HERE: "DOES HTC HAVE AN ENTIRE OSCILLATOR DISPOSED UPON SAID INTEGRATED CIRCUIT SUBSTRATE AND CONNECTED TO SAID CENTRAL PROCESSING UNIT, SAID OSCILLATOR CLOCKING SAID CENTRAL PROCESSING UNIT AT A CLOCK RATE BEING CONSTRUCTED," ET CETERA.

PATENT LANGUAGE FOR: "IN THIS CLAIM, YOU HAVE TO HAVE AN ENTIRE OSCILLATOR ON THE SUBSTRATE, THAT OSCILLATOR CLOCKS THE CPU."

AND THEN WE KNOW FROM HIS HONOR THAT "THE 'ENTIRE OSCILLATOR' IS PROPERLY UNDERSTOOD TO EXCLUDE ANY EXTERNAL CLOCK USED TO GENERATE THE SIGNAL USED TO CLOCK THE CPU."

ALL FANCY LANGUAGE FOR, WHEN WE ASKED DR. O, WE SAID, SO WHAT DOES THIS REALLY MEAN? THIS MEANS THAT IF ANYTHING IS USED TO GENERATE THE CLOCKING SIGNAL THAT COMES FROM OFF THE CHIP, WE DON'T INFRINGE.

IF ANYTHING USED TO GENERATE THE SIGNAL USED TO CLOCK THE CPU COMES FROM OFF THE CHIP, WE DON'T INFRINGE.

AND YOUR HONOR'S GOING TO GIVE YOU A JURY INSTRUCTION AND THE JURY INSTRUCTION -- YOU SAW IT UP ON THE ELMO JUST A LITTLE

BIT AGO. HE SAYS, "UNLESS OTHERWISE EXCLUDED BY CONSTRUCTION OF THE COURT," THE CLAIM CAN BE WHAT IT IS AND PEOPLE CAN ADD THINGS TO IT AND STILL INFRINGE.

BUT THE IMPORTANT PART HERE -- CAN WE HAVE THE ELMO, PLEASE -- IS THAT IT ACTUALLY SAYS -- LET'S SEE. IF I WANT TO MAKE IT LITTLER -- THERE WE GO.

SO WHAT THE JUDGE IS -- WHOOPS. WHAT THE JUDGE IS SAYING HERE -- WHAT MR. OTTESON TRIED TO SAY, YOU KNOW, HE TRIED TO SAY THAT HTC IS SAYING, "OH, IT HAS ALL THESE OTHER ELEMENTS. IT HAS A PLL. IT HAS ALL THESE OTHER THINGS. IT HAS REFERENCE TO A CRYSTAL CLOCK."

MR. OTTESON WAS, I THINK, TRYING TO SAY THAT YOU CAN STILL HAVE ALL THOSE INFRINGE, BUT THAT'S NOT WHAT THE JUDGE IS TELLING US. THE JUDGE IS SAYING, "UNLESS OTHERWISE EXCLUDED BY CONSTRUCTION OF THE COURT," YOU CAN HAVE THESE OTHER THINGS.

BUT THE JUDGE'S CONSTRUCTION TELLS US THAT WHAT IS EXCLUDED IS IF THE SIGNAL, IF ANY PART OF THE SIGNAL THAT'S USED TO GENERATE THE CLOCKING SIGNAL COMES FROM OFF OF THE CHIP, THEN YOU DON'T INFRINGE.

CAN WE GO BACK TO THE SLIDES.

AND CLAIM 6 WE ALREADY LOOKED AT, AND THEN THE VARYING LIMITATION, AND WE'LL GET INTO THAT A LITTLE BIT LATER, TOO.

BUT THE CLAIM REQUIRES THAT THE VARYING THE PROCESSING FREQUENCY OF THE DEVICES AS A FUNCTION OF, WE'VE HEARD THIS A LOT, P, V, OR T. SO PROCESS, VOLTAGE, OR TEMPERATURE.

INVENTED.

NEXT.

MR. FISH SAID, "AN ON-CHIP RING OSCILLATOR TIED TO A FIXED-FREQUENCY CRYSTAL, IS THAT NOT THE FISH CLOCK?

"THAT'S CORRECT.

"SO A PLL WOULD NOT BE YOUR INVENTION EITHER?

"NO."

NEXT. MR. FISH GOES ON. WE ASKED HIM, "I BELIEVE YOU TESTIFIED EARLIER THAT IF YOU WOULD TIME A CPU USING A PLL-BASED FREQUENCY SYNTHESIZER AS WE'VE DESCRIBED, THAT WOULD DEFEAT THE PURPOSE OF VARIABLE SPEED TIMING DESCRIBED IN THE '336 PATENT. IS THAT FAIR?

YES."

NEXT.

MR. MOORE SAID, HERE IN COURT, I ASKED HIM, I SAID, "WHAT YOU CLAIM TO HAVE INVENTED IS THE STRUCTURE, THE UNIQUE STRUCTURE OF PUTTING THE RING OSCILLATOR ON THE CHIP TO COMMUNICATE DIRECTLY WITH THE CPU WITH NOTHING IN BETWEEN; RIGHT?"

HE SAID, "YES."

IN OTHER WORDS, DON'T SURROUND IT WITH A PLL. DON'T SURROUND IT WITH OTHER THINGS. LET THE RING TALK DIRECTLY TO THE CPU. LET THEM TALK DIRECTLY TO EACH OTHER.

NEXT.

I EVEN ASKED HIM, THAT INTELLISYS CHIP THAT THEY MAY HAVE

PRODUCED THAT DIDN'T HAVE ANY COMMERCIAL PRODUCTION OF, "THE INTELLISYS CHIP THAT YOU MENTIONED, AGAIN, THAT, IN YOUR MIND, HAD THE PATENTED INVENTION OF A NAKED RING OSCILLATOR, OR A RING OSCILLATOR DIRECTLY CLOCKING THE CPU; CORRECT?

"YES."

NEXT.

AND THAT'S EXACTLY WHAT FIGURE 17 SHOWS, THIS FIGURE THAT WE'VE SEEN ON AND ON THROUGHOUT THE ENTIRE CASE IS WE SEE AN OSCILLATOR, THE RING COUNTER VARIABLE SPEED CLOCK, WE'VE HEARD IT CALLED A RING OSCILLATOR, DIRECTLY CLOCKING THE CPU. IN OTHER WORDS, IT JUST GOES STRAIGHT IN (INDICATING). DON'T GET INTERRUPTED BY SOMETHING ELSE. DON'T GET HAMPERED DOWN. DON'T TALK TO ANYTHING OFF THE CHIP. DON'T LET YOURSELF GET, YOU KNOW, TAMPED DOWN. TALK DIRECTLY TO THE CPU.

AND THAT'S WHAT THE CLAIM CALLS FOR. IT CALLS FOR THAT ENTIRE OSCILLATOR TO NOT TALK TO ANYBODY OFF THE CHIP.

NEXT.

BUT HTC'S PHONES DON'T DO THAT. HTC'S PHONES USE A PLL IN BETWEEN IN ORDER TO CLOCK THE CPU. IN THE HTC PHONES, I THINK EVERYBODY IS AGREED, THERE'S AN EXTERNAL CRYSTAL CLOCK (INDICATING), THIS PARTICULAR ONE HAPPENS TO BE THE QUALCOMM ONE BECAUSE WE HEARD THE MOST ABOUT IT, THAT'S THE TCXO, THE TEMPERATURE CONTROLLED CRYSTAL CLOCK (INDICATING), THAT SIGNAL IS GOING TO COME INTO THE PHASE LOCKED LOOP, AND WE HEARD A LOT ABOUT THE FACT THAT, OH, IT COMES IN AS A SQUARE WAVE, BUT THEN

IT'S NO LONGER A SQUARE WAVE. IT BECOMES SOMETHING ELSE.

DOESN'T MATTER. THE INFORMATION FROM IT IS GOING ALL THE WAY THROUGH THIS PHASE LOCKED LOOP WITH A FORMULA THAT WE KNOW, F IN TIMES SOME MULTIPLIER OR DIVIDED BY, DEPENDING ON WHICH PERSON YOU WANTED TO LISTEN TO, EQUALS F OUT (INDICATING).

THIS IS THE SIGNAL YOU HAVE TO BE LOOKED FOR (INDICATING). THIS IS THE SIGNAL USED TO GENERATE THAT SIGNAL THAT CLOCKS THE CPU (INDICATING). IT'S WHETHER OR NOT THIS SIGNAL HERE (INDICATING) RELIES ON THIS SIGNAL HERE (INDICATING). AND HERE IT DOES. THE PLL IS SITTING IN BETWEEN. THE PLL IS ADDING INFORMATION. IT'S CHANGING THE SIGNAL. IT'S TAKING WHAT'S DONE BY THAT RING OSCILLATOR AND MODIFYING IT USING THE SIGNAL FROM OFF THE CHIP TO GENERATE WHAT EVENTUALLY COMES OUT OF THE CHIP (INDICATING).

NEXT.

ACTUALLY LOOKS A LOT LIKE TALBOT. YOU HEARD MR. GAFFORD SAY IT'S A LOT LIKE TALBOT. YOU'VE GOT THE EXTERNAL CRYSTAL (INDICATING). YOU'VE GOT A PLL USED TO CLOCK THE CPU (INDICATING).

NEXT.

MR. GAFFORD SAID, "ALL OF THE HTC PHONES USE A PLL SIMILAR TO THE ONE IN TALBOT?"

"YES, THEY DO."

NEXT.

SO WHAT DID THE EVIDENCE SHOW? NOT JUST WHAT MR. GAFFORD

THOUGHT, BUT WHAT DID THE ACTUAL EVIDENCE SHOW? WE'RE GOING TO GO THROUGH EACH OF THE WITNESS AND WHAT THEY TOLD YOU HERE IN THE COURTROOM.

NEXT.

JUST TO BRING US BACK TO THE RIGHT QUESTION, I KNOW IT'S A LITTLE REPETITIVE, BUT DR. O, RIGHT THERE, SAYING "IF THERE'S AN OFF-CHIP CLOCK THAT'S USED TO GENERATE THE SIGNAL THAT CLOCKS THE CPU, THERE'S NO INFRINGEMENT; RIGHT?

"WELL, THE ELEMENT A IS NOT SATISFIED AND THAT WILL KNOCK THEM BOTH OUT."

SO IN OTHER WORDS, RIGHT, IF YOU HAVE TO USE A SIGNAL FROM OFF THE CHIP TO CLOCK THE CPU, YOU DON'T INFRINGE.

NEXT.

DR. O SAYS, "OKAY, YEAH, THERE'S DEFINITELY QUALCOMM CHIPS, TI CHIPS, AND SAMSUNG CHIPS, BUT FOR THE PURPOSES OF INFRINGEMENT ANALYSIS FOR THIS CASE, THEY GENERALLY WORK THE SAME."

SO REALLY THEY'RE ALL WORKING ESSENTIALLY THE SAME WAY WITH THAT RING OSCILLATOR INSIDE OF A PLL TALKING TO THE EXTERNAL CRYSTAL BEFORE GENERATING THE SIGNAL THAT GOES OUT TO THE CPU.

NEXT.

NOW, WE BROUGHT THE QUALCOMM ENGINEER, MR. SINA DENA, THE MAN WHO HELPED DESIGN MANY OF THE CHIPS THAT ARE IN THE PHONES THAT ARE ACCUSED IN THIS CASE, THE MAN WHO WORKS WITH THEM DAY

THE SAME THING.

NEXT.

YOU ALSO HEARD FROM MR. LIANG. MR. LIANG IS AN HTC EMPLOYEE WHO SAYS, YEAH, WHEN I PUT THE PHONES TOGETHER, I USE THESE CHIPS AND THESE CHIPS HAVE OFF-CHIP REFERENCE SIGNALS AND THE OFF-CHIP REFERENCE SIGNAL, THE TCXO, IS USED FOR THE PLL. AND HE SENDS THE INPUT SIGNAL -- OR RATHER, THE INPUT SIGNAL SENDS ITS STUFF THROUGH THE PLL BEFORE A SIGNAL CAN BE GENERATED TO CLOCK THE CPU.

NEXT.

AND MR. GAFFORD CONFIRMED IT. "ALL THE HTC PHONES USE AN EXTERNAL CLOCK TO GENERATE THE CPU?

"YES.

"HOW DO THEY USE THAT?

"THEY USE IT AS A REFERENCE SIGNAL FOR THE PLL."

NEXT.

MR. GAFFORD GOES ON TO SAY THAT HE ACTUALLY TESTED THESE THINGS TO SEE HOW THEY WORKED. HE ACTUALLY TESTED IT. AT -- AS THE FIRST STEP OF REMOVING THE CLOCK, THEY ASKED HIM, WHAT WOULD HAPPEN? HE SAID, OKAY, I TOOK THE CRYSTAL OUT AND I WANTED TO SEE WHAT HAPPENED.

HE SAID HE TRIED POWERING THE PHONE BACK UP AND IT DIDN'T WORK.

"WAS THAT TRUE EVEN IF YOU PLUGGED IT INTO SOMETHING ELSE?" SO MAYBE THE PHONE LOST BATTERY, LET'S SEE IF SOMETHING

ELSE HAPPENED.

AND HE SAID, "YEAH, IT WAS ALL SET TO WORK. IT HAD EVERYTHING IT NEEDED. BUT WITH THE CRYSTAL GONE IT WOULDN'T WORK." SO HE TESTED IT.

DR. O DIDN'T TEST THAT. HE DIDN'T TAKE THE CRYSTAL OUT TO SEE WHAT WOULD HAPPEN.

MR. GAFFORD DID, AND MR. DENA AND MR. HAROUN TOLD YOU WHAT WOULD HAPPEN IF THE CRYSTALS WERE TAKEN OUT OF THEIR CHIPS.

NEXT.

DR. OKLOBDZIJA ACTUALLY DOES AGREE THAT THERE'S A PLL THAT SENDS OUT A CLOCK THAT CLOCKS THE CPU. IT'S THE OUTPUT OF THE PLL THAT IS THE SIGNAL THAT CLOCKS THE CPU.

DR. OKLOBDZIJA ALSO AGREED THAT THE PLL NEEDS AN EXTERNAL REFERENCE. IN OTHER WORDS, IT CAN'T WORK WITHOUT IT.

NEXT.

SO EVERY SINGLE WITNESS FOUND THAT THE EXTERNAL CLOCK WAS USED TO GENERATE THE SIGNAL TO CLOCK THE CPU, EXCEPT DR. OKLOBDZIJA. AND EVEN HE FOUND THAT IT WAS THERE, HE JUST TRIED TO SAY, OH, BUT IT'S NOT GENERATING IT. IT'S USING IT, BUT IT'S NOT GENERATING IT. IT'S JUST THE RING. WE ARE ONLY LOOKING AT THE RING. WE'RE NOT GOING TO LOOK AT ALL THE MATH AROUND IT.

BUT THE EVIDENCE SHOWS THAT, IN FACT, IN THE HTC CHIPS, THE OFF-CHIP CRYSTAL CLOCK IS USED TO GENERATE THE SIGNAL TO CLOCK THE CPU.

NEXT.

HERE WE ACTUALLY CAME UP WITH AN ANIMATION TO KIND OF SHOW WHAT WE'VE BEEN TALKING ABOUT OVER AND OVER AGAIN. WE HAVE THE EXTERNAL CLOCK ON THE -- OFF THE CHIP IN THE HTC PHONES, WE HAVE A PLL, WITHIN THE PLL THERE'S AN OSCILLATOR, RING OSCILLATOR, AND THEN HERE'S THE CPU THAT NEEDS TO BE CLOCKED (INDICATING).

GO AHEAD AND RUN IT.

SO A SIGNAL COMES IN, IT COMES IN IN WAVE FORM (INDICATING); THE INFORMATION FROM THE SIGNAL IS USED, IT'S FED UNTIL THE OSCILLATOR CHANGES (INDICATING); AND ONLY WHEN IT CHANGES BASED ON WHAT'S HAPPENING WITH THE EXTERNAL CLOCK DOES THE CLOCK SIGNAL COME OUT (INDICATING).

SO YOU HAVE TO USE THE INFORMATION FROM THE EXTERNAL CLOCK BEFORE ANY CLOCK SIGNAL IS GENERATED (INDICATING).

NEXT.

SO THAT DEALS WITH THAT LIMITATION AND SHOWS WHY HTC DOESN'T INFRINGE.

IF YOU ONLY FIND THAT LIMITATION MISSING, HTC DOESN'T INFRINGE. IT'S KIND OF LIKE BOWLING. THEY HAVE TO ROLL A STRIKE. THEY HAVE TO KNOCK DOWN EVERY SINGLE PIN. IF EVEN ONE IS LEFT STANDING, WE DON'T INFRINGE.

AND SINCE WE DON'T HAVE ENTIRE OSCILLATORS IN OUR CHIPS, THAT PIN IS LEFT STANDING, SO WE DON'T INFRINGE.

BUT WE ALSO DON'T INFRINGE THE VARYING LIMITATION.

THE VARYING LIMITATION IN THE CLAIM SAYS THAT THE DEVICES HAVE TO -- "VARYING THE PROCESS FREQUENCY OF THE FIRST PLURALITY OF ELECTRONIC DEVICES AND THE CLOCK RATE OF SAID PLURALITY OF ELECTRONIC DEVICES IN THE SAME WAY," SO YOU'RE GOING TO VARY PROCESSING FREQUENCY, IN OTHER WORDS, CLOCK RATE, TOGETHER. SO IF IT GETS FASTER -- IF IT GETS HOTTER, IT'S GOING TO GET SLOWER. IF IT GETS COLDER, IT'S GOING TO GET FASTER.

SAME THING WITH VOLTAGE. SAME THING WITH PROCESSING PARAMETERS AS A FUNCTION OF THAT.

AND ANY ONE OF THEM -- I AGREE WITH MR. OTTESON, IT CAN BE ANY ONE. IF THE CHIP IS MADE SO THAT IT'S ALLOWED TO VARY BY ANY ONE OF THOSE, THEN IT WOULD MEET THAT LIMITATION.

BUT WE DON'T. WE DON'T. OUR CHIPS ARE MADE TO BE LOCKED DOWN BY THAT PLL, SO THEY DON'T VARY WITH TEMPERATURE. YOU HEARD THAT FROM ALMOST EVERYBODY.

THEY DON'T VARY WITH VOLTAGE. YOU HEARD THAT AS WELL.

WHAT YOU HEARD INSTEAD IS THAT THIS BINNING IDEA IS WHERE THE CHANGE HAPPENS.

BUT BINNING JUST SAYS, I'VE GOT SLOW CHIPS, MEDIUM CHIPS, AND FAST CHIPS, AND THEN THEY CAN ALL GO AS FAST AS ALL THE FAST CHIPS IN THE BIN.

WE AGREE THAT OUR CHIPS WERE AT SOME POINT POTENTIALLY BINNED, ALTHOUGH IT'S NOT OURS, IT WAS DONE BY SOMEBODY ELSE.

BUT ONCE THEY'RE PUT IN OUR PHONES, THEY'RE LOCKED BY THE

THE FIRST QUESTION IS, COURT'S DEFINITION OF "GENERATE," PAGE 26, LINES 4 AND 5.

THE SECOND QUESTION IS, CAN YOU DEFINE WHAT IS MEANT BY "OTHER PARTS" ON PAGE 29, LINE 14?

I TAKE IT THAT THE PAGE AND LINE REFERENCES IN THE QUESTIONS ARE TAKEN FROM THE WRITTEN VERSION OF THE FINAL JURY INSTRUCTIONS THAT WERE POSTED.

I WILL CONFESS, STARTING WITH THE FIRST QUESTION, THAT I AM A BIT AT A LOSS AS TO HOW MUCH FURTHER CONSTRUCTION OR META CONSTRUCTION I'M AUTHORIZED TO PERFORM TO HELP THE JURY IN THIS SITUATION.

MY UNDERSTANDING, AND I'D LIKE TO HEAR FROM EACH OF YOU, IS THAT HAVING MADE MY CONSTRUCTION IN LIGHT OF THE PROSECUTION HISTORY, THE WRITTEN DESCRIPTION AND ALL OF THAT, THE COURT'S TASK IS AT AN END AND THAT THERE'S NO AUTHORITY FROM THE FEDERAL CIRCUIT, OR ANY OTHER COURT, WHICH WOULD ALLOW THE COURT TO FURTHER DEFINE TERMS BY RE-ENGAGING IN EITHER THE INTRINSIC OR EXTRINSIC EVIDENCE.

IF EITHER OF YOU HAVE A DIFFERENT VIEW, I'M EAGER TO HEAR IT.

MR. OTTESON, I'LL LET YOU GO FIRST.

MR. OTTESON: YOUR HONOR, I THINK YOU'RE CORRECT. I THINK THE ONLY THING YOU CAN TELL THEM IS TO APPLY PLAIN AND ORDINARY MEANING.

THE COURT: OF THOSE TERMS AND CONSTRUCTION?

MR. OTTESON: OF THOSE WORDS, YES.

THE COURT: WHAT DO YOU THINK, MS. KEEFE?

MS. KEEFE: I ALSO AGREE THAT THERE'S NOTHING YOU CAN DO.

I JUST NOTE FOR THE RECORD THAT THIS IS EXACTLY WHAT WE WERE WORRIED ABOUT WHEN WE WERE ASKING FOR CLARIFICATION OF YOUR DEFINITIONS, BECAUSE IT SEEMS LIKE THE JURY IS NOW ENGAGING IN CLAIM CONSTRUCTION INSTEAD OF APPLYING FACTS.

THE COURT: YOUR PREVIOUS OBJECTION IS NOTED.

I'LL JUST MAKE THE OBSERVATION THAT THIS IS A PROBLEM INHERENT IN ANY CLAIM CONSTRUCTION, RIGHT?

MR. OTTESON: THAT'S RIGHT.

MS. KEEFE: IT CAN BE.

I THINK HERE, THOUGH, I'M NOT SURE THAT THERE IS ANYTHING THAT YOU CAN DO. IN FACT, I'M NOT SURE THAT I WOULD EVEN GO SO FAR AS TO SAY THEY HAVE TO APPLY PLAIN AND ORDINARY MEANING. I THINK YOU JUST HAVE TO SAY THAT THAT'S A QUESTION FOR THEM TO ANSWER.

THE COURT: OKAY. ALL RIGHT. WELL -- I THINK WHAT I'LL TELL THEM IS THIS, UNLESS ANYONE HAS ANY BETTER SUGGESTION. I'LL TELL THEM THAT THEY ARE TO APPLY THE DEFINITION OF "GENERATE" THAT IS CONSISTENT WITH THEIR PLAIN AND ORDINARY UNDERSTANDING OF THE TERM.

ANY OBJECTION TO THAT? I'M TRYING TO GIVE THEM SOMETHING.

MR. OTTESON: NO OBJECTION, YOUR HONOR, FROM US.

THE COURT: WHAT DO YOU THINK, MS. KEEFE?

MS. KEEFE: I THINK THE ONLY THING I MIGHT ADD IS "AND IN VIEW OF THE EVIDENCE THAT WAS PRESENTED" OR SOMETHING LIKE THAT.

OH, AND IN THE ENTIRE TERM.

MR. OTTESON: WELL, I DON'T THINK THAT'S PROPER AT ALL. I THINK THAT'S COMPLETELY IMPROPER. I THINK YOU TELL THEM TO APPLY THE PLAIN AND ORDINARY MEANING OF THE TERM IN ENGLISH.

THE COURT: ALL RIGHT. HERE'S WHAT I'LL DO: I'LL TELL THEM THAT THE COURT HAS NO FURTHER DEFINITION OF "GENERATE," PERIOD, END STOP, AND I'LL LEAVE IT AT THAT.

MS. KEEFE: THANK YOU, YOUR HONOR.

THE COURT: OKAY. AS TO THEIR SECOND QUESTION, WHICH IS, WHAT IS MEANT BY "OTHER PARTS," I'M GOING TO LOOK AT PAGE 29, LINE 14. "OTHER PARTS" KIND OF MEANS OTHER PARTS, DOESN'T IT? I'M NOT SURE WHAT ELSE I CAN SAY.

MR. WEINSTEIN: WE HAD A PROPOSAL. I THINK WHAT'S CONFUSING ABOUT -- WHAT THEY MAY BE CONFUSED ABOUT IS THAT THEY MAY NOT UNDERSTAND THAT WHEN YOUR HONOR'S INSTRUCTION IS REFERRING TO OTHER PARTS, YOU'RE REFERRING TO THINGS THAT ARE NOT RECITED IN THE CLAIM. IT'S NOT ABOUT, YOU KNOW, THE PARTS. IT'S ABOUT THINGS THAT ARE OUTSIDE THE SCOPE OF THE CLAIM.

THE PROPOSAL THAT WE HAD WAS SOMETHING ALONG THE LINES OF

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN JOSE DIVISION

PRESIDING: JUDGE PAUL S. GREWAL

CASE NO: CV08-00882 PSG
CASE TITLE: HTC Corporation, et al. v. Technology Properties Limited, et al.

NOTE FROM THE JURY DURING DELIBERATIONS

Date: 10/02/13
Time: 14:45

Note No. 1

1. The Jury has reached a unanimous verdict. [Please mark] (____)

or

2. The Jury has the following question:

COURTS DEFINITION of "GENERATE"
Pg 26 LINES 4+5

The court has no further definition.

Judge Grewal

Signature of Juror

A9041; A9043-A9045; A9050-A9052; A9054; A9056-A9058

REMOVED DUE TO CONFIDENTIAL MATERIAL

SC32442A43

USER'S MANUAL

Revision 1.1

SAMSUNG ELECTRONICS

FUNCTIONAL DESCRIPTION

CLOCK ARCHITECTURE

Figure 7-1 shows a block diagram of the clock architecture. The main clock source comes from an external crystal (XTIpll) or an external clock (EXTCLK). The clock generator includes an oscillator (Oscillation Amplifier), which is connected to an external crystal, and also has two PLLs (Phase-Locked-Loop), which generate the high frequency clock required in the SC32442A.

CLOCK SOURCE SELECTION

Table 7-1 shows the relationship between the combination of mode control pins (OM3 and OM2) and the selection of source clock for the SC32442A. The OM[3:2] status is latched internally by referring the OM3 and OM2 pins at the rising edge of nRESET.

Table 7-1. Clock Source Selection at Boot-Up

Mode OM[3:2]	MPLL State	UPLL State	Main Clock source	USB Clock Source
00	On	On	Crystal	Crystal
01	On	On	Crystal	EXTCLK
10	On	On	EXTCLK	Crystal
11	On	On	EXTCLK	EXTCLK

NOTE

1. Although the MPLL starts just after a reset, the MPLL output (Mpll) is not used as the system clock until the software writes valid settings to the MPLLCON register. Before this valid setting, the clock from external crystal or EXTCLK source will be used as the system clock directly. Even if the user does not want to change the default value of MPLLCON register, the user should write the same value into MPLLCON register.
2. OM[3:2] is used to determine a test mode when OM[1:0] is 11.

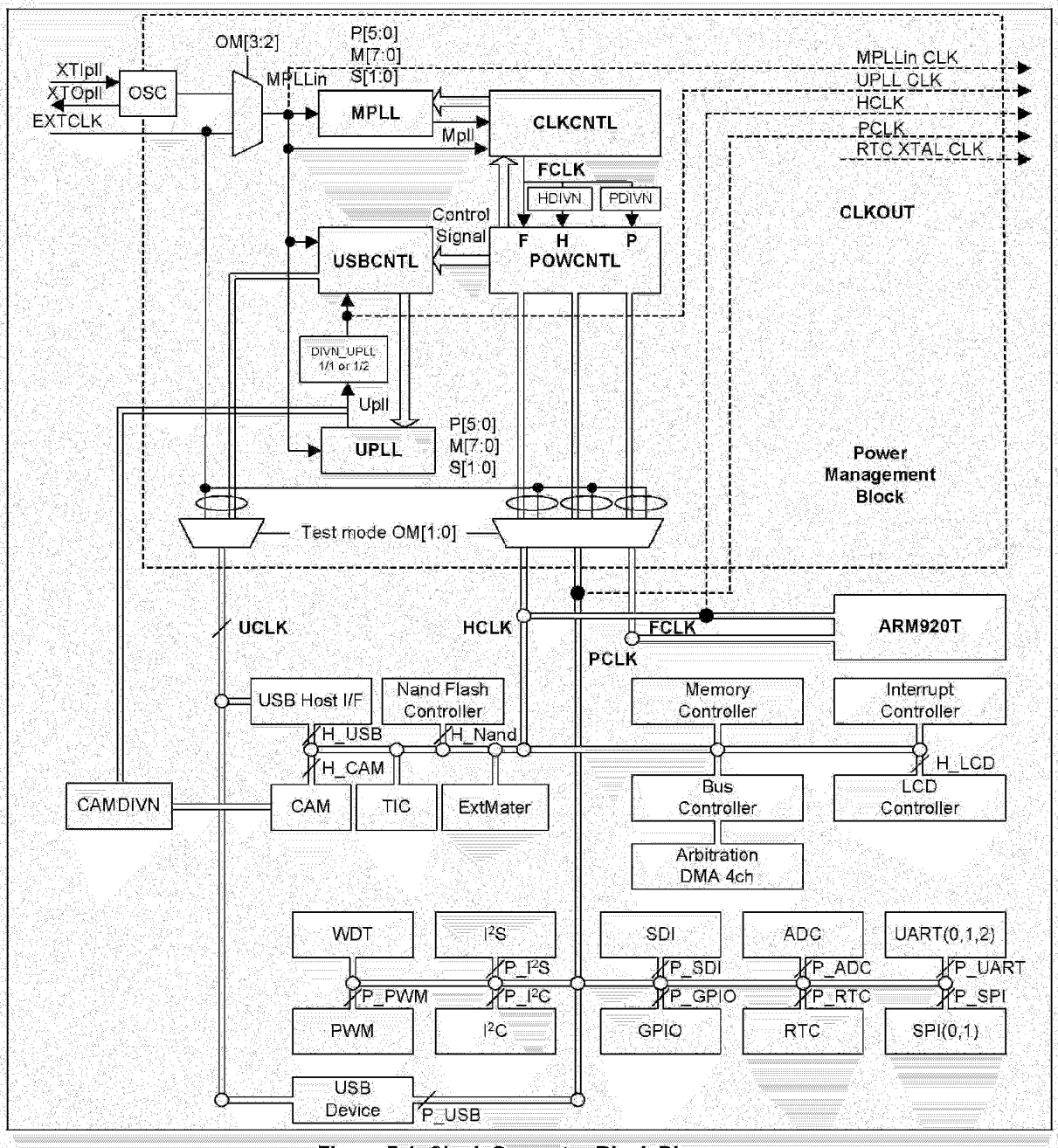


Figure 7-1. Clock Generator Block Diagram

PHASE LOCKED LOOP (PLL)

The MPLL within the clock generator, as a circuit, synchronizes an output signal with a reference input signal in frequency and phase. In this application, it includes the following basic blocks as shown in Figure 7-2: the Voltage Controlled Oscillator (VCO) to generate the output frequency proportional to input DC voltage, the divider P to divide the input frequency (Fin) by p, the divider M to divide the VCO output frequency by m which is input to Phase Frequency Detector (PFD), the divider S to divide the VCO output frequency by "s" which is Mpll (the output frequency from MPLL block), the phase difference detector, the charge pump, and the loop filter. The output clock frequency Mpll is related to the reference input clock frequency Fin by the following equation:

$$Mpll = (2*m * Fin) / (p * 2^{s})$$

m = M (the value for divider M)+ 8, p = P (the value for divider P) + 2

The UPLL within the clock generator is similar to the MPLL in every aspect.

The following sections describes the operation of the PLL, including the phase difference detector, the charge pump, the Voltage controlled oscillator (VCO), and the loop filter.

Phase Frequency Detector (PFD)

The PFD monitors the phase difference between Fref and Fvco, and generates a control signal (tracking signal) when the difference is detected. The Fref means the reference frequency as shown in the Figure 7-2.

Charge Pump (PUMP)

The charge pump converts PFD control signals into a proportional change in voltage across the external filter that drives the VCO.

Loop Filter

The control signal, which the PFD generates for the charge pump, may generate large excursions (ripples) each time the Fvco is compared to the Fref. To avoid overloading the VCO, a low pass filter samples and filters the high-frequency components out of the control signal. The filter is typically a single-pole RC filter with a resistor and a capacitor.

Voltage Controlled Oscillator (VCO)

The output voltage from the loop filter drives the VCO, causing its oscillation frequency to increase or decrease linearly as a function of variations in average voltage. When the Fvco matches Fref in terms of frequency as well as phase, the PFD stops sending control signals to the charge pump, which in turn stabilizes the input voltage to the loop filter. The VCO frequency then remains constant, and the PLL remains fixed onto the system clock.

Usual Conditions for PLL & Clock Generator

PLL & Clock Generator generally uses the following conditions.

Loop filter capacitance	C_{LF}	MPLLCAP: 820 pF ± 5%
		UPLLCAP: 1500 pF ± 5%
External X-tal frequency	-	12 – 20 MHz (note)
External capacitance used for X-tal	C_{EXT}	15 – 22 pF

NOTES:
1. The value could be changed.
2. $FCLK_{OUT}$ must be bigger than 200MHz(It does not mean that the ARM core has to run more than 200Mhz).

A9065-A9066; A9068-A9069; A9072-A9073
REMOVED DUE TO CONFIDENTIAL MATERIAL

ITSELF. BUT WHEN SPECIFICALLY ASKED, DID YOU TEST IT AND DID IT DO IT IN THESE DEVICES, HE ANSWERED NO. INSTEAD HE ANSWERED THAT, IN POINT OF FACT, THE PLL'S IN THESE DEVISES DID RELY ON THOSE VERY FORMULAS THAT WE'VE TALKED ABOUT AND THE EVIDENCE THAT WAS ADDUCED AT TRIAL INDICATING THAT THE OFF-CHIP CRYSTAL WAS ALWAYS USED TO CLOCK THE CPU.

THE COURT: ALL RIGHT. I THINK I UNDERSTAND YOUR POSITION.

MS. KEEFE: THANK YOU, YOUR HONOR.

THE COURT: MR. OTTESON.

MR. OTTESON: THANK YOU, YOUR HONOR. I FEEL KIND OF LIKE *GROUNDHOG DAY*. I FEEL LIKE THIS IS AN ISSUE THAT WE HAVE BEEN OVER REPEATEDLY, AND FROM THE COURT'S QUESTIONS I THINK YOU REALLY UNDERSTAND THEM. THIS IS REALLY A CLAIMS CONSTRUCTION ISSUE. THEY DON'T LIKE THE CLAIM CONSTRUCTION. OBVIOUSLY, WE GOT THE SUMMARY JUDGMENT ORDER FROM YOUR HONOR SHORTLY BEFORE TRIAL, AND THEY MADE AN EMERGENCY MOTION TO MODIFY THE JURY INSTRUCTIONS. AND --

THE COURT: AS I RECALL, MR. OTTESON, I THINK -- I BELIEVE I GAVE THEM PART, BUT NOT ALL OF THE RELIEF THEY SOUGHT, CORRECT?

MR. OTTESON: CORRECT.

THE COURT: I DID MODIFY THE CONSTRUCTION TO SOME DEGREE.

MR. OTTESON: YES.

THE COURT: AT LEAST AS PROVIDED TO THE JURY.

MR. OTTESON: I ACTUALLY DO BELIEVE THAT YOU'RE ALL OVER THIS ISSUE. I MEAN, YOU KNOW EXACTLY WHERE I'M GOING WITH THIS, WHICH IS THEY ASKED FOR TWO MODIFICATIONS TO THE JURY INSTRUCTIONS. YOU LARGELY GAVE THEM ONE OF THOSE, AND IT HAD TO DO WITH -- I'LL GET THE EXACT LANGUAGE HERE THAT YOUR HONOR ADOPTED.

"THE TERM 'ENTIRE OSCILLATOR' IN CLAIMS 6 AND 13 IS PROPERLY UNDERSTOOD TO EXCLUDE ANY EXTERNAL CLOCK USED TO GENERATE THE SIGNAL USED TO CLOCK THE CPU."

SO YOU GAVE THEM THAT. AND WHAT THEY'RE REALLY TRYING TO ARGUE NOW IS THAT THEY WISH THE CONSTRUCTION WOULD HAVE ALSO INCLUDED THIS OTHER THING THEY WERE ASKING FOR, WHICH IS THAT AN ACCUSED PRODUCT CAN INFRINGE ONLY IF IT DOES NOT RELY ON AN INPUT CONTROL TO DETERMINE ITS FREQUENCY.

THE COURT: WHICH WAS MY LANGUAGE FROM THE SUMMARY JUDGMENT ORDER.

MR. OTTESON: RIGHT, RIGHT. AND THAT'S WHY THEY BROUGHT THEIR EMERGENCY MOTION TO MODIFY THE JURY INSTRUCTIONS RIGHT BEFORE TRIAL.

AND IF YOU'LL RECALL, WE STOOD HERE BEFORE TRIAL AND I TOLD YOUR HONOR, HEY, YOU KNOW, THERE'S A BIG DIFFERENCE BETWEEN A GENERATION OF A CLOCK SIGNAL AND SETTING ITS FREQUENCY. AND I SAID, IF WHAT YOUR CONSTRUCTION MEANS IN THE

SUMMARY JUDGMENT ORDER IS THAT AN EXTERNAL CLOCK OR AN EXTERNAL CRYSTAL CAN'T BE USED TO -- FOR FREQUENCY REGULATION, THEN I LOSE AND WE SHOULDN'T GO TO TRIAL.

SO WHAT HAPPENED AS A RESULT OF THAT -- AND THIS IS AN ARGUMENT THAT'S BEEN MADE REPEATEDLY, LIKE I SAID, FOUR OR FIVE TIMES NOW -- IS THAT YOU ADOPTED ONE PART OF WHAT THEY SOUGHT, WHICH HAS TO DO WITH NOT USING AN EXTERNAL CRYSTAL TO GENERATE A CLOCK SIGNAL, BUT REJECTED THEIR REQUEST FOR SOMETHING THAT WOULD PROHIBIT THE USE OF AN EXTERNAL CLOCK OR SIGNAL FOR FREQUENCY REGULATION. THAT WAS REJECTED.

THAT'S A CLAIM CONSTRUCTION ISSUE, AS THE COURT HAS ALREADY RECOGNIZED IN ITS QUESTIONING OF MS. KEEFE. IF THEY DON'T LIKE IT, THEY CAN TAKE IT TO THE FEDERAL CIRCUIT. THAT'S FINE. I'M SURE WE'LL HAVE DISCUSSIONS ABOUT CLAIM CONSTRUCTION AT THE FEDERAL CIRCUIT.

BUT THIS IS A RULE 50(B) MOTION. RIGHT? AND FOR A RULE 50(B) MOTION, THE QUESTION IS WHETHER THERE WAS SUBSTANTIAL EVIDENCE TO SUPPORT THE JURY'S VERDICT, AND I THINK ALSO THE COURT'S ALREADY RECOGNIZED THERE DEFINITELY WAS.

DR. OKLOBDZIJA WHEN HE WAS ASKED POINT BLANK -- AND YOU ALREADY KNOW WHERE IT IS IN THE TRANSCRIPT. I MEAN, I WAS GOING TO POINT YOU TO IT. YOU ALREADY KNEW WHERE IT WAS. HE WAS ASKED IF THE EXTERNAL CRYSTAL WAS USED TO GENERATE THE CLOCK SIGNAL THAT IS USED TO CLOCK THE CPU, AND HE SAID NO, IT'S NOT.

AND, IN FACT, THERE WAS LOTS OF TESTIMONY AT TRIAL -- AND I'M SURE YOU RECALL A LOT OF IT, AND WE'VE CITED IT IN OUR PAPERS, TOO -- THAT THE RING OSCILLATOR THAT IS IN THE PLL IS WHAT GENERATES THE CLOCK SIGNAL THAT CLOCKS THE CPU. ALL THAT OTHER STUFF IN THE PLL IS USED FOR FREQUENCY CONTROL. IT'S USED TO TRY TO KEEP THAT FREQUENCY OF THE CLOCK SIGNAL WITHIN RANGE, BUT FREQUENCY IS A -- IS A CHARACTERISTIC OF A CLOCK SIGNAL. IT'S NOT PART AND PARCEL OF A CLOCK SIGNAL BEING GENERATED.

AND I THINK YOUR HONOR'S RULINGS RECOGNIZE THAT. THEY WANT TO REARGUE CLAIM CONSTRUCTION. I MEAN, I CAN CITE YOU A WHOLE BUNCH OF EVIDENCE, YOU KNOW, FROM THE TRANSCRIPT ABOUT HOW IT'S THE RING OSCILLATOR THAT GENERATES THE CLOCK SIGNAL. AND, IN FACT, WE CITED TESTIMONY FROM MR. GAFFORD IN OUR PAPERS WHERE HE RECOGNIZED THAT, HEY, THIS RING OSCILLATOR HERE IS WHAT'S GOING AT 200 GIGAHERTZ -- TWO GIGAHERTZ, WHICH IS 100 TIMES FASTER THAN THE REFERENCE CLOCK SIGNAL COMING FROM THE EXTERNAL CRYSTAL. SO -- AND WHAT'S CLOCKING THE CPU IS THAT TWO GIGAHERTZ SIGNAL THAT'S COMING OUT OF THE RING OSCILLATOR.

SO THERE'S LOTS OF EVIDENCE ON THAT, I THINK YOUR HONOR WELL UNDERSTANDS THAT. SO I DON'T THINK I REALLY NEED TO BELABOR THE POINT. IF YOU HAVE ANY SPECIFIC QUESTIONS, I'M HAPPY TO ANSWER THOSE. BUT I THINK YOUR QUESTIONS TO COUNSEL HAVE ALREADY INDICATED YOU UNDERSTAND WHAT THE ISSUES ARE.

A9316-A9317

REMOVED DUE TO CONFIDENTIAL MATERIAL

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT
HTC Corporation v. Technology Properties Limited, 2014-1076, -1317

CERTIFICATE OF SERVICE

I, Elissa Matias, being duly sworn according to law and being over the age of 18, upon my oath depose and say that:

Counsel Press was retained by Cooley LLP, Attorneys for Cross-Appellants to print this document. I am an employee of Counsel Press.

On **October 8, 2014**, counsel has authorized me to electronically file the foregoing **Corrected JOINT APPENDIX (CONFIDENTIAL AND NON-CONFIDENTIAL VERSIONS)** with the Clerk of Court using the CM/ECF System, which will serve via e-mail notice of such filing to any of the following counsel registered as CM/ECF users:

James C. Otteson
Thomas T. Carmack
Philip W. Marsh
AGILITY IP LAW, LLP
149 Commonwealth Dr.
Menlo Park, CA 94025
(650) 227-4800
Attorneys for Defendants-Appellants Technology Properties Limited, Patriot Scientific Corporation and Alliacense Limited

Additionally on this date, the corrected Confidential Joint Appendix will be emailed to the above counsel and paper copies will be mailed to the above principal counsel.

Upon acceptance by the Court of the e-filed document, six paper confidential copies will be filed with the Court within the time provided in the Court's rules.

The Joint Appendix was originally filed and served by Appellant's Counsel on October 6, 2014.

October 8, 2014

/s/ Elissa Matias.
Elissa Matias
Counsel Press