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By: /Larry E. Henneman, Jr./

Attorney Docket No.: 0081-011D3C1X1
Merged with: 0081-011D3C1X2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Ex Parte Reexamination:

Control No.: 90/008,227
Filed: September 21, 2006

merged with

Control No.: 90/010,596
Filed: May 29, 2009

U.S. Patent No. 6,598,148

Examiner: POKRZYWA, Joseph R.

Technology Center/Art Unit: 3992

Customer No. 40972

For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLAOCK

AMENDMENT IN RESPONSE TO NON FINAL OFFICE ACTION IN EX PARTE REEXAMINATION PROCEEDINGS

Mail Stop ***Ex Parte Reexamination***
Central Reexamination Unit
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Sir:

In response to the non final office action mailed December 11, 2009, in the merged reexamination proceedings, please enter the following amendments.

A listing of the claims begins on page 2.

Remarks begin on page 5.

1. (Original) A microprocessor integrated circuit comprising:

a program-controlled processing unit operative in accordance with a sequence of program instructions;

a memory coupled to said processing unit and capable of storing information provided by said processing unit;

a plurality of column latches coupled to the processing unit and the memory, wherein, during a read operation, a row of bits are read from the memory and stored in the column latch; and

a variable speed system clock having an output coupled to said processing unit;

said processing unit, said variable speed system clock, said plurality of column latches, and said memory fabricated on a single substrate, said memory using a greater area of said single substrate than said processing unit, said memory further using a majority of a total area of said single substrate.

2. (Original) The microprocessor integrated circuit of claim 1 wherein said memory is dynamic random-access memory.

3. (Original) The microprocessor integrated circuit of claim 1 wherein said memory is static random-access memory.

4. (Original) A microprocessor integrated circuit comprising:

a processing unit disposed upon an integrated circuit substrate, said processing unit operating in accordance with a predefined sequence of program instructions;

a memory coupled to said processing unit and capable of storing information provided by said processing unit, said memory occupying a larger area

of said integrated circuit substrate than said processing unit said memory further occupying a majority of a total area of said single substrate; and

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said integrated circuit substrate.

5. (Original) The microprocessor integrated circuit of claim 4 wherein said memory is dynamic random-access memory.

6. (Original) The microprocessor integrated circuit of claim 4 wherein said memory is static random-access memory.

7. (Original) The microprocessor integrated circuit of claim 4 wherein said memory is capable of supporting read and write operations.

8. (Cancelled).

9. (Original) The microprocessor integrated circuit of claim 8 wherein a first of said interface ports includes a column latch, said column latch facilitating serial communication through said first of said interface ports.

10. (Cancelled).

11. (Original) A microprocessor computational system comprising:

a first processing unit disposed upon a first substrate;

a first memory disposed upon said first substrate and coupled to said first processing unit, said first memory occupying a greater area of said first substrate than said first processing unit, said memory further occupying a majority of a total area of said substrate;

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said first substrate; and

a second processing unit coupled to said first processing unit and configured for interprocessor communication with said first processing unit.

12. (Original) The microprocessor computational system of claim 11 wherein said second processing unit and a second memory are disposed upon a second substrate, said second memory occupying a greater area of said second substrate than said second processing unit said second memory further occupying a majority of a total area of said substrate.

13. (Original) The multiprocessor computational system of claim 11 wherein said first processing unit includes an interface port for establishing said interprocessor communication between an internal register of said first processing unit and second processing unit.

14-15. (Canceled).

REMARKS

This amendment is filed in response to the office action mailed December 11, 2009 in the merged Reexamination Proceedings. Claims 1-15 were previously presented or original. Claims 4, 6, 7, 8 10, 11, and 13-15 are subject to re-examination. Claims 1-3, 5, 9 and 12 are not subject to reexamination. Claims 8 and 10 were previously cancelled. Claims 14 and 15 are cancelled herein. Claims 4, 6, 7, 11 and 13 are rejected.

The rejections

Claims 4, 6, 7, 14 and 15 are rejected under 35 USC 103(a) as being unpatentable over Kajigaya et al. (US patent number 4,956,811, hereafter "Kajigaya") in view of Tanimura et al. (US patent number 4,660,180, hereinafter "Tanimura").

Claims 4, 7, 14, and 15 are rejected under 35 USC 103(a) as being unpatentable over "A 5V Self-Adaptive Microcomputer with 16 KB of E2 Program Storage and Security", written by a Mark Bagula et al., 1983 IEEE International Solid-State Circuits Conference, pages 34-35 (hereinafter "Bagula") in view of Tanimura et al. (US patent number 4,660,180, hereafter "Tanimura").

Claims of 4, 7, 11 and 13-15 are rejected under 35 USC 103(a) as being unpatentable over "A 553K-Transistor LISP Processor Chip", written by Patrick W. Bosshart et al., IEEE Journal Of Solid-State Circuits, Vol. SC-22, No. 5, October 1987 (hereinafter the LISP reference"), further in view of "A 553K-Transistor LISP Processor Chip" also written by Patrick W. Bosshart et al., IEEE International

Solid-State Circuits Conference, February 26, 1987, pages 202, 203 and 402 (hereinafter the "LISP conference reference"), and further in view of US patent number 4,763,297, issued to the Uhlenhoff on Aug. 9, 1988 (hereinafter "Uhlenhoff").

US'148 has expired. "Broadest Reasonable Interpretation" no longer applies.

US'148 expired on Aug. 3, 2009. This affects two aspects of this reexamination. First, claims can no longer be amended or added. For this reason added claims 14 and 15 are cancelled. Second, the claim construction standard, "broadest reasonable constructon consistent with the specification," is replaced by the rule of construction used by the courts. ExParte Papst-Motoren, 1 USPQ 2d 1655 (BPAI 1986).

Controlling authority for the proper interpretation of claims in courts is the en banc Federal Circuit case of Phillips v. AWH Corporation, 415 F.3d 1303 (Fed.Cir.2005) (en banc). Claim terms should be given their ordinary meaning as understood by those skilled in the art at the time of the effective filing date of the patent, consistent with the specification and prosecution history. Id. If there remains an ambiguity, the claims must be construed to preserve their validity. Id., at 1327.

The claims of US '148 have been previously construed by the courts in Technology Properties Ltd. v. Matsushita Electric Industrial Co., 514 F.Supp. 2d 916 (ED Texas 2007); *affirmed in part,* Technology Properties Ltd. v. Arm, Ltd., 276 Fed appendix 1019, May 9, 2008 (not selected for publication in the Federal Register, number 2008-1020), rehearing denied (June 6, 2008). The court construed the following claim terms in section B of the opinion:

1) "microprocessor"

"an electronic circuit that interprets and executes programmed instructions."

2) "processing unit"

"an electronic circuit that controls the interpretation and execution of programmed instructions."

3) "total area of said single substrate"

or

"total area of said substrate"

"the total top surface area of the substrate."

4) "area of said single substrate"

or

"area of said substrate"

"the top surface area of the substrate."

5) "system clock"

"a circuit that generates the signal(s) used for timing the operation of the CPU."

CPU was interpreted at B(1)(a) to mean "an electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions." ("Processing unit" and "CPU" have essentially the same meaning.)

6) "ring oscillator"

"an oscillator having a multiple, odd number of inversions arranged in a loop."

Id., at 929-931.

Response to the §103(a) rejections

Kajigaya in view of Tanimura

Claims 4, 6, 7, 14 and 15 are rejected under 35 USC 103(a) as being unpatentable over Kajigaya in view of Tanimura. The office action repeats in substance the same rejection entered in the 90/008,227 proceeding on January 26, 2009. Patent Owners responded with a traverse to that office action on March 27, 2009. Patent owners hereby incorporate that response by reference in its entirety. Neither Kajigaya or Tanimura disclose a microprocessor, nor do they disclose a "processing unit ...operating in accordance with a predefined sequence of program

instructions," nor do they disclose a "ring oscillator" that provides a "system clock" to a processing unit.

Claim 4 is independent. Claims 6 and 7 depend from claim 4. Claims 14 and 15 are canceled.

The Proper Construction of "Processing Unit" is "*an electronic circuit that controls the interpretation and execution of program instructions.*"

In the March 3, 2009 interview, the examiner justified citing DRAM combinational logic circuits such as Kajigaya' RAC (redundant address control circuit) and Tanimura's row and column address decoders, and multiplexors, to show claim 4's "processing unit" limitation because under the "broadest reasonable interpretation" they could not be excluded. Patent owners were invited to show from dictionaries what those of ordinary skill would understand "processing unit" to mean and to show that "processing unit" was consistently used in the specification to describe a device that processed programmed instructions. Patent owners did just that, citing an IEEE dictionary that showed that the processing unit of a microprocessor (the subject matter of claim 4[1]) was known to be the mechanism in a computer that accepts and executes programs; and further listed a dozen cites to the specification where the term "microprocessor" (claim 4 is directed to a microprocessor having as an element, a "processing unit") was consistently defined as having a "central **processing unit**" ("CPU") that executes instructions. Amendment dated March 27, 2009, at 10-11.[2]

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[1] Claim 4 begins, "A microprocessor integrated circuit..."

[2] "A microprocessor, as of the filing of the application that resulted in U.S. 6,598,148, was known by those skilled in the art to mean a "mechanism that accepts a program as input, prepares it for execution, and executes the process so defined with data to produce results." IEEE Standard Dictionary of Electrical and Electronics Terms, Fourth Edition, July 8, 1988 (definition of "processor"). Further, the specification shows that the broadest reasonable interpretation consistent with the specification of the recited processing unit is a device configured to execute the predefined sequence of program instructions. (Col. 4, ll. 1-3 "Microprocessor 50 includes a central processing unit (CPU) 70."; Col. 4, ll. 62-64 "Most instructions execute in 20 nanoseconds in the microprocessor

Patent owner submits that the only "broadest reasonable construction consistent with the specification" of "processing unit" is also its "proper" construction, the construction given it by the district court in TPL v. Matsushita: "*an electronic circuit that controls the interpretation and execution of programmed instructions.*"

But even if the understanding of those skilled in the art of what a processing unit of a microprocessor is and the consistent usage in the specification in the same sense were not enough, claim 4 explicitly requires that the "processing unit" "operat[es] in accordance with a predefined sequence of program instructions." This limits the range of devices that could possibly be mistaken for a "processing unit." The device must operate in accordance with a predefined sequence of programmed instructions. Thus, a device that merely accepts signals to produce a result is not sufficient to be deemed the processing unit of claim 4. It must further operate in accordance with a predefined sequence of program instructions.

Kajigaya Does Not Disclose a Microprocessor

Claim four is directed to "[a] microprocessor integrated circuit." Kajigaya is directed to an improved DRAM. The Kajigaya improvement is directed to allowing the circuit's operation to be changed, not by changing masks, but by blowing fuses and bonding mode setting terminals.

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50. The microprocessor can therefore execute instructions at 50 peak MIPS . . . ."; Col. 5, ll. 41-52; Col. 10, ll. 35-43; Col. 14, ll. 2-4; Col. 14, ll. 6-8; Col. 16, ll. 43-51; Col. 17, ll. 23-24; Col. 18, ll. 13-16; Col. 18, ll. 44-46; Col. 22, l. 40 – Col. 25, l. 50)."

[57] **ABSTRACT**

A semiconductor memory wherein an operating mode is selectively set by effecting bonding with respect to predetermined pads provided on a common semiconductor substrate in a predetermined combination or by cutting off predetermined fuse means provided on the common semiconductor substrate in a predetermined combination and a bit pattern is selectively set by changing a part of a photomask applied to the common semiconductor substrate.

Kajigaya, Abstract

Kajigaya contains conventional DRAM circuitry, such as address decoders and refresh circuits. In particular, Kajigaya's RAC, the circuit called a "processing unit," in the office action, merely comprises circuits and ordinary logic gates that do not operate in accordance with a predefined sequence of programmed instructions. One of ordinary skill in the art at the time of the invention would not have a reason to look to Kajigaya to find a processing unit operating in accordance with a predefined sequence of programmed instructions as claimed in claim 4. DRAM address decoders are not such processors.

The office action states that both Kajigaya and Tanimura are "microprocessor integrated circuit[s]," and that Tanimura may be combined with Kajigaya, because both are directed to "integrated circuit memory devices, which have memory arrays, a processing unit, and clock generators." Action, at 8. However, while both Kajigaya and Tanimura may be directed to "memory devices," they are not directed to "microprocessors," which the district court construed to mean "an electronic circuit that interprets and executes programmed instructions." DRAMs are memories that do not execute program instructions, and no one of ordinary skill in the art at the time of the patent application would confuse a DRAM memory with a microprocessor. *See*, the IEEE definition of "microprocessor;" *supra*, at n. 2.

Kajigaya's RAC is Not a Processing Unit

The office action cited Kajigaya's RAC as a "processing unit," but Kajigaya's RAC is not a "processing unit." According to Kajigaya, this structure merely controls the redundant word and data lines (*see*, e.g., Kajigaya at column 9, lines 49-56), but it is not "an electronic circuit that controls the interpretation and execution of programmed instructions," as required. One of ordinary skill in the art would not confuse a DRAM's address decoder with a microprocessor's "processing unit."

Moreover, Kajigaya's RAC does not operate in accordance with a predefined sequence of program instructions. Kajigaya's RAC has a number of operating modes; such as first page mode, static column mode, nibble mode, mask write mode, and serial mode, but these modes are never invoked by a "predefined sequence of program instructions." Rather a single mode is permanently invoked by bonding external mode setting terminals FP0 and FP1. See figure 1; column 13, lines 27-54; column 15, lines 24-39.

As shown in FIG. 1, the mode control circuit of the common section COM in the timing generating circuit TG is arranged such that the mode setting external terminals FP0 and FP1 are connected to either the circuit ground potential or the power supply voltage Vcc in a predetermined combination, whereby the above-described internal control signals SC, NE, SR and MS are selectively shifted to the high level H or the low level L in the combinations shown in Table 1 below. As described above, the connection between the mode setting external terminals FP0, FP1 on the one hand and the circuit ground potential and the power supply voltage Vcc on the other is made by carrying out bonding between predetermined pads.

TABLE 1

		Bit patterns					
		Pads		Internal control signals			
Operating modes		FP0	FP1	SC	NE	SR	MS
x1, x4	FP	NC	NC	L	L	L	L
x1, x4	SC	Vss	NC	H	L	L	L
x1	N	NC	Vcc	L	H	L	L
x4	MW	SC	Vcc	L	L	L	H
x1, x4	SR	Vss	Vcc	L	H	H	L

FP . . . first page mode
SC . . . static column mode
N . . . nibble mode
MW . . . mask write mode
SR . . . serial mode

Kajigaya, Col. 13, lines 27-54

Tanimura Does Not Disclose a Microprocessor

As discussed above, claim four is directed to "a microprocessor integrated circuit." Tanimura, like Kajigaya, is directed to an improved DRAM. The Tanimura improvement is directed to a two-mode refresh circuit.

[57] **ABSTRACT**

The dynamic RAM has a refresh circuit with two operation modes. In the first operation mode, a variety of signals necessary for the refresh operation are formed in the dynamic RAM. Accordingly, the refresh operation of the dynamic RAM is performed completely automatically. As long as the refresh operation is being carried out, a busy signal is produced from the dynamic RAM to prevent an erroneous writing operation or reading operation. In the second operation mode, the refresh operation of the dynamic RAM is performed in synchronism with a starting signal supplied from an external unit. The busy signal produced by the dynamic RAM that is working under the first operation mode can be used as a starting signal for the dynamic RAM that is working under the second operation mode. Therefore, the refresh operation is effected in synchronism for the dynamic RAM's that constitute the memory system, and the through-put of the memory system is enhanced.

Tanimura, Abstract

Other than the two refresh modes, Tanimura appears to be merely comprised of conventional DRAM circuitry: address decoders and refresh circuits. Because Tanimura is not a microprocessor, one of ordinary skill in the art at the time of the invention would not look to Tanimura to find the circuitry claimed in claim four.

Tanimura's Row and Column Address Decoders, and Multiplexer, are not a Processing Unit

The office action cited Tanimura's row (R-DCR) and column (C-DCR) address decoders, and multiplexer (MPX) as a "processing unit." Tanimura's row and column address decoders, and multiplexer cannot be characterized as the claimed "processing unit" because they do not "operat[e] in accordance with a predefined sequence of program instructions." Further, one of ordinary skill in the art would not confuse a DRAM's address decoder with a microprocessor's "processing unit."

Tanimura's Ring Oscillator does not Provide a System Clock to a Processing Unit

The office action concedes that Kajigaya does not clearly disclose that its ring oscillator provides a "system clock" to the recited "processing unit." Tanimura also lacks such a disclosure.

The examiner cited column 15, line 67-column 16, line 22 to suggest that Tanimura's ring oscillator provided a system clock to the "processing unit;" which the examiner states consists of the row and column address decoders, and a multiplexer. However, the cited passage states that the ring oscillator controls a timing circuit, which, as described at column 10, lines 52-56, controls the self-actuated refresh period of the improved DRAM. Such a refresh circuit (REFC) cannot be characterized as the claimed "processing unit," because it does not "operat[e] in accordance with a predefined sequence of program instructions."

Not only do Kajigaya and Tanimura not disclose microprocessors, neither has a "processing unit," and both lack a "ring oscillator" that provides a "system clock" to circuitry cited by the office action to be the "processing unit." For all these reasons, the references do not disclose and neither do they suggest the combination of elements claimed in claim four.

Bagula in view of Tanimura

Claims 4, 7, 14, and 15 stand rejected under 35 USC 103(a) as being unpatentable over Bagula view of Tanimura. The office action repeats in substance the same rejection entered in the 90/008,227 proceeding on January 26, 2009. Patent Owners responded to that office action on March 27, 2009. Patent owners hereby incorporate that response by reference in its entirety.

Claim 4 is independent. Claims 6 and 7 depend from claim 4. Claims 14 and 15 are canceled.

Bagula discloses a microprocessor; Tanimura discloses a DRAM; they are not combinable

The office action cites Bagula for showing all the elements of claim four except for its clock generator being a "ring oscillator," which claim four further requires to provide a "system clock" to the "processing unit." The office action cites Tanimura for showing a "ring oscillator" providing a "system clock" to a "processing unit." While the office action states that both Bagula and Tanimura are "microprocessor integrated circuits," it later states that Bagula may be combined with Tanimura since both are directed to "integrated circuit memory devices, which have memory arrays, a processing unit, and clock generators." Action, at 12. However, while Tanimura may be directed to a "memory device," specifically a DRAM, it is not directed to a microprocessor. No one of ordinary skill in the art at the time of the patent application would confuse a DRAM memory with a microprocessor. Further, Bagula is directed to a microprocessor, and is not directed to a "memory device." They are not combinable for at least this reason in that they are directed to widely different devices and further because Tanimura is not a microprocessor as required by the claim. There is simply no teaching that the ring

oscillator disclosed in Tanimura that controls the delay of the start of a memory refresh circuit could successfully clock a microprocessor of the type disclosed by Bagula.

Tanimura does not Disclose a "Processing Unit," nor a "Ring Oscillator" that Provides a "System Clock" to the "Processing Unit"

Tanimura further does not disclose a "processing unit" or a "ring oscillator" that provides a "system clock" to the "processing unit." See, the discussion of Tanimura in this regard, supra.

LISP reference in view of LISP conference reference, further in view of Uhlenhoff

Claims of 4, 7, 11 and 13-15 stand rejected under 35 USC 103(a) as being unpatentable over the LISP reference, in view of the LISP conference reference, and further in view Uhlenhoff. Claims 4 and 11 are independent. Claim 7 depends from claim 4. Claim 13 depends from claim 11. Claims 14 and 15 are cancelled.

The LISP references are cited to show all the elements of both claims 4 and 7 except for a "ring oscillator" that provides a "system clock" to the "processing unit," with "the ring oscillator disposed on the integrated circuit substrate." Uhlenhoff is cited to show a microprocessor having a "processing unit," and a "ring oscillator" that provides a "system clock" to the "processing unit."

Patent owners respectfully traverse. First, the LISP memory does not occupy a majority of the total area of the substrate. Second, there's no expected advantage in modifying the system of the LISP reference to include the ring oscillator of Uhlenhoff.

LISP's Memory Occupies Significantly Less than "a majority of the total area of the substrate."

The office action cites portions of the LISP reference for showing that the on-chip RAM occupies "a large fraction of the chip area...." Action, at 14-15. It cites page 402 of the LISP conference reference for its labeling of memory, which the examiner concludes to show that the memory occupies "a majority of the total area of the substrate." The examiner does not cite any portion of either reference which states that the memory occupies "a majority of the total area of the substrate."

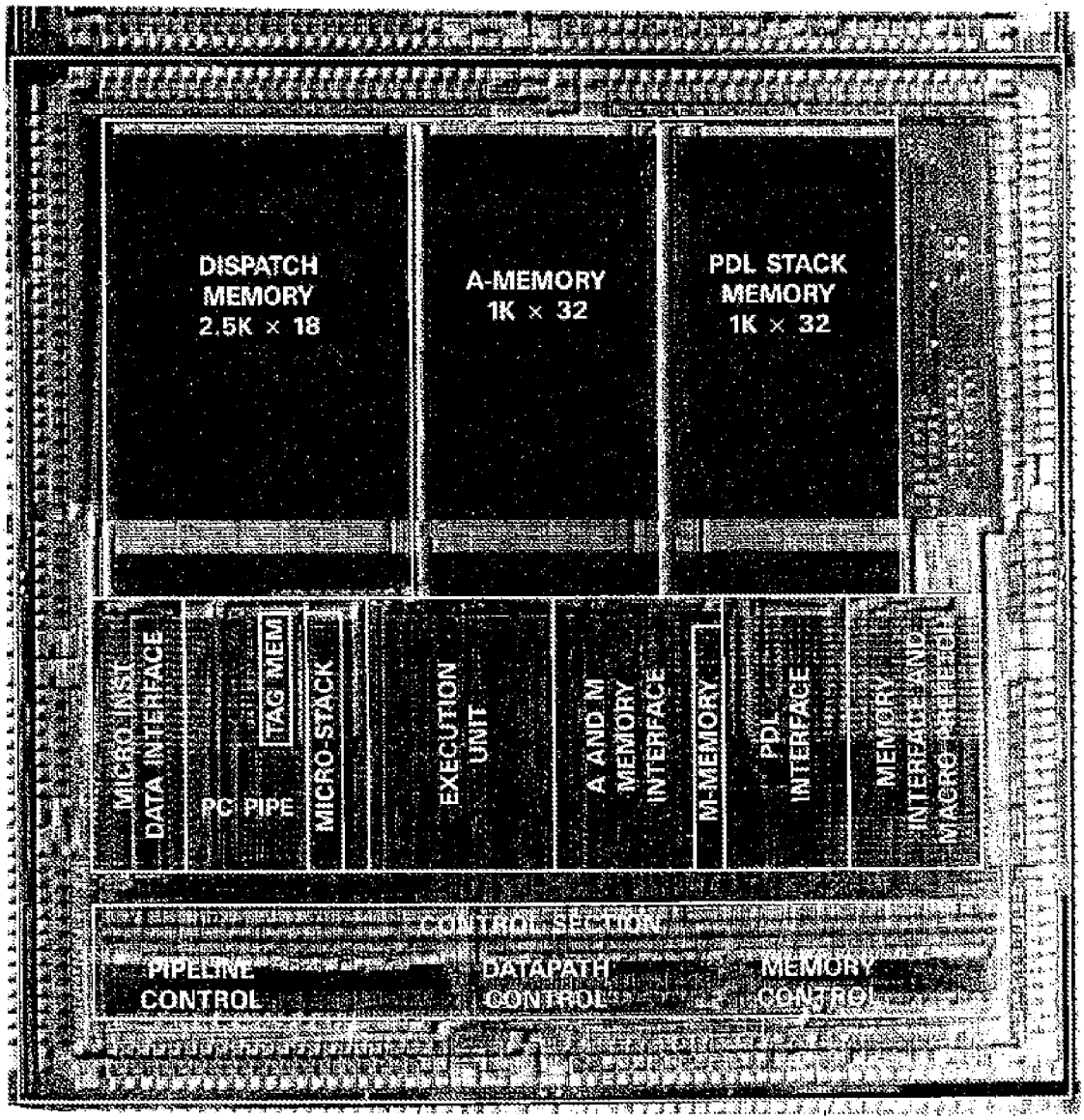


FIGURE 1—Chip photomicrograph.

LISP conference reference, at 402

The references themselves show the integrated circuit and the labeled memory disposed upon it. The description of the LISP integrated circuit describes

seven different memories; six RAMs totaling 114 Kb and one 16K of microcode ROM.

VI. On-Chip Memories

Eighty-eight percent of the transistors on the LISP chip are incorporated into memories. These include six RAM's totaling 114K bits, and 16K of microcode ROM used for self-test and boot load. The implementation of these memories has a large impact on chip area and performance.

LISP Reference, pg. 811

From Fig. 2, three large memory arrays and their associated sizes are disclosed; Dispatch Memory of 45 K (2.5K x 18), A-Memory of 32K and PDL memory of 32K. The reference further describes three remaining RAM memories and their sizes totaling 5Kb: Micro-stack memory of 2K (64 x 32); Tag memory of 1K and M-Memory of 2K.

Three RAMs totaling 5Kb reside in the processor datapath. Their bit lines run parallel to the second level metal global

LISP Conference Reference, pg. 203

each of the four pipeline stages. A 64-word×32-bit microstack memory stores return information for microcode subroutine calls, and the 2.5K-word×18-bit dispatch memory provides for multiway branches. Dispatch mem-

LISP Reference, pg. 810

delayed branch (as does the jump instruction). Not shown in Fig. 2 is the 1K tag memory, which functions similarly to the dispatch memory. It allows simpler tests based on

LISP Reference, pg 810

A 1Kx32b RAM (A-memory) provides one source for the execution unit, while several registers, a 64x32b register file (M-memory), and a 1K word stack (PDL) memory drive the other

LISP Conference Reference, pg. 202

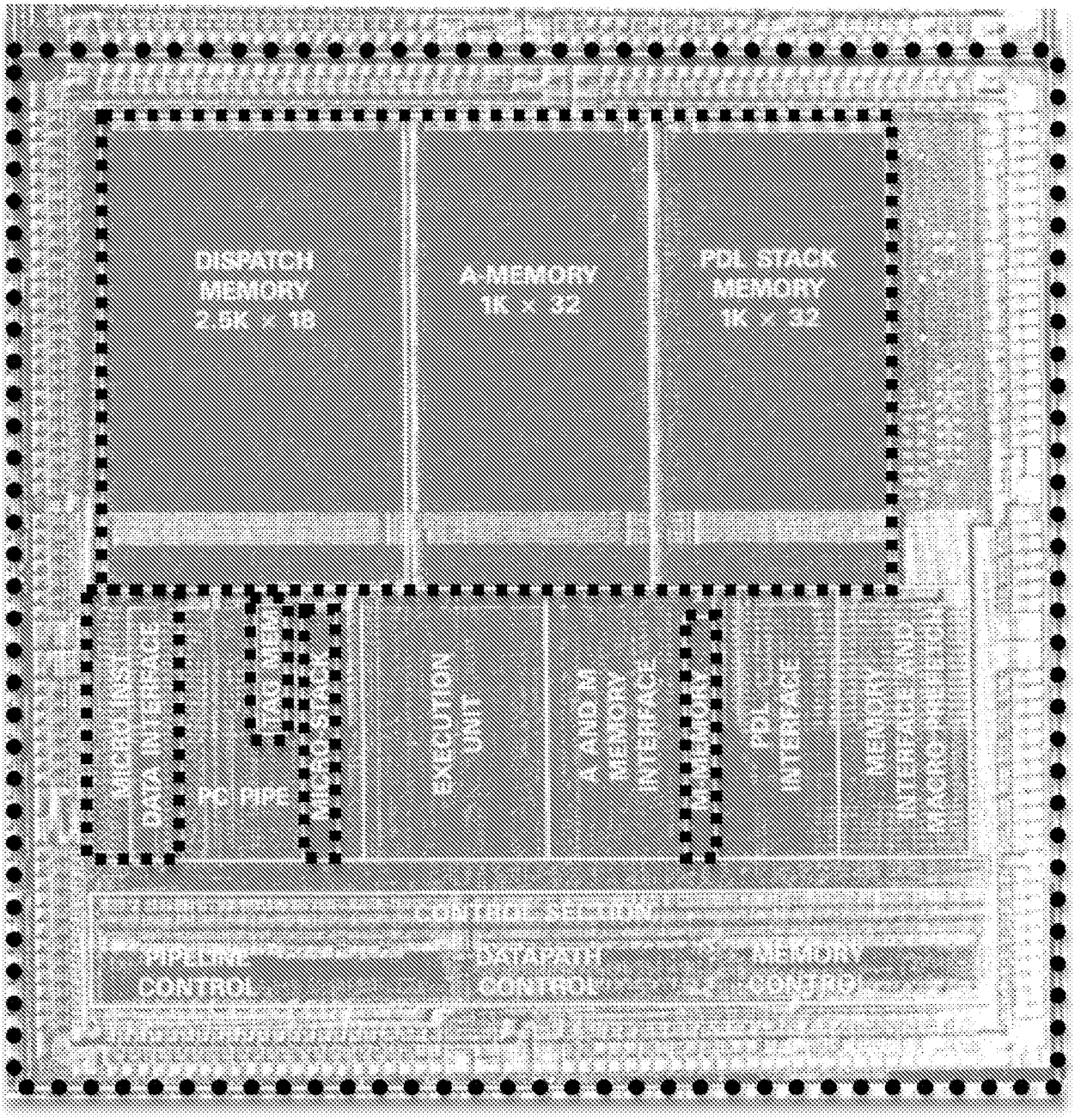
The total capacity of all six RAMs sum to 114Kb thereby matching the LISP description and thus confirms that these memory blocks are the described six RAMs. The 16Kb of on-chip microinstruction ROM is further disclosed in the LISP reference.

C. Self-Test and Memory Test

A 256-word×64-bit microinstruction ROM is included on chip for self-test and boot load. Prior to initializing off-chip microinstruction memory and starting execution

LISP Reference, pg. 816

Patent Owner has highlighted the ROM below as "Micro Inst Data Interface" noting that although it is possible that the "Micro Inst Data Interface" contains additional non-memory circuitry, there is not enough information to determine so and thus and Patent Owner generously includes this circuit area in the memory percentage calculation. Further, Patent Owner has highlighted scribe lines in Fig. 2 delimiting the boundaries of the integrated circuit substrate.



LISP Conference Report, Fig. 2

● ● ● ● ● ● ● indicates boundary of integrated circuit substrate

■ ■ ■ ■ ■ ■ ■ ■ ■ ■
indicates boundary of memory

From a visual measurement of Fig. 2's memory area, the microprocessor of LISP contains on-chip memory which occupies no more than 39% of the integrated circuit substrate even with a generous estimate of ROM area. 39% is significantly less than "a majority of a total area of the single substrate" as required by claims 4 and 11.

No Expected Advantage in Modifying the System of the LISP Reference to Include the Ring Oscillator of Uhlenhoff

The Office Action indicates:

> "However, the LISP reference does not expressly disclose if the "clock", is a ring oscillator...." Action, at 15.

Uhlenhoff is cited to show a ring oscillator that provides a system clock to a processing unit. The Office Action continues,

> The LISP reference & Uhlenhoff are combinable because they are from the same field of endeavor, being CMOS integrated digital circuits. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the internal ring oscillator, as disclosed by Uhlenhoff, within the system described in the LISP reference. The suggestion/motivation for doing so would have been that the integrated circuit in the LISP reference would reduce radio interference, as recognized by Uhlenhoff on col. 3, lines 18-24, and also that the integrated circuit in the LISP reference would additionally benefit from the capability of having increased speed, as recognized by Uhlenhoff on col. 1, lines 62-66. Therefore, it would have been obvious to combine the ring oscillator teachings of Uhlenhoff with the system of the LISP reference to obtain the invention as specified in claim 4.

Action, at 16.

Patent Owners respectfully traverse.

There is no motivation to combine LISP and Uhlenhoff because LISP has none of the problems identified and solved by Uhlenhoff. The purpose of Uhlenhoff's invention is "reducing the crystal surface in digital circuits" (col. 1, lines 50-51). Uhlenhoff accomplishes this purpose by replacing large parallel processing circuits with a relatively small serial data processing circuits. This substitution is made possible by providing the clock signal (f) to serial data processing circuit 120 with a ring oscillator 101 so that serial data processing circuit 120 can operate faster than the rest of the system.

The Office Action states that a suggestion or motivation for including the ring oscillator of Uhlenhoff in the system of the LISP reference would be to reduce radio interference, as recognized by Uhlenhoff. In contrast, the LISP reference has no discussion of any problem associated with a radio interference problem. So even if both LISP and Uhlenhoff are broadly directed to integrated circuits, there would be no motivation to combine LISP and Uhlenhoff. Moreover, merely replacing the system clock of the LISP processor with the ring oscillator of Uhlenhoff would not provide the stated advantage, because the system clock lines of LISP would still be distributed according to its design. There would be no reduction of wiring, which is purported to provide the advantage in the device of Uhlenhoff.

Further the Action states that a suggestion or motivation to combine the two references would be to increase the speed of the system of the LISP reference. However, LISP does not discuss any problem about speed in any way related to its clocking techniques. Further, LISP has no suggestion that it can run faster, let alone multiple times faster. Therefore, there would be no expected advantage in substituting the ring oscillator of Uhlenhoff for the system clock of the LISP reference.

Patent owners respectfully submit that the LISP references do not provide an adequate prima facie basis for rejecting claims 4 and 11. Uhlenhoff does not add

what is missing from the LISP references. Patent owners respectfully submit that claims 4 and 11 are patentable over the LISP references in view of Uhlenhoff.

Dependent claims 6 and 7, and 13 depend from independent claims 4 and 11 respectively, and are patentable for the same reasons that claims 4 and 11 are patentable.

Patent owner respectfully submits that all claims under reexamination are confirmable as patentable.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 269-279-8820.

Respectfully submitted,

Dated: February 11, 2010

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reexamination of: U.S. Patent No.: 6,598,148 Reexamination Control No.:: 90/008,227 Filed: September 21, 2006 merged with: Reexamination Control No.:: 90/010,562 Filed: May 29, 2006 Titled: HIGH PERFORMANCE MICRO-PROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK	Customer No.: 40972 Examiner: Joseph R. Pokrzywa Art Unit: 3992 CERTIFICATION OF SERVICE UNDER 37 C.F.R. §1.510(b)(5) and MPEP §2220

CERTIFICATION OF SERVICE

The undersigned hereby certifies pursuant to 37 C.F.R. §1.550(f) and MPEP §2266.03 that a complete copy of the attached papers (Amendment In Response To Non Final Office Action In Ex Parte Reexamination Proceedings) is being served via first class mail, simultaneously with the filing of this paper, upon the attorneys of record for the third party reexamination requestors in a manner provided by 37 C.F.R. §1.248:

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Date: February 11, 2010

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CERTIFICATE OF MAILING (37 CFR 1.8(A))

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