**PUBLIC VERSION**

**UNITED STATES INTERNATIONAL TRADE COMMISSION**
**Washington, D.C.**

| **In the Matter of** | |
|---|---|
| **CERTAIN WIRELESS CONSUMER ELECTRONICS DEVICES AND COMPONENTS THEREOF** | **Inv. No. 337-TA-853** |

## COMMISSION OPINION

On September 6, 2013, the presiding administrative law judge ("ALJ") issued his final initial determination ("ID"), finding no violation of section 337, and his recommended determination on remedy and bonding.

Having examined the record of this investigation, including the ALJ's final ID, the petitions for review and the responses thereto, and the parties' submissions on review, the Commission has determined to find no violation of section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337 ("section 337") with respect to U.S. Patent No. 5,809,336 ("the '336 patent"). Specifically, the Commission affirms the ID's claim constructions as to claims 6 and 13 of the '336 patent. Regarding infringement, the Commission affirms with modification the ALJ's finding that the accused products do not satisfy the "entire oscillator," "varying," and "external clock" limitations of claims 6 and 13. Moreover, the Commission affirms the ALJ's finding that Complainants failed to prove indirect infringement. With respect to the domestic industry requirement, the Commission finds that Complainants have satisfied the economic prong of the domestic industry requirement based on modified reasoning. The Commission has determined to adopt the ALJ's findings that are consistent with the Commission's opinion as set

forth below.

## I. BACKGROUND

### A. Procedural History

The Commission instituted this investigation on August 24, 2012, based on a complaint filed by Technology Properties Limited LLC ("TPL") and Phoenix Digital Solutions LLC ("PDS"), both of Cupertino, California; and Patriot Scientific Corporation of Carlsbad, California (collectively "Complainants"). 77 *Fed. Reg.* 51572-573 (August 24, 2012). The complaint alleges violations of section 337 in the importation into the United States, the sale for importation, and the sale within the United States after importation of certain wireless consumer electronics devices and components thereof by reason of infringement of claims 1, 6, 7, 9-11, and 13-16 of the '336 patent. The Commission's notice of investigation named the following respondents: Acer, Inc. of Taipei, Taiwan and Acer America Corporation of San Jose, California (collectively "Acer"); Amazon.com, Inc. of Seattle, Washington ("Amazon"); Barnes and Noble, Inc. of New York, New York ("B&N"); Garmin Ltd of Schaffhausen, Switzerland, Garmin International, Inc. of Olathe, Kansas, and Garmin USA, Inc. of Olathe, Kansas (collectively "Garmin"); HTC Corporation of Taoyuan, Taiwan and HTC America of Bellevue, Washington (collectively "HTC"); Huawei Technologies Co, Ltd. of Shenzhen, China ("Huawei Tech."); Huawei North America of Plano, Texas ("Huawei NA"); Kyocera Corporation of Kyoto, Japan and Kyocera Communications, Inc. of San Diego, California (collectively "Kyocera"); LG Electronics, Inc. of Seoul, Republic of Korea and LG Electronics U.S.A., Inc. of Englewood Cliffs, New Jersey (collectively "LG"); Nintendo Co. Ltd. of Kyoto, Japan and Nintendo of America, Inc. of Redmond, Washington (collectively "Nintendo"); Novatel Wireless, Inc. of San

Diego, California ("Novatel"); Samsung Electronics Co., Ltd., of Seoul, Korea and Samsung Electronics America, Inc. of Ridgefield Park, New Jersey (collectively "Samsung"); Sierra Wireless, Inc. of British Columbia, Canada and Sierra Wireless America, Inc. of Carlsbad, California (collectively "Sierra"); and ZTE Corporation of Shenzhen, China and ZTE (USA) Inc. of Richardson, Texas (collectively "ZTE"). The Office of Unfair Import Investigations was named as a participating party. The issue of public interest was delegated to the ALJ. 77 *Fed. Reg.* at 51572.

The Commission later amended the Notice of Investigation to remove Huawei NA as a respondent and to add Huawei Device Co., Ltd. of Shenzhen, China; Huawei Device USA Inc. of Plano, Texas; and Futurewei Technologies, Inc. d/b/a Huawei Technologies (USA) of Plano, Texas ("new Huawei respondents") as respondents. 78 *Fed. Reg.* 12354 (Feb. 22, 2013). The Commission later terminated respondents Sierra, Kyocera, Amazon, and Acer from the investigation. Notice (Feb. 4, 2013); Notice (Sept. 20, 2013); 78 *Fed. Reg.* 71643-45 (Nov. 29, 2013) ("Notice of Review").[1]

On March 5, 2013, the ALJ held a Markman hearing with respect to the disputed claim language in the asserted patent. On April 18, 2013, the ALJ issued Order No. 31 ("the Markman Order") construing the disputed claim terms of the '336 patent.

On September 6, 2013, the ALJ issued his final ID, finding no violation of section 337,

[1] The remaining respondents in this investigation are as follows: B&N, Garmin, HTC, Huawei Tech. and the new Huawei respondents, LG, Novatel, Samsung, and ZTE (hereinafter "Respondents"). Respondent Nintendo was accused of infringing only claims 1 and 11, for which the Commission determined not to review the ALJ's findings of no infringement. 78 *Fed. Reg.* at 3-4.

and his recommended determination on remedy and bonding. In particular, the ALJ found that the importation requirement of section 337 is satisfied. The ALJ also found that none of the accused products directly or indirectly infringe the asserted claims of the '336 patent. In addition, the ALJ found that the asserted claims of the '336 patent have not been proven to be invalid.[2] Further, the ALJ found that respondents have not shown that the accused LG product is covered by a license to the '336 patent. With respect to the issue of domestic industry, the ALJ found that Complainants have satisfied the domestic industry requirement for the '336 patent pursuant to 19 U.S.C. § 1337(a)(3)(C) for the '336 patent. The ALJ also found that no public interest issues are raised by enforcement of a remedy with respect to any of the respondents that would preclude issuance of a remedy if the Commission were to find a violation of section 337.[3]

On September 12, 2013, the ALJ issued a Notice of Clarification supplementing the final ID, explaining that the list of chips referenced on page 119 of the ID is located on page 88 of the ID. Notice of Clarification Regarding Final Initial Determination (Sept. 12, 2013) ("Notice of Clarification").

On September 23, 2013, Complainants filed a petition for review of certain aspects of the final ID, concerning only asserted claims 6 and 13 of the '336 patent. In particular, Complainants requested review of the ID's construction of the "entire oscillator" limitations recited in claims 6 and 13 and the ID's infringement findings based on those limitations.

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[2] Respondents withdrew their invalidity defenses against the '336 patent during the evidentiary hearing on June 10, 2013. Final ID at 288 (citing Tr. at 1523-1525). Pursuant to 35 U.S.C. § 282, the ALJ found that the '336 patent is, therefore, presumed to be valid. *Id.*

[3] As noted above, the Commission ordered the ALJ to take evidence and to render findings of fact concerning the public interest in the Notice of Institution. 77 *Fed. Reg.* 51572 (Aug. 24, 2012).

Complainants also requested review of the ID's infringement findings concerning the limitations "varying," "independent," and "asynchronous" recited in claims 6 and 13. Also on September 23, 2013, Respondents filed a contingent petition requesting review of the ID's finding that Complainants have satisfied the domestic industry requirement based on their licensing activities.

On November 25, 2013, the Commission determined to review the final ID in part with respect to the ID's findings concerning claim construction and infringement of claims 6 and 13 of the '336 patent. 78 *Fed. Reg.* at 71644. The Commission also determined to review the ID's finding of domestic industry to consider the question of whether the alleged industry still exists given TPL's relinquishment of its right to license the '336 patent prior to the complaint being filed and to consider whether Complainants have satisfied the economic prong of the domestic industry requirement. *Id.* at 71644-45. The Commission further determined to review the ID's statement that Complainants need not show that at least one of their licensees practices the patent-in-suit to demonstrate a license-based domestic industry. *Id.* at 71644; *see* ID at 296 (Public Ver.) (Oct. 24, 2013). The Notice of Review included briefing questions regarding the certain issues under review. *Id.* at 71644-45.

The Commission determined not to review the remaining issues decided in the final ID, including the ID's finding of no violation with respect to asserted claims 1, 7, 9, 10, 11, and 16 of the '336 patent. *Id.* at 71644. The Commission also determined not to review the ID's finding that Complainants failed to satisfy their burden of proof with respect to infringement of claims 6 and 13 as to the accused chips listed at page 88 of the ID and the products containing

these chips. *Id.*[4]

On December 23, 2013, Complainants, Respondents, and the Commission investigative attorney ("IA") filed initial submissions responding to the Commission's request for briefing. On January 6, 2014, the parties filed reply submissions.

**B. Patent at Issue**

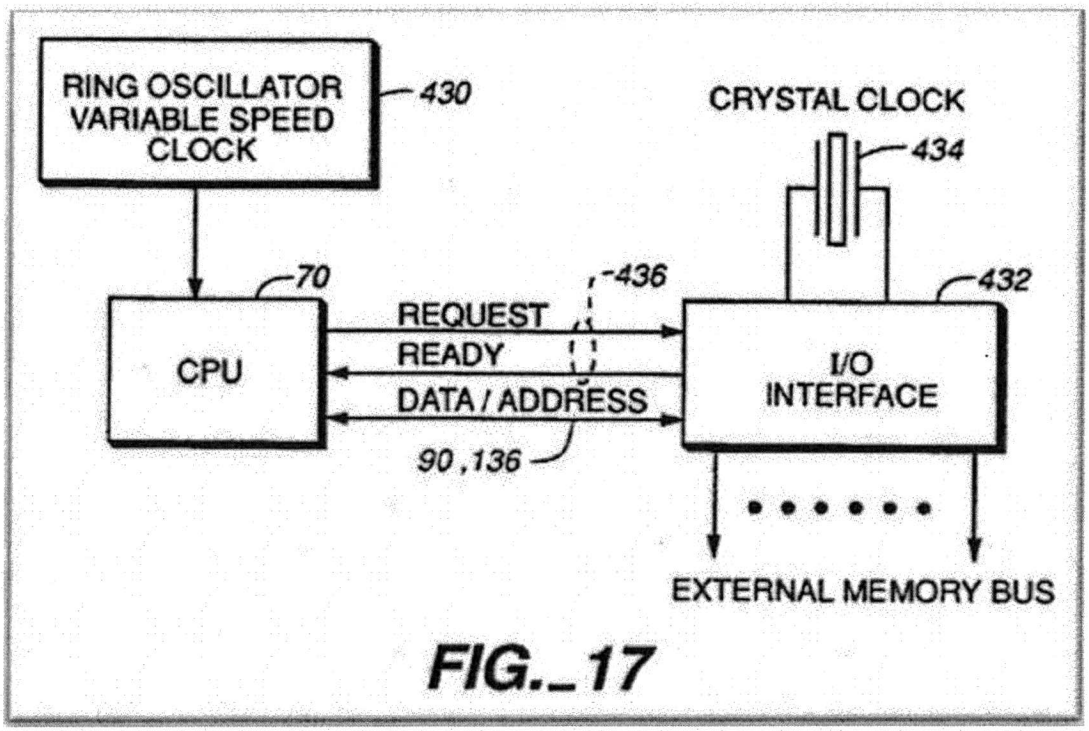
The '336 patent is entitled "High Performance Microprocessor Having Variable Speed System Clock," and is directed to a microprocessor system having a central processing unit ("CPU") and an oscillator, both formed on the same semiconductor die, where the CPU operates at a variable processing frequency dependent upon the clock speed of the oscillator. The patent is further directed to a microprocessor system which includes an input/output ("I/O") interface, which is independently clocked by a second clock. The '336 patent has 16 claims (following reexamination), of which claims 1, 6, 7, 9-11, and 13-16 were asserted against the respondents. Presently only claims 6 and 13 are still asserted against the active respondents.

Microprocessors must operate over: (1) variable temperature ranges, (2) voltage variations, and (3) variations in semiconductor manufacturing processing ("PVT parameters" for "process," "voltage" and "temperature"), each of which affects operating speed and transistor propagation delays. ID at 7 (citing Technology Stipulation at 2.); '336 patent at 16:44-48. Traditionally, CPUs were designed so that the circuit would function at a rated clock speed that would operate properly in the worst case conditions with respect to the PVT parameters. '336

[4] The Commission also extended the target date for completion of the investigation to January 29, 2014. *Id.* at 71645. On December 19, 2013, the Commission further extended the target date for completion of the investigation to February 19, 2014. Notice (Dec. 19, 2013).

patent at 16:48-53. As a result, prior art circuit designs were clocked a factor of two slower than their maximum theoretical performance. *Id.*

The '336 patent discloses a microprocessor system having: (1) an on-chip variable speed clock and (2) a second independent clock connected to an I/O interface. ID at 7 (citing Technology Stipulation at 2.) The '336 patent discloses a microprocessor having a clock circuit and a CPU fabricated on the same substrate. *Id.*; *see* '336 at 16:57-58. The clock circuit, thus, "tracks the parameters which similarly affect all other transistors on the same silicon die" and allows the CPU to "execute[] at the fastest speed possible[.]" '336 at 16:63-17:10, 17:19-22. The '336 patent specification discloses the following embodiment:




*Id.* at Fig. 17. In the illustrated embodiment, CPU **70** operates asynchronously with I/O interface **432**. ID at 7 (citing Technology Stipulation at 2.) I/O interface **432** is controlled independently by crystal clock **434**. *Id.* The on-chip ring oscillator variable speed clock **430** clocks the CPU **70**.

*Id.* Decoupling the variable speed of the CPU **70** from the fixed speed of the I/O interface **432** optimizes the performance of each by allowing the CPU **70** to operate at the maximum frequency dictated by the speed of the on-chip ring oscillator variable speed clock **430**. '336 patent at 17:11-37.

The asserted claims of the '336 patent recite the inventive concept of a CPU and a variable speed clock on the same chip and which vary together due to manufacturing (fabrication) and/or operational (temperature and/or voltage) parameters, where the CPU communicates with an I/O interface, which is clocked using a second clock that is independent of the variable speed clock. The claims variously recite that the first clock comprises a ring oscillator, that the operational parameters include operating temperature or operating voltage of the substrate, and that the second clock is off-chip.

### C. Products at Issue

The accused products are, in general, wireless consumer electronics devices. Complainants accuse products identified in Appendix A to the final ID, including desktop personal computers, notebook personal computers, tablet computers, e-readers, navigation devices, smartphones, mobile phones, portable handheld gaming devices, mobile hotspots, USB modems, and wireless home phones (collectively, "Accused Products").[5] ID at 11. The Accused Products included microprocessor chips that are manufactured by Qualcomm, Texas Instruments

[5] The phrase "Accused Products" as used herein does not include the products listed on page 88 of the final ID. The Commission previously determined not to review the ALJ's finding that Complainants have not met their burden of proof concerning infringement for those products. 78 *Fed. Reg.* at 71644; *see* ID at 118-119;

("TI"), Samsung, and LSI. Comp. Pet. at 6. LSI's products are no longer in the investigation.[6]

The Accused Products generally use phase lock loop ("PLL") technology.[7] A PLL, using a phase checker, generally compares a signal from a reference oscillator and a signal from a second oscillator, *e.g.*, a voltage controlled oscillator ("VCO") or current controlled oscillator ("ICO"), and determines whether the two signals are in phase or out of phase. If the second signal is not in phase with the reference signal, the phase checker, using a charge pump, causes the second oscillator to speed up or slow down until the two signals are in phase. The frequency of the VCO/ICO is, therefore, set by the instruction that comes from the phase match element. The output of the VCO/ICO may be used as a clock. The output of the VCO/ICO is also fed back into the phase checker of the PLL as the second signal, thus allowing the PLL to actively adjust the frequency of the VCO/ICO based on the reference signal. Because the frequency of the VCO/ICO may be an order of magnitude higher than the frequency of the reference oscillator, the signal from the VCO/ICO is typically sent through a frequency divider, which divides the frequency such that it is in the same magnitude as the frequency of the reference signal (*e.g.*, gigahertz divided down to megahertz).

## II. STANDARD ON REVIEW

Once the Commission determines to review an initial determination, its review is conducted *de novo*. *Certain Polyethylene Terephthalate Yarn and Prods. Containing Same*, Inv.

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[6] Only the Accused Products containing chips manufactured by Qualcomm, TI, and Samsung remain in the investigation. *See* Comp. Review Br. at 4 n. 2.

[7] The summary provided here of this technology is drawn from the technical tutorial given by Respondents' expert, Dr. Subramanian. Tr. at 44-53. We have avoided any discussion in his testimony that is argumentative on behalf of Respondents.

No. 337-TA-457, Comm'n Op. at 9 (June 18, 2002). Upon review, the "Commission has 'all the powers which it would have in making the initial determination,' except where the issues are limited on notice or by rule." *Certain Flash Memory Circuits and Prods. Containing Same,* Inv. No. 337-TA-382, USITC Pub. 3046, Comm'n Op. at 9-10 (July 1997) (quoting *Certain Acid-Washed Denim Garments and Accessories,* Inv. No. 337-TA-324, Comm'n Op. at 5 (Nov. 1992)). Commission practice in this regard is consistent with the Administrative Procedure Act. *Certain EPROM, EEPROM, Flash Memory, and Flash Microcontroller Semiconductor Devices and Prods. Containing Same,* Inv. No. 337-TA-395, Comm'n Op. at 6 (Dec. 11, 2000) ("*EPROM*"); *see also* 5 U.S.C. § 557(b).

Upon review, "the Commission may affirm, reverse, modify, set aside or remand for further proceedings, in whole or in part, the initial determination of the administrative law judge. The Commission may also make any findings or conclusions that in its judgment are proper based on the record in the proceeding." 19 C.F.R. § 210.45. This rule reflects the fact that the Commission is not an appellate court, but is the body responsible for making the final agency decision. On appeal, only the Commission's final decision is at issue. *See EPROM*, Comm'n Op. at 6, citing *Fischer & Porter Co. v. Int'l Trade Comm'n*, 831 F.2d 1574, 1576-77 (Fed. Cir. 1987).

## III. ANALYSIS CONCERNING ISSUES THE COMMISSION HAS DETERMINED TO REVIEW

### A. Claim Construction

Claim construction "begin[s] with and remain[s] centered on the language of the claims themselves." *Storage Tech. Corp. v. Cisco Sys., Inc.*, 329 F.3d 823, 830 (Fed. Cir. 2003);

*Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*). The language used in a claim bears a "heavy presumption" that it has the ordinary and customary meaning that would be attributed to the words used by persons skilled in the relevant art. *Phillips*, 415 F.3d at 1312-13. To help inform the court of the ordinary meaning of the words, a court may consult the intrinsic evidence, including the claims themselves, the specification, and the prosecution history, as well as extrinsic evidence, such as dictionaries and treatises and inventor and expert testimony. *Id.* at 1314. In particular "the specification 'is always highly relevant to the claims construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'" *Id.* at 1315 (citations omitted).

A court must "take care not to import limitations into the claims from the specification." *Abbott Labs. v. Sandoz, Inc.*, 566 F.3d 1282, 1288 (Fed. Cir. 2009). "When the specification describes a single embodiment to enable the invention, this court will not limit broader claim language to that single application 'unless the patentee has demonstrated a clear intention to limit the claim scope using "words or expressions of manifest exclusion or restriction."'" *Id.* (citations omitted). "By the same token, the claims cannot enlarge what is patented beyond what the inventor has described as the invention. Thus this court may reach a narrower construction, limited to the embodiment(s) disclosed in the specification, when the claims themselves, the specification, or the prosecution history clearly indicate that the invention encompasses no more than that confined structure or method." *Id.* (citations omitted).

"[T]he distinction between using the specification to interpret the meaning of a claim and importing limitations from the specification into the claim can be a difficult one to apply in practice … [h]owever, the line between construing terms and importing limitations can be

discerned with reasonable certainty and predictability if the court's focus remains on understanding how a person of ordinary skill in the art would understand the claim terms." *Phillips*, 415 F.3d at 1323 (citations omitted). In attempting to discern whether a "patentee is setting out specific examples of the invention . . . or whether the patentee instead intends for the claims and the embodiments in the specification to be strictly coextensive . . . [t]he manner in which the patentee uses a term within the specification and claims usually will make the distinction apparent." *Id.*

"[W]here the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender." *Omega Eng'g., Inc. v. Raytek Corp.*, 334 F.3d 1314, 1324 (Fed.Cir.2003). "Such a use of the prosecution history ensures that claims are not construed one way in order to obtain their allowance and in a different way against accused infringers." *Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005). Disavowal of claim scope made "in the course of prosecuting [a] patent, through arguments made [by the applicant] to distinguish prior art references . . . [must] constitute clear and unmistakable surrenders of subject matter." *Cordis Corp. v. Medtronic Ave,, Inc.*, 511 F.3d 1157, 1177 (Fed. Cir. 2008).

**a. Proceedings Before the ALJ**

The ALJ construed the disputed claim limitation "an entire oscillator disposed upon said integrated circuit substrate" recited in claims 6 and 13 of the '336 patent to mean "an oscillator that is located entirely on the same substrate as the central processing unit and does not rely on a control signal or an external crystal/clock generator to generate a clock signal." Markman Order

at 40-41; ID at 15.[8] Asserted claims 6 and 13 recite the following, with the disputed limitation highlighted:

Claim 6 of the '336 patent provides:

> 6. A microprocessor system comprising:
> a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;
> **an entire oscillator disposed upon said integrated circuit substrate** and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and
> an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.

Claim 13 of the '336 patent provides:

> 13. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central

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[8] The ALJ based his construction of the limitation "an entire oscillator disposed upon said integrated circuit substrate" of claims 6 and 13 on his reasoning concerning the construction of the similar limitation "an entire ring oscillator variable speed system clock in said single integrated circuit" of claims 1 and 11. *See* Markman Order at 41. Our analysis of the ID's claim construction will, therefore, also reference his findings for the limitation in claims 1 and 11. *See id.* at 20-40.

processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

**an entire oscillator disposed upon said integrated circuit substrate** and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;

an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and further wherein said central processing unit operates asynchronously to said input/output interface.

'336 patent C1 at 2:13-41, 3:29-4:9.

The parties' proposed constructions of the disputed limitation in claims 6 and 13 were as follows:

| Claim Term | Respondents | Complainants | IA |
|---|---|---|---|
| "an entire oscillator disposed upon said integrated circuit substrate" | An oscillator that is located entirely on the same semiconductor substrate as the central processing unit and does not rely on a control signal or an external crystal/clock generator to generate a clock signal | An oscillator that is located entirely on the same semiconductor substrate as the central processing unit | An oscillator that includes all components that determine oscillator frequency located on the same semiconductor substrate as the CPU |

Markman Order at 40.

Complainants argued during the Markman proceedings that the "entire oscillator" limitation merely requires "a[n] . . . oscillator with circuitry that is entirely integrated in the same semiconductor as the . . . CPU." *Id.* at 20. Complainants asserted that the claim language does not suggest that the claimed "oscillator cannot use a 'control signal' or reference an 'external crystal.'" *Id.* Respondents argued that the patent applicants clearly disavowed reliance on "any off-chip crystals, off-chip clock generators, or control signals" during the initial prosecution of the '336 patent. *Id.* at 21-22. The IA argued that, during prosecution, the patent applicants explicitly amended the claims and presented arguments distinguishing the claims from prior art systems that relied on off-chip components, *e.g.*, an external crystal, or control signals to determine clock frequency. *Id.* at 29-30.

The ALJ rejected Complainants' proposed construction because it did not account for the prosecution history. *Id.* at 38. The ALJ noted that, in distinguishing over U.S. Patent No. 4,503,500 to Magar ("Magar"), the patent applicant specifically argued that "Magar's clock generator 'is not an entire oscillator in itself' because it 'relies on an external crystal connected to terminals X1 and X2 to oscillate.'" *Id.* (citing JXM-16 at TPL853_02954559).[9] The ALJ further noted the patent applicants' assertion that the clock of Magar "is specifically distinguished from the instant case in that it is *both* fixed-frequency (being crystal based) and requires an external crystal or external frequency generator.'" *Id.* (emphasis in original) (citing JXM-16 at TPL853_02954561). The ALJ found that Respondents' proposed construction properly

[9] The citations to the prosecution history in this Opinion refer to the final admitted exhibits, updating the preliminary exhibits citations in the Markman Order.

"expresses the fact that the [oscillator] is a self-contained oscillator and clock which does not utilize external components (as is disclosed in Fig. 18 of the '336 patent)." *Id.* at 39.

The ALJ further found that Respondents' proposed construction captures the patent applicants' distinction over U.S. Patent No. 4,670,837 to Sheets ("Sheets"), where the applicants argued that "'[t]he present invention does not similarly rely upon provision of frequency control information to an external clock[;] . . . Sheets' system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.'" *Id.* (citing JXM-17 at TPL853_02954574). The ALJ rejected the IA's proposed construction as being overly broad in requiring that "all components that determine clock frequency" be included in the construction of the limitation "entire oscillator" because "[h]ow literally the word 'determine' is to be applied in the context of the claim is a subject that invites further debate." *Id.*

**b. Analysis**

The Commission affirms the ALJ's claim construction of the claim limitation "an entire oscillator disposed upon said integrated circuit substrate," and provides additional reasoning in support of this construction. Specifically, while the ALJ's discussion relies exclusively on the prosecution history (*see* Markman Order at 38-41), both the language of claims 6 and 13, as well as the patent specification, further bolster his construction.

With respect to the claim language, the limitation in question cannot be fully understood by reading it in a vacuum without reference to the claim as a whole. Claims 6 and 13 both recite the following:

> **an entire oscillator disposed upon said integrated circuit substrate** and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, *thus varying the processing frequency* of said first plurality of electronic devices [*i.e.*, the CPU] *and the clock rate* of said second plurality of electronic devices *in the same way* **as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate**, thereby enabling said processing frequency to track said clock rate *in response to said parameter variation*

'336 patent C1, 2:18-30, 3:34-46 (emphasis added). By the plain language of the claims, the "clock rate" of the oscillator and the CPU must "vary in the same way[10] . . . as a function of" the PVT parameters of the chip on which both the oscillator and CPU are situated such that the processing frequency of the CPU tracks the clock rate of the oscillator. Notably, the claim does not recite that the processing frequency and clock rate vary "as a function of . . . *at least* one or more fabrication or operation parameters associated with said integrated circuit substrate[.]" The addition of "at least" in the claim would indicate that the processing frequency and clock rate may vary due to other factors in addition to the fabrication and/or operation parameters. Far from simply requiring that the "entire oscillator" be disposed upon the same chip as the CPU, the plain language of the claim requires that the operating rates of the oscillator and the CPU be allowed to change in response to the chip's PVT parameters as opposed to as the result of some other influence.

The specification of the '336 patent is consistent with this interpretation. The specification explains in detail that the failure of prior art "[t]raditional CPU designs" is that the

[10] Complainants do not challenge the ALJ's construction of the limitation "varying … in the same way" as having its plain and ordinary meaning. *See* Markman Order No. 31 at 68.

chips were deliberately clocked at the slowest speed necessary to accommodate "the worst case of the [PVT] parameters." '336 patent at 16:44-54. By contrast, the microprocessor of the disclosed invention operates such that "[t]he ring oscillator frequency is determined by the [PVT] parameters[.]" *Id.* at 16:59-60. Similarly, all other components on the chip, including the CPU, are affected by the same PVT factors as the oscillator. *Id.* at 16:65-67. The specification teaches using this fact to solve the problem of prior art microprocessors by fabricating the oscillator clock "on the same silicon chip as the rest of the microprocessor **50**" so that all components, including the oscillator and the CPU, are affected by identical PVT factors. 16:57-58. The specification further explains that

> By deriving system timing from the ring oscillator **430**, *CPU **70** will always execute at the maximum frequency possible*, but never too fast. For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor **50** will operate slower than normal. Since the microprocessor **50** ring oscillator clock **430** is made from the same transistors on the same die as the latches and gates, it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.

*Id.* at 16:67-17:10 (emphasis added). As with the claim language, the teaching of the specification is antithetical to allowing outside influences to affect the clock rate of the on-chip oscillator, which is how prior art microprocessors operated. Rather, the specification explicitly teaches precisely the opposite, that the use of external sources for timing was inefficient and that the solution is to allow the clock rate of the oscillator to vary solely due to the same parameters that are affecting the operational efficiency of the remainder of the on-chip components, *e.g.*, the CPU. As such, the specification of the '336 patent does not allow for the on-chip oscillator to be

influenced by some outside source, *e.g.* an external crystal such as is used in a PLL, which, by definition, isolates the clock rate of the on-chip oscillator from the effects of the chip's PVT parameters.

With respect to the prosecution history, Complainants argue that the prior art references cited by the USPTO examiner—Magar and Sheets—lacked any on-chip oscillator, and that the patent applicants did not disclaim[] any use of a control signal or an external crystal/clock generator to generate a clock signal. A close reading of the prosecution history, however, shows that Complainants are mistaken.

The examiner initially rejected certain claims of the patent application as obvious over Sheets. JXM-17 ('336 prosecution history, Apr. 11, 1996 amendment). Specifically, the examiner noted that "Sheets teaches a microprocessor system having a microprocessor and a variable speed clock generator[,]" contending that, although Sheets does not teach that the "clock is implemented using a ring oscillator . . . 'a counter is a basis component of [a] clock generator.'" *Id.* at TPL853 02954573. In response, the applicants contended that Sheets teaches "the use of discrete, commercially available microprocessor chips . . . driven by a separate clock (VCO **12** of FIG. 1)" and further teaches "a technique for adjusting the frequency of VCO **12** in accordance with a desired operating frequency of the microprocessor **101**." *Id.* at TPL853 02954574. The applicants noted that "[s]pecifically, a digital word indicative of this desired operating frequency is written by microprocessor **101** to VCO **12** by way of data bus **104** as a means of adjusting the clock frequency." *Id.* The applicants contrasted the microprocessor disclosed in Sheets with the microprocessor taught by the patent application, arguing that:

> The present invention does not similarly rely upon provision of frequency control information to an external clock, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, since *the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance.* Sheets' system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.

*Id.* (emphasis added). The applicants further noted the rejected claims were amended to explicitly recite that the "ring oscillator and microprocessor are provided within the same integrated circuit" and that the transistors that comprise the ring oscillator clock "have operating characteristics which *vary similarly* to operating characteristics of transistors included within the microprocessor, *thereby enabling the processing frequency of the microprocessor to track the speed of the ring oscillator clock*[.]" *Id.* (emphasis added). The applicants argued that, in contrast, the "VCO **12** [of Sheets] . . . clearly is not adapted to mimic variation in the speed of transistors within the microprocessor **101**." *Id.* at TPL853 029545745.

Although Sheets does teach "provid[ing] 'control information' – in the form of a 'digital word' – to an external clock," in traversing the rejection over Sheets, the applicants clearly argued that, unlike the invention claimed in the patent application, Sheets not only fails to disclose an on-chip clock, but also fails to disclose a clock that "is [] adapted to mimic variation in the speed of" the CPU "*as a function of various parameters (e.g., temperature) affecting circuit performance.*" Based on this amendment, the patent applicants indicated that the invention recited in the claims of the patent application requires that the CPU "track the speed"

of the on-chip clock due to the operating parameters of the chip, not merely that the clock must be on the same chip as the CPU.

The patent applicants subsequently clarified the novel aspect of the invention in an amendment submitted in response to a telephone interview between the patent examiner and the applicants' counsel, during which counsel further discussed the distinction of the invention over Sheets. JXM-21 ('336 prosecution history, Jan. 13, 1997 amendment). In the amendment, the applicants noted that:

> In the interview, the fact that operating characteristics of electronic devices in an integrated circuit will track one another *depending on variations in the manufacturing process used to make the integrated circuit* was discussed. . . . This fact is utilized in the present invention to provide a variable speed clock for the microprocessor, with the clock speed varying in the same way as variations in the operating characteristics of the electronic devices making up the microprocessor. *This allows the microprocessor to operate at its fastest safe operating speed, given its manufacturing process or changes in its operating temperature or voltage. In contrast, prior art microprocessor systems are given a rated speed based on possible worst case operating conditions and an external clock is used to drive them no faster than the rated speed.* Under other than worst case operating conditions, the prior art microprocessors are actually capable of operating at a faster clock speed than their rated speed.
>
> . . .
>
> Even if the Examiner is correct that the variable clock in Sheets is in the same integrated circuit as the microprocessor of system **100**, that still does not give the claimed subject matter. In Sheets, a command input is required to change the clock speed. *In the present invention, the clock speed varies correspondingly to variations in operating parameters of the electronic devices of the microprocessor because both the variable speed clock and the microprocessor are fabricated together in the same integrated circuit. No command input is necessary to change the clock frequency.*

*Id.* at TPL853_00002448-49 (emphasis added). Based on this later filing, it is clear that the

patent applicants explicitly disclaimed the use of command signals to adjust the clock rate of the on-chip oscillator.

The patent examiner next rejected certain claims of the patent application as obvious over Magar in view of Pelgrom. JXM-19 ('336 prosecution history, Apr. 3, 1997 office action). The examiner relied on Figure 1 of Magar as disclosing "a data processing system having a single chip microcomputer **10** and an I/O interface **12[,]**" and the examiner relied on Figure 2a of Magar to show "that the microprocessor includes [a] clock generator and a CPU[.]" *Id.* at TPL853_00002434. The examiner further relied on Pelgrom's teaching that "electronic components would exhibit [the] same characteristics if they are manufactured by the same process technology" to conclude that "it would have been obvious, from the teaching of Pelgrom, to a person of ordinary skill in the art to have the components of Magar'[s] microprocessor and clock (oscillator) [made] of the same process for ensuring processing frequency of the CPU to track [*sic*] the clock rate in response to the parameter variations." *Id.*

In overcoming the rejection, the patent applicants distinguished between the "conventional crystal clock" disclosed in Magar and the "variable speed clock" of the invention, describing the difference as "a primary point of departure from the prior art[.]" JXM-18 ('336 prosecution history, July 7, 1997 amendment) at TPL853_00002427. The applicants went on to explain that:

> Contrary to the Examiner's assertion in the rejection that "one of ordinary skill in the art should readily recognize that the speed of the CPU and the clock vary together due to manufacturing variation, operating voltage and temperature of the IC", [*sic*] *one of ordinary skill in the art should readily recognize that the speed of the CPU and the clock do not vary together due to manufacturing variation, operating voltage and temperature of the IC in the*

> *Magar microprocessor, as taught in the above quotation from the reference. This is simply because the Magar microprocessor clock is frequency controlled by a crystal which is also external to the microprocessor. Crystals are by design fixed-frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The Magar microprocessor in no way contemplates a variable speed clock as claimed.*
>
> ...
>
> The present invention is unique in that it applies, and can only apply, in the circumstance where the oscillator or variable speed clock is fabricated on the same substrate as the driven device. The example given is a non-crystal controlled circuit, a ring oscillator. *A ring oscillator will oscillate at a frequency determined by its fabrication and design and the operating environment.* Thus in this example, the user designs the ring oscillator (clock) to oscillate at a frequency appropriate for the driven device when both the oscillator and the device are under specified fabrication and environmental parameters. *Crucial to the present invention is that since both the oscillator or variable speed clock and [the] driven device are on the same substrate, when the fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together.* This differs from all cited references in that the oscillator or variable speed clock and the driven device are on the same substrate, and that *the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so.*

*Id.* at TPL853_00002427-28 (emphasis added). The patent applicants specifically distinguished the present invention from Magar and other similar prior art microprocessors which "operate at a frequency determined by [an] external crystal." *Id.* at TPL853_00002428.

Finally, in responding to yet another rejection over Magar and Pelgrom, the patent applicants submitted an additional response, in which the claims were amended to clarify that the claimed oscillator is on-chip. JXM-16 ('336 prosecution history, Feb. 10, 1998 amendment) at TPL853 02954559. In further distinguishing the invention over Magar, the patent applicants

stated that:

> Magar's clock generator relies on an external crystal connected to terminals Xl and X2 to oscillate, as is conventional in microprocessor designs. It is not an entire oscillator in itself. *And with the crystal, the clock rate generated is also conventional in that it is at a fixed, not a variable, frequency. The Magar clock is comparable in operation to the conventional crystal clock* ***434*** *depicted in Fig. 17 of the present application for controlling the I/O interface at a fixed rate frequency, and not at all like the clock on which the claims are based,* as has been previously stated.
>
> ...
>
> The signals PHASE 0, PHASE 1, PHASE 2, and PHASE 3 in Applicant's Fig 18 are synonymous with Ql, Q2, Q3, and Q4 depicted in Magar Fig. 2a. *The essential difference* is that the frequency or rate of the PHASE 0, PHASE 1, PHASE 2, and PHASE 3 signals *is determined by the processing and/or operating parameters of the integrated circuit* containing the Fig. 18 circuit, while the frequency or rate of the Ql, Q2, Q3, and Q4 signals depicted in Magar Fig. 2a are *determined by the fixed frequency of the external crystal connected to the circuit* portion outputting the Ql, Q2, Q3, and Q4 signals shown in Magar Fig. 2a.
>
> The Magar teaching is well known in the art as a conventional crystal controlled oscillator. *It is specifically distinguished from the instant case in that it is* ***both*** *fixed-frequency (being crystal based)* ***and*** *requires an external crystal or external frequency generator.*

*Id.* at TPL853 02954559-61 (emphasis added). The patent applicants' statement in the final sentence quoted above, in particular, shows that the applicants intended to disclaim, not only an external crystal/frequency generator, but ***also*** a fixed-frequency, crystal controlled oscillator. Thus, the "entire oscillator" limitation requires both that the circuitry required to generate and/or determine (or adjust) the frequency of the oscillator's clock rate must be entirely on-chip.

The Commission, therefore, affirms the ALJ's construction of the limitation "entire oscillator" in claims 6 and 13 of the '336 patent to mean: "an oscillator that is located entirely on

the same substrate as the central processing unit and does not rely on a control signal or an external crystal/clock generator to generate a clock signal" with the elaboration discussed above.

**B. Direct Infringement**

The unfair acts covered under section 337 include "all forms of infringement, including direct, contributory, and induced infringement." *Certain Home Vacuum Packaging Machines*, Inv. No. 337-TA-496, Order No. 44, 2004 ITC LEXIS 202 * 2, n.2 (Mar. 3, 2004); *see Spansion, Inc. v. Int'7 Trade Comm'n,* 629 F.3d 1331, 1355 (Fed. Cir. 2010) (affirming Commission's finding of a violation of section 337 based on contributory infringement); *see also Kyocera Wireless Corp. v. Int'l Trade Comm'n,* 545 F.3d 1340 (Fed. Cir. 2008) (ruling on the merits of the Commission's finding that respondent had violated section 337 based on induced infringement).[11] To establish infringement, there must be a preponderance of evidence. *See Kao Corp. v. Unilever United States, Inc.*, 441 F.3d 963 (Fed. Cir. 2006). A determination of patent infringement encompasses a two-step analysis. *Advanced Cardiovascular Sys., Inc. v. Scimed Life Sys., Inc.*, 261 F.3d 1329, 1336 (Fed. Cir. 2001) ("*Scimed*"). First, the court determines the scope and meaning of the patent claims asserted, and then the properly construed claims are compared to the allegedly infringing device. *Id.* "Literal infringement of a claim exists when each of the claim limitations reads on, or in other words is found in, the accused device." *Allen Eng. Corp. v. Bartell Indus.*, 299 F.3d 1336, 1345 (Fed. Cir. 2002). Under the doctrine of equivalents, "a product or process that does not literally infringe upon the express terms of a

[11] The U.S. Court of Appeals for the Federal Circuit recently addressed under what circumstances a section 337 violation may be based on induced infringement. *Suprema v. Int'l Trade Comm'n*, No. 12-1170, 2013 WL 6510929, at *5-12 (Fed. Cir. 2013).

patent claim may nonetheless be found to infringe if there is equivalence between the elements of the accused product or process and the claimed elements of the patented invention." *Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 21 (1997).

Direct infringement includes the making, using, selling, offering for sale and importing into the United States an infringing product, without authority. 35 U.S.C. § 271(a). To prove direct infringement, the plaintiff must establish by a preponderance of the evidence that one or more claims of the patent read on the accused device either literally or under the doctrine of equivalents. *Scimed*, 261 F.3d at 1336.

The ID finds that the Accused Products do not directly infringe the asserted claims of the '336 patent. ID at 17-275. In particular, the ALJ found that Complainants failed to provide any evidence concerning infringement under the doctrine of equivalents. ID at 275. Complainants did not challenge this finding. In addition, the ALJ found that Complainants failed to present sufficient evidence to show that the TI audio codecs found in the accused Nintendo products include a CPU, as required by asserted claims 6 and 13. *Id.* at 270-275. Complainants did not contest this finding.

Furthermore, the ID finds that Complainants failed to present sufficient evidence to show that any of the products listed in Attachments B and C of Respondents' post-hearing brief infringes any asserted claim of the ' 336 patent. *Id.* at 284-287. Specifically, the ALJ found that "[t]o the extent those [listed] products overlap with the Accused Products as defined above, the [ALJ] finds that those products do not infringe the asserted claims of the '336 patent[.]" *Id.* at 287. Complainants did not contest this finding. The ID also finds that that there is insufficient support in the record to determine whether the accused [ ] chips listed at page 88 of the

ID contain an oscillator as required by claims 6 and 13 of the '336 patent. ID at 118-119. The Commission determined not to review this finding. 78 *Fed. Reg.* at 71644.

This Opinion, therefore, address only the following issues regarding direct infringement: (1) the ID's finding that the Accused Products do not satisfy the "entire oscillator" limitation of claims 6 and 13, focusing in particular on the use of "current-starved" technology [ ]; (2) the ID's finding that the Accused Products do not satisfy the "varying" limitations of claims 6 and 13; and (3) the ID's findings concerning the "external clock" limitations.

**1. "Entire Oscillator"**

**a. Proceedings Before the ALJ**

Based on his construction the limitation "an entire oscillator disposed upon said integrated circuit substrate" recited in claims 6 and 13 to mean "an oscillator that is located entirely on the same substrate as the central processing unit and does not rely on a control signal or an external crystal/clock generator to generate a clock signal" (Markman Order at 40-41), the ALJ found that the Accused Products do not satisfy the "entire oscillator" limitations of the asserted claims. ID at 118-132.

Specifically, the ALJ found that Respondents' expert, Dr. Subramanian, and TI's corporate witnesses, Mr. Haroun and Mr. Kekre, "all testified that the PLLs in the Accused Products require, and thus rely on, a control signal to determine the generated clock frequency signal." *Id.* at 119. The ALJ further noted that Complainants' expert, Dr. Oklobdzija, "affirm[ed] that a PLL has circuitry that is used to set the frequency of a VCO to a multiple of another oscillator frequency functioning as a reference clock." *Id.*

The ALJ also noted that, in the textbook co-authored by Dr. Oklobdzija, a section of the

book concerning clock generation states that "the VCO generates the internal clock by virtue of a control voltage created in response to the external reference." *Id.* at 120 (citing RX-2283 at GARMIN 92907). The ALJ found that "this process includes more than simply delivering sufficient power to enable the oscillator to oscillate." *Id.* at 121. Rather, "[t]he clock signal that is generated is a product of a control signal provided by the PLL and the reference frequency of the external crystal/clock." *Id.* The ALJ concluded that "the processes of setting the frequency of a clock signal and generating a clock signal are inseparable, because a clock signal must have a frequency, since its sole purpose is to provide a frequency for timing the operations of devices." *Id.* The ALJ further found that "[t]he external reference signal is integral to the generation of a clock signal, and by acknowledging that the PLL sets the frequency of the VCO in reaction to a reference clock signal from an external crystal or clock generator, Dr. Oklobdzija concedes that the PLL and its components rely on an external crystal/clock to generate a clock signal." *Id.* at 121-122. The ALJ, therefore, found that none of the Accused Products satisfy the "entire oscillator" limitations of the asserted claims. *Id.* at 122.

The ALJ rejected Complainants' argument that the Accused Products infringe even though they use an external crystal/clock generator to set or adjust the frequency of a clock signal. *Id.* at 122-124. Accordingly, the ALJ found that the oscillators in the Accused Products rely on control signals from within the PLL and on an external crystal/clock generator to generate a clock signal. *Id.* at 124. In particular, Respondents argued that "for the PLLs whose structures are known, the ring oscillators used in the VCO or ICO, as the case may be, cannot operate without a control signal from other PLL circuitry" and that "*all* of the ring oscillators use [ ] and therefore require and rely on control signals from other PLL

circuitry to operate." ID at 69 (emphasis added); *see also id.* at 69-73 (Respondents discussion of the so-called [ ] in the accused [ ]. The ALJ found that the so-called [ ] in the Accused Products operate only [ ] and that "[w]ithout those control signals [ ], 'oscillation unequivocally stops.'" *Id.* at 125 (citing Subramanian Tr., 1502-03).

The ALJ, however, addressed only the "current-starved" technology used in the accused [ ] chips and did not analyze the accused [ ] chips. *See* ID at 125-132. The Commission, therefore, determined to review the ID's findings concerning the "entire oscillator" limitation and posed the following question in the Notice of Review:

> With respect to the Accused Products using so-called "current-starved technology," specifically identify which accused chips are implicated, cite to the relevant evidence in the record, and discuss whether those products satisfy the "entire oscillator" limitation of claims 6 and 13 of the '336 patent.

78 *Fed. Reg.* at 71644.

**b. Analysis**

The parties agree that all of the [ ] chips in the Accused Products use "current-starved" technology. The parties also clarified in their submissions on review that the accused LSI chips only concerned terminated respondent Acer and are, therefore, no longer a part of the investigation. *See* 78 *Fed. Reg.* at 4 (terminating Acer). The primary dispute concerning the "entire oscillator" limitation comes down to how broadly the ALJ's construction of that limitation can be fairly read. Specifically, in responding to the Commission's request for briefing concerning the "entire oscillator" limitation, Complainants

again argue (as they did before the ALJ) that the ring oscillators [

] as long as they have a power supply, emphasizing the alleged difference between the PLLs in the Accused Products using an external crystal to set the frequency of the controlled oscillators and using an external crystal to generate the clock signal of the controlled oscillators.

We find that the ALJ's application of his construction of the "entire oscillator" limitation to the Accused Products was correct, including in particular his discussion of the intricate relationship between the generation and frequency of a clock signal. ID at 119-122. Specifically, the basis of the ALJ's finding concerning the reliance of the oscillators in the Accused Products on an "external crystal/clock generator" is that a "PLL controls the frequency of [a] VCO or ICO and adjusts it to match the reference frequency" and that "a PLL has circuitry that is used to set the frequency of a VCO to a multiple of another oscillator frequency functioning as a reference clock." ID at 119 (citing Oklobdzija Tr., 831, 824). The ALJ noted that Dr. Oklobdzija and his fellow authors concluded in a graduate-level textbook that, in a PLL, "the VCO generates the internal clock by virtue of a control voltage created in response to the external reference." *Id.* at 120. The ALJ found that "this process includes more than simply delivering sufficient power to enable the oscillator to oscillate[.]" *Id.* at 121. Furthermore, the ALJ found that "the process of setting the frequency of a clock signal and generating a clock signal are inseparable, because a clock signal must have a frequency, since it sole purpose is to provide a frequency for timing the operations of devices." *Id.* We affirm the ALJ's finding and analysis.

With respect to the use of "control signals," the ALJ found that "there are control signals within the PLLs themselves that are used to control the oscillation of the oscillators." *Id.* at 122

(citing Subramanian, Tr., 1316-32), 124.[12] The ALJ found that, in the [ ] shown in RX-621C, [ ]. *Id.* at 125.[13] In particular, he found that, even when [

]. *Id.* at 125-127 (citing Subramanian Tr., 1502-05). He also found that, contrary to Complainants' assertions, the [ ] shown in RX-621C [

]. ID at 128-129.

In finding that the [ ], the ALJ credited Dr. Subramanian's testimony that, according to the graph illustrated in Figure 2-11 (RX-621C at [

]. *Id.* at 130-131 (citing Subramanian Tr., 1454-1455). The ALJ disagreed with Complainants' argument that the graph at Figure 2-11 shows that the [

]. *Id.* Complainants' arguments provide no reasoned basis to disturb the ALJ's reliance on Dr. Subramanian's testimony.

Although the ALJ doesn't explicitly address the issue, we note that his analysis regarding the [ ] shown in RX-621C applies equally to the configuration of the same

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[12] The ID mistakenly cites Subramanian's testimony at beginning at 1306 instead of 1316.

[13] Respondents assert that [ ] use a [ ] and exhibit the same behavior as the [ ]. As such, we reject Respondents assertion in their reply submission that the [ ] is not representative of at least the [ ].

[ ] shown in Figures RDX-4.118C and 4.129C. *See* ID at 31-35. As with [ ] shown in RX-621C, the chip in RDX-4.129C provides [

] *See* Subramanian Tr., 1448:25-1449:10 (discussing [ ]). As such, [

] (*e.g.*, [ ] in RX-621C or [ ] in RDX-4.129C) cannot satisfy the requirements of claims 6 and 13 that the "entire oscillator" be "clocking said [CPU] at a clock rate." 336 patent at 2:18-21, 3:35-4-37. The ALJ correctly found that the Accused Products containing Qualcomm chips use a control signal to generate a clock signal and adopt the ALJ's finding of no infringement on this point.

With respect to the accused TI OMAP chips, we note that Complainants make no specific allegations regarding these chips in their review submissions, instead focusing their discussion entirely on the accused Qualcomm chips. The ALJ found that the accused TI OMAP chips also require a control signal. ID at 131. Specifically, the ALJ relied on the testimony of TI's corporate witness, Mr. Haroun, that the [

]. Furthermore, Mr. Haroun stated that [

].

The ALJ also relied on Mr. Haroun's testimony that [

]. The ALJ noted that Dr. Subramanian testified consistently. *Id.* at 131-132 (citing Subramanian Tr., 1186-89, 1319-20). Based on the ALJ's analysis, we agree that the ALJ correctly found that the Accused Products containing TI OMAP chips use a control signal to generate a clock signal and adopt the ALJ's finding of no infringement on this point.

With respect to the accused Samsung chips, the ID offers no analysis to support the ALJ's blanket finding that none of the oscillators in the Accused Products satisfy the "entire oscillator" limitation. *See* ID at 132. This is, however, not surprising considering Complainants made no specific arguments before the ALJ concerning the Samsung chips except to assert that they all use PLLs having VCOs that are ring oscillators. ID at 22. In their review submission, Complainants note only that the oscillators in the accused Samsung chips [ ] such that [ ]. The applied current, however, is the precise "control signal" that takes the Accused Products out of the scope of the "entire oscillator" limitation. We, therefore, affirm the ALJ's finding of no infringement with respect to the Samsung chips.

Respondents also provide specific evidence concerning the Samsung chips, which Complainants do not rebut. Specifically, Dr. Subramanian describes the accused Samsung PLLs as [

] *See* Subramanian Tr., 1198:14-1199:5, 1200:15-23; JX37C

at 853Samsung 170096-97 [ ]; *see also* Oklobdzija Tr., 988:18-989:15 [ ]. Respondents further note that exhibit JX-37C shows that [ ] *Id.* (citing Subramanian Tr., 1199:6-13; JX37C at 853Samsung 170096-97). Based on this evidence, we find that the Accused Products containing Samsung chips use control signals to generate a clock signal and, therefore, do not infringe the "entire oscillator" limitation.

Based on the preceding discussion, the Commission affirms the ALJ's finding that the Qualcomm, TI OMAP, and Samsung chips in the Accused Products do not satisfy the "entire oscillator" limitation due to the fact that all of the accused chips use PLLs having [ ].

**2. "Varying . . . in the Same Way"**

**a. Proceedings Before the ALJ**

The ALJ found that the limitation "varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way" of claims 6 and 13 requires no construction and would have been understood by a person of ordinary skill in the art at the time of the invention according to its plain and ordinary meaning." Markman Order No. 31 at 68; *see* ID at 16. Based on this claim construction, the ID finds that the Accused Products do not satisfy the "varying … in the same way" limitations of the asserted claims. ID at 189-213. No party petitioned for review of this construction.

With respect to infringement, the ALJ found, as an initial matter, that Complainants

failed to "perform any testing and did not produce any empirical evidence of their own, despite the fact that Dr. Oklobdzija . . . thought it appropriate and desirable to do so." *Id.* at 190. While the ALJ did not find that Complainants' failure was fatal to its infringement case, he noted that "under the particular facts and circumstances of this case, the weight of the evidence is affected by the presence or absence, as the case may be, of evidence of that caliber." *Id.* at 192, n. 19. The ALJ concluded that the Accused Products, which use PLLs, do not infringe because "a PLL outputs a very stable and fixed frequency," as shown by the results of Dr. Subramanian's tests. *Id.* at 182-193.

The ALJ took particular note of Complainants' argument that the processing frequency of the CPU will always track the "entire" oscillator's clock rate because the oscillator's clock rate is what clocks the CPU. *Id.* at 193-194. The ALJ found that Complainants reasoning is flawed because "it avoids the fact that the 'entire' oscillator terms are inextricably tied to the 'varying' term of the claims." *Id.* at 194 (citing Markman Order No. 31 at 42). The ALJ found that "the evidence shows that none of the Accused Products meet any of the 'entire' limitations of the asserted claims[] because the frequencies of the oscillators in the Accused Products are fixed by external crystals/clock generators as well as internally by the PLLs." *Id.* at 194. The ALJ rejected Dr. Oklobdzija's testimony about infringement of the "varying" terms as improperly divorced from the effects of external crystals and their associated PLLs. *Id.* at 194-195. By contrast, the ALJ found that Dr. Subramanian properly "took into account the 'entire' terms, as construed, in addressing the 'varying' limitations and that the testing he described and the data

obtained therefrom are reliable and support his opinion" of non-infringement. *Id.* at 196.[14] Complainants did not challenge the ALJ's findings concerning the results of Dr. Subramanian's testing in their petition for review.

Complainants further asserted that the chip manufacturing industry "engages in a common practice called 'binning'" to account for the varying performance levels of chips due to the manufacturing process, and that this procedure satisfies the "varying" limitations of claims 6 and 13. *Id.* at 143-144.. *Id.* at 143-144. The ALJ found that "while binning is a reflection that variations exist in the performance capabilities of microprocessors . . . this does not constitute evidence that any of the Accused Products meet the 'varying' limitations of the asserted claims." *Id.* at 209. Specifically, the ALJ concluded that "Dr. Subramanian's testimony and the testing it was based on empirically demonstrate that the operation frequencies of the chips, no matter their individual differences[,] are fixed." *Id.* (citing Subramanian Tr., 1265-66).

Complainants argued in their petition for review that the ALJ failed to take into account the specific language of asserted claims 6 and 13 and consider whether the CPU and clock rate of the oscillator vary in the same way due strictly to their fabrication process, as opposed to operational parameters. Complainants contended that the fact that the chips in the Accused Products are subjected to "binning" proves that processing frequency of the CPU in the Accused Products will always vary with the clock rate of the on-chip oscillator as a function of the fabrication parameters that were fixed in the chip at the factory.

[14] The ALJ made detailed findings concerning Dr. Subramanian's testing at pages 196-204 of the final ID.

**b. Analysis**

Claims 6 and 13 recite two different "varying" limitations: "varying . . . as a function of" and "varying . . . in the same way."[15] Complainants' arguments concern only the former phrase. We, therefore, focus our analysis on the question of whether the Accused Products satisfy the requirement of claims 6 and 13 that the "processing frequency" of the CPU and the "clock rate" of the on-chip oscillator must "vary . . . as a function of parameter variation in one or more fabrication or operational parameters associated with [the] integrated circuit substrate[.]" *See* '366 patent at 2:22-28, 3:38-45. We also note that Complainants did not argue in their petition for review that the Accused Products infringe claims 6 and 13 due to the effects of any operational parameters, *i.e.* operating temperature and operative voltage, instead focusing solely on whether the Accuse Products infringe due to the effects of fabrication parameter variations and, as a result, the concept of "binning." We find, therefore, that Complainants have abandoned any argument concerning operational parameters. *See* 19 C.F.R. § 210.43(b)(2) ("Any issue not raised in a petition for review will be deemed to have been abandoned by the petitioning party and may be disregarded by the Commission in reviewing the initial determination (unless the Commission chooses to review the issue on its own initiative under § 210.44)).

Furthermore, we disagree with Complainants regarding the significance of the binning process. The binning process merely sorts individual chips based on the maximum processing frequency at which a chip is capable of operating and has nothing to do with the actual frequency and clock rate at which a chip operates. *See* Subramanian Tr., 1264:5-1265:10, 1264:19-1265:18;

[15] The parties requested construction only of the limitation "varying . . . in the same way." Markman Order at 57-68.

1271:21-25). Complainants' expert confirmed our understanding on this point. *See* Oklobdzija Tr., 1030:18-21; *see also id.* 300:20-21 (emphasis in original) ("So we'll sell [the chips] out according to their *ability* to run."). Claims 6 and 13, on the other hand, require variation in the chip's "processing frequency," or the frequency at which the chip operates, not variation in the chip's maximum processing frequency capability. This distinction is made evident by comparing the phrase "processing frequency" in claims 6 and 13 with the phrase "processing frequency capability" in claims 1 and 11 of the '336 patent.

The ID properly recognizes this distinction, finding that "[b]y conflating these two distinctly-claimed elements, Dr. Oklobdzija disregards an important fact about the accused chips and products: by design, a PLL compensates for any PVT-related effects in order to maintain a stable and fixed frequency." *Id.* at 210 (citing Subramanian Tr., 1273; RDX-4C.111)). The ALJ noted in particular the testimony of Respondents' expert, Dr. Subramanian, that "while PVT affects the maximum operating capability of a transistor, the PLL and its components are not running at this maximum capability, and this allows them to provide a fixed output frequency[.]" *Id.* at 210-11 (citing Subramanian Tr., 1295). The ALJ concluded that "a part's processing frequency capability may change with PVT, but its actual speed, or processing frequency, remains constant. . . .While oscillators in the PLLs of the Accused Products are capable of variable frequencies in response to PVT factors, nevertheless, they are constrained to provide fixed clocking signals to the CPU[.]" *Id.* at 211. We agree with the ALJ's conclusion that the "maximum achievable performance" (*see* Subramanian Tr., 1122:1-1123:7) which is affected by the fabrication process is different from the actual "processing frequency" at which a chip operates at a given time. The "processing frequency" of the Accused Products during operation

is precisely what must "vary[] . . . as a function of parameter variation" in order to satisfy claims 6 and 13.

Dr. Subramanian's empirical tests do not directly address the issue of whether accused chips that were sorted differently according to the "binning" process do, in fact, operate differently in terms of frequency. Nevertheless, the fact that his tests showed how the PLL maintains a fixed frequency of operation regardless of variations in temperature and voltage is easily extrapolated to conclude that the PLL similarly affects chips that may be assigned different operating capabilities during "binning," *i.e.*, maintains them at a fixed operating frequency. *See* ID at 193. We further note that Complainants did not present any empirical evidence to support their position or to rebut Dr. Subramanian's test results.

We also reject Complainants' argument that the ALJ ignored the disjunctive nature of the claim limitation, which recites that the oscillator clock signal and the CPU processing frequency vary "as a function of parameter variation in one *or* more fabrication or operational parameters." '336 patent at 2:22-28, 3:38-44 (emphasis added). Rather, the ALJ correctly noted that, because the Accused Products use PLLs, there is no variation in their processing frequency due to ***any*** parameter, be it fabrication or operational-based. *See* ID at 210-211 (discussing the effect of a PLL on the processing frequency of a transistor).[16]

In addressing the Commission's question concerning "current-starved" oscillators, Complainants present an entirely new argument regarding why the [

[16] The specification of the '336 patent describes how the fabrication ("processing") of a chip can affect the operating speed of the chip if allowed and not merely affect the maximum speed capability of the chip. *See* '336 patent at 17:2-10.

] satisfy the "entire oscillator" limitation of claims 6 and 13. Specifically, Complainants now argue that the [ ] is an "operational parameter." In making this argument, Complainants necessarily implicate the "varying" limitation. We again note that Complainants did not challenge the ID's findings that the Accused Products do not satisfy the "varying" limitations with respect to "operational parameters" in their petition for review, instead focusing solely on the "fabrication parameters." As stated above, we find that Complainants have, thus, abandoned any argument that the Accused Products infringe claims 6 and 13 due to the effects of "operational parameters." Nevertheless, Complainants' arguments are also incorrect on the merits.

In arguing that the [

] is, in fact, one of the "operational parameters" recited in the asserted claims and not a forbidden "control signal," Complainants attempt to draw a distinction based on the doctrine of claim differentiation between the term "operational parameters" in claims 6 and 13 and the specific recitation of the terms "temperature" and "voltage" as a type of operational parameter in dependent claims 7 and 14. Specifically, Complainants argue that the term "operational parameters" as used in claims 6 and 13 must be broader and encompass other operational parameters beyond temperature and voltage. In particular, Complainants advocate for extending "operational parameters" to include current as well as voltage. Complainants assert that, because the oscillator clocks the CPU, the "clock rate" of the "entire oscillator" will *always* "vary . . . in the same way" as the "processing frequency" of the CPU in the accused chips by definition. Complainants contend that, as a result, the clock rate of the oscillator and, consequently, the processing frequency of the CPU vary "as a function of parameter variation" in

the [ ]. Complainants conclude that, because the [ ] is an "operational parameter," it cannot have been disclaimed despite the limitation in the claim construction of "entire oscillator" of not relying on "control signals" to "generate a clock signal."

Respondents argue that Complainants waived this novel argument by never before presenting the concept of a bias current being an "operational parameter." We agree. *See Hazani v. Int'l Trade Comm'n*, 126 F.3d 1473, 1479 (Fed. Cir. 1997) (finding argument not raised before the ALJ waived); *Broadcom Corp. v. Int'l Trade Comm'n*, 542 F.3d 894, 900-1 (Fed. Cir. 2008) (declining to address arguments not raised before the ALJ or the Commission).

Moreover, the ALJ explicitly found that the frequency of the oscillators in the Accused Products do not vary as a function of PVT parameters. *Id.* at 3 (citing ID at 192-204 (discussing Dr. Subramanian's empirical testing of the accused chips)). Rather, the ALJ found that the very function of the PLLs in the accused chips is to maintain the oscillators in those chips at a constant, un-varying frequency as a function of the frequency of an external crystal oscillator. ID at 119 (noting Dr. Oklobdzija testimony that "'the PLL controls the frequency of that VCO or ICO and adjusts it to match the reference frequency.'"); *id.* at 121-122 ("[B]y acknowledging that the PLL sets the frequency of the VCO in reaction to a reference clock signal from an external crystal or clock generator, Dr. Oklobdzija concedes that the PLL and its components rely on an external crystal/clock to generate a clock signal."). The ALJ specifically noted that "the 'entire' oscillator terms are inextricably tied to the 'varying' term of the claims." *Id.* at 194. The ALJ, thus, concluded that "[t]he relevant oscillators in the Accused Products" clock their associated [CPUs] by providing a fixed frequency, instead of varying the frequency, through the

involvement of their external crystals/clock generators and the PLL circuitry in which the oscillators reside." *Id.* at 195. This finding by the ALJ is independent of his finding that the accused chips also rely on control signals, which is the only factor implicated by Complainants' new "[ ] as operational parameter" argument. Complainants' new assertion cannot, therefore, overcome the conclusion that the oscillators in the Accused Products do not satisfy the "entire oscillator" limitation or the "varying" limitation.

Complainants also fail in the context of the requirement that the claimed "varying" be independent of control signals. In particular, Complainants' current argument is at odds with the very point they made before the ALJ concerning the source of the claimed "operational parameters." Complainants' expert, Dr. Oklobdzija relied on a specific passage from a textbook concerning microprocessors in arguing that "transistors on the same chip are similarly affect by variations in process, voltage and temperature." ID at 134. The textbook states the following:

> Variation is the deviation from intended or designed values for a structure or circuit parameter of concern. The electrical performance of microprocessors or other integrated circuits are impacted by two sources of variation. *Environmental factors* arise during the operation of a circuit, and include variations in *power supply*, switching activity and *temperature of the chip or across the chip*. Physical factors during manufacture result in structural device and interconnect variations that are essentially permanent. These variations arise due to processing and masking limitations, and result in random or spatially varying deviations from designed parameters.

*Id.* (emphasis added) (citing CX-154 at TPL853_0297444; Oklobdzija Tr., 416-418). Complainants emphasized that "the environmental factors that cause variations in performance include changes in '*power supply*' (voltage) and 'temperature[.]'" *Id.* at 134-135 (emphasis added). Complainants further asserted that "no one disputes that *all of the transistors on the*

*same chip, including ring oscillators and CPUs, will be affected by changes in PVT.*" *Id.* (emphasis added). As such, based on Complainants' own explanation, the voltage or current that may be considered an "operational parameter" as recited in claims 6 and 13 must result from an "environmental factor" that affects "all of the transistors on the same chip, including the ring oscillators and CPUs," such as the chip's "power supply."

Complainants provide no evidence or argument regarding how the [ ] used to control the frequency of the oscillators in the Accused Products can be considered the "power supply" that is available to "all of the transistors on the same chip, including the ring oscillators and CPUs." Moreover, the evidence shows that the [ ], for example, [ ]. *See* ID at 127-128. Dr. Oklobdzija confirmed that the same is true for the [ ]. Oklobdzija Tr., 968-989, 1058-1059 (explaining that the [ ].

We find that the evidence does not support extending the ALJ's finding concerning the power supply [ ] to all of the accused chips. In particular, with respect to the accused TI OMAP chips, TI's corporate witness, Mr. Haroun, testified that [ ]. However, Complainants do not present any evidence, nor could we find any from Mr. Haroun's testimony, that the CPU in the TI OMAP chips is not independently powered. It is Complainants' burden to do so given that they must show the Accused Products do not rely on control signals to generate the clock signal in the on-chip

oscillators.

Based on the preceding discussion, the Commission rejects Complainants' new argument that the [ ] is an operational parameter and not a control signal as waived and, moreover, unsupported by the record. We also note that Complainants' argument has no bearing on the ALJ's finding that the oscillators in the Accused Products do not "vary . . . as a function of" PVT parameters because the PLLs in those chips control the oscillators to match their output frequency to the reference frequency of an "external crystal/clock generator." The Commission, therefore, affirms the ID's finding that the Accused Products do not satisfy the "varying" limitations of claims 6 and 13.

### 3. "External Clock [] Operative At A Frequency Independent" and "Asynchronously"

#### a. Proceedings Before the ALJ

The ALJ construed the limitation "[an] external clock is operative at a frequency *independent* of a clock frequency of said oscillator" in claims 6 and 13 of the '336 patent to mean "an external clock wherein a change in the frequency of either the external clock or oscillator does not affect the frequency of the other." Markman Order No. 31 at 11 (emphasis added); *see* ID at 14. This construction was uncontested. *Id.* The ALJ also construed the limitation "wherein said central processing unit operates *asynchronously* to said input/output interface" of claim 13 to mean "the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them." *Id.* at 74 (emphasis added); *see* ID at 16. Complainants did not petition for review of the ALJ's construction of the