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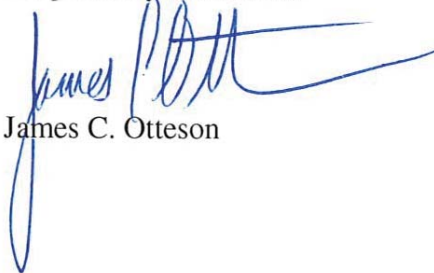
Lisa R. Barton
Acting Secretary
U.S. International Trade Commission
500 E Street, S.W.
Washington, DC 20436

**Re: *Certain Wireless Consumer Electronics Devices and Components Thereof,*
Inv. No. 337-TA-853**

Dear Secretary Barton:

Enclosed for filing please find **Complainants' Petition for Review of Initial Determination on Violation of Section 337 and Recommended Determination on Remedy and Bond (Public Version)** in the above-referenced investigation.

Respectfully submitted,



James C. Otteson

Enclosures

UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.

Before the Honorable E. James Gildea
Administrative Law Judge

In the Matter of

Certain WIRELESS CONSUMER
ELECTRONICS DEVICES AND
COMPONENTS THEREOF

Investigation No. 337-TA-853

COMPLAINANTS' PETITION FOR REVIEW OF
INITIAL DETERMINATION ON VIOLATION OF SECTION 337 AND
RECOMMENDED DETERMINATION ON REMEDY AND BOND

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Table of Abbreviations

ALJ	The Administrative Law Judge presiding over the current Investigation
'336 patent	U.S. Patent No. 5,809,336, admitted as JXM-1.
Complainants	Technology Properties Limited LLC, Phoenix Digital Solutions LLC and Patriot Scientific Corporation
HT	Hearing Transcript for the evidentiary hearing held in this Investigation from June 3, 2013 through June 11, 2013
ID	Initial Determination on Violation of Section 337 and Recommended Determination on Remedy and Bond (Sept. 6, 2013), Inv. No. 337-TA-853
Patriot	Complainant Patriot Scientific Corporation
PDS	Complainant Phoenix Digital Solutions
Respondents	Respondents Acer Inc., Acer America Corporation, Amazon.com, Inc., Barnes & Noble, Inc., Garmin Ltd., Garmin International, Inc., Garmin USA, Inc., HTC Corporation, HTC America, Huawei Technologies Co., Ltd., Huawei North America, Huawei Device Co., Ltd., Huawei Device USA Inc., Futurewei Technologies, Kyocera Corporation, Kyocera Communications, Inc., LG Electronics, Inc., LG Electronics U.S.A., Inc., Nintendo Co., Ltd., Nintendo of America, Inc., Novatel Wireless, Inc., Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Sierra Wireless, Inc., Sierra Wireless America, Inc., ZTE Corporation, and ZTE (USA) Inc.
TPL	Complainant Technology Properties Limited

*All emphasis in this brief is added, unless otherwise noted.
Emphasis is added to figures using yellow highlighting and colored rectangles.*

I. ISSUES UPON WHICH REVIEW IS SOUGHT

1. Whether the ID's findings regarding the "entire oscillator" limitations of claims 6 and 13 are clearly erroneous findings of material fact because they fail to consider Complainants' substantial evidence that the accused products have ring oscillators.
2. Whether the ID's conclusions regarding the "entire oscillator" limitations of claims 6 and 13 are clearly erroneous as a matter of law because the ID failed to apply the correct claim construction for "entire oscillator."
3. Whether the ID's conclusions regarding the "varying" limitations of claims 6 and 13 are clearly erroneous as a matter of law because the ID failed to apply the actual claim language: "varying . . . in the same way as a function of parameter variation *in one or more* fabrication **or** operational parameters."
4. Whether the ID's conclusions regarding the "independent" limitation of claims 6 and 13 are clearly erroneous as a matter of law because the ID failed to apply the controlling claim construction of "independent."
5. Whether the ID's findings regarding the "independent" limitation of claims 6 and 13 are clearly erroneous findings of material fact because they: (a) are based on evidence that applies only to claims 1 and 11; and (b) fail to consider Complainants' evidence concerning claims 6 and 13.
6. Whether the ID's conclusions regarding the "asynchronous" limitation of claim 13 is clearly erroneous as a matter of law because the ID failed to apply the controlling claim construction of "asynchronous."
7. Whether the ID's findings regarding the "asynchronous" limitation of claim 13 are clearly erroneous findings of material fact because the ID discarded testimonial and documentary evidence showing that the Accused Products meet this limitation.
8. Whether the ID's findings that Complainants have not established that Respondents Barnes & Noble, Garmin, HTC, Huawei, and Samsung had a commercially significant inventory in the United States are erroneous in fact and law.

II. INTRODUCTION

In 1989, when Messrs. Moore and Fish filed their application for the '336 patent, the fastest commercially available microprocessor was Intel's 486 processor operating at 33 MHz. That same year, using the invention claimed in the '336 patent, the inventors were able to produce an inexpensive processor that ran more than twice as fast, at 70 MHz. They achieved

this substantial performance boost through an innovation regarding how they clocked their processor.

The speed of all microprocessors is governed by timing control signals called clocks. Requiring processors to perform operations in cycles timed to a specific frequency allows them to operate in concert with other components. Up until Messrs. Moore and Fish's invention, timing control was achieved through the use of crystals that could be caused to resonate and produce an oscillating signal used as a clock. However, the use of crystals was fundamentally limited because crystals cannot be located on the chip with the CPU and because crystals cannot be processed with enough precision to produce frequencies higher than roughly 30 MHz. In other words, without an advance in clocking technology, processor performance would have been stuck at the level the 1989 Intel 486 processor. Without the additional speed found in today's microprocessors, operations like watching a video, surfing the Internet and other now-common activities would be impossible.

The '336 patent solves the external crystal speed barrier by moving the clock onto the same chip as the CPU. However, due to manufacturing limitations, a crystal cannot be moved on chip; the inventors needed another structure. They selected a known structure that had not been used to clock CPUs in the past, known as a ring oscillator. A ring oscillator is a circuit that receives a voltage or current input that passes through multiple inverters and then loops back on itself to cause the current or voltage to oscillate between a high and low state with a specific periodicity or frequency. This results in a wave pattern of highs and lows in which faster frequencies are represented by faster oscillations between the high and low states.

Today, virtually all modern microprocessors, including those in Respondents' phones, tablets, and other accused products, use ring oscillators incorporated onto the same chip as the CPU to produce clock signals. They all exploit the performance advantage first realized by Messrs. Moore and Fish in 1989, and which the '336 patent protects. Complainants, Patriot and TPL, are successors-in-interest to the '336 patent. Complainants have heavily invested in a

domestic industry through licensing the '336 patent. They come to the Commission now to seek protection of that domestic industry.

The ID presents a series of clearly erroneous legal and factual findings relating to the '336 patent's claims: (1) the "entire oscillator" limitations of Claims 6 and 13; (2) the "varying" limitations of Claims 6 and 13; and (3) and the external second clock limitations of claims 6 and 13.¹ The ID also committed clear error in declining to issue cease and desist orders. On these grounds, Complainants respectfully petition for review.

The ID clearly errs with respect to (1) the "entire oscillator" limitations for two reasons. First, the ALJ issued an erroneous construction of these terms. Specifically, the ALJ's construction of "entire" impermissibly imports limitations into the claims. Still, Complainants proved that Respondents' accused products infringed Claims 6 and 13 under the ALJ's impermissibly limited construction. Second, in the ID the ALJ applied a wholly new (and unsupported) construction of "entire". Only under this new and unsupported construction could the ALJ conclude Respondents' accused products did not infringe.

The ID commits clear error with respect to (2) the "varying" limitations by failing to take into account substantive differences between claims 6 and 13 and the other claims. Independent Claims 6 and 13 of the '336 patent require that the "entire oscillator" and CPU vary together due to at least one of three conditions -- **p**rocess, **v**oltage **or** **t**emperature ("PVT"). Other asserted claims required variation due to **all three** conditions. Complainants elicited undisputed evidence at the hearing that the CPU and the "entire oscillator" in Respondents' accused products vary together due to at least one condition -- **p**rocess variation. Process variation occurs when two chips of the same design have different maximum operating speeds to due to variations in the manufacturing process. Respondents' expert admitted that **all** manufacturers of the processors in the accused products engage in a practice called "binning" -- sorting processors based upon

¹ In an attempt to streamline this Petition, Complainants have chosen to focus only on claims 6 and 13 of the '336 patent. At the hearing, Complainants accused claims 1, 7, 9, 10, 11, 13, 14, 15 and 16.

speed differences created due to process variation. This alone satisfies Claims 6 and 13’s “varying” limitations. The ID committed error by failing to recognize that process variation alone satisfies Claims 6 and 13, requiring instead variation according to process, voltage, *and* temperature.

The ID commits two clear errors that warrant review of its findings relating to (3) the external second clock limitations. First, the ID applies an infringement test that is inconsistent with the ALJ’s claim construction. Rather than determine whether the first and second clocks are dependent on each other, the ID finds noninfringement because the first clock and second clocks supposedly share the same reference signal—an irrelevant factor under the operative claim construction. Second, the ID fails to evaluate the unique aspects of “independent” and “asynchronous” limitations as they appear in claims 6 and 13, which require the second clock to be *external* to the microprocessor. Instead, the ID examines three exemplary arguments from Respondents regarding *internal* clocks relevant only to claims 1 and 11 and then mistakenly extends them to all the claims.

Finally the ID did not recommend the issuance of cease and desist orders, finding that Complainants did not prove “commercially significant” inventories of accused products in the U.S. This finding ignores the parties’ admitted stipulations showing Respondents’ inventories.

For these reasons, Complainants respectfully ask the Commission to review the ID.

III. STATEMENT OF FACTS

A. The ’336 Patent.

The ’336 patent issued on September 15, 1998 to Charles Moore and Russell Fish, based on a parent application filed on August 4, 1989. JXM-1. The ’336 patent has faced six *ex parte* reexamination challenges, and has overcome 607 prior art references. Respondents did not challenge its validity. The ’336 patent teaches the use of two independent clocks in a microprocessor system: (1) an on-chip ring oscillator as a CPU/system clock to time the CPU; and (2) a second independent clock to time the on-chip I/O interface. ’336 patent, Figs. 17, 18.

Decoupling the ring oscillator CPU clock from the I/O clock permits the clocks to run independently, and frees the CPU clock to run much faster than any crystal oscillator.

Essentially all modern wireless products use the '336 patent's invention. Indeed, Complainants technical expert, Dr. Vojin Oklobdzija, testified that "a ring oscillator is basically a source for all the clocks in all the microprocessor systems that I know." HT 262:7-11. One important reason for this is that microprocessors for modern wireless products must run at very high frequencies, frequencies higher than any crystal oscillator can produce. HT 1379:10-1380:13; 1378:24-1379:3 ("difficult and economically unviable to cut quartz crystals precisely to produce oscillations in the gigahertz range"). Further, Dr. Oklobdzija testified that, "[t]he oscillator that generates the clock signal has to be integrated on the chip," because "the frequency that that ring oscillator produces is too high to be delivered from the – through the outside pins." HT 414:15-415:1.

In addition to massively increased speed, the '336 invention also exploits advantages gained by placing the ring oscillator clock and the CPU on the same silicon chip. The transistors on the same silicon die are affected in a similar manner; not only by processing differences, but also by changes in operating conditions, like changes in voltage and temperature. HT 278:22-279:19; HT 462:12-463:5; HT 1121:18-25; CDX-5C.39, CX-154 at TPL853_02927444-45. Semiconductor manufacturing or "processing" differences cause different chips to have different operating characteristics, even if they nominally have the same design. HT 302:9-303:17; 1272:1-3. This allows a better match between the CPU/system clock and the CPU of the microprocessor. At the same time, the I/O interfaces are unaffected and run at their own speed. HT 279:20-280:6.

B. The Accused Products; Overview of PLLs.

The Accused Products comprise a diverse range of consumer electronic products: Barnes & Noble's e-readers and tablet computers; Garmin's navigation devices; HTC's smartphones and tablet computers; Huawei's smartphones and tablet computers; LG's smartphones and mobile phones; Novatel Wireless's mobile hotspots; Samsung's smartphones; and ZTE's smartphones,

mobile phones, mobile hotspots, USB modems, tablet computers, and wireless home phones.² For trial, Complaints grouped the Accused Products of each Respondent into categories with common proof, such as products that contained the same microprocessor.

The accused products include microprocessor chips that exploit the '336 invention, made by Qualcomm, Texas Instruments or Samsung. In particular, the accused products each include a ring oscillator (within a PLL) used as the CPU/system clock. The ring oscillator *generates* the clock signal for the CPU, while the additional PLL circuitry *adjusts* the frequency of the clock signal generated by the ring oscillator. HT 1048:25-1049:24; HT 1051:12-1052:3; HT 1053:1-7.

The ring oscillator in the PLLs automatically generates a high frequency clock signal as long as it has an analog power supply. HT 389:14-390:16; HT 957:21; CX-648C (regarding ring oscillator in ██████████ PLL). The ring oscillator does not rely on any digital control signal or external crystal to generate its clock signal. HT 1054:5-1055:3. After the ring oscillator generates the clock signal, that signal passes through a frequency divider, which divides it down to a lower frequency that is then passed to a phase detector. RDX-4.115; HT 1397:22-1398:2; 1398:23-1399:4; *see also* 1386:25-1387:25, 1388:13-19. The frequency divider reduces the high speed ring oscillator clock signal down to a level where it can be compared to a much slower reference signal. The phase detector compares the divided-down frequency with a reference signal (similar to a "speed limit" sign) obtained from an external crystal oscillator. RDXM-1-21; HT 1381:11-1382:12, 1388:20-1389:15. Based upon this comparison, the phase detector provides appropriate correction signals to a filter to adjust the variation detected in the ring oscillator. The filter then provides a smooth analog power supply (voltage/current) to the ring oscillator. RDXM-1-21; RDX-4.94; HT 1389:16-22; 1383:11-1384:3.

² Complainants have moved to terminate Acer, Amazon and Kyocera from the Investigation. Those motions are pending. Dkt. 853-068C; 853-069C; 853-070C.

C. The Evidentiary Hearing.

The ALJ conducted an evidentiary hearing on June 3-11, 2013. Complainants presented testimony from their technical expert, Dr. Vojin Oklobdzija, a foremost expert in the clocking of microprocessors, and the president elect of one of the IEEE societies. HT 243:24-250:9. Respondents presented testimony from a single technical expert, Dr. Vivek Subramanian of U.C. Berkeley. Respondents withdrew their invalidity case, as well as all of their fact witnesses during the hearing. HT 1524:9-1525:10; 1828:5-1829:3.

IV. INFRINGEMENT

A. The ALJ Committed Clear Errors of Fact and Law to Find Noninfringement Based on the “Entire Oscillator” Limitations of Claims 6 and 13.

1. The ALJ committed clear error by ignoring undisputed evidence that all Accused Products include ring oscillators.

The ALJ concluded that Complainants did not meet their burden of proof that the accused chips included the claimed ring oscillators because they supposedly relied on a “blanket assumption.” “[m]ore is required than a blanket assumption based on Dr. Oklobdzija’s general knowledge of digital system clocking to warrant reliance.” ID at 118-19. The ID’s suggestion that Complainants relied on an “assumption” ignores overwhelming evidence from Respondents’ engineers, the engineers of third party chip makers, as well as detailed schematics of ring oscillators found within the [REDACTED] chips in Respondents’ products. Finally, the ALJ entirely ignored Dr. Oklobdzija’s specific testimony about this evidence, which identifies specific ring oscillators in the particular accused products in this Investigation.

a. *The Texas Instruments (“TI”) OMAP processors use ring oscillators to generate a clock signal.*

The TI OMAP processors may be divided into two families: (1) the OMAP4 family, including the OMAP4470, OMAP4460 and OMAP4430 processors, and (2) the OMAP3 family,

including the OMAP3530, OMAP3611, OMAP3621 and OMAP3630.³ Various Respondents incorporate these chips into their Accused Products, including [REDACTED]

TI's corporate witness appeared at the hearing and testified that [REDACTED]

[REDACTED]

The OMAP3 and OMAP4 chips at issue contain a [REDACTED]

[REDACTED] HT 181:8-18.⁹ TI's witness specifically confirmed that each of these [REDACTED]

³ HT 172:11-16, 174:16-20, 175:13-24, 1182:24-1183:15; RDX-4.71C.

[REDACTED]

⁵ HT 171:17-172:10, 181:1-4, 196:18-25, 197:1-4; CX-318C at AMZ_TPL_00039975; CX-316C at AMZ_TPL_00024483; CX-321C at AMZ_TPL_00059492; CX0366C at GARM-N37xx-031357; CX-353C at GARMIN068385; CX1142 at 65:5-12, 73:13-16.

⁶ HT 171:3-5 (confirming that OMAP processors are "systems on chip"), 179:3-8, 181:5-7, 196:18-25, 480:2-21, 481:12-25, 484:3-7, 489:16-25; CDX-6C.18, 20, 22, 28.

⁷ CX-318C (OMAP4470 TRM) at AMZ_TPL_00040084. *See also* CX-316C (OMAP4460 TRM) at AMZ_TPL_00024590; CX-321C (OMAP4430 TRM) at AMZ_TPL_00059599; CX-366C (OMAP35x TRM) at GARM-N37xx-031493 [REDACTED]

[REDACTED] CX-353C (OMAP36xx TRM) at GARMIN068489 (same).


⁸ CX-318C (OMAP4470 TRM) at AMZ_TPL_00040085. *See also* CX-316C (OMAP4460 TRM) at AMZ_TPL_00024591; CX-321C (OMAP4430 TRM) at AMZ_TPL_00059600; CX-366C (OMAP35x TRM) at GARM-N37xx-031496 [REDACTED]

[REDACTED] CX-353C (OMAP36xx TRM) at GARMIN068492 [REDACTED]

[REDACTED]

⁹ *See also* CX-318C (OMAP4470 TRM) at AMZ_TPL_00040084 [REDACTED] CX-316C (OMAP4460 TRM) at AMZ_TPL_00024590 (same); CX-321C (OMAP4430 TRM) at AMZ_TPL_00059599 (same); CX-366C (OMAP35x TRM) at GARM-N37xx-031493 [REDACTED]

[REDACTED] CX-353C (OMAP36xx TRM) at GARMIN068489 (same);

¹⁰ These ring oscillators generate an oscillation (*i.e.*, a clock signal) due to the presence of an odd number of inversions arranged in a loop. HT 190:1-23. *TI's witness drew representations of the ring oscillators in the OMAP3 and OMAP4 chips* in CDX-80C¹¹:



Respondents' expert also confirmed that these differential inverter structures are "ring oscillators" under the ALJ's claim construction. HT 1392:4-13; 1392:25-1393:23; 1394:16-1395:5.

Despite TI's testimony—including the drawing of ring oscillators found in Respondents' accused products—the ALJ did not consider any of this evidence in pronouncing that Complainants had relied on a "blanket assumption." This was a clear error.

b. *The Qualcomm processors use ring oscillators to generate a clock signal.*

Complainants proved that the Qualcomm microprocessors in the accused products contain ring oscillators (within PLLs) to clock the CPU. Dr. Oklobdzija testified that Qualcomm

HT 178:24-179:2 (referring to Fig. 3-32 of CX-318C), 179:9-12, 180:3-25, 198:20-199:6, 199:17-20, 200:4-14.

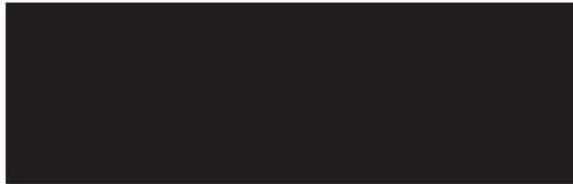
¹⁰ HT 190:6-191:20, 192:25-194:10, 197:15-198:9. Dr. Oklobdzija confirmed this. *See* HT 474:6-485:2, 486:20-489:15; CDX-6C.2, 7, 10, 12, 13, 14, 18, 20, 21, 22, 23, 24.

¹¹ HT 192:25-194:12, 1189:22-1190:3.

uses the same (or similar) PLL designs for [REDACTED]

[REDACTED] HT 445:23-446:5.¹²

For example, the [REDACTED] include the [REDACTED] Qualcomm processor. This chip family uses an on-chip oscillator within a [REDACTED] to clock the CPU.¹³ The ring oscillator in the [REDACTED] is shown below:



See CX-648C at QTPL-0001070; CDX-5C.21; HT451:4-17 [REDACTED]

[REDACTED] CDX-16C.09; HT 552:1-553:16 (discussing ring oscillators in [REDACTED] processor family).

The [REDACTED] family's clock generation takes place entirely on the same chip as the CPU core. CX-663C at QTPL-0047361; CDX-5C.22; HT 451:18-452:2 ("So everything in blue is on the same silicon. [REDACTED] product contains . . . processors . . . and a clock generation block, which clocks or this generates the clock to clock those processors.").

Complainants furnished voluminous evidence showing ring oscillators in other Qualcomm processors for [REDACTED] Accused

¹² For example, the Accused Products include Qualcomm [REDACTED] (HT 356:1-358:11), Qualcomm [REDACTED] RX-621C; HT 1450:5-19), and Qualcomm [REDACTED] (CX-648C; HT 362:5-366:9).

¹³ CX-663C at QTPL-0047361 [REDACTED] HT 352:7-353:1 [REDACTED] accord CX-262C [REDACTED] at [REDACTED] Respondents' expert confirmed that the [REDACTED] processor family uses the Qualcomm [REDACTED] See RDX-4.42C; HT 1147:13-1148:7; RDX-4.64C; HT 1174:18-25 ("it's the [REDACTED] that is associated with the accused core functionality. And this is a [REDACTED] technology node chip.").

Products.¹⁴ Testimony from Complainant’s expert to the effect that 99% of all microprocessors contain ring oscillators is no reason for the ID to ignore the mountain of evidence specific to the ring oscillators in Respondents’ actual Accused Products. Ignoring this evidence was clear error.

¹⁴ Ring oscillators exist, for example, in the [REDACTED] processors within the [REDACTED] Accused Products. See CX-1208C; HT 1409:6-1411:23 (“Q. And if we look at the schematic at the bottom of this figure here from CX-1208C, that’s a ring oscillator; right? A. Under the judge’s constructions, yes, I agree.”). Ring oscillators in the Qualcomm [REDACTED] processor are used in the [REDACTED] Accused Products. See CX-1220C at LGE800ITC0309550 [REDACTED]

CX-619C at [REDACTED]

[REDACTED] HT 452:22-453:21; 431:3-16; CDX-5C.26; CDX-5C.08. Similarly, the [REDACTED] products using the [REDACTED] chips contain ring oscillators. See CX-658C at QTPL-0022840; CX-658C at QTPL-0022890; RDX-4.42C; HT 1147:13-1148:7; RDX-4.61C; HT 1172:2-14; CX-1212C at QTPL-0013833; CX-1214C at QTPL-0001792, QTPL-0001836.

The [REDACTED] products incorporate the [REDACTED] Qualcomm processor. CX-577C [REDACTED] The [REDACTED] is in the same family of processors as the [REDACTED]. See, e.g., RX-545C.0001. It uses the same ring oscillator found in the [REDACTED] Accused Products. Similarly, the [REDACTED] products incorporate the [REDACTED] Qualcomm processor. CX-591C [REDACTED] It uses the same ring oscillator found in the [REDACTED]

Some of the [REDACTED] incorporate the [REDACTED] processor. CX-515C [REDACTED] RDX-4.23C; HT 1135:7-16 [REDACTED] These LG accused products use the same ring oscillators found in the [REDACTED] products. A number of the [REDACTED] products incorporate the [REDACTED] processor, which use the same ring oscillators found in the [REDACTED] products. See RX-727C [REDACTED]

[REDACTED] RX-756C [REDACTED] RX-784C [REDACTED] RX-760C [REDACTED] RX-763C [REDACTED] RX-764C [REDACTED] RX-749C [REDACTED] RX-751C [REDACTED]

Some of the [REDACTED] products incorporate the [REDACTED] processor or the related [REDACTED] from the same family, which use the same ring oscillators found in the [REDACTED] RX-1027C; RDX-4.21C; HT 1133:24-1134:12; CX-658C at QTPL-002809 [REDACTED] CX-659C at QTPL-0023454 [REDACTED] HT 446:6-447:7. Some of the [REDACTED]

[REDACTED] products incorporate the [REDACTED] Qualcomm processor. See RX-723C [REDACTED] RX-725C [REDACTED] RX-737C [REDACTED] RX-726C [REDACTED] The [REDACTED] is in the same family as the [REDACTED] See CX-238 [REDACTED]

[REDACTED] see also RDX-4.42C [REDACTED]

c. *The relevant [REDACTED] processors use ring oscillators to generate a clock signal.*

[REDACTED] designee on the [REDACTED] processors testified that [REDACTED] CX-913C [REDACTED] 104:12-22; 99:20-100:16 [REDACTED] [REDACTED] technical documents confirm this. *See, e.g., JX-37C at [REDACTED]*



Respondents' expert also confirmed that the relevant [REDACTED] PLLs each have [REDACTED] [REDACTED] HT 1200:15-23. Dr. Oklobdzija confirmed that [REDACTED] [REDACTED] disclose that the [REDACTED] HT 519:15-520:4.

Yet, the ALJ failed to consider the undisputed evidence provided by [REDACTED] corporate designee, by both Complainants' and Respondents' experts, and by the [REDACTED] technical documents. This was a clear error.

[REDACTED] Accordingly, the ring oscillators found in the [REDACTED] processor for the [REDACTED] products can similarly be found in the [REDACTED] processor used in these [REDACTED] Accused Products. A number of the [REDACTED] products use either the [REDACTED] processor or the [REDACTED] processor. RX-1033C; RDX-4.26C; HT 1136:3-15 [REDACTED] RX-1033C; RDX-4.26C; HT 1136:3-15CX-515C [REDACTED]

2. The ALJ’s construction of “entire oscillator” in claims 6 and 13 was clearly erroneous, because it incorporated unnecessary and incorrect limitations from the prosecution file history.

The ALJ committed clear error in his claim construction order (Order No. 31) because he incorrectly construed the “entire oscillator” element of claims 6 and 13 based on intrinsic evidence. Thus, the ALJ’s construction of “entire oscillator” should be reversed. Under the correct construction of “entire oscillator,” overwhelming evidence demonstrates that the Accused Products infringe. Thus, if the Commission reverses the ALJ’s claim construction, the Commission may find infringement without need to remand the issue to the ALJ for a determination of infringement under the correct construction.

Claim interpretation is a legal issue that lies exclusively within the province of the Court. *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 372 (1996). To determine the meaning of claim terms, the Court must examine the intrinsic evidence: the claims, specification and file history. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995), *aff’d*, 517 U.S. 370, 116 S. Ct. 1384, 134 L. Ed. 2d 577 (1996); *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). The Court should begin the claim construction process by reviewing the claims. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*) (“It is a ‘bedrock principle’ of patent law that ‘the claims of a patent define the invention to which the patentee is entitled the right to exclude.’”) (citation omitted). Claim terms are “generally given their ordinary and customary meaning,” which is “the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, *i.e.*, as of the effective filing date of the patent application.” *Id.* at 1312-13 (citations omitted).

Claim terms are not be construed in a vacuum, “but in the context of the entire patent, including the specification.” *Phillips*, at 1313. Therefore, “claims ‘must be read in view of the specification, of which they are a part.’” *Id.* at 1315 (citing *Markman*, 52 F.3d at 979). “[T]he specification ‘is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.’” *Id.* (citing *Vitronics*, 90 F.3d at 1582).

While claim limitations must be construed in light of the specification and prosecution history, it is improper to import limitations into the claims where such limitations are not present in the language of the claim itself. *Phillips*, 415 F.3d at 1323. A difference exists between construing a term appearing in a claim versus adding a limitation that does not appear in the claim in the first instance. The former is permissible, the latter is forbidden. *See, e.g., Interactive Gift Express, Inc. v. Compuserve, Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001) (“in looking to the specification to construe claim terms, care must be taken to avoid reading ‘limitations appearing in the specification . . . into [the] claims’”) (citations omitted); *Burke, Inc. v. Bruno Indep. Living Aids, Inc.*, 183 F.3d 1334, 1340 (Fed. Cir. 1999) (“Consistent with the principle that the patented invention is defined by the claims, we have often held that limitations cannot be read into the claims from the specification or the prosecution history”).

Although the specification may identify certain preferred embodiments, references to preferred embodiments are not claim limitations. *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1327 (Fed. Cir. 2002) (“the number of embodiments disclosed in the specification is not determinative of the meaning of disputed claim terms”); *DSW, Inc. v. Shoe Pavilion, Inc.*, 537 F.3d 1342, 1348 (Fed. Cir. 2008) (“[W]hen claim language is broader than the preferred embodiment, it is well-settled that claims are not to be confined to that embodiment.”).

Here, the intrinsic evidence supports the following construction of the “entire oscillator” elements of claims 6 and 13, which the ALJ *should* have adopted:

- ❖ *An oscillator that is located entirely on the same semiconductor substrate as the central processing unit*

The ALJ’s construction of “entire oscillator,” set out below, incorrectly imported limitations, bolded and underlined, from the file history:

- ❖ *An oscillator that is located entirely on the same semiconductor substrate as the central processing unit **and does not rely on a control signal or an external crystal/clock generator to generate a clock signal***

See Order No. 31 at 37-41. The file history did not support the addition of the underlined limitations.¹⁵

a. *The plain language of the '336 claims supports Complainants' construction of "entire oscillator."*

Complainants' construction of the "entire" phrases – a CPU/system clock **that is located entirely on the same semiconductor substrate as the central processing unit** – is consistent with the plain language of the claims of the '336 patent. Claims 6 and 13 simply recite "an entire oscillator" as a system clock that is "disposed upon [the same] integrated circuit substrate" as the CPU. Nothing in this language suggests the CPU/system clock can never use a "control signal" or an "external crystal/clock generator" – the improper limitations the ALJ added. Rather, the claims simply make clear that the "entire oscillator" – the CPU/system clock – must be on the same silicon chip as the CPU.

b. *The specification also supports Complainants' construction of "entire oscillator."*

The '336 patent's specification fully supports Complainants' construction of "entire oscillator." It does *not* support the additional limitations the ALJ included. The patent states that the CPU/system clock "is the familiar 'ring oscillator' . . . fabricated on the same silicon chip as the rest of the microprocessor." '336 16:56-58; *see also* Figs. 17, 18. Because the on-chip system clock/"entire oscillator" is fabricated of transistors on the same substrate as the rest of the microprocessor, the transistors of the system clock and the CPU will be similarly affected by variations in semiconductor the fabrication process. *Id.* at 17:2-10. Thus, for example, "if the processing of a particular die is not good resulting in slow transistors," the transistors of both the CPU and the on-chip system clock (the "entire oscillator") will operate slower than normal. *Id.*

¹⁵ In response to arguments by Respondent HTC to add the bolded and underlined limitations in a parallel case involving the '336 patent in the Northern District of California, Judge Paul S. Grewal declined to include the limitation "does not rely on a control signal." See Exh. 1 (Order Re: Emergency Motion for Addendum to Jury Instructions).

Nothing in the '336 specification suggests that the ring oscillator/system clock/"entire oscillator" cannot be used in conjunction with *additional* components such as a "control signal" or an "external crystal/clock generator." Respondents have asserted that the '336 specification disclaims any use of an external crystal clock to "control" the *frequency* of the on-chip ring oscillator/system clock/"entire oscillator." This significantly mischaracterizes the specification, which merely teaches that the *system clock* that clocks the CPU must be *on the same chip* as the CPU. The specification says nothing to indicate that the "system clock/"entire oscillator"/system clock" cannot refer to an external crystal *as a reference*, as in a PLL.

As described above, a typical PLL uses an external crystal *as a reference* – like a speed limit sign or a metronome – to adjust the frequency of the on-chip ring oscillator clock. The ring oscillator generates the clock signal; the external crystal is merely used to adjust its frequency. The addition of PLL circuitry does not conflict with the patent's teaching that the CPU should be clocked by an "entire oscillator" (*i.e.*, a ring oscillator) that is on the same chip as the CPU – thus enabling both components to vary "in the same way as a function of parameter variation *in one or more* [semiconductor] *fabrication or operational* [*i.e.*, voltage and temperature] parameters associated with said integrated circuit substrate." *See* JXM-1 ('336 patent), claim 6.

c. The file history supports Complainants' construction of "entire oscillator."

The file history supports Complainants' construction of "entire oscillator." The ALJ relied on the two references (Magar and Sheets) to find – incorrectly – that the patent applicants disclaimed any use of a control signal or an external crystal/clock generator to generate a clock signal. However, those references lacked *any* on-chip oscillator. They relied on an external oscillator to clock the CPU – exactly as the '336 patent described the prior art. JXM-1; JXM-15 (Magar); RXM-21 (Sheets). Thus, the ALJ's addition of limitations based on the file history's discussion of Magar and Sheets was clearly erroneous.

The applicants added the word "entire" during prosecution to distinguish Magar because the CPU clock for the Magar chip came from an oscillating signal *from an external crystal*:

Magar's clock generator relies on an external crystal connected to terminals X1 and X2 to oscillate, as is conventional in microprocessor designs. It is not an entire oscillator in itself.

CXM-0011 (2/10/98 Amendment) at 3. Thus, the applicants observed that the "entire oscillator" of the '336 invention needed to be on the same chip as the CPU – unlike Magar. This comports with the '336 patent's claims and specification: the ring oscillator clock is on the same die as the CPU.

This cannot possibly constitute a "clear disavowal" of claim scope, because the Magar reference was entirely different from the '336 invention, and was instead identical to prior art specifically discussed in the '336 patent. The "disavowal" doctrine is a rule of claim construction that is frequently invoked but rarely applicable. The doctrine only applies where the disavowal is "clear and unmistakable." *See Cordis Corp. v. Medtronic AVE, Inc.*, 511 F.3d 1157, 1177 (Fed Cir. 2008) ("alleged disavowing actions or statements made during prosecution [must] be both clear and unmistakable").

i. The file history does not support the ALJ's improper importation of the phrase "and does not rely on . . . an external crystal/clock generator to generate a clock signal."

In Order No. 31, the ALJ latched onto a single isolated phrase in the file history – "does not utilize external components" – to find that the on-chip "entire oscillator" cannot "rely on an external crystal/clock generator to generate a clock signal." *See* Order No. 31 at 39. This mischaracterizes the file history – especially to the extent the ALJ and Respondents now also argue that "rely on" now means that the "entire oscillator" cannot be associated with an external crystal/clock generator for *any* purpose. The applicants never disclaimed the use of an external crystal/clock generator as a *reference* – as in a PLL. Rather, they distinguished the '336 invention – which has an oscillator entirely on the same silicon chip as the CPU – from prior art, in which an off-chip crystal oscillator *creates* the clock signal for the CPU.

The ALJ's assertion that the entire oscillator can never "utilize external components" is wrong. *See* Order No. 31 at 39. First, the Magar reference in the file history teaches the use of

an off-chip crystal oscillator to generate the clock signal actually used by the CPU of the microprocessor. During prosecution, the patent applicants explained this significant difference between Magar – which uses an *off-chip* crystal to create the CPU’s clock signal – and the ’336 invention which includes an *on-chip* ring oscillator to generate the CPU’s clock signal:

In making the rejection based on Magar, the examiner appears to be confusing the multiple uses and meanings of the technical term “clock.” A clock is simply an electrical pulse relative to which events take place. **Conventionally, a CPU is driven by a clock that is generated by [an off-chip] crystal. The crystal might be connected directly to two pins on the CPU, as in Magar,** and be caused to oscillate by circuitry contained in the CPU with the aid of possibly other external components. . .

The present invention is unique in that it applies, and can only apply, in the circumstance where the oscillator or variable speed clock is fabricated on the same substrate as the driven device. . . Thus in this example, the user designs the ring oscillator (clock) to oscillate at a frequency appropriate for the driven device when both the oscillator and the device are under specified fabrication and environmental parameters. . .

JXM-18 (7/1997 Amendment) at 4-5.

The reexamination portion of the prosecution history confirms this:

[Magar’s] CLOCK GEN circuitry, however, has crystal oscillator inputs X1 and X2. This leads to the supposition that CLOCK GEN is not a resonator itself, but rather circuitry that amplifies, filters or otherwise prepares the crystal resonator output for use as a CPU clock.

CXM-21 (Reexam. File History) at 9-10.

Thus, Magar differed from the claimed invention because it disclosed no on-chip oscillator. Rather, an off-chip crystal oscillator generated the actual CPU clock for the microprocessor in Magar. The applicants’ discussion of Magar had *nothing* to do with whether the on-chip “entire oscillator” of the invention could be used in a PLL that uses an external crystal as a reference signal.

The portion of the file history that the ALJ cites in Order No. 31 supports this same conclusion. In describing the oscillator/clock 430 of the ’336 invention, the applicants explained:

It is an oscillator in that **it oscillates without external components (unlike the Magar reference).** *An example of such an oscillator circuit which does not utilize external components* is given in Fig. 18 of the present application.

JXM-0016 (2/1998 Amendment) at 4; *see also* Order No. 31 at 37-38. By this statement, the applicants were completely consistent with everything else they said about the Magar reference. In Magar, the oscillation used to create a clock signal for the CPU came from the external crystal oscillator. But with the '336 invention, the oscillator/clock for the CPU is on the same chip as the CPU. The applicants' statement – “does not utilize external components” – was substantially mischaracterized by the ALJ. The file history does *not* teach that external components can never be used for any purpose. It simply teaches that the components needed to *generate* an oscillating clock signal must be on the same silicon chip as the CPU.

Respondents will undoubtedly argue that the applicants distinguished their invention from the prior art on the basis that the on-chip oscillator of the invention can never “use” or “rely on” an external crystal or frequency generator for any purpose. Again, this is manifestly incorrect: The patent applicants observed that the *only* oscillator disclosed in Magar to *generate* a clock signal was the external crystal – there was no on-chip oscillator. Applicants confirmed this when they added the word “entire” to modify the CPU/system clock in each of the claims:

[T]he independent claims have been rewritten to specify that the **entire** ring oscillator variable speed system clock, variable speed clock or oscillator be provided in the integrated circuit, in order to sharpen the distinction over the prior art . . . [T]he prior art circuits **require** an external crystal . . .

Magar's clock generator relies on an external crystal connected to terminals X1 and X2 **to oscillate**, as is conventional in microprocessor designs. It is not an entire oscillator in itself.

JXM-16 (2/1998 Amendment) at 3. The applicants correctly observed that Magar “requires” an external crystal to oscillate and generate a clock signal. *Id.* at 4 (Magar “*requires* an external crystal”; Magar's “clock gen” block “lacks the crystal or external generator that it *requires*”); *Id.* at 5 (Magar “*requires* an external crystal or external frequency generator”).

Thus, the file history is clear that the patent applicants made a single critical distinction between Magar (and similar prior references) and the '336 invention: the oscillator that *generates* the CPU clock in Magar is an off-chip crystal, while the oscillator that *generates* the CPU clock in the '336 invention is an on-chip ring oscillator. On this record, there can be no

“disavowal” that is “clear and unmistakable.” *See Cordis*, 511 F.3d at 1177. The Commission should therefore reverse the ALJ’s construction of “entire oscillator.”

ii. The file history does not support the ALJ’s improper importation of the phrase “and does not rely on a control signal . . . to generate a clock signal.”

The ALJ also found – incorrectly – that the applicants disclaimed all use of “control signals” for the “entire oscillator,” based on their distinction of the Sheets reference. Order No. 31 at 39-40. The Commission should reverse the ALJ’s improper importation of a limitation that prohibits any use of a “control signal.”

The ALJ’s flawed analysis on this point is readily apparent from the only quotation he includes in his analysis regarding Sheets. *See* Order No. 31 at 39. In the passage quoted by the ALJ, the applicants merely observed that *Sheets lacked any on-chip oscillator*. Sheets instead provided “control information” – in the form of a “**digital word**” – to an **external clock**:

The present invention does not similarly rely upon provision of frequency control information to an **external clock**, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. . . . Sheets’ system for providing clock control signals to an **external clock** is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.

JXM-17 (4/1996 Amendment) at 8; *see also* RXM-21 (Sheets) at 2:54-68 (“Microprocessor 101 . . . writes a **digital word** . . . via data bus 104 to VCO 102”).¹⁶

In a subsequent amendment, the applicants noted that the Sheets clock “*required*” a “**digital word**” or “**command input**.” By contrast, in the ’336 invention, “both the variable speed clock and the microprocessor *are fabricated together in the same integrated circuit*. No command input is *necessary* to change the clock frequency.” JXM-21 (1/1997 Amendment) at 4.

¹⁶ The applicants also explained that Sheets would not meet the claims even if the Sheets clock were located on the same integrated circuit as the microprocessor (which it was not):

Moreover, the VCO 12 clearly is not comprised of transistors having operating characteristics disposed to vary similarly to those of transistors within the microprocessor 101. Rather, the VCO 12 is seen to be comprised of an LC oscillator (col. 3, line 58 and FIG. 6), which clearly is not adapted to mimic variation in the speed of transistors within the microprocessor 101.

JXM-17 (4/1996 Amendment) at 9.

Thus, the applicants distinguished Sheets on two bases: (1) unlike the '336 invention, Sheets lacked an on-chip clock/oscillator; and (2) the off-chip clock in Sheets *required* a “digital word”/“command input.” These distinctions do not come close to constituting a disclaimer of any “control signal” for any purpose. Indeed, the analog voltage and/or current supplied to a ring oscillator in a PLL is nothing like the “digital command word” in Sheets. For example, while a ring oscillator needs power to oscillate (*i.e.*, analog voltage/current), it does not have the ability to accept and process a “digital command word” – nor could it be “*required*” to do so.

Disavowal requires “clear and unmistakable” statements or actions. *See Cordis*, 511 F.3d at 1177 (Fed Cir. 2008) (“alleged disavowing actions or statements made during prosecution [must] be both clear and unmistakable”). Here, the applicants did not clearly and unmistakably disavow the use of a “control signal” for *any* purpose. Moreover, in the parallel action in the Northern District of California, Judge Grewal specifically declined to adopt Respondent HTC’s request to include “does not rely on a control signal” in the construction of “entire oscillator.” *See* Exh. 1 (Order Re: Emergency Motion for Addendum to Jury Instructions), and Exh. 2 (Order Granting Emergency Motion for Clarification of Order on Addendum to Jury Instructions).

Accordingly, Complainants respectfully ask the Commission to reject the ALJ’s improper importation into the construction of “entire oscillator” the phrase: “does not rely on a control signal or an external crystal/clock generator to generate a clock signal.” Instead, the Commission should adopt the correct construction of “entire oscillator”: “**an oscillator that is located entirely on the same semiconductor substrate as the central processing unit.**”

d. *The Accused Products satisfy the “entire oscillator” element under the correct construction of that term.*

Overwhelming evidence establishes that the Accused Products include ring oscillators “located entirely on the same semiconductor substrate as the central processing unit.” *See* IV.A.1 (above). Thus, the Accused Products satisfy the “entire oscillator” limitation under the correct construction of that term.

3. The Accused Products include the “entire oscillator” limitation even under the ALJ’s erroneous construction, but the ALJ committed clear error by relying upon a *different* claim construction to find noninfringement.

As discussed above, the ALJ erred by incorrectly construing “entire oscillator.” However, Complainants presented substantial evidence at trial to prove that the Accused Products infringed claims 6 and 13, even under the ALJ’s erroneous construction. However, following the hearing, the ALJ mischaracterized and further changed the already incorrect construction of “entire oscillator” in two different ways.

a. *The ALJ ignored his own claim construction’s plain English syntax to find that the “entire oscillator” cannot use a “control signal” for any purpose.*

The ALJ mischaracterized his own incorrect construction of “entire oscillator” to suggest that a “control signal” cannot be used for *any* purpose, as opposed to not being relied upon “to generate a clock signal.” The ALJ had construed “entire oscillator” as:

An oscillator that is located entirely on the same semiconductor substrate as the central processing unit and does not rely on a control signal or an external crystal/clock generator to generate a clock signal.”

Order No. 31 at 41. Under this construction: (1) the “entire oscillator” cannot “rely on a control signal . . . to generate a clock signal;” and (2) the “entire oscillator” cannot “rely on . . . an external crystal/clock generator to generate a clock signal.” But the ALJ ignored his claim construction’s syntax, finding: “There are two elements to this construction: **first, the oscillator does not rely on a control signal [presumably, for *any* purpose]**, and second, the oscillator does not rely on an external crystal/clock generator to generate a clock signal.” ID at 124. Thus, the ALJ improperly divorced “does not rely on a control signal” from “to generate a clock signal.” This, in and of itself, constitutes clear legal error that warrants review of the ID.

b. *The ALJ failed to apply his construction of “entire oscillator” by changing “to generate a clock signal” to mean “to adjust the frequency of a clock signal.”*

According to the natural English language meaning of the ALJ’s incorrect claim construction, Complainants presented substantial evidence at trial to prove that the Accused

Products infringed claims 6 and 13, *even under the erroneous construction*. Complainants showed that each of the Accused Products has a ring oscillator that “generates a clock signal” without relying on any “control signal” or “external crystal/clock generator.” For purposes of this Petition for Review, it is not necessary to burden the Commission with that evidence, which is discussed in detail in Complainants’ post-hearing briefing. Complainants can review the evidence of infringement – even under the ALJ’s incorrect construction of “entire oscillator” – if the Commission grants review of the ID.

However, *the ALJ did not even apply his own construction of “entire oscillator.”* Rather, he ignored the fact that the Accused Products do not “rely on a control signal or an external crystal/clock generator **to generate a clock signal.**” Instead, the ALJ applied a *different* construction for “entire oscillator” from the one he adopted in Order No. 31, which if expressly defined would be:

an oscillator that is located entirely on the same substrate as the central processing unit and does not rely a control signal or an external crystal/clock generator to *set or adjust the frequency* of a clock signal

Worse, the ALJ did not appreciate that he was applying a different construction for “entire oscillator.” Instead, he mistakenly equated the concept of “frequency adjustment” with “clock generation.” A few quotations from the ID opinion demonstrate the ALJ’s application of this new construction – which for the first time prohibits *any* adjustment to clock frequency:

- “Dr. Subramanian, [REDACTED] all testified that the PLLs in the Accused Products required, and thus rely on, a control signal *to determine the* generated clock *frequency* signal.” ID at 119.
- “So the PLL *controls the frequency* of that VCO or ICO and *adjusts it to match the reference frequency.*” ID at 119.
- “[Dr. Oklobdzija] affirms that a PLL has circuitry that is used *to set the frequency* of a VCO to a multiple of another oscillator frequency functioning as a reference clock.” ID at 119.
- “[Dr. Oklobdzija] testified that, *to set the output frequency*, the PLL compares the frequency of the VCO with the external reference frequency, and based on the difference, the PLL generates a voltage that controls the frequency of the VCO.” ID at 119-120.
- “[T]he evidence shows that none of the Accused Products meet any of the ‘entire’ limitations of the asserted claims, because *the frequencies* of the oscillators in the

Accused Products *are fixed by external crystals/clock generators as well as internally by the PLLs.*” ID at 194.

Thus, the ALJ repeatedly (and incorrectly) stated that the Accused Products do not infringe because they use a control signal or an external crystal/clock generator **to set or adjust the frequency** of the clock signal – **not** to “*generate* a clock signal,” which was the ordered construction.¹⁷ But equating “setting a clock’s frequency” with “generating a clock signal” is fundamentally incorrect. Frequency is a *characteristic* of a clock signal – it is *not* the same as a clock signal, let alone “generating a clock signal.” In fact, Respondents’ expert provided a detailed explanation of this concept:

So we’ll go to RDXM-1-8. And this shows a hypothetical clock signal, and as was pointed out earlier, a clock signal is a signal that is, essentially, a periodic signal, so it tends to have regularity in its period. If I were to look as a function of time, I will see these pulses coming at a regular interval spaced out over time.

And it tends to oscillate between two levels, which I’ll call zero and one. And zero just means a very low voltage, and one means a high voltage, and it’s essentially going back and forth between them. Now, you’ve, therefore, seen – I’ve already introduced one idea of clocks, and that is **clocks tend to have a certain frequency.**

And so we could figure out the **frequency** by counting how many times it oscillates between zero and one in a given second, and that would be called its frequency in hertz, and that’s where the term comes from. **So that’s one characteristic of a clock.**

Now, clocks can have multiple – **you can design clocks to run at different frequencies.** So, for example, you can have a clock running at a low frequency, as is shown on the top of RDXM-1-9, and **a lower frequency means its fewer pulses per second.**

Or we could design it to run at a **higher frequency**, such as the one shown on the bottom of RDXM-1-9, and **this is oscillating more at more pulses per second.** So that’s the idea of **frequency.**

¹⁷ The ALJ bases his erroneous conclusion on Respondents’ deeply flawed analysis in their post-hearing briefing:

[T]he processes of setting the frequency of a clock signal and generating a clock signal are inseparable, because a clock signal must have a frequency, since its sole purpose is to provide a frequency for timing the operations of devices. . . . This periodicity is the frequency of the clock signal. In order for a clock signal to carry out its objective, it must have frequency, which the PLL circuitry sets in reaction to a reference signal from an external crystal or clock generator.
ID at 121.

Tutorial Tr. 35:8-36:15 (Subramanian). Dr. Subramanian explained what is self-evident: frequency is *not* the same as a clock signal; rather, frequency is one *characteristic* of a clock signal. Nor does setting a frequency equate to generating a clock signal. As Dr. Subramanian explained, the same clock signal can have a low frequency or a high frequency; its frequency simply characterizes how rapidly the clock signal pulses. *Id.*

Just because a clock signal has a frequency or “periodicity” does not mean that “setting the frequency of a clock signal and generating a clock signal are inseparable.” The clock signal and its frequency are distinct concepts. Once a clock signal has been generated, its frequency can be changed. The ALJ initially recognized this concept during his examination of Complainants’ expert:

- Q. As I understand it, there’s something else that’s generating the frequency to begin with.
- A. Right.
- Q. And the control signal, rather than generating that frequency, it’s regulating it.
- A. Very correct.
- Q. Is that understanding correct?
- A. Very correct.
- Q. I have no further questions. Thank you.
- A. Let me just clarify the answer. You cannot control something that is not generated. Let’s say if a ring oscillator is dead, it doesn’t generate any frequency, there’s no point of regulating it, because it’s not generating. So you can regulate the traffic when there is traffic, but when there is no traffic, what is the point of regulating it? Basically, that’s my analogy. So it has to generate first before I can regulate it.
- Q. But my question is, what does the – the control signal itself is not doing the generating.
- A. The control signal regulates. It doesn’t generate. And you are very correct in the terms that you used for that.

HT 1092:17-1093:19 (Oklobdzija).

The ’336 patent specification and claims themselves also make apparent the difference between a **clock signal** and its **frequency**. For example:

The ring oscillator 430 is useful as a **system clock** . . . because **its performance** tracks the parameters which similarly affect all other transistors on the same silicon die.

'336 at 16:63-67. In other words, the “performance” of the clock – *i.e.*, its speed or frequency – is *not* the same as the clock itself: its performance (frequency) changes, because it “tracks the parameters which similarly affect all other transistors on the same silicon die.”

Similarly, claim 6 discusses “**an entire oscillator**” that “clock[s] said central processing unit *at a clock rate.*” Plainly, the clock (*i.e.*, the entire oscillator) is not the same as its “clock rate” (*i.e.*, its frequency), which is a *characteristic* of the clock. Further, the “clock rate” in claim 6 has the ability to “vary” based on changes in “one or more fabrication or operational parameters.” Obviously, the identity and source of the clock itself – the “entire oscillator” – does not change. By contrast, the “clock rate” (frequency) – which is a *characteristic* of the entire oscillator – can vary based on conditions.

To find infringement, the ALJ retreated from the simple fact that the *generation* of a clock signal and the *regulation* of its frequency are two distinct concepts. This is also at odds with the conclusion of Judge Paul Grewal, in a parallel case in the Northern District of California, in which he specifically declined to equate “clock generation” with “frequency control,” despite Respondent HTC’s invitation for him to rule that the two were indistinguishable. *See* Exh. 3 (Order re: HTC’s Motions for Summary Judgment of Non-Infringement and No Willfulness).

Equating “clock signal” and “frequency of the clock signal” is just plain wrong. This is clear error that warrants review of the ID.

B. The ALJ Clearly Erred by Failing to Apply the Actual Claim Language of Claims 6 and 13, Which Should Have Resulted in a Finding that the Accused Products Satisfy the “Varying” Limitations as a Result of Binning.

The ALJ committed clear error by failing to apply the plain language of claims 6 and 13, under which a product satisfies the “varying” limitation if the processing frequency of the CPU and the clock rate of the entire oscillator “vary . . . in the same way as a function of parameter variation **in one or more fabrication** or operational **parameters.**” In other words, the ALJ failed to properly consider whether the CPU and clock rate of the oscillator vary in the same way due strictly to their fabrication process, regardless of operational parameters.

Undisputed evidence – including testimony from both sides’ experts – establishes that the transistors on the same microprocessor chips in the Accused Products vary in the same way as a result of their semiconductor *fabrication*. Both experts testified that microprocessor manufacturers exploit process variation by sorting chips based on speed, or “binning” them. This enables the sale of faster chips for a premium, and permits manufacturers to sell, rather than discard, slower chips: they run at lower frequencies, and are sold at a lower price point.

“Varying” based on differences in semiconductor fabrication does *not* result in changes in the frequency or the clock rate of the “entire oscillator” *during operation* – nor do claims 6 and 13 require operational varying. Rather, “varying” based on fabrication is a permanent characteristic of different chips in the same fabrication batch: some identically designed chips are simply faster than others.

These fabrication differences have nothing to do with frequency variation *during operation* of a single chip. The ALJ’s extensive analysis of Respondents’ operational testing evidence is entirely irrelevant to whether the Accused Products meet the “varying” limitations of claims 6 and 13. Rather, undisputed evidence about “binning” proves “varying” due to fabrication differences. Thus, the Accused Products satisfy the “varying” limitation of claims 6 and 13. The ALJ’s failure to recognize this fact based on undisputed evidence and under the plain language of claims 6 and 13 constitutes clear error that warrants reversal.

- 1. Both sides’ experts agree that the “entire oscillators” and CPUs of all products “vary together” with variations in the semiconductor fabrication process, which indisputably satisfies the “varying” of claims 6 and 13.**

Undisputed evidence at trial proved that the Accused Products satisfy the “varying” limitations due to variations in chip semiconductor “fabrication” or “process.” By itself, this satisfies the “varying” limitations of claims 6 and 13, as discussed above.

Complainants’ expert Dr. Oklobzija testified that variations in semiconductor fabrication or processing lead to variations in performance that similarly affect all transistors on a chip. For

additional support, Dr. Oklobdzija cited a book chapter authored by Boning and Nassif, world-renowned experts on the subject from MIT and IBM, respectively:

Variation is the deviation from intended or designed values for a structure or circuit parameter of concern. The electrical performance of microprocessors or other integrated circuits are impacted by two sources of variation. *Environmental factors* arise during the operation of a circuit, and include variations in power supply, switching activity and temperature of the chip or across the chip. *Physical factors* during manufacture result in structural device and interconnect variations that are essentially permanent. These variations arise due to processing and masking limitations, and result in random or spatially varying deviations from designed parameter values.

CX-154 at TPL853_02927444 (emphasis in original); HT 416:18-418:2; *see also* CDX-5C.39.

As discussed in the excerpt, the “[e]nvironmental factors” like “power supply” (voltage) and “temperature” arise “*during the operation of the chip.*” By contrast, “[p]hysical factors” relate to variations in semiconductor processing or manufacture that are “*essentially permanent,*” because they are set at the factory.

Respondents’ expert Dr. Subramanian repeatedly testified that the microprocessor chips in the Accused Products do, in fact, vary with variations in semiconductor processing:

In the tutorial, and here again I will point out that it is widely accepted that process can have variability, which can affect performance. Now, what is process? I’ve been working in process for a large part of my career. Process is the method by which we fabricate these systems. And it turns out the *fabrication is never perfectly set up*. In other words, if I look at 100 different wafers and look at 100 different integrated circuits on those wafers, *they won’t all be exactly the same, even though they are nominally designed the same.*

And one of the consequences of that is, *the maximum achievable performance for one integrated circuit might be 100 megahertz. . . Whereas another nominally very similar processor, just because of the variations in the process, might only be able to run at 50 megahertz.*

HT 1122:1-1123:7; *see also* RDX-4.10. Thus, in this example, Dr. Subramanian testified that variations in process could result in performance differences of 200% (50 MHz versus 100 MHz).

As Boning and Nassif explained, these variations are “physical factors” that are “essentially permanent” because they are set at the factory. CX-154 at TPL853_02927444; CDX-5C.39.

As a result of these permanent variations that are fixed in the chip at the factory, Dr. Subramanian also explained that the industry engages in a common practice called “binning”:

We acknowledge that when parts are made, *when chips are manufactured, chip to chip there can be differences. There's no disagreement between Dr. Oklobdzija and me on that point.*

. . . I used to work in the memory industry. *Binning is standard practice. So we perform binning.*

And what does binning mean? We will take all the chips that we make, and we use a giant tester, a high-precision tester, to test what's the maximum frequency capability, or at least some indicator thereof, of a given chip. So I might find one chip that can run at a gigahertz and another chip that can run at 1.2 gigahertz. . .

And this is when we say, okay, this is a 1-gigahertz chip, this is a 1.2-gigahertz chip. I'm going to sell this one for \$200 and this one for \$100, because *if they run at different speeds you can sell them for different prices. That is binning, where you bin them based on their performance.*

HT 1263:23-1265:18. Dr. Oklobdzija's explanation of binning and process variations was entirely consistent. *See, e.g.,* HT 296:10-301:22; 494:20-495:6. According to Dr. Subramanian, if process conditions "dictate that the maximum achievable performance has dropped, *everything will drop: both the clock and therefore the operation of the CPU.*" HT 1121:18-25. In other words, all transistors on the chip – for both the "entire oscillator" and the CPU – are similarly affected.

Drs. Subramanian and Oklobdzija (and Boning and Nassif) all agree that there are significant variations that are permanently fixed into microprocessor chips at the factory as a result of process variations. Typically, such variations can be on the order of 20% (1 GHz versus 1.2 GHz), or even as much as 200% (50 MHz vs. 100 MHz), according to Dr. Subramanian. As a result, manufacturers can sell "faster" chips for a higher price, and "slower" chips at a lower price. Even though the chips have PLLs that attempt to control a chip's frequency *during operation*, Dr. Subramanian admitted that process differences from "chip to chip" occur at the factory, which permits chips "that are nominally designed the same" to be sold at different prices to run at different speeds. HT 1122:1-1123:7; 1263:23-1265:18 ("[I]f they run at different speeds you can sell them for different prices. That is binning, where you bin them based on their performance.").

Thus, it is undisputed that chips in the Accused Products have process variations that are fixed at the factory, so that the CPUs and "entire oscillators" on the same chip, together, are

faster than the CPUs and entire oscillators on other chips with nominally the same design. There can also be no dispute that this process variation – *by itself* – satisfies the “varying” limitation of claims 6 and 13, as discussed above.

It is also undisputed that the clock rate of the “entire oscillator” is always used to clock the CPU. Thus, the processing frequency of the CPU will *always* vary with the clock rate of the entire oscillator as a function of the fabrication parameters that were fixed in the chip at the factory – parameters that admittedly affect both the “entire oscillator” and the CPU. As a result, there can be no doubt that all Accused Products satisfy the “varying” requirement of claims 6 and 13. The ALJ’s failure to reach this conclusion requires reversal of the ID.

2. The ALJ committed clear error by ignoring the disjunctive “in one or more” language in claims 6 and 13, which only requires “varying” based on semiconductor “fabrication.”

Complainants provided ample evidence that the Accused Products satisfied the “varying” limitations of claims 6 and 13 by processing/fabrication variations *alone* – even if the clock frequencies of the products do *not* vary *during operation* (due to changes in voltage and/or temperature).

The relevant language of claim 6¹⁸ makes this clear¹⁹:

a central processing unit²⁰ disposed upon **an integrated circuit²¹** . . . being constructed of **a first plurality of electronic devices;**

an entire oscillator²² disposed upon **said integrated circuit** . . . being constructed of **a second plurality of electronic devices,**

¹⁸ Claim 13 has identical language for the “varying” limitation.

¹⁹ Complainants have color-coded the relevant language from claim 6, for the Commission’s convenience.

²⁰ Complainants have used blue shading for the CPU and its characteristics in claim 6 above.

²¹ Complainants have used yellow shading to identify the language associated with the integrated circuit substrate or chip in the language quoted above from claim 6.

²² Complainants have used pink shading to identify the “entire oscillator” and its characteristics in the language of claim 6 above.

thus varying²³ the processing frequency of said first plurality of electronic devices [the CPU] and the clock rate of said second plurality of electronic devices [the entire oscillator] in the same way as a function of *parameter variation in one or more fabrication or operational parameters* associated with said integrated circuit substrate, thereby enabling said processing frequency [of the CPU] to track said clock rate [of the entire oscillator] in response to said parameter variation;

JXM-1 ('336 patent), claim 6. The “central processing unit” or “CPU” is composed of a “first plurality of electronic devices,” or transistors. The CPU also has a “processing frequency,” which is the speed at which it runs. A CPU always gets this speed from the system/CPU clock (which, in this case, is the “entire oscillator”).

The “entire oscillator” is a ring oscillator on the same chip (“integrated circuit”) as the CPU. The entire oscillator is constructed of a “second plurality of electronic devices,” or transistors. The entire oscillator also has a “clock rate,” which is the frequency of the clock signal that it provides to the CPU.

The CPU and the entire oscillator are both on the same chip or “integrated circuit substrate.” Because they are on the same chip, the CPU and entire oscillator will experience similar changes with variations in voltage and temperature (during operation), and will be similarly affected by variations in semiconductor fabrication (which creates permanent variations from chip to chip during the manufacturing process). HT 302:9-303:17; 1272:1-3.

Significantly, claims 6 and 13 state that the processing frequency of the CPU and the clock rate of the entire oscillator “vary . . . in the same way as a function of *parameter variation IN ONE OR MORE fabrication OR operational parameters*.” Thus, according to the plain language of claims 6 and 13, *a product can satisfy the “varying” requirement based solely on fabrication variations – even if there is no variation based on operational parameters, like changes in operating temperature and/or voltage.*

²³ Complainants have used green shading to identify above represents language of claim 6 that is associated with how the CPU and entire oscillator “vary . . . in the same way” with variations in fabrication or operational parameters.

The '336 patent's specification specifically identifies parameter variation due to semiconductor fabrication differences – which is set at the factory – and does *not* cause changes to the frequency of the chip *during operation*:

For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor 50 will operate slower than normal. Since the microprocessor 50 ring oscillator clock 430 is made from the same transistors on the same die as the latches and gates, it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.

JXM-1 ('336 patent), 17:2-10.

In the ID, the ALJ recognized that Complainants made this same argument, but then ignored it in his analysis of whether the Accused Products satisfy “varying”:

Complainants claim . . . that it is undisputed that [Accused Products] satisfy the “varying limitations due to variations in chip “fabrication” or “process” . . .

* * *

Thus, argue Complainants, in this example Dr. Subramanian testified that variations in process could result in performance variations of 200 percent (50 megahertz versus 100 megahertz). . . As the authors Boning and Nassif explained, these variations are “physical factors” that are “essentially permanent” because they are set at the factory. . . As a result of these permanent variations that are fixed in the chip at the factory, Dr. Subramanian testified that the industry engages in a common practice called “binning” . . .

* * *

Thus, argue Complainants, it is undisputed that chips in the Accused Products have process variations that are fixed at the factory, and therefore CPUs and clocks of some chips are faster than others with “nominally the same design.” . . . Complainants argue that there can be no dispute that this process variation, by itself, satisfies the “varying” limitations of claims [6 and 13].

ID at 143-145 (reciting Complainants' argument in post-hearing brief).

However, in his analysis regarding whether the Accused Products satisfied the “varying” limitation, the ALJ ignored the disjunctive language of claims 6 and 13 – “in **one or more fabrication or** operational parameters” – which establishes that a product can practice the claims based on parameter variation due to fabrication alone. *See, e.g.*, ID at 189-213 (ALJ's “Findings and Conclusions” re: “varying”). The ALJ's only discussion of “varying” based on “fabrication” parameters appears his “Findings and Conclusions” on page 209 of the ID:

As for Dr. Oklobdzija's assertion that binning is evidence of variations due to manufacturing process, **the Administrative Law Judge concludes that while binning is**

a reflection that variations exist in the performance capabilities of microprocessors (Tr. (Subramanian) at 1264), this does not constitute evidence that any of the Accused Products meet the “varying” limitations of the asserted claims. Dr. Subramanian’s testimony and the testing it was based on empirically demonstrate that the operational frequencies of the chips, no matter their individual differences are fixed. (Tr. (Subramanian) at 1265-66.) Once again, Dr. Oklobdzija and Complainants apply the “varying” limitation in a hermetic fashion as though an oscillator having a power source is the claimed “entire oscillator” and it does not matter that the frequency of the oscillators in the Accused Products are fixed, both internally and externally.

ID at 209. But the ALJ’s conclusion that “binning is a reflection that variations exist in the performance capabilities of microprocessors” *does* prove “varying” based on differences in “fabrication” parameters. Dr. Subramanian’s testing and testimony that the “*operational* frequencies of the chips” are fixed is irrelevant; claims 6 and 13 do not require “varying” based on “operational parameters.” It is enough to show that variations in fabrication parameters cause “varying” of the processing frequency of the CPU and the clock rate of the entire oscillator “in the same way.” As discussed below, undisputed testimony from both sides’ experts proves this.

The ALJ’s failure to even apply the actual language of claims 6 and 13 – “in **ONE OR MORE fabrication OR** operational parameters” – constitutes legal error that requires review and reversal of the ID.

3. The ALJ committed clear error by focusing on the operational parameters affecting the “entire oscillator;” operational parameters are irrelevant to determine infringement based on variation due to fabrication parameters.

Instead of applying the disjunctive language of claims 6 and 13 – “**in one or more fabrication or** operational parameters” – the ID focuses its “varying” analysis on whether the clock frequency of the accused chips changes *during operation*. Varying during operation – based on claimed “operational parameters” of voltage and/or temperature – is irrelevant to Complainants’ Petition for Review on the “varying” limitation; variation based on fabrication satisfies this element, as discussed above in detail.

Failing to grasp this crucial requirement of the claim language, the ID states:

The Administrative Law Judge finds that there is a basic flaw that permeates Complainants’ and Dr. Oklobdzija’s reasoning regarding infringement of the “varying” limitations: it avoids the fact that the “entire” oscillator terms are inextricably tied to the “varying” terms of the claims. . . . As previously discussed and determined, the evidence

shows that none of the Accused Products meet any of the “entire” limitations of the asserted claims, because the frequencies of the oscillators in the Accused Products are fixed by external crystals/clock generators as well as internally by the PLLs.

* * *

Although Complainants do give lip service to the concept of “entire oscillator” in their argument (*see* CBr. At 40-41) ***they leave out the actual operational aspects of the relevant oscillators in the Accused Products, which do not perform in accordance with the “varying” limitations of the asserted claims.***

ID at 194-96. By tying his analysis of “varying” to the “operational aspects of the oscillators in the Accused Products,” the ALJ confirms that he improperly limited his analysis to varying based on “operational parameters,” and improperly ignored variation due to “fabrication.”

The ALJ spends nine pages of the ID discussing Dr. Subramanian’s tests regarding whether the frequency of the Accused Products varies ***during operation*** based on temperature and/or voltage. ID at 196-204. But these tests are utterly irrelevant to “varying” based on semiconductor ***fabrication*** parameters, and the Commission can ignore this entire section of the ID for purposes of this Petition. Similarly irrelevant are jitter (ID at 206), Qualcomm documents regarding PVT (ID at 207-09), and dead band (ID at 211-12). These passages all relate only to ***operational*** variation, which is ***not*** necessary to practice the “varying” limitation of claims 6 and 13.

In its final analysis of “varying,” the ID asserts: “Succinctly put, a part’s processing frequency capability may change with PVT, but its actual speed, or processing frequency, remains constant.” ID at 211. But this statement is dead wrong when it comes to variation as a result of fabrication parameters. According to claims 6 and 13, the ’336 patent’s specification, and even Respondents’ expert, “varying” due to differences in manufacturing occurs from chip to chip – ***not*** within the same chip ***during operation***. *See* JXM-1 (’336 patent) at 17:2-10; HT 1263:23-1265:18 (Subramanian). That is why chip manufacturers can sell faster chips for a higher price than slower chips: the speed at which a “good” chip is set to run is faster than the speed at which a “slow” chip is set to run. HT 1122:1-1123:7, 1263:23-1265:18 (Subramanian); *see also* RDX-4.10. This satisfies the “varying” limitation of claims 6 and 13, and the ID should be reversed on this issue.

C. The ID Committed Clear Errors of Fact and Law in Finding Noninfringement Based on the “External” Second Clock Limitation.

Two pervasive errors underlie the ID’s findings relating to the external second clock limitations. First, in adopting Respondents’ argument, the ID concludes that the first and second clocks are not independent or asynchronous because they share the same reference signal. This finding is irrelevant under the ALJ’s claim construction, which requires either a comparison between the first and second clocks, or a determination of whether the timing control of the first clock is derived from the timing control of the I/O interface. Further, with respect to many accused second clocks in Respondents’ products, the finding is factually inaccurate—the first and second clocks do not share a reference signal.

Second, to find that none of the Accused Products contain an *external* second clock, as required by claims 6 and 13, the ID relies on evidence related to *internal* clocks that applies only to claims 1 and 11. Based on three examples regarding *internal* clocks, the ID finds that Complainants’ evidence is conclusory and insufficient. This finding is clearly erroneous as a matter of fact and law. Not only are examples regarding internal clocks completely irrelevant to the limitations at issue in claims 6 and 13, they are factually erroneous as well. Infringement is a two-step process requiring the construction of claims and the application of the construed claims to the accused products. Because the ID applied only the second clock limitations of claims 1 and 11 to the Accused Products, its finding as to claims 6 and 13 is clearly erroneous as a matter of law.

1. Construction and Overview of the External Second Clock Limitations of Claims 6 and 13

In addition to the “entire oscillator” first clock, claims 6 and 13 require a second clock:

Claim 6	Claim 13
an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip [a] external clock is operative at a frequency independent of a clock frequency of said	an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip [a] external clock is operative at a frequency independent of a clock frequency of said

oscillator and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.	oscillator and further [b] wherein said central processing unit operates asynchronously to said input/output interface.
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JXM-1.

The ALJ adopted the constructions of bolded terms [a] and [b] in these elements:

Term	Construction
[a] (“independent”) external clock is operative at a frequency independent of a clock frequency of said oscillator	an external clock wherein a change in the frequency of either the external clock or oscillator does not affect the frequency of the other
[b] (“asynchronous”) wherein said central processing unit operates asynchronously to said input/output interface	the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them

Order No. 31 [Corrected] (April 18, 2013) at 11, 74.

In a given microprocessor-based system, various off-chip components such as memory, USB, camera, Bluetooth, etc. must interact with the processor. To facilitate this interaction, the claimed invention includes an on-chip input/output interface. However, the off-chip components connected to this I/O interface often operate at a fixed speed that is much slower than the desired speed of the microprocessor. The inventors addressed this by offloading the timing of the microprocessor’s slower input/output interface from the first clock to a second independent clock. This preserves the performance gains achieved through the use of an on-chip first clock:

Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor 50 provides a dual-clock scheme as shown in FIG. 17, with the CPU 70 operating asynchronously to I/O interface 432 forming part of memory controller 118 (FIG. 2) and the I/O interface 432 operating synchronously with the external world of memory and I/O devices.

By decoupling the variable speed of the CPU 70 from the fixed speed of the I/O interface 432, optimum performance can be achieved by each.

JXM-1 ('336 patent) at 17:12-19, 32-34.

While claims 1 and 11 place no limitation on whether the second clock is located on or off the chip, claims 6 and 13 require it to be “off-chip.” None of the claims place any limitation on what type of clock may serve as the claimed second clock. Figure 17 illustrates the use of a fixed crystal 434 as an off-chip second clock for the I/O interface 432. The red box indicates the boundaries of the microprocessor. CDXM-0001.048:

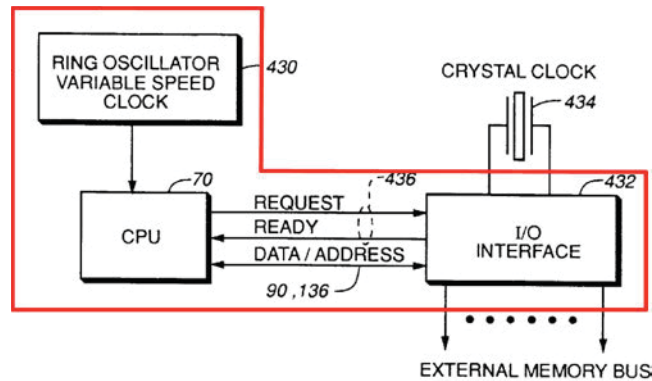


FIG. 17

Complainants accused the clocks associated with various interfaces in Respondents’ products as the claimed second external clocks of claims 6 and 13 including: USB (universal serial bus peripheral interface), CAMIF (camera interface), CSI (camera serial interface), ABE (audio back end interface), SPI (serial peripheral interface bus), I2C (inter-integrated circuit bus), MIPI (mobile industry processor interface for camera or display) and HDMI (high definition multimedia interface for audio and video). *See, e.g.*, CDX-0009C, HT 530:5-542:12; CDX-0030C HT 705:1-710:17, 718:7-21; CDX-0034C, HT 710:18-715:6, 716:20-717:5; CDX-0035C; CDX-0038C; CDX-0039C; CDX-0041C; CDX-0043C; CDX-0046C; CDX-0049C, HT 747:11-749:2; CDX-0050C; CDX-0051C; CDX-0055C, HT 719:14-7:22:10; CDX-0056C; CDX-0059C; CDX-0062C; CDX-0063C; CDX-0064C.

2. The ID Discards the Controlling Claim Construction of “Independent” in Order to Find Noninfringement.

Pursuant to the parties’ agreed-upon claim construction—which the ALJ adopted—an accused second clock is “independent” if “a change in the frequency of either the external clock

[second clock] or oscillator [first clock] does not affect the frequency of the other.” In other words, the relevant question is whether the two clocks are *dependent on each other* for changes in frequency. Unrefuted evidence shows that the two clocks are *not* dependent on each other.

Dr. Oklobdzija confirmed this when he testified that two PLLs that share the same reference clock are nevertheless independent because “they are sourced by different ring oscillators” within those PLLs. HT 1060:23-1061:18.²⁴ The ID cites to no contrary evidence because there is none; the only evidence Respondents presented regarding the “independent” limitation is irrelevant testimony regarding shared reference signals.

The ID did not apply the unrefuted evidence to the proper claim construction, but instead applied a new test. Specifically, it relies on testimony from Respondents’ expert, Dr. Subramanian, that two clocks receiving the same external reference signal cannot be independent. ID at 252. This is wrong for two reasons. First, the basic proposition underlying the argument is false—supplying an upstream reference signal to two clocks does not render them dependent on each other. Second, it incorrectly presupposes that the reference signal generates the clock signal, not the oscillator—essentially the same incorrect argument the ID adopts with respect to the “entire” first clock limitations.

The ID’s inquiry into reference signals is conceptually flawed. Even if it is accepted that (A) the first and second clocks in the Accused Products receive the same reference signal, and (B) a change in the reference signal ultimately results in a change in speed to both the first and second clocks, this arrangement sheds no light on whether the first and second clocks are *dependent on each other*. During Respondents’ *Markman* tutorial Dr. Subramanian compared

²⁴ The ID claims that “Dr. Oklobdzija failed to address the parties’ agreed claim construction” with respect to the external clock element of claims 6 and 13. ID at 245. Not so. At the hearing, Dr. Oklobdzija presented demonstratives with the constructions of “independent” and “asynchronous” and when asked for each term “Did you consider the Court’s construction in connection with this claim term” he responded: “I did, and I agree with it.” CDX-0004.14, 4.18; HT 303:21-304:2, 311:12-313:11.

the PLLs in Respondents' Accused Products to cruise control in a car. RDXM 1-30. This analogy illustrates the flaw in the ID's reasoning here.

When a car is travelling on the road its speed—generated by the engine—responds to environmental conditions, such as hills. The purpose of the cruise control is to cause the engine to adjust its output to match a pre-determined speed. If a car is travelling on the freeway and the driver sets the cruise control to match the posted speed limit of 65, the cruise control will cause the engine to produce more speed when the car starts to slow on an incline and will cause the engine to reduce output when the car speeds up on downhill slopes. In this analogy, the ring oscillator is the engine, the PLL is the cruise control and the speed limit sign is the external reference signal. Changes in environmental conditions, such as temperature or voltage cause the ring oscillator to speed up or slow down. The PLL compensates for these changes in frequency to bring the ring oscillator in line with some multiple of the reference frequency. With respect to the “entire” limitations, the ID and Respondents essentially argue that the speed limit sign and cruise control generate the speed of the car while Complainants argue that it is the engine. But this is irrelevant under the controlling interpretation of “independent.” The proper question under this construction is whether the speed of one car is dependent on the speed of *other cars*.

In other words, when two separate cars are driving through a 65 MPH zone and both make use of cruise control, is it true—pursuant to the ALJ's claim construction—that “a change in the frequency [speed] of either the external clock [second car] or oscillator [first car] does not affect the frequency of the other?” Using the cruise control analogy, it is obvious that the speed of one car using cruise control on the freeway does not affect the speed of another car using cruise control simply because both drivers see a 65 MPH sign. The same is true with respect to the Accused Products—the fact that two PLLs (cruise control) receive the same reference signal (65 MPH sign) does not make the speed of their oscillators (engines) dependent on each other. Accordingly, by failing to apply the controlling construction of “independent,” the ID clearly erred.

The ID’s finding on the external second clock limitations fails conceptually for another reason. Even accepting *arguendo* the proposition that examining whether two PLLs share the same reference signal is relevant under the ALJ’s claim construction, the inquiry bootstraps the same theory the ID advances with respect to the “entire” limitations: that when a ring oscillator is incorporated into a PLL that receives a reference signal, it is the reference signal not the oscillator that generates the resulting clock signal. If it is accepted that the *ring oscillator* generates the clock signal—not the PLL and/or reference signal—it is irrelevant whether either PLL receives a reference signal, much less whether two PLLs receive the same or different reference signals. Accordingly, if the ALJ’s conclusion regarding the “entire” limitations is wrong, the ID’s finding on the external second clock limitations can be rejected without further consideration.

3. The ID’s Finding that Complainants Failed to Offer Evidence Sufficient to Meet Their Burden is Clearly Erroneous.

Based on three discrete examples, the ID discredited *all* of Complainants’ evidence regarding *all* second clocks in *all* of the Accused Products, concluding: “On the whole, with respect to whether *any* of the Accused Products satisfies the ‘independent’ aspect of the ‘second’ and ‘external’ clock limitations, the Administrative Law Judge finds that Dr. Oklobdzija’s testimony *was refuted* by Dr. Subramanian.” ID at 255. Conditioning its ultimate conclusion on these limited examples is clearly erroneous because the examples do not even apply to the unique external clock limitations of claims 6 and 13 and the examples themselves are factually incorrect.

a. Respondents’ Accused Products Meet the “Independent” Limitation of Claims 6 and 13.

The three examples upon which the ID relies relate to (1) the accused LSI chip found solely in Respondent Acer’s Accused Products,²⁵ (2) an accused internal camera interface, and (3)

²⁵ Because Complainants and Acer have reached settlement and moved to terminate the Investigation as to Acer, Complainants do not address the LSI argument in detail.

an accused internal USB interface. As discussed above, these examples deal only with *internal* clocks and have no relation to the *external* camera and USB clocks accused under claims 6 and 13.

Respondents' examples are irrelevant to Complainants' proof with respect to numerous other *external* second clocks that satisfy this claim element. For, Complainants offered expert testimony and underlying documentation showing that various Accused Products have external second clocks originating in HDMI modules. Dr. Oklobdzija's trial slide CDX-0039C sets forth evidence of the "Independent Second Clock: External HDMI" in a number of [REDACTED] phones. See CDX-0039C.03 (emphasis in original) (citing CX-0653C and CX-1323). Excerpts from the product schematics show the relevant clock lines, indicate the source of the external clock signal and show that the device can be connected to external HDMI peripherals via a cable.



Dr. Oklobdzija specifically testified about this evidence. HT 571:22-574:11. In addition, when testifying about other Accused Products, Dr. Oklobdzija offered further testimony of general

applicability regarding external HDMI second clocks, based on his expertise. Of note, he testified that “the clock that HDMI carries is a differential clock,” which is “an external clock that originates from the HDMI device, that could be a display or it could be something else that uses HDMI protocol” and that “since we don’t know what can be connected there, that clock is definitely independent and *has no relationship with the clocks on the chip.*” HT 706:10-707:7. In other words, because devices with HDMI interfaces may be connected to different HDMI peripherals, they must follow the HDMI standard and include external clock connections from those peripherals that are unrelated to the first CPU clock. This evidence stands uncontroverted because Respondents offered no testimony or other evidence regarding HDMI, CSI and other external second clocks that Complainants accused. The ALJ’s failure to consider evidence related to other second clocks is sufficient reason alone to grant review of the ID.

With respect to Qualcomm processors, Respondents rely on documentation and expert testimony for the [REDACTED] phone with a Qualcomm [REDACTED] processor, which they claim to be representative of the remaining accused Qualcomm processors for this claim limitation. According to Respondents and the ID, Dr. Subramanian showed that the clock signals for the [REDACTED] originate from PLLs [REDACTED] [REDACTED] and which receive the same external crystal reference signal. ID at 218-220, 247-249.

However, as the ID’s own citations reveal, with respect to the [REDACTED] Complainants accused only an *internal* camera clock and did not accuse any USB clock on the same device. *See* ID at 218 (citing CDX-0044C.3). Specifically, Complainants’ second clock allegations relating to the [REDACTED] phone are contained in CDX-0044C.3 which identifies a single “Independent Second Clock: Internal Camera” (emphasis in original) and identifies no USB clock. As an *internal* clock, this particular [REDACTED] clock is applicable only to claims 1 and 11,

not claims 6 and 13, which require an *external* second clock.²⁶ Because the ID finds that the Accused Products do not practice the second *external* clock limitation of claims 6 and 13 by examining evidence related only to a different limitation from claims 1 and 11, it is clearly erroneous as a matter of both fact and law.

The ID commits the same error with respect to Accused Products with microprocessors from Samsung and Texas Instruments. It relies on testimony from Dr. Subramanian that the [REDACTED] clocks in the Samsung and Texas Instruments chips originate from PLLs that [REDACTED] receive the same off-chip reference signal. *See* ID at 222-223, 250-251.

Again, Complainants on-chip (internal) clock signals are irrelevant to the off-chip (external) second clock requirements of claims 6 and 13. For example, with respect to Samsung products, Complainants accused an external USB clock originating from a connected peripheral. *See, e.g.*, CDX-0059C.07. As Dr. Oklobdzija testified, this interface's clock signal [REDACTED]

[REDACTED] HT 593:12-20 (discussing RX-0727C). Because the clock signal originates from an unrelated device, it neither depends on the Accused Product's first clock nor receives the same reference signal, as required by the industry standard USB specification. HT 531:9-534:4 (discussing CX-0117, USB specification).

Similarly, with respect to products containing Texas Instruments chips, Complainants accused a number of internal clocks, in addition to external embedded USB clock signals operating in accordance with the USB specification—the same external second clock

²⁶ Complainants also dispute the accuracy of Respondents' claims about this second clock. Dr. Oklobdzija confirmed on redirect that Respondents were addressing a different camera clock than had been asserted in this Investigation. HT 1063:4-1064:13. Moreover, as discussed above, Respondents' argument relies on the fallacy that because two PLLs receive the same reference signal, they cannot be independent. However, because Complainants' petition for review is limited to claims 6 and 13 and the internal clocks that are the subject of the ID are not relevant to those claims, the inaccuracy of Respondents' arguments is irrelevant as well.

Complainants asserted against the Samsung products. *See, e.g.*, CDX-0034C [REDACTED]

[REDACTED] HT 714:1-715:6 [REDACTED]

[REDACTED] CX-0339C, CX-0340C and CX-0034C.06). As discussed above, the internal clocks related to claims 1 and 11 have nothing to do with the external clocks Complainants' accused related to claims 6 and 13. In short, the ID's blanket application of arguments related only to the internal second clocks Complainants accused of practicing claims 1 and 11 to claims 6 and 13, and subsequent failure to independently analyze Respondents' infringement of claims 6 and 13 is clearly erroneous.

Further, the ID explicitly refuses to address Complainants' proof regarding external USB second clocks. It acknowledges: (1) Respondents' argument that Complainants may not rely on external USB connections because the Accused Products are not connected to USB peripherals as imported; and (2) Complainants' citation to *Certain Elec. Devices with Image Processing Sys., Components Thereof, & Associated Software ("Image Processing Sys.")*, Inv. No. 337-TA-724, 2012 WL 3246515 (U.S.I.T.C. Dec. 21, 2011), cited in *In re Certain Video Game Systems & Wireless Controllers & Components Thereof*, Inv. No. 337-TA-770, 2012 WL 3246515, at *10 (U.S.I.T.C. Aug. 31, 2012), which holds that Respondents' argument does not apply to apparatus claims like claims 6 and 13 of the '336 patent. Inexplicably, however, the ID then goes on to state: "Inasmuch as it has been found that there is no infringement by any of the Accused Products, there is no need to address this issue." ID at 253. The ID likewise fails to render a determination with respect to Complainants' inducement claim, which centers on the external USB second clocks described above. Rather than address Complainants' evidence of inducement, the ID simply offers two sentences stating that there can be no indirect infringement because the ALJ found there was no direct infringement. The ID's failure to address Complainants' external USB evidence is clear error.

Finally, the ID faults Complainants for failing to present testing evidence with respect to the second and external clock elements, calling it a "hole in the evidence." ID at 245. This

criticism is particularly puzzling because neither Complainants' expert nor Respondents' expert so much as implied that any testing could have, or should have, been done to determine independence or asynchronicity. Likewise, the ID is silent on what type of testing Complainants supposedly could have performed with respect to these claim elements. The ID's requirement that Complainants use testing in order to carry their burden of proof is clearly erroneous as a matter of law.²⁷

b. Respondents' Accused Products Meet the "Asynchronous" Limitation of Claim 13.

Complainants presented both expert testimony and documentary evidence to show that "the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them." The ID rejects Complainants' expert testimony because the ALJ did not understand it, or as the ID put it: "It does appear, as Respondents argue, that Dr. Oklobdzija was testifying about something else, [sic other than] the phase relationship between the PLL and the external clock. ID at 258. The ID also rejects technical documents confirming

²⁷ See *Liquid Dynamics Corp. v. Vaughan Co., Inc.*, 449 F.3d 1209, 1219 (Fed. Cir. 2006) ("A patentee may prove direct infringement ... by either direct or circumstantial evidence."); *Johns Hopkins Univ. v. CellPro, Inc.*, 152 F.3d 1342, 1349-50, 1356 (Fed. Cir. 1998) (affirming judgment of literal infringement where the district court noted that the plaintiff "could prove infringement without testing the accused cell suspensions" because the defendant's documents showed that a claim limitation was met); *MGM Well Servs., Inc. v. Mega Lift Sys., LLC*, 505 F. Supp. 2d 359, 370 & n.12 (S.D. Tex. 2007) (rejecting an actual-testing requirement and relying on patentee's expert testimony, which was based on the "laws of physics"); *Nielsen v. Alcon, Inc.*, No. 3-08-CV-2239-B-BD, 2011 WL 4529762, at *6 (N.D. Tex. Sept. 2, 2011) ("[A]n expert is not required to perform direct physical testing on an accused device in order to prove infringement.") (citing *Liquid Dynamics*); see also *Amgen Inc. v. Hoffman-La Roche Ltd.*, 580 F.3d 1340, 1385-86 (Fed. Cir. 2009) (finding that patentee "not required to have duplicated [defendant's] actual production process" in order to prove infringement and could rely on documents and testimony); *Martek Biosciences Corp. v. Nutrinova, Inc.*, 579 F.3d 1363, 1372-74 (Fed. Cir. 2009) (finding expert testimony concerning "scientific fact" and literature regarding the corrosive effects of chlorides on stainless steels sufficient to prove infringement without testing); *Water Techs. Corp. v. Calco, Ltd.*, 850 F.2d 660, 667 (Fed. Cir. 1988) (upholding district court's finding of infringement where no testing conducted and district court relied on expert testimony).

that the accused CPUs are asynchronous from the rest of the device. Both findings are clearly erroneous.

The problem with the ID's finding for this claim limitation is similar to the conceptual error committed in relation to the "independent" limitation. With respect to the "asynchronous" limitation, both the claim language and the adopted claim construction involve a comparison of the timing control of the CPU (first clock) to the timing control of the I/O interface (second clock). Neither has *any* requirement involving a reference signal, *or* a comparison between the phase relationship of a reference signal and the first or second clocks. Yet this is the argument the ID adopted from Respondents' briefing. ID at 220-221.

Respondents' argument relies on the faulty assumption that a predictable phase relationship exists between the reference signal and the first/second clock to argue that the first and second clocks must also have such a relationship. Dr. Oklobdzija explained why this is not true: "if there is a predictable phase relationship [between the reference and the first/second clock], there is no error signal, and you don't need PLL; the PLL has no purpose any more." HT 1026:14-1028:8. In other words, it is technically inaccurate to state that a predictable phase relationship exists between the reference signal and a PLL. Hence, the ALJ's (and Respondents') extension of the assumption to say that two PLLs that receive the same reference signal must have the same relationship compounds the error.

Respondents pointed out that Dr. Oklobdzija's offered testimony with respect to a specific PLL from one of the Accused Products. However, Dr. Oklobdzija's testimony discusses universal principles applicable to PLLs, which Dr. Oklobdzija, as one of the foremost experts in microprocessor clocking, well understands. Further, neither Respondents nor the ID can state what the "something else" is that Dr. Oklobdzija's testimony supposedly addressed.

In addition, Complainants presented uncontroverted evidence from the chip manufacturers establishing that the CPU operates asynchronously from the various claimed I/O interfaces. For the Accused Products using [REDACTED] the technical reference manuals unequivocally state: [REDACTED]

They further state that the

²⁸ The Qualcomm chips likewise support the “asynchronous” limitation. For example, the design guidelines document discusses

while the discuss

²⁹ Samsung’s documents confirm that, for the the chip ³⁰

While Respondents and the ID speculate that this technical documentation may not mean the same thing by “asynchronous” as the construed claim, they can offer no suggestion about what else the term could mean in the context of clocking a microprocessor. On the other hand, Dr. Oklobdzija specifically testified that he both agreed with the ALJ’s construction of “asynchronous” and that the technical documentation confirmed that the Accused Products fit within this definition. HT 312:8-313:11 (discussing construction in conjunction with CDX-0004.17), 488:21-489:15 (opining that confirms that first clock is asynchronous from second clocks). For these reasons, the ID’s findings regarding the “asynchronous” limitation are clearly erroneous.

V. CEASE AND DESIST ORDERS

Section 337 authorizes the Commission to issue cease and desist orders as a remedy for violation of Section 337. *See* 19 U.S.C. § 1337(f)(1). The Commission generally issues a cease

²⁸ CX-318C at AMZ_TPL_0040819 CX-321C at AMZ_TPL_00060327
CX-316C at AMZ_TPL_00025320 CX-366C at GARM-N37xx-031361
CX-353C at GARMIN068388

²⁹ CX-663C at QTPL-0047334 CX-653C at QTPL-0010453

³⁰ RX-696C.0440 RX-702C.0308

RX-696C.0440; RX-702C.0308.

and desist order directed to a domestic respondent when a “commercially significant” amount of infringing, imported product is in the United States. See *In re Certain Hardware Logic Emulation Sys. & Components Thereof*, Inv. No. 337-TA-383, U.S.I.T.C. Pub. 3089, Comm’n Op. on Remedy, the Public Interest, and Bonding at 25, 1998 WL 307240 (U.S.I.T.C. Mar. 1998) and *In re Certain Crystalline Cefadroxil Monohydrate*, Inv. No. 337-TA-293, Comm’n Op. on the Issue Under Review, and on Remedy, the Public Interest and Bonding at 37-42, Pub. No. 2391 (U.S.I.T.C. June 1991).

In the ID, the ALJ recommended that the Commission decline to issue any cease and desist orders because Complainants supposed failed to show that Respondents’ inventories were “commercially significant.” However, a closer look at Complainants’ evidence reveals that the following Respondents do, in fact, maintain commercially significant inventories of the accused products in the United States: Barnes & Noble, Garmin, HTC, Huawei, and Samsung.

Simply put, [REDACTED]

[REDACTED] See Exs. 6, 8, 9, 10 and 11 to Complainants’ Pre-Hearing Brief, Dkt. 508779. Rather than find that these inventories are not commercially significant, however, the ID simply ignores them. This is error because the Commission has held that even “one infringing product is sufficient to constitute a ‘sufficient inventory’ for purposes of a cease and desist order.” *In re Certain Unified Commc’ns Sys., Products Used with Such Sys., & Components Thereof*, Inv. No. 337-TA-598, Pub. No. 4136 (U.S.I.T.C. Mar. 2010). See also *Certain Electronic Digital Media Devices & Components Thereof*, Inv. No. 337-TA-796, RD on Remedy and Bond (U.S.I.T.C. Nov. 7, 2012) (finding that thousands of units in inventory was “commercially significant”); *In re Certain Self-Cleaning Litter Boxes & Components Thereof*, Inv. 337-TA-625, RD on Remedy and Bond (U.S.I.T.C. Dec. 1, 2008) (finding that thousands of units in inventory was “commercially significant”).

Respondent [REDACTED] merely represents an “inventory snapshot” on a single day. The [REDACTED] indicates that [REDACTED]

██████████ of its products in inventory in the United States. *See* Ex. 10 to Complainants' Pre-Hearing Brief, Dkt. 508779. While this inventory amount is theoretically based on only "one day," ██████████ offers no explanation of why this commercially significant amount is not accurate or representative of the remaining 364 days in a year. Further, it is unclear how any inventory figure could represent something other than a snapshot of a single point in time.

Samsung also maintains a commercially significant inventory of wireless consumer electronics devices in the United States. *See, e.g., Certain Electronic Digital Media Devices & Components Thereof*, Inv. No. 337-TA-796, RD on Remedy and Bond (U.S.I.T.C. Nov. 7, 2012). In *Certain Electronic Digital Media Devices*, ALJ Pender held that both Samsung Electronics America ("SEA") and its affiliate Samsung Telecommunications America ("STA") maintain a commercially significant inventory of wireless consumer electronics devices. *Id.* at 6. Specifically, ALJ Pender held that STA's Chicago distribution center regularly receives shipments of thousands mobile phones (*i.e.* wireless electronics devices) with a combined value in the hundreds of thousands of dollars, and that SEA's American Distribution Center maintains "on-hand" inventory of more than 26,000 units of the Galaxy Tab (another wireless electronic device) worth more than \$10.5 million. *Id.* at 5-6.

Accordingly, cease and desist orders should issue against Barnes & Noble, Garmin, HTC, Huawei, and Samsung.

VI. CONCLUSION

For the foregoing reasons, Complainants respectfully request that the Commission grant review of the ID pursuant to Rule 210.43.

Dated: September 23, 2013

Respectfully submitted,

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**UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.**

Before the Honorable E. James Gildea
Administrative Law Judge

In the Matter of

**CERTAIN WIRELESS CONSUMER
ELECTRONICS DEVICES AND
COMPONENTS THEREOF**

Investigation No. 337-TA-853

CERTIFICATE OF SERVICE

I, Sherri Mills, hereby certify that on September 23, 2013, a copy of the foregoing document was served upon the following parties or their counsel in the manner indicated:

**COMPLAINANTS' PETITION FOR REVIEW OF INITIAL DETERMINATION
ON VIOLATION OF SECTION 337 AND RECOMMENDED DETERMINATION
OF REMEDY AND BOND (CONFIDENTIAL)**

<i>Acting Secretary</i>	
The Honorable Lisa R. Barton Acting Secretary U.S. International Trade Commission 500 E Street, S.W., Room 112A Washington, D.C. 20436	<input checked="" type="checkbox"/> Via EDIS <input checked="" type="checkbox"/> Via Overnight Courier <i>Eight Copies</i>
<i>Administrative Law Judge</i>	
The Honorable E. James Gildea U.S. International Trade Commission 500 E Street, S.W., Room 317 Washington, D.C. 20436	<input type="checkbox"/> Via Hand Delivery <input checked="" type="checkbox"/> Via Overnight Courier <i>Two Copies</i>
<i>Administrative Law Judge Attorney Advisors</i>	
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**CERTAIN WIRELESS CONSUMER ELECTRONICS
DEVICES AND COMPONENTS THEREOF**

Inv. No. 337-TA-853

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DEVICES AND COMPONENTS THEREOF**

Inv. No. 337-TA-853

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**CERTAIN WIRELESS CONSUMER ELECTRONICS
DEVICES AND COMPONENTS THEREOF**

Inv. No. 337-TA-853

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/s/ Sherri Mills

Sherri Mills

EXHIBIT 1

United States District Court
For the Northern District of California

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UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA,)
INC.,)
)
Plaintiffs,)
)
v.)
)
TECHNOLOGY PROPERTIES LIMITED,)
et al.,)
)
Defendants.)

Case No.: 5:08-cv-00882-PSG
**ORDER RE: EMERGENCY MOTION
FOR ADDENDUM TO JURY
INSTRUCTIONS**
(Re: Docket Nos. 513, 590)

Before the court is Plaintiff HTC Corporation and HTC America, Inc.’s
(collectively “HTC”) Emergency Motion for Addendum to Jury Instructions. The parties appeared
for a hearing earlier today. After considering the parties’ arguments the court rules as follows:


The court’s final jury instructions will instruct the jury that the terms “entire ring oscillator
variable speed system clock” (in claims 1 and 11), “entire oscillator” (in claims 6 and 13), and
“entire variable speed clock” (in claims 10 and 16) are properly understood to exclude any external
clock used to generate a signal.¹

¹ See Docket No. 513 at 11.

IT IS SO ORDERED.

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Dated: September 20, 2013



PAUL S. GREWAL
United States Magistrate Judge

United States District Court
For the Northern District of California

EXHIBIT 2

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 11 HTC CORPORATION and
 HTC AMERICA, INC.

12
 13 UNITED STATES DISTRICT COURT
 14 NORTHERN DISTRICT OF CALIFORNIA
 15 SAN JOSE DIVISION

16 HTC CORPORATION and HTC
 17 AMERICA, INC.,

18 Plaintiffs,

19 v.

20 TECHNOLOGY PROPERTIES
 LIMITED, PATRIOT SCIENTIFIC
 21 CORPORATION and ALLIACENSE
 LIMITED,

22 Defendants.

Case No. 5:08-cv-00882 PSG

[Related to Case No. 5:08-cv-00877 PSG]

~~PROPOSED~~ ORDER GRANTING
 EMERGENCY MOTION FOR
 CLARIFICATION OF ORDER ON
 ADDENDUM TO JURY INSTRUCTIONS

Complaint Filed: February 8, 2008

Trial Date: September 23, 2013

Date: September 23, 2013

Time: 9:00 a.m.

Place: Courtroom 5, 4th Floor


Judge: Hon. Paul S. Grewal

1 Having considered Defendants' Emergency Motion for Clarification of the Order on
2 Addendum to the Joint Proposed Jury Instructions, the record in this case and all related facts and
3 circumstances, and good cause appearing therefor, IT IS HEREBY ORDERED THAT:

4 The court's final jury instructions will instruct the jury that the terms "entire ring
5 oscillator variable speed system clock" (in claims 1 and 11), "entire oscillator" (in claims 6 and
6 13), and "entire variable speed clock" (in claims 10 and 16) are properly understood to exclude
7 any external clock used to generate the signal used to clock the CPU.

8 IT IS SO ORDERED.

9
10 Dated: September 23, 2013

11
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13 Hon. Paul S. Grewal
14 United States Magistrate Judge

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EXHIBIT 3

United States District Court
For the Northern District of California

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UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA,)
INC.,)
)
Plaintiffs,)
)
v.)
)
TECHNOLOGY PROPERTIES LIMITED,)
et al.,)
)
Defendants.)

Case No.: 5:08-cv-00882-PSG
**ORDER RE: HTC’S MOTIONS FOR
SUMMARY JUDGMENT OF
NON-INFRINGEMENT AND
NO WILLFULNESS**
(Re: Docket Nos. 457, 458)

Before the court in this patent case are two motions for summary judgment brought by Plaintiffs HTC Corporation and HTC America, (collectively “HTC”). HTC first moves for “full” summary judgment of non-infringement and no willful infringement of U.S. Patent No. 5,809,336 (“the ’336 patent”). HTC separately moves for partial summary judgment of non-infringement of the ’336 patent and U.S. Patent No. 5,530,890 (“the ’890 patent”) and no willful infringement of the ’890 patent. On August 13, 2013, the parties appeared for a hearing. Having considered the papers and arguments of counsel:

The court DENIES HTC’s motion for summary judgment of “full” non-infringement of the ’336 patent.

1 The court DENIES HTC's motion for partial summary judgment of non-infringement of the
2 '336 patent.

3 The court DENIES HTC's motion for summary judgment of no willful infringement of the
4 '336 patent.

5 The court GRANTS HTC's motion for partial summary judgment of non-infringement of
6 the '890 patent.

7 The court GRANTS-IN-PART HTC's motion for partial summary judgment of no willful
8 infringement of the '890 patent.

9 The court sets forth its reasoning below.

10 **I. BACKGROUND**

11
12 HTC Corporation is a Taiwan corporation with its principal place of business in Taoyuan,
13 Taiwan, R.O.C. HTC's subsidiary, HTC America, is a Texas corporation with its principal place
14 of business in Bellevue, Washington. Defendants Technology Properties Limited and Alliacense,
15 Limited ("Alliacense") are California corporations with their principal place of business in
16 Cupertino, California; Patriot Scientific Corporation ("Patriot") is a Delaware corporation with its
17 principal place of business in Carlsbad, California. These defendants – Technology Properties
18 Limited, Alliacense, and Patriot (collectively "TPL") – claim ownership of a family of related
19 microprocessor patents. TPL refers to those patents as the Moore Microprocessor Portfolio patents
20 ("MMP patents"), in recognition of co-inventor Charles Moore's contributions. HTC filed this suit
21 on February 8, 2008, seeking a judicial declaration that four of the MMP patents – U.S. Patent Nos.
22 5,809,336 ("the '336 patent"), 5,784,584 ("the '584 patent"), 5,440,749 ("the '749 patent"), and
23 6,598,148 ("the '148 patent") – are invalid and/or not infringed.¹ TPL counterclaimed for
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28 ¹ See Docket No. 1.

1 infringement of the '336, '749, '148, and '890 patents on November 21, 2008.² On April 25, 2008,
 2 TPL filed two complaints in the Eastern District of Texas against HTC alleging infringement of the
 3 four patents at issue in the pending declaratory judgment action.³ On June 4, 2008, TPL filed
 4 additional patent infringement actions against HTC in the Eastern District of Texas asserting U.S.
 5 Patent No. 5,530,890 ("the '890 patent").⁴ On July 10, 2008, HTC amended its complaint before
 6 this court, adding claims for declaratory relief with respect to the '890 patent.⁵ On February 23,
 7 2009 the parallel Texas litigation was dismissed without prejudice following Judge Fogel's
 8 decision to deny TPL's Motion to Dismiss, or in the Alternative, to Transfer Venue in the
 9 California action.⁶ On March 25, 2010, the court accepted the parties' stipulation to dismiss the
 10 '584 patent from this litigation.⁷ On August 24, 2012, Technology Properties Limited, Patriot, and
 11 Phoenix Digital Solutions initiated an International Trade Commission ("ITC") investigation
 12 regarding HTC's alleged infringement of the '336 patent.⁸ On July 17, 2013, the court accepted
 13 the parties' stipulation to dismiss the '148 and '749 patents from this litigation.⁹

14
 15 The bottom line is that only the '336 and '890 patents remain at issue for the purposes of
 16 this litigation.
 17

18 **A. The '336 Patent**

19 ² See Docket No. 60 at 6-8.

20 ³ See Docket No. 16 at 3.

21 ⁴ See Docket No. 35 at 5.

22 ⁵ See Docket No. 34.

23 ⁶ See Docket Nos. 49 (denying motion to dismiss, to transfer venue, and to stay) and 88 (granting
 24 motion for leave to file motion for reconsideration and denying motion for reconsideration).

25 ⁷ See Docket No. 152.

26 ⁸ See Docket No. 561-1. Claims 1, 6, 7, 9-11, and 13-16 were asserted in the investigation. On
 27 September 6, 2013, Administrative Law Judge James Gildea issued an Initial Determination from
 28 in the ITC proceeding holding that HTC did not violate Section 337 of the Tariff Act of 1930.
See id.

⁹ See Docket No. 462.

1 The '336 patent issued on September 15, 1998 and describes a microprocessor with an
2 internal variable speed clock, or oscillator, that drives the processor's central processing unit
3 ("CPU"). Traditional microprocessors use external, fixed speed crystals to clock the CPU. A
4 CPU's maximum possible processing capacity depends on process, voltage, and temperature
5 ("PVT parameters"). An external clock must therefore set the timing of the CPU to suboptimal
6 PVT conditions, resulting in waste of the CPU's processing speed under optimal conditions. The
7 internal, variable clock described in the '336 patent claims real-time adjustment of the timing of the
8 CPU by placing the clock on the chip itself. Thus, the CPU can perform optimally under any set of
9 parameters. The microprocessor nevertheless requires a second external clock because devices
10 other than the CPU do not operate at variable speed.

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12
13 TPL claims that HTC's accused products infringe the '336 patent by their internal, variable
14 speed oscillator on their microprocessors. At issue are claims 1, 6, 10, 11, 13, and 16.¹⁰

15 Claim 1 provides:

16 A microprocessor system, comprising a single integrated circuit including a central
17 processing unit and an entire ring oscillator variable speed system clock in said
18 single integrated circuit and connected to said central processing unit for clocking
19 said central processing unit, said central processing unit and said ring oscillator
20 variable speed system clock each including a plurality of electronic devices
21 correspondingly constructed of the same process technology with corresponding
22 manufacturing variations, a processing frequency capability of said central
23 processing unit and a speed of said ring oscillator variable speed system clock
24 varying together due to said manufacturing variations and due to at least operating
25 voltage and temperature of said single integrated circuit; an on-chip input/output
26 interface connected to exchange coupling control signals, addresses and data with
27 said central processing unit; and a second clock independent of said ring oscillator
28 variable speed system clock connected to said input/output interface, wherein a
clock signal of said second clock originates from a source other than said ring
oscillator variable speed system clock.

Claim 6 provides:

A microprocessor system comprising:

¹⁰ Docket No. 494 at 7.

1 a central processing unit disposed upon an integrated circuit substrate, said central
2 processing unit operating at a processing frequency and being constructed of a first
3 plurality of electronic devices; an entire oscillator disposed upon said integrated
4 circuit substrate and connected to said central processing unit, said oscillator
5 clocking said central processing unit at a clock rate and being constructed of a
6 second plurality of electronic devices, thus varying the processing frequency of said
7 first plurality of electronic devices and the clock rate of said second plurality of
8 electronic devices in the same way as a function of parameter variation in one or
9 more fabrication or operational parameters associated with said integrated circuit
10 substrate, thereby enabling said processing frequency to track said clock rate in
11 response to said parameter variation; an on-chip input/output interface, connected
12 between said central processing unit and an off-chip external memory bus, for
13 facilitating exchanging coupling control signals, addresses and data with said central
14 processing unit; and an off-chip external clock, independent of said oscillator,
15 connected to said input/output interface wherein said off-chip external clock is
16 operative at a frequency independent of a clock frequency of said oscillator and
17 wherein a clock signal from said off-chip external clock originates from a source
18 other than said oscillator.

19 Claim 10 provides:

20 In a microprocessor system including a central processing unit, a method for
21 clocking said central processing unit comprising the steps of: providing said central
22 processing unit upon an integrated circuit substrate, said central processing unit
23 being constructed of a first plurality of transistors and being operative at a
24 processing frequency; providing an entire variable speed clock disposed upon said
25 integrated circuit substrate, said variable speed clock being constructed of a second
26 plurality of transistors; clocking said central processing unit at a clock rate using
27 said variable speed clock with said central processing unit being clocked by said
28 variable speed clock at a variable frequency dependent upon variation in one or
more fabrication or operational parameters associated with said integrated circuit
substrate, said processing frequency and said clock rate varying in the same way
relative to said variation in said one or more fabrication or operational parameters
associated with said integrated circuit substrate; connecting an [on chip] on-chip
input/output interface between said central processing unit and an off-chip external
memory bus, and exchanging coupling control signals, addresses and data between
said input/output interface and said central processing unit; and clocking said
input/output interface using an off-chip external clock wherein said off-chip external
clock is operative at a frequency independent of a clock frequency of said variable
speed clock and wherein a clock signal from said off-chip external clock originates
from a source other than said variable speed clock.

Claim 11 provides:

A microprocessor system, comprising a single integrated circuit including a central
processing unit and an entire ring oscillator variable speed system clock in said
single integrated circuit and connected to said central processing unit for clocking
said central processing unit, said central processing unit and said ring oscillator

1 variable speed system clock each including a plurality of electronic devices
2 correspondingly constructed of the same process technology with corresponding
3 manufacturing variations, a processing frequency capability of said central
4 processing unit and a speed of said ring oscillator variable speed system clock
5 varying together due to said manufacturing variations and due to at least operating
6 voltage and temperature of said single integrated circuit; an on-chip input/output
7 interface connected to exchange coupling control signals, addresses and data with
8 said central processing unit; and a second clock independent of said ring oscillator
9 variable speed system clock connected to said input/output interface, wherein said
10 central processing unit operates asynchronously to said input/output interface.

11 Claim 13 provides:

12 A microprocessor system comprising: a central processing unit disposed upon an
13 integrated circuit substrate, said central processing unit operating at a processing
14 frequency and being constructed of a first plurality of electronic devices; an entire
15 oscillator disposed upon said integrated circuit substrate and connected to said
16 central processing unit, said oscillator clocking said central processing unit at a
17 clock rate and being constructed of a second plurality of electronic devices, thus
18 varying the processing frequency of said first plurality of electronic devices and the
19 clock rate of said second plurality of electronic devices in the same way as a
20 function of parameter variation in one or more fabrication or operational parameters
21 associated with said integrated circuit substrate, thereby enabling said processing
22 frequency to track said clock rate in response to said parameter variation; an on-chip
23 input/output interface, connected between said central processing unit and an off-
24 chip external memory bus, for facilitating exchanging coupling control signals,
25 addresses and data with said central processing unit; and an off-chip external clock,
26 independent of said oscillator, connected to said input/output interface wherein said
27 off-chip external clock is operative at a frequency independent of a clock frequency
28 of said oscillator and further wherein said central processing unit operates
asynchronously to said input/output interface.

Claim 16 provides:

In a microprocessor system including a central processing unit, a method for locking
said central processing unit comprising the steps of providing said central
processing unit upon an integrated circuit substrate, said central processing unit
being constructed of a first plurality of transistors and being operative at a
processing frequency; providing an entire variable speed clock disposed upon said
integrated circuit substrate, said variable speed clock being constructed of a second
plurality of transistors; clocking said central processing unit at a clock rate using
said variable speed clock with said central processing unit being clocked by said
variable speed clock at a variable frequency dependent upon variation in one or
more fabrication or operational parameters associated with said integrated circuit
substrate, said processing frequency and said clock rate varying in the same way
relative to said variation in said one or more fabrication or operational parameters
associated with said integrated circuit substrate; connecting an on-chip input/output
interface between said central processing unit and an off-chip external memory bus,

1 and exchanging coupling control signals, addresses and data between said
2 input/output interface and said central processing unit; and clocking said
3 input/output interface using an off-chip external clock wherein said off-chip external
4 clock is operative at a frequency independent of a clock frequency of said variable
5 speed clock, wherein said central processing unit operates asynchronously to said
6 input/output interface.

7 **B. The '890 Patent**

8 The '890 patent first issued on June 25, 1996 and originally included ten claims, nine of
9 which depended from the sole independent claim, claim 1.¹¹ On January 19, 2009, the '890 patent
10 was subjected to ex parte reexamination.¹² An amended version of the patent emerged on
11 March 1, 2011.¹³ The reexamination proceeding resulted in the cancellation of claims 1-4,
12 confirmation of the patentability of claims 5-10, and addition of claims 11-20. At issue in this suit
13 are claims 11, 12, 13, 17, and 19.¹⁴

14 Claim 11, the amended independent claim on which all of the other claims depend,
15 describes:

16 A microprocessor, which comprises a main central processing unit and a separate
17 direct memory access central processing unit in a single integrated circuit
18 comprising said microprocessor, said main central processing unit having an
19 arithmetic logic unit, a first push down stack with a top item register and a next item
20 register, connected to provide inputs to said arithmetic logic unit, an output of said
21 arithmetic logic unit being connected to said top item register, said top item register
22 also being connected to provide inputs to an internal data bus, said internal data bus
23 being bidirectionally connected to a loop counter, said loop counter being connected
24 to a decremter, said internal data bus being bidirectionally connected to a stack
25 pointer, return stack pointer, mode register and instruction register, said stack
26 pointer pointing into said first push down stack, said internal data bus being
27 connected to a memory controller, to a Y register of a return push down stack, an X
28 register and a program counter, said Y register, X register and program counter
providing outputs to an internal address bus, said internal address bus providing
inputs to said memory controller and to an incrementer, said incrementer being
connected to said internal data bus, said direct memory access central processing

¹¹ See Docket No. 458 at 2.

¹² See *id.*

¹³ See *id.*

¹⁴ See *id.*

1 unit providing inputs to said memory controller, said memory controller having an
2 address/data bus and a plurality of control lines for connection to a random access
3 memory.

4 During reexamination, the patentee added the phrase “said stack pointer pointing into said first
5 push down stack,” which did not appear in claim 1.

6 II. SUMMARY JUDGMENT STANDARDS

7 Summary judgment is appropriate only if there is “no genuine dispute as to any material
8 fact and the movant is entitled to judgment as a matter of law.”¹⁵ The moving party bears the
9 initial burden of production by identifying those portions of the pleadings, discovery, and affidavits
10 which demonstrate the absence of a triable issue of material fact.¹⁶ The standard for summary
11 judgment differs depending on whether the moving party bears the burden of persuasion at trial.¹⁷
12 If the moving party bears the burden of persuasion at trial, that party must present “credible
13 evidence” showing that he is entitled to a directed verdict.¹⁸ The burden of production then shifts
14 to the non-moving party to produce evidence raising a genuine issue of material fact.¹⁹ On the
15 other hand, if the moving party does not bear the burden of persuasion at trial, he can prevail on a
16 motion for summary judgment in two ways: by proffering “affirmative evidence negating an
17 element of the non-moving party’s claim,” or by showing the non-moving party has insufficient
18 evidence to establish an “essential element of the non-moving party’s claim.”²⁰ If met by the
19 moving party, the burden of production then shifts to the non-moving party, who must then provide
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23 ¹⁵ Fed. R. Civ. P. 56(a).

24 ¹⁶ See Fed. R. Civ. P. 56(c)(1); *Celotex Corp. v. Catrett*, 477 U.S. 317, 323 (1986).

25 ¹⁷ See *Celotex Corp.*, 477 U.S. at 331.

26 ¹⁸ *Id.*

27 ¹⁹ See *id.*

28 ²⁰ *Id.*

1 specific facts showing a genuine issue of material fact for trial.²¹ In both instances, the ultimate
 2 burden of persuasion remains on the moving party.²² In reviewing the record, the court must
 3 construe the evidence and the inferences to be drawn from the underlying evidence in the light
 4 most favorable to the non-moving party.²³

5 III. DISCUSSION

6 A. HTC's Motion for Summary Judgment of Non-Infringement and No Willful 7 Infringement of the '336 Patent

8 1. Non-Infringement of the '336 Patent

9 The court first considers HTC's motion for summary judgment of "full" non-infringement
 10 of the '336 patent. HTC argues that summary judgment is warranted because when the
 11 independent claims of the '336 patent are properly construed, HTC's products do not perform the
 12 claimed invention. HTC specifically points to three terms that each appear in two claims:
 13 (1) "entire ring oscillator variable speed system clock" (claims 1 and 11), (2) "entire oscillator"
 14 (claims 6 and 13), and (3) "an entire variable speed system clock" (claims 10 and 16).
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16 HTC argues as follows. The prosecution history of the '336 patent demonstrates the
 17 applicants' repeated and express disclaimer that the claimed timing element – the oscillator or
 18 variable speed clock – had any connection to or dependence on a reference signal from an external
 19 crystal or other fixed timing piece. To further distinguish the '336 patent, the applicants added the
 20 "entire" term to explicitly claim only a timing element that wholly and exclusively appeared with
 21 the CPU on the chip. HTC's processors, in contrast, rely on an external crystal timing piece (called
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25 ²¹ See *id.* at 330; *T.W. Elec. Service, Inc. v. Pac. Elec. Contractors Ass'n*, 809 F.2d 630, 630
 26 (9th Cir. 1987).

27 ²² See *id.*

28 ²³ See *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 248 (1986); *Matsushita Elec. Indus. Co. v. Zenith Radio Corp.*, 475 U.S. 574, 587 (1986).

1 a phase-locked loop or “PLL”). Unlike the invention, therefore, the timing elements of HTC’s
2 processors do not sit entirely on the chip and do not vary with PVT parameters.

3 TPL responds that HTC improperly seeks reconsideration of this court’s previous claim
4 construction. The court properly construed the “entire variable speed system clock” term and this
5 construction should extend to the other three “entire” terms. HTC’s additional limitations are not
6 supported by the specification, which does not speak to whether the oscillator or variable speed
7 system clock also could work with an external crystal. As for any disclaimer, the applicants never
8 disclaimed all reliance or reference to an off-chip crystal. Instead, the disclaimer to avoid the
9 Magar reference was to an off-chip oscillator that generated the on-chip clock. As to the Sheets
10 reference, the applicants distinguished their clock reference by pointing out that it was not an
11 on-chip oscillator but rather an off-chip clock, and that off-chip clock required a command input to
12 change its frequency. The oscillator taught by the ’336 patent, in contrast, is self-generating on the
13 chip itself and does not require an outside command to change frequency. As to the variation
14 argument, even by HTC’s own admission, the on-chip HTC oscillators vary and the PLLs in fact
15 serve to limit that variation. That the net result may be a minimal change in the frequency of the
16 clock is not enough to take HTC’s accused products beyond the claim language.

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19 HTC replies that the on-chip oscillator does not “generate” the CPU clock unless it
20 communicates with the PLL, making the PLL necessary to “generate” the clock – and thereby
21 outside of the claim language (as construed in light of the disclaimers). HTC further replies that
22 frequency control in fact is generation of the clock because the oscillator does not begin to run
23 independently. The PLL controls the oscillator and sets the frequency, which generates the clock.
24 As to the variation issue, HTC argues that a person of ordinary skill in the art would understand the
25 de minimis variation experienced by its products as rendering the timing element essentially fixed.
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1 The court agrees with HTC that the disputed limitations are properly understood to exclude
 2 any external clock used to generate a signal.²⁴ Nevertheless, there remains a factual dispute
 3 whether HTC’s products contain an on-chip ring oscillator that is self-generating and does not rely
 4 on an input control to determine its frequency. While HTC’s expert says that the PLLs generate
 5 the clock, TPL’s expert counters that the ring oscillators generate the clock and the PLLs merely
 6 buffer or fix the frequency.²⁵ This is a classic factual question that requires a trial to answer.

7 2. Willful Infringement of the ’336 Patent

8 To “establish willful infringement, a patentee must show by clear and convincing evidence
 9 that the infringer acted despite an objectively high likelihood that its actions constituted
 10 infringement of a valid patent.”²⁶ A patentee therefore must establish two elements. First, the
 11 patentee must show the accused infringer acted with “objective recklessness.” Objective
 12 recklessness remains a question of law “predicated on underlying mixed questions of law and
 13 fact.”²⁷ The objective recklessness prong “entails an objective assessment of potential defenses
 14 based on the risk presented” by the patent which “may include questions of infringement but also
 15 can be expected in almost every case to entail questions of validity that are not necessarily
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19 ²⁴ The patentee’s arguments traversing the prior art narrowed the claims. *See Festo Corp. v.*
 20 *Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722, 740 (2002) (“A patentee’s decision to
 21 narrow his claims through amendment may be presumed to be a general disclaimer of the territory
 22 between the original claim and the amended claim.”); *cf. Saeilo Inc. v. Colt’s Mfg. Co.*,
 23 26 F. App’x 966, 973 (Fed. Cir. 2002) (“Where an amendment narrows the scope of a claim for a
 24 reason related to the statutory requirements for patentability, prosecution history estoppel acts as a
 25 complete bar to the application of the doctrine of equivalents to the amended claim element.”).

26 ²⁵ *Compare* Docket No. 457 at 16 (“the oscillators in the accused products indisputably rely on an
 27 external crystal or clock generator to clock” the CPU), *with* Docket No. 470 at 14 (“Each HTC
 28 product includes a CPU/system clock – a **ring oscillator** within a PLL – that **generates** a clock
 signal **on its own**, as long as it has a power supply.”) (emphasis in original).

²⁶ *In re Seagate Tech., LLC*, 497 F.3d 1360, 1371 (Fed. Cir. 2007) (*en banc*).

²⁷ *See Bard Peripheral Vascular, Inc. v. W.L. Gore & Assocs., Inc.*, 682 F.3d 1003, 1006-07
 (Fed. Cir. 2012) (holding that the objective determination of recklessness, even though predicated
 on underlying mixed questions of law and fact, is decided by the judge as a question of law subject
 to de novo review).

1 dependent on the factual circumstances of the particular party accused of infringement.”²⁸ Second,
2 if the requisite threshold objective recklessness is established, then the patentee must show that the
3 “objectively-defined risk” of infringement determined by the record developed in the infringement
4 proceeding “was either known or so obvious that it should have been known to the accused
5 infringer.”²⁹

6 HTC argues that TPL has not presented sufficient evidence to make a prima facie case of
7 willful infringement, in view of its “clear, legitimate, and objectively reasonable defenses” to
8 HTC’s claims of infringement.³⁰ In particular, its proposed constructions have been adopted by
9 other tribunals and the ITC in particular. HTC’s non-infringement position at the ITC was
10 “sufficiently compelling and reasonable” that both the ITC staff attorney and Judge Gildea himself
11 agreed with HTC’s position.³¹

12 TPL takes issue with HTC’s reference in this case to the ITC litigation. Different theories
13 of infringement and different products are implicated by the two cases. Different claim
14 constructions have issued in the cases. The staff attorney’s position and Judge Gildea’s
15 conclusions are therefore irrelevant. Separately, TPL’s successful licensing of the MMP patent
16 portfolio suggests that HTC could not reasonably or realistically expect its invalidity or
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21 ²⁸ *Id.* at 1006.

22 ²⁹ *Seagate*, 497 F.3d at 1371.

23 ³⁰ Looking to Fed. R. Civ. P. 37(c)(1) HTC further points out that TPL failed to substantively
24 respond to its interrogatory about willful infringement. *See* Fed. R. Civ. P. 37(c)(1) (“If a party
25 fails to provide information or identify a witness as required by Rule 26(a) or (e), the party is not
26 allowed to use that information or witness to supply evidence on a motion, at a hearing, or at a trial,
27 unless the failure was substantially justified or is harmless.”). But TPL’s response raising a host of
28 objections appears substantially justified, even if it is not ultimately persuasive, and in any event
HTC does not appear to have taken any steps whatsoever in the intervening four years to compel a
more complete response.

³¹ Judge Gildea’s Initial Determination (“ID”) did not issue until September 6, 2013, after the
papers for this motion were filed.

1 non-infringement defenses to succeed in this litigation. Finally, direct pre-suit communication
2 between HTC and TPL establishes that HTC had notice of its allegedly infringing activities.

3 District courts appear split as to whether current evidence that a party's actions were
4 objectively reasonable is relevant to a willfulness analysis under *Seagate*. In *i4i Ltd. P'ship v.*
5 *Microsoft Corp.*, Judge Davis held that the correct willfulness analysis "focuses on whether, given
6 the facts and circumstances prior to [the accused infringer's] infringing actions, a reasonable
7 person would have appreciated a high likelihood that acting would infringe a valid patent."³² The
8 "number of creative defenses that Microsoft is able to muster in an infringement action after years
9 of litigation and substantial discovery is irrelevant to the objective prong of the *Seagate* analysis."³³
10 Judge Davis then explained that the court should more properly focus on whether defenses would
11 have been objectively reasonable and apparent before Microsoft infringed and was sued.³⁴ In
12 *Uniloc USA, Inc. v. Microsoft Corp.*, Judge Smith was "not convinced that such a 'before and after'
13 line is so easily drawn, or for that matter appropriate, to measure the objective likelihood (or lack
14 thereof) that a party acted to infringe a valid patent."³⁵ Judge Smith emphasized that "the inquiry
15 is case-specific" and should focus on an objective view of the record.³⁶

16
17
18 The court agrees with HTC that favorable court rulings can support the objective
19 reasonableness of its non-infringement positions. The court cannot help but take note of the
20 analogous issue of the "book of wisdom" when addressing patent damages. The Supreme Court
21 has affirmed that after-arising "[e]xperience . . . is a book of wisdom that courts may not
22

23
24 ³² 670 F. Supp. 2d 568, 582 (E.D. Tex. 2009).

25 ³³ *Id.*

26 ³⁴ *See id.*

27 ³⁵ 640 F. Supp. 2d 150, 177 n. 33 (D.R.I. 2009).

28 ³⁶ *Id.*

1 neglect.”³⁷ Nonetheless, “as the party moving for summary judgment” HTC “must do more than
 2 persuade [the court] that its defenses were reasonable.”³⁸ Instead, HTC “must establish that ‘there
 3 is no genuine dispute as to any material fact’ and that [the accused infringer] ‘is entitled to
 4 judgment as a matter of law’—in other words, that *no reasonable fact-finder* could find willful
 5 infringement.”³⁹

6 Viewing the evidence in the light most favorable to TPL, the court concludes that a
 7 reasonable fact finder could plausibly find facts sufficient to support a conclusion of willful
 8 infringement. TPL’s burden to show willful infringement by clear and convincing evidence is a
 9 steep one. But where factfinding is necessary, trial courts generally reserve willfulness until after a
 10 full presentation of the evidence on the record to the jury.⁴⁰ The record supports a finding that
 11 HTC knew about the patents and TPL’s claims of infringement before it began the activities that
 12 allegedly infringe and as explained above, here there remains an important issue regarding the role
 13 of the external crystal in HTC’s products in generating a signal.⁴¹ Under these circumstances
 14 summary judgment on the issue of willfulness is not warranted.

15
 16
 17 **B. Partial Summary Judgment of Non-Infringement of the ’336 Patent and the ’890
 18 Patent and No Willful Infringement of the ’890 Patent**

19 HTC next moves for partial summary judgment of non-infringement of the ’336 patent and
 20 the ’890 patent based on the doctrine of absolute intervening rights. By this same motion, HTC
 21 also seeks summary judgment of no willful infringement under the ’890 patent.

22
 23 ³⁷ *Sinclair Ref. Co. v. Jenkins Petroleum Process Co.*, 289 U.S. 689, 690 (1933).

24 ³⁸ *Kimberly-Clark Worldwide, Inc. v. First Quality Baby Products, LLC*, Case No. 1:09-cv-1685,
 2013 WL 1465403, at *2 (M.D. Pa. Apr. 11, 2013)

25 ³⁹ *Id.* (citing Fed. R. Civ. P. 56(a)).

26 ⁴⁰ *See, e.g. Bard*, 682 F.3d at 1008; *Fujitsu Ltd. v. Belkin Int’l, Inc.*, Case No. 10-cv-03972-LHK,
 27 2012 WL 4497966, at *39 (N.D. Cal. Sept. 28, 2012).

28 ⁴¹ *See* Docket No. 470-1, Ex. A (Nov. 7, 2006 correspondence from Alliacense to HTC);
 Docket No. 470-1, Ex. B (Nov. 20, 2006 correspondence from Alliacense to HTC).

1 Under 35 U.S.C § 307(b), a patent owner may not recover for infringement of claims that
2 are invalidated or amended through the reexamination process.⁴² The “reexamination statute
3 restricts a patentee’s ability to enforce the patent’s original claims to those claims that survive
4 reexamination in ‘identical’ form.”⁴³ “‘Identical’ does not mean verbatim, but means at most
5 without substantive change.”⁴⁴ The court must therefore determine whether the scope of the claims
6 are the same, not just whether the same words are used.⁴⁵ Section 307 shields “those who deem an
7 adversely held patent to be invalid; if the patentee later cures the infirmity by reissue or
8 reexamination, the making of substantive changes in the claims is treated as an irrebuttable
9 presumption that the original claims were materially flawed.”⁴⁶ The “statute relieves those who
10 may have infringed the original claims from liability during the period before the claims are
11 validated.”⁴⁷

12
13 Whether “amendments made to overcome rejections based on prior art are substantive
14 depends on the nature and scope of the amendments, with due consideration to the facts in any
15 given case that justice will be done.”⁴⁸ “An amendment that clarifies the text of the claim or makes
16 it more definite without affecting its scope is generally viewed as identical.”⁴⁹ To make its
17 determination under the so-called doctrine of intervening rights, the court must consider “the scope
18 of the original and reexamined claims in light of the specification, with attention to the references
19
20

21 ⁴² See *Fresenius USA, Inc. v. Baxter Intern., Inc.*, 721 F.3d 1330, 1339 (Fed. Cir. 2013).

22 ⁴³ *Id.* (listing cases).

23 ⁴⁴ *Id.*

24 ⁴⁵ See *id.*

25 ⁴⁶ *Bloom Eng’g Co. v. N. Am. Mfg. Co.*, 129 F.3d 1247, 1249 (Fed. Cir. 1997).

26 ⁴⁷ *Id.*

27 ⁴⁸ *Id.*

28 ⁴⁹ *Id.*

1 that occasioned the reexamination, as well as the prosecution history and any other relevant
2 information.”⁵⁰

3 **1. Non-Infringement of the '336 Patent**

4 As noted earlier the '336 patent issued September 15, 1998, and included ten
5 originally-issued claims.⁵¹ A series of ex parte reexamination requests were filed against the '336
6 patent between October 2006 and January 2007.⁵² When the reexamination proceedings
7 completed, claims 1, 6, and 10 emerged with modified language, and new independent claims 11,
8 13, and 16 were added. TPL amended claim 1 to further describe the “second clock independent of
9 said ring oscillator” to say that “wherein a clock signal of said clock originates from a source other
10 than said ring oscillator variable speed system clock.” Claim 6 was amended to describe the
11 “off-chip external clock” to likewise derive its “clock signal” “from a source other than said
12 oscillator.” Claim 10 includes a similar amendment that adds that the “off-chip external clock” has
13 a “clock signal” that “originates form a source other than said variable speed clock.” Claims 6 and
14 10 also added “off-chip” references to the descriptions of the second clocks. Claims 11, 13, and 16
15 were based on independent claims 1, 6, and 10, but during reexamination TPL added an additional
16 clause to the end of each claim: “wherein said central processing unit operates asynchronously to
17 said input/output interface.”
18
19

20 In HTC’s view, it should not be held liable for infringement of the '336 patent claims 1, 6,
21 10, 11, 13, and 16 because those claims were either substantially narrowed or newly-added through
22 reexamination. Any recovery for the '336 patent should be limited to the date of the issuance of
23 the reexamination certificate on December 15, 2009, because the amendments were sufficiently
24 substantive to preclude recovery from before the amendments.
25

26 ⁵⁰ *Id.*

27 ⁵¹ *See* Docket No. 458 at 5.

28 ⁵² *Id.*

1 TPL responds that these amendments serve as nothing more than clarification of the claim
2 language and that the scope of the claims have not changed. Several excerpts from the prosecution
3 history of the reexamination demonstrate that the patentee believed the amended claim language
4 only clarified how the second clock was “independent”⁵³ and that the “external” components were
5 in fact “off-chip”⁵⁴.

6 HTC replies that the original claims differ from the amended claims in scope because the
7 original claims spoke only to the difference in frequency control – and that is what “independence”
8 really references in these claim terms. Because a clock with signal origins from the ring oscillator
9 but with an independent frequency could exist under the original claims but not under the amended
10 claims, the claim is narrower and therefore substantively different. For claims 11, 13, and 16, the
11 “independent” clock signals could have a “readily predictable phase relationship.” Because of that
12 possibility, the claims are narrower and thereby substantively different. Further, the court should
13 not credit self-serving testimony from the prosecution history.⁵⁵

14
15 On balance, the court finds that the amended claim language added during reexamination
16 did not substantively amend the asserted ‘336 claims’ scope. “Independent” in the disputed claims
17 must be understood to be just that: without dependence of any kind. While HTC offers a more
18 nuanced interpretation that focuses exclusively on frequency control, it cites no intrinsic – or for
19 that matter extrinsic evidence – to support its position. Coupled with the references in the
20 prosecution history indicating that the amendments really were for clarification purposes only,
21 TPL’s argument is more persuasive.
22

23
24 ⁵³ See Docket No. 471-5, Ex. E at 2; Docket No. 471-6, Ex. F at 11, 27; Docket No. 471-7,
Ex. G at 8-12, 14.

25 ⁵⁴ See Docket No. 471-7, Ex. G at 12, 16.

26 ⁵⁵ See *Moleculon Research Crop. v. CBS, Inc.*, 793 F.2d 1261, 1270 (Fed. Cir. 1986) (holding that
27 documents submitted by the patentee during prosecution may be considered for claim interpretation
28 purposes, but “might very well contain merely self-serving statements which likely would be
accorded no more weight than testimony of an interested witness or argument of counsel. Issues of
evidentiary weight are resolved on the circumstances of each case.”).

1 **2. Motion for Partial Summary Judgment of Non-Infringement and No Willful**
 2 **Infringement of the '890 Patent**

3 **a. Non-Infringement of the '890 Patent**

4 The court next considers HTC's motion for summary judgment of non-infringement of the
 5 '890 patent claims 11, 12, 13, 17, and 19. As noted above, claims 12, 13, 17, and 19 all depend on
 6 independent claim 11.

7 HTC again argues the doctrine of absolute intervening rights entitles it to summary
 8 judgment of non-infringement. During reexamination, TPL added claim language further defining
 9 a stack pointer as "pointing into said first push down stack," after the examiner identified no
 10 function for the stack pointer in the original claim language. The examiner noted that the
 11 amendment to claim 1 prevented the claim from being anticipated by the prior art under
 12 35 U.S.C. § 102. This change to the '890 patent during reexamination was substantive and that the
 13 absolute intervening rights doctrine bars liability arising before the reexamination terminated.
 14

15 TPL initially responds that HTC's assertion of the absolute intervening rights doctrine is
 16 untimely because it did not include the affirmative defense in its answer to TPL's complaint.⁵⁶ As
 17 to the merits, TPL says that the amendment only clarified the claim scope but did not substantively
 18 amend the claim, precluding the absolute intervening rights doctrine. Further, in *Norwood v.*
 19 *Vance* the Ninth Circuit noted that parties may raise affirmative defenses for the first time at
 20 summary judgment only if the opposing party is not prejudiced.⁵⁷ Allowing HTC to assert the
 21 defense – four years into this litigation – would subject it to unfair prejudice.
 22

23 The court is not persuaded that TPL has established the prejudice necessary to bar HTC's
 24 assertion of the absolute intervening rights doctrine at this stage in the litigation. TPL does not, for
 25

26 ⁵⁶ The initial declaratory judgment complaint in this case was filed February 8, 2008.
 27 *See supra* note 1. The '890 patent did not reissue following reexamination until March 1, 2011.
 28 *See supra* note 13.

⁵⁷ 591 F.3d 1062, 1075 (9th Cir. 2010).

1 example, articulate the discovery it might have otherwise taken had HTC promptly moved to
2 amend its answer in 2011.

3 Turning to the merits, HTC asserts estoppel and argues claim 11 emerged from
4 reexamination substantively different from former claim 1. During reexamination, the examiner
5 found claim 1 invalid. In an August 12, 2010, advisory action the examiner noted that claim 1
6 failed to provide a function for the “stack pointer” and the claim language only identified the stack
7 pointer as “bidirectionally connected to an internal bus,” – an error claim 11 corrected. The
8 examiner also observed that the additional language in claim 11 avoided the May reference,
9 U.S. Patent No. 4,758,948 (“the ’948 patent”), that teaches using a push down stack but not
10 expressly a stack pointer performing the function that the amended language defines. Therefore,
11 that the absolute intervening rights doctrine bars infringement liability prior to the issuance of the
12 reexamination certificate.
13

14 TPL sees it differently. The change to claim 11 only makes the claim more definite. The
15 examiner’s primary concern with claim 1 centered on the discussion in the May patent of an
16 instruction pointer. The instruction pointer identifies the instructions of a process and under the
17 broadest interpretation the stack pointer likewise could be construed to read onto the prior art. No
18 person of ordinary skill in the art would understand a stack pointer could not perform equivalently
19 to an instruction pointer. As described in claim 1, the stack pointer would be understood by a
20 person of ordinary skill in the art to point only to the first push down stack referenced in claim 1
21 – and so the additional language only explicitly states what a person of ordinary skill in the art
22 already would understand claim 1 to teach.
23
24

25 HTC replies that TPL’s arguments rely on extrinsic evidence and that the intrinsic evidence
26 reveals that absent the added limitation, the stack pointer was impermissibly vague and the
27 amendment substantively narrowed the claim.
28

1 The court agrees with HTC. As the examiner's office actions indicated, in the original
2 claim language the stack pointer did nothing except connect to the internal data bus, but TPL's
3 argument that a person of ordinary skill in the art necessarily would color in the ambiguity with an
4 understanding that the stack pointer points only to the first push down stack is not persuasive. As
5 HTC points out, claim 1 (and claim 11) employs the term "comprising," which reveals that the
6 claim is "inclusive or open-ended and does not exclude additional, unrecited elements or method
7 steps."⁵⁸ Given that the specification in fact references a second push down stack, the second stack
8 must be presumed to be distinct from the return stack identified in the claim language, other push
9 down stacks potentially could be used and still fall within claim 1. Thus, where the stack pointer
10 points matters. If multiple push down stacks were included in a processor, it is unclear under the
11 language of claim 1 whether the stack pointer points to one of the stacks, all of the stacks, or some
12 multiple in between.

14 At bottom, the court finds the added language limits the stack pointer to the first push down
15 stack and substantively changes the scope of the claim. Because the added claim language narrows
16 the scope of the claims, any claims of infringement before the date of the issuance of the
17 reexamination certificate must be precluded.

19 **b. Willful Infringement of the '890 Patent**

20 The court finally addresses the issue of willful infringement related to the '890 patent.

21 HTC asserts that under the objective recklessness prong, the reexamination and amendment
22 of the '890 patent supports HTC's position that it was not objectively reckless. HTC points out
23 that TPL has offered no evidence that it even knew of the '890 patent before the suit. HTC also
24 argues that the failure by TPL to pursue a preliminary injunction suggests that willful infringement
25 is not at issue.
26

27
28 ⁵⁸ *CollegeNet, Inc. v. ApplyYourself, Inc.*, 418 F.3d 1225, 1235 (Fed. Cir. 2005).

1 TPL responds that it provided notice to HTC of the patents and of its infringing behavior in
 2 2006. The reexamination process actually cuts against HTC because most of the substance of the
 3 patents in fact survived intact with a “second stamp of validity from the PTO.”⁵⁹ The PTO accepts
 4 92% of reexamination applications, so the PTO’s grant of patent reexamination is not enough to
 5 undercut willful infringement.⁶⁰ A “substantial question of patentability raised by a reexamination
 6 request is not dispositive” in a willfulness inquiry.⁶¹

7
 8 Although the record at least suggests that HTC was made aware of the patents-in-suit as
 9 early as November 2006,⁶² as discussed above the reexamined ’890 patent bars claims of
 10 infringement before the date of the issuance of the certificate because the additional language
 11 added to independent claim 11 narrowed the scope of the claim.⁶³ It follows that because HTC
 12 cannot be held liable for infringement before March 1, 2011, willful infringement for this period is
 13 precluded.

14
 15 The court next turns to whether HTC can be found to have willfully infringed the ’890
 16 patent following reexamination. Generally, a “patentee who does not attempt to stop an accused
 17 infringer’s activities [by moving for a preliminary injunction] should not be allowed to accrue

18
 19
 20

⁵⁹ Docket No. 469 at 17.

21 ⁶⁰ *See id.* n.11.

22 ⁶¹ *Plumley v. Mockett*, 836 F. Supp. 2d 1053, 1075 (C.D. Cal. 2010); *see also See Lucent Techs.,*
 23 *Inc. v. Gateway, Inc.*, Case No. 07-cv-2000-H, 2007 WL 6955272, at *7 (S.D. Cal. Oct. 30, 2007)
 24 (“The Court does not assume that a reexamination order will always prevent a plaintiff from
 meeting their burden on summary judgment regarding willful infringement, but it does consider
 this as one factor among the totality of the circumstances.”).

25 ⁶² *See* Docket No. 469-12, Ex. C (correspondence from Alliacense notifying HTC that HTC was
 26 infringing the patents contained in the MMP Portfolio, including the ’890 patent).

27 ⁶³ Moreover, at least one district court has noted, albeit in dicta, that “a patentee’s willful
 28 infringement claim fails as a matter of law where the PTO requires amendments to the patent
 before issuing a reexamination certificate.” *Plumley*, 836 F. Supp. 2d at 1075 (explaining court’s
 opinion in *TGIP, Inc. v. AT & T Corp.*, 527 F. Supp. 2d 561 (E.D. Tex. 2007)).

1 enhanced damages based solely on the infringer’s post-filing conduct.”⁶⁴ But as TPL happily
 2 highlights, HTC conceded in prior litigation “that *Seagate* did not create a *per se* bar to claims for
 3 post-filing willful infringement where an injunction was not sought.”⁶⁵ “Because *Seagate* did not
 4 create a *per se* bar, the determination of whether a patentee may pursue a claim for willful
 5 infringement based on post-filing conduct without seeking a preliminary injunction ‘will depend on
 6 the facts of each case.’”⁶⁶ Patentees who neither practice the invention nor directly compete with
 7 the accused infringer are “excused from *Seagate*’s rule that a patentee must seek an injunction to
 8 sustain a claim for post-filing willful infringement.”⁶⁷ There may be circumstances “where an
 9 infringer’s post-filing conduct was found to be willful” where “some material change that could
 10 create an objectively high likelihood of infringing a valid patent, such as a patent surviving a
 11 reexamination proceeding without narrowed claims.”⁶⁸

12
 13 Viewing the evidence in the light most favorable to TPL and drawing all reasonable
 14 inferences in its favor, especially TPL’s successful licensing program related to the patents-in-suit,
 15 the court concludes that a reasonable fact finder could plausibly find facts supporting a conclusion
 16 of willful infringement following the reexamination of the ’890 patent.
 17

18
 19
 20
 21 ⁶⁴ *Seagate*, 497 F.3d at 1372; see also *Anascape, Ltd. v. Microsoft Corp.*, Case No. 9:06-cv-158,
 22 2008 WL 7182476 (E.D. Tex. Apr. 25, 2008) (patentee who did not move for preliminary
 injunction was not entitled to benefit from its lack of diligence by obtaining enhanced damages for
 willfulness during the post-filing period).

23 ⁶⁵ *DataQuill Ltd. v. High Tech Computer Corp.*, 887 F. Supp. 2d 999, 1015 (S.D. Cal. 2011).

24 ⁶⁶ *Id.* (citing *Seagate* 497 F.3d at 1374).

25 ⁶⁷ *Id.*

26 ⁶⁸ *LML Holdings, Inc. v. Pac. Coast Distrib. Inc.*, Case No. 11-cv-06173-YGR, 2012 WL 1965878
 27 (N.D. Cal. May 30, 2012) (citing *St. Clair Intellectual Prop. Consultants, Inc. v. Palm, Inc.*,
 Case No. 04–1436–JJF–LPS, 2009 WL 1649751, at *1 (D. Del. Jun.10, 2009)); see also *Webmap*
 28 *Technologies, LLC v. Google, Inc.*, Case No. 2:09–cv–343–DF–CE, 2010 WL 3768097, at *2-3
 (E.D. Tex. Sep. 10, 2010).

IT IS SO ORDERED.

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Dated: September 17, 2013



PAUL S. GREWAL
United States Magistrate Judge

United States District Court
For the Northern District of California

**UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.**

Before the Honorable E. James Gildea
Administrative Law Judge

In the Matter of

**CERTAIN WIRELESS CONSUMER
ELECTRONICS DEVICES AND
COMPONENTS THEREOF**

Investigation No. 337-TA-853

CERTIFICATE OF SERVICE

I, Sherri Mills, hereby certify that on October 22, 2013 a copy of the foregoing document was served upon the following parties or their counsel in the manner indicated:

**COMPLAINANTS' PETITION FOR REVIEW OF INITIAL
DETERMINATION ON VIOLATION OF SECTION 337 AND
RECOMMENDED DETERMINATION ON REMEDY AND BOND
(PUBLIC VERSION)**

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**CERTAIN WIRELESS CONSUMER ELECTRONICS
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