UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

Before the Honorable E. James Gildea
Administrative Law Judge

In the Matter of **CERTAIN WIRELESS CONSUMER ELECTRONICS DEVICES AND COMPONENTS THEREOF**	**Investigation No. 337-TA-853**

COMMISSION INVESTIGATIVE STAFF'S INITIAL MARKMAN BRIEF

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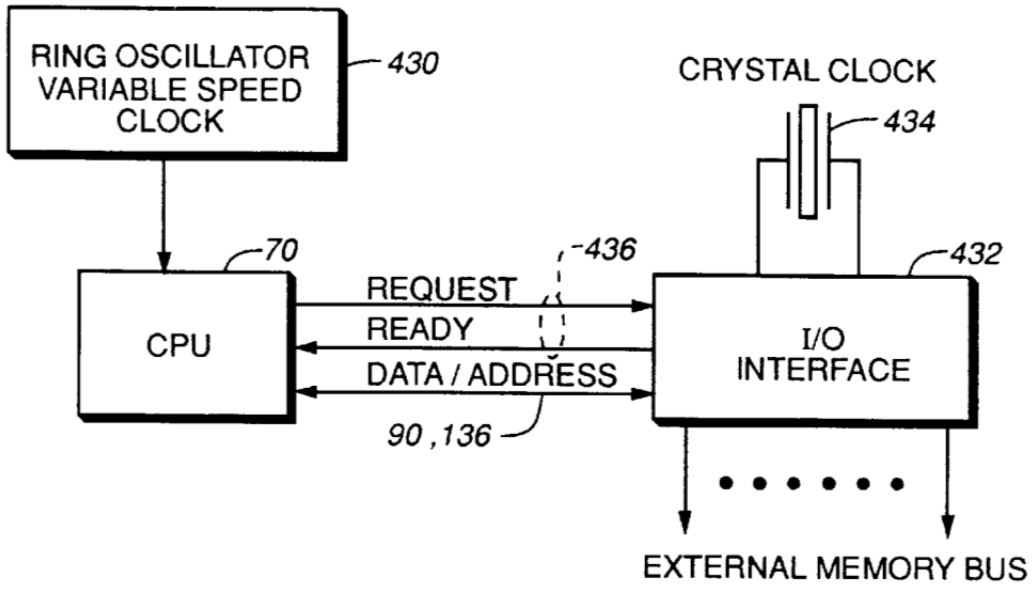
I. PROCEDURAL BACKGROUND

Pursuant to Order No. 15 (January 9, 2013), the Commission Investigative Staff ("Staff") respectfully submits its initial *Markman* brief. The Staff notes that the discussion below is directed at the presently disputed claim terms. Should the private parties raise additional claim construction disputes in the future, *e.g.*, as part of their rebuttal *Markman* briefs or as part of the parties' pre-hearing statements and briefs, the Staff may seek to address such disputes if and when appropriate. The Staff further notes that insofar as expert and fact discovery is not yet completed, it may become necessary for the Staff to modify constructions proposed herein in light of future discovery.

II. TECHNICAL OVERVIEW

U.S. Patent No. 5,809,336 ("the '336 patent"), titled "High Performance Microprocessor Having Variable Speed System Clock," is the sole asserted patent in this investigation. The '336 patent issued on September 15, 1998 from U.S. Patent Application No. 08/484,918 ("the '918 application"), which was filed June 7, 1995. Reexamination of the '336 patent has been requested six times: (i) Request No. 90/008,237 on November 17, 2006; (ii) Request No. 90/008,306 on October 19, 2006; (iii) Request No. 90/008,474 on January 30, 2007; (iv) Request No. 90/009,457 on August 24, 2009; (v) Request No. 90/010,551 on May 26, 2009; and (vi) Request No. 90/011,168 on August 20, 2010. On December 15, 2009, the U.S. Patent & Trademark Office ("USPTO") issued an Ex Parte Reexamination Certificate, confirming the patentability of claims 1, 6, and 10, as amended during reexamination, dependent claims 2, 7, 9, and new claims 11-16. JXM-0001, '336 patent, at TPL853_000000053. Claims 1, 6, 7, 9-11, and 13-16 of the '336 patent, as amended or added through reexamination, are asserted in this Investigation. *See* 77 Fed. Reg. 51572-73 (August 24, 2012) ("Notice of Investigation").

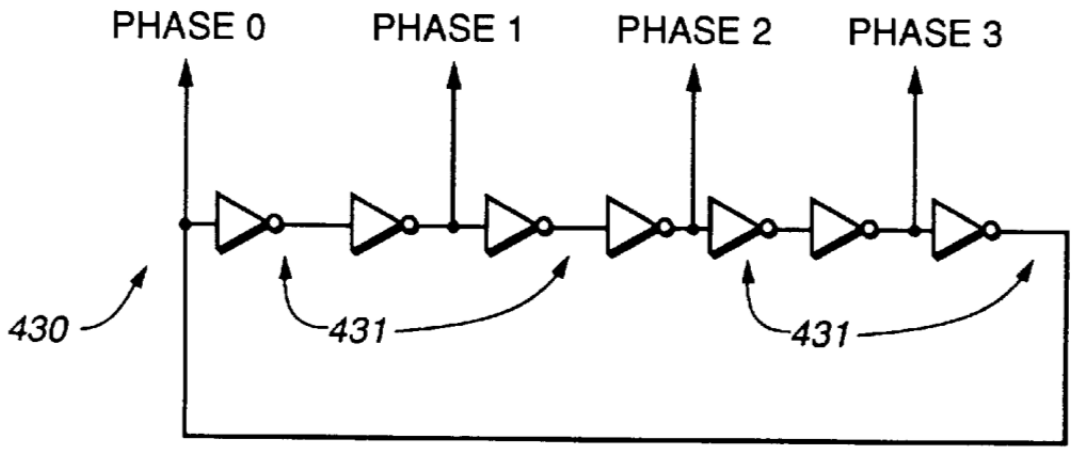
The '336 patent discloses a high-performance microprocessor system using a variable speed system clock employing an optimal CPU clock scheme. JXM-0001, '336 patent, Abstract, Figs. 17-19, col. 16:43-17:10. According to the patent, conventional CPU designs "must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in wors[t] case conditions." JXM-0001, '336 patent, col. 16:50-53. "Temperature, voltage, and process [variations] all affect transistor propagation delays," and thus maximum CPU clock speed. *See id.* at col. 16:47-48. However, by implementing the system clock entirely on-chip using a ring oscillator, variations in temperature, voltage, and process will affect the ring oscillator in the same manner as they affect the processor. *See id.* at col. 16:59-17:10. Accordingly, "CPU 70 (as shown below in Fig. 17) will always execute at the maximum frequency possible, but never too fast." *Id.* at 17:1-2. This concept is depicted in Figure 17, which shows a ring oscillator variable speed clock 430 and a CPU 70 that are implemented on the same chip:



JXM-0001, '336 patent, Fig. 17. In addition to the on-chip system clock, Fig. 17 depicts an

external crystal clock 434 for use in synchronizing input/output ("I/O") communications with the external memory bus. JXM-0001, '336 patent, Fig. 17, 17:14-19.

According to the '336 patent, the ring oscillator variable speed clock 430 can be implemented using the type of ring oscillator shown in Fig. 18:



JXM-0001, '336 patent, Fig. 18. This bi-stable loop of seven inverters generates a clock signal at a speed that depends on the propagation delay through those inverters. *See id.* at col. 16:63-17:2. "At room temperature, the frequency will be in the neighborhood of 100 MHZ. At 70 degrees Centigrade, the speed will be 50 MHz." *Id.* at col. 16:60-63. Because the clock is implemented on-chip using the same transistors as the CPU, its performance varies with the CPU's performance, thus compensating for temperature, voltage, and process variations and allowing the CPU to operate at the highest possible speed. *See id.* at col. 16:59-17:10. The clock speed is determined solely by its operating parameters (*i.e.*, temperature, voltage, and process), as there are no mechanisms provided to otherwise vary or control its operating frequency. In this manner, the clock can sometimes be operated at speeds higher than worst case conditions would permit.

III. LEGAL STANDARDS

Claim construction is a matter of law exclusively for the court. *Cybor Corp. v. FAS Techs. Inc.*, 138 F.3d 1448, 1455-56 (Fed. Cir. 1998) (en banc); *Markman v. Westview Instruments Inc.*, 52 F.3d 969, 976 (Fed. Cir. 1995) (en banc) ("*Markman*"), *aff'd*, 116 S. Ct. 1384 (1996). The ordinary and customary meaning of the language of a claim to one of ordinary skill in the art at the time of the invention is the starting point for the analysis. *Phillips v. A.W.H. Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (en banc) ("*Phillips*"); *Alloc, Inc., v. U.S. International Trade Commission*, 342 F.3d 1361, 1368 (Fed. Cir. 2003) ("*Alloc*"). In short, "[t]he claims themselves provide substantial guidance as to the meaning of particular claim terms." *Phillips*, 415 F.3d at 1314; *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996) ("*Vitronics*"); *ACTV, Inc. v. The Walt Disney Co.*, 346 F.3d 1082, 1088 (Fed. Cir. 2003) ("*ACTV*") ("the context of the surrounding words of the claim also must be considered in determining the ordinary and customary meaning of those terms").

However, "the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Phillips*, 415 F.3d at 1313. The specification may act as a dictionary, explaining the invention and defining the terms used in the claims, but if a patentee is acting as his or her own lexicographer, any special definition given to a word must be clear in the specification. *Id*. at 1316; *Vitronics*, 90 F.3d at 1582-83. Moreover, the specification (and prosecution history) should not "enlarge, diminish or vary" the limitations of the claims. *Vitronics*, 90 F.3d at 1582-83; *Markman*, 52 F.3d at 979-80; *Intel Corp. v. U.S. International Trade Commission*, 946 F.2d 821, 836 (Fed. Cir. 1991) ("Where a specification does not require a limitation, that limitation should not be read from the specification into the claims."). Furthermore, every term in a claim is presumed to have meaning and any construction

that would render a claim term superfluous is discouraged. *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111 (Fed. Cir. 2004) ("While not an absolute rule, all claim terms are presumed to have meaning in a claim.") ("*Innova*"); *Cardiac Pacemakers, Inc. v. St. Jude Med., Inc.*, 296 F.3d 1106, 1115 (Fed. Cir. 2002) ("An alternative construction would render the first monitoring term meaningless. That construction is therefore improper; this court will not rewrite claims.").

In addition, the prosecution history "provides evidence of how the PTO and the inventor understood the patent." *Phillips*, 415 F.3d at 1317. As such, "it may inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Id.*; *Vitronics*, 90 F.3d at 1582-83; *see also Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) ("The purpose of consulting the prosecution history in construing a claim is to exclude any interpretation that was disclaimed during prosecution.").

Extrinsic evidence may also be considered, if needed, to assist in determining the meaning or scope of technical terms in the claims. *Phillips*, 415 F.3d at 1317-18; *Vitronics*, 90 F.3d at 1582-83. Expert testimony may be useful to "provide background on the technology at issue, to explain how an invention works, to ensure that the court's understanding of the technical aspects of the patent is consistent with that of a person of skill in the art, or to establish that a particular term in the patent or the prior art has a particular meaning in the pertinent field." *Phillips*, 415 F.3d at 1318. However, it remains the intrinsic record, including the specification and prosecution history, that is the most significant evidence and thus determinative for interpreting the legally operative meaning of patent claim language. *Id*. at 1317.

IV. DISCUSSION

TPL has asserted claims 1, 6, 7, 9-11, and 13-16 of the '336 patent in this investigation. *See* 77 Fed. Reg. 51572-73 (August 24, 2012) ("Notice of Investigation"). The parties have agreed to the meaning of the following term:

Term	Joint Construction
"second clock independent of said ring oscillator…system clock" (claims 1, 11)	a second clock wherein a change in the frequency of either the second clock or ring oscillator system clock does not affect the frequency of the other

This proposed construction reflects the plain and ordinary meaning of the term "independent," and is consistent with the intrinsic evidence. The Staff thus submits that this term should be interpreted to mean "a second clock wherein a change in the frequency of either the second clock or ring oscillator system clock does not affect the frequency of the other." Each disputed term is addressed below.

A. "an entire ring oscillator variable speed system clock in said single integrated circuit"/ "an entire oscillator/variable speed clock disposed upon said integrated circuit substrate"

The parties dispute the meaning of the phrases "an entire ring oscillator variable speed system clock in said single integrated circuit" in claim 1, "an entire oscillator disposed upon said integrated circuit substrate" in claims 6 and 13, and "an entire variable speed clock disposed upon said integrated circuit substrate in claims 10 and 16 of the '336 patent. Claim 1, which is representative, reads as follows:

> **Claim 1.** A microprocessor system, comprising a single integrated circuit including a central processing unit and ***an entire ring oscillator variable speed system clock in said single integrated circuit*** and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable

> speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit, and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.

JXM-0001, '336 patent, Ex Parte reexamination Certificate, US 5,809,336 C1, col. 1:59-2:11, at TPL853_00000052 (December 15, 2009) (emphasis added). The dispute over this limitation appears to turn primarily on the meaning of the term "entire." Yet neither TPL nor Respondents attempt to define that term, as demonstrated by the parties' proposed constructions:

Term	Proposed Constructions		
	Complainants	**Respondents**	**Staff**
"an entire ring oscillator variable speed system clock in said single integrated circuit" (claim 1)	a ring oscillator, variable speed system clock, wherein the ring oscillator is located entirely on the same semiconductor substrate as the central processing unit	a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an external crystal/clock generator to generate a clock signal	a ring oscillator variable speed system clock that includes all components that determine clock frequency located on the same semiconductor substrate as the CPU
"an entire oscillator disposed upon said integrated circuit substrate" (claims 6 and 13)	an oscillator that is located entirely on the same semiconductor substrate as the central processing unit	an oscillator that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an external crystal/clock generator to generate a clock signal	an oscillator that includes all components that determine oscillator frequency located on the same semiconductor substrate as the CPU
"an entire variable speed clock disposed upon said integrated circuit substrate" (claims 10 and	a variable speed clock that is located entirely on the same semiconductor substrate as the central processing unit	a variable speed clock that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an	a variable speed clock that includes all components that determine clock frequency located on the same semiconductor substrate as the CPU

16)		external crystal/clock generator to generate a clock signal	

During prosecution of the application that resulted in the '336 patent, the patentee amended the claims so as to distinguish U.S. Patent No. 4,503,500 ("Magar"). Magar discloses an on-chip clock generator that relies upon off-chip components to determine clock frequency, namely, an external crystal, which was allegedly distinct from the claimed invention. JXM-0002, at TPL853_00002401 ("In response, the independent claims have been rewritten to specify that the entire ring oscillator variable speed system clock, variable speed clock or oscillator be provided in the integrated circuit, in order to sharpen the distinction over prior art. Because the prior art does not provide an entire ring oscillator variable speed system clock, variable speed clock or oscillator in the integrated circuit, in that the prior art circuits require an external crystal, the prior art fails to teach or suggest the invention now claimed."). The patentee further explained that "[a]s a self-contained on-chip circuit, Magar's clock gen is distinguished from an oscillator in at least that it lacks the crystal or external generator that it requires." *Id.* at TPL853_00002402.

Similarly, in distinguishing U.S. Patent No. 4,670,837 ("Sheets"), the patentee asserted that "[t]he present invention does not [] rely upon provision of frequency control information to an external clock, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, since the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *Id.* at TPL853_00002473.

Complainants' proposed construction is improper to the extent that it fails to reflect these disclaimers. And while Respondents' proposed construction appears to accurately capture the patentee's clear disclaimer, Respondents still have not offered a construction for the term "entire." Incorporating a proper construction of the term "entire" excludes the disclaimed disclaimer, because the prior art distinguished by patentee does not disclose an entire oscillator in the same integrated circuit as a microprocessor. Indeed, both Magar and Sheets disclose oscillators relying upon off-chip components to determine frequency. The Staff therefore believes that its constructions better capture the meaning of the disputed phrases, as they would be understood by one of ordinary skill in the art.

For at least these reasons, the Staff respectfully submits that the phrase "an entire ring oscillator variable speed system clock in said single integrated circuit" should be interpreted to mean "a ring oscillator variable speed system clock that includes all components that determine clock frequency located on the same semiconductor substrate as the CPU," the phrase "an entire oscillator disposed upon said integrated circuit substrate" should be interpreted to mean "an oscillator that includes all components that determine oscillator frequency located on the same semiconductor substrate as the CPU," and the phrase "an entire variable speed clock disposed upon said integrated circuit substrate" should be interpreted to mean "a variable speed clock that includes all components that determine clock frequency located on the same semiconductor substrate as the CPU."

B. "central processing unit"

The parties dispute the meaning of the phrase "central processing unit" in claims 1, 6, 10, 11, 13, and 16 of the '336 patent. Claim 1, which is representative, reads:

> **Claim 1.** A microprocessor system, comprising a single integrated circuit including a ***central processing unit*** and an entire ring oscillator variable speed system clock in said single integrated circuit and connected

> to said ***central processing unit*** for clocking said ***central processing unit***, said ***central processing unit*** and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said ***central processing unit*** and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit, and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.

'336 patent, Ex Parte reexamination Certificate, US 5,809,336 C1, col. 1:59-2:11 (December 15, 2009) (emphasis added). This phrase was construed in prior litigation by Judge Ward to mean "an electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions." SXM-0001, App., Tab 1, at 0009, *Technology Properties Ltd. v. Matsushita Electric Industrial Co., Ltd.*, Case No. 2:05cv494, Memorandum Opinion and Order at 9 (E.D. Tex. June 15, 2007) ("*Markman* Order I"). Consistent with Judge Ward's construction, TPL represented to the U.S. District Court for the Northern District of California ("N.D. Cal.") on October 29, 2010 that the phrase "central processing unit" should be construed to mean "electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions." *See* SXM-0004, App., Tab 4, at 0065.

However, TPL now take a contrary position seeking to remove a limitation dictated by the plain language of the claim. On the other hand, Respondents propose a construction that is consistent with: (i) the plain language of the claim; (ii) Judge Ward's prior construction; and (iii) TPL's agreed construction before N.D. Cal. In this regard, the Staff agrees with Respondents. The parties' proposed constructions are as follows:

Term	Proposed Constructions		
	Complainants	**Respondents**	**Staff**
"central processing unit" (claims 1, 6, 10, 11, 13, 16)	**No construction necessary. But if construed:** electronic circuit that controls the interpretation and execution of programmed instructions	electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions	electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions

The parties' proposed constructions differ in only one respect—whether the claimed "central processing unit" must be located on an integrated circuit. In this regard, the plain language of the claim is determinative. Claim 1 recites "a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit." Thus, the plain language of the claim dictates that the "central processing unit" is included on the claimed integrated circuit.

Accordingly, the Staff submits that phrase "central processing unit" should be interpreted to mean "electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions."

C. "wherein said central processing unit operates asynchronously to said input/output interface"

The private parties dispute the meaning of the phrase "wherein said central processing unit operates asynchronously to said input/output interface" in claims 11, 13, and 16 of the '336 patent. Claim 11, which is representative, reads as follows:

> **Claim 11.** A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central

> processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, ***wherein said central processing unit operates asynchronously to said input/output interface***.

JXM-0001, '336 patent, Ex Parte reexamination Certificate, US 5,809,336 C1, col. 3:7-26 (December 15, 2009) (emphasis added). On June 12, 2012, Judge Ware construed this phrase to mean "the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them." SXM-0002, App., Tab 2, at 0049 ("*Markman* Order II").

The private parties now disagree as to whether the phrases "independently of" and "not derived from" have the same meaning. However, it is unclear to the Staff whether the parties have an actual, substantive dispute. Unless TPL provides compelling reasons to do otherwise, the Staff agrees with Respondents and proposes that this phrase be construed consistently with Judge Ware's prior construction. The parties' proposed constructions are as follows:

Term	**Proposed Constructions**		
	Complainants	**Respondents**	**Staff**
"wherein said central processing unit operates asynchronously to said input/output interface" (claims 11, 13, 16)	the timing control of the central processing unit operates independently of (not derived from) the timing control of the input/output interface such that there is no readily predictable phase relationship between them	the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them	the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them

Accordingly, should it be construed, the Staff submits that the phrase "wherein said central processing unit operates asynchronously to said input/output interface" should be interpreted to mean "the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them."

D. "varying together/varying in the same way/varying…in the same way"

The parties dispute the meaning of the phrase "varying together" in claims 1 and 11, the phrase "varying in the same way" in claims 10 and 16, and the phrase "varying…in the same way" in claims 6 and 13 of the '336 patent. However, the parties agree that each of these phrases should be given the same meaning. Claim 1, which is representative, reads:

> **Claim 1.** A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock ***varying together*** due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit, and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.

JXM-0001, '336 patent, Ex Parte reexamination Certificate, US 5,809,336 C1, col. 1:59-2:11, at TPL853_00000052 (December 15, 2009) (emphasis added). In prior litigation, Judge Ward construed these phrases to mean "increasing and decreasing proportionally." App., Tab. 1, *Markman* Order I, at 0015-16. TPL later agreed with this construction before the U.S. District

for the Northern District of California. SXM-0004, App., Tab 4, at 0068. However, TPL now proposes a similar, but slightly different construction.

It is unclear to the Staff whether the parties have an actual, substantive dispute concerning the meaning of this phrase. Unless TPL provides compelling reasons to do otherwise, the Staff agrees with Respondents and proposes that this phrase be construed consistently with Judge Ward's prior construction. The parties' proposed constructions are as follows:

Term	Proposed Constructions		
	Complainants	**Respondents**	**Staff**
"varying together" (claims 1, 11) "varying in the same way" (claims 10, 16) "varying…in the same way" (claims 6, 13)	**No construction necessary. But if construed:** changing in a corresponding manner	increasing and decreasing proportionally	increasing and decreasing proportionally

Accordingly, should these terms be construed, the Staff submits that phrases "varying together," "varying in the same way," and "varying…in the same way" should be interpreted to mean "increasing and decreasing proportionally."

E. "thereby enabling said processing frequency to track said clock rate in response to said parameter variation"

The parties dispute the meaning of the phrase "thereby enabling said processing frequency to track said clock rate in response to said parameter variation" in claims 6 and 13 of the '336 patent. Claim 6 reads as follows:

> **Claim 6.** A microprocessor system comprising:
> a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

> an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, ***thereby enabling said processing frequency to track said clock rate in response to said parameter variation***;
>
> an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and
>
> an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.

JXM-0001, '336 patent, Ex Parte reexamination Certificate, US 5,809,336 C1, col. 2:13-31, at TPL853_00000052 (December 15, 2009) (emphasis added). Within a larger context, the claim recites "varying the processing frequency…in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation." *Id.* at col. 2:22-31. In the prior litigation, the litigants disputed the required relationship between operational parameter variation and the clock rate. In this regard, Judge Ware considered the phrase "as a function of parameter variation." SXM-0002, App., Tab 2, *Markman* Order II, at 0046. Although he declined to construe that phrase, Judge Ware did find that "a person of ordinary skill in the art reading the patent would understand that the phrase 'as a function of' is describing a variable that depends on and varies with another." *Id.*

Here, as in the prior litigation, the parties dispute the nature of the relationship between operational parameter variation and the clock rate. Respondents contend that parameter variation directly causes the processing frequency to track the clock rate. However, TPL disputes that a

causal relationship is required. The Staff agrees with Respondents, as reflected in the parties' proposed constructions:

Term	Proposed Constructions		
	Complainants	**Respondents**	**Staff**
"thereby enabling said processing frequency to track said clock rate in response to said parameter variation" (claims 6, 13)	[thereby enabling] the processing frequency of the central processing unit to follow said clock rate in response to said parameter variation	said parameter variation directly causing said processing frequency to track said clock rate	said parameter variation directly causing said processing frequency to track said clock rate

The '336 patent disparages conventional CPU clocking techniques for failing to achieve maximum theoretical performance. JXM-0001, '336 patent, at col. 16:44-53. "Traditional CPU designs are done so that with the wors[t] case of the three parameters [(*i.e.*, temperature, voltage, and process variations)], the circuit will function at the rated clock speed." *Id.* at col. 16:48-50. As a result, conventional microprocessor systems "must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in wors[t] case conditions." *Id.* at col. 16:50-53.

As discussed above, in order to overcome this purported deficiency in prior art designs, the '336 patent proposes using a variable speed ring oscillator clock that is located entirely on the same integrated circuit as the microprocessor. *Id.* at 16:54-58. The frequency of the variable speed ring oscillator clock is determined, not by an external crystal or off-chip components, but by "the parameters of temperature, voltage, and process." *Id.* at col. 16:59-60. Accordingly, parameter variations affect the microprocessor performance and the clock speed in the same manner, and the disclosed clock inherently compensates for such parameter variations, such that

"CPU 70 will always execute at the maximum frequency possible, but never too fast." *Id.* at 17:1-2.

The purpose of the variable speed clock is thus to overcome deficiencies in the prior art that require designers to limit performance such that the system will correctly function under worst case conditions. *See id.* at col. 16:44-53. Accordingly, one of ordinary skill in the art at the time of invention would understand the invention as requiring direct causality between parameter variation and clock speed.

Moreover, the plain language of the claim requires direct causality between parameter variation and processing speed. The claim recites varying "the processing frequency…as a function of parameter variation." As stated above, Judge Ware found that "a person of ordinary skill in the art reading the patent would understand that the phrase 'as a function of' is describing a variable that depends on and varies with another." SXM-0002, App., Tab 2, *Markman* Order II, at 0046. Such a dependence gives rise to a direct causal relationship. Accordingly, the construction proposed by Respondents and the Staff is consistent with both the claim and the specification.

For the reasons set forth above, the Staff submits that the phrase "thereby enabling said processing frequency to track said clock rate in response to said parameter variation" should be interpreted to mean "said parameter variation directly causing said processing frequency to track said clock rate."

F. "on-chip input/output interface"

The parties dispute the meaning of the phrase "on-chip input/output interface" in claims 1, 6, 10, 11, 13, and 16 of the '336 patent. Claim 1, which is representative, reads as follows:

> **Claim 1.** A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected

> to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an ***on-chip input/output interface*** connected to exchange coupling control signals, addresses and data with said central processing unit, and a second clock independent of said ring oscillator variable speed system clock connected to ***said input/output interface***, wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.

JXM-0001, '336 patent, Ex Parte reexamination Certificate, US 5,809,336 C1, col. 1:59-2:11, at TPL853_00000052 (December 15, 2009) (emphasis added). Tthe parties' proposed constructions are as follows:

Term	Proposed Constructions		
	Complainants	**Respondents**	**Staff**
"on-chip input/output interface" (claims 1, 6, 10, 11, 13, 16)	**No construction necessary. But if construed:** a circuit for input/output communications, where that circuit is located on the same semiconductor substrate as the CPU	a circuit having logic for input/output communications, where that circuit is located on the same semiconductor substrate as the CPU	a circuit having logic for input/output communications, where that circuit is located on the same semiconductor substrate as the CPU

In prior District Court litigation, TPL agreed that the term "on-chip input/output interface" should be interpreted as now proposed by Respondents and the Staff. *See* SXM-0001, App., Tab 1, *Markman* Order I, at 0007-8. However, TPL now seeks a different construction that does not require that the on-chip input/output interface "have logic." Thus, under TPL's new construction, the "on-chip input/output interface" could arguably be met by a wire. But such a construction is inconsistent with the intrinsic evidence. The '336 patent provides very little description

regarding the claimed input/output interface. However, it is clear that the claimed I/O interface must perform synchronization:

> The external world must be synchronized to the microprocessor 50 for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface 432, speed of which is controlled by a conventional crystal clock 434. The interface 432 processes requests for memory accesses from the microprocessor 50 and acknowledges the presence of I/O data.

JXM-0001, '336 patent, at 17:22-29. Without logic to perform the requisite synchronization, the I/O interface would be unable "to exchange coupling control signals, addresses and data with said central processing unit" as claimed. TPL's construction is thus inconsistent both with the plain language of the claim and with the specification. To the contrary, Respondents and the Staff propose a construction that was agreed upon by TPL in prior litigation, and that broadly recites necessary structure (*i.e.*, "logic") without improperly importing limitations from the preferred embodiment.

For the reasons set forth above, the Staff submits that the phrase "on-chip input/output interface" should be interpreted to mean "a circuit having logic for input/output communications, where that circuit is located on the same semiconductor substrate as the CPU."

G. "external clock is operative at a frequency independent of a clock frequency of said oscillator/variable speed clock"

The parties dispute the meaning of the phrase "external clock is operative at a frequency independent of a clock frequency of said oscillator" in claims 6 and 13 of the '336 patent, and the meaning of the phrase "external clock is operative at a frequency independent of a clock frequency of said variable speed clock" in claims 10 and 16 of the '336 patent. Claim 6, which is representative, reads:

> **Claim 6.** A microprocessor system comprising:
>
> a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;
>
> an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;
>
> an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and
>
> an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip ***external clock is operative at a frequency independent of a clock frequency of said oscillator*** and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.

JXM-0001, '336 patent, Ex Parte reexamination Certificate, US 5,809,336 C1, col. 2:13-31, at TPL853_00000052 (December 15, 2009) (emphasis added). It is unclear to the Staff whether the parties have an actual, substantive dispute. The parties' proposed constructions are as follows:

Term	Proposed Constructions		
	Complainants	**Respondents**	**Staff**
"external clock is operative at a frequency independent of a clock frequency of said oscillator" (claims 6 and 13)	an external clock wherein a change in the frequency of either the external clock or oscillator does not affect the frequency of the other	an external clock wherein a change in the frequency of either the external clock or oscillator does not affect the frequency of the other	an external clock wherein a change in the frequency of either the external clock or the oscillator does not affect the frequency of the other
"external clock is operative at a frequency independent of a clock frequency of said variable speed clock"	an external clock wherein a change in the frequency of either the external clock or variable speed clock does not affect the frequency of the other	an external clock wherein a change in the frequency of either the external clock or on-chip variable speed clock does not affect the frequency of the	an external clock wherein a change in the frequency of either the external clock or the variable speed clock does not affect the frequency of the other

(claims 10 and 16)		other	

The parties have thus proposed substantially similar constructions that appear to differ in only one respect – the construction of the word "said." And with respect to this issue, the Staff submits that the term "said" would be understood by one of ordinary skill in the art to mean "aforementioned." *See* App., Tab 5, WEBSTER'S NINTH NEW COLLEGIATE DICTIONARY, at 0085 (1985); *see also In re Self*, 671 F.2d 1344, 1347 (C.C.P.A. 1982). Consistent with this definition, the Staff proposes that "said oscillator" and "said variable speed clock" be construed so as to properly refer back to those elements as previously recited in the claim, by construing those terms as "the oscillator" and "the variable speed clock." TPL's proposed constructions are improper to the extent that they fail to given any meaning to the term "said." *See Merck & Co., Inc. v. Teva Pharm. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) ("A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so.").

Accordingly, the Staff submits that the phrase "external clock is operative at a frequency independent of a clock frequency of said oscillator" should be interpreted to mean "an external clock wherein a change in the frequency of either the external clock or the oscillator does not affect the frequency of the other." The phrase "external clock is operative at a frequency independent of a clock frequency of said variable speed clock" should be interpreted to mean "an external clock wherein a change in the frequency of either the external clock or the variable speed clock does not affect the frequency of the other."

H. "ring oscillator"

The parties dispute the meaning of the phrase "ring oscillator" in claims 1, 9, 11, and 15 of the '336 patent. Claim 1 reads:

> **Claim 1.** A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ***ring oscillator*** variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ***ring oscillator*** variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ***ring oscillator*** variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit, and a second clock independent of said ***ring oscillator*** variable speed system clock connected to said input/output interface, wherein a clock signal of said second clock originates from a source other than said ***ring oscillator*** variable speed system clock.

JXM-0001, '336 patent, Ex Parte reexamination Certificate, US 5,809,336 C1, col. 1:59-2:11, at TPL853_00000052 (December 15, 2009) (emphasis added). On December 4, 2012, Magistrate Judge Paul S. Grewal issued an order construing "ring oscillator" to mean "an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment." SXM-0003, App., Tab 3, at 0053 ("*Markman* Order III").

Although TPL's proposed construction is consistent with the plain and ordinary meaning of the term, it improperly encompasses disclaimed subject matter. The Staff agrees with Judge Grewal and Respondents that the claimed ring oscillator must be variable based on the temperature, voltage and process parameters in the environment. However, Respondents' proposed construction is improper to the extent that it would require the oscillator to also be "noncontrollable." The parties' proposed constructions are as follows:

Term	**Proposed Constructions**		
	Complainants	**Respondents**	**Staff**
"ring oscillator" (claims 1, 9, 11,	interconnected electronic components	an oscillator having a multiple, odd number	an oscillator having a multiple, odd number

15)	comprising multiple odd numbers of inversions arranged in a loop, where three or more inversions are required to maintain an oscillating output	of inversions arranged in a loop, wherein the oscillator is: (1) noncontrollable; and (2) variable based on the temperature, voltage, and process parameters in the environment	of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment

The parties appear to essentially agree that the claimed "ring oscillator" is an oscillator having "multiple, odd numbers of inversions arranged in a loop," as this phrase appears in each proposed construction. However, the parties disagree as to existence and scope of a disclaimer arising from the reexamination of U.S. Patent No. 6,598,148 ("the '148 patent"). SXM-0006, App., Tab 6. The '148 patent was filed on July 29, 1998 as a division of the '918 application that resulted in the '336 patent. The asserted '336 patent and the '148 patent share essentially the same specification and drawings. During reexamination of the '148 patent, the patentee argued that U.S. Patent No. 4,689,581 ("Talbot") does not teach a ring oscillator. SXM-0007, App., Tab 7, February 21, 2008 Response, at 0144 ("Talbot does not teach, disclose, or suggest the ring oscillator recited in claim 4…. Talbot discloses a voltage-controlled oscillator (VCO) 12, but does not teach or disclose a ring oscillator. Talbot provides two different implementations of the VCO 12 in FIGS. 3-4, neither of which is a ring oscillator."). However, Talbot discloses an oscillator having a multiple, odd number of inversions arranged in a loop, as demonstrated in the following figure:

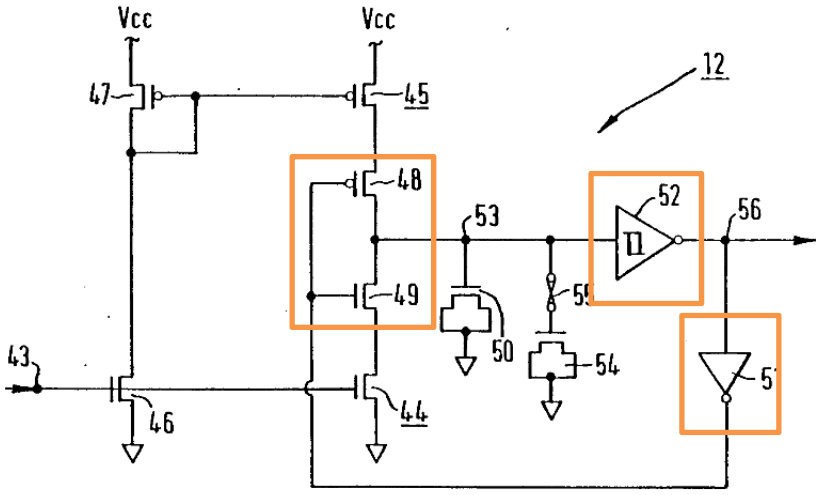


FIG. 3

Talbot, Fig. 3 (emphasis added). Each of the highlighted components shown in Figure 3 represents an inverting element. Thus, Talbot discloses three inversions arranged in a loop. Yet the patentee made clear, unequivocal statements that Talbot did not teach a ring oscillator. Thus, the patentee has disclaimed the subject matter set forth in Talbot. The only remaining question is the scope of this disclaimer.

Respondents assert that the patentee has disclaimed controllable ring oscillators based on patentee's representations distinguishing Talbot. However, the patentee did not argue that "controllability" was the reason that Talbot's oscillators were not the claimed "ring oscillators." Furthermore, Talbot can be distinguished fully based on the fact that the frequency of the variable speed ring oscillator clock of the '336 patent is determined, not by an external crystal or off-chip components, but by "the parameters of temperature, voltage, and process" as described

in the specification and articulated throughout the intrinsic record. *See* JXM-0001, '336 patent, at col. 16:59-60.

For at least these reasons, the Staff respectfully submits that the phrase "ring oscillator" should be interpreted to mean "an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment."

I. "clocking said central processing unit"

The parties dispute the meaning of the phrase "clocking said central processing unit" in claims 1, 6, 10, 11, 13, and 16 of the '336 patent. Claim 1, which is representative, reads as follows:

> **Claim 1.** A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for ***clocking said central processing unit***, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit, and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.

JXM-0001, '336 patent, Ex Parte reexamination Certificate, US 5,809,336 C1, col. 1:59-2:11, at TPL853_00000052 (December 15, 2009) (emphasis added). The parties dispute with respect to this limitation is whether the invention requires that the CPU be clocked at maximum speed. In *Markman* Order II, Judge Ware stated:

> A further issue tendered with respect to this phrase is whether, based on the written description, the construction should include a limitation of the maximum or optimum frequency of the "clocking" function. In the written description of the '336 Patent, the phrase "maximum frequency possible" is used with respect to an embodiment. A description of an embodiment in the specification may not be imposed as a limitation "unless the patentee has demonstrated a clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'" *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 111 (Fed. Cir. 2004) (citation omitted). Here, the Court finds that the cited language does not demonstrate "a clear intention to limit the claim scope." *Id.*

SXM-0002, App., Tab 2, *Markman* Order II, at 0045-46 (footnote omitted). According, Judge Ware construed "clocking said central processing unit" to mean "providing a timing signal to said central processing unit." The Staff agrees with Complainants and Judge Ware that a "maximum speed" limitation should not be imported from the specification. The parties' proposed constructions are as follows:

Term	Proposed Constructions		
	Complainants	**Respondents**	**Staff**
"clocking said central processing unit" (claims 1, 6, 10, 11, 13, 16)	providing a timing signal to said central processing unit	timing the operation of the CPU such that it will always execute at the maximum speed possible, but never too fast	providing a timing signal to said central processing unit

1. The Staff's Construction is Consistent with the Plain Language of the Claims, the Intrinsic Record of the '336 Patent, and Prior *Markman* Orders

The specification of the '336 patent describes an embodiment of a microprocessor system using clocking techniques that overcome prior art limitations requiring that clock speeds be restricted based on worst-case conditions. JXM-0001, '336 patent, at col. 15:44-53. According to the patent:

> The microprocessor 50 uses the technique shown in Figs. 17-19 to generate the system clock and its required phases. Clock circuit 430 is the familiar "ring oscillator" used to test process performance. The clock is fabricated on the same silicon chip as the rest of the microprocessor 50.

Id. at col. 16:54-58. Although the disclosed clocking technique purportedly allows a microprocessor to be clocked at optimal speed, the specification does not express a clear intent to so limit the claims. *See id.* Based on the disclosure, it is possible for a designer to vary clock speed by changing the number of inverters used in the ring inverter. *See* JXM-0001, '336 patent, at Fig. 18. This disclosure is consistent with the construction proposed by TPL and the Staff, and adopted by Judge Ware in *Markman* Order II. *See* SXM-0002, App., Tab. 2, *Markman* Order II, at 0045-46. Moreoever, the plain language of the claim does not require or even suggest that the CPU must be clocked at the maximum speed possible. Instead, the speed of the disclosed clock is dependent on the propagation delay of the ring oscillator. Should too few inverters be used, the clock would oscillate too fast, and should too many inverters be used, the microprocessor would operate sub-optimally. In light of the plain language of the claim and the intrinsic evidence, the Staff's proposed construction is thus correct.

2. Respondents' Proposed Construction is Flawed

Respondents' construction, in contrast, attempts to import limitations from a disclosed embodiment into the claims. Such a construction is improper in the absence of an expression of intent by the patentee. *Phillips*, 415 F.3d at 1323; *Vitronics*, 90 F.3d at 1582-83; *Markman*, 52 F.3d at 979-80; *Intel Corp. v. U.S. International Trade Commission*, 946 F.2d at 836 ("Where a specification does not require a limitation, that limitation should not be read from the specification into the claims.").

Respondents contend that "clocking said central processing unit" should be construed to mean "timing the operation of the CPU such that it will always execute at the maximum speed possible, but never too fast." In this regard, the specification describes an optimal CPU clock scheme such that "CPU 70 will always execute at the maximum frequency possible, but never too fast." JXM-0001, '336 patent, at col. 17:1-2. Moreover, the specification states that using

conventional clock schemes, microprocessors "must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse case conditions." *Id.* at col. 16:50-53. But while the '336 patent describes a design that purports to operate at the maximum frequency possible, the Staff does not believe that the intrinsic evidence shows an express intent to import this limitation. *See Thorner v. Sony Computer Entertainment America, LLC*, 669 F.3d 1362, 1368 (Fed. Cir. 2012) ("*Thorner*") ("It is … not enough that the only embodiments, or all of the embodiments, contain a particular limitation. We do not read limitations from the specification into claims; we do not redefine words."). Thus, Respondents' proposed construction is improper.

3. Conclusion

For at least these reasons, the Staff respectfully submits that the phrase "clocking said central processing unit" should be interpreted to mean "providing a timing signal to said central processing unit."

V. CONCLUSION

For all of the foregoing reasons, the Staff respectfully submits that the disputed claim terms should be construed as set forth above.

Respectfully Submitted,

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February 8, 2013

Certain Wireless Consumer Electronics Devices and Components Thereof **Investigation No. 337-TA-853**

CERTIFICATE OF SERVICE

The undersigned certifies that on February 8, 2013, he caused the foregoing **COMMISSION INVESTIGATIVE STAFF'S INITIAL MARKMAN BRIEF** to be served by hand upon Administrative Law Judge E. James Gildea (2 copies) and served upon the parties (1 copy each) in the manner indicated below:

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