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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

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CENTRAL REEXAMINATION UNIT

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/008,227*.

PATENT NO. *6598148*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Office Action in Ex Parte Reexamination	Control No. 90/008,227	Patent Under Reexamination 6598148	
	Examiner JOSEPH R. POKRZYWA	Art Unit 3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

a☒ Responsive to the communication(s) filed on *26 February 2008* . b☐ This action is made FINAL.
c☐ A statement under 37 CFR 1.530 has not been received from the patent owner.

A shortened statutory period for response to this action is set to expire 2 month(s) from the mailing date of this letter. Failure to respond within the period for response will result in termination of the proceeding and issuance of an *ex parte* reexamination certificate in accordance with this action. 37 CFR 1.550(d). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).** If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☒ Information Disclosure Statement, PTO/SB/08.
3. ☐ Interview Summary, PTO-474.
4. ☐ _____.

Part II SUMMARY OF ACTION

1a. ☒ Claims *4,7,8,10 and 14-25* are subject to reexamination.
1b. ☒ Claims *1-3,5,6,9 and 11-13* are not subject to reexamination.
2. ☐ Claims _____ have been canceled in the present reexamination proceeding.
3. ☐ Claims _____ are patentable and/or confirmed.
4. ☒ Claims *4,7,8,10 and 14-25* are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ The drawings, filed on _____ are acceptable.
7. ☐ The proposed drawing correction, filed on _____ has been (7a)☐ approved (7b)☐ disapproved.
8. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
   a)☐ All b)☐ Some* c)☐ None of the certified copies have
   1☐ been received.
   2☐ not been received.
   3☐ been filed in Application No. _____ .
   4☐ been filed in reexamination Control No. _____.
   5☐ been received by the International Bureau in PCT application No. _____.
   * See the attached detailed Office action for a list of the certified copies not received.
9. ☐ Since the proceeding appears to be in condition for issuance of an *ex parte* reexamination certificate except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte* Quayle, 1935 C.D. 11, 453 O.G. 213.
10. ☐ Other: _____

cc: Requester (if third party requester)

DETAILED ACTION

Response to Amendment

1. **Claims 4, 7, 8, and 10** of U.S. Patent Number 6,598,148 (hereafter "the '148 Patent") were requested to be reexamined, and were each rejected in an Office action dated 12/21/07. Continuing, in the response dated 2/26/08, the Patent Owner argues that the references utilized in the above noted rejection do not particularly teach the claimed invention, and further adds new **claims 14-25**. Thus, currently, **claims 4, 7, 8, 10, and 14-25** are the subject of this reexamination.

Information Disclosure Statement

2. First, it is noted that the numerous Court documents submitted on 5/27/08 are acknowledged by the examiner. However, the citations of the various Court papers and documents, as listed in the Information Disclosure Statement dated 5/27/08, within the "Other Prior Art – Non Patent Literature Documents" section, have been indicated as having a line through their citations. The indicated Court documents are not considered as "Prior Art" documents, since the Court documents are each dated in the years 2007 and 2008, which is after the publication date of the '148 Patent being Jul. 22, 2003, and is not prior to the effective filing date of the '148 Patent of Aug. 3, 1989. Thus, the citations of these Court documents should not be listed in the Information Disclosure Statement.

3. Similarly, the numerous Patent Office papers of related reexamination proceedings are also listed in the Information Disclosure Statement dated 5/27/08, whereby these documents are also not considered as "Prior Art", as the dates are after the publication date of the '148 Patent being Jul. 22, 2003, and not before the effective filing date of the '148 Patent. Thus, the citations of these documents should not be listed in the Information Disclosure Statement, and have been indicated as having a line through their citations.

4. Further, the Information Disclosure Statement dated 5/27/08 includes documents that have no clear date (such as Citation Nos. CY, CZ, DC, and DF), and also documents (such as Citation No. EK-EO, being reports regarding U.S. Pat. 5,440,749) that have dates that are later than the publication dated of the '148 Patent, being July 22, 2003, and being after the effective filing date of the '148 Patent. Thus, these documents cannot be considered as prior art, since a date cannot be established so as to be considered as "prior art".

5. With this, there are numerous other references listed in the Information Disclosure Statement submitted on 5/27/08, which have been considered by the examiner (see attached PTO/SB/08).

6. However, the examiner notes that MPEP 2256, under the heading "Prior Art Patents and Printed Publications Reviewed by Examiner in Reexamination" states, in part:

> Where patents, publications, and other such items of information are submitted by a party (patent owner or requester) in compliance with the requirements of the rules, **the requisite degree of consideration to be given to such information will be normally limited by the degree to which the party filing the information citation has explained**

> **the content and relevance of the information**. The initials of the examiner placed adjacent to the citations on the form PTO/SB/08A and 08B or its equivalent, without an indication to the contrary in the record, do not signify that the information has been considered by the examiner any further than to the extent noted above. [emphasis added]

Further, MPEP 609.05(b) states:

> The information contained in information disclosure statements which comply with both the content requirements of 37 CFR 1.98 and the requirements, based on the time of filing the statement, of 37 CFR 1.97 will be considered by the examiner. Consideration by the examiner of the information submitted in an IDS means that **the examiner will consider the documents in the same manner as other documents in Office search files are considered by the examiner while conducting a search of the prior art in a proper field of search**. The initials of the examiner placed adjacent to the citations on the ** PTO/SB/08A and 08B or its equivalent mean that the information has been considered by the examiner to the extent noted above. [emphasis added]

With this, the examiner notes that with the large number of references submitted in the above noted PTO/SB/08A, the references were considered to at least the "degree to which the party filing the information citation has explained the content and relevance of the information", and in "the same manner as other documents in Office search files are considered by the examiner while conducting a search of the prior art in a proper field of search".

Response to Arguments

7. Patent Owner's arguments, filed 2/26/08, with respect to the rejection(s) of **claim(s) 4, 7, 8, and 10** under 35 U.S.C.103(a) as being unpatentable over U.S. Patent Number 4,689,581, issued to Talbot, Gerald R. (referred to as "Talbot'581") in view of European Patent Publication EP 0 113 516, issued to May, Michael D., being European Patent Application No. 83307078.2 (referred to as "May'516"), have been fully considered and are persuasive. Therefore, the rejection, as cited in the previous Office action, has been withdrawn.

8. Particularly, the references of Talbot'581 and May'516 do not particularly show that "said memory further occupying a majority of a total area of said single substrate". Patent Owner's arguments on pages 8 through 12 discuss how these references teach that the disclosed memory may be the largest component on the substrate, but this may not be a majority of the total area of the substrate. Further, the reference of Talbot'518 describes an oscillator circuit, but the specific features are unclear if the components actually make a ring oscillator.

9. However, upon further consideration, a new ground(s) of rejection is made in view of Kajigaya *et al.* (U.S. Patent Number 4,956,811), with a full discussion appearing below.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

11. **Claims 15-25** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

12. With respect to each of the newly added dependent claims, upon review of the specification of the '148 Patent, the examiner cannot find a description or indication that the oscillator/clock 316 seen in Fig. 9 is actually a ring oscillator. Further, the examiner cannot find a specific description of the memory having a specific area being just larger than twice, three times, or four times as large as the processing unit and the ring oscillator combined. Additionally, there is no description that the total area is actually just "the sum of active areas" of the substrate, nor is there a description that the total area is an area provided by an entire top surface of the single substrate.

13. Particularly, as seen in Figs. 7 and 8 of the '148 Patent, the die includes a crystal oscillator clock 282, which is noted as the Motorola 50 MegaHertz crystal oscillator clock. However, this would not be the same as a ring oscillator on the same substrate as that seen in

Fig. 9. Further, the specification of the '148 Patent describes the ring oscillator in col. 14, lines 37-60, and further states that "The clock is fabricated on the same silicon chip as the rest of the microprocessor 50." However, in Fig. 9, "clock/timing 316" is shown. The examiner cannot find in the specification of the '148 Patent where the circuit of clock/timing 316 shown in Fig. 9 is described. The specification does describe the CPU 316, in col. 10, lines 54-59, being the same component number as that of clock/timing 316, but the CPU s shown as item 314. However, the ALU, the Instruction Decode and the Clock/Timing are each seen as item 316. Is the clock 316, the ALU 316, and the instruction decode 316 each the same component?

14. But the '148 Patent specification describes a microprocessor 310, whereby in col. 6, lines 49-65, the '148 Patent states that "Fig. 9 shows another microprocessor 310 that is provided integrally with 1 megabit of DRAM 311 in a single integrated circuit 312...The microprocessor 310 is equivalent to the microprocessor 50 in Figs. 1-8." Continuing, the examiner notes that in Fig. 9, there is no microprocessor 310 labeled, as the processors of the ALU 316 and the DMA CPU 314 shown and described in col. 10, lines 43-67. With these sections, it appears that the entire drawing of Fig. 9 is referred to as microprocessor 310, which can thus replace that of microprocessor 50 seen within the layout diagram of Fig. 7, which is described as including a "clock is fabricated on the same silicon chip as the rest of the microprocessor 50".

15. However, as further described in col. 8, lines 62-67, the '148 Patent states "There are certain differences between the microprocessor 310 and the microprocessor 50 that arise from providing the microprocessor 310 on the same die 312 with the DRAM 311. Integrating the

DRAM 311 allows architectural changes in the microprocessor 310 logic to take advantage of existing on-chip DRAM 311 circuitry." Thus, while the microprocessor 310 and 50 may be equivalent, there are differences because of the "architectural changes in the microprocessor 310".

16. As discussed on pages 12 and 13 of the arguments, the Patent Owner relies on Fig. 9 as supporting each of the newly added claims. However, the examiner notes that the added claims include a range that the memory occupies an area greater than two times, greater than three times, or greater than four times the area occupied by the processing unit and the ring oscillator. First, the drawing in Fig. 9 does not teach these ranges. Referring to Fig. 9, there is no clear teaching of the area that the processing unit and the ring oscillator actually occupies. Further, there is no clear teaching of the memory occupying each of the possible ranges. For instance, there is no teaching that the memory occupies an area just over two times the area of a processing unit and oscillator combined. Continuing, there is no clear teaching that the total area only consists of active areas on the substrate. There is no discussion of active areas or inactive areas, and what would be considered an "active area". Additionally, there is no clear teaching that the total area refers to an entire top surface of the substrate.

17. Thus, the newly added claims 15-25 contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim Rejections - 35 USC § 102

18. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

19. **Claims 4, 7, 8, 10, and 14-25** are rejected under 35 U.S.C. 102(e) as being anticipated by Kajigaya *et al.* (U.S. Patent Number 4,956,811, hereafter "Kajigaya").

Regarding independent ***claim 4***, Kajigaya teaches of a microprocessor integrated circuit [see col. 3, lines 44-60, wherein "Circuit elements constituting each block shown in Fig. 32 and each of the circuit elements shown in Figs. 1-30 are, although not necessarily limitative, formed on a single semiconductor substrate such as a single crystal silicon by a known semiconductor integrated circuit manufacturing technique."] comprising:

a processing unit disposed upon an integrated circuit substrate [PC2, which includes for instance, "redundant address control circuit RAC", as read on col. 15, lines 10-23, and seen in Figs. 32 and 33; also see Figs. 23 and 24, being "circuit diagrams showing one example of a redundant address control circuit of a dynamic type RAM to which the present invention is applied", as noted in col. 3, lines 10-13],

said processing unit operating in accordance with a predefined sequence of program instructions [see col. 4, lines 18-44, whereby when the DRAM is adapted for the x 1 bit pattern, the operating modes are programmed as "a first page mode, static column mode, nybble mode, and serial mode", and when the DRAM is adapted for the x 4 bit pattern, the operating modes are programmed as "first page mode, static column mode and serial mode, and mask write mode"; also see col. 15, lines 24-51];

a memory coupled to said processing unit and capable of storing information provided by said processing unit [memory arrays MARY0-MARY3, also see Figs. 32 and 33],

said memory occupying a larger area of said integrated circuit substrate than said processing unit said memory further occupying a majority of a total area of said single substrate [see Fig. 33, whereby memory arrays MARY0-MARY3 occupy the majority of the total area of the substrate]; and

a ring oscillator having a variable output frequency [see col. 12, lines 55-58, wherein "Each of the substrate back bias voltage generating circuits includes a ring oscillator having five CMOS inverter circuits..."; also see Fig. 6, whereby the timing generating circuit TG includes a plurality of odd number of inverters, being the defining feature of a ring oscillator],

wherein the ring oscillator provides a system clock to the processing unit [see Fig. 6, being the timing generating circuit TG],

the ring oscillator disposed on said integrated circuit substrate [see col. 12, lines 55-58, wherein "Each of the substrate back bias voltage generating circuits includes a ring oscillator having five CMOS inverter circuits...", also see col. 15, lines 10-23, wherein "At one end of the semiconductor substrate SUB, ...a peripheral circuit PC1 which includes the timing generating circuit TG...is disposed between the pads TF to A9 and the memory arrays MARY0 to MARY3."].

Regarding ***claim 7***, Kajigaya discloses the microprocessor integrated circuit discussed above in claim 4, and further teaches that said memory is capable of supporting read and write operations [see col. 4, line 45-col. 5, line 10; also see col. 15, lines 24-51].

Regarding independent ***claim 8***, Kajigaya teaches of a microprocessor integrated circuit [see col. 3, lines 44-60, wherein "Circuit elements constituting each block shown in Fig. 32 and each of the circuit elements shown in Figs. 1-30 are, although not necessarily limitative, formed on a single semiconductor substrate such as a single crystal silicon by a known semiconductor integrated circuit manufacturing technique."] comprising:

a processing unit having one or more interface ports for interprocessor communication [for instance PC2, which a "redundant address control circuit RAC", as read on col. 15, lines 10-23, and seen in Figs. 32 and 33; also see Figs. 23 and 24, being "circuit diagrams showing one example of a redundant address control circuit of a dynamic type RAM to which the present

invention is applied", as noted in col. 3, lines 10-13, whereby the RAC includes various ports for interprocessor communication],

said processing unit disposed upon an integrated circuit substrate [see Figs. 32 and 33, whereby the PC2, which includes a "redundant address control circuit RAC" is disposed on the single substrate with the DRAM],

a memory disposed upon said substrate and coupled to said processing unit [memory arrays MARY0-MARY3, also see Figs. 32 and 33],

said memory occupying a greater area of said substrate than said processing unit, said memory further comprising a majority of a total area of said substrate [see Fig. 33, whereby memory arrays MARY0-MARY3 occupy the majority of the total area of the substrate]; and

a ring oscillator having a variable output frequency [see col. 12, lines 55-58, wherein "Each of the substrate back bias voltage generating circuits includes a ring oscillator having five CMOS inverter circuits..."; also see Fig. 6, whereby the timing generating circuit TG includes a plurality of odd number of inverters, being the defining feature of a ring oscillator],

wherein the ring oscillator provides a system clock to the processing unit [see Fig. 6, being the timing generating circuit TG],

the ring oscillator disposed on said substrate [see col. 12, lines 55-58, wherein "Each of the substrate back bias voltage generating circuits includes a ring oscillator having five CMOS inverter circuits...", also see col. 15, lines 10-23, wherein "At one end of the semiconductor substrate SUB, ...a peripheral circuit PC1 which includes the timing generating circuit TG...is disposed between the pads TF to A9 and the memory arrays MARY0 to MARY3."].

Regarding ***claim 10***, Kajigaya discloses the microprocessor integrated circuit discussed above in claim 8, and further teaches of including memory controller means coupled to said memory for performing direct memory access data transfer through said one or more interface ports [see col. 4, line 45-col. 5, line 10; also see col. 9, line 47-col. 10, line 18; also see col. 15, lines 24-51].

Regarding ***claims 14 and 20***, Kajigaya discloses the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and further teaches that the memory comprises a plurality of physically separate memory portions [see Figs. 32 and 33, being memory arrays MARY0, MARY1, MARY2, and MARY3].

Regarding ***claims 15 and 21***, Kajigaya discloses the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and further teaches that the memory occupies an area greater than twice as large as an area occupied by the processing unit and the ring oscillator combined [see Figs. 32 and 33].

Regarding ***claims 16 and 22***, Kajigaya discloses the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and further teaches that the memory occupies an area greater than three times as large as an area occupied by the processing unit and the ring oscillator combined [see Figs. 32 and 33].

Regarding ***claims 17 and 23***, Kajigaya discloses the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and further teaches that the memory occupies an area approximately four times as large as an area occupied by the processing unit and the ring oscillator combined [see Figs. 32 and 33].

Regarding ***claims 18 and 24***, Kajigaya discloses the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and further teaches that the total area consists of a sum of active areas of the single substrate comprising circuit elements of the integrated circuit [see Figs. 32 and 33, also see col. 14, lines 52-65, wherein "the dynamic type RAM is, although not necessarily limitative, formed on a semiconductor substrate SUB which is defined by one single crystal silicon."].

Regarding ***claims 19 and 25***, Kajigaya discloses the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and further teaches that the total area is an area provided by an entire top surface of the single substrate [see Fig. 33, also see col. 14, lines 52-65, wherein "the dynamic type RAM is, although not necessarily limitative, formed on a semiconductor substrate SUB which is defined by one single crystal silicon."].

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. **Claims 4, 7, 8, and 14-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over "A 5V Self-Adaptive Microcomputer with 16Kb of E2 Program Storage and Security", written by Mark Bagula et al., 1983 IEEE International Solid-State Circuits Conference, pages 34-35 (hereafter "Bagula") in view of Hashimoto *et al.* (U.S. Patent Number 4,882,710, hereafter "Hashimoto").

Regarding independent ***claim 4***, Bagula teaches of a microprocessor integrated circuit [see Figs. 1-4] comprising:

a processing unit disposed upon an integrated circuit substrate [see Fig. 4, "ALU and Temp Reg."],

said processing unit operating in accordance with a predefined sequence of program instructions [see page 34, col. 1, wherein "This architecture was chosen as the basis for this circuit because its microcoded instruction set and generalized building block type layout greatly facilitated the instruction set change and control circuit modifications necessary to implement EEROM memory"];

a memory coupled to said processing unit and capable of storing information provided by said processing unit [being the Microcode ROM , RAM and EEPROM Arrays, which comprise 48% of the die area],

said memory occupying a larger area of said integrated circuit substrate than said processing unit said memory further occupying a majority of a total area of said single substrate [see Figure 4; also see Table 1, wherein the memory arrays, which comprise 48% of the die area utilization, with 21.9% being "Interconnect unused area and scribe"; Thus, 48% of the active areas on the substrate comprises a majority of a total area of active areas on the single substrate. This interpretation is reasonable, especially in light of the newly added dependent claim 18, which states "wherein the total area consists of a sum of **active areas of the single substrate**"]; and

an oscillator having a variable output frequency [see "Clock Generator" in Figure 4, as well as "OSC" in Fig. 1],

wherein *the oscillator* provides a system clock to the processing unit [see Figs. 1-4 on page 35],

the oscillator disposed on said integrated circuit substrate [see "Clock Generator" in Fig. 4].

However, Bagula does not expressly disclose if the oscillator is a ring oscillator. But Bagula does state that the chip used in the design of the substrate was "developed under license from Texas Instruments" [see page 34, bottom of col. 1].

Hashimoto, having the assignee of Texas Instruments, describes a microprocessor integrated circuit comprising:

a processing unit [1A, 1B, and 4],

a memory coupled to said processing unit and capable of storing information provided by said processing unit [being the dynamic memory arrays seen in Fig. 1A]; and

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit [see Fig. 1A, and col. 2, lines 26-42].

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to utilize a ring oscillator, as described by Hashimoto, as the clock generator, described and shown by Bagula. Bagula & Hashimoto are combinable because they are from the same field of endeavor, being systems developed under the same license, having memory arrays, processing unit, and clock generators. The suggestion/motivation for doing so would have been that ring oscillators were known at the time and commonly used as system clocks, as shown by Hashimoto. Therefore, it would have been obvious to combine the teachings of Hashimoto with the system of Bagula to obtain the invention as specified in claim 4.

Regarding ***claim 7***, Bagula and Hashimoto disclose the microprocessor integrated circuit discussed above in claim 4, and Bagula further teaches that said memory is capable of supporting read and write operations [see page 34, col. 2, "Signature Read" and "Block write/clear"].

Regarding independent ***claim 8***, Bagula teaches of a microprocessor integrated circuit [see Figs. 1-4] comprising:

a processing unit having one or more interface ports for interprocessor communication [see Figs. 1 and 4 on page 35, being "ALU and Temp Reg."], said processing unit being disposed on a single substrate [see Fig. 4],

a memory disposed upon said substrate and coupled to said processing unit [being the Microcode ROM , RAM and EEPROM Arrays, which comprise 48% of the die area],

said memory occupying a greater area of said substrate than said processing unit, said memory further comprising a majority of a total area of said substrate [see Figure 4; also see Table 1, wherein the memory arrays, which comprise 48% of the die area utilization, with 21.9% being "Interconnect unused area and scribe"; Thus, 48% of the active areas on the substrate comprises a majority of a total area of active areas on the single substrate. This interpretation is reasonable, especially in light of the newly added dependent claim 18, which states "wherein the total area consists of a sum of **active areas of the single substrate**"]; and

an oscillator having a variable output frequency [see "Clock Generator" in Figure 4, as well as "OSC" in Fig. 1],

wherein *the oscillator* provides a system clock to the processing unit [see Figs. 1-4 on page 35],

the oscillator disposed on said integrated circuit substrate [see "Clock Generator" in Fig. 4].

However, Bagula does not expressly disclose if the oscillator is a ring oscillator. But Bagula does state that the chip used in the design of the substrate was "developed under license from Texas Instruments" [see page 34, bottom of col. 1].

Hashimoto, having the assignee of Texas Instruments, describes a microprocessor integrated circuit comprising:

a processing unit [1A, 1B, and 4],

a memory coupled to said processing unit [being the dynamic memory arrays seen in Fig. 1A]; and

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit [see Fig. 1A, and col. 2, lines 26-42].

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to utilize a ring oscillator, as described by Hashimoto, as the clock generator, described and shown by Bagula. Bagula & Hashimoto are combinable because they are from the same field of endeavor, being systems developed under the same license, having memory arrays, processing unit, and clock generators. The suggestion/motivation for doing so would have been that ring oscillators were known at the time and commonly used as system clocks, as shown by Hashimoto. Therefore, it would have been obvious to combine the teachings of Hashimoto with the system of Bagula to obtain the invention as specified in claim 8.

Regarding ***claims 14 and 20***, Bagula and Hashimoto disclose the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and Bagula further teaches

that the memory comprises a plurality of physically separate memory portions [see Fig. 4, being the EEROM, the RAM, and the ROM].

Regarding ***claims 15 and 21***, Bagula and Hashimoto disclose the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and Bagula further teaches that the memory occupies an area greater than twice as large as an area occupied by the processing unit and the ring oscillator combined [see Fig. 4; also see Table 1].

Regarding ***claims 16 and 22***, Bagula and Hashimoto disclose the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and Bagula further teaches that the memory occupies an area greater than three times as large as an area occupied by the processing unit and the ring oscillator combined [see Fig. 4; also see Table 1].

Regarding ***claims 17 and 23***, Bagula and Hashimoto disclose the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and Bagula further teaches that the memory occupies an area approximately four times as large as an area occupied by the processing unit and the ring oscillator combined [see Fig. 4; also see Table 1].

Regarding ***claims 18 and 24***, Bagula and Hashimoto disclose the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and Bagula further teaches that the total area consists of a sum of active areas of the single substrate comprising circuit elements of the integrated circuit [see Fig. 4; also see Table 1].

Regarding ***claims 19 and 25***, Bagula and Hashimoto disclose the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and Bagula further teaches that the total area is an area provided by an entire top surface of the single substrate [see Fig. 4; also see Table 1].

Additional Pertinent Prior Art

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Aoki *et al.* (U.S. Patent Number 4,701,884) discloses a semiconductor memory integrated circuit disposed on a single semiconductor substrate, as read in the abstract and seen in Fig. 28;

Conclusion

23. Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that *ex parte* reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extensions of time in *ex parte* reexamination proceedings are provided for in 37 CFR 1.550(c).

24. In order to ensure full consideration of any amendments, affidavits or declarations, or other documents as evidence of patentability, such documents must be submitted in response to this Office action. Submissions after the next Office action, which is intended to be a final action, will be governed by the requirements of 37 CFR 1.116, after final rejection and 37 CFR 41.33 after appeal, which will be strictly enforced.

25. The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent No. 6,598,148 throughout the course of this reexamination proceeding.

NOTICE RE PATENT OWNER'S CORRESPONDENCE ADDRESS

Effective May 16, 2007, 37 CFR 1.33(c) has been revised to provide that:

The patent owner's correspondence address for all communications in an *ex parte* reexamination or an *inter partes* reexamination is designated as the correspondence address of the patent.

> *Revisions and Technical Corrections Affecting Requirements for Ex Parte and Inter Partes Reexamination*, 72 FR 18892 (April 16, 2007)(Final Rule)

The correspondence address for any pending reexamination proceeding not having the same correspondence address as that of the patent is, by way of this revision to 37 CFR 1.33(c), automatically changed to that of the patent file as of the effective date.

This change is effective for any reexamination proceeding which is pending before the Office as of May 16, 2007, including the present reexamination proceeding, and to any reexamination proceeding which is filed after that date.

Parties are to take this change into account when filing papers, and direct communications accordingly.

In the event the patent owner's correspondence address listed in the papers (record) for the present proceeding is different from the correspondence address of the patent, it is strongly encouraged that the patent owner affirmatively file a Notification of Change of Correspondence Address in the reexamination proceeding and/or the patent (depending on which address patent owner desires), to conform the address of the proceeding with that of the patent and to clarify the record as to which address should be used for correspondence.

Telephone Numbers for reexamination inquiries:

Reexamination and Amendment Practice	(571) 272-7703
Central Reexam Unit (CRU)	(571) 272-7705
Reexamination Facsimile Transmission No.	(571) 273-9900

26. ALL correspondence relating to this ex parte reexamination proceeding should be directed as follows:

Please mail any communications to:

Attn: Mail Stop "Ex Parte Reexam"
Central Reexamination Unit
Commissioner for Patents
P. O. Box 1450
Alexandria VA 22313-1450

Please FAX any communications to:

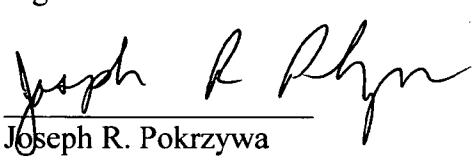
(571) 273-9900
Central Reexamination Unit

Please hand-deliver any communications to:

Customer Service Window
Attn: Central Reexamination Unit
Randolph Building, Lobby Level
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

Signed:



Joseph R. Pokrzywa
Primary Examiner
Central Reexamination Unit 3992
(571) 272-7410

Conferees:

ROLAND G. FOSTER
PRIMARY EXAMINER

ERIC S. KEASEL
CRU SPE-AU 3992

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 11

Complete if Known	
Application Number	90/008,227
Filing Date	September 21, 2006
First Named Inventor	Moore
Art Unit	3992
Examiner Name	Joseph R. Pokrzywa
Attorney Docket Number	0081-011D3C1X1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
JP	AA	US-5,241,636	08-31-1993	Kohn	
JP	AB	US-5,127,092	06-30-1992	Gupta et al.	
JP	AC	US-5,127,091	06-30-1992	Boufarah et al.	
JP	AD	US-5,121,502	06-09-1992	Rau et al.	
JP	AE	US-5,091,846	02-25-1992	Sachs et al.	
JP	EX	US- 5,031,092	07-09-1991	Edwards et al.	
JP	EY	US-4,989,133	01-29-1991	May et al.	
JP	EZ	US-4,980,821	12-25-1990	Koopman et al.	
JP	AF	US-4,967,326	10-30-1990	May	
JP	AG	US-4,933,835	06-12-1990	Sachs	
JP	AH	US-4,926,323	05-15-1990	Baror et al.	
JP	AI	US-4,899,275	02-06-1990	Sachs et al.	
JP	AJ	US-4,833,599	05-23-1989	Colwell et al.	
JP	FA	US-4,819,151	04-04-1989	May	
JP	FB	US-4,794,526	12-27-1988	May et al.	
JP	FC	US-4,758,948	07-19-1988	May et al.	
JP	FD	US-4,724,517	02-09-1988	May	
JP	AK	US-4,714,994	12-22-1987	Oklobdzija	
JP	FE	US-4,704,678	11-03-1987	May	
JP	AL	US-4,680,698	07-14-1987	Edwards et al.	
JP	AM	US-4,566,063	01-21-1986	Zolnowsky	
JP	AN	US-4,462,073	07-24-1984	Grondalski	
JP	AO	US-4,402,042	08-30-1983	Guttag	
JP	AP	US-4,390,946	06-28-1983	Lane	
JP	AQ	US-4,348,743	09-07-1982	Dozier	
JP	AR	US-4,295,193	10-13-1981	Pomerene	
JP	AS	US-3,976,977	08-27-1976	Porter et al.	

Examiner Signature	Joseph R Pokrzywa	Date Considered	6/23/08

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] Kind Codes of U.S. Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	90/008,227
				Filing Date	September 21, 2006
				First Named Inventor	Moore
				Art Unit	3992
(Use as many sheets as necessary)				Examiner Name	Joseph R. Pokrzywa
Sheet	2	of	11	Attorney Docket Number	0081-011D3C1X1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
J.P.	AT	IBM Systems Reference Library, IBM System/360 Model 67 Functional Characteristics, File No. S360-01, Form A27-2719-0, published by IBM (1967).	☐
J.P.	AU	ANDERSON, D.W., "The IBM System/360 Model 91: Machine Philosophy and Instruction Handling, IBM Journal, (1967).	☐
J.P.	AV	GE-625 / 635 Programming Reference Manual, revised January 1966.	☐
J.P	AW	CLIPPER™ 32-Bit Microprocessor, Introductions to the CLIPER Architecture, published by Fairchild in 1986.	☐
J.P.	AX	SIMPSON et al., "The IBM RT PC ROMP processor and Memory management unit architecture," IBM systems Journal, 26(4):346-360.	☐
J.P.	AY	M68300 Family MC68332 User's Manual, published by Motorola, Inc. in 1995.	☐
J.P.	AZ	DITZEL et al., "The Hardware Architecture of the CRISP Microprocessor," AT & T Information Systems, ACM, pages 309-319 and table of contents (1987).	☐
J.P.	BA	i860 64-Bit Microprocessor, published by Intel Corporation February 1989.	☐
J.P.	BB	RAU et al., "The Cydra 5 Departmental Supercomputer, Design Philosophies, Decisions, and Trade-offs," IEEE, pages 12-36 (1989).	☐
J.P.	BC	Datasheet for Intel 4004 Single Chip 4-Bit 9-Channel Microprocessor , pages 8-15 to 8-23 .	☐
J.P.	BD	Intel MCS-4 Micro Computer Set (November 1971)	☐

Examiner Signature	Joseph R Pokrzywa	Date Considered	6/23/08

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Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 3 of 11

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Art Unit	3992
Examiner Name	Joseph R. Pokrzywa
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J.P.	BE	Intel 8008 8-Bit Parallel Central Processor Unit, published by Intel (November 1972)	
J.P.	BF	iAPX 386 High Performance 32-Bit Microprocessor Product Review, published by Intel (April 1984)	☐
J.P.	BG	Intel 80386 Programmer's Reference Manual, published by Intel (1986)	☐
J.P.	BH	Motorola MC68020 32-Bit Microprocessor User's Manual (1984)	☐
J.P.	BI	THORNTON, J. E., "Design of a Computer, The Control Data 6600," published by Advanced Design Laboratory (1970).	☐
J.P.	BJ	6400/6500/6600 Computer Reference Manual, published by Control Data® (1965, 1966, 1967).	☐
J.P.	BK	GRISHMAN, R., "Assembly Language Programming for the Control Data 6600 and Cyber Series Algorithmics,".	☐
J.P.	BL	HENNESSY et al., "MIPS: A Microprocessor Architecture," IEEE, pages 17-22 (1982).	☐
J.P.	BM	HENNESSY et al., "Hardware/software tradeoff for increased performance," Proceedings of the Symposium on Architectural Support for Programming Languages and Operating Systems,, pages 2-11. ACM, April 1982	☐
J.P.	BN	HENNESSY et al., "MIPS: A VLSI Processor Architecture, Technical Report 223," Computer Systems Laboratory, Department of Electrical Engineering and Computer Science, Standford University November 1981	☐
J.P.	BO	GROSS et al., "Measurement and evaluation of MIPS architecture and processor," ACM Trans. Computer Systems, pp.229-257 August 1988.	☐

Examiner Signature	Joseph R Pokrzywa	Date Considered	6/23/08

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				Filing Date	September 21, 2006
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Sheet	4	of	11	Attorney Docket Number	0081-011D3C1X1

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J.P.	BP	BIT SPARC Integer Unit B5000 Datasheet attached to a presentation by Anant Agrawal in 1989	☐
J.P.	BQ	SEQUIN et al., "Design and Implementation of RISC I," pages 276-298 from *VLSI Architecture*, B. Randell and P.C. Treleaven, editors, Prentice Hall, 1983.	☐
J.P.	BR	UNGAR et al., "Architecture of SOAR: Smalltalk on a RISC," Proceedings of the 11th Annual International Symposium on Computer Architecture ISCA '84. ACM Press, New York, NY, pages 188-197 (1984).	☐
J.P.	BS	Cray-1 Computer System Hardware Reference Manual, Publication No. 2240004, Rev C, November 4, 1997	☐
J.P.	BT	Acorn Computers, Ltd., Acorn RISC Machine CPU Software Manual, Issue 1.00 October 1985	☐
J.P.	BU	PATTERSON et al., "Architecture of a VLSI Instruction Cache for A RISC," ACM, pages 108-116 (1983).	☐
J.P.	BV	PATTERSON, D. A., "Reduced Instruction Set Computers" Communication of the ACM, , 28(1):.8-21, January 1985	☐
J.P.	BW	PATTERSON, D. A., "RISC watch", pages 11-19 (March 1984).	☐
J.P.	BX	SHERBURNE, R. W., "Processor Design Tradeoffs in VLSI," U.C. Berkeley, May, 1984. PhD Dissertation.	☐
	BY	Excerpt from A Seymour Cray Perspective http://research.Microsoft.com/users/gbell/craytalk/sld/001.htm (Slide 1)	☐
	BZ	~~Excerpt from A Seymour Cray Perspective http://research.microsoft.com/users/gbell/craytalk/sld029.htm (Slide 29)~~	☐

Examiner Signature	Joseph R Pokrzywa	Date Considered	6/23/08

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	CA	~~RISC Roots: CDC 6600 (1965)~~	☐
	CB	~~http://www.bitsavers.org/pdf/cdc/6x00/~~	☐
J.P.	CC	SIMPSON, R.O., " The IBM RT Personal computer," BYTE 11(11):43-78 (October 1986).	☐
J.P.	CD	RYAN, D.P., "Intel's 80960: An Architecture Optimized for Embedded Control," IEEE Micro, published in June 1988.	☐
J.P.	CE	WATERS, F., "IBM RT Personal Computer Technology," IBM Corp. 1986.	☐
	CF	~~Alliacense Product Report, USP 5784584, TLCS-900/H1 Series TMP92C820, Toshiba Microcontroller TMP92C820 / TLCS-900/H1 Series 16-bit Microcontroller, pages 1-9, filed 8/14/06 in 2:05-CV-00494-TJW~~	☐
	CG	~~Alliacense Product Report, NEC Microcomputer, USP 5784584, V850E2 32 Bit Microcontroller, pp.1-8 (2006)~~	☐
	CH	~~Application Serial No. 08/484,935, Amendment of June 12, 1997.~~	☐
	CI	Request for Reexamination of ~~US Patent 5,784,584 as filed by NEC 9/21/06.~~	☐
	CJ	~~Office action of 2/3/07 in application 90/008,225.~~	☐
	CK	Office action of ~~2/12/07 in application 90/008,225.~~	☐

Examiner Signature	Joseph R Pokrzywa	Date Considered	6/23/08

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61303249

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				Filing Date	September 21, 2006
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	~~CL~~	~~Decision of 6/14/07 Merging application nos. 90/008,225 and 90/008,299~~	☐
	~~CM~~	~~This space left intentionally blank~~	☐
	~~CN~~	~~Request by Toshiba for Reexamination of US Patent 5,784,584 as filed 10/19/06.~~	☐
	CO	~~Office action of 12/22/06 in application no. 90/008,299~~	☐
	CP	~~Office action of 6/26/07 in combined case 90/008,225 and 90/008,299~~	☐
	~~CQ~~	~~Daniels Deposition transcript, 8/10/07, in 2-05CV-494 (TJW)~~	☐
	~~CR~~	~~Exhibit 1 to Daniels deposition of 8/10/07 in 2-05CV-494 (TJW): Subpoena of 8/1/07 for Gary Daniels in 2-05CV-494 (TJW)~~	☐
	~~CS~~	~~Exhibit 2 to Daniels deposition of 8/10/07 in 2-05CV-494 (TJW): Motorola Semiconductor Products Sector, Microprocessor Products Group, Milestones for Management Review~~	☐
J.P.	CT	Exhibit 3 to Daniels deposition of 8/10/07 in 2-05CV-494 (TJW): "How to Take Control" product brochure by Motorola (1988)	☐
J.P.	CU	Exhibit 4 to Daniels deposition of 8/10/07 in 2-05CV-494 (TJW): "Embedded Control Solutions, Powered by Motorola" product brochure by Motorola	☐
J.P.	CV	Exhibit 5 to Daniels deposition of 8/10/07 in 2-05CV-494 (TJW): 10/20/88 Letter to Daniels from Fisher.	☐

Examiner Signature	Joseph R Pokrzywa	Date Considered	6/23/08

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 7 of 11

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J.P.	CW	Exhibit 6 to Daniels deposition of 8/10/07 in 2-05CV-494 (TJW): List of Motorola Microcontroller business major goals for 1989	☐
J.P.	CX	Exhibit 7 to Daniels deposition of 8/10/07 in 2-05CV-494 (TJW): Sales brochure, "Motorola Microcontroller Division, Customer Management Briefing Summary"	☐
	~~CY~~	~~Exhibit 8 to Daniels deposition of 8/10/07 in 2-05CV-494 (TJW): Document titled "Motorola's MC68332 Microcontroller"~~	☐
	~~CZ~~	~~Exhibit 9 to Daniels deposition of 8/10/07 in 2-05CV-494 (TJW): Die photo~~	☐
J.P.	DA	Exhibit 10 to Daniels deposition of 8/10/07 in 2-05CV-494 (TJW): Article by Daniels, "A Participant's Perspective," IEEE Micro, 16(6):21-31 plus cover page and 2 unnumbered pages at back of document (1996).	☐
J.P	DB	Exhibit 11 to Daniels deposition of 8/10/07 in 2-05CV-494 (TJW): "A legacy of leadership," Mos Talk, 22(9): 4 pages (1997)	☐
	~~DC~~	~~Exhibit 12 to Daniels deposition of 8/10/07 in 2-05CV-494 (TJW): Photo of 68332 with other support chips~~	☐
	~~DD~~	~~McDermott Deposition transcript, 8/9/07, in 2-05CV-494 (TJW)~~	☐
	~~DE~~	~~Exhibit 1 to McDermott deposition of 8/9/07 in 2-05CV-494 (TJW): Subpoena of 8/1/07 for Mark McDermott in 2-05CV-494 (TJW)~~	☐
	~~DF~~	~~Exhibit 2 to McDermott deposition of 8/9/07 in 2-05CV-494 (TJW): "Motorola's MC68332 Microcontroller" layout design~~	☐
	~~DG~~	~~Exhibit 3 to McDermott deposition of 8/9/07 in 2-05CV-494 (TJW): Photos of wafers pre-chip I and II and final wafer and die photo of chip~~	☐

Examiner Signature	Joseph R Pokrzywa	Date Considered	6/23/08

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61303249

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				Art Unit	3992
(Use as many sheets as necessary)				Examiner Name	Joseph R. Pokrzywa
Sheet	8	of	11	Attorney Docket Number	0081-011D3C1X1

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	DH	~~Exhibit 4 to McDermott deposition of 8/9/07 in 2-05CV-494 (TJW): Photo of Motorola's GMP-X 32-bit Microcontroller~~	☐
	DI	~~Exhibit 5 to McDermott deposition of 8/9/07 in 2-05CV-494 (TJW): Photo of individual die from pre-chip I, II and the final chip~~	☐
	DJ	~~Exhibit 7 to McDermott deposition of 8/9/07 in 2-05CV-494 (TJW): Patent Application transmittal letter received by USPTO 8/26/88 for application 237022~~	☐
J.P.	DK	Exhibit 8 to McDermott deposition of 8/9/07 in 2-05CV-494 (TJW): Schematic used to lay out chip	☐
J.P.	DL	Exhibit 10 to McDermott deposition of 8/9/07 in 2-05CV-494 (TJW): McDermott et al., "Testability Features Of the MC68332 Modular Microcontroller," 1989 International Test Conference, paper 28.2, pages 615-623 (1989)	☐
J.P.	DM	Exhibit 11 to McDermott deposition of 8/9/07 in 2-05CV-494 (TJW): McDermott et al., "Modular Design of a High Performance 32-bit Microcontroller," IEEE 1989 Custom Integrated Circuits Conference, pages 23.8.1-23.8.4 (1989)	☐
	DN	~~Exhibit 12 to McDermott deposition of 8/9/07 in 2-05CV-494 (TJW): Notes from class taken at University of Texas (September 1987).~~	☐
	DO	~~1/15/08 letter by fax from Rangel (PTI) to McFarlane, Hoge, Agarawal & Spears re: non-confidential status of~~ deposition transcripts of Daniels and Mcdermott	☐
	DP	~~1/17/08 letter via e-mail from McFarlane to Hoge, Agarwal, & Spears re: "Attorney Eyes Only" status of~~ depositions of Daniels and McDermott	☐
J.P	DQ	"8 bit Dual 1-chip Microcomputer MN1890 Series User's Manual," translation of original Japanese language document, by Matsushita Electric Industrial Co., Ltd. Semiconductor Sales Division	☐
J.P	DR	"Public Availability Date Request," from matt Antonelli of Weil Gotshal & Manges LLP re: Transputer Reference Manual, INMOS Ltd., 1988	☐

Examiner Signature	Joseph R Pokrzywa	Date Considered	6/23/08

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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
J.P.	DS	SIBIGTROTH, J. M., "Motorola's MC68HC11: Definition and Design of a VLSI Microprocessor," IEEE Micro, 4(1):54-65 (1984)	☐
J.P.	DT	"Specification Sheet, MN18882 (Book[1])," translation of the Japanese language original, Code No. MIG0175, Matsushita Electronics Industry Corporation, Microcomputer Products Division, 10/2/90	☐
J.P.	DU	"DS5000 Soft Microcontroller User's Guide Preliminary V 1.0," Dallas Semiconductor	☐
	~~DV~~	~~MEI Invalidity Contentions on '148 and '336 patents filed 8/22/07 in case # 2-05CV-494 (TJW)~~	☐
	~~DW~~	~~MEI claim charts on MOSTEK 3873 chip, filed 9/8/07 in case # 2-05CV-494 (TJW)~~	☐
	~~DX~~	~~Defendants MEI, PNA, and JVC Preliminary Invalidity Contentions filed 9/18/06 in case # 2-05CV-494 (TJW)~~	☐
	~~DY~~	~~Defendant NEC Preliminary Invalidity Contentions filed 9/18/06 in case # 2-05CV-494 (TJW)~~	☐
	~~DZ~~	~~Defendant Toshiba Preliminary Invalidity Contentions filed 9/18/06 in case # 2-05CV-494 (TJW)~~	☐
	~~EA~~	~~Defendant NEC Preliminary Invalidity Contentions filed 9/25/06 in case # 2-05CV-494 (TJW)~~	☐
	~~EB~~	~~Defendant ARM Preliminary Invalidity Contentions filed 10/12/06 in case # 2-05CV-494 (TJW)~~	☐
J.P.	EC	MN188166 User's Manual, Japanese language document with English translation.	☐

Examiner Signature	Joseph R Pokrzywa	Date Considered	6/23/08

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	90/008,227
				Filing Date	September 21, 2006
				First Named Inventor	Moore
				Art Unit	3992
(Use as many sheets as necessary)				Examiner Name	Joseph R. Pokrzywa
Sheet	10	of	11	Attorney Docket Number	0081-011D3C1X1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
	ED	Complaint for Declaratory Judgment filed 2/8/08 by HTC vs. TPL, Patriot, and Alliacense, case # C08 00882 JL	☐
	EE	Asustek First Amended Complaint for Declaratory Judgment vs. TPL, Patriot, MCM and Alliacense, filed 2/13/07, case C08 00884 EMC	☐
	EF	Complaint for Declaratory Judgment filed 2/8/08 by Acer and Gateway vs. TPL, Patriot, and Alliacense, case # C08 00877 HRL	☐
	EG	Asustek Complaint for Declaratory Judgment vs. TPL, Patriot and Alliacense, filed 2/8/08, case C08 00884 EMC	☐
	EH	Order of Dismissal of NEC Electronics of 12/20/07, case # 2:05-CV-00494 (TJW)	☐
	EI	Order of Dismissal of Matsushita, Panasonic, JVC Americas, and Toshiba of 12/20/07, case # 2:05-CV-00494 (TJW)	☐
	EJ	Order of Partial Judgment of Non-Infringement of 9/12/07, case # 2:05-CV-00494 (TJW)	☐
	EK	Alliacense Product Report - Preliminary Review, USP 5,440,749; GPS Car Navigation Main Processor	☐
	EL	Alliacense Product Report - Preliminary Review, USP 5,440,749; GPS Navigation System GPS Chipset	☐
	EM	Alliacense Product Report - Preliminary Review, USP 5,440,749; GPS Navigation System Main Microprocessor	☐
	EN	Alliacense Product Report - Preliminary Review, USP 5,440,749; Kyocera Digital Camera Finecam S3R Image Processor	☐

Examiner Signature	Joseph R Pokrzywa	Date Considered	6/23/08

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Substitute for form 1449B/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	90/008,227
				Filing Date	September 21, 2006
				First Named Inventor	Moore
				Art Unit	3992
(Use as many sheets as necessary)				Examiner Name	Joseph R. Pokrzywa
Sheet	11	of	11	Attorney Docket Number	0081-011D3C1X1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	EO	~~Alliacense Product Report - Preliminary Review, USP 5,440,749; PDA/Mobile Navigation, GPS Processor~~	☐
J.P.	EP	Motorola MC68020 32-bit Microprocessor User's Manual, 2nd Edition, Rev. 1, Prentice-Hall, 1985.	☐
J.P.	EQ	BARRON et al., "The Transputer," Electronics, pages 109-115 (1983)	☐
J.P.	ER	Burroughs Corporation, "Burroughs B7700 Systems Reference Manual," 1973	☐
J.P.	ES	FIASCONARO, J., "Microarchitecture of the HP9000 Series 500 CPU," Microarchitecture of VLSI Computers, NATO ASI Series No. 96, Antognetti, eds., pages 55-81.	☐
J.P.	ET	MACGREGOR et al., "The Motorola MC68020," IEEE Micro, 4(4):103-118 (1984).	☐
	EU	~~Request for Reexamination of US Patent 5,440,749 as filed 2/11/08 (ARM)~~	
	EV	~~Office action response of 9/26/07 in combined case 90/008,225 and 90/008,299.~~	
	EW	~~Supp. office action response of 11/13/07 in combined case 90/008,225 and 90/008,299.~~	☐

Examiner Signature	Joseph R Pokrzywa	Date Considered	6/23/08

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[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Notice of References Cited	Application/Control No. 90/008,227	Applicant(s)/Patent Under Reexamination 6598148	
	Examiner JOSEPH R. POKRZYWA	Art Unit 3992	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-4,956,811	09-1990	Kajigaya et al.	365/51
*	B	US-4,882,710	11-1989	Hashimoto et al.	365/189.05
*	C	US-4,701,884	10-1987	Aoki et al.	365/189.09
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"A 5V Self-Adaptive Microcomputer with 16Kb of E2Program Storage and Security", written by Mark Bagula et al., 1983 IEEE International Solid-State Circuits Conference, pages 34-35.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Reexamination	Application/Control No.	Applicant(s)/Patent Under Reexamination
	90/008,227	6598148
	Certificate Date	Certificate Number

Requester Correspondence Address: ☐ **Patent Owner** ☒ **Third Party**

FOLEY AND LARDNER LLP
3000 K STREET NW
WASHINGTON, DC 20007

LITIGATION REVIEW ☒	**J.P.** (examiner initials)	**6/12/08** (date)
Case Name		Director Initials
Panasonic Corp. et al. v. Patriot Scientific Corp. et al. Case No. 5:05cv4844 and 3:05cv4844, D.C. N.D. California		Lee Hasel for GM
Toshiba America Inc. et al. v. Toshiba Corp et al. Case No. 5:05cv4838 and 3:05cv4838, D.C. N.D. California		
NEC Corp. et al. v. Technology Properties Ltd. Inc. et al. Case No. 3:05cv4847, D.C. N.D. California		
Fujitsu Computer Syst. Corp. et al. v. Fujitsu Ltd. et al. Case No. 3:05cv4837, D.C. N/D. California		
JVC Americas Corp. v. Patriot Scientific Corp. et al. Case No. 4:05cv4845 and 3:05cv4845, D.C. N.D. California		
TECHNOLOGY PROP. LTD. INC. V. FUJITSU LTD. ETAL. CASE NO. 2:05 CV 494, D.C. E.D. TEXAS		

COPENDING OFFICE PROCEEDINGS	
TYPE OF PROCEEDING	**NUMBER**
1. reexaminations of a patent from a divisional application	90/008,237,90/008,306, 90/008,474
2. reexamination of a patent from a divisional application	90/008,225, 90/008,299
3.	
4.	

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
90/008,227	6598148
Examiner	**Art Unit**
JOSEPH R. POKRZYWA	3992

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date									
Final	Original	12/4/07	6/19/08								
	1	N	N								
	2	N	N								
	3	N	N								
	4	✓	✓								
	5	N	N								
	6	N	N								
	7	✓	✓								
	8	✓	✓								
	9	N	N								
	10	✓	✓								
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Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
90/008,227	6598148	
Examiner	**Art Unit**	
JOSEPH R. POKRZYWA	3992	

SEARCHED			
Class	Subclass	Date	Examiner

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST text search	6/9/2008	J.P.
review file history	6/9/2008	J.P.