

CXM-0021**337-TA-853**

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PTO/SB/57 (04-05)
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(Also referred to as FORM PTO-1465)

71338

U.S.

REQUEST FOR EX PARTE REEXAMINATION TRANSMITTAL FORM

71338

U.S. PTO

90008237

09/21/06

Address to:

Mail Stop Ex Parte Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450



Attorney Docket No.: 069974-0160

09/21/06

Date: September 21, 2006

1. ☒ This is a request for *ex parte* reexamination pursuant to 37 CFR 1.510 of patent number 5,809,336 issued September 15, 1998. The request is made by:

☐ patent owner.
☒ third party requester.
2. ☒ The name and address of the person requesting reexamination is:

Matthew A. Smith, on behalf of NEC Electronics America, Inc.
Foley & Lardner LLP
3000 K Street, NW, Suite 500, Washington, DC 20007
3. ☐ a. A check in the amount of \$_____ is enclosed to cover the reexamination fee, 37 CFR 1.20(c)(1);
☐ b. The Director is hereby authorized to charge the fee as set forth in 37 CFR 1.20(c)(1) to Deposit Account No. _____ (submit duplicative copy for fee processing); or
☒ c. Payment by credit card. Form PTO-2038 is attached.
4. ☐ Any refund should be made by ☐ check or ☐ credit to Deposit Account No. _____. 37 CFR 1.26(c). If payment is made by credit card, refund must be to credit card account.
5. ☒ A copy of the patent to be reexamined having a double column format on one side of a separate paper is enclosed. 37 CFR 1.510(b)(4)
6. ☐ CD-ROM or CD-R in duplicate, Computer Program (Appendix) or large table
☐ Landscape Table on CD
7. ☐ Nucleotide and/or Amino Acid Sequence Submission
If applicable, items a. - c. are required.
 - a. ☐ Computer Readable Form (CRF)
 - b. Specification Sequence Listing on:
 - i. ☐ CD-ROM (2 copies) or CD-R (2 copies); or
 - ii. ☐ paper
 - c. ☐ Statements verifying identity of above copies
8. ☐ A copy of any disclaimer, certificate of correction or reexamination certificate issued in the patent is included.
9. ☒ Reexamination of claim(s) 1 - 10 is requested.
10. ☒ A copy of every patent or printed publication relied upon is submitted herewith including a listing thereof on Form PTO/SB/08, PTO-1449, or equivalent.

09/26/2006 INCDU50 00000003 90008237
 01 FC:1812 2520.00 0P
11. ☐ An English language translation of all necessary and pertinent non-English language patents and/or printed publications is included.

[Page 1 of 2]

This collection of information is required by 37 CFR 1.510. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop Ex Parte Reexam, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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TPL853_02992802

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12. ☒ The attached detailed request includes at least the following items:
- a. A statement identifying each substantial new question of patentability based on prior patents and printed publications. 37 CFR 1.510(b)(1)
 - b. An identification of every claim for which reexamination is requested, and a detailed explanation of the pertinency and manner of applying the cited art to every claim for which reexamination is requested. 37 CFR 1.510(b)(2)
13. ☐ A proposed amendment is included (only where the patent owner is the requester). 37 CFR 1.510(e)
14. ☒ a. It is certified that a copy of this request (if filed by other than the patent owner) has been served in its entirety on the patent owner as provided in 37 CFR 1.33(c).
The name and address of the party served and the date of service are:
- Mr. Drew S. Hamilton
- Knobbe, Martens, Olson & Bear, LLP
- 550 W C St. Suite 120, San Diego, CA 92101
- Date of Service: September 21, 2006; or
- ☐ b. A duplicate copy is enclosed since service on patent owner was not possible.

15. Correspondence Address: Direct all communication about the reexamination to:

☒ The address associated with Customer Number: 22428

OR

☐ Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

16. ☒ The patent is currently the subject of the following concurrent proceeding(s):

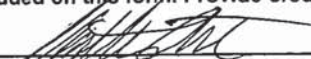
- ☐ a. Copending reissue Application No. _____
- ☐ b. Copending reexamination Control No. _____
- ☐ c. Copending Interference No. _____
- ☒ d. Copending litigation styled: _____

Technology Properties Limited, Inc. v. Fujitsu Limited et al.,

Case No. 2:05-cv-00494-TJW, Federal District Court for the Eastern

District of Texas, Marshall Division

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Authorized Signature

Matthew A. Smith

Typed/Printed Name

Sept. 21, 2006
Date

49,003

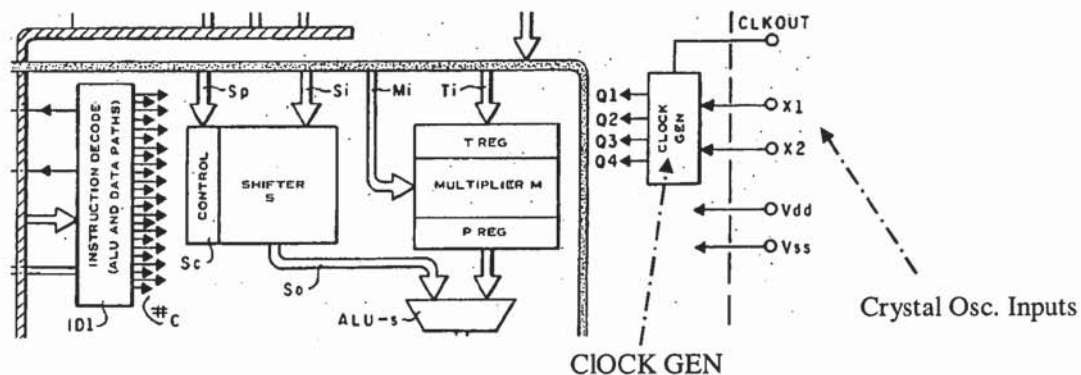
Registration No.

☐ For Patent Owner Requester

☒ For Third Party Requester

Crucial to the present invention is that since both the oscillator or variable speed clock and driven device are on the same substrate, when the fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together. This differs from all cited references in that the oscillator or variable speed clock and the driven device are on the same substrate.... [Exhibit 10, p. 5] (emphasis added).

The Office was not able to rebut such statements during original prosecution, which were true only in the limited vacuum of the “cited prior art”. The reference before the Examiner that most closely approximated the “on-chip ring oscillator” or “variable speed system clock” was the Magar patent, (U.S. Pat. No. 4,503,500, Exhibit 11). The Magar patent described an off-chip crystal oscillator, with on-chip clock generation circuitry. The pertinent portions of Fig. 2A from the Magar patent are shown below, with dashed arrows added by the Requester to indicate particular features:



Magar shows “CLOCK GEN” circuitry on the right-hand side of Fig. 2A that is on a single substrate with the CPU. The CLOCK GEN circuitry, however, has crystal oscillator inputs X1 and X2. This leads to the supposition that CLOCK GEN is not a resonator itself, but rather circuitry that amplifies, filters or otherwise prepares the crystal resonator output for use as

a CPU clock. Since the crystal resonator of Magar was off-chip, the Applicants were able to assert:

one of ordinary skill in the art should readily recognize the speed of the CPU and the clock *do not* vary together due to manufacturing variation, operating voltage and temperature of the IC in the Magar microprocessor, as taught in the above quotation from the reference. This is simply because the Magar microprocessor clock is frequency-controlled by a crystal which is also external to the microprocessor. Crystals are by design fixed-frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The Magar microprocessor in no way contemplates the variable speed clock as claimed. (emphasis in original) [Amendment of July 3, 1997, Exhibit 10, p. 3-4]

If the Office had had access to the best prior art, it could have quickly met this argument with a better rejection. In fact, by 1980, the use of on-chip ring oscillators to clock integrated circuits was *undergraduate textbook knowledge*, appearing in Mead & Conway (Exhibit 18). In Chapter 7, the Mead & Conway textbook discusses integrated circuit clocks, stating that they are most easily constructed using on-chip ring oscillators, and that the frequency of the ring oscillators will vary with ambient conditions and process technology:

Process variation in integrated circuit fabrication does not allow accurate resonant networks to be fabricated by usual means, but it is perfectly feasible, indeed essential for self-contained VLSI systems, to generate clock signals on the chip....[T]he role of the clock in a synchronous system is to connect sequence and time....A *model* of the temporal behavior of the systems being clocked is built into the clock generator or in the choice of times for the various timers. The easiest way to build these timers is as chains of inverters. The propagation delay time of such a chain will of course vary with τ , according to the way in which the fabrication process, aging, temperature and power voltage affect τ . However, these variations only make the inverter chain a better model of the system being clocked than a fixed timer would be....Clocks that employ these delays as timers are all elaborations