In the Matter of
Certain Wireless Consumer Electronics Devices and Components Thereof

Investigation No. 337-TA-853

Complainants' Claim Construction Presentation

Before the Honorable E. James Gildea

March 5, 2013

CDXM-0001.001

Patent Reexaminations Confirm Strength of Patent

- '336 Patent Reexamination – 4 Reexaminations
  - Existing claims 1, 2, 6, 7, 9, 10 allowed (as amended)
    - clarified that the clock signal of the second clock originates from a source other than the on-chip oscillator
    - no amendment or discussion re meaning of "ring oscillator"
  - New claims 11-16

Disputed Terms For Construction

- “ring oscillator”
- “entire oscillator/clock”
- “varying” limitations terms
- “thereby enabling said processing frequency to track said clock rate in response to said parameter variation”
- “clocking said CPU”
- “operates asynchronously to”

Disputed Terms For Construction

- "ring oscillator" – *claims 1, 9, 11, 15*
- "entire oscillator/clock"
- "varying" limitations terms
- "thereby enabling said processing frequency to track said clock rate in response to said parameter variation"
- "clocking said CPU"
- "operates asynchronously to"

"ring oscillator"

TPL's Construction	Respondents' Construction	Staff's Construction
Interconnected electronic components comprising multiple odd numbers of inversions arranged in a loop, where three or more inversions are required to maintain an oscillating output	An oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is: (1) noncontrollable; and (2) variable based on the temperature, voltage, and process parameters in the environment	An oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment

The Parties Agree on at Least a Portion of the Construction

TPL's Construction	Respondents' Construction	Staff's Construction
Interconnected electronic components comprising multiple odd numbers of inversions arranged in a loop, where three or more inversions are required to maintain an oscillating output	An oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is: (1) noncontrollable; and (2) variable based on the temperature, voltage, and process parameters in the environment	An oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment

“ring oscillator”

- A ring oscillator is dependent upon having at least three inverters to maintain an oscillating output.
- A ring oscillator “oscillates” because as the signal moves around the loop, it changes from 1 to 0 to 1 to 0, etc.

"ring oscillator"

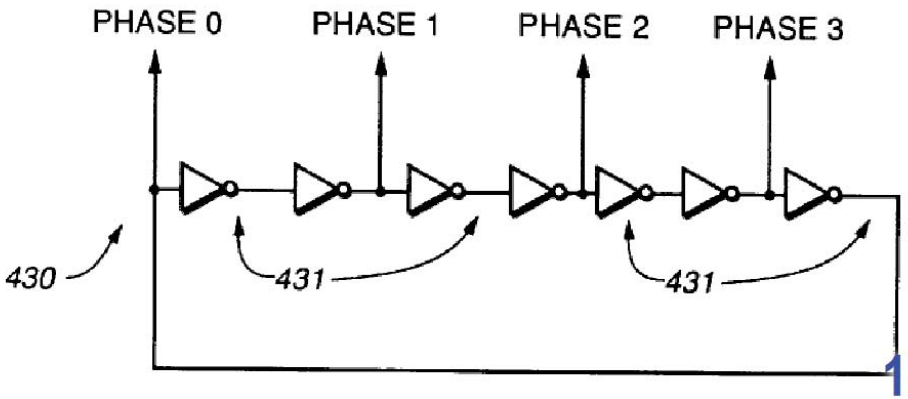


FIG._18

“ring oscillator”

- A ring oscillator will not work with even numbers of inverters – the signal will always be the same at the same point in the loop.

- A ring oscillator will not work with one inverter

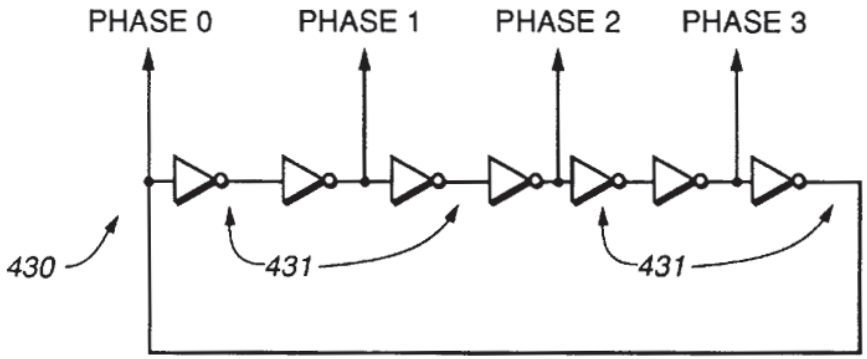


FIG._18

"ring oscillator"

TPL's Construction

Interconnected electronic components comprising multiple odd numbers of inversions arranged in a loop, where three or more inversions are required to maintain an oscillating output

- TPL's additional structural language delineates the well-known ring oscillator from other circuits/oscillators with multiple odd numbers of inversions in loop.

"ring oscillator"

- Talbot discloses a VCO, but:
  - "Relaxation oscillator" with three inversion stages
  - Not a ring oscillator
  - Schmitt trigger will oscillate with only one inversion

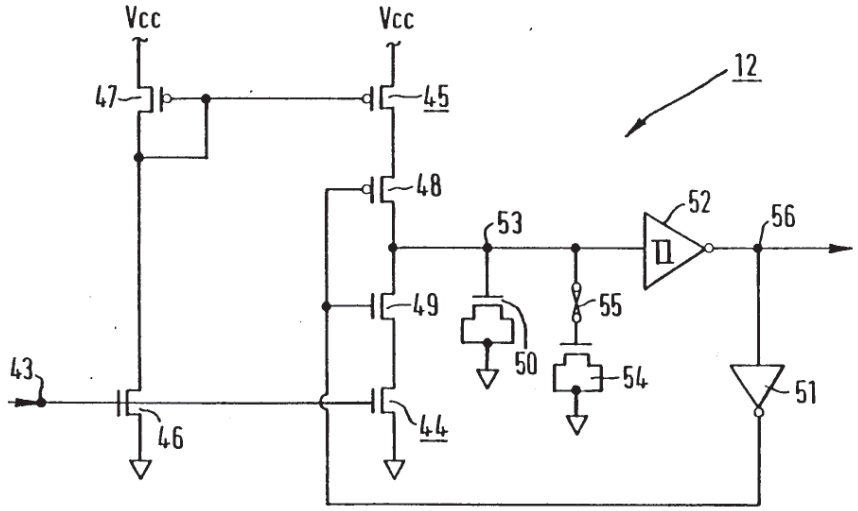
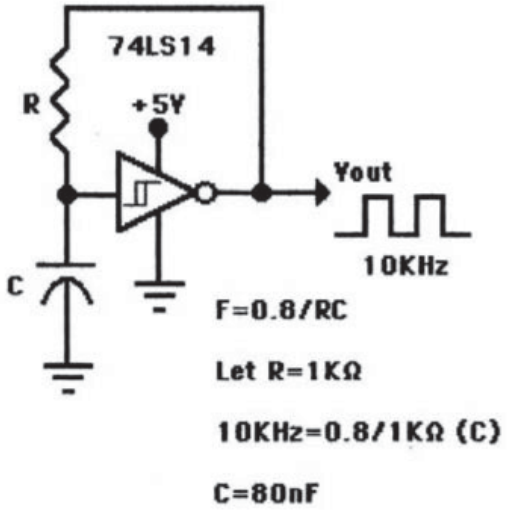
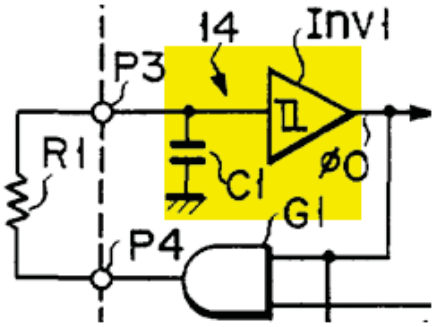


FIG. 3

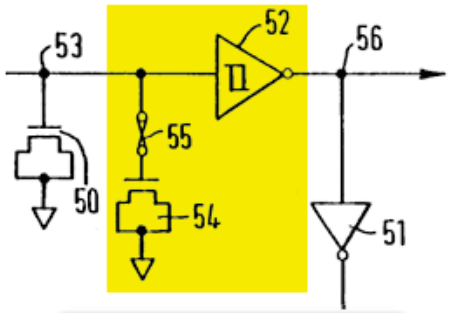


"ring oscillator"

- Kato confirms Talbot's circuitry is not a ring oscillator:



From Kato Fig. 1



From Talbot Fig. 3

> A first clock generating circuit **14** comprises a first clock generating section **141**, _ _ _ _ _ _ _

RXM-0006 (Kato) col. 8, lines 22-23

> first clock generating section **141** may be replaced by a ring oscillator of the known type

RXM-0006 (Kato) col. 10, lines 67-68

"ring oscillator"

- The Examiner agreed that Kato's drawings do not show a ring oscillator
  - The Examiner instead cited Kato, which says the first clock generating section 141 *may be replaced by a ring oscillator*:

> **and an entire ring oscillator variable speed system clock** (Kato; col. 10, line 68 through col. 11, line 7, "first clock generating section 141 may be replaced by a ring oscillator of the known type...When a ring oscillator is used, its output frequency lowers in proportion to the speed of the data processing circuit")
>
> *JXM-0024 (3/09 Final Office Action) at TPL853_02992771*

"ring oscillator"

TPL's Construction

Interconnected electronic components comprising multiple odd numbers of inversions arranged in a loop, where three or more inversions are required to maintain an oscillating output

- Therefore, TPL's additional language is needed:

  "where three or more inversions are required to maintain an oscillating output."

"ring oscillator"

Respondents Want to Import Two Extraneous Limitations:

Respondents' Construction

An oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is: (1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters in the environment.

"ring oscillator"

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An oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is: (1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters in the environment.

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"ring oscillator"

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An oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is: (1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters in the environment.

"ring oscillator"

Respondents have proven no clear and unambiguous disavowal of control of the ring oscillator

A disavowing statement must be "so clear as to show reasonable clarity and deliberateness, and so unmistakable as to show unambiguous evidence of disclaimer."

Omega Eng'g, Inc. v. Rayteck Corp., 334 F.3d 1314, 1325 (Fed. Cir. 2003).

The disavowal doctrine only applies where a disavowal is "both clear and unmistakable."

Cordis Corp. v. Medtronic AVE, Inc., 511 F.3d 1157, 1177 (Fed. Cir. 2008).

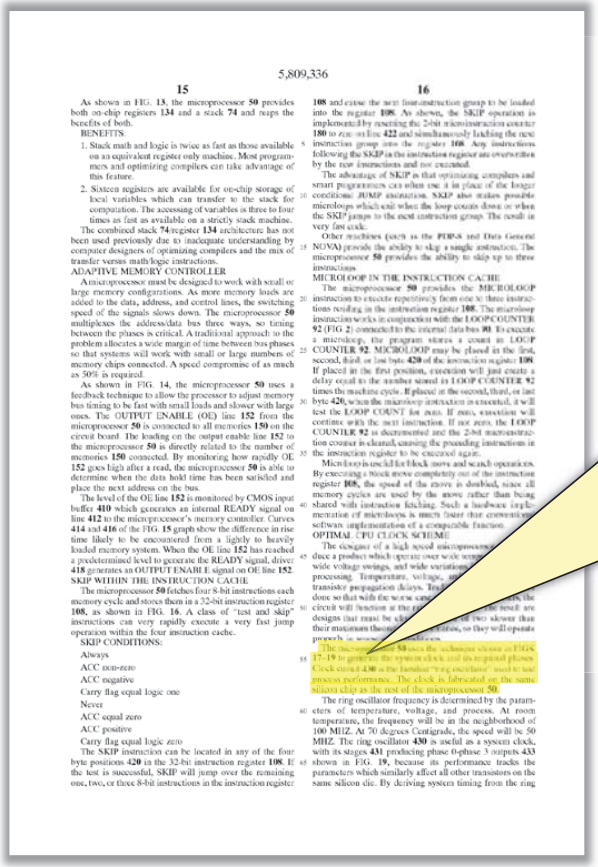
"ring oscillator"

Respondents have proven no clear and unambiguous disavowal of control of the ring oscillator

- The term "non-controllable" does not appear in the claims or the specification

"ring oscillator"

The specification reinforces the understanding that "ring oscillator" has its common and ordinary meaning



5,809,336

15 16

As shown in FIG. **13**, the microprocessor **50** provides both on-chip registers **134** and a stack **74** and reaps the benefits of both.

BENEFITS:

1. Stack math and logic is twice as fast as those available on an equivalent register only machine. Most programmers and optimizing compilers can take advantage of this feature.
2. Sixteen registers are available for on-chip storage of local variables which can transfer to the stack for computation. The accessing of variables is three to four times as fast as available on a strictly stack machine.

The combined stack **74**/register **134** architecture has not been used previously due to inadequate understanding by computer designers of optimizing compilers and the mix of transfer versus math/logic instructions.

ADAPTIVE MEMORY CONTROLLER

A microprocessor must be designed to work with small or large memory configurations. As more memory loads are added to the data, address, and control lines, the switching speed of the signals slows down. The microprocessor **50** multiplexes the address/data bus three ways, so timing between the phases is critical. A traditional approach to the problem allocates a wide margin of time between bus phases so that systems will work with small or large numbers of memory chips connected. A speed compromise of as much as 50% is required.

As shown in FIG. **14**, the microprocessor **50** uses a feedback technique to allow the processor to adjust memory bus timing to be fast with small loads and slower with large ones. The OUTPUT ENABLE (OE) line **152** from the microprocessor **50** is connected to all memories **150** on the circuit board. The loading on the output enable line **152** to the microprocessor **50** is directly related to the number of memories **150** connected. By monitoring how rapidly OE **152** goes high after a read, the microprocessor **50** is able to determine when the data hold time has been satisfied and place the next address on the bus.

The level of the OE line **152** is monitored by CMOS input buffer **410** which generates an internal READY signal on line **412** to the microprocessor's memory controller. Curves **414** and **416** of the FIG. **15** graph show the difference in rise time likely to be encountered from a lightly to heavily loaded memory system. When the OE line **152** has reached a predetermined level to generate the READY signal, driver **418** generates an OUTPUT ENABLE signal on OE line **152**.

SKIP WITHIN THE INSTRUCTION CACHE

The microprocessor **50** fetches four 8-bit instructions each memory cycle and stores them in a 32-bit instruction register **108**, as shown in FIG. **16**. A class of "test and skip" instructions can very rapidly execute a very fast jump operation within the four instruction cache.

SKIP CONDITIONS:

Always
ACC non-zero
ACC negative
Carry flag equal logic one
Never
ACC equal zero
ACC positive
Carry flag equal logic zero

The SKIP instruction can be located in any of the four byte positions **420** in the 32-bit instruction register **108**. If the test is successful, SKIP will jump over the remaining one, two, or three 8-bit instructions in the instruction register **108** and cause the next four-instruction group to be loaded into the register **108**. As shown, the SKIP operation is implemented by resetting the 2-bit microinstruction counter **180** to zero on line **422** and simultaneously latching the next instruction group into the register **108**. Any instructions following the SKIP in the instruction register are overwritten by the new instructions and not executed.

The advantage of SKIP is that optimizing compilers and smart programmers can often use it in place of the longer conditional JUMP instruction. SKIP also makes possible microloops which exit when the loop counts down or when the SKIP jumps to the next instruction group. The result is very fast code.

Other machines (such as the PDP-8 and Data General NOVA) provide the ability to skip a single instruction. The microprocessor **50** provides the ability to skip up to three instructions.

MICROLOOP IN THE INSTRUCTION CACHE

The microprocessor **50** provides the MICROLOOP instruction to execute repetitively from one to three instructions residing in the instruction register **108**. The microloop instruction works in conjunction with the LOOP COUNTER **92** (FIG. **2**) connected to the internal data bus **90**. To execute a microloop, the program stores a count in LOOP COUNTER **92**. MICROLOOP may be placed in the first, second, third, or last byte **420** of the instruction register **108**. If placed in the first position, execution will just create a delay equal to the number stored in LOOP COUNTER **92** times the machine cycle. If placed in the second, third, or last byte **420**, when the microloop instruction is executed, it will test the LOOP COUNT for zero. If zero, execution will continue with the next instruction. If not zero, the LOOP COUNTER **92** is decremented and the 2-bit macroinstruction counter is cleared, causing the preceding instructions in the instruction register to be executed again.

Microloop is useful for block moves and search operations. By executing a block move completely out of the instruction register **108**, the speed of the move is doubled, since all memory cycles are used by the move rather than being shared with instruction fetching. Such a hardware implementation of microloops is much faster than conventional software implementation of a comparable function.

OPTIMAL CPU CLOCK SCHEME

The designer of a high speed microprocessor must produce a product which operate over wide temperature, wide voltage swings, and wide variations in transistor processing. Temperature, voltage, and transistor propagation delays. To be done so that with the worst case circuit will function at the The result are designs that must be clocked and two slowest than their maximum theoretical frequencies, so they will operate properly at

The ring oscillator frequency is determined by the parameters of temperature, voltage, and process. At room temperature, the frequency will be in the neighborhood of 100 MHZ. At 70 degrees Centigrade, the speed will be 50 MHZ. The ring oscillator **430** is useful as a system clock, with its stages **431** producing phase 0-phase 3 outputs **433** shown in FIG. **19**, because its performance tracks the parameters which similarly affect all other transistors on the same silicon die. By deriving system timing from the ring

"The microprocessor 50 uses the technique shown in FIGS. 17-19 to generate the system clock and its required phases. Clock circuit 430 is the familiar "ring oscillator" used to test process performance. The clock is fabricated on the same silicon chip as the rest of the microprocessor 50."

JXM-0001 ('336 patent) col. 16:54-58

"ring oscillator"

Respondents have proven no clear and unambiguous disavowal of control of the ring oscillator

- The term "non-controllable" does not appear in the claims or the specification
- The term "non-controllable" is itself ambiguous

"Courts construe claim terms in order to assign a fixed, unambiguous, legally operative meaning to the claim."

Chimie v. PPG Indus., Inc., 402 F.3d 1371, 1378 (Fed. Cir. 2005) ("dust free" could not be interpreted to mean "very low dust" because the latter is a relative phrase and thus ambiguous and indefinite)

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- In the '148 patent re-examination prosecution history, the Examiner – *not the patentee* – used the term "non-controllable"

"ring oscillator"

- In the '148 patent re-examination prosecution history, the Examiner – *not the patentee* – used the term "non-controllable" in summarizing a multi-issue interview

Continuation of Description of the general nature of what was agreed to if an agreement was reached, or any other comments:

Discussed differences in the prior art and the claimed invention. Particularly, the patent owner argued that the references failed to teach of the limitation requiring "said memory further occupying a majority of the total area of said single substrate". The patent owner further pointed out that the reference of May, noted above, describes that the memory can be the largest and densest component on the chip, but this is different than being the "majority of the total area",

Continuing, the patent owner further argued that the reference of Talbot does not teach of a "ring oscillator". The patent owner discussed features of a ring oscillator, such as being non-controllable, and being variable based on the environment. The patent owner argued that these features distinguish over what Talbot teaches. The examiner will reconsider the current rejection based on a forthcoming response, which will include arguments similar to what was discussed.

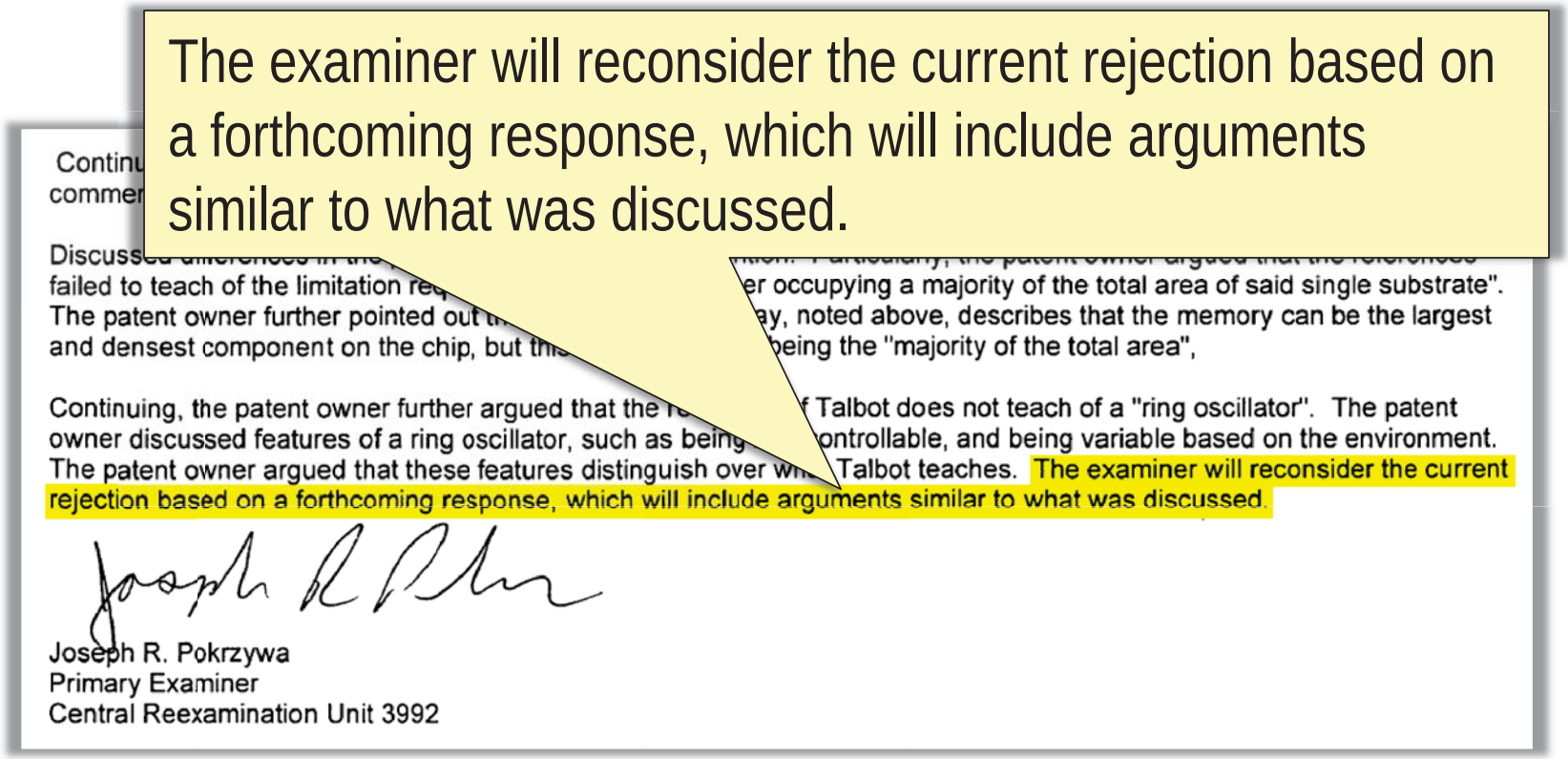
Joseph R. Pokrzywa
Primary Examiner
Central Reexamination Unit 3992

JXM-0014 (2/08 interview summary) at TPL853_02954312

"ring oscillator"

- The Examiner made clear that his decision on patentability would be based on a later written submission from the patentee.

The examiner will reconsider the current rejection based on a forthcoming response, which will include arguments similar to what was discussed.



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"ring oscillator"

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- The term "non-controllable" is itself ambiguous
- In the '148 patent re-examination prosecution history, the Examiner – *not the patentee* – used the term "non-controllable"
- The patentee's written submission distinguished the Talbot reference because Talbot lacked a ring oscillator, never mentioning a requirement of "non-controllability"

"ring oscillator"

- The patentee's written submission distinguished the Talbot reference because Talbot lacked a ring oscillator, never mentioning a requirement of "non-controllability"

Further, Talbot does not teach, disclose, or suggest the ring oscillator recited in claim 4. The Examiner cited col. 3, ll. 26-36, and oscillator circuit 12 shown in FIG. 1 of Talbot as teaching the recited ring oscillator. Talbot discusses a voltage-controlled oscillator (VCO) 12, but does not teach or disclose a ring oscillator. Talbot provides two different implementations of the VCO 12 in FIGS. 3-4, neither one of which is a ring oscillator. Talbot refers to the oscillator of FIG. 3 as a "frequency controlled oscillator" (col. 7, ll. 21-22) and the oscillator of FIG. 4 simply as a "voltage controlled oscillator" (col. 8, ll. 59-65). As the sole inventor of the cited reference, Talbot presumably possesses at least ordinary skill in the art, yet Talbot did not characterize either of the disclosed oscillators as ring oscillators. Applicants respectfully assert that the reason they were not characterized by Talbot as ring oscillators is because they are not ring oscillators. For at least the foregoing reasons, Talbot does not teach, disclose, or suggest a ring oscillator as recited in the claims.

JXM-0010 (2/08 Am.) at TPL853_02954325

"ring oscillator"

- The Examiner expressly relied on the patentee's written submission as "persuasive," and allowed the claims without requiring or mentioning "non-controllable"

Response to Arguments

7. Patent Owner's arguments, filed 2/26/08, with respect to the rejection(s) of **claim(s) 4, 7, 8, and 10** under 35 U.S.C.103(a) as being unpatentable over U.S. Patent Number 4,689,581, issued to Talbot, Gerald R. (referred to as "Talbot'581") in view of European Patent Publication EP 0 113 516, issued to May, Michael D., being European Patent Application No. 83307078.2 (referred to as "May'516"), have been fully considered and are persuasive. Therefore, the rejection, as cited in the previous Office action, has been withdrawn.

CXM-0009 (6/08 office action) at TPL853_02954489

"ring oscillator"

Allegedly disavowing statements must be both "so clear as to show reasonable clarity and deliberateness, and unmistakable as to show unambiguous evidence of disclaimer" in order for a court to limit the meaning of a claim term.

Omega Eng'g, Inc. v. Raytek Corp., 334 F3.d 1314, 1325 (Fed. Cir. 2003)

Where an "examiner and applicant [are] talking past one another" and "the record finally reflects the examiner's acquiescence to the claim language chosen by the applicant, [t]his is not clear evidence of the patentee's disavowal of claim scope."

Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc., 381 F.3d 1111, 1124 (Fed. Cir. 2004)

"ring oscillator"

The original prosecution of the '336 patent includes no disavowal of control of the ring oscillator

- The word "non-controllable" appears ***nowhere*** in the '336 patent prosecution history.
- Patentees did not disclaim any and all control of ring oscillators
- Patentees distinguished the prior art on very narrow grounds which did not disclaim all use of voltage controlled oscillators in the '336 invention

"ring oscillator"

"The placement of these elements within the same integrated circuit obviates the need for provisions of the type of frequency control information described by Sheets."

JXM-0017 (4/96 Am., Responding to rejection over Sheets) at TPL853 02954574

"In Sheets, a command input is required to change the clock speed [but in] the present invention . . . [n]o command input is necessary to change the clock frequency."

JXM-0021 (1/97 Am., Responding to rejection over Sheets) at TPL853_00002449

"[T]he oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so."

JXM-0018 (7/97 Am., Responding to rejection over Magar) at TPL853_00002429

"ring oscillator"

Respondents have proven no clear and unambiguous disavowal of control of the ring oscillator

- The term "non-controllable" does not appear in the claims or the specification
- The term "non-controllable" is itself ambiguous
- In the '148 patent re-examination prosecution history, the Examiner – *not the patentee* – used the term "non-controllable"
- The patentee's written submission distinguished the Talbot reference because Talbot lacked a ring oscillator, never mentioning a requirement of "non-controllability"
- The original prosecution history includes no clear and unmistakable disclaimer of all voltage controlled oscillators

"ring oscillator"

Respondents Want to Import Two Extraneous Limitations:

Respondents' Construction

An oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is: (1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters in the environment.

"ring oscillator"

The Claims Already Address Variations Due to Manufacturing/Process, Voltage and Temperature

Already in Claims 1 and 11	What Respondents Want to Add to "ring oscillator"
"varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit"	variable based on the temperature, voltage, and process parameters in the environment

"ring oscillator"

"In the Environment" Is Superfluous and Ambiguous

- Phrase "in the environment" is not in the claims
- Phrase "in the environment" is not in the specification
- Phrase "environmental parameters" was used during prosecution *only* to refer to temperature and voltage, not manufacturing variations

Respondents improperly seek to rely on inventor testimony

In *Howmedica*, the accused infringer attempted to use the inventor's testimony in the same manner the Respondents are here: to narrow the claims.

> It is well settled that "inventor testimony as to the inventor's subjective intent is irrelevant to the issue of claim construction."
>
> *Howmedica Osteonics Corp. v. Wright Medical Tech., Inc.*, 540 F.3d 1337, 1347 (Fed.Cir.2008).

> This is consistent with the long settled precedent of *Markman* itself: "While presumably the inventor has approved any changes to the claim scope that have occurred via amendment during the prosecution process, it is not unusual for there to be a significant difference between what an inventor thinks his patented invention is and what the ultimate scope of the claims is after allowance by the PTO."
>
> *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 985 (Fed.Cir.1995).

"ring oscillator"

TPL's Claim Construction

Interconnected electronic components comprising multiple odd numbers of inversions arranged in a loop, where three or more inversions are required to maintain an oscillating output

CPU Clock-Related Terms

- "ring oscillator"
- "entire oscillator/clock" – *claims 1, 6, 10, 11, 13, 16*
- "varying" limitations terms
- "thereby enabling said processing frequency to track said clock rate in response to said parameter variation"
- "clocking said CPU"
- "operates asynchronously to"

"entire oscillator/clock"

TPL's Construction	Respondents' Construction	Staff's Construction
a ring oscillator, variable speed system clock, wherein the ring oscillator is located entirely on the same semiconductor substrate as the central processing unit	a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU **and does not rely on a control signal or an external crystal/clock generator to generate a clock signal**	a ring oscillator variable speed system clock that includes all components that determine clock frequency located on the same semiconductor substrate as the CPU

The Parties Agree on at Least a Portion of the Construction

TPL's Construction	Respondents' Construction	Staff's Construction
a ring oscillator, variable speed system clock, wherein the ring oscillator is located entirely on the same semiconductor substrate as the central processing unit	a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an external crystal/clock generator to generate a clock signal	a ring oscillator variable speed system clock that includes all components that determine clock frequency located on the same semiconductor substrate as the CPU

"entire oscillator/clock"

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a ring oscillator, variable speed system clock, wherein the ring oscillator is located entirely on the same semiconductor substrate as the central processing unit	a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an external crystal/clock generator to generate a clock signal	a ring oscillator variable speed system clock that includes all components that determine clock frequency located on the same semiconductor substrate as the CPU

"entire oscillator/clock"

Staff Also Wants to Import An Extraneous Limitation:

TPL's Construction	Respondents' Construction	Staff's Construction
a ring oscillator, variable speed system clock, wherein the ring oscillator is located entirely on the same semiconductor substrate as the central processing unit	a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU **and does not rely on a control signal or an external crystal/clock generator to generate a clock signal**	a ring oscillator variable speed system clock that includes all components that determine clock frequency located on the same semiconductor substrate as the CPU

During prosecution, the Applicants made it clear that Sheets was fundamentally different from the '336 invention

Regarding the '336 invention:

"Applicants again observe that the present invention is directed to a system and method for clocking a central processing unit disposed *within the same integrated circuit* as a ring oscillator variable speed system clock. This allows, for example, the central processing unit to track variations in the speed of the ring oscillator variable speed system clock, since the elements of each are disposed in the same integrated circuit."

JXM-0017 (4/96 Am.) at TPL853_02954573 (emphasis in original)

Regarding Sheets:

"Sheets describes the use of discrete, commercially available microprocessor chips, e.g., the Motorola 68000 (col. 5, line 16), driven by a *separate* clock (VCO) 12 of FIG. 1). . . [S]uch microprocessor chips include terminals or pins, such as the CLK and INT terminals of microprocessor (FIG. 1), for receiving inputs from external devices like the VCO 12 and fixed oscillator 103. Because *the VCO 12 is not integral with the microprocessor 101*, Sheets has proposed a technique for adjusting the frequency of VCO 12 in accordance with a desired operating frequency of the microprocessor 101."

JXM-0017 (4/96 Am.) at TPL853_02954574 (emphasis added)

Sheets is fundamentally different from the '336 invention

United States Patent [19]

Sheets

[11] **Patent Number: 4,670,837**

[45] **Date of Patent: Jun. 2, 1987**

[54] **ELECTRICAL SYSTEM HAVING VARIABLE-FREQUENCY CLOCK**

[75] Inventor: **Laurence L. Sheets**, St. Charles, Ill.

[73] Assignees: **American Telephone and Telegraph Company; AT&T Bell Laboratories**, both of Murray Hill, N.J.

[21] Appl. No.: **624,469**

[22] Filed: **Jun. 25, 1984**

[51] **Int. Cl.**[4] **H03K 5/04**

[52] **U.S. Cl.** **364/200**; 328/38.1

[58] **Field of Search** 364/200, 900; 328/62, 328/38; 365/222

[56] **References Cited**

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4,037,090	7/1977	Raymond, Jr.	364/200
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4,241,418	12/1980	Stanley	364/900
4,331,924	5/1982	Elliot et al.	328/38
4,414,637	11/1983	Stanley	364/569
4,438,490	3/1984	Wilder, Jr.	364/200
4,447,870	5/1984	Tague et al.	364/200
4,463,440	7/1984	Nishiura et al.	364/900

FOREIGN PATENT DOCUMENTS

0098653	6/1983	European Pat. Off. .
2248170	4/1974	Fed. Rep. of Germany .

Primary Examiner—Gareth D. Shaw
Assistant Examiner—Randy W. Lacasse
Attorney, Agent, or Firm—Ross T. Watland

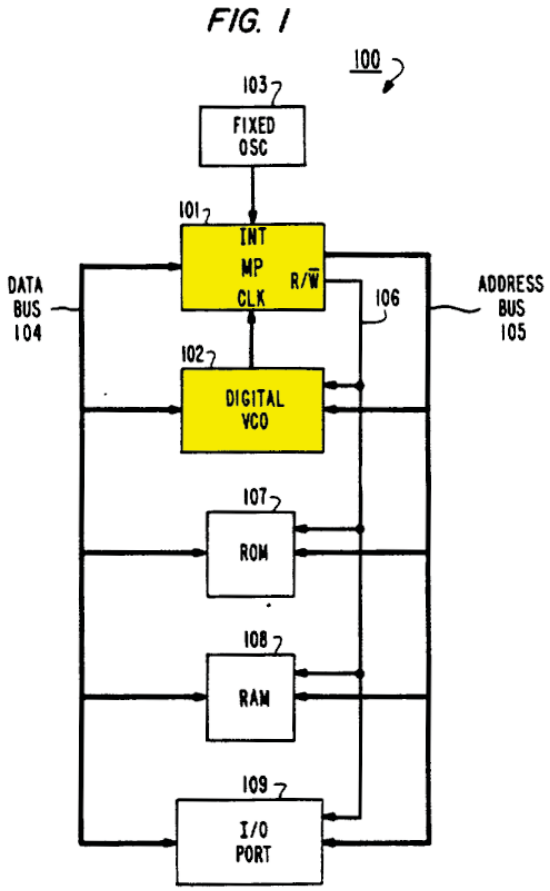
[57] **ABSTRACT**

The microprocessor unit of a system implemented using metal-oxide-silicon (MOS) technology, is driven by a variable-frequency clock. The microprocessor controls the clock frequency based on the present rate of required microprocessor activity. By driving the microprocessor unit at a lower clock frequency when such activity rate is low, the energy dissipated by the microprocessor unit is reduced due to the MOS power-frequency characteristic.

7 Claims, 6 Drawing Figures

Sheets is fundamentally different from the ’336 invention

Sheets ’837 Patent, Fig. 1



“FIG. 1 is a block diagram of an exemplary microprocessor-based system 100 illustrating the principles of the present invention. The system is controlled by a microprocessor 101 which communicates with associated devices via a data bus 104 and an address bus 105.”

RXM-0021 (’837 patent) col. 2:7-11

“It is to be recognized that any of a number of microprocessor families can be advantageously used in such systems. One specific example is the Motorola 68000 microprocessor and its associated devices.”

RXM-0021 (’837 patent) col. 5:13-17

Sheets is fundamentally different from the ’336 invention

The applicants correctly observed that the Sheets microprocessor chip (101) used a *separate off-chip clock* (VCO 102).

> “Sheets describes the use of discrete, commercially available microprocessor chips, e.g., the Motorola 68000 (col. 5, line 16), driven by a *separate* clock (VCO) 12 of FIG. 1). . . [S]uch microprocessor chips include terminals or pins, such as the CLK and INT terminals of microprocessor (FIG. 1), for receiving inputs from external devices like the VCO 12 and fixed oscillator 103. Because *the VCO 12 is not integral with the microprocessor 101*, Sheets has proposed a technique for adjusting the frequency of VCO 12 in accordance with a desired operating frequency of the microprocessor 101.”
>
> *JXM-0017 (4/96 Am.) at TPL853_02954574 (emphasis added)*

Sheets is fundamentally different from the ’336 invention

Contrasting Sheets from ’336 invention:

“The present invention does *not* similarly rely upon provision of frequency control information *to an external clock*, but instead contemplates providing *a ring oscillator clock* and the *microprocessor* within the *same integrated circuit*. . . Sheets’ system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.”

JXM-0017 (4/96 Am.) at TPL853_02954574 (emphasis added)

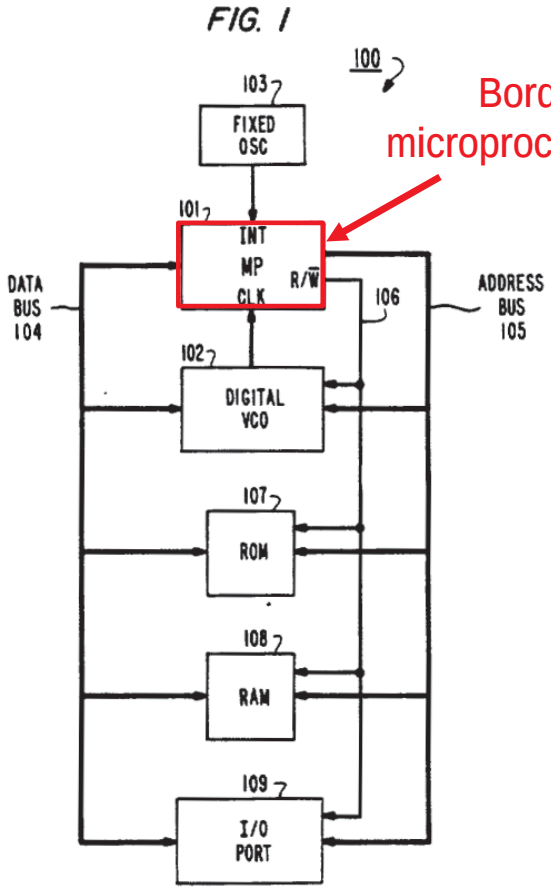
Contrasting Sheets from ’336 invention:

“[C]laims 19 and 65 now explicitly recite that the *ring oscillator* and *microprocessor* are provided *within the same integrated circuit*. Moreover, these claims further state that the plurality of transistors included within the ring oscillator clock have operating characteristics which vary similarly to operating characteristics of transistors included within the microprocessor, thereby enabling the processing frequency of the microprocessor to track the speed of the ring oscillator clock”

JXM-0017 (4/96 Am.) at TPL853_02954574 (emphasis added)

Sheets is fundamentally different from the ’336 invention

Sheets ’837 Patent, Fig. 1



’336 Patent, Fig. 17

Border of microprocessor chip

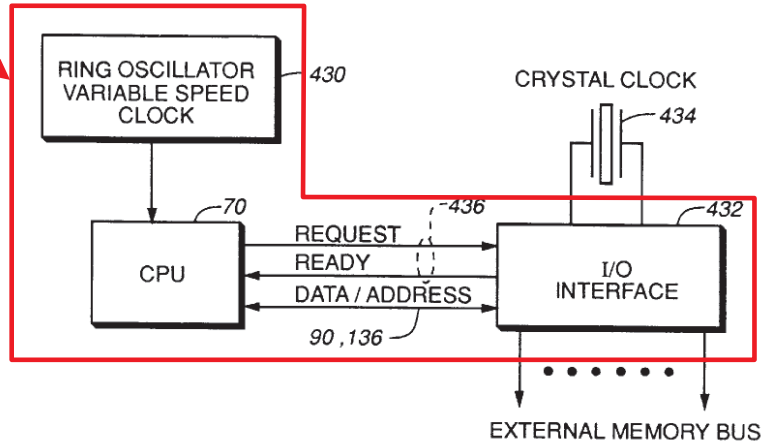


FIG._17

The Applicants only disclaimed the specific disclosure of Sheets: Requiring a command input signal to change the speed of an off-chip clock

After a further rejection based on Sheets, the Applicant successfully rebutted the Examiner's contention that the system of Sheets was on a single chip:

> "[T]he Examiner contends that the Sheets reference 'clearly indicates . . . that the system 100 shown in Figure 1 is fabricated *on a single chip* using MOS technology.' Specific issue is taken with the inclusion of the italicized language in this characterization of the reference. Sheets does not say that the system 100 is on a single chip, only that it is implemented in MOS technology. At column 5, lines 15-17, a specific example of the Motorola 68000 is given. That microprocessor is driven by an external clock that provides a clock signal to a designated pin of the microprocessor integrated circuit package."
>
> *JXM-0021 (1/97 Am.) at TPL853_0000249 (italics in original)*

The Applicants only disclaimed the specific disclosure of Sheets: Requiring a command input signal to change the speed of an off-chip clock

- Next, the Applicant observed that the invention of Sheets *required* the microprocessor to provide a command input control signal to an *external* clock:

> "Even if the Examiner is correct that the variable clock in Sheets is in the same integrated circuit as the microprocessor of system 100, that still does not give the claimed subject matter. In Sheets, a command input is *required* to change the clock speed. In the present invention, the clock speed varies correspondingly to variations in operating parameters of the electronic devices of the microprocessor because both the variable speed clock and the microprocessor are fabricated together in the same integrated circuit. No command input is *necessary* to change the clock frequency."
>
> *JXM-0017 (4/96 Am.) at TPL853_02954574 (emphasis added)*

- *At most, Applicants disclaimed a requirement that the microprocessor must provide a command input control signal to change the speed of an off-chip clock.*

After giving up on Sheets, the Examiner asserted Magar, which the Applicants observed was also very different from the '336 invention

The Applicants observed that Magar used a prior art clocking system:

> "A review of the Magar reference shows that it is apparently no more pertinent than prior art acknowledged in the application, in that the clock disclosed in the Magar reference is in fact driven by a fixed frequency crystal, which is external to the Magar integrated circuit."
>
> *JXM-0018 (7/97 Am.) at TPL853_00002426 (emphasis added)*

> "The clock gen circuit shown at the lower right hand edge of Fig. 2a in the Magar patent is of the same general type as shown at 434 in Fig. 17 of the present application, but depicted differently in that it shows the clock gen circuit portion which is on the semiconductor substrate, while Fig. 17 shows the external crystal at 434, connected to I/O interface 432 in the present invention."
>
> *JXM-0018 (7/97 Am.) at TPL853_00002426 (emphasis added)*

Magar is fundamentally different from the ’336 invention

’336 Patent, Fig. 17

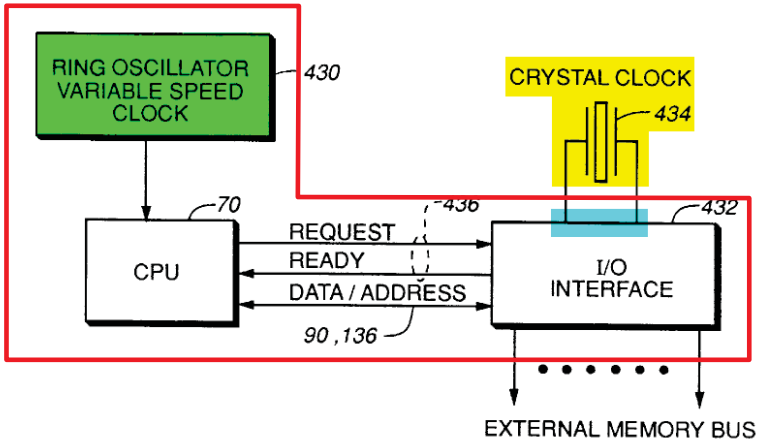
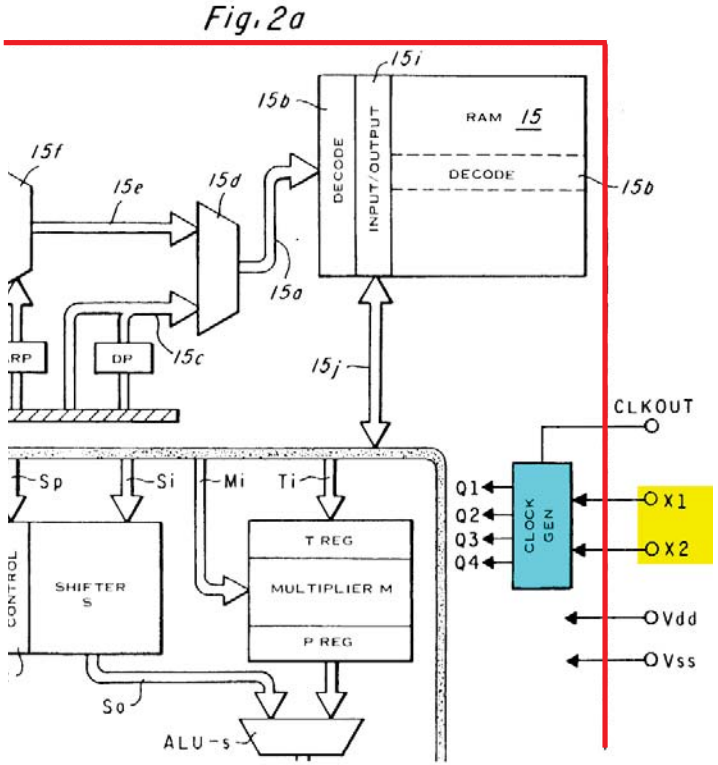


FIG._17

Magar ’500 Patent, Fig. 2a



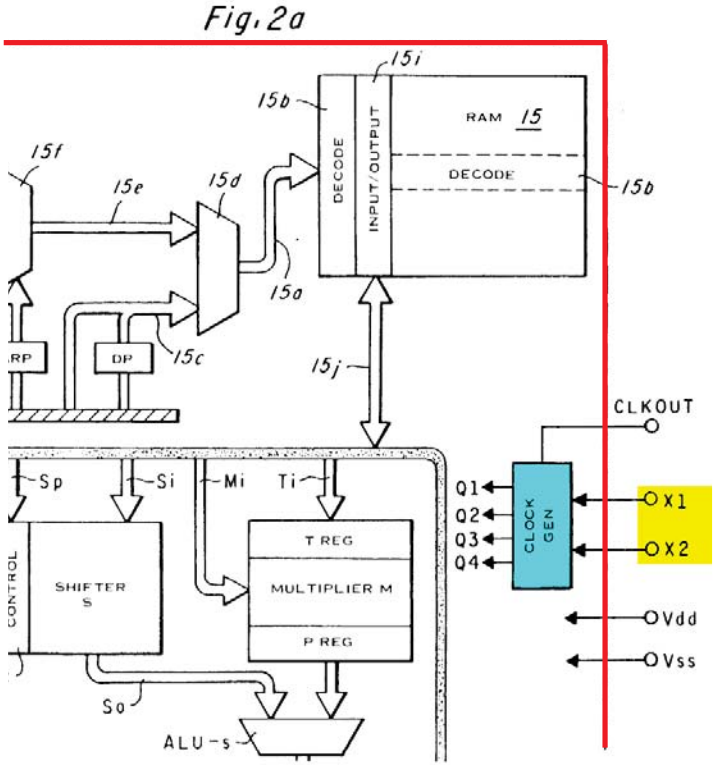
CDXM-0001.052

Magar is fundamentally different from the ’336 invention

“The chip 10 includes a clock generator 17 which has two external pins X1 and X2 to which a crystal (or external generator) is connected. The basic crystal frequency is up to 20 MHz and is represented by a clock 0 of FIG. 3a. This clock 0 has a period of 50 ns, minimum, and is used to generate four quarter-cycle clocks Q1, Q2, Q3 and Q4 seen in FIGS. 3b-3e, providing the basic internal timing for the microcomputer chip 10. A set of four quarter cycle clocks Q1 to Q4 defines one machine state time of 200 ns, minimum; the states are referred to as S0, S1, S2, in FIG. 3.”

JXM-0015 (’500 patent) col. 15:26-36

Magar ’500 Patent, Fig. 2a



CDXM-0001.053

Magar is fundamentally different from the ’336 invention

The Applicants observed regarding Magar:

> “[I]t is clear that *the element in Fig. 17 missing from Fig. 2a in Magar is the ring counter variable speed clock 430*, and that Magar is merely representative of the ‘most microprocessors’ acknowledged as prior art in the above description from the present application, which prior art microprocessors use a ‘conventional crystal clock.’”
>
> *JXM-0018 (7/97 Am.) at TPL853_00002427*

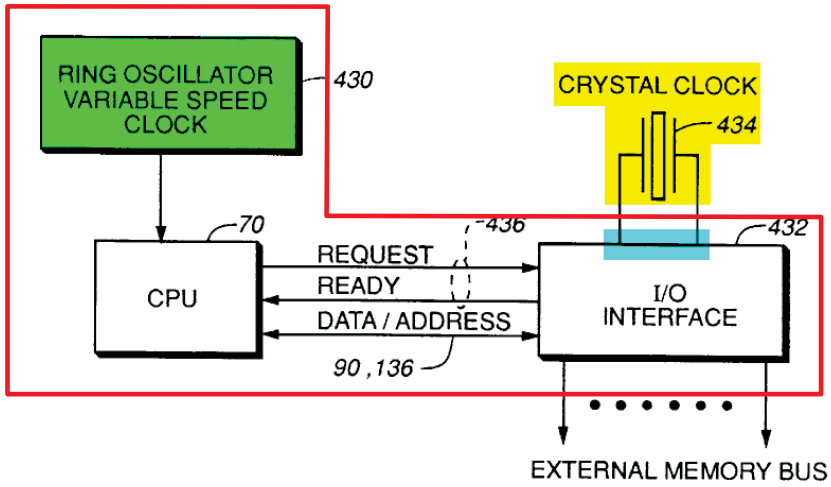


FIG._17

Magar is fundamentally different from the '336 invention

In Magar, the CPU was clocked by an external crystal:

"[O]ne of ordinary skill in the art should readily recognize that the speed of the cpu and the clock [in Magar] *do not* vary together due to manufacturing variation, operating voltage and temperature of the IC in the Magar microprocessor, as taught in the quotation from the reference. This is simply because the Magar microprocessor clock is frequency controlled by a crystal which is also *external* to the microprocessor."

JXM-0018 (7/97 Am.) at TPL853_00002427-28

However, the Examiner still did not understand Magar:

"In the communication filed on July 07, 1997, applicants contend that Magar's clock is external to the IC. . . The clock is clearly on-chip."

10/16/97 Office Action, p. 3

Applicants' addition of "entire" emphasized that all of the circuitry for the oscillator must be on the same chip as the CPU

In a February 1998 Amendment, the Applicants added "entire" to make clear that all of the oscillator circuitry must be on the same chip as the CPU:

> "[T]he independent claims have been rewritten to specify that the entire ring oscillator variable speed system clock, variable speed clock or oscillator be provided in the integrated circuit, in order to sharpen the distinction over the prior art."
>
> *JXM-0016 (02/98 Am.) at TPL853_02954559*

Applicants also observed that the Magar clock COULD NOT oscillate without the external crystal:

> "[T]here would be no 'tracking' of the clock rate produced by the Magar clock generator, because the entire circuit is not provided on the integrated circuit. Magar's clock generator *relies on* an external crystal connected to terminals X1 and X2 to oscillate, as is conventional in microprocessor designs. *It is not an entire oscillator in itself*."
>
> *JXM-0016 (02/98 Am.) at TPL853_02954559*

Applicants' addition of "entire" emphasized that all of the circuitry for the oscillator must be on the same chip as the CPU

Applicants observed that the Magar system REQUIRED an off-chip crystal to oscillate:

> "Thus while most of Magar's clock (generator) circuitry is on the IC, the entire oscillator, which because it *requires* an external crystal, is not."
>
> *JXM-0016 (02/98 Am.) at TPL853_02954560*

> "Magar's clock gen is distinguished from an oscillator in at least that it lacks the crystal or external generator *that it requires*. Thus Magar's circuit is not an entirely on-chip oscillator as contemplated in the present case . . ."

By contrast, Applicants observed that the "ring oscillator variable speed system clock (430)" is an entirely on-chip oscillator:

> Ring oscillator "430 is both an oscillator and a clock in the conventional senses. It is an oscillator in that it oscillates without external components (unlike the Magar reference)."
>
> *JXM-0016 (02/98 Am.) at TPL853_02954560*

"entire ring oscillator"/"entire oscillator"

- During the first reexamination proceeding, NEC confirmed:
  - Magar's CLOCK GEN is not an oscillator
  - The off-chip crystal oscillator output is the CPU clock

> Magar shows "CLOCK GEN" circuitry on the right-hand side of Fig. 2A that is on a single substrate with the CPU. The CLOCK GEN circuitry, however, has crystal oscillator inputs X1 and X2. This leads to the supposition that CLOCK GEN is not a resonator itself, but rather circuitry that amplifies, filters or otherwise prepares the crystal resonator output for use as a CPU clock.
>
> *CXM-0021 at TPL8530292804-05*

"entire ring oscillator"/"entire oscillator"

The Staff improperly imports unsupported limitations

- Staff imports limitations into the claimed oscillator: "all components"

- Staff's construction would include all components that affect the:
  - Voltage, such as power supplies and voltage regulators.
  - Temperature, such as heat sinks and fans.
  - Manufacturing process, such as the equipment used to manufacturing the integrated circuit.

- Thus, the Staff's construction is irreparably broad and should be rejected.

"entire ring oscillator"/"entire oscillator"

TPL's Construction
a ring oscillator, variable speed system clock, wherein the ring oscillator is located entirely on the same semiconductor substrate as the central processing unit

CPU Clock-Related Terms

- "ring oscillator"
- "entire oscillator/clock"
- "varying" limitations terms – *claims 1, 6, 10-11, 13, 16*
- "thereby enabling said processing frequency to track said clock rate in response to said parameter variation"
- "clocking said CPU"
- "operates asynchronously to"

"varying" limitations terms

TPL's Construction	Respondents' and Staff's Construction
No construction necessary. But if construed: "changing in a corresponding manner"	Increasing and decreasing **proportionally**

"varying" limitations terms

- Respondents seek to import an extraneous, unsupported limitation not found anywhere

"varying" limitations terms

- Respondents seek to import an extraneous, unsupported limitation not found anywhere
- Nothing in the claims requires a "proportional" relationship between the clock and the CPU
  - The terms "varying together" and "varying in the same way"
    - Do not invoke a mathematical relationship
    - Loosely convey that the '336 invention takes advantage of the laws of physics

"varying" limitations terms

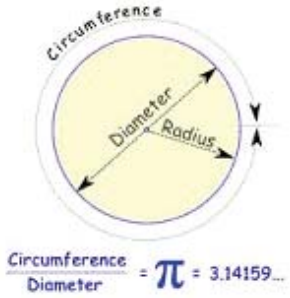
- Respondents seek to import an extraneous, unsupported limitation not found anywhere
- Nothing in the claims requires a "proportional" relationship between the clock and the CPU
- Nothing in the specification teaches a "proportional" relationship between the clock and the CPU
  - Specification only loosely defines the relationship
  - For example, the ring oscillator performance "tracks the parameters which *similarly affects* all transistors on the die" including the transistors of the CPU. *'336 at 6:65-67*

"varying" limitations terms

- Respondents seek to import an extraneous, unsupported limitation not found anywhere
- Nothing in the claims requires a "proportional" relationship between the clock and the CPU
- Nothing in the specification teaches a "proportional" relationship between the clock and the CPU
- Nothing in the prosecution history supports Respondents' construction
  - Neither the term "proportional" nor "proportionally" is ever used
  - The prosecution history merely acknowledges that transistors manufactured on the same substrate will be affected in a similar or "corresponding" manner with respect to PVT

"varying" limitations terms

- Respondents seek to import an extraneous, unsupported limitation not found anywhere
- Nothing in the claims requires a "proportional" relationship between the clock and the CPU
- Nothing in the specification teaches a "proportional" relationship between the clock and the CPU
- Nothing in the prosecution history supports Respondents' construction
- "Proportionality" may imply a mathematical relationship when none is required in the intrinsic evidence



"varying" limitations terms

Judicial Estoppel Does Not Apply

- TPL's current position is not "clearly inconsistent" with it's earlier position

"varying" limitations terms

Judicial Estoppel Does Not Apply

- TPL's current position is not "clearly inconsistent" with it's earlier position
  - TPL has consistently opposed any claim construction that expressly imports a mathematical relationship.
    - The accused infringers in NDCA tried unsuccessfully to import a mathematical relationship requirement through the construction of "as a function of parameter variation"
    - Judge Ware flatly rejected any requirement of a mathematical relationship.
    - TPL now opposes the importation of a mathematical relationship through use of "proportionally."

"varying" limitations terms

Judicial Estoppel Does Not Apply

- TPL's current position is not "clearly inconsistent" with it's earlier position
- TPL derives no "unfair advantage" from its position.

"varying" limitations terms

Judicial Estoppel Does Not Apply

- TPL's current position is not "clearly inconsistent" with it's earlier position
- TPL derives no "unfair advantage" from its position.
  - TPL has consistently opposed any imposition of a mathematical relationship on the varying limitations.
  - Respondents will obtain an unfair advantage if "proportionally" is used to import a mathematical limitation.
- If "proportionally" is adopted, it should be accompanied with clarification that no mathematical relationship is required.

CPU Clock-Related Terms

- "ring oscillator"
- "entire oscillator/clock"
- "varying" limitations terms
- "thereby enabling said processing frequency to track said clock rate in response to said parameter variation" – *claims 6, 13*
- "clocking said CPU"
- "operates asynchronously to"

"thereby enabling said processing frequency to track said clock rate in response to said parameter variation"

TPL's Construction	Respondents' and Staff's Construction
thereby enabling the processing frequency of the central processing unit to follow said clock rate in response to said parameter variation	said parameter variation **directly causing** said processing frequency to track said clock rate

"thereby enabling"

- Two major problems:
  - Respondents ignore the words "thereby enabling"
  - Respondents ignore preceding structural claim limitations.

"thereby enabling"

Respondents ignore the words "thereby enabling"

Proper claim construction begins with the words of the claims themselves.

Vitronics Corp. v. Conceptronic, Inc., 90 F.3d1576, 1582 (Fed. Cir. 1996)

"Words of a claim 'are generally given their ordinary and customary meaning.'"

Philips v. AWH Corp., 415 F.3d 1303, 1313 (Fed. Cir. 2005) (citing Vitronics, 90 F.3d at 1582)

"thereby enabling"

Respondents ignore the words "thereby enabling"

- "thereby enabling" plainly means "allowing" or "making possible"
- "thereby enabling" <u>does not mean</u> "directly causing"

"thereby enabling"

Respondents ignore preceding claim limitations.

Respondents ignore the structural elements preceding "thereby enabling":

- CPU and oscillator are on the same substrate
- Both are constructed of a plurality of electronic devices
- The oscillator is connected to clock the CPU

"thereby enabling"

Respondents ignore preceding claim limitations.

The incorporation of the preceding structural elements results in two inherent attributes:

- "thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate" (claim 6 & 13)

- "thereby enabling said processing frequency to track said clock rate in response to said parameter variation" (claim 6 & 13)

"thereby enabling"

Respondents ignore preceding claim limitations.

The incorporation of the preceding structural elements results in two inherent attributes:

- "thus varying the processing frequency of said first plurality of

Respondents incorrectly assert that parameter variation "directly causes" the processing frequency of the CPU to track the clock rate of the oscillator.

- "thereby enabling said processing frequency to track said clock rate in response to said parameter variation" (claim 6 & 13)

"thereby enabling"

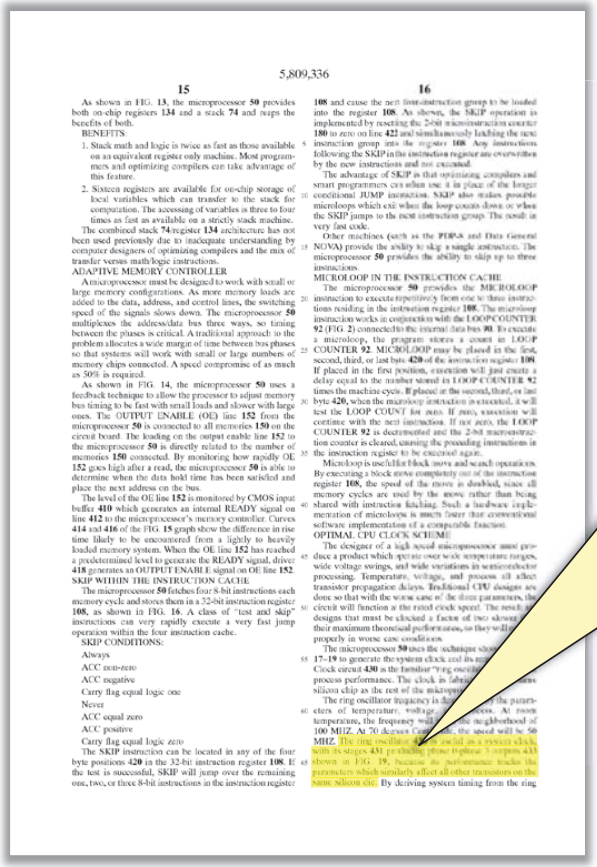
But in their brief, Respondents concede that there is an *indirect* relationship between a parameter variation and processing frequency

"The specification teaches that the PVT parameters (i.e. temperature, voltage, and process) determine the ring oscillator frequency, *which in turn* drives the CPU frequency."

RCCB at 44, emphasis added.

"thereby enabling"

Although the claim language is clear, the specification confirms that "track" means to follow generally, not exactly.



5,809,336

15

As shown in FIG. **13**, the microprocessor **50** provides both on-chip registers **134** and a stack **74** and reaps the benefits of both.

BENEFITS:

1. Stack math and logic is twice as fast as those available on an equivalent register only machine. Most programmers and optimizing compilers can take advantage of this feature.
2. Sixteen registers are available for on-chip storage of local variables which can transfer to the stack for computation. The accessing of variables is three to four times as fast as available on a strictly stack machine.

The combined stack **74**/register **134** architecture has not been used previously due to inadequate understanding by computer designers of optimizing compilers and the mix of transfer versus math/logic instructions.

ADAPTIVE MEMORY CONTROLLER

A microprocessor must be designed to work with small or large memory configurations. As more memory loads are added to the data, address, and control lines, the switching speed of the signals slows down. The microprocessor **50** multiplexes the address/data bus three ways, so timing between the phases is critical. A traditional approach to the problem allocates a wide margin of time between bus phases so that systems will work with small or large numbers of memory chips connected. A speed compromise of as much as 50% is required.

As shown in FIG. **14**, the microprocessor **50** uses a feedback technique to allow the processor to adjust memory bus timing to be fast with small loads and slower with large ones. The OUTPUT ENABLE (OE) line **152** from the microprocessor **50** is connected to all memories **150** on the circuit board. The loading on the output enable line **152** to the microprocessor **50** is directly related to the number of memories **150** connected. By monitoring how rapidly OE **152** goes high after a read, the microprocessor **50** is able to determine when the data hold time has been satisfied and place the next address on the bus.

The level of the OE line **152** is monitored by CMOS input buffer **410** which generates an internal READY signal on line **412** to the microprocessor's memory controller. Curves **414** and **416** of the FIG. **15** graph show the difference in rise time likely to be encountered from a lightly to heavily loaded memory system. When the OE line **152** has reached a predetermined level to generate the READY signal, driver **418** generates an OUTPUT ENABLE signal on OE line **152**.

SKIP WITHIN THE INSTRUCTION CACHE

The microprocessor **50** fetches four 8-bit instructions each memory cycle and stores them in a 32-bit instruction register **108**, as shown in FIG. **16**. A class of "test and skip" instructions can very rapidly execute a very fast jump operation within the four instruction cache.

SKIP CONDITIONS:

Always
ACC non-zero
ACC negative
Carry flag equal logic one
Never
ACC equal zero
ACC positive
Carry flag equal logic zero

The SKIP instruction can be located in any of the four byte positions **420** in the 32-bit instruction register **108**. If the test is successful, SKIP will jump over the remaining one, two, or three 8-bit instructions in the instruction register

16

108 and cause the next four-instruction group to be loaded into the register **108**. As shown, the SKIP operation is implemented by resetting the 2-bit microinstruction counter **180** to zero on line **422** and simultaneously latching the next instruction group into the register **108**. Any instructions following the SKIP in the instruction register are overwritten by the new instructions and not executed.

The advantage of SKIP is that optimizing compilers and smart programmers can often use it in place of the longer conditional JUMP instruction. SKIP also makes possible microloops which exit when the loop counts down or when the SKIP jumps to the next instruction group. The result is very fast code.

Other machines (such as the PDP-8 and Data General NOVA) provide the ability to skip a single instruction. The microprocessor **50** provides the ability to skip up to three instructions.

MICROLOOP IN THE INSTRUCTION CACHE

The microprocessor **50** provides the MICROLOOP instruction to execute repetitively from one to three instructions residing in the instruction register **108**. The microloop instruction works in conjunction with the LOOPCOUNTER **92** (FIG. 2) connected to the internal data bus **90**. To execute a microloop, the program stores a count in LOOP COUNTER **92**. MICROLOOP may be placed in the first, second, third, or last byte **420** of the instruction register **108**. If placed in the first position, execution will just create a delay equal to the number stored in LOOP COUNTER **92** times the machine cycle. If placed in the second, third, or last byte **420**, when the microloop instruction is executed, it will test the LOOP COUNT for zero. If zero, execution will continue with the next instruction. If not zero, the LOOP COUNTER **92** is decremented and the 2-bit macroinstruction counter is cleared, causing the preceding instructions in the instruction register to be executed again.

Microloop is useful for block moves and search operations. By executing a block move completely out of the instruction register **108**, the speed of the move is doubled, since all memory cycles are used by the move rather than being shared with instruction fetching. Such a hardware implementation of microloops is much faster than conventional software implementation of a comparable function.

OPTIMAL CPU CLOCK SCHEME

The designer of a high speed microprocessor must produce a product which operate over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing. Temperature, voltage, and process all affect transistor propagation delays. Traditional CPU designs are done so that with the worst case of the three parameters, the circuit will function at the rated clock speed. The result designs that must be clocked a factor of two slower their maximum theoretical performance, so they will properly in worst case conditions.

The microprocessor **50** uses the technique shown **17–19** to generate the system clock and its Clock circuit **430** is the familiar "ring oscil process performance. The clock is fabri silicon chip as the rest of the microp

The ring oscillator frequency is fu eters of temperature, voltage, pro temperature, the frequency will 100 MHZ. At 70 degrees Centigrade, the speed will be 50 MHZ. The ring oscillator 430 is useful as a system clock, with its stages 431 producing phase 0-phase 3 outputs 433 shown in FIG. 19, because its performance tracks the parameters which similarly affect all other transistors on the same silicon die. By deriving system timing from the ring

"The ring oscillator 430 is useful as a system clock, with its stages 431 producing phase 0-phase 3 outputs 433 shown in FIG. 19, because its performance tracks the parameters which *similarly* affect all other transistors on the same silicon die."

JXM-0001 ('336 patent), col. 16:63-67

CPU Clock-Related Terms

- "ring oscillator"
- "entire oscillator/clock"
- "varying" limitations terms
- "thereby enabling said processing frequency to track said clock rate in response to said parameter variation"
- "clocking said CPU" – *claims 1, 6, 10, 11, 13, 16*
- "operates asynchronously to"

"clocking said CPU"

TPL's and Staff's Construction	Respondents' Construction
Providing a timing signal to said central processing unit	Timing the operation of the CPU such that it will always execute at the maximum frequency possible, but never too fast

"clocking said CPU"

TPL and the Staff Adopt Judges Ware and Grewal's Construction

TPL's and Staff's Construction	Respondents' Construction
Providing a timing signal to said CPU	Timing the operation of the CPU such that it will always execute at the maximum frequency possible, but never too fast

"clocking said CPU"

Respondents Want to Import An Extraneous Limitation:

TPL's and Staff's Construction	Respondents' Construction
Providing a timing signal to said CPU	Timing the operation of the CPU such that it will always execute at the maximum frequency possible, but never too fast

"clocking said CPU"

Respondents Want to Import An Extraneous Limitation:

TPL's and Staff's Construction	Respondents' Construction
Providing a timing signal to said CPU	Timing the operation of the CPU such that it will always execute at the maximum frequency possible, but never too fast

"clocking said CPU"

Respondents' proposed construction improperly imports a limitation from the specification into the claims, and is vague and ambiguous

- Respondents improperly read an extraneous limitation into the claims
- Respondents incorrectly argue that "always execute at the maximum frequency possible but never too fast" describes the sole embodiment in the specification
- There is no clear disavowal that prevents the CPU from operating at a frequency *less* than the maximum frequency possible
- The proposed claim construction is vague and ambiguous
- Three district court judges have already rejected this limitation

"clocking said CPU"

Respondents' proposed construction improperly imports a limitation from the specification into the claims, and is vague and ambiguous

- Respondents improperly read an extraneous limitation into the claims

While claim limitations must be construed in light of the specification and prosecution history, it is improper to import limitations into the claims where such limitations are not present in the language of the claim itself.

Phillips, 415 F.3d at 1323.

"clocking said CPU"

Respondents' proposed construction improperly imports a limitation from the specification into the claims, and is vague and ambiguous

- Respondents incorrectly argue that the specification describes the invention as "always execut[ing] at the maximum frequency possible but never too fast"
  - Respondents focus on one embodiment that includes CPU 70:

> "By deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast."
>
> *JXM-0001 ('336 patent) col. 16:59-17:2, emphasis added*

  - Respondents ignore other embodiments that include, for example, CPU 316:

> "The microprocessor 310 CPU 316 resides on an already crowded DRAM die 312."
>
> *JXM-0001 ('336 patent) col. 12:66-67, emphasis added*

"clocking said CPU"

Respondents flatly misrepresent the use of the phrase "always execute at the maximum frequency possible but never too fast"

- Respondents wrongly assert that the patentee described any embodiment as "the invention itself."
- The patentees did not describe "the invention itself" using the phrase "always execute at the maximum frequency possible but never too fast"

"clocking said CPU"

Respondents flatly misrepresent the use of the phrase "always execute at the maximum frequency possible but never too fast"

"[E]ven where a patent describes only a single embodiment, claims will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction."

Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc., 381 F3d 1111,1117 (Fed. Cir. 2004)

"clocking said CPU"

Respondents' proposed construction improperly imports a limitation from the specification into the claims, and is vague and ambiguous

- The specification does not include a clear disavowal of a CPU operating at a frequency less than the maximum frequency

A description of an embodiment in the specification is not a clear disavowal "unless the patentee has demonstrated a clear intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'"

Liebel–Flarsheim Co. v. Medrad, Inc., 358 F.3d 898, 906 (Fed. Cir. 2004)

"clocking said CPU"

Respondents' proposed construction improperly imports a limitation from the specification into the claims, and is vague and ambiguous

- The proposed claim construction is vague and ambiguous

> "Courts construe claim terms in order to assign a fixed, unambiguous, legally operative meaning to the claim."
>
> *Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1378 (Fed. Cir. 2005)

- The phrases "maximum frequency possible" and "never too fast" are vague, indefinite and ambiguous

“clocking said CPU”

TPL’s and Staff’s Construction

Providing a timing signal to said central processing unit

CPU Clock-Related Terms

- "ring oscillator"
- "entire oscillator/clock"
- "varying" limitations terms
- "thereby enabling said processing frequency to track said clock rate in response to said parameter variation"
- "clocking said CPU"
- "operates asynchronously to" – *claims 11, 13, 16*

"operates asynchronously to"

TPL's Construction	Respondents' and Staff's Construction
The timing control of the central processing unit operates independently of (not derived from) the timing control of the input/output interface such that there is no readily predictable phase relationship between them	The timing control of the central processing unit operates independently of and not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them

"operates asynchronously to"

- "not derived from" is part of "independent of"
  - The claims require a second clock independent of the oscillator/system clock
  - "independent" clocks cannot be derived from the same source
  - Therefore "not derived from" is not a separate requirement from "independent of"
- Respondents' "and" wrongly indicates that there are separate requirements

"operates asynchronously to"

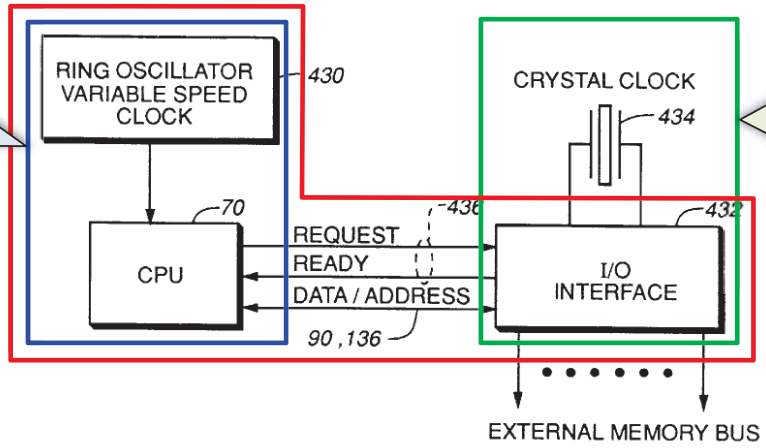
The Patentee Provided the Definition of *"Operates Asynchronously to"* During Prosecution

An *asynchronous* system is one containing two or more independent clock signals. So long as each clock drives independent logic circuitry, such a system is effectively a collection of independent synchronous systems. The logical combination of signals derived from independent clocks, however, poses difficulty because of the unpredictability of their phase relationship. In this section we briefly explore this problem and discuss its consequences.
(emphasis in the original)

JXM-0023 (9/08 Am.) at TPL853_02992755

"operates asynchronously to"

clocking said central processing unit at a clock rate using said variable speed clock



clocking said input/output interface using an off-chip external clock

FIG._17

wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock, wherein said central processing unit operates asychronously [sic] to said input/output interface.

JXM-0001 ('336 patent) claim 16

"operates asynchronously to"

TPL's Claim Construction

The timing control of the central processing unit operates independently of (**not derived from**) the timing control of the input/output interface such that there is no readily predictable phase relationship between them