EXHIBIT A

Exhibit A
Proposed Claim Constructions
Inv. No. 337-TA-853

Term	Complainant	Respondents	Staff
an entire ring oscillator variable speed system clock in said single integrated circuit (Claims 1, 13)	a ring oscillator, variable speed system clock, wherein the ring oscillator is located entirely on the same semiconductor substrate as the central processing unit	a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an external crystal/clock generator to generate a clock signal	a ring oscillator variable speed system clock that includes all components that determine clock frequency located on the same semiconductor substrate as the CPU
an entire oscillator disposed upon said integrated circuit substrate (Claims 6, 13)	an oscillator that is located entirely on the same semiconductor substrate as the central processing unit	an oscillator that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an external crystal/clock generator to generate a clock signal	an oscillator that includes all components that determine oscillator frequency located on the same semiconductor substrate as the CPU
an entire variable speed clock disposed upon said integrated circuit substrate (Claims 10, 16)	a variable speed clock that is located entirely on the same semiconductor substrate as the central processing unit	a variable speed clock that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an external crystal/clock generator to generate a clock signal	a variable speed clock that includes all components that determine clock frequency located on the same semiconductor substrate as the CPU
central processing unit (Claims 1, 6, 10, 11, 13, 16)	**(All parties agree):** electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions		
wherein said central processing unit operates asynchronously to said input/output interface (Claims 11, 13, 16) [RESPONDENTS]	the timing control of the central processing unit operates independently of (not derived from) the timing control of the input/output interface such that there is no readily predictable phase relationship between them	the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them	the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them
varying together; (Claims 1, 11) [RESPONDENTS] varying in the same way; (Claims 10, 16) [RESPONDENTS] varying . . . in the same way; (Claims 6, 13) [RESPONDENTS]	**No construction necessary. But if construed:** changing in a corresponding manner	increasing and decreasing proportionally	increasing and decreasing proportionally

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second clock independent of said ring oscillator . . . system clock (Claims 1, 11) [RESPONDENTS]	**(All parties agree):** a second clock wherein a change in the frequency of either the second clock or ring oscillator system clock does not affect the frequency of the other		
thereby enabling said processing frequency to track said clock rate in response to said parameter variation (Claims 6, 13) [RESPONDENTS]	thereby enabling the processing frequency of the central processing unit to follow said clock rate in response to said parameter variation	said parameter variation directly causing said processing frequency to track said clock rate	said parameter variation directly causing said processing frequency to track said clock rate
on-chip input/output interface (Claims 1, 6, 10, 11, 13, 16) [RESPONDENTS]	**(All parties agree):** a circuit having logic for input/output communications, where that circuit is located on the same semiconductor substrate as the CPU		
external clock is operative at a frequency independent of a clock frequency of said oscillator (Claims 6, 13) [RESPONDENTS]	**(All parties agree):** an external clock wherein a change in the frequency of either the external clock or oscillator does not affect the frequency of the other		
external clock is operative at a frequency independent of a clock frequency of said variable speed clock (Claims 10, 16) [RESPONDENTS]	**(All parties agree):** an external clock wherein a change in the frequency of either the external clock or the variable speed clock does not affect the frequency of the other		
ring oscillator (Claims 1, 9, 11, 15) [RESPONDENTS]	interconnected electronic components comprising multiple odd numbers of inversions arranged in a loop, where three or more inversions are required to maintain an oscillating output	an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is: (1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters in the environment	an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment
clocking said central processing unit (Claims 1, 6, 10, 11, 13, 16) [RESPONDENTS]	providing a timing signal to said central processing unit	timing the operation of the CPU such that it will always execute at the maximum speed possible, but never too fast	providing a timing signal to said central processing unit