

Exhibit C: Defendants' Proposed Constructions and Identification of Evidence
 TPL v. Matsushita et al., Civil Action No. 2:05-CV-494 (TJW)

<u>Claim Terms for U.S. Pat. No. 6,598,148</u>				
Claim	Term	Defendants' Construction	Defendants' Intrinsic Evidence	Defendants' Extrinsic Evidence
4, 7, 8, 10	integrated circuit substrate	<i>a single supporting material upon or within which is formed a miniature circuit</i>	The claims themselves; Abstract; Figs. 1 and 9; Col. 3, ll. 36-39; Col. 6, ll. 49-58; Col. 16, ll. 57-67.	THE ILLUSTRATED COMPUTER DICTIONARY 151, 281 (3d ed. 1986). Defendants reserve the right to submit and rely on an expert declaration in rebuttal to any expert declaration submitted by Plaintiffs.
4, 7, 8, 10	memory	<i>Construe only as part of "a memory" below</i>		
4, 7, 8, 10	a memory	<i>Term is indefinite, but if construction is possible, an information storing array that does not include registers, cache or column latches</i>	The claims themselves; Col. 1, ll. 41-50; Col. 2, ll. 10-16; Col. 4, ll. 1-30; Col. 4, ll. 40-51; Col. 5, ll. 21-28; Col. 5, l. 53 - Col. 6, l. 30; Col. 6, ll. 49-56; Fig. 9; Col. 7, ll. 5-15; Col. 8, l. 48 - Col. 9, l. 16; Col. 9, ll. 16-18; Col. 9, ll. 23-35; Col. 10, l. 54 - Col. 11, l. 11;	Defendants reserve the right to submit and rely on an expert declaration in rebuttal to any expert declaration submitted by Plaintiffs.

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			Col. 12, ll. 41-67; Col. 13, ll. 12-18; Col. 15, l. 55 - Col. 16, l. 36; Col. 18, ll. 41-63; U.S. Pat. No. 5,784,584, claims 1 and 29; 1/31/00 OA, pp. 2-3.	
4, 7	total area of said single substrate	<i>area enclosed by the outermost edges of the substrate</i>	The claims themselves; Col. 3, ll. 36-39; Col. 6, ll. 49-56.	Defendants reserve the right to submit and rely on an expert declaration in rebuttal to any expert declaration submitted by Plaintiffs.
8, 10	total area of said substrate	<i>area enclosed by the outermost edges of the substrate</i>	The claims themselves; Col. 3, ll. 36-39; Col. 6, ll. 49-56.	Defendants reserve the right to submit and rely on an expert declaration in rebuttal to any expert declaration submitted by Plaintiffs.
4, 7	area of said integrated circuit substrate	<i>No construction necessary</i>	The claims themselves; Abstract; Col. 2, ll. 8-16; Col. 3, ll. 36-39; Col. 6, ll. 49-56.	Defendants reserve the right to submit and rely on an expert declaration in rebuttal to any expert declaration submitted by Plaintiffs.
4, 7	area of said single substrate	<i>No construction necessary</i>	The claims themselves; Abstract;	Defendants reserve the right to submit and rely on an expert

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			Col. 2, ll. 8-16; Col. 3, ll. 36-39; Col. 6, ll. 49-56.	declaration in rebuttal to any expert declaration submitted by Plaintiffs.
8, 10	area of said substrate	<i>No construction necessary</i>	The claims themselves; Abstract; Col. 2, ll. 8-16; Col. 3, ll. 36-39; Col. 6, ll. 49-56.	Defendants reserve the right to submit and rely on an expert declaration in rebuttal to any expert declaration submitted by Plaintiffs.
4, 7, 8, 10	a [ring oscillator] having a variable output frequency	<i>a [ring oscillator] having an output speed (frequency) that is not tightly controlled and varies more than minimally</i>	The claims themselves; Figs. 17 and 18; Col. 14, l. 26 - Col. 15, l. 20; Orig. Appl., pp. 24-56 to 25-56; 1/31/00 OA, pp. 2-3; 4/29/02 Amdmt., pp. 1-11. From the '336 patent: The claims themselves; Abstract; Col. 3, ll. 26-35; Col. 16, ll. 43 - Col. 17, l. 50; Figs. 1, 5, 17-19; 6/7/95 Orig. Appl., pp. 31-33, 64-83; 12/12/95 OA, pp. 2-3; 4/11/96 Amdmt., pp. 1-10;	Mathys, Robert J., Crystal Oscillator Circuits (1983) [MEI-ED00010233-MEI-ED00010279]; Cordell, Robert R. & Garrett, William G., <i>A Highly Stable VCO for Application in Monolithic Phase-Locked Loops</i> , IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. SC-10, No. 6, Dec. 1975 [TPL-SC-10, No. 6, Dec. 1975 [TPL-ED0398601 to 606]; Murthi, Enjeti N., <i>A Monolithic Phase-Locked Loop with Post Detection Processor</i> , IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. SC-14, No. 1, Feb. 1979 [TPL-

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			7/8/96 OA, pp. 2-4; 1/8/97 Amdmt., pp. 1-5; 4/3/97 OA, p. 2; 7/3/97 Amdmt, p. 1-5; 10/16/97 OA, p.2-4; 2/6/98 Amdmt, p. 1-5; 4/24/98 Supp. Amdmt., pp. 1-3; 5/13/98 Interview Summ. Rec.; U.S. Pat. No. 4,503,500 (Magar); U.S. Pat. No. 4,627,082 (Pelgrom); U.S. Pat. No. 4,338,675 (Palmer); U.S. Pat. No. 4,680,698 (Edwards et al.); U.S. Pat. No. 4,453,229 (Schaire); U.S. Pat. No. 4,670,837 (Sheets); U.S. Pat. No. 5,440,749, file history 12/31/92 OA, pp. 1-10; 7/28/93 Amdmt., pp. 11-17.
			ED0400976 to 981]; Santos, Joseph T., <i>A One-Pin Crystal Oscillator for VLSI Circuits</i>, IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. SC-19, No. 2, April 1984 [TPL-ED0405711 to 719]; Uzunoglu, Vasil & White, Marvin H., <i>The Synchronous Oscillator: A Synchronization and Tracking Network</i>, IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. SC-20, No. 6, Dec. 1985 [TPL-ED0407561 to 573]; Sleeckx, Frans V.J. & Sansen, Willy M.C., <i>A Wide-Band Current-Controlled Oscillator Using Bipolar-JFET Technology</i>, IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. SC-15, No. 5, Oct. 1980 [TPL-ED0402669 to 675]; Fleischer, Paul E., et al., <i>A Switched Capacitor Oscillator with Precision Amplitude Control and Guaranteed Start-Up</i>, IEEE JOURNAL OF SOLID-

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Claim	Term	Defendants' Construction	Defendants' Intrinsic Evidence	Defendants' Extrinsic Evidence
				STATE CIRCUITS, Vol. SC-20, No. 2, April 1985 [TPL-ED0407015 to 021]; Cordell, Robert R., et al., <i>A 50MHz Phase- and Frequency-Locked Loop</i>, IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. SC-14, No. 6, Dec. 1979 [TPL-ED0401776 to 783]; MEAD & CONWAY, INTRODUCTION TO VLSI SYSTEMS 233-36 (1980) [MEI-ED00012333 to MEI-ED00012336]; MOHAMMED S. GHAUSI, ELECTRONIC DEVICES AND CIRCUITS: DISCRETE AND INTEGRATED 508 (1985); THE AMERICAN HERITAGE DICTIONARY 457, 1337 (1985); MCGRAW-HILL DICTIONARY OF SCIENTIFIC AND TECHNICAL TERMS 1339-40, 2016 (4th ed. 1989). Defendants reserve the right to submit and rely on an expert declaration in rebuttal to any

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<u>Claim Terms for U.S. Pat. No. 6,598,148</u>				
Claim	Term	Defendants' Construction	Defendants' Intrinsic Evidence	Defendants' Extrinsic Evidence
4, 7, 8, 10	ring oscillator	Same as "ring oscillator", in '336 patent.	The claims themselves; Figs. 17 and 18; Col. 14, l. 26 - Col. 15, l. 20. From the '336 patent: The claims themselves. Figs. 17-19; Col. 3, ll. 27-35; Col. 16, l. 43 - Col. 17, l. 37.	expert declaration submitted by Plaintiffs. Same extrinsic evidence as cited for "a [ring oscillator] having a variable output frequency" term.
4, 7 8, 10	the [ring oscillator] disposed on said integrated circuit substrate (claims 4, 7); the [ring oscillator] disposed on said substrate (claims 8 & 10)	a [ring oscillator] that is on-chip and does not rely on a control signal or an external crystal/clock generator	The claims themselves; Figs. 17 and 18; Col. 14, l. 26 - Col. 15, l. 20; Orig. Appl., pp. 24-56 to 25-56; 1/31/00 OA, pp. 2-3; 4/29/02 Amdmt., pp. 1-11. From the '336 patent: The claims themselves; Abstract; Col. 3, ll. 26-35; Col. 16, ll. 43 - Col. 17, l. 50; Figs. 1, 5, 17-19; 6/7/95 Orig. Appl., pp. 31-	Same extrinsic evidence as cited for "a [ring oscillator] having a variable output frequency" term.

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<u>Claim Terms for U.S. Pat. No. 6,598,148</u>				
Claim	Term	Defendants' Construction	Defendants' Intrinsic Evidence	Defendants' Extrinsic Evidence
			33, 64-83; 12/12/95 OA, pp. 2-3; 4/11/96 Amdmt., pp. 1-10; 7/8/96 OA, pp. 2-4; 1/8/97 Amdmt., pp. 1-5; 4/3/97 OA, p. 2; 7/3/97 Amdmt, p. 1-5; 10/16/97 OA, p.2-4; 2/6/98 Amdmt, p. 1-5; 4/24/98 Supp. Amdmt., pp. 1-3; 5/13/98 Interview Summ. Rec.; U.S. Pat. No. 4,503,500 (Magar); U.S. Pat. No. 4,627,082 (Pelgrom); U.S. Pat. No. 4,338,675 (Palmer); U.S. Pat. No. 4,680,698 (Edwards et al.); U.S. Pat. No. 4,453,229 (Schaire); U.S. Pat. No. 4,670,837 (Sheets); U.S. Pat. No. 5,440,749, file history 12/31/92 OA, pp. 1-10; 7/28/93 Amdmt., pp. 11-	

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Claim	Term	Defendants' Construction	Defendants' Intrinsic Evidence	Defendants' Extrinsic Evidence
4, 7, 8, 10	variable	<i>not tightly controlled and varying more than minimally</i>	17. The claims themselves; Figs. 17 and 18; Col. 14, l. 26 - Col. 15, l. 20; Orig. Appl., pp. 24-56 to 25-56; 1/31/00 OA, pp. 2-3; 4/29/02 Amdmt., pp. 1-11. From the '336 patent: The claims themselves; Abstract; Col. 3, ll. 26-35; Col. 16, ll. 43 - Col. 17, l. 50; Figs. 1, 5, 17-19; 6/7/95 Orig. Appl., pp. 31-33, 64-83; 12/12/95 OA, pp. 2-3; 4/11/96 Amdmt., pp. 1-10; 7/8/96 OA, pp. 2-4; 1/8/97 Amdmt., pp. 1-5; 4/3/97 OA, p. 2; 7/3/97 Amdmt, p. 1-5; 10/16/97 OA, p.2-4; 2/6/98 Amdmt, p. 1-5; 4/24/98 Supp. Amdmt., pp. 1-3;	Same extrinsic evidence as cited for "a [ring oscillator] having a variable output frequency" term.

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<u>Claim Terms for U.S. Pat. No. 6,598,148</u>				
Claim	Term	Defendants' Construction	Defendants' Intrinsic Evidence	Defendants' Extrinsic Evidence
			5/13/98 Interview Summ. Rec.; U.S. Pat. No. 4,503,500 (Magar); U.S. Pat. No. 4,627,082 (Pelgrom); U.S. Pat. No. 4,338,675 (Palmer); U.S. Pat. No. 4,680,698 (Edwards et al.); U.S. Pat. No. 4,453,229 (Schaire); U.S. Pat. No. 4,670,837 (Sheets); U.S. Pat. No. 5,440,749, file history 12/31/92 OA, pp. 1-10; 7/28/93 Amdmt., pp. 11-17.	
4, 7, 8, 10	system clock	Same as "system clock" in the '336 patent	The claims themselves.	McGraw-Hill Dictionary of Scientific and Technical Terms 366 (4th ed. 1989). Defendants reserve the right to submit and rely on an expert declaration in rebuttal to any expert declaration submitted by Plaintiffs.

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<u>Claim Terms for U.S. Pat. No. 6,598,148</u>				
Claim	Term	Defendants' Construction	Defendants' Intrinsic Evidence	Defendants' Extrinsic Evidence
8, 10	interface ports for interprocessor communication	<i>channels through which data is transferred between two separate processing units</i>	The claims themselves.	MCGRAW-HILL DICTIONARY OF SCIENTIFIC AND TECHNICAL TERMS 977 (4th ed. 1989). Defendants reserve the right to submit and rely on an expert declaration in rebuttal to any expert declaration submitted by Plaintiffs.

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<u>Claim Terms for U.S. Pat. No. 5,784,584¹</u>				
Claims	Term	Defendants' Construction	Defendants' Intrinsic Evidence	Defendants' Extrinsic Evidence
29	microprocessor system	<i>No construction of the phrase is necessary, The preambles containing this phrase are not claim limitations</i>	Preamble of claim 29.	Defendants reserve the right to submit and rely on an expert declaration in rebuttal to any expert declaration submitted by Plaintiffs.
29	central processing unit	<i>Same as "central processing unit", in '336 patent</i>		MCGRAW-HILL DICTIONARY OF SCIENTIFIC AND TECHNICAL TERMS 318 (4th ed. 1989). Defendants reserve the right to submit and rely on an expert declaration in rebuttal to any expert declaration submitted by Plaintiffs.
29	instruction group	<i>sets of from 1 to a maximum number of sequential instructions, in which the execution of the</i>	Abstract; Figs. 4, 16, 20; Col. 1, ll. 28-38;	Defendants reserve the right to submit and rely on an expert declaration in rebuttal to any

¹ Plaintiffs have represented that they are accusing only ARM core chips of infringing the '584 Patent. Accordingly, Defendants have deferred to the constructions proposed by ARM with respect to the '584 Patent. Defendants reserve the right to raise additional claim construction issues and to make additional proposals regarding claim construction in the event that plaintiffs seek to add additional chips beyond the ARM core chips currently accused.

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<u>Claim Terms for U.S. Pat. No. 5,784,584¹</u>				
Claims	Term	Defendants' Construction	Defendants' Intrinsic Evidence	Defendants' Extrinsic Evidence
		<i>instructions depends on each set being provided to the instruction register as a unit and in which any operand that is present must be right justified and which cannot encompass a single 32-bit RISC instruction</i>	Col 2, ll. 11-17; Col 2, ll. 29-34; Col. 2, ll. 42-55; Col. 5, ll. 25-26; Col. 10, ll. 56-67; Col. 11, ll. 12-21; Col. 14, ll. 4-39; Col. 14, ll. 41-64; Col. 16, ll. 6-26; Col. 18, ll. 21-27; Col. 18, ll. 42-57; Col. 19, ll. 17-36; Col. 20, l. 36 - Col. 21, l. 28; Col. 21, ll. 43-45; Col. 22, ll. 42-47; Col. 22, ll. 58-67; Col. 23-24; Col. 28, ll. 62-67; Col. 29, ll. 1-24; 4/8/96 Amdmt. pp. 11-13; 12/12/96 OA, pp. 3-4; 6/12/97 Amdmt. pp. 7-13; 8/22/97 OA, pp. 3-4; 11/21/97 Amdmt. pp. 6-10; 2/5/98 Amdmt. pp. 5-9; U.S. Pat. No. 5,440,749, file	expert declaration submitted by Plaintiffs.

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<u>Claim Terms for U.S. Pat. No. 5,784,584¹</u>				
Claims	Term	Defendants' Construction	Defendants' Intrinsic Evidence	Defendants' Extrinsic Evidence
29	instruction register	<i>a hardware element that receives and holds an instruction group as it is extracted from memory; the register either contains or is connected to circuits that interpret the instructions in the group</i>	history 10/25/94 Interview; 11/9/94 Info. Discl. Stmt. Abstract; Figs. 4, 16, 20; Col. 2, ll. 14-15; Col. 2, ll. 26-32; Col. 5, ll. 63-67; Col. 9, ll. 51-53; Col. 10, ll. 56-67; Col. 14, ll. 4-9; Col. 14, ll. 19-27; Col. 14, ll. 41-48; Col. 16, ll. 9-18; Col. 19, ll. 22-32; Col. 19, ll. 55-58; 4/8/96 Amdmt. pp. 11-13; 12/12/96 OA, pp. 3-4; 6/12/97 Amdmt. pp. 7-10, 12-13; 8/22/97 OA, pp. 3-4; 11/21/97 Amdmt. pp. 6, 8-10; 2/5/98 Amdmt. pp. 5-9.	Defendants reserve the right to submit and rely on an expert declaration in rebuttal to any expert declaration submitted by Plaintiffs.
29	operand	<i>an input to a single operation specified by an instruction that is encoded as part of the instruction</i>	Col. 11, ll. 12-21; Col. 16, ll. 6-26; Col. 20, ll. 41- Col. 21, ll.	Defendants reserve the right to submit and rely on an expert declaration in rebuttal to any

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<u>Claim Terms for U.S. Pat. No. 5,784,584¹</u>				
Claims	Term	Defendants' Construction	Defendants' Intrinsic Evidence	Defendants' Extrinsic Evidence
		<i>where the size of the input can vary depending on the value of the input</i>	28; Col. 28, ll. 63-67; Col. 29, ll. 1-25; 4/8/96 Amdmt. pp. 11-13; 12/12/96 OA, pp. 3-4; 6/12/97 Amdmt. pp. 7-13; 8/22/97 OA, pp. 3-4; 11/21/97 Amdmt. pp. 1-11; 2/5/98 Amdmt. pp. 5-9; U.S. Pat. No. 5,440,749, file history 10/25/94 Interview; 11/9/94 Info. Discl. Stmt.	expert declaration submitted by Plaintiffs.
29	said instruction groups include at least one instruction that, when executed, causes an access to an operand or an instruction or both	<i>the instruction being executed causes the CPU to use data or execute a second instruction</i>	Abstract; Col. 2, ll. 5-55; Col. 14, ll. 20-27, 32-35; Col. 16, ll. 14-16; Col. 19, ll. 17-36; Col. 20, ll. 36-37; Col. 21, ll. 43-45; Col. 22, l. 66; Col. 23-24; 4/8/96 Amdmt. pp. 11-13; 12/12/96 OA, pp. 3-4; 6/12/97 Amdmt. pp. 7-13; 8/22/97 OA, pp. 3-4; 11/21/97 Amdmt. pp. 1-11;	Defendants reserve the right to submit and rely on an expert declaration in rebuttal to any expert declaration submitted by Plaintiffs.

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Claims	Term	Defendants' Construction	Defendants' Intrinsic Evidence	Defendants' Extrinsic Evidence
			2/5/98 Amdmt. pp. 5-9; U.S. Pat. No. 5,440,749, file history 10/25/94 Interview; 11/9/94 Info. Discl. Stmt.	
29	said operand or instruction being located at a predetermined position from a boundary of said instruction groups	<i>the bits forming the accessed operand or instruction either begin or end at a position defined in relation to the boundaries of the instruction group in the instruction register rather than the currently executing instruction</i>	Abstract; Col. 2, ll. 9-16; Col. 2 ll. 28-34; Col. 14, ll. 20-27, 32-35; Col. 16, ll. 6-26; Col. 19, ll. 17-32; Col. 20, ll. 36-37; Col. 21, ll. 16-21, 43-45; Col. 22, l. 66; Col. 23-24; Col. 28, ll. 62-67; Col. 29, ll. 1-24; 4/8/96 Amdmt. pp. 11-13; 12/12/96 OA, pp. 3-4; 6/12/97 Amdmt. pp. 7-13, 8/22/97 OA, pp. 3-4; 11/21/97 Amdmt. pp. 1-11; 2/5/98 Amdmt. pp. 5-9; U.S. Pat. No. 5,440,749, file history 10/25/94 Interview; 11/9/94 Info. Discl. Stmt.	Defendants reserve the right to submit and rely on an expert declaration in rebuttal to any expert declaration submitted by Plaintiffs.

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29	decoding said at least one instruction to determine said predetermined position	<i>interpreting an instruction, in particular the portion thereof that signifies the operation to be performed, in order to identify a position relative to the beginning or end of the current instruction group</i>	Fig. 4; Col. 2, ll. 20-24; Col. 2, ll. 37-41; Col. 6, ll. 2-5; Col. 6, ll. 5-8; Col. 16, ll. 18-26; Col. 19, ll. 22-36; Col. 21, ll. 16-21; Col. 21, ll. 60-62; Col. 29, ll. 8-14; 4/8/96 Amdmt. pp. 11-13; 12/12/96 OA, pp. 3-4; 6/12/97 Amdmt. pp. 7-10, 12-13; 8/22/97 OA, pp. 3-4; 11/21/97 Amdmt. pp. 6, 8-10; 2/5/98 Amdmt. pp. 5-9.	Defendants reserve the right to submit and rely on an expert declaration in rebuttal to any expert declaration submitted by Plaintiffs.
29	locating said predetermined position	<i>Using the results of the decoding step to ascertain the address of the accessed operand or instruction by referencing the current instruction group address rather than the current executing instruction address without adding or subtracting an operand with the</i>	Abstract; Col. 14, ll. 41-58; Col. 20, ll. 41- Col. 21, ll. 28; 4/8/96 Amdmt. pp. 11-13; 12/12/96 OA, pp. 3-4; 6/12/97 Amdmt. pp. 7-10, 12-13;	Defendants reserve the right to submit and rely on an expert declaration in rebuttal to any expert declaration submitted by Plaintiffs.

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Claims	Term	Defendants' Construction	Defendants' Intrinsic Evidence	Defendants' Extrinsic Evidence
		<i>current Program Counter</i>	8/22/97 OA, pp. 3-4; 11/21/97 Amdmt. pp. 6, 8-10; 2/5/98 Amdmt. pp. 5-9.	