IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

TECHNOLOGY PROPERTIES LIMITED, INC.,	§	
Plaintiff,	§	Civil Action No. 2:05-CV-494 (TJW)
vs.	§	**JURY DEMANDED**
FUJITSU LIMITED, ET AL.,	§	
Defendants.	§	

OPPOSITION OF MEI, PNA, AND JVC[1] TO TPL'S MOTION TO AMEND ITS PRELIMINARY INFRINGEMENT CONTENTIONS

I. INTRODUCTION

TPL's motion for leave to submit corrected preliminary infringement contentions does not seek merely to correct inconsistencies and errors, leaving the number of products at issue in this lawsuit the same. Quite the contrary. TPL's motion seeks amendment of TPL's preliminary infringement contentions so that "chip families"—which include hundreds of chips for which TPL still has not provided claim charts as required by the Patent Local Rules—will now be a part of this lawsuit. Under TPL's proposal, defendants would be forced to provide discovery on hundreds of chips that TPL has no basis to assert infringe its patents. The prejudice to defendants is not simply delay. It is the massive burden of having to defend hundreds of chips against TPL's overbroad and baseless infringement allegations—precisely what the Patent Local Rules are intended to prevent.

The claim charts that TPL provided to date are directed toward specific individual chips, not chip families. They do not even pretend to provide a basis for accusing entire families of

[1] This opposition is submitted on behalf of defendants Matsushita Electric Industrial Co., Ltd., Panasonic Corporation of North America, and JVC Americas Corp.

chips of infringing TPL's patents. Indeed, in its original set of corrected preliminary infringement contentions (PICs),[2] TPL as much as admitted that it had no basis to accuse entire chip families of infringement. In its original set of corrected PICs, TPL attempted to expand its infringement contentions to include chip families only "if discovery establishes that the products identified by 'Chip Part Number' are representative of the products identified by 'Chip Family.'"

TPL now simply pretends that it never acknowledged that it does not have a basis to assert that the chips it charted are representative of the chip families. In its current corrected PICs, TPL deleted its statements about the need for discovery, and instead baldly asserts that the specific individual chips are representative of the chip families. TPL goes so far as to argue that "each of the representative chips is, for purposes of the infringement analysis, *identical* to the other members of its chip family." But TPL does not explain what changed in the two week period between serving its original set of corrected PICs and filing its motion with its new set of corrected PICs.

The truth is that TPL has no basis to assert that every chip in the chip families is identical for purposes of its infringement contentions. Indeed, TPL's own infringement contentions show that there are important differences between chips in the same chip families. Defendants should not be put to the incredibly burdensome task of providing discovery on every chip in the chip families identified by TPL on the basis of TPL's unsupportable assertion that the chips are identical for purposes of determining infringement.

II. FACTUAL BACKGROUND

Defendants received TPL's preliminary infringement contentions on July 17, 2006. [Exh. 1, Baker-Lehne July 17, 2006 email.] After reviewing them, defendants wrote to TPL because

[2] As TPL pointed out in its brief, TPL provided defendants with a set of corrected PIC's before filing its motion. What TPL failed to mention, however, is that those corrected PIC's are different from the corrected PIC's that TPL submitted to the Court with its motion.

the particular chips identified in TPL's original PICs did not match the claim charts that TPL provided. [Exh. 2, Lender, Antonelli, Cook email exchange] On July 25, 2006, TPL responded that "the claim charts are correct; the PIC text should match the PIC charts, but does not" and promised to send a correction. [Exh. 2, Lender, Antonelli, Cook email exchange]

On July 27, 2006, defendants received a set of corrected PICs. [Exh. 3, Cook letter and Original Corrected PICs.] These PICs did not simply correct the errors identified by defendants, but also purported to add "chip families" to the extent discovery showed they were the same as the representative products:

> [E]ach of the MEI products identified by "Chip Family" in that table infringes the same claims **if discovery establishes that products identified by "Chip Part Number" are representative** of the products identified by "Chip Family."

Id. at 2.

The next day, defendants participated in a telephone conference with TPL. Defendants explained that their objection to TPL's proposed corrected PICs was not primarily the delay involved, but rather the fact that TPL was attempting to expand its infringement allegations to include "chip families" of hundreds of chips for which it had not provided claim charts and for which it admittedly did not have a basis to allege infringed its patents.

Two weeks later, in the Corrected PICs submitted with its motion, TPL deleted the statement from its original set of corrected PICs acknowledging that it does not have a basis to claim that the charted chips are representative of the chip families. In its place, TPL asserted in its second set of Corrected PICs, with no support, that the charted chips are representative:

> Each of the MEI products identified by the 'Chip Part Number' . . . **is representative** for purposes of its associated Chip Family. Each of the MEI products identified by 'Chip Family' in that table infringes the same claims as the associated representative chip . . . .

[Exh. 4, Second Set of Corrected PICs.] TPL's second set of corrected PICs, like its first set of corrected PICs, did not provide any new claim charts.

III. TPL IS REQUIRED TO PROVIDE CLAIM CHARTS DISCLOSING ITS SPECIFIC INFRINGEMENT THEORY FOR EACH ACCUSED PRODUCT

Under the Patent Local Rules, TPL is required to provide claim charts specifically setting forth its infringement theories for each accused product:

> [A] party claiming patent infringement must serve on all parties a "Disclosure of Asserted Claims and Preliminary Infringement Contentions." Separately for each opposing party, the "Disclosure of Asserted Claims and Preliminary Infringement Contentions" shall contain the following information:
> . . . .
> (b) **Separately for** each asserted claim, **each** accused apparatus, product, device, process, method, act, or other instrumentality ("Accused Instrumentality") of each opposing party of which the party is aware. **This identification must be as specific as possible**.
> . . . .
> (c) A chart identifying specifically where each element of each asserted claim is found within **each** Accused Instrumentality . . . .

P.R. 3-1 (emphasis added).

The Patent Local Rules contemplate that patent owners will conduct their infringement investigations before filing suit, and be in a position to provide claim charts that show their specific infringement theories before discovery begins:

> [T]he Patent Rules are designed to streamline the discovery process. They provide structure to discovery and enable the parties to move efficiently toward claim construction and the eventual resolution of their dispute. **The Patent Rules demonstrate high expectations as to plaintiffs' preparedness before bringing suit, requiring plaintiffs to disclose their preliminary infringement contentions before discovery has begun.**

Am. Video Graphics v. Elec. Arts, 359 F. Supp.2d 558, 560 (E.D. Tex. 2005) (internal cites omitted) (emphasis added); cf. InterTrust Tech's Corp. v. Microsoft Corp., No. C 01-1640, 2003

WL 23120174, *2 (N.D. Cal., Dec. 1, 2003) ("The overriding principle of the [similar N.D. Cal.] Patent Local Rules is that they are designed to make the parties more efficient, to streamline the discovery process, **and to articulate with specificity the claims and theory of a plaintiff's infringement claims**.") (emphasis added).

Of course it would be acceptable to provide a single chart for a series of products when there is a fair basis to believe that the separate products are the same for purposes of infringement. Cf., e.g., Renesas Tech. Corp. v. Nanya Tech. Corp., No. C03-05709JFHRL, 2004 WL 2600466 (N.D. Cal., Nov. 10, 2004). Indeed, defendants are not objecting to TPL providing a single claim chart for the MN102xx19 series of chips. But that does not mean that TPL can comply with the Patent Local Rules for entire chip families by submitting claim charts for specific chips, and then asserting, with no support, that the claimed chips are identical for purposes of infringement. Cf. In the Matter of Certain Point of Sale Terminals and Components Thereof, 2005 WL 1542620, No 337-TA-524, *8-*9 (U.S.I.T.C. June 7, 2005) (sanctioning patent owner for accusing family of products based on analysis of single product when there was no basis to conclude that the products were the same for purposes of infringement).

IV. THE CHIPS WITHIN EACH FAMILY ARE NOT IDENTICAL

TPL does not dispute that it has not provided claim charts setting forth its infringement contentions for each of the chips in the "chip families" that it now seeks to add to this case. Instead, TPL now argues that its claim charts for specific "representative" chips are sufficient because "each of the representative chips is, for purposes of the infringement analysis, *identical* to the other members of its chip family." [TPL's Motion to Amend, p. 3.] Not so.

Not only is TPL's argument inconsistent with TPL's first set of corrected PICs, in which TPL purported to add chip families only to the extent that discovery showed that chips were the

same as the representative chips, it is also inconsistent with the specific claim charts that TPL did provide. For example, TPL provided claim charts for three specific chips in the "MN101 (AM1)" family: MN101CF91D, MN101C78A, and MN101EF01MAF. Despite its current claim that the hundreds of chips in the MN101 family are identical for purposes of infringement, TPL's infringement allegations are different for each of the three MN101 chips that it charted. TPL provided claim charts alleging that the MN101CF91D chip infringes the '584 and '336 patents, but did not provide a chart asserting that it infringes the '148 patent. TPL provided charts alleging that the MN101C78A chip infringes the '584 patent, but did not provide charts asserting that it infringes the '336 patent or the '148 patent. And TPL provided a chart alleging that the MN101EF01MAF chip infringes the '148 patent, but did not provide charts asserting that it infringes the '336 patent or the '584 patent. Similarly, for the "ARM" family of chips, TPL provided separate claim charts asserting that the MN1A7T0200 chip infringes the '336 and '584 patents, but only provided a single claim chart for the MN1A92070R chip, asserting only that it infringes the '584 patent. These differences in TPL's allegations are simply not reconcilable with its current claim that all of the chips in each family are identical for purposes of infringement.

In one instance, TPL did accuse a series of chips with a single claim chart. TPL provided claim charts that set forth its theory that the "MN102xx19" series of chips infringe the '336 and '584 patents. The "xx" in the chip model number "MN102xx19" means that the name refers to a series of chips: the MN1020019, MN1020219, MN1020419, and MN1020819 chips. In this case, TPL did provide an infringement chart to show its theory that a limited series of chips, the MN102xx19 family, infringes its patents. When TPL meant to accuse a given series of chips of infringement, it certainly knew how. But TPL still has not even attempted to provide claim

charts that would show how all of the chips in each chip family are identical for purposes of determining infringement.

The truth is that there are significant differences between chips that make it inappropriate to proceed against entire the chip families identified by TPL on the basis of "representative" chips. For example, the claims of TPL's '148 patent require at least 50% of the chip substrate to be occupied by memory. But different chips within the MN101 "family" of chips have different amounts of memory. Attached as Exhibit 5 is a specification for the Microcomputer Family AM Series. As can be seen in the third, fourth, and fifth columns, the specific chip charted by TPL (the MN101EF01MAF chip) contains a total of 408 Kilobytes of memory, which TPL argues takes up more than 50% of the substrate. Other chips within the MN101 family, however, do not include the same amounts of memory. Indeed, the vast majority of the hundreds of additional chips have less memory than the MN101EF01MAF chip. These include the specific MN101 chips for which TPL did provided specific claim charts for its other patents, but not its '148 patent (i.e., the MN101C78A and MN101CF91D chips). Those two chips have a total of 33.5 Kilobytes and 68 Kilobytes of memory respectively, i.e., less than 10% and 20% of the memory of the "representative" MN101EF01MAF chip. Chips with less memory obviously cannot be fairly represented by a chip with more memory for purposes of a patent that requires a minimum amount of memory to infringe.

Important differences exist for TPL's '336 patent also. The claims of TPL's '336 patent require an on-chip I/O interface that is connected to a second independent clock. TPL provided only one claim chart asserting that a MN101 chip infringes the '336 patent. In that chart, the only structure that TPL identified as meeting the "second independent clock" limitation is an I2C bus connected to the chip through the SCL2 pin. [Exh. 9, MN101CF91D report for the 336

Patent p. 6]. This bus is not present in all MN101 chip series. For example, the MN101C115 chip does not include an I2C bus port. [Exh. 10, MN101C115 LSI User's Manual, p. 12].

Similar differences that are directly relevant to determining infringement under the 336 patent also exist with respect to the MN103 chips. TPL provided claim charts for two MN103 chips, the MN103E010H chip and the MN103SC2A chip. For the MN103E010H chip, TPL identified the Serial Interfaces, Analog Front End Interface, and I2C Controller as meeting this requirement. [Exh. 6, MN103E010H report p. 7]. For the MN103SC2A chip, however, TPL identified only the Serial Interfaces as meeting this requirement. [Exh. 6, MN103E010H report p. 7]. TPL's claim charts for just two of the many chips in the MN103 family thus alone show important differences in the chips for the purposes of the infringement analysis. Additionally, TPL alleges that these interfaces can be connected to a second independent clock because they can receive clocking signals from another device off of the chip. [Exh. 6, MN103E010H report p. 7]. Whether the accused chips are actually connected to other devices that provide clocking signals to the interfaces that TPL points to is completely ignored by TPL in its infringement contentions. The answer will of course depend on how the individual chips are actually used, which will vary among the many chips in the family. See, e.g., [Exh. 5, Microcomputer AM Series Specification, page 26-28] (listing various applications for different MN103 chips).

Important differences also exist for TPL's third asserted patent, the '584 patent. The '584 patent requires instruction groups to be fetched into an instruction register from memory. The accused MEI chips do not use instruction groups. But TPL believes that the "instruction groups" limitation is somehow met because the MN103 series chips have variable length instruction formats. As can be seen in TPL's own infringement contentions, however, the instruction

formats for the two chips for which TPL provided claim charts are different. See [Exh. 7, MN103E010H report p. 7], and [Exh. 8, MN103SC2A report p. 6].

It only takes a single example of a relevant difference to establish that TPL should not be allowed to proceed against all chips in a chip family based on its bald assertion that the chips are identical for purposes of infringement. The Court should deny TPL's motion because its premise—the supposed identity of the chips within families for purposes of infringement—is, as demonstrated above, false. Defendants should not be forced to take up the burden of defending hundreds of chips based on TPL's unsupported—and unsupportable—assertion that all chips in a chip family are identical for determining infringement.

V. ALTERNATIVELY, THE COURT SHOULD LIMIT DISCOVERY TO THE REPRESENTATIVE CHIPS

If the Court decides to allow TPL to proceed against all chips in the chip families based on TPL's representation that all of the chips in a family are identical for purposes of determining infringement, then the Court should limit TPL to discovery of only those chips that it contends are representative. After all, that is the theory under which TPL is proceeding. Of course defendants should be free to prove that certain chips do not infringe for reasons independent of the reasons why the representative chips do not infringe. Moreover, if defendants are able to prove that any particular chip in family does not infringe, that showing should apply to all chips within the chip families. In other words, if TPL is allowed to proceed against all chips in the chip families, TPL should be held to its position that all of the chips are identical for purposes of determining infringement.

VI. CONCLUSION

For the foregoing reasons, TPL's motion to submit corrected preliminary infringement contentions should be denied. Alternatively, if the Court decides to grant TPL's motion,

defendants request that the Court order discovery by TPL limited to the representative chips and TPL held to its position that all chips within a given chip family are identical for purposes of determining infringement.

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing document was filed electronically in compliance with Local Rule CV-5(a) on this 29th day of August, 2006. As of this date, all counsel of record has consented to electronic service and are being served with a copy of this document through the Court's CM/ECF system under Local Rule CV-5(a)(3)(A).

/s/ Debbie Skolaski