(Counsel listed on signature page)

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN JOSE DIVISION

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. BARNES & NOBLE, INC., Defendants.	Case No. 3:12-cv-03863-VC (PSG) **PATENT LOCAL RULE 4-3 JOINT CLAIM CONSTRUCTION AND PREHEARING STATEMENT**
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. HUAWEI TECHNOLOGIES CO., LTD., HUAWEI DEVICE CO., LTD., HUAWEI DEVICE USA INC., FUTUREWEI TECHNOLOGIES, INC., HUAWEI TECHNOLOGIES USA INC., Defendants.	Case No. 3:12-cv-03865-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. GARMIN LTD., GARMIN INTERNATIONAL, INC., and GARMIN USA, INC., Defendants.	Case No. 3:12-cv-03870-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. ZTE CORPORATION and ZTE (USA) INC., Defendants.	Case No. 3:12-cv-03876-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. SAMSUNG ELECTRONICS CO., LTD. and SAMSUNG ELECTRONICS AMERICA, INC., Defendants.	Case No. 3:12-cv-03877-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. LG ELECTRONICS, INC. and LG ELECTRONICS U.S.A., INC., Defendants.	Case No. 3:12-cv-03880-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. NINTENDO CO., LTD. and NINTENDO OF AMERICA, INC., Defendants.	Case No. 3:12-cv-03881-VC (PSG)

Pursuant to the Court's Order Granting Defendants' Unopposed Motion to Modify Case Schedule, and to maximize the efficiency to the Court, the parties from all eight above-captioned related actions, Plaintiffs Phoenix Digital Solutions LLC, Patriot Scientific Corporation, and Technology Properties Limited LLC (collectively, "Plaintiffs"), and Defendants Barnes & Noble, Inc., Huawei Technologies Co., Ltd., Huawei Device Co., Ltd., Huawei Device USA Inc., Futurewei Technologies, Inc., Huawei Technologies USA Inc., Garmin International, Inc., Garmin USA, Inc., ZTE Corporation, ZTE (USA) Inc., Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., LG Electronics, Inc., LG Electronics U.S.A., Inc., Nintendo Co., Ltd., and Nintendo of America, Inc. (collectively, "Defendants") hereby submit the following Joint Claim Construction and Prehearing Statement pursuant to Patent Local Rule 4-3.

I. AGREED CLAIM CONSTRUCTION TERMS (Patent Local Rule 4-3(a))

Exhibit A sets forth a list of claim terms and their respective constructions that have been agreed upon by all the parties in the related actions.

II. DISPUTED CLAIM CONSTRUCTION TERMS (Patent Local Rule 4-3(b))

Exhibit B is a chart that sets forth disputed claim terms from U.S. Patent Nos. 5,440,749, 5,530,890, and 5,809,336, and the respective constructions proposed by each party. All three patents are at issue in the above-captioned related actions.

The proposed identification of evidence for each disputed claim term provided by plaintiffs Phoenix Digital Solutions LLC, Patriot Scientific Corporation and Technology Properties Limited LLC is attached hereto as Exhibit C.

The proposed identification of evidence for each disputed claim term provided by Defendants is attached hereto as Exhibit D.

III. IDENTIFICATION OF MOST SIGNIFICANT CLAIM TERMS (Patent Local Rule 4-3(c))

The Court has ordered the parties in all eight actions to identify the ten claim terms most significant to the resolution of the issues in the case. The parties have accordingly identified the following claim terms as being most significant to the resolution of the issues in that case at this time, including identification of which terms are believed to be case or claim dispositive:

1. instruction register ('749/'890 Patents)

2. means . . . for fetching instructions for said central processing unit integrated circuit on said bus from said memory, said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle ('749 Patent)

3. push down stack connected to said arithmetic logic unit ('749 Patent) / push down stack . . . connected to provide inputs to said arithmetic logic unit ('890 Patent)

4. address/data bus ('890 Patent)

5. an internal data bus, said internal data bus being bidirectionally connected to a [ ] ('890 Patent)

6. incrementer / decrementer ('890 Patent)

7. return push down stack ('890 Patent)

8. separate direct memory access central processing unit ('890 Patent)

9. X register / Y register ('890 Patent)

10. an entire oscillator disposed upon said integrated circuit substrate ('336 Patent)

Defendants believe that the construction of each of the above terms may be dispositive as to the claims in which those terms appear. Plaintiffs agree that the "means . . . for fetching" term listed as item 2 is claim dispositive for the claim in which it appears.

IV. ANTICIPATED LENGTH OF CLAIM CONSTRUCTION HEARING (Patent Local Rule 4-3(d))

The claim construction hearing has been scheduled for February 26, 2016 at 10:00 a.m. The technology tutorial has been scheduled for February 19, 2016 at 10:00 a.m.

Plaintiffs expect that the length of the claim construction hearing should be no more than 3 hours total (1.5 hours per side) and expect that the length for the tutorial should be no more than 1 hour (30 minutes per side).

Defendants request that Court provide the parties a full day, with equal time for each side, for the claim construction hearing. Although the Court has previously considered certain terms of

the Asserted Patents in a prior case, the present Defendants have not previously presented their positions, the majority of the terms listed in Section III have not been previously construed by the Court, and the asserted '749 and '890 Patents were not part of the trial in the prior case (indeed only one term from the previously tried '336 Patent is presented for construction here). For similar reasons, Defendants request that the Court provide two hours (one hour per side) for the technology tutorial.

V. WITNESSES FOR THE CLAIM CONSTRUCTION HEARING (Patent Local Rule 4-3(e))

Plaintiffs and Defendants do not currently plan to call any fact or expert witnesses to testify live at the claim construction hearing. However, to the extent that Plaintiffs or Defendants later decide that expert testimony is necessary and offer such testimony, then the parties agree that the other side may submit rebuttal expert testimony.

Respectfully submitted,

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ATTESTATION PER GENERAL ORDER 45

I, Barry J. Bumgardner, am the ECF User whose ID and password are being used to file this Stipulation. In compliance with General Order 45, X.B., I hereby attest that the counsel listed above have concurred with this filing.

Dated: June 23, 2015

Exhibit A

Claim Terms and Constructions Agreed Upon by the Parties

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
		'749 PATENT		
1.	a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item	a portion of the first push down stack that receives items pushed from the means for storing next item and stores items on a "last in, first out" basis	a portion of the first push down stack that receives items pushed from the means for storing next item and stores items on a "last in, first out" basis	
2.	arithmetic logic unit	a digital circuit that performs arithmetic and logical operations	a digital circuit that performs arithmetic and logical operations	
3.	central processing unit	electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions	electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions	
4.	central processing unit integrated circuit	miniature circuit, on a single semiconductor substrate, that controls the interpretation and execution of programmed instructions	miniature circuit, on a single semiconductor substrate, that controls the interpretation and execution of programmed instructions	
5.	configured and connected to . . . supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle	configured and connected to . . . provide the multiple sequential instructions in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during a single memory cycle	configured and connected to . . . provide the multiple sequential instructions in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during a single memory cycle	

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
6.	first input of said ALU	a first input of the [ALU] for receiving data	a first input of the [ALU] for receiving data	
7.	means for storing a next item	Construed pursuant to 35 U.S.C. § 112(6) Structure: a register or its equivalents Function: storing a next item	Construed pursuant to 35 U.S.C. § 112(6) Structure: a register or its equivalents Function: storing a next item	
8.	means for storing a top item	Construed pursuant to 35 U.S.C. § 112(6) Structure: a register or its equivalents Function: storing a top item	Construed pursuant to 35 U.S.C. § 112(6) Structure: a register or its equivalents Function: storing a top item	
9.	memory external of said central processing unit integrated circuit	a memory on a separate substrate from the [central processing unit integrated circuit]	a memory on a separate substrate from the [central processing unit integrated circuit]	
10.	multiple sequential instructions	two or more instructions in a program sequence	two or more instructions in a program sequence	
11.	multiplexing means	a multiplexer	a multiplexer	
12.	second input of said ALU	a second input, distinct from the first input, of the ALU for receiving data	a second input, distinct from the first input, of the ALU for receiving data	
13.	single memory cycle	the time required to read information from the memory	the time required to read information from the memory	

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
		'890 PATENT		
14.	bus	a group of conductors	a group of conductors	
15.	central processing unit	electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions.	electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions.	
16.	loop counter	counter circuit in the main [CPU] that stores a variable value representing a remaining number of times a particular instruction or group of instructions is to be executed by the main [CPU]	counter circuit in the main [CPU] that stores a variable value representing a remaining number of times a particular instruction or group of instructions is to be executed by the main [CPU]	
17.	mode register	register that stores mode bits.	register that stores mode bits.	
18.	multiplexing means	a multiplexer	A multiplexer	
19.	return stack pointer	storage element in the main [central processing unit], separate and distinct from the stack pointer, that stores a value representing a location in the return push down stack	storage element in the main [central processing unit], separate and distinct from the stack pointer, that stores a value representing a location in the return push down stack	
20.	ring oscillator	an [oscillator] having multiple, odd number of inversions arranged in a loop, wherein the [oscillator] is variable based on the temperature, voltage and process parameters in the environment	an [oscillator] having multiple, odd number of inversions arranged in a loop, wherein the [oscillator] is variable based on the temperature, voltage and process parameters in the environment	

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
		'336 PATENT		
21.	central processing unit	electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions	electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions	
22.	clocking said central processing unit	providing a timing signal to said [central processing unit]	providing a timing signal to said [central processing unit]	
23.	external clock is operative at a frequency independent of a clock frequency of said oscillator	external clock wherein a change in the frequency of either the external clock or [oscillator] does not affect the frequency of the other	external clock wherein a change in the frequency of either the external clock or [oscillator] does not affect the frequency of the other	
24.	external memory bus	a [bus] coupled between the I/O interface and an external storage device	a [bus] coupled between the I/O interface and an external storage device	
25.	integrated circuit	miniature circuit on a single semiconductor substrate	miniature circuit on a single semiconductor substrate	`
26.	microprocessor	electronic circuit that interprets and executes programmed instructions	electronic circuit that interprets and executes programmed instructions	
27.	off-chip external clock	clock not on the integrated circuit substrate	clock not on the integrated circuit substrate	

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
28.	on-chip input/output interface	circuit having logic for input/output communications, where that circuit is located on the same semiconductor substrate as the [CPU]	circuit having logic for input/output communications, where that circuit is located on the same semiconductor substrate as the [CPU]	
29.	oscillator	circuit capable of maintaining an alternating output	circuit capable of maintaining an alternating output	
30.	oscillator . . . clocking	[oscillator] that generates the signal(s) used for timing the operation of the [CPU]	[oscillator] that generates the signal(s) used for timing the operation of the [CPU]	
31.	processing frequency	speed at which the [CPU] operates.	speed at which the [CPU] operates	
32.	ring oscillator	an [oscillator] having multiple, odd number of inversions arranged in a loop, wherein the [oscillator] is variable based on the temperature, voltage and process parameters in the environment	an [oscillator] having multiple, odd number of inversions arranged in a loop, wherein the [oscillator] is variable based on the temperature, voltage and process parameters in the environment	
33.	varying . . . in the same way	increasing and deceasing proportionally	increasing and deceasing proportionally	
34.	wherein said central processing unit operates asynchronously to said input/output interface	The timing control of the [central processing unit] that operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them.	The timing control of the [central processing unit] that operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them.	

Exhibit B

Claim Terms and Constructions Disputed by the Parties

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
		'749 PATENT		
1.	instruction register	A register that receives and holds one or more instructions for supplying to circuits that interpret the instructions.	register that holds an instruction while the instruction is being decoded and executed, and that excludes temporary registers upstream of the register	

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
2.	means … for fetching instructions for said central processing unit integrated circuit on said bus from said memory, said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle	Construed pursuant to 35 U.S.C. § 112(6) Structure: memory controller Function: fetching instructions for the [central processing unit integrated circuit] on the [bus] from said memory, being [configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle]	Function: "fetching instructions for said central processing unit integrated circuit on said bus from said memory . . . to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle" Indefinite for insufficient disclosure of corresponding structure. No algorithm disclosed to perform function.	
3.	push down stack connected to said arithmetic logic unit	A last-in-first-out data storage element connected to the [arithmetic logic unit].	last-in-first-out storage element that outputs data to the [arithmetic logic unit] in response to instructions with only implied addresses	

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
4.	wherein the means for fetching instructions . . . comprises supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched	wherein the means for fetching instructions includes supplying the multiple sequential instructions in parallel (as opposed to one-by-one) to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched in parallel (as opposed to one-by-one)	indefinite	The parties have agreed to forego briefing on this term during the claim construction phase in light of the pending motion for judgment on the pleadings.

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
		'890 PATENT		
5.	an address/data bus	A [bus] which carries address and/or data signals.	a [bus] including at least one conductor that carries address and data information on the same conductor	

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
6.	an internal data bus, said internal data bus being bidirectionally connected [to a loop counter]	A [bus] internal to the [microprocessor] that is connected such that data can flow in two directions.	a [bus], internal to the [microprocessor], including at least one conductor that carries data into the [loop counter] and out of the [loop counter] on the same conductor	
7.	decrementer	A circuit that decrements a register.	logic circuit separate from the [arithmetic logic unit] designed to decrease its input and output the result	
8.	incrementer	A circuit that increments a register.	logic circuit separate from the [arithmetic logic unit] designed to increase its input and output the result	
9.	instruction register	A register that receives and holds one or more instructions for supplying to circuits that interpret the instructions.	a register that holds an instruction while the instruction is being decoded and executed, and that excludes temporary registers upstream of the register	

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
10.	means for fetching instructions for said central processing unit on said address/data bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle	Construed pursuant to 35 U.S.C. § 112(6) Structure: an internal data bus of sufficient width to retrieve multiple instructions at one time, an internal address bus, and a multiplexer to selectively connect the internal data and address busses to the [address/data bus], and structural equivalents thereof. Function: fetching instructions for said [central processing unit] on said [address/data bus].	Function: fetching instructions for said [central processing unit] on said [address/data bus], said means for fetching instructions being configured to fetch multiple sequential instructions in a [single memory cycle] Corresponding structure: indefinite for insufficient disclosure of corresponding structure. No algorithm disclosed to perform function.	Although the parties dispute the construction of this term, the parties have agreed to not include this term as one of the top 10 terms whose construction will be most significant to the resolution of the case.
11.	push down stack . . . connected to provide inputs to said arithmetic logic unit	A last-in-first-out storage unit connected to provide data to the [arithmetic logic unit].	last-in-first-out storage element that provides data to the [arithmetic logic unit] in response to instructions with only implied addresses	
12.	return push down stack	last-in-first-out data storage element that stores return addresses	last-in-first-out data storage element in the main [central processing unit], separate from the first push down stack, that stores return addresses	

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
13.	separate direct memory access central processing unit	A central processing unit that accesses memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit.	central processing unit that accesses memory, that fetches and executes instructions for itself directly and separately from the main central processing unit, and that fetches instructions for the main central processing unit	
14.	X register	A first register used in memory operations.	memory pointer which can be used for memory access and simultaneously incremented or decremented	
15.	Y register	A second register used in memory operations.	memory pointer which can be used for memory access and simultaneously incremented or decremented	

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
'336 PATENT				
16.	an entire oscillator disposed upon said integrated circuit substrate	An [oscillator] that is located entirely on the same semiconductor substrate as the [central processing unit].	an [oscillator] that is located entirely on the same semiconductor substrate as the [central processing unit] and does not rely on a control signal or an external crystal/clock generator to cause clock signal oscillation or control clock signal frequency	

Exhibit C

Claim Terms, Plaintiffs' Proposed Constructions, and Intrinsic and Extrinsic Evidence Citations

A. U.S. Pat. No. 5,440,749[1]

Nos.	'749 Patent Claim Term	Proposed Construction	Intrinsic Evidence Citations	Extrinsic Evidence Citations
1.	instruction register	A register that receives and holds one or more instructions for supplying to circuits that interpret the instructions.	'749 Pat., at Fig. 2, Fig. 16, Fig. 20, 2:39 - 3:15, 4:50-63, 5:8-9, 5:15-25, 6:24 - 7:28, 7:50 - 8:42, 9:18-36, 10:44 - 11:20, 11:56 - 12:2, 14:13-20, 16:21 - 17:17, 17:59 - 18:18, 18:35-56, 19:6-43, 22:12 - 23:8, 35:58 - 36:41, 37:45-50 '749 Pat. Prosecution History: Response to Office Action (Jan. 19, 2010), at pp. 37-44	Hordeski at 177 Judge Grewal's Claim Construction Order

[1] Language in brackets "[]" are words/terms construed elsewhere. References to figures in a patent also includes references to the portions of the patent that discuss the figures.

Exhibit C

Claim Terms, Plaintiffs' Proposed Constructions, and Intrinsic and Extrinsic Evidence Citations

2.	means … for fetching instructions for said central processing unit integrated circuit on said bus from said memory, said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle	Construed pursuant to 35 U.S.C. § 112(6) Structure: memory controller Function: fetching instructions for the [central processing unit integrated circuit] on the [bus] from said memory, being [configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle]	'749 Pat. at Figs. 2, 4, 11, 12, 16, and 20, 2:13-26, 2:34-48, 5:45, 5:54-58, 7:12-22, 7:33-35, 7:50-8:16, 14:25-26, 14:66-15:20, 18:10-13, 18:34-56, 20:33-22:40, 25:65-26:35, 31:35-32:16, 33:13-17 '749 Pat. Prosecution History: Response to Office Action (June 3, 1992) at pp. 12-13, 15-16 Response To Office Action (June 30, 1993) pp. 12-13 Response to Office Action (Mar. 17, 1994) at pp. 4-7 Response to Office Action (Nov. 9, 1994) at pp. 4-6 '749 Pat. Prosecution History: Office Action (Feb. 11, 2011) at p. 8 Response to Office Action (Jan. 25, 2011) at pp. 17-19 Examiner's Interview Summary (Nov. 24, 2010) Response to Office Action (Nov. 29, 2010) at pp. 18-20, 23-35 Response to Office Action (Jan. 19, 2010) at pp. 25-35 Response to Office Action (May	

Exhibit C

Claim Terms, Plaintiffs' Proposed Constructions, and Intrinsic and Extrinsic Evidence Citations

			4, 2009) at. pp. 26-27, 34-35 Examiner's Interview Summary (Apr. 7, 2009) '890 Patent: '890 Pat. at 29:25-30:2	

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Claim Terms, Plaintiffs' Proposed Constructions, and Intrinsic and Extrinsic Evidence Citations

Nos.	'749 Patent Claim Term	Proposed Construction	Intrinsic Evidence Citations	Extrinsic Evidence Citations
3.	push down stack connected to said arithmetic logic unit	A last-in-first-out data storage element connected to the [arithmetic logic unit].	'749 Pat. at Figs. 2, 4, 11, 12, 13, 16, 20, and 21, 2:13-26, 3:4-15, 3:36-66, 5:45, 5:54-58, 6:24-35, 7:18-22, 7:50-56, 8:4-16, 14:25-65, 14:66, 15:20, 15:24-52, 18:10-13, 19:6-8, 22:14-24, 25:65-26:11, 26:16-29, 31:35-32:16, claims 1 and 9. '749 Pat. Prosecution History: Response to Office Action (June 30, 1993) at pp. 9-10 Response to Office Action (Nov. 9, 1994) at pp. 4-6 '890 Patent: '890 Pat. at 17:65-18:11, 18:24-45, 21:5-37, 21:51-54, 24:10-20 Reexamination App. No. 90,009,388: Response to Office Action (Jan. 5, 2010), at p. 6-7 Response to Office Action (June 29, 2010), at pp. 10-19	Hordeski at 15, 292, 313, 369-70 Microsoft Computer Dictionary at 20, 271, 327 Judge Ware's Claim Construction Order

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Claim Terms, Plaintiffs' Proposed Constructions, and Intrinsic and Extrinsic Evidence Citations

4.	wherein the means for fetching instructions . . . comprises supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched	wherein the means for fetching instructions includes supplying the multiple sequential instructions in parallel (as opposed to one-by-one) to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched in parallel (as opposed to one-by-one)	'749 Pat. at Figs. 2, 4, 11, 12, 16, and 20, 2:13-26, 2:34-48, 5:45, 5:54-58, 7:12-22, 7:33-35, 7:50-8:16, 14:25-26, 14:66-15:20, 18:10-13, 18:34-56, 20:33-22:40, 25:65-26:35, 31:35-32:16, 33:13-17 '749 Pat. Prosecution History: Response to Office Action (June 3, 1992) at pp. 12-13, 15-16 Response To Office Action (June 30, 1993) pg. 12-13 Response to Office Action (Mar. 17, 1994) at pp. 4-7 Response to Office Action (Nov. 9, 1994) at pp. 4-6 Office Action (Feb. 11, 2011) at p. 8 Response to Office Action (Jan. 25, 2011) at pp. 17-19 Examiner's Interview Summary (Nov. 24, 2010) Response to Office Action (Nov. 29, 2010) at pp. 18-20, 23-35 Response to Office Action (Jan. 19, 2010) at pp. 25-35 Response to Office Action (May 4, 2009) at. pp. 26-27, 34-35 Examiner's Interview Summary (Apr. 7, 2009)	Hordeski at 223 Judge Grewal's Claim Construction Order

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Claim Terms, Plaintiffs' Proposed Constructions, and Intrinsic and Extrinsic Evidence Citations

Nos.	'749 Patent Claim Term	Proposed Construction	Intrinsic Evidence Citations	Extrinsic Evidence Citations
			'890 Patent: '890 Pat. at 29:25-30:2	

B. U.S. Pat. No. 5,530,890

Nos.	'890 Patent Claim Term	Proposed Construction	Citations to Intrinsic Evidence	Citations to Extrinsic Evidence
5.	address/data bus	A [bus] which carries address and/or data signals.	'890 Pat., at Abstract, Figs. 2, 4-6, 10-13, 17, 19, 21, 2:6-36, 5:48-65, 6:17-7:10, 7:30-67, 8:1-40, 8:56-9:41, 10:19-11:13, 11:45-50, 12:50-60, 13:33-14:49, 15:10-31, 16:11-29, 17:4-30, 17:44-64, 20:53-67, 21:55-67, 22:1-23:67, 27:48-29:15, 32:44-33:11	Hordeski at 7, 43-44 Microsoft Computer Dictionary at 10, 49

Exhibit C

Claim Terms, Plaintiffs' Proposed Constructions, and Intrinsic and Extrinsic Evidence Citations

Nos.	'890 Patent Claim Term	Proposed Construction	Citations to Intrinsic Evidence	Citations to Extrinsic Evidence
6.	an internal data bus, said internal data bus being bidirectionally connected	A [bus] internal to the [microprocessor] that is connected such that data can flow in two directions.	'890 Pat., at Abstract, Figs. 10-13, 17, 19, 2:6-36, 3:4-15, 5:48-52, 6:17-17:10, 7:36-67, 8:1-21, 8:56-9:41, 11:45-50, 13:16-20, 13:33-14:49, 15:10-31, 16:11-29, 17:4-30, 17:44-64, 20:53-67, 21:55-67, 32:34-67	Hordeski at 7, 43-44 Microsoft Computer Dictionary at 10, 49
7.	decrementer	A circuit that decrements a register.	'890 Pat., at Abstract, Figs. 2, 5, 2:43-3:3, 4:46-57, 5:4-5, 5:12-13, 6:17-48, 8:1-24, 9:5-10, 10:18-11:4, 11:32-37, 16:12-28, 17:7-12, 18:12-14, 20:17-41, 21:1-22:50, 23:62-67, 25:39-29:15, 32:44-67 '890 Pat. Reexam Certificate (Mar. 1, 2011), at Abstract, 1:22-47	Hordeski at 89-90 Microsoft Computer Dictionary at 100

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Claim Terms, Plaintiffs' Proposed Constructions, and Intrinsic and Extrinsic Evidence Citations

Nos.	'890 Patent Claim Term	Proposed Construction	Citations to Intrinsic Evidence	Citations to Extrinsic Evidence
8.	incrementer	A circuit that increments a register.	'890 Pat., at Abstract, Figs. 2, 5, 2:43-3:3, 4:46-57, 5:4-5, 5:12-13, 6:17-48, 8:1-24, 9:5-10, 10:18-11:4, 11:32-37, 16:12-28, 17:7-12, 18:12-14, 20:17-41, 21:1-22:50, 23:62-67, 25:39-29:15, 32:44-67 '890 Pat. Reexam Certificate (Mar. 1, 2011), at Abstract, 1:22-47	Hordeski at 171 Microsoft Computer Dictionary at 183
9.	instruction register	A register that receives and holds one or more instructions for supplying to circuits that interpret the instructions.	'890 Pat. at Abstract, Figs. 2, 4, 16, 20, 2:43-3:3, 4:46-57, 5:4-21, 6:17, 6:30-33, 6:47-48, 7:36-8:24, 9:5-10, 10:18-57, 11:23-37, 15:40-16:35, 16:47-67, 17:7-12, 17:44-64, 18:12-14, 20:42-21:55, 29:25-30:2, 32:44-67 '890 Pat. Reexam Certificate (Mar. 1, 2011) at Abstract, 1:22-47 '749 Patent: '749 Pat., at 31:35-32:16	Hordeski at 177, 330 Microsoft Computer Dictionary at 190, 295 Judge Grewal's Claim Construction Order

Exhibit C

Claim Terms, Plaintiffs' Proposed Constructions, and Intrinsic and Extrinsic Evidence Citations

Nos.	'890 Patent Claim Term	Proposed Construction	Citations to Intrinsic Evidence	Citations to Extrinsic Evidence
10.	means for fetching instructions for said central processing unit on said address/data bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle	Construed pursuant to 35 U.S.C. § 112(6) Structure: an internal data bus of sufficient width to retrieve multiple instructions at one time, an internal address bus, and a multiplexer to selectively connect the internal data and address busses to the [address/data bus], and structural equivalents thereof. Function: fetching instructions for said [central processing unit] on said [address/data bus].	'890 Pat. at Abstract, Figs. 2, 4-6, 10-13, 17, 19, 21, 2:6-36, 5:48-65, 6:17-7:10, 7:30-67, 8:1-40, 8:56-9:41, 10:19-11:13, 11:45-50, 12:50-60, 13:33-14:49, 15:10-31, 16:11-29, 17:4-30, 17:44-64, 20:53-67, 21:55-67, 22:1-23:67, 27:48-29:15, 32:44-67, 33:1-11	Hordeski at 7, 43-44, 75, 174, 223 Microsoft Computer Dictionary at 10, 49, 187-88

Exhibit C

Claim Terms, Plaintiffs' Proposed Constructions, and Intrinsic and Extrinsic Evidence Citations

11.	push down stack . . . connected to provide inputs to said arithmetic logic unit	A last-in-first-out storage unit connected to provide data to the [arithmetic logic unit].	'890 Pat., at Abstract, Figs. 2, 4, 9, 13, claims 1 and 9, 2:5-33, 3:4-4:36, 4:60-63, 6:18-7:67, 8:64-9:13, 11:4-12:43, 14:50-15:10, 17:33-43, 17:65-19:26, 21:1-67, 24:1-44, 25:38-32:67, 34:10-17 '890 Pat. Reexam Certificate (Mar. 1, 2011), at Abstract, 1:22-47, 2:37-45 '749 Patent: '749 Pat., at Figs. 2, 13, 21, claims 1 and 9, 3:4-15, 3:36-66, 6:28-35, 7:18-22, 15:24-52, 19:6-8, 25:65-26:11 '749 Prosecution History: Response to Office Action (July 6, 1993), at pp. 9-10 Re-Exam App. 90,009,388: Response to Office Action (Jan. 5, 2010), at pp. 7 Response to Office Action (June 29, 2010), at pp. 17-18 Office Action (12/31/92; page 3) and Applicant's response (deposited 6/30/93; page 9)	Hordeski at 15, 292, 313, 369-370 Microsoft Computer Dictionary at 20, 271, 327

Exhibit C

Claim Terms, Plaintiffs' Proposed Constructions, and Intrinsic and Extrinsic Evidence Citations

Nos.	'890 Patent Claim Term	Proposed Construction	Citations to Intrinsic Evidence	Citations to Extrinsic Evidence
12.	return push down stack	last-in-first-out data storage element that stores return addresses	'890 Pat., at Abstract, Figs. 2, 12, 6:28-46, 11:32-37, 14:28-50, 21:2-55, 23:34-40, 26:58-30:53, 32:33-38, claim 1	

Exhibit C

Claim Terms, Plaintiffs' Proposed Constructions, and Intrinsic and Extrinsic Evidence Citations

Nos.	'890 Patent Claim Term	Proposed Construction	Citations to Intrinsic Evidence	Citations to Extrinsic Evidence
13.	separate direct memory access central processing unit	A central processing unit that accesses memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit.	'890 Pat., at Abstract, Figs. 2, 5, 9, 12, 17, 1:52-2:37, 3:26-63, 4:46-5:5, 5:12-16, 5:33-42, 6:17-48, 8:1-24, 8:56-9:61, 10:18-57, 11:32-50, 12:61-13:57, 14:27-49, 16:14-16, 16:36-17:43, 18:12-14, 21:1-55, 32:44-33:11, 33:33-34:33 '890 Pat. Reexam Certificate (Mar. 1, 2011), at Abstract, 1:22-59, 2:23-61 '148 Reexamination Response to Office Action (Mar. 27, 2009), at pp. 6-7 (Interview Summary), and pp. 9-11 '148 Reexam File History (90/008,227): 3/3/2009 Examiner's Interview Summary, p. 2	Microsoft Computer Dictionary at 108 Judge Grewal's Claim Construction Order

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Claim Terms, Plaintiffs' Proposed Constructions, and Intrinsic and Extrinsic Evidence Citations

Nos.	'890 Patent Claim Term	Proposed Construction	Citations to Intrinsic Evidence	Citations to Extrinsic Evidence
14.	X register	A first register used in memory operations.	'890 Pat., at Figs. 2, 4, 5, 12, 13, 16, 20-23, 6:17-7:16, 7:36-67, 8:1-24, 10:18-11:4, 11:23-33, 14:28-15:21, 15:41-16:46, 17:45-19:26, 21:1-67, 25:38-32:42	Hordeski at 330 Microsoft Computer Dictionary at 295
15.	Y register	A second register used in memory operations.	'890 Pat., at Figs. 2, 4, 5, 12, 13, 16, 20-23, 6:17-7:16, 7:36-67, 8:1-24, 10:18-11:4, 11:23-33, 14:28-15:21, 15:41-16:46, 17:45-19:26, 21:1-67, 25:38-32:42	Hordeski at 330 Microsoft Computer Dictionary at 295

Exhibit C

Claim Terms, Plaintiffs' Proposed Constructions, and Intrinsic and Extrinsic Evidence Citations

C. U.S. Pat. No. 5,809,336

Nos.	'336 Patent Claim Term	Proposed Construction	Intrinsic Evidence Citations	Extrinsic Evidence Citations
16.	an entire oscillator disposed upon said integrated circuit substrate	An [oscillator] that is located entirely on the same semiconductor substrate as the [central processing unit].	'336 Pat., at Abstract, Figs. 1, 17-19, 1:14-3:35, 4:41-5:42, 5:53-6:27, 6:47-10:60, 11:8-15:63, 16:14-18:4, 18:20-19:50, 20:27-21:57, 22:4-24:15, 24:28-25:47, 26:40-53, 27:16-21, 28:59-29:10, 30:28-45, and 32:12-34:28 '336 Pat. Reexam Certificate (Dec. 15, 2009), at 2:13-41, 3:29-4:9 '336 Prosecution History, Amendment B, mailed April 11, 1996, at pp. 6-7 '336 Prosecution History, Amendment D, mailed July 3, 1997, at pp. 4-5 '336 Prosecution History, Amendment E, mailed February 6, 1998, at pp. 3-4 '148 Re-exam Response to Office Action February 21, 2008, at p. 7 (interview summary), pp. 11-12	Hordeski at 58, 94, 178, 269, 316, 336, 377 Microsoft Computer Dictionary at 250 Judge Ward's Claim Construction Order

Exhibit D

Claim Terms, Defendants' Proposed Constructions, and Intrinsic and Extrinsic Evidence Citations

U.S. Patent No. 5,440,749

Nos.	Identified Term[1]	Defendants Proposed Construction(s)	Intrinsic Support	Extrinsic Support
1.	instruction register (claims 1, 59) *(Defendants)*	register that holds an instruction while the instruction is being decoded and executed, and that excludes temporary registers upstream of the register	'749 patent, Claims; '749 patent, Figs. 2, 4; '749 Patent at 2:40-43, 4:47-5:30, 7:50-55, 8:7-16, 18:35-56, 22:65 – 23:3; '388 Reexamination of the '890 patent at 6/29/2010: Amdmt. at 7, 10-11, 19. 1/19/2010 Remarks '034 Reexamination of '749 patent discussing "The Motorola MC68020" written by Doug MacGregor at 1/19/2010 Remarks at 26 and 44-50; 11/29/2010 interview summary at 19-20; 11/29/10 Remarks at 30-31, and 33-35; 12/16/2010 Advisory Action at 10-11, and 13-17; 2/10/2011 Notice of Intent to Issue Ex Parte	Michael F. Hordeski, The Illustrated Dictionary of Microcomputers (3rd ed. 1990), at p. 177. Defendants may also offer expert testimony for this term. The testimony is expected to discuss why their construction is consistent with how one of ordinary skill in the art would understand the term in context of the patent. Deposition of named inventors, including in this case and cases involving the same patent.

[1] Claims 1, 43, and 59 are asserted. Claim 43 depends from independent claim 1. Claim 59 depends from independent claim 9.

Nos.	Identified Term[1]	Defendants Proposed Construction(s)	Intrinsic Support	Extrinsic Support
			Reexamination Certificate at 8-11; Doug McGregor, The Motorola MC 68020, 110-111.	
2.	means … for fetching instructions for said central processing unit integrated circuit on said bus from said memory, said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle (claim 1[2]) *(Defendants – 112 ¶ 6)*	Function: "fetching instructions for said central processing unit integrated circuit on said bus from said memory . . . to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle" Indefinite for insufficient disclosure of corresponding structure. No algorithm disclosed to perform function.	'749 patent, Claims; '749 patent at 4:47-5:30, 7:12, 7:50-55, 10:44-55, 16:21-23, 18:10-12, 20:38-52, 21:30-34, 22:19-22, 22:30-33, 26:31-32.	Defendants may also offer expert testimony for this term. The testimony is expected to discuss why their construction is consistent with how one of ordinary skill in the art would understand the term in context of the patent. Deposition of named inventors, including in this case and cases involving the same patent.

[2] Note the claim 9 recites similar language: "means … for fetching instructions for said central processing unit on said bus from said dynamic random access memory, said means for fetching instructions being configured to fetch multiple sequential instructions from said dynamic random access memory in parallel and supply the multiple instructions to said central processing unit during a single memory cycle."

Nos.	Identified Term[1]	Defendants Proposed Construction(s)	Intrinsic Support	Extrinsic Support
3.	push down stack connected to said ALU (claims 1, 9) *(TPL/Defendants)*	last-in-first-out storage element that outputs data to the [arithmetic logic unit] in response to instructions with only implied addresses	'749 patent, Claims; '749 patent, Figs. 2, 13, 22, 23; '749 Patent at 4:34-40, 4:47-5:30, 6:28-35, 7:12-22, 15:22-52, 19:6-8, 29-44, 51-68, 20:26-32, table at col. 21, 1st through 15th line; table at col. 23, third and fourth line; 25:6-10, 25:64 – 26:18, 32:17-62, 33:33 – 34:40; 90/009,388 Reexamination: 6/29/10 Amdmt. at 7-8, 10-11, 17-18; 90/009,388 Reexamination: 1/5/2010 Response at 2-3, U.S. Pat. No. 4,989,113 (Hull Jr.) at Fig. 2 and 5:60 -6:3, and 7:55-9:3. '749 patent file history: 7/6/1993 Amdmt. at 6; '749 patent file history: 11/10/1994 Response at 1, 2 and 5. Intel 80386 Programmer's Reference Manual at 29, 31-33, 35-39, 46-47, 49-64, 239-411;	Rudolf F. Graf, Modern Dictionary of Electronics (6th ed. 1984) at pp. 798-99. Rudolf F. Graf, Modern Dictionary of Electronics (7th ed. 1999) at p. 603. Defendants may also offer expert testimony for this term. The testimony is expected to discuss why their construction is consistent with how one of ordinary skill in the art would understand the term in context of the patent. Deposition of named inventors, including in this case and cases involving the same patent.

Nos.	Identified Term[1]	Defendants Proposed Construction(s)	Intrinsic Support	Extrinsic Support
			'749 patent file history: 3/21/1994 Response at 6; '749 patent file history: 7/6/1993 Response at 4, 9-10.	
4.	wherein the means for fetching instructions … comprises supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched (claims 1, 59) *(Defendants – 112 ¶ 6)*	indefinite	'749 patent, Claims; Ex Parte Reexam Cert. at 1:29-6:47 (re-examined claims).	Defendants may offer expert testimony for this term to discuss why a person of ordinary skill in the art would understand that this term renders the asserted claims invalid for lack of definiteness.

U.S. Patent No. 5,530,890

	Identified Term[3]	Defendants Proposed Construction(s)	Intrinsic Support	Extrinsic Support
5.	an address/data bus (claims 1, 11, 12, 13) *(Defendants)*	a [bus] including at least one conductor that carries address and data information on the same conductor	'890 patent, Claims; '890 patent, Figs. 3, 4, 10, 11;	Defendants may also offer expert testimony for this term. The testimony is expected to discuss why

[3] Claims 7, 9, 11, 12, 13, 17, and 19 are asserted. Claims 7 and 9 depend from independent claim 1. Claims 12, 13, 17, and 19 depend from independent claim 11.

	Identified Term[3]	Defendants Proposed Construction(s)	Intrinsic Support	Extrinsic Support
			'890 patent at 4:53-5:25, 7:16-29, 7:54-55, 13:33-14:27.	their construction is consistent with how one of ordinary skill in the art would understand the term in context of the patent. Deposition of named inventors, including in this case and cases involving the same patent.
6.	an internal data bus, said internal data bus being bidirectionally connected [to a loop counter] (claims 1, 11) *(Defendants)*	a [bus], internal to the [microprocessor], including at least one conductor that carries data into the [loop counter] and out of the [loop counter] on the same conductor	'890 patent, Claims; '890 patent, Abstract; '890 patent at 13:16-20, 6:28-30, 4:53 – 5:25; '388 Reexamination: 6/9/2010 Response at 13, 18-19; '749 patent file history, 7/6/1993 Response at 9.	Joseph Greenfield, Microprocessor Handbook 75 (1985) IEEE Standard Dictionary of Electrical and Electronics Terms 93 (Jay, 4th ed. 1988) Michael F. Hordeski, The Illustrated Dictionary of Microcomputers (3rd ed. 1990), at p. 30 Rudolf F. Graf, Modern Dictionary of Electronics (6th ed. 1984) at p. 96.

	Identified Term[3]	Defendants Proposed Construction(s)	Intrinsic Support	Extrinsic Support
				Rudolf F. Graf, Modern Dictionary of Electronics (7th ed. 1999) at pp. 68-69. Defendants may also offer expert testimony for this term. The testimony is expected to discuss why their construction is consistent with how one of ordinary skill in the art would understand the term in context of the patent. Deposition of named inventors, including in this case and cases involving the same patent.
7.	decrementer (claims 1, 11) *(Defendants)*	logic circuit separate from the [arithmetic logic unit] designed to decrease its input and output the result	'890 patent, Claims; '890 patent, Abstract; '890 patent, Fig. 2; '890 patent at 4:53-5:25, 6:28-30, 8:12-21.	Defendants may also offer expert testimony for this term. The testimony is expected to discuss why their construction is consistent with how one of ordinary skill in the art would understand the term in context of the patent.

	Identified Term[3]	**Defendants Proposed Construction(s)**	**Intrinsic Support**	**Extrinsic Support**
				Deposition of named inventors, including in this case and cases involving the same patent.
8.	incrementer (claims 1, 11) *(Defendants)*	logic circuit separate from the [arithmetic logic unit] designed to increase its input and output the result	'890 patent, Claims; '890 patent, Fig. 2; '890 patent at 4:53-5:25, 20:25-27, 21:20-21, 21:24-25, 22:11-13, 23:10-34, 23:54-55.	Defendants may also offer expert testimony for this term. The testimony is expected to discuss why their construction is consistent with how one of ordinary skill in the art would understand the term in context of the patent. Deposition of named inventors, including in this case and cases involving the same patent.
9.	instruction register (claims 1, 11) *(Defendants)*	a register that holds an instruction while the instruction is being decoded and executed, and that excludes temporary registers upstream of the register	'890 patent, Claims; '890 patent, Figs. 2 and 4; '890 patent at 4:53-5:25, 6:30-33, 2:43-48, 7:39-41, 21:26-29,	Michael F. Hordeski, The Illustrated Dictionary of Microcomputers (3rd ed. 1990), at p. 177 Defendants may also offer expert testimony for this

	Identified Term[3]	Defendants Proposed Construction(s)	Intrinsic Support	Extrinsic Support
			15:41-45, 11:23-25, 7:61-67, 20:53-67; '388 Reexamination: 6/29/10 Amdmt. at 7, 10-11, 19. '034 Reexamination of '749 patent discussing "The Motorola MC68020" written by Doug MacGregor at 1/19/10 Remarks at 26 and 44-50; 11/29/10 interview summary at 19-20; 11/29/10 Remarks at 30-31 and 33-35; 12/16/10 Advisory Action at 10-11, and 13-17; 2/10/11 Notice of Intent to Issue Ex Parte Reexamination Certificate at 8-11. Doug MacGregor, The Motorola MC 68020, 110-111.	term. The testimony is expected to discuss why their construction is consistent with how one of ordinary skill in the art would understand the term in context of the patent. Deposition of named inventors, including in this case and cases involving the same patent.
10.	means for fetching instructions for said central processing unit on said address/data bus, said means for fetching instructions being configured to fetch	Function: fetching instructions for said [central processing unit] on said [address/data bus], said means for fetching instructions being configured to fetch multiple	'890 patent, Claims; '890 patent at 4:53-5:25, 7:1, 7:36-51, 10:18-26, 15:40-43,	Defendants may also offer expert testimony for this term. The testimony is expected to discuss why their construction is consistent with how one

	Identified Term[3]	**Defendants Proposed Construction(s)**	**Intrinsic Support**	**Extrinsic Support**
	multiple sequential instructions in a single memory cycle (claim 13) *(Defendants – 112 ¶ 6)*	sequential instructions in a [single memory cycle] Corresponding structure: indefinite for insufficient disclosure of corresponding structure. No algorithm disclosed to perform function.	17:22-25, 19:31-45, 20:17-21, 20:48-50, 20:56-60, 24:33-35.	of ordinary skill in the art would understand the term in context of the patent. Deposition of named inventors, including in this case and cases involving the same patent.
11.	push down stack . . . connected to provide inputs to said arithmetic logic unit (claims 1, 11) *(Defendants)*	last-in-first-out storage element that provides data to the [arithmetic logic unit] in response to instructions with only implied addresses	'890 patent, Claims; '890 patent at 4:43-5:25, 6:21-27, 7:1-10, 14:50-15:10; 18:13-14, 32-45, 21:5-35, 23:6-10, 24:1-22, 30:3-47, 31:11- 32:7; 90/009,'388 Reexamination patent file history: 6/29/10 Amendment at 7-8 of 21, 10-11 of 21, and 17-18 of 21; 90/009,388 Reexamination patent file history: 1/5/2010 Response to First Office Action at pages 2-3, U.S. Patent No. 4,989,113 (Hull Jr.) at Fig. 2 and 5:60 -6:3, and 7:55-9:3.	Rudolf F. Graf, Modern Dictionary of Electronics (6th ed. 1984) at pp. 798-99. Rudolf F. Graf, Modern Dictionary of Electronics (7th ed. 1999) at p. 603. Defendants may also offer expert testimony for this term. The testimony is expected to discuss why their construction is consistent with how one of ordinary skill in the art would understand the term in context of the patent.

	Identified Term[3]	**Defendants Proposed Construction(s)**	**Intrinsic Support**	**Extrinsic Support**
			’749 patent file history: 11/10/94 Response to 5th office action at pages 1, 2 and 5. Intel 80386 Programmer’s Reference Manual at 29, 31-33, 35-39, 46-47, 49-64, 239-411. ’749 patent file history: 3/21/94 Response to 4th office action at page 6 ’749 patent file history: 7/6/93 Response to 3rd office action at page 4, 9, and 10.	Deposition of named inventors, including in this case and cases involving the same patent.
12.	return push down stack (claims 1, 11) *(Defendants)*	last-in-first-out data storage element in the main [central processing unit], separate from the first push down stack, that stores return addresses	’890 patent, Claims; ’890 patent, Figs. 2, 12 ’890 patent at 6:28-46, 11:32-37, 14:27-15:10, 21:1-55, 33-36, 23:38:40, 26:59-62, 27:1-46, 29:32-45, 30:14-32, 33:33-37 June 29, 2010 Amendment, pp. 9-19	Defendants may also offer expert testimony for this term. The testimony is expected to discuss why their construction is consistent with how one of ordinary skill in the art would understand the term in context of the patent. Deposition of named inventors, including in this case and cases involving the same patent.

	Identified Term[3]	**Defendants Proposed Construction(s)**	**Intrinsic Support**	**Extrinsic Support**
13.	separate direct memory access central processing unit (claims 1, 11) *(TPL/Defendants)*	central processing unit that accesses memory, that fetches and executes instructions for itself directly and separately from the main central processing unit, and that fetches instructions for the main central processing unit	'890 patent, Claims; '890 patent, Abstract; '890 patent, Figs. 2, 5; '890 patent at 1:51-58, 2:1-5, 2:31-37, 4:53-5:25, 6:17-21, 8:1-24; '749 Patent, Abstract '749 Patent File History: 6/8/1992 Amdmt. at 14-15, 7/15/1992 IDS at 3, 7/6/93 Amdmt. at 15; '227 Reexam of '148 patent: 3/3/2009 Examiner's Interview Summary at 2.	*Acer, et al. v. TPL, et al.*, Case No. C08-00877 PSG (N.D. Cal.), Dkt. No. 514 (August 21, 2013) Claim Construction Order at pp. 12-14 Defendants may also offer expert testimony for this term. The testimony is expected to discuss why their construction is consistent with how one of ordinary skill in the art would understand the term in context of the patent. Deposition of named inventors, including in this case and cases involving the same patent.
14.	X register (claims 1, 11) *(Defendants)*	memory pointer which can be used for memory access and simultaneously incremented or decremented	'890 patent, Claims; '890 patent, Fig. 2; '890 patent, Abstract;	Defendants may also offer expert testimony for this term. The testimony is expected to discuss why their construction is consistent with how one

	Identified Term[3]	Defendants Proposed Construction(s)	Intrinsic Support	Extrinsic Support
			'890 patent at 4:53-5:25, 21:2-54, 21:56-60, 27:56-59, 4:46-47, 6:35-44, 10:59-64; '388 Reexamination: 6/29/10 Amdmt. at 7, 10-11, 19.	of ordinary skill in the art would understand the term in context of the patent. Deposition of named inventors, including in this case and cases involving the same patent.
15.	Y register (claims 1, 11) *(Defendants)*	memory pointer which can be used for memory access and simultaneously incremented or decremented	'890 patent, Claims; '890 patent, Fig. 2; '890 patent, Abstract; '890 patent at 21:2-54, 21:56-60, 27:59-62, 4:46-47, 4:53-5:25, 6:35-44, 10:59-64; '388 Reexamination, 6/29/2010 Amdmt. at 7, 10-11, 19.	Defendants may also offer expert testimony for this term. The testimony is expected to discuss why their construction is consistent with how one of ordinary skill in the art would understand the term in context of the patent. Deposition of named inventors, including in this case and cases involving the same patent.

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	Identified Term[4]	**Defendants Proposed Construction(s)**	**Intrinsic Support**	**Extrinsic Support**
16.	an entire oscillator disposed upon said integrated circuit substrate (claims 6, 13) *(Defendants)*	an [oscillator] that is located entirely on the same semiconductor substrate as the [central processing unit] and does not rely on a control signal or an external crystal/clock generator to cause clock signal oscillation or control clock signal frequency	'336 patent, Claims; '336 patent, Figs. 1, 5, 17-19; '336 patent, Abstract; '336 patent at 3:26-35, 4:41-45, 5:10-16, 16:43-17:50; 6/7/95 Orig. Appl. at 31-33, 64-83; 12/12/95 OA at 2-3; 4/11/96 Amdmt. at 1-10; 7/8/96 OA at 2-4; 1/8/97 Amdmt. at 1-5; 4/3/97 OA at 2; 7/3/97 Amdmt. at 1-5; 10/16/97 OA at 2-4; 2/6/98 Amdmt. at 1-5; 4/24/98 Supp. Amdmt. at 1-3; 5/13/98 Interview Summ. Rec.. U.S. Pat. No. 3,967,104 (Brantingham);	Defendants may also offer expert testimony for this term. The testimony is expected to discuss why their construction is consistent with how one of ordinary skill in the art would understand the term in context of the patents. Order No. 31: Construing the Terms of the Asserted Claims of The Patent at Issue, issued in USITC Inv. No. 337-TA-853 (Apr. 18, 2013), at pp. 20-42. First Claim Construction Order (Jun. 12, 2012), Case No. 5:08-cv-00877, *Acer, Inc. et al. v. Tech. Props. Ltd., et al.*, including at pp. 18-19. Memorandum Opinion and Order (Jun. 15, 2007), Case No. 2:05-cv-00494, *Tech. Props Ltd. et al. v.*

[4] Claims 6, 7, 9, 13, 14, and 15 are asserted. Claims 7 and 9 depend from independent claim 6. Claims 14 and 15 depend from independent claim 13.

	Identified Term[4]	Defendants Proposed Construction(s)	Intrinsic Support	Extrinsic Support
			U.S. Pat. No. 4,503,500 (Magar); U.S. Pat. No. 4,627,082 (Pelgrom); U.S. Pat. No. 4,338,675 (Palmer); U.S. Pat. No. 4,680,698 (Edwards et al.); U.S. Pat. No. 4,453,229 (Schaire); U.S. Pat. No. 4,670,837 (Sheets); U.S. Pat. No. 4,689,581 (Talbot); U.S. Pat. No. 5440,749 file history: 12/31 92 OA at 1-10; 7/28/93 Amdmt. at 11-17.	*Matsushita Elec. Indus. Co., Ltd. et al.* , including at pp. 11-12. Corrected Amended Patent Local Rule 4-3 Joint Claim Construction and Prehearing Statement at pp. 4-9, filed as D.I. 336 in *HTC Corp. v. Tech. Props. Ltd.*, Case No. 5:08-cv-00882-PSG. Declaration of Nan E. Joesten, Ex. A, filed as D.I. 305 in *HTC Corp. v. Tech. Props. Ltd.*, Case No. 5:08-cv-00882-PSG. Deposition of named inventors, including in cases involving the same patents (such as USITC Inv. No. 337-TA-853).