EXHIBIT 3

EXHIBIT E-1 – CLAIM CHART FOR INFRINGEMENT OF U.S. PATENT NO. 5,809,336 By Samsung

Claim 6		Claim Element
6. A microprocessor system comprising:	On information and belief, each Accused Product listed in the attached list of Accused Products (Ex. A.4), including phones, printers, and home entertainment systems, contains a **microprocessor** ("Accused Microprocessors").[1] For example, the Samsung GT-i5500 Galaxy 5 / Corby Smartphone contains a Qualcomm MSM7227. *See* Ex. A.4 for listings of microprocessors in the Accused Products with information obtained from http://www.phonescoop.com/; http://pdadb.net/; http://www.gsmarena.com/. *See also* Samsung service manuals at PDSND085415- PDSND085766, PDSND088713-PDSND108874, PDSND109662- PDSND110077. Each microprocessor is an electronic circuit that interprets and executes programmed instructions.	6.a
a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;	On information and belief, each Accused Microprocessor in each Accused Product contains a **central processing unit** (CPU), which is an electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions. Each CPU operates at a processing frequency. Each CPU and an entire oscillator are constructed on a single integrated circuit comprising semiconductor-based transistors, or electronic devices. An integrated circuit is a miniature circuit on a single semiconductor substrate. *See* http://www.merriam-webster.com/dictionary/microprocessor. For example: • The Qualcomm MSM7227 microprocessor includes an ARM core CPU.	6.b

[1] Infringement by the Accused Products is largely based on the operation of and implementation of the microprocessors they contain. This chart provides some examples of such operation that, on information and belief, are representative of the operation of the processors in each of the Accused Products. Discovery is in the early stages, and Plaintiffs anticipate receiving additional documents showing the exact operation of the processor in each of the Accused Products with respect to the accused functionality. But because many documents that Plaintiffs would rely on to establish infringement are confidential and have not yet been produced in this litigation, Plaintiffs anticipate receiving additional documents to confirm the operational principles shown in this chart from Defendants and/or third parties. Accordingly, Plaintiffs reserve the right to amend, supplement, or augment their claim charts, infringement contentions, or infringement theories based on documents and information later received through discovery.

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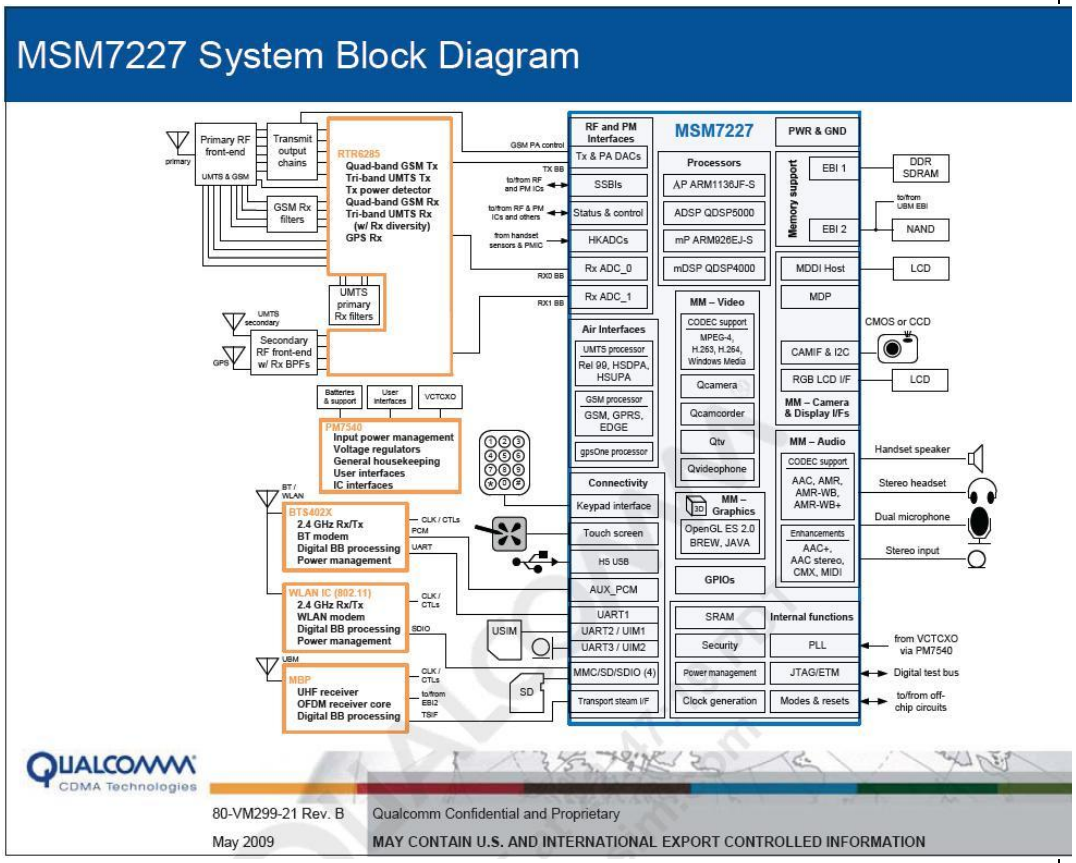

MSM7227 Chipset Training at 7.

- The Qualcomm MSM8960 microprocessor includes a Krait CPU.

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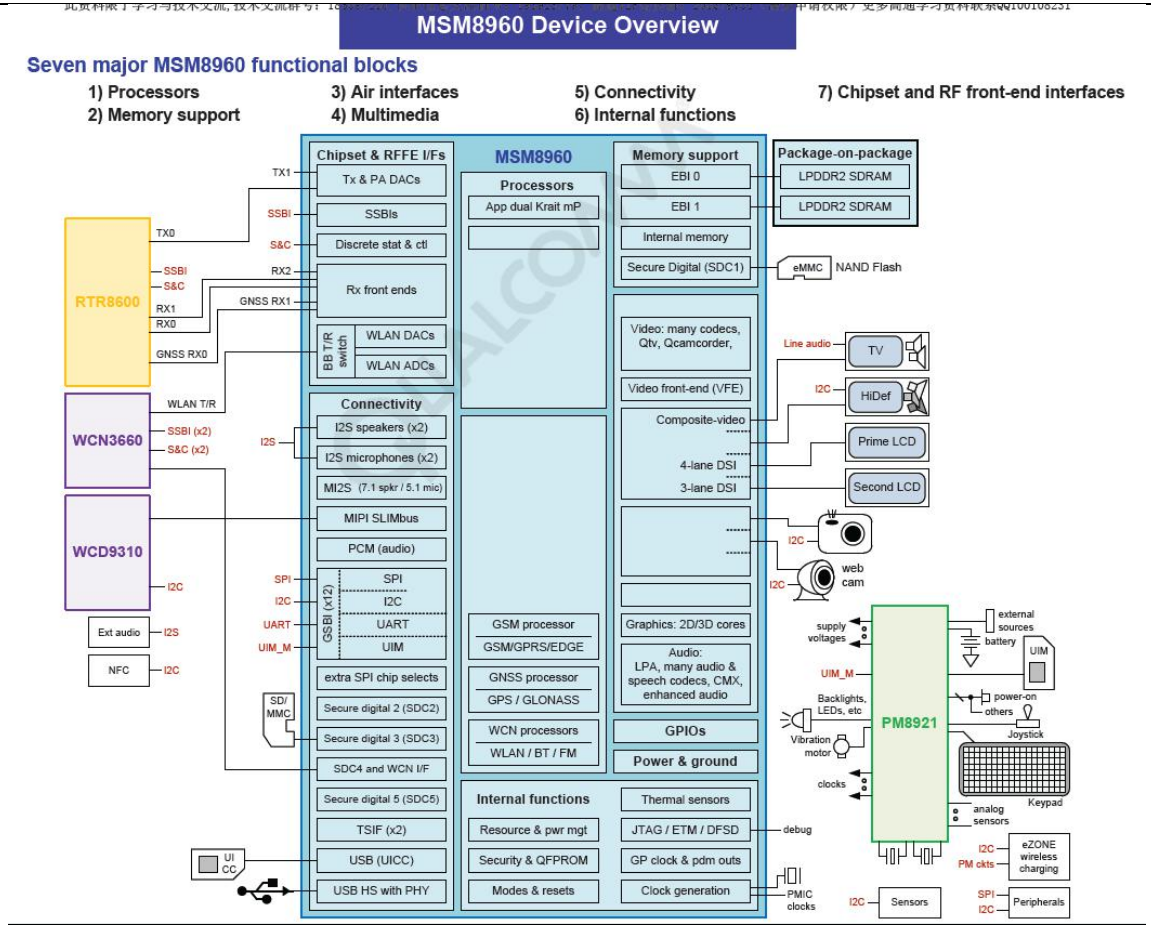

MSM8960 Chipset Training at 9.

- The Qualcomm MSM8660 microprocessor includes a Scorpion processor.

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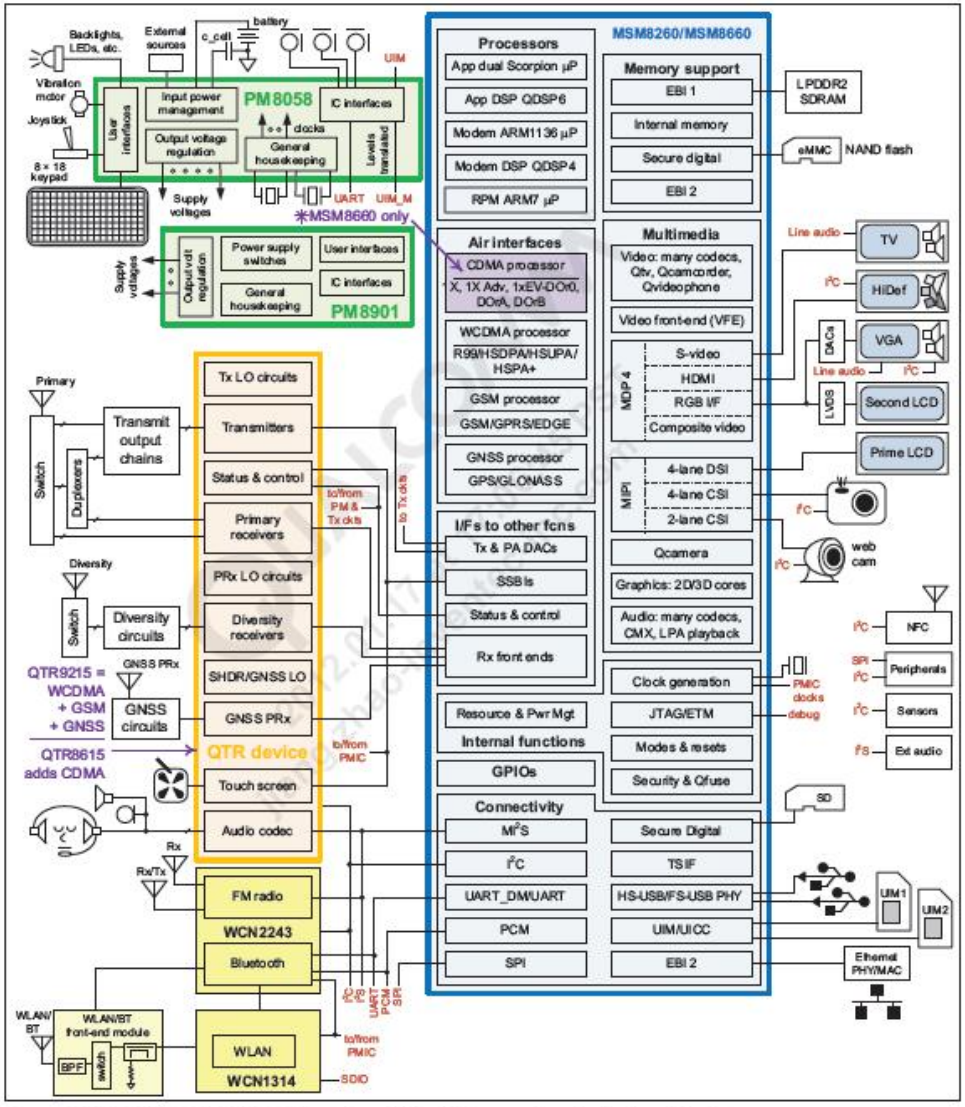


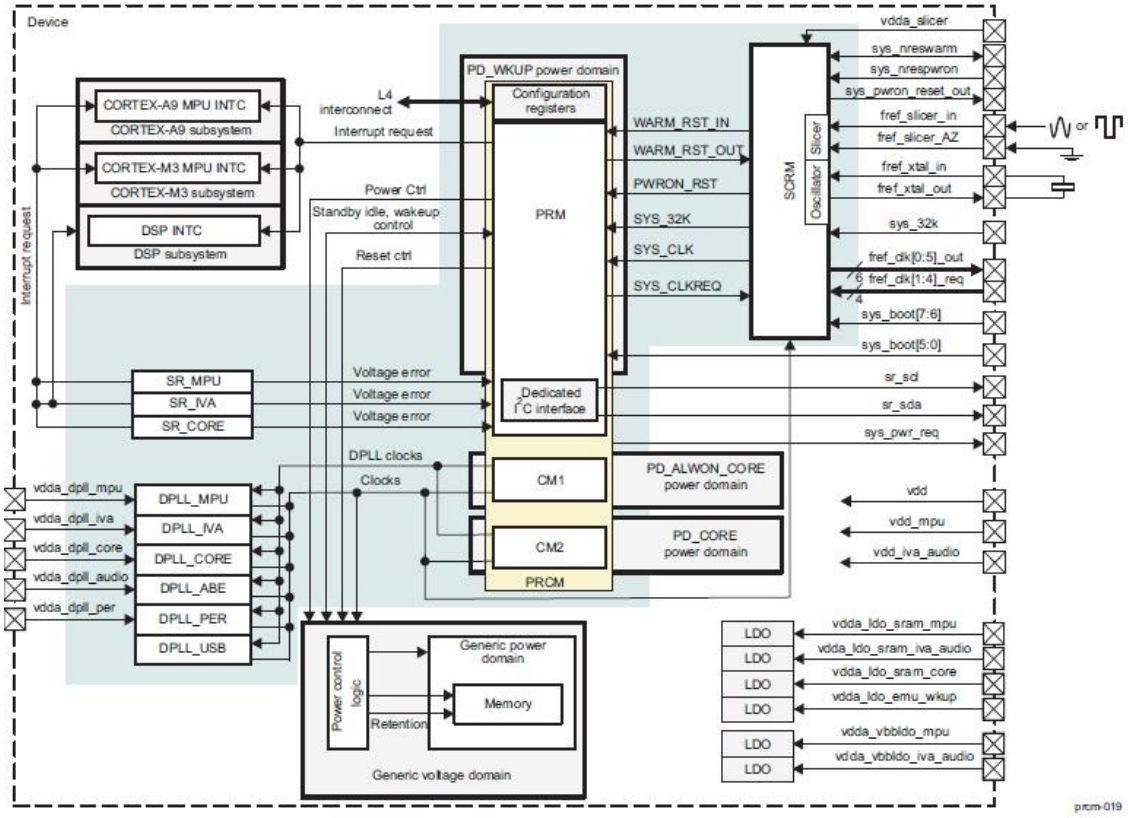
Figure 1-1 MSM8260/MSM8660 functional block diagram in a typical application

MSM8260/MSM8660 Mobile Station Modem User Guide at 16.

EXHIBIT E-1 – CLAIM CHART FOR INFRINGEMENT OF U.S. PATENT NO. 5,809,336 By Samsung

- The TI OMAP4430 includes an ARM Cortex-A9 CPU.

Figure 3-18. PMFW Overview

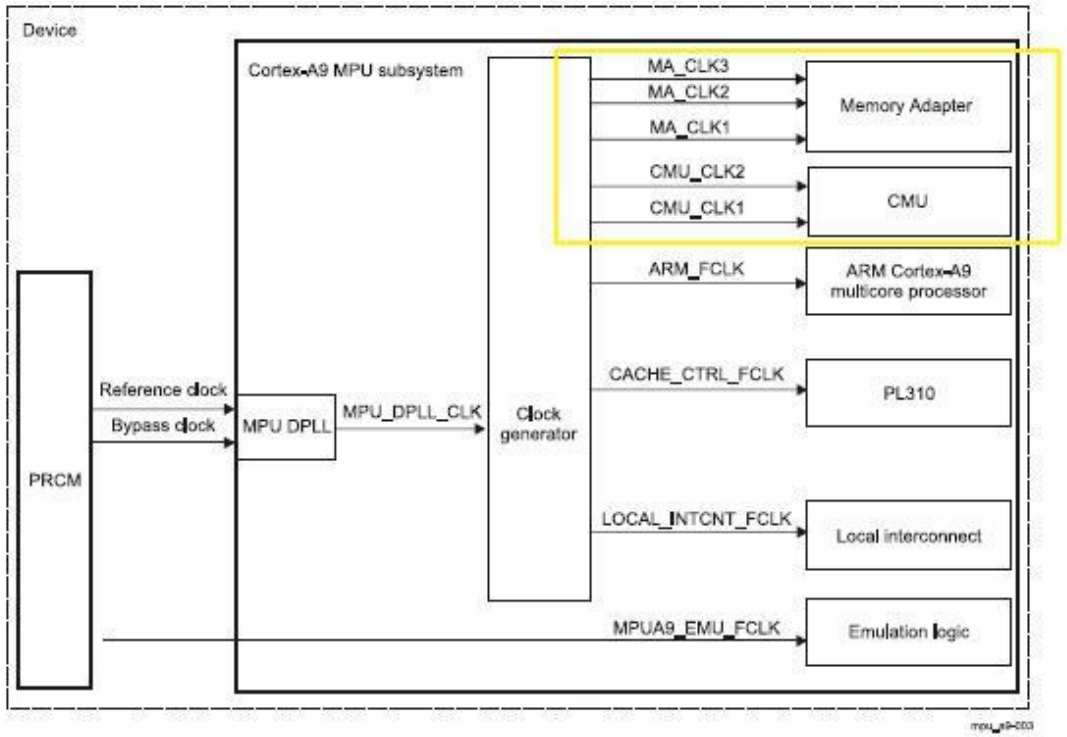


OMAP4430 Technical Reference Manual at 337.

- The TI OMAP4460 includes an ARM cortex-A9 MPU.

EXHIBIT E-1 – CLAIM CHART FOR INFRINGEMENT OF U.S. PATENT NO. 5,809,336 By Samsung

Figure 4.2. Cortex-A9 MPU Subsystem Clocking Scheme



OMAP4430/4460 TRM Addendum Technical Reference Manual at 69.

- Both the MPU and MPU_DPLL reside on the OMAP4470 chip, which is a single IC. TPLBN044564 (OMAP4470 Technical Ref Manual).

- The claimed central processing unit ARM1176JZF-S (ARM11) resides on the S3C6410 chip, which is a single IC. TPLBN002468 (S3C6410X User's Manual). The ARM CPU in the S3C6410 chip of the Accused Products operates at a processing frequency of 667MhZ. TPLBN034229 (Nook Hardware Comparison – nookDevs). The microprocessor is fabricated of multiple electronic devices (e.g., transistors) by a 65nm CMOS process. TPLBN002467

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	(S3C6410X RISC Microprocessor User's Manual) ("The S3C6410X is implemented using an advanced 65nm CMOS process."). *See* other microprocessor user guides at PDSND000001-PDSND012125; PDSND012126-PDSND048086; PDSND085767-PDSND088712.	
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,	On information and belief, each Accused Microprocessor in each Accused Product **clocks its CPU** at a clock rate, generating the signals used for timing the operation of the CPU, using PLL circuitry containing an **entire oscillator** disposed upon the integrated circuit substrate, connected to the CPU, and constructed of a second plurality of electronic devices. Each oscillator does not use any external clock to generate the signal used to clock the CPU. For example: • The **MSM8960** clocks its CPU using a PLL:	6.c

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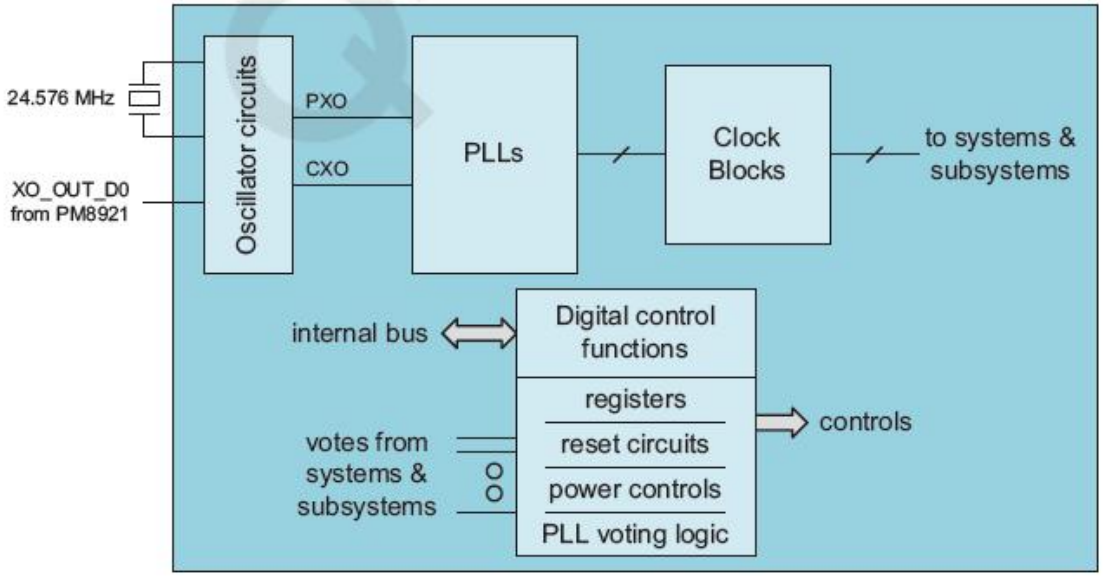

MSM8960 Chipset Schematics and Design Guidelines at 103-108.

- The **MSM8660** clocks its CPU using a PLL:

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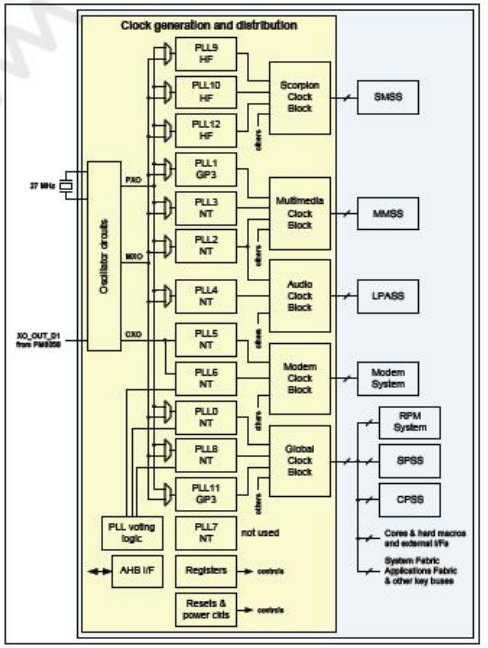
Clock Generation and Distribution

- The on-chip PLLs (PLL0 through PLL12)
  - PLL0 (reserved)
  - PLL1 (multimedia PLL0)
  - PLL2 (multimedia PLL1)
  - PLL3 (multimedia PLL2)
  - PLL4 (LPASS PLL)
  - PLL5 (modem PLL0)
  - PLL6 (modem PLL1)
  - PLL7 (unused)
  - PLL8 (peripheral PLL)
  - PLL9 (SC1 PLL0)
  - PLL10 (SC2 PLL1)
  - PLL11 (EBI1 PLL)
  - PLL12 (SC1/2 L2 PLL)

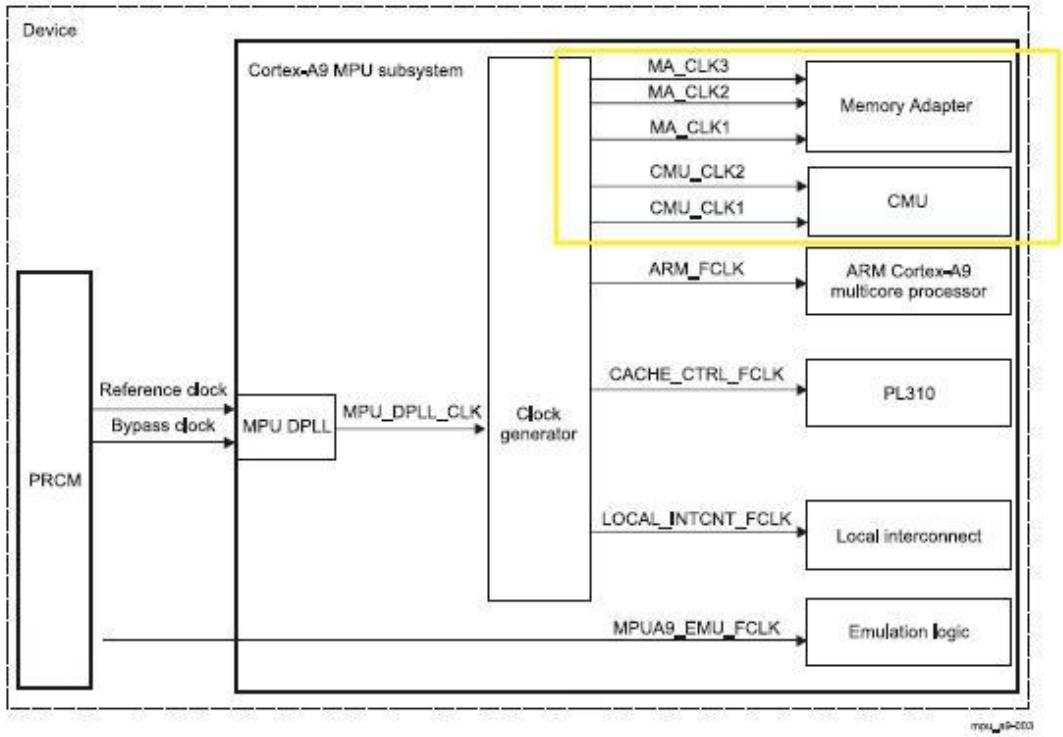


MSM8660 Mobile Station Modem Architecture and Features at 40; *see also* MSM8260/MSM8660 Mobile Station Modem User Guide at 72, 73 (Clock generation and distribution).

- The TI **OMAP4460** clocks its CPU using a PLL. The DPLL_MPU generates a clock for the MPU subsystem.

EXHIBIT E-1 – CLAIM CHART FOR INFRINGEMENT OF U.S. PATENT NO. 5,809,336 By Samsung

Figure 4.2. Cortex-A9 MPU Subsystem Clocking Scheme



OMAP4430/4460 TRM Addendum Technical Reference Manual at 69.

- The TI **OMAP4430** clocks its CPU using a PLL. The DPLL_MPU generates a clock for the MPU subsystem.

  To generate high-frequency clocks, the device supports multiple on-chip DPLLs controlled directly by the PRCM module. They are of two types, identified as type A and type B DPLLs.

  Following DPLLs belong to type A:
  - DPLL_MPU

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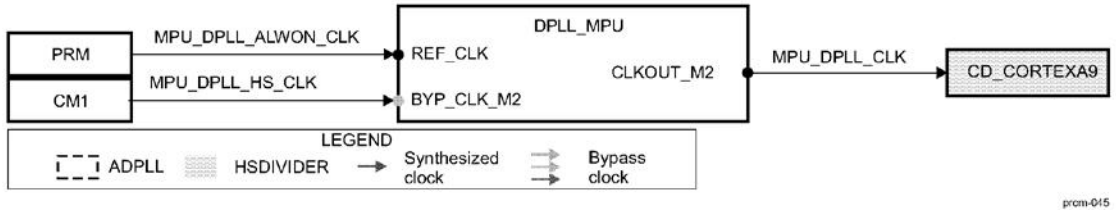
	• DPLL_IVA • DPLL_CORE • DPLL_PER • DPLL_ABE Following DPLLs belong to type B: • DPLL_USB TPLBN037652 (OMAP 4430 Tech Ref Manual). *See also* TPLBN037641-TPLBN037755 (OMAP 4430 Tech Ref Manual). DPLL_MPU supplies the source clock for the MPU subsystem, which uses this source clock to internally generate all subsystem clock signals within the MPU subsystem. **Figure 3-50. DPLL_MPU Overview**  TPLBN037679, TPLBN038343 (OMAP4430 Tech Ref Manual).	

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Table 4-2. Clocks and Resets

Module Instance	Destination Signal Name	Source Signal Name	Source	Description
		Clocks		
CORTEXA9	MPU_DPLL_CLK	MPU_DPLL_CLK	PRCM	Interface and functional clock
		Resets		
CORTEXA9	CORTEXA9_PWRON_RSTN	CORTEXA9_PWRON_RSTN	PRCM	Power-on reset for all the modules inside the MPU system power domain, nonretention
	CORTEXA9_RSTN	CORTEXA9_RSTN	PRCM	Warm reset for all the modules inside the MPU system power domain, nonretention

4.2.1 Clock Distribution

The Cortex-A9 MPU clock generator is fed by the MPU DPLL, which can be gated off by the global power, reset, and clock management (PRCM) module when system power domain is in a low-power state. There is a global clock gating for each CPU. Due to the MPU DPLL, the Cortex-A9 MPU subsystem is asynchronous from the rest of the device.

The clock generator generates the following clocks from the MPU DPLL output clock:

- ARM_FCLK – ARM Cortex-A9 MPCore functional clock
- LOCAL_INTCNT_FCLK – Local interconnect functional clock
- CACHE_CTRL_FCLK – PL310 cache controller functional clock

TPLBN038343 (OMAP4430 Tech Ref Manual).

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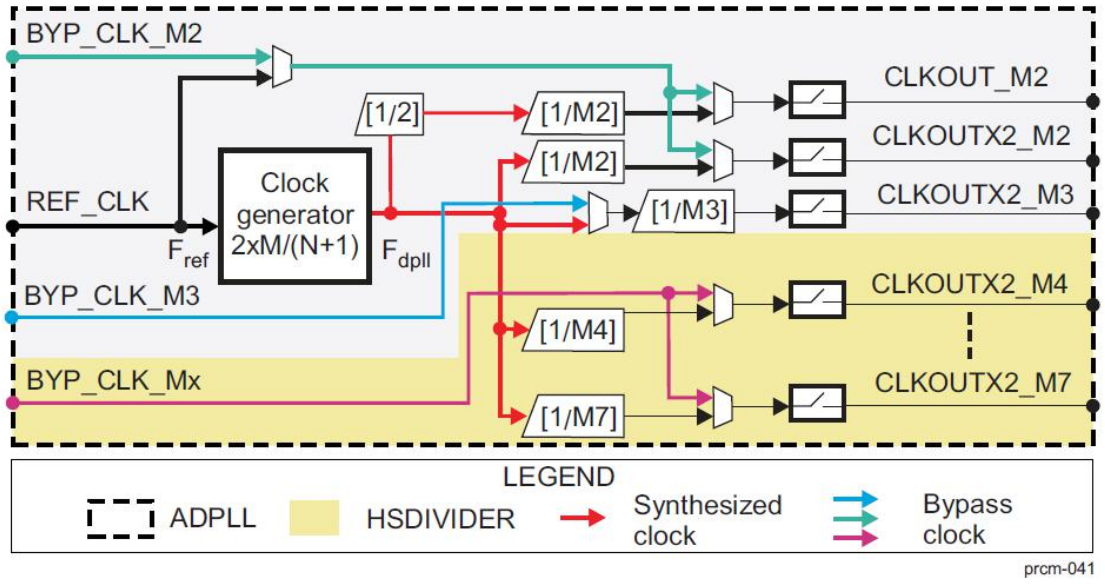
Figure 3-40. Generic DPLL Functional Diagram



TPLBN037653 (OMAP4430 Tech Ref Manual).

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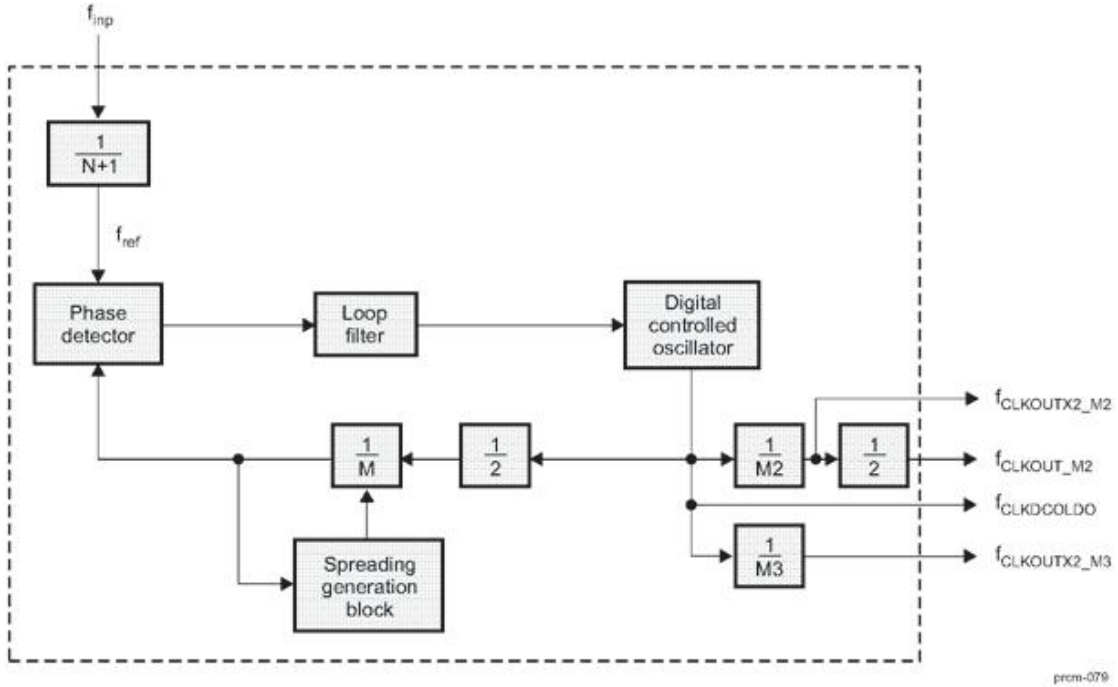
Figure 3-41. DPLL With SSC Reduction Feature



TPLBN037657 (OMAP4430 Tech Ref Manual).

- The TI **OMAP4470** clocks its CPU using a PLL:

  The applicative subsystem integrates nine DPLLs and four DLLs. The PRM and CM drive six of them, while the display subsystem controls three other DPLLs (DSI1_1 DPLL, DS11_2 DPLL, and HDMI DPLL).

  The six main DPLLs are:

  - DPLL1 (MPU)
  - DPLL2 (IVA)

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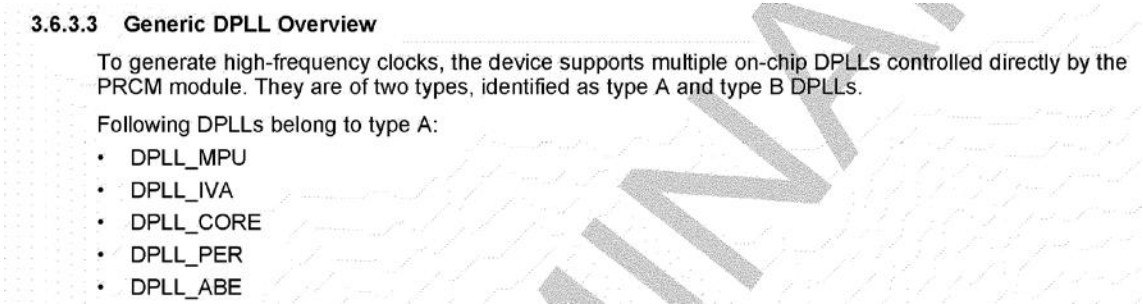
	• DPLL3 (CORE) • DPLL4 (PER) • DPLLS (ABE) • DPLL6 (USB) . . . Of the nine DPLLs embedded in the OMAP4470 device, the DSI1_1 DPLL, DSI1_2 DPLL, and HDMI DPLL are controlled directly by the display subsystem. TPLBN043211 (OMAP 4470 Data Manual); *See also* TPLBN043854-TPLBN043971 (OMAP4470 Technical Ref Manual). The DPLL_MPU generates a clock for the MPU subsystem.  3.6.3.3 Generic DPLL Overview To generate high-frequency clocks, the device supports multiple on-chip DPLLs controlled directly by the PRCM module. They are of two types, identified as type A and type B DPLLs. Following DPLLs belong to type A: • DPLL_MPU • DPLL_IVA • DPLL_CORE • DPLL_PER • DPLL_ABE TPLBN043865 (OMAP4470 Technical Ref Manual). DPLL_MPU supplies the source clock for the MPU subsystem, which uses this source clock to internally generate all subsystem clock signals within the MPU subsystem.	

EXHIBIT E-1 – CLAIM CHART FOR INFRINGEMENT OF U.S. PATENT NO. 5,809,336 By Samsung

Table 4-2. Clocks and Resets

Module Instance	Destination Signal Name	Source Signal Name	Source	Description
		Clocks		
CORTEXA9	MPU_DPLL_CLK	MPU_DPLL_CLK	PRCM	Interface and functional clock
		Resets		
CORTEXA9	CORTEXA9_PWRON_RSTN	CORTEXA9_PWRON_RSTN	PRCM	Power-on reset (POR) for all the modules inside the MPU system power domain; nonretention
	CORTEXA9_RSTN	CORTEXA9_RSTN	PRCM	Warm reset for all the modules inside the MPU system power domain; nonretention

TPLBN044564 (OMAP4470 Technical Ref Manual).

4.2.1 Clock Distribution

The Cortex-A9 MPU clock generator is fed by the MPU digital phase-locked loop (DPLL), which can be gated off by the global power, reset, and clock management (PRCM) module when system power domain is in a low-power state. There is a global clock gating for each CPU. Because of the MPU DPLL, the Cortex-A9 MPU subsystem is asynchronous from the rest of the device.

The clock generator generates the following clocks from the MPU DPLL output clock:

- ARM_FCLK: ARM Cortex-A9 MPCore functional clock
- LOCAL_INTCNT_FCLK: Local interconnect functional clock
- CACHE_CTRL_FCLK: PL310 cache controller functional clock
- CMU_CLK1 and CMU_CLK2: CMU functional clocks
- MA_CLK1, MA_CLK2 and MA_CLK3: MA functional clocks

TPLBN044564 (OMAP4470 Technical Ref Manual).

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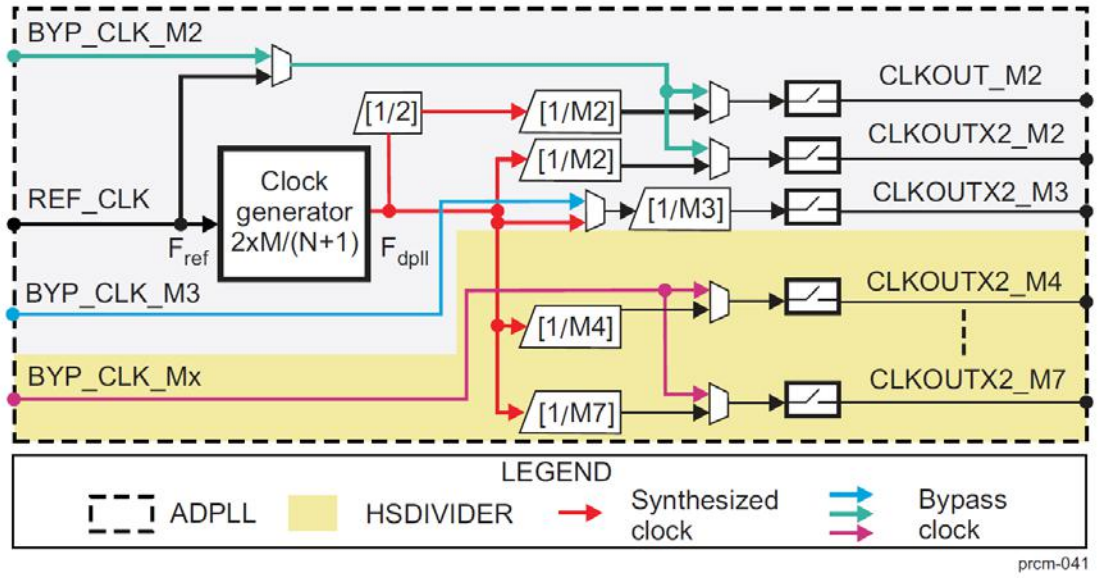
Figure 3-40. Generic DPLL Functional Diagram



TPLBN043866 (OMAP4470 Technical Ref Manual).

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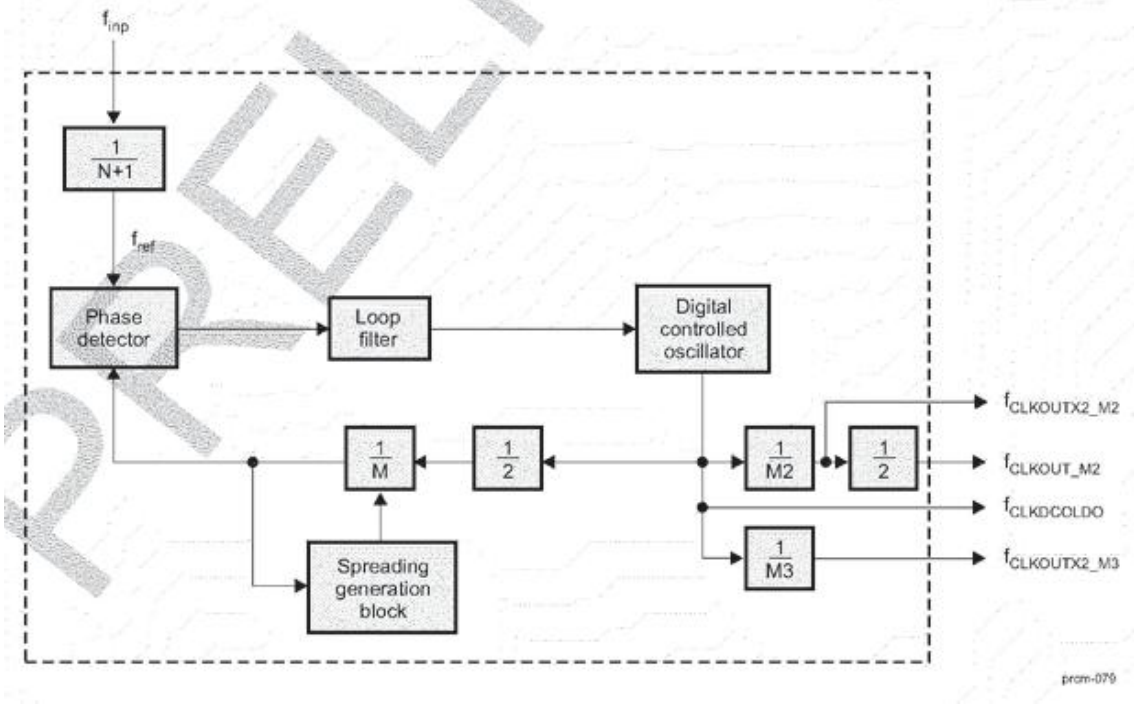
Figure 3-41. DPLL With SSC Reduction Feature



TPLBN043870 (OMAP4470 Technical Ref Manual).

- The **S3C6410X** Processor clocks its CPU using a ring oscillator in PLL circuitry, located on a single integrated circuit with the CPU:

  System operating clock generation
  − Three on-chip PLLs, APLL, MPLL & EPLL
  − APLL generates an independent ARM operating clock
  − MPLL generates the system reference clock
  − EPLL generates clocks for peripheral IPs

TPLBN002480 (S3C6410X RISC Microprocessor User's Manual).

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Figure 3-4 illustrates the clock generation logic. S3C6410X has three PLLs which are APLL for ARM operating clock, MPLL for main operating clock, and EPLL for special purpose. The operating clocks are divided into three groups. The first thing is ARM clock, which is generated from APLL. MPLL generates the main system clocks, which are used for operating AXI, AHB, and APB bus operation. The last group is generated from EPLL. Mainly, the generated clocks are used for peripheral IPs, i.e., UART, IIS, IIC, and etc.

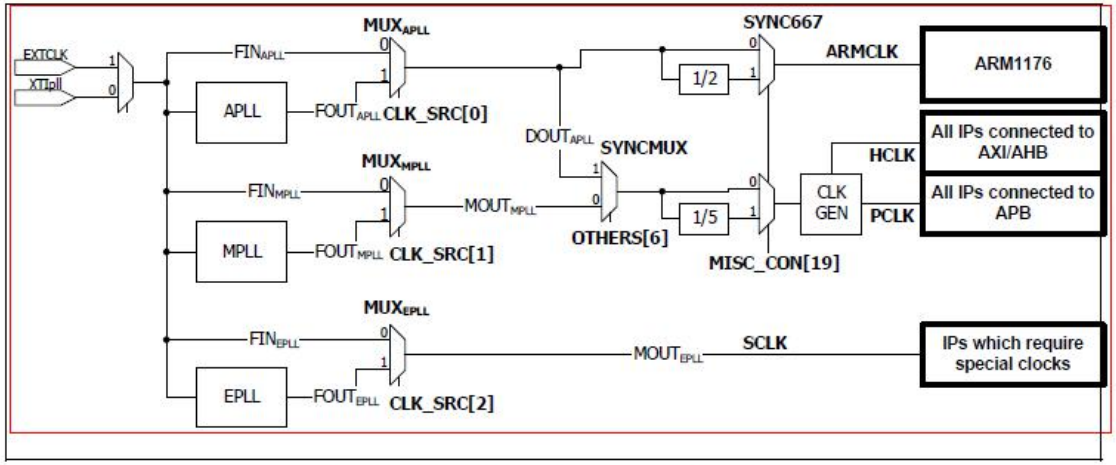

Figure 3-4. Clock generation from PLL outputs

TPLBN002531 (S3C6410X RISC Microprocessor User's Manual).

See other microprocessor user guides at PDSND000001-PDSND012125; PDSND012126-PDSND048086; PDSND085767-PDSND088712; *see also* http://en.wikipedia.org/wiki/Phase-locked_loop.

The presence of a PLL indicates the presence of a voltage or current controlled oscillator, which itself will include the claimed oscillator. The claimed oscillator is disposed upon the integrated circuit substrate, connected to the central processing unit,

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	and is clocking the central processing unit. The oscillator is constructed of a second plurality of electronic devices.	
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate,	In each Accused Microprocessor of each Accused Product, because the central processing unit and the entire oscillator reside on the same integrated circuit, they were constructed using the same process technology and will have corresponding manufacturing variations. One of ordinary skill in the art would understand this with respect to the Accused Products based on generally accepted principles relating to semiconductor ICs. *Design of High-Performance Microprocessor Circuits* pp. 98, 101 (Anatha Chandrakasan et al. eds., IEEE Press, 2001) [*Models of Process Variations in Device and Interconnect* (Duane Boning and Sani Nassif)] (TPL853_02927444 – TPL853_02927464). **6.1 INTRODUCTION: SOURCES OF VARIATION** Variation is the deviation from intended or designed values for a structure or circuit parameter of concern. The electrical performance of microprocessors or other integrated circuits are impacted by two sources of variation. *Environmental factors* arise during the operation of a circuit, and include variations in power supply, switching activity, and temperature of the chip or across the chip. *Physical factors* during manufacture result in structural device and interconnect variations that are essentially permanent. These variations arise due to processing and masking limitations, and result in random or spatially varying deviations from designed parameter values. In this chapter we focus on *parametric variation* due to continuously varying structural or electrical parameters, as these can significantly impact not only yield but also performance in high-speed microprocessor and other digital circuits. Such parametric variation is becoming a larger concern, as variation and margins for device and interconnect do not appear to be scaling at the same rate. Figure 6.1	6.d

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6.2 Overview: Statistical Descriptions 101

While a simplified distribution is often assumed to capture the variance die-to-die, it is often possible and helpful to characterize and model systematic trends across the wafer. For example, chip speed may depend on some parameter that varies in a systematic "bowl" fashion across the wafer; accurate speed binning or yield analysis and improvement may depend on understanding such patterns from one die to the next. In typical circuit design, die-to-die variations are the simplest to analyze; a small number of situations may be analyzed in which all device or interconnect parameters on the chip are mean shifted together up or down by some amount (e.g., 2–3σ).

TI confirms that processing frequency, the speed at which the CPU operates, and the clock rate of the oscillator vary in the same way, increasing and decreasing proportionally, as a function of parameter variation in one or more fabrication or operational parameters, such as temperature or voltage, associated with the integrated circuit substrate:

> Figure 1 below gives a general view of how performance and power dissipation vary with process, temperature and voltage. . . .

	Performance	Power Dissipation
Process	Linear	Linear
Temperature	1/Logarithmic	Exponential
Voltage	Exponential	Exponential

Figure 1. Overview of key dependencies.

> . . . ICs can be manufactured in a variety of silicon processes. Processes in use today include 180-nm, 130-nm, and 90-nm processes. The performance of an IC depends on the characteristics of the underlying process. When manufacturers design an IC, they target the nominal process characteristics. However, variations in the process generate devices that are sometimes weaker ("colder")

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	than desired or sometimes stronger ("hotter") than a nominal device. Hot devices can provide higher levels of performance than cold or nominal devices, and vice-versa. A typical relationship is shown in Figure 2 on the following page. The performance documented in a data sheet takes into account the worse-case process variation. In other words, the maximum operational frequency given in the data sheet is determined by the weakest, cold devices. As illustrated in Figure 2, these weak devices represent only a fraction of the devices shipped. Therefore, the maximum performance of most devices exceeds the data sheet specification. Similarly, the data sheet provides an operational temperature range, say –40°C–105°C. The documented performance is for the worst performance across the temperature limits. Figure 2 shows how the operational frequency of a device tends to increase with decreasing temperatures. A given device can have a significantly higher performance level if it is run below maximum temperature specification, e.g., at 75°C instead of 105°C.	

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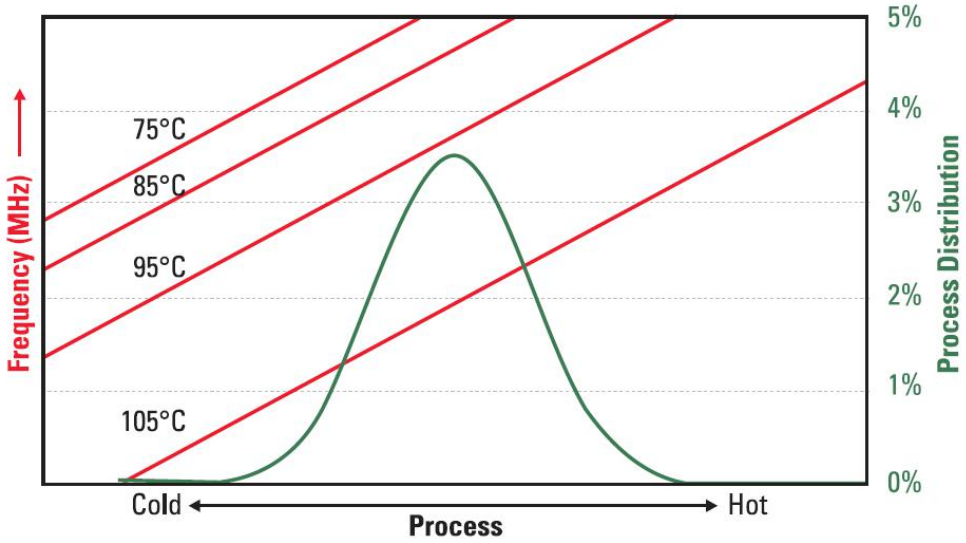

Figure 2. Dependency on process variation and temperature.

There is a similar relationship with respect to voltage. A device provides more performance as the voltage increases. In Figure 3, the minimum voltage Va determines the performance listed in the specification. At higher voltages (Vb, Vc, Vd, respectively), the performance tends to improve.

All of these trends provide the basis for the final specification provided to a customer. In order to provide some margin, each parameter is guard banded to ensure the specification is met under all voltage, frequency, temperature, and process conditions, for a particular number of power-on hours. If a device does not meet the required performance at the limit of the specification plus guard band, the device is discarded.

From a batch of devices that meet the specification, most are likely able to outperform the data sheet performance limits.

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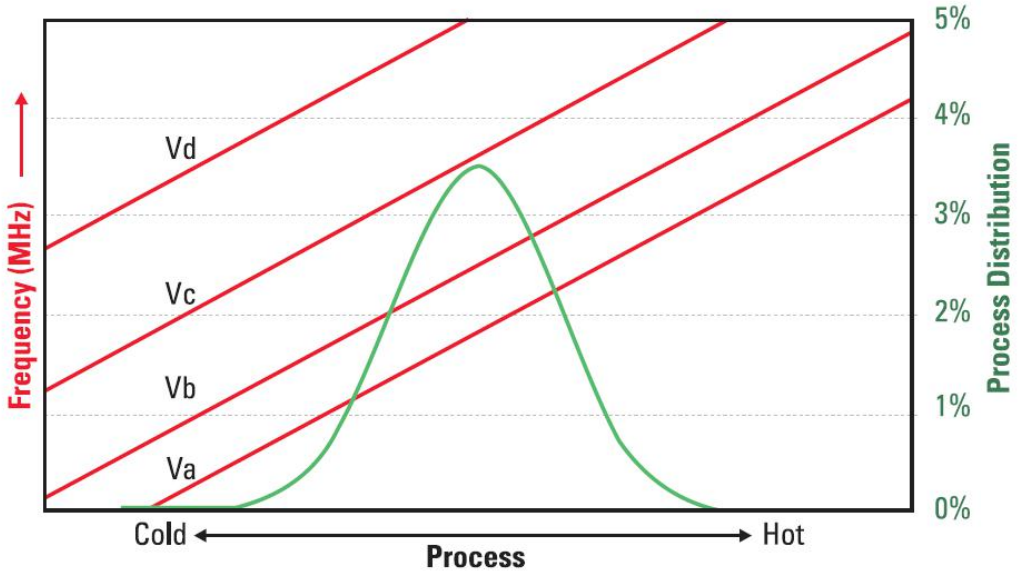

Figure 3. Dependency on voltage.

. . . So, what does all of this mean to the engineer designing the system? It means:

• An application that is performance-centric can find additional performance by lowering the temperature, or by increasing the voltage, or both. . . .

• Most devices have higher performance and lower power dissipation than the data sheet suggests. . . .

By understanding these details behind the data sheet specification, you can create the product you need—even when the data sheet says it is impossible.

TPLBN033411-15 (Frantz, Mai, and Garcia, *Push Performance and Power Beyond the Data Sheet*, Texas Instruments White Paper (July 2007)).

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On information and belief, the OMAP processors employ a mechanism called "Dynamic Voltage Frequency Scaling," or "DVFS," whereby the ring oscillator and the CPU run at various operating points or "OPP." Making use of DVFS allows the chip to be run at a slower frequency to conserve power and battery life when faster processing is not required. Sometimes you actually want to change the frequency of the signal output from the ring oscillator and that the chip may run at different speeds depending on the needs of the system. The only way to vary the clock speed output from the ring oscillator is to vary the input current. Even when purposeful variation of the ring oscillator output frequency is not desired, the output frequency will still vary by a few percentage points.

Further, the OMAP processors and first clocks vary together as a result of process conditions. TI employs binning to separate chips with different process capabilities that result from process variations.

Table 4-15. DPLL1 Clock Frequency Ranges

Clock Signal	Description		Max	Unit
ARM_CLK	DPLL1 output clock.	OPP6(1)	720	MHz
		OPP5	600	MHz
		OPP4	550	MHz
		OPP3	500	MHz
		OPP2	250	MHz
		OPP1(2)	125	MHz

(1) OPP6 frequency range is only supported on high-speed grade OMAP3530/25 devices.
(2) Cannot boot in OPP1. If OPP1 is desired, boot in higher OPP then switch to OPP1.

TPLBN037143 (indicating "speed binning"). *See also* TPL853_02993475-84 (ISSCC 2004 / Session 26 / *Optical and Fast IO 26.10*) (CX-0170); TPL853_02993485-96 (CX-0171).

Similarly, on information and belief, Samsung's own documents will show that Samsung is concerned with PVT variation in the design and operation of its chips because CPU processing frequency and the clock rate of the oscillator in Samsung microprocessors also vary in the same way, increasing and decreasing proportionally, as a function of parameter variation in one or more fabrication or operational parameters,

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	such as temperature or voltage, associated with the integrated circuit substrate.	
thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	The central processing unit and the oscillator in each Accused Microprocessor of each Accused Product are constructed on the same integrated circuit using the same process technology. Accordingly, the processing frequency of the central processing unit is enabled to track the clock rate, increasing and decreasing proportionally, in response to said parameter variation, including variation in fabrication, operating voltage or temperature of the integrated circuit. One of ordinary skill in the art would understand this with respect to the Accused Products based on generally accepted principles relating to semiconductor ICs. *See Design of High-Performance Microprocessor Circuits* p. 98 (Anatha Chandrakasan et al. eds., IEEE Press, 2001) [*Models of Process Variations in Device and Interconnect* (Duane Boning and Sani Nassif)] (TPL853_02927444 – TPL853_02927464). **6.1 INTRODUCTION: SOURCES OF VARIATION** Variation is the deviation from intended or designed values for a structure or circuit parameter of concern. The electrical performance of microprocessors or other integrated circuits are impacted by two sources of variation. *Environmental factors* arise during the operation of a circuit, and include variations in power supply, switching activity, and temperature of the chip or across the chip. *Physical factors* during manufacture result in structural device and interconnect variations that are essentially permanent. These variations arise due to processing and masking limitations, and result in random or spatially varying deviations from designed parameter values. In this chapter we focus on *parametric variation* due to continuously varying structural or electrical parameters, as these can significantly impact not only yield but also performance in high-speed microprocessor and other digital circuits.	6.e
an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	On information and belief, each Accused Microprocessor in each Accused Product includes on-chip input/output interfaces, which are circuits having logic for input/output communications, located on the same semiconductor substrate as the CPU. The input/output interfaces are connected between the central processor unit and an off-chip external memory bus, which is a group of conductors coupled between the I/O interface and an external storage device, as well as other peripherals, for facilitating exchanging	6.f

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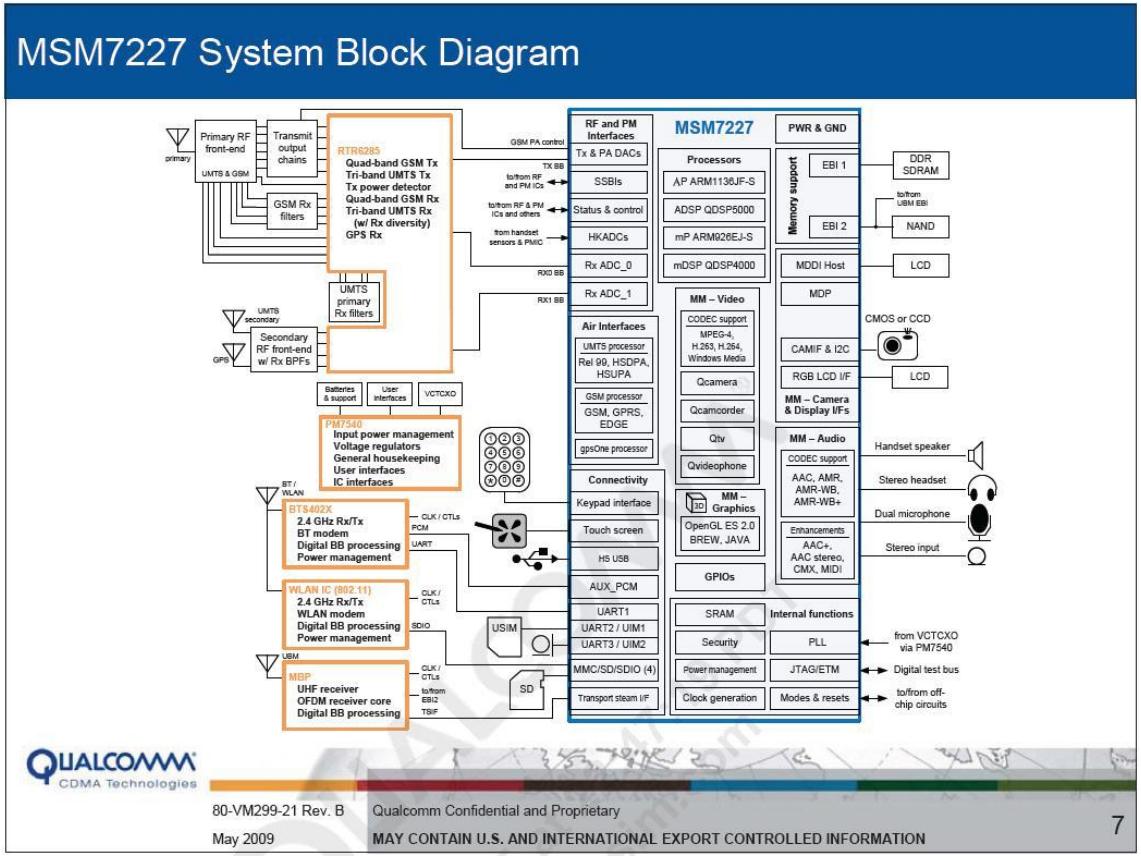
coupling control signals, addresses and data with said central processing unit.

On information and belief, each Accused Microprocessor in each Accused Product includes on-chip USB input/output interfaces connected between the CPU and an off-chip external memory bus, as well as other peripherals.

For example,

- The **MSM7227** includes I/O interfaces:



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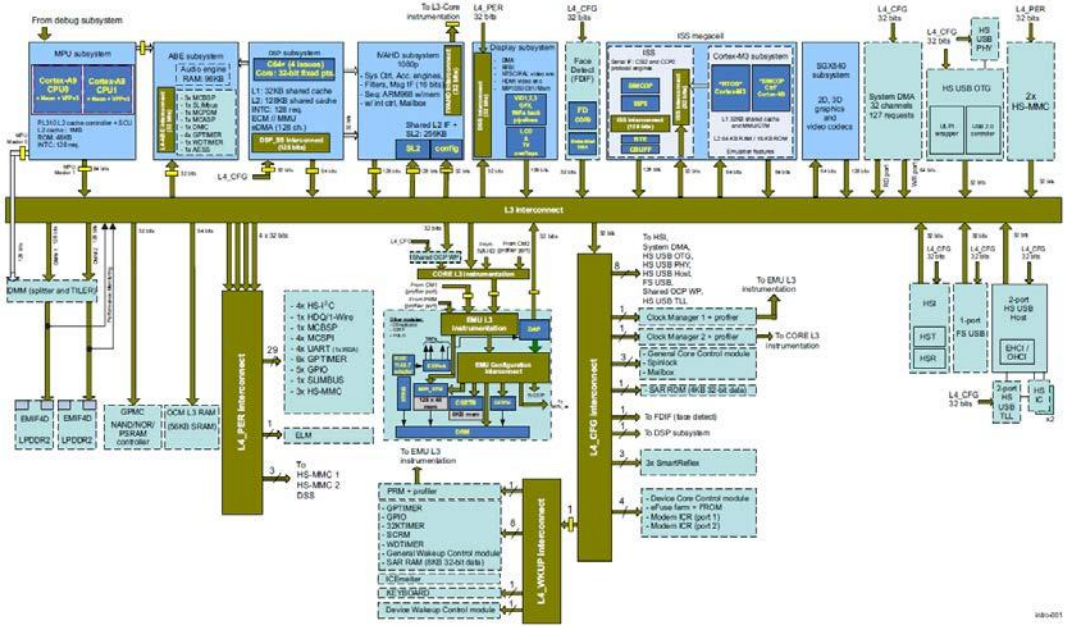
MSM7227 Chipset Training at 7.

- *See supra* **MSM8960** Chipset Training at 9, and **MSM8260/MSM8660** Mobile Station Modem User Guide at 16;

- The **OMAP4430** includes I/O interfaces:

Figure 1-2. OMAP4430 Block Diagram



TPLBN037538 (OMAP4430 Tech Ref Manual).

- **S3C6410**:

The S3C6410 input/output interfaces are connected to exchange coupling control signals, addresses and data with the central processing unit via a peripheral bus system that uses an Advance High-performance bus (AHB) and advance peripheral bus (APB).

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	See TPLBN002468 (Figure 1-1. S3C6410 Block Diagram); TPLBN002467 ("The 64/32-bit internal bus architecture is composed of AXI, AHB and APB buses"). The input/output interfaces of the S3C6410 are connected to on-board modules such as USB, via off-chip external memory bus. *See* TPLBN002468 (Figure 1-1. S3C6410 Block Diagram). Data transfer from an input/output interface to a module is performed by first storing the data in a memory buffer associated with the input/output interface. After proper handshaking, the data is sent to the module via an external memory bus. The module receives the data via the external memory bus and stores it temporarily in a memory buffer associated with the module for further processing. Data transfer from a module to an input/output interface occurs similarly in the reverse direction. For example, the on-chip USB (Universal Serial Bus) interface connects between the CPU, via the AXI bus and an off-chip external memory bus, and the on-board USB module, for facilitating exchanging coupling control signals, addresses and data with the CPU. *See*, *generally*, TPLBN003282-3358 (S3C6410X User's Manual USB sections).	

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	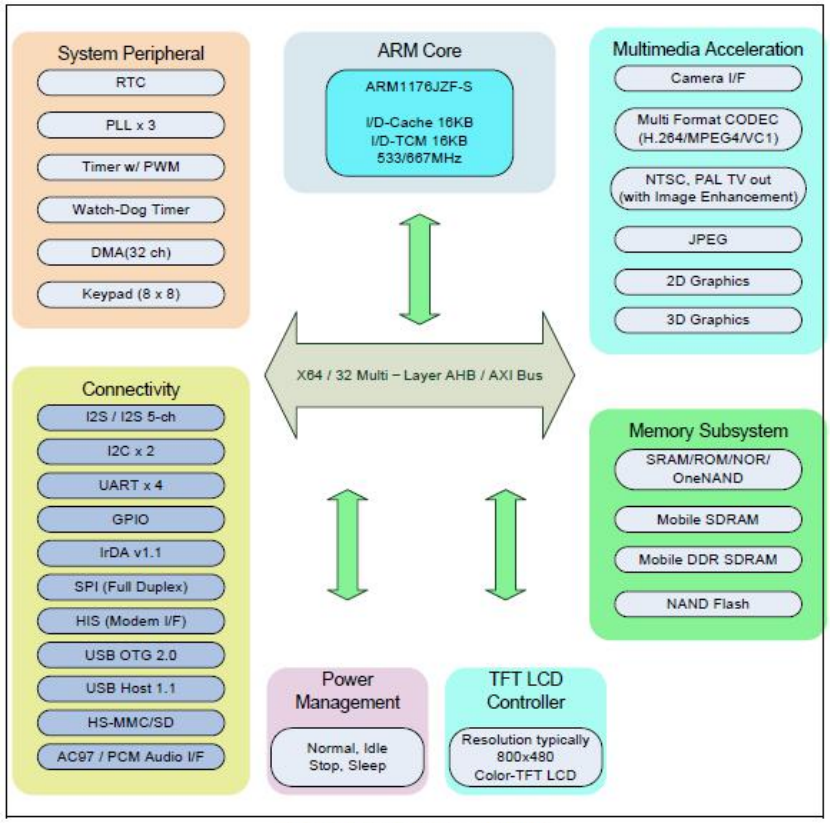 Figure 1-1 S3C6410X Block Diagram TPLBN002468 (Figure 1-1. S3C6410 Block Diagram). *See* other microprocessor user guides at PDSND000001-PDSND012125; PDSND012126-PDSND048086; PDSND085767-PDSND088712.	
an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency	On information and belief, each Accused Product includes one or more off-chip external clocks, which are not on the integrated circuit substrate, independent of the oscillator, connected to one or more of the input/output interfaces. The off-chip external clocks operate at a frequency independent of the clock frequency of the oscillator: a change in	6.g

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independent of a clock frequency of said oscillator and	the frequency of either the external clock or oscillator does not affect the frequency of the other. When an Accused Product receives data via its USB connection to a PC or Mac, it receives a clock signal encoded in that data. This clock signal is independently generated on the PC or Mac and is received on the Accused Product's USB data pins. The clock signal sent by the PC or Mac is recovered in the USB PHY (a physical implementation of the USB I/O interface), and is used to clock the data transfer in the Accused Product. *See* http://en.wikipedia.org/wiki/USB*; see also* USB specification at http://www.usb.org/developers/docs/. For example, in the SGH-Z310 phone, the MSM6275 USB interface is connected with off-chip clock:	

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	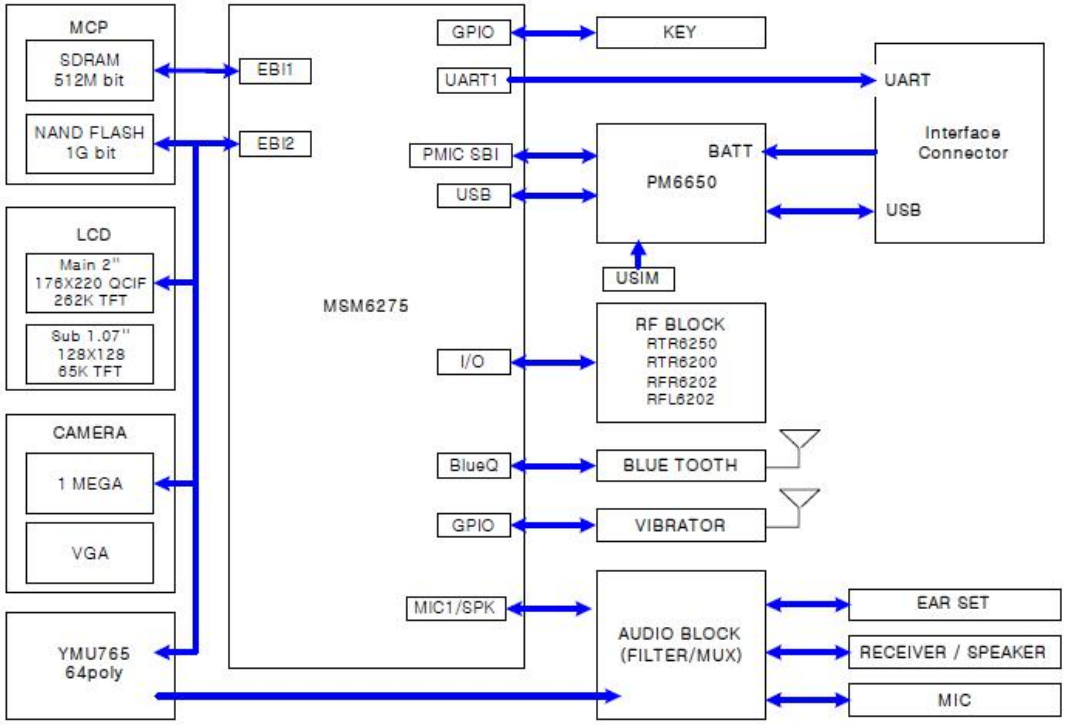 SGH-Z310 Service Manual at 7-2. *See* other service manuals at PDSND085415-PDSND085766, PDSND088713-PDSND108874, PDSND109662-PDSND110077. On information and belief, the schematics of the Accused Products will also show similar pins and operation, for USB, UART, and other interfaces.	
wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.	In each Accused Product, the off-chip external clock generates a clock signal that originates from a source other than the oscillator. Each external second clock originates from an external device, separate from the Accused Product, and thus is both independent from and **asynchronous to** the CPU clock. Therefore, the timing control of the central processing unit operates	6.h

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	independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them. For example, the clock signals encoded in the data stream received by each Accused Product from PC and Mac peripherals via USB originate from the peripherals. The source of these clock signals is therefore independent and asynchronous from any clock source in the Accused Product. In its user manuals and publications, Samsung instructs its users regarding how to connect each Accused Product to PC or Mac peripherals in order to transfer data and receive system updates. For example, the HT-C5200 Home Theatre System Service Manual at 4-25 instructs users to update the system via USB storage. The CLP-300 Printer User's Guide at 2-6 instructs users to connect the printer to a computer via USB for printing. *See* PDSND085415- PDSND085766, PDSND088713-PDSND108874, PDSND109662-PDSND110077 for service manuals and PDSND095934-PDSND108874 for user manuals.	

Claim 7	
7. A microprocessor system of claim 6	*See* Claim Element 6.a.
wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	*See* Claim Elements 6.d, 6.e.

Claim 9	
9. A microprocessor system of claim 6	*See* Claim Element 6.a.
wherein said oscillator comprises a ring	*See* Claim Element 6.c.

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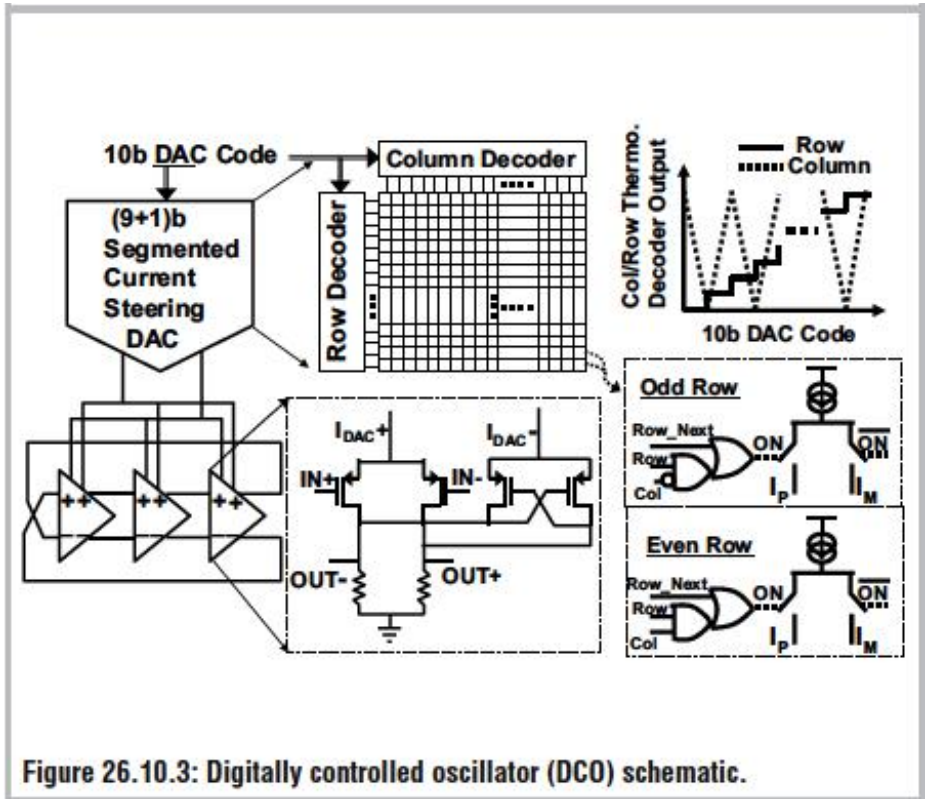
oscillator.	On information and belief, in each Accused Microprocessor, the PLL clocking the CPU includes either a Voltage Controlled Oscillator (VCO) or a Current Controlled Oscillator (ICO), which is a **ring oscillator**, having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment. *See* http://en.wikipedia.org/wiki/Ring_oscillator. For example, generally in **TI microprocessors**, PLLs have voltage-controlled oscillators, which are circuits capable of maintaining an alternating output. TI has published papers regarding its DPLLs confirming the use of ring oscillators.  Figure 26.10.3: Digitally controlled oscillator (DCO) schematic. TPL853_02993475-84, Fig. 26.10.3 (ISSCC 2004 / Session 26 / *Optical and Fast IO 26.10*) (CX-0170).

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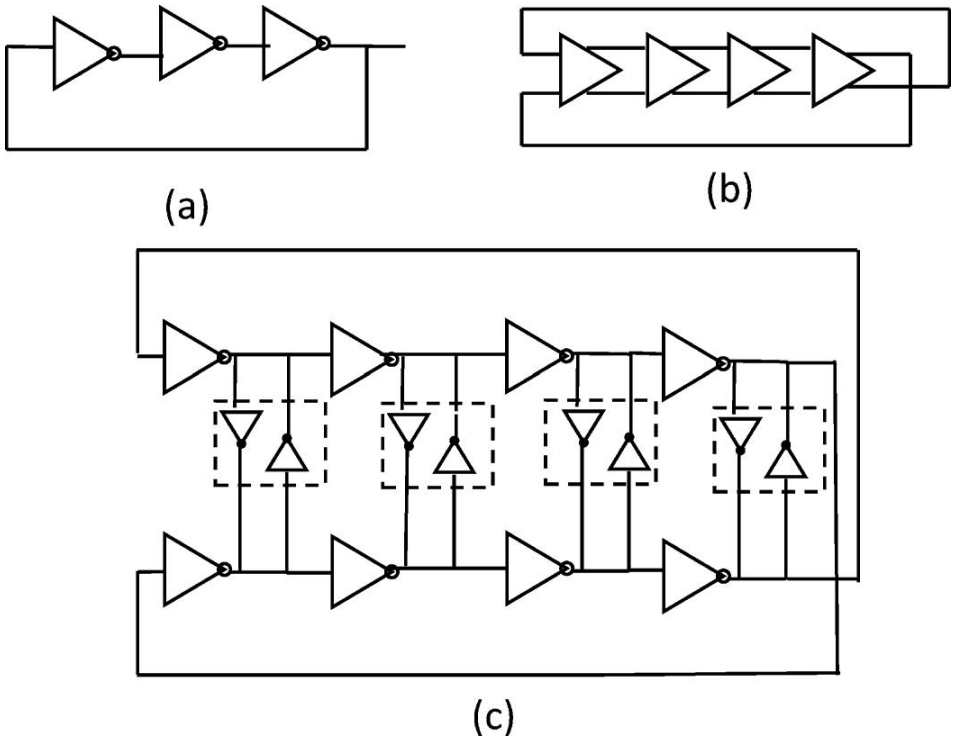

TPL853_02993485-96, Fig. 3 (CX-0171). "Figs. 17 and 18 show the die micrographs of two Digital PLLs implemented in 65 nm and 45 nm CMOS. . . . Both use a simple three stage ring oscillator shown in Fig. 3(a)." TPL853_02993494.

The TI OMAP4 family of processors is also implemented in 45 nm CMOS technology: "The OMAP4470 high-performance multimedia application device is based on enhanced OMAP architecture and uses 45-nm technology." TPLBN043746 (OMAP4470 Technical Ref Manual). *See also* TPLBN037535 (OMAP4430 Tech Ref Manual).

Furthermore, on information and belief, each of the OMAP3 and OMAP4 chips at issue contains a DPLL that outputs a clock signal for the MPU. Within each of these DPLLs is either a single-ended or differential ring oscillator. This component of the PLL generates an oscillation (*i.e.*, a clock signal). The ring oscillator is able to

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	produce an oscillation due to the presence of an odd number of inversions arranged in a loop. *See also HTC Corporation v. Technology Properties Limited*, 08-cv-00882-PSG, Trial Tr. 341:13-347:1, 333:20-374:16 (Haroun testimony). On information and belief, the only input to the ring oscillators in the OMAP3 and OMAP4 chips is a current. In addition, while the bias DAC ("digital to analog converter") in the DPLL may receive a digital word, it does not pass this control signal on to the ring oscillator. Indeed, without the bias component of the PLL, the ring oscillators in the OMAP chips would still output an oscillation. Barring the application of dividers to the ring oscillator's output, the only way to change the frequency of the ring oscillator is to change the input current. In other words, the ring oscillator will always generate a clock signal as long as a current is applied to it. In another example, in **Samsung Microprocessors:** Three PLLs within S3C6410X, APLL, MPLL, and EPLL, synchronizes an output signal with a reference input clock in operating frequency and phase. In this application, it includes the following basic blocks as illustrated in Figure 3-3. The Voltage Controlled Oscillator (VCO) generates the output frequency proportional to input DC voltage. The pre-divider divides the input frequency (FIN) by P. The main divider divides the VCO output frequency by M, which is input to Phase Frequency Detector (PFD). The post scaler divides the VCO output frequency by S. The phase difference detector calculates the phase difference and the charge pump increases / decreases the output voltage. The output clock frequencies of each PLL can be calculated.

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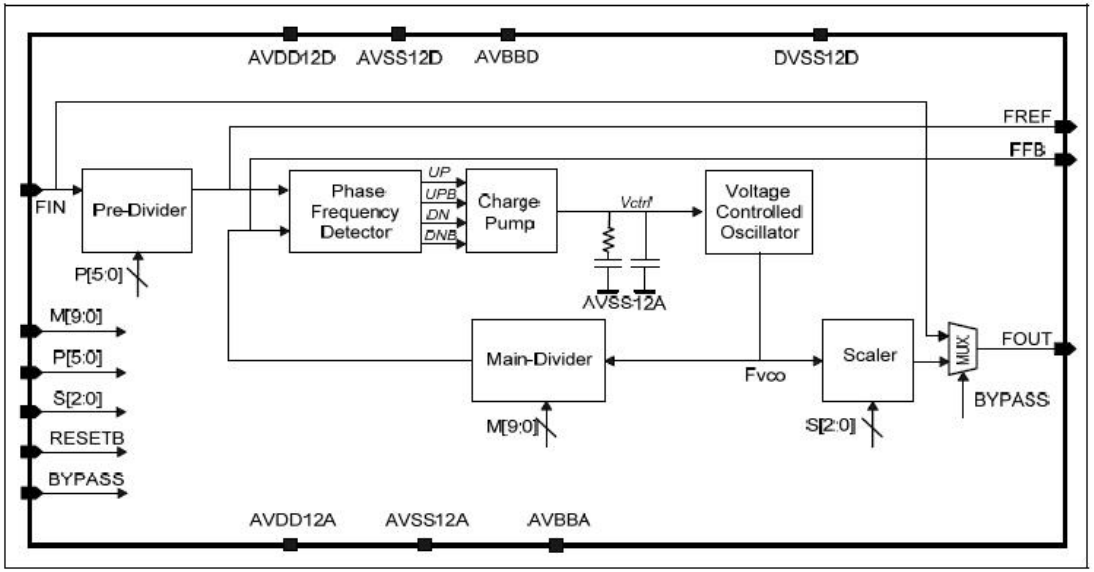

Figure 3-3. PLL block diagram (APLL, MPLL only)

TPLBN002530-31 (S3C6410X RISC Microprocessor User's Manual).

Furthermore, on information and belief, Samsung's PLLs are conceptually similar, and that each contained a ring oscillator.

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Claim 13	
13. A microprocessor system comprising:	*See* Claim Element 6.a.
a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;	*See* Claim Element 6.b.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,	*See* Claim Element 6.c.
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate,	*See* Claim Element 6.d.
thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	*See* Claim Element 6.e.
an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	*See* Claim Element 6.f.
an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and further	*See* Claim Element 6.g.
wherein said central processing unit operates asynchronously to said input/output interface.	*See* Claim Element 6.h.

Claim 14

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14. A microprocessor system of claim 13	*See* Claim Element 6.a.
wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	*See* Claim Elements 6.d, 6.e.

Claim 15	
15. A microprocessor system of claim 13	*See* Claim Element 6.a.
wherein said oscillator comprises a ring oscillator.	*See* Claim Element 6.c, and Claim 9.