EXHIBIT U

PUBLIC VERSION

THE UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of **CERTAIN WIRELESS CONSUMER ELECTRONICS DEVICES AND COMPONENTS THEREOF**	**Investigation No. 337-TA-853**

RESPONDENTS' JOINT RESPONSE AND OPPOSITION TO COMPLAINANTS' PETITIONS FOR REVIEW OF THE FINAL INITIAL DETERMINATION

PUBLIC VERSION

TABLE OF CONTENTS

Page

I. INTRODUCTION 1

II. TECHNICAL BACKGROUND 2

A. Technology Background 2

B. The Patent at Issue 3

C. The Products at Issue 5

1. Accused products 5

2. Design and operation of relevant components 5

a. Qualcomm chips 6

b. TI OMAP chips 12

c. Samsung chips 14

III. STANDARD OF REVIEW 18

IV. COMPLAINANTS DO NOT DISPUTE MOST OF THE ID'S FINDINGS AND RULINGS 18

V. THE "ENTIRE OSCILLATOR" LIMITATION OF CLAIMS 6 AND 13 20

A. The ID correctly found that Complainants failed to show that many of the accused products include an oscillator or a ring oscillator 20

1. The petition mischaracterizes the ID's finding on this issue 20

2. Complainants failed to demonstrate that certain Qualcomm chips meet the "oscillator" and "ring oscillator" limitations. 22

3. Complainants' petition further highlights the complete lack of evidence of an "oscillator" in many accused Qualcomm chips 23

B. The ALJ correctly construed the "entire oscillator" limitation of claims 6 and 13 25

1. Overview of the claimed invention as relevant to the "entire oscillator" limitation 26

2. The ALJ's correct claim construction 30

3. The intrinsic evidence supports the ALJ's correct construction 30

PUBLIC VERSION

TABLE OF CONTENTS (cont'd)

Page

a. The '336 patent prosecution history expressly disclaims reliance on external crystals and frequency generators 30

i. The ALJ's construction correctly incorporated the clear prosecution disclaimers 30

ii. Complainants' criticisms of the ALJ's reliance on these clear disclaimers are misplaced 36

b. The '336 patent's prosecution history also clearly disclaims reliance on control signals 40

c. The claim language also supports the ALJ's construction 42

d. The specification further supports the ALJ's construction.....43

4. The district court claim constructions support the ALJ's construction 46

5. The Accused Products do not practice the "entire oscillator" limitations even under Complainants' construction 47

C. The ALJ correctly found that the accused products do not meet the "entire oscillator" limitation 48

1. Review should *not* be granted in response to Complainants' perfunctory assertion that the accused products infringe under the ALJ's claim construction.....48

2. The ALJ correctly found noninfringement under his proper construction of the "entire oscillator" limitation.....50

a. Complainants waived any infringement argument under the ALJ's correct application of his claim construction.....50

b. Complainants' arguments are each without merit 51

i. Contrary to Complainants' mischaracterizations, the ALJ correctly found that setting the frequency of a clock is an inseparable part of clock signal generation....51

ii. Complainants also mischaracterize the ALJ's findings regarding control signals.....55

iii. The alleged "change" in the ALJ's claim construction is in fact a claim requirement.....55

iv. Complainants ignore the ALJ's unchallenged findings that the accused products rely on external crystals and control signals to cause the on-chip oscillators to oscillate 56

PUBLIC VERSION

TABLE OF CONTENTS (cont'd)

Page

VI. THE "VARYING" LIMITATION OF CLAIMS 6 AND 13 57

A. Complainants' argument based on binning is misplaced 58

1. Binning relates to maximum processing frequency *capability* 58

2. Maximum processing frequency *capability* is irrelevant to claims 6 and 13 and does not reflect the actual processing frequency or clock rate in the accused products 60

3. Complainants' other evidence regarding maximum processing capability is equally irrelevant 63

B. The claimed speed/frequency variation must occur during chip operation 67

1. The limitation "as a function of [fabrication] parameter variation" in claims 6 and 13 must occur during operation 68

2. Empirical evidence confirms that the processing frequency does not vary as a function of PVT 71

VII. THE "OFF-CHIP EXTERNAL CLOCK" LIMITATION OF CLAIMS 6 AND 13 77

A. The ID correctly found that the accused products do not meet the "external clock is operative at a frequency independent of a clock frequency of said oscillator" limitation of claims 6 and 13 77

1. Dr. Oklobdzija's conclusory testimony is insufficient 77

2. The Commission should reject Complainants' misinterpretation of the undisputed construction 80

a. Complainants disregard the agreed-upon construction 80

b. Complainants' argument based on the "entire" limitations is specious 84

3. Complainants' eleventh-hour focus on "external" I/O clocks cannot remedy their failure of proof 85

a. Commission precedent precludes infringement based on an "external clock" located on a different device 85

b. Complainants' argument about testing is a strawman 88

B. The ID correctly found that the accused products do not meet the "wherein … asynchronous" limitation of claim 13 89

PUBLIC VERSION

TABLE OF CONTENTS (cont'd)

Page

1. Complainants cannot satisfy the "no readily predictable phase relationship" requirement of the undisputed construction 89

2. Complainants' citations to the word "asynchronous" in documents cannot satisfy their burden 92

3. Complainants have not petitioned on or offered evidence addressing the "derived from the timing control of the input/output interface" requirement of the undisputed construction 95

VIII. CEASE & DESIST ORDER 96

IX. CONCLUSION 96

PUBLIC VERSION

TABLE OF AUTHORITIES

Page(s)

Cases

Abbott Labs. v. Sandoz, Inc.,
566 F.3d 1282 (Fed. Cir. 2009) (*en banc*) 39

Agfa Corp. v. Creo Prods. Inc.,
451 F.3d 1366 (Fed. Cir. 2006) 84

Am. Piledriving Equip. v. Geoquip, Inc.,
637 F. 3d 1324 (Fed. Cir. 2011) 36, 41

Ballard Med. Prods. v. Allegiance Healthcare Corp.,
268 F.3d 1352 (Fed. Cir. 2001) 40

Broadcom Corp. v. Int'l Trade Comm'n,
542 F.3d 894 (Fed. Cir. 2008) 20, 50, 51, 87

Certain Acid-Washed Denim Garments and Accessories,
Inv. No. 337-TA-324, Comm'n Notice, 1992 WL 738782 (Nov. 1992) 18

Certain Electronic Devices with Image Processing Sys.,
Inv. No. 337-TA-724, Comm'n Op., 2012 WL 3246515 (Dec. 21, 2011) 59, 86, 87

Certain Video Game Sys.,
Inv. No. 337-TA-770, Comm'n Notice (Nov. 6, 2012) 87

Certain Video Game Sys.,
Inv. No. 337-TA-770, Init. Determ., 2012 WL 4480570 (Aug. 31, 2012) 87

Chicago Bd. Options Exch. Inc. v. Int'l Secs. Exch. LLC,
677 F.3d 1361 (Fed. Cir. 2012) 45

Chimie v. PPG Indus., Inc.,
402 F.3d 1371 (Fed. Cir. 2005) 36

Computer Docking Station Corp. v. Dell, Inc.,
519 F.3d 1366 (Fed. Cir. 2008) 35

Digital Biometrics, Inc. v. Identix, Inc.,
149 F.3d 1335 (Fed. Cir. 1998) 35

PUBLIC VERSION

TABLE OF AUTHORITIES (cont'd)

Page(s)

Elkay Mfg. Co. v. Ebco Mfg. Co.,
192 F.3d 973 (Fed. Cir. 1999) 41

Gillespie v. Dywidag Systs. Int'l, USA,
501 F.3d 1285 (Fed. Cir. 2007) 35

Johnston v. IVAC Corp.,
885 F.2d 1574 (Fed. Cir. 1989) 83, 85, 92

Kim v. ConAgra Foods, Inc.,
465 F.3d 1312 (Fed. Cir. 2006) 80, 94

Krippelz v. Ford Motor Co.,
667 F.3d 1261 (Fed. Cir. 2012) 35

Microsoft Corp. v. Multi-Tech. Sys., Inc.,
357 F.3d 1340 (Fed. Cir. 2004) 36, 41

N. Am. Container Inc. v. Plastipak Packaging Inc.,
415 F.3d 1335 (Fed. Cir. 2005) 36

Phillips v. AWH Corp.,
415 F.3d 1303 (Fed. Cir. 2005) (*en banc*) 40, 43, 45

Revolution Eyewear, Inc. v. Aspex Eyewear, Inc.,
563 F.3d 1358 (Fed. Cir. 2009) 67

Rheox, Inc. v. Entact, Inc.,
276 F.3d 1319 (Fed. Cir. 2002) 35

SciMed Life Sys. v. Advanced Cardiovascular Sys.,
242 F.3d 1337 (Fed. Cir. 2001) 45

Seachange Int'l, Inc. v. C-COR, Inc.,
413 F.3d 1361 (Fed. Cir. 2005) 36, 41

Southwall Techs., Inc., v. Cardinal IG Co.,
54 F.3d 1570 (Fed. Cir. 1995) 35

Springs Window Fashions LP v. Novo Indus., L.P.,
323 F.3d 989 (Fed. Cir. 2003) 36

PUBLIC VERSION

TABLE OF AUTHORITIES (cont'd)

Page(s)

Other Authorities

19 C.F.R. § 210.42(a)(1)(ii) 96

19 C.F.R. § 210.43(a)(1) 96

19 C.F.R. § 210.43(b)(2) 19, 49, 50

19 C.F.R. § 210.43(d)(2) 18

19 C.F.R. § 210.46 96

PUBLIC VERSION

TABLE OF ABBREVIATIONS

'336 patent	U.S. Patent No. 5,809,336, entitled "High Performance Microprocessor Having Variable Speed Clock"
ALJ	Administrative Law Judge
C&D	Cease & Desist
CBr.	Complainants' Initial Post-Hearing Brief
CRBr.	Complainants' Reply Post-Hearing Brief
CDX	Complainant's Demonstrative Exhibit
Complainants	Complainants Phoenix Digital Solutions, Patriot Scientific Corporation and Technology Properties Limited
CX	Complainants' Exhibit
CXM	Complainants' *Markman* Exhibit
ID	Final Initial Determination, issued on September 6, 2013
JX	Joint Exhibit
JXM	Joint *Markman* Exhibit
MTr.	Transcript of *Markman* Hearing
Qualcomm	Qualcomm Incorporated
Pet.	Complainants' Petition for Review of ID, filed on September 23, 2013
RBr.	Respondents' Initial Post-Hearing Brief
RRBr.	Respondents' Reply Post-Hearing Brief
RDX	Respondents' Demonstrative Exhibit
RD	Recommended Determination, issued on September 6, 2013
Respondents[1]	Barnes & Noble, Inc. ("Barnes & Noble"); Garmin Ltd., Garmin International, Inc. and Garmin USA, Inc. (collectively, "Garmin"); HTC Corporation & HTC America, Inc. (collectively, "HTC"); Huawei Technologies Co., Ltd., Huawei Device Co., Ltd., Huawei Device USA Inc., and Futurewei Technologies, Inc. (collectively, "Huawei"); LG

[1] For purpose of this submission, "Respondents" do not include the respondents that have recently settled with Complainants and filed a motion to terminate the Investigation as to them pursuant to settlement. The respondents that have filed such motions to terminate are: Acer Inc. and Acer America Corporation; Amazon.com, Inc.; Kyocera Corporation and Kyocera Communications, Inc.

	Electronics, Inc. and LG Electronics U.S.A., Inc. (collectively, "LG"); Nintendo Co., Ltd., and Nintendo of America Inc. (collectively, "Nintendo"); Novatel Wireless, Inc. ("Novatel Wireless"); Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively, "Samsung"); and ZTE Corporation and ZTE (USA) Inc. (collectively, "ZTE")
RPX	Respondents' Physical Exhibit
RX	Respondents' Exhibit
SBr.	Staff's Initial Post-Hearing Brief
SRBr.	Staff's Reply Post-Hearing Brief
TI	Texas Instruments Inc.
Tr.	Transcript of Pre-Hearing Conference and Hearing

Note: Unless otherwise noted, all emphases in this brief have been added.

PUBLIC VERSION

I. INTRODUCTION

Administrative Law Judge Gildea's thorough and well-supported Initial Determination correctly concluded that none of the Respondents violated Section 337. In his ID, the ALJ meticulously analyzed the evidence and arguments presented by the private parties and the Office of Unfair Import Investigations, and correctly concluded that Respondents' accused products do not meet at least three separate and independent limitations of each asserted claim.

These findings rest on an exhaustive review of the record and reflect the ALJ's sound understanding and rejection of Complainants' positions. In this regard, the ALJ's noninfringement findings reflect his determination that Complainants' infringement claims are in most respects contrary to the objective evidence, and that in all other respects the Complainants failed to meet their burden to provide evidence supporting their claims. The ALJ also provided a reasoned assessment of the testimony of Complainants' sole expert witness, Dr. Oklobdzija – through whom Complainants elicited most of their "evidence" – and found that Dr. Oklobdzija's testimony was conclusory and lacked credibility, often because Dr. Oklobdzija's litigation-driven opinions directly contradicted his own pre-litigation statements in a textbook that he co-authored. Complainants' failure to support their claims stands in stark contrast to the evidence and testimony presented by Respondents and their expert, Dr. Subramanian, whom the ALJ credited with providing detailed, reliable, well-supported, and compelling testimony establishing noninfringement. In short, the ID presents an unassailable determination of no infringement which should be adopted by the Commission.

As explained in more detail below, Complainants' petition starkly demonstrates the weakness of Complainants' case, as they have now abandoned (1) eight of the ten patent claims previously asserted at trial, (2) all contentions of indirect infringement, (3) any potential assertion under the Doctrine of Equivalents, (4) their contentions against many specified

respondent products, and (5) all of their claims against respondent Nintendo. Moreover, Complainants allege error as to only one of the ALJ's many claim constructions in this investigation, and that supposed claim of error is wholly without merit.

Complainants' petition does little more than present a subset of the infringement arguments and evidence that the ALJ already considered and rejected. As reflected in the ID, the ALJ rejected these positions, because they lacked evidentiary support, because they relied solely on expert testimony that the ALJ found to lack either substance or credibility, or because of both. Hoping to mislead the Commission into reviewing the ID, Complainants' petition incorrectly asserts that the ALJ allegedly failed to consider certain evidence (which he clearly did consider), that the ALJ supposedly failed to apply his own claim constructions (which is belied by the ALJ's actual analysis in the ID), and that the ALJ allegedly erred by construing one of the three separate claim limitations found not to be infringed (an argument that is contrary to conclusive intrinsic evidence that the ALJ thoroughly analyzed during the *Markman* process).

Complainants' naked assertions of factual and legal error, like their underlying infringement arguments, are wholly conclusory and do not raise any legitimate basis for review of the ID. The record evidence clearly shows that the ID's noninfringement findings (each of which presents a separate and independent basis for affirmance) are wholly correct.

II. TECHNICAL BACKGROUND

A. Technology Background

On March 5, 2013, Respondents' technical expert, Dr. Vivek Subramanian, gave a technology tutorial as part of the *Markman* hearing. [Markman Tr. (Subramanian) 31:19-72:22.] This tutorial discussed, among other things, clocking microprocessors, phase locked loops ("PLLs"), crystal oscillators, voltage controlled oscillator ("VCOs"), and ring oscillators. As described in more detail below with respect to the operation of the relevant components of the

accused products, the technology at issue generally concerns the clocking of microprocessors.

B. The Patent at Issue

Complainants assert U.S. Patent No. 5,809,336 (the "'336 patent"), titled "High Performance Microprocessor Having a Variable Speed Clock." [Order No. 31 at 5; JXM-1 at 1.] Although Complainants asserted claims 1, 6-7, 9-10, 11, and 13-16 at the hearing,[2] their petition only seeks review of the ID's findings on independent claims 6 and 13.

The '336 patent relates to a variable-speed clock that controls the speed of a CPU incorporated on the same integrated circuit substrate as the clock. [Order No. 31 at 5-6; JXM-1 at Abstract & 16:60-17:2.] The patent explains that a high-speed microprocessor must "operate over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing" that "all affect transistor propagation delays." [Order No. 31 at 5; JXM-1 at 16:44-48.] These three parameters – "processing," "voltage" and "temperature" – are referred to as "PVT" parameters.

As the specification explains, traditional prior art microprocessor systems are designed with a single fixed clock for all parts of the system. [JXM-1 at 16:48-50, 17:12-13.] This fixed clock sets the frequency of the CPU at a speed that is slow enough to ensure error-free operation during the worst-case conditions for all PVT parameters. [*Id.*] As a result, traditional microprocessor systems "must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse [sic] case conditions" to ensure error-free operation. [*Id.* at 16:50-53; Tr. (Subramanian) 1112:12-1113:5; RDX-4.5.]

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[2] With respect to Nintendo, Complainants only asserted claims 1 and 11. Because Complainants only seek review on claims 6 and 13, they necessarily waived any objections to, and abandoned the ability to seek review of, the ALJ's noninfringement ruling regarding Nintendo. Hence, this brief will not address any issue related to Nintendo, including the codec chips that were unique to this respondent.

To overcome this limitation on CPU speed and allow the CPU to always operate at or near its maximum performance capabilities, the '336 patent discloses a microprocessor system in which an on-chip variable speed system clock controls the CPU's speed. The frequency of that variable speed clock changes in real time as a function of PVT parameters to match the CPU's capabilities under those same PVT parameters. [JXM-1 at 3:26-34, 16:60-17:2; Tr. (Subramanian) 1113:6-1115:17; RDX-4.6.] That is, the clock's frequency varies together with the CPU's capabilities. [JXM-1 at 3:26-34, 16:60-17:2; Tr. (Subramanian) 1111:12-1112:11.]

Because certain devices which communicate with the CPU cannot tolerate a variable speed clock, the system requires a second clock that is independent of the variable speed oscillator that is connected to an I/O interface. [ID at 7; Order No. 31 at 5-6; JXM-1 at 17:22-34.] The frequency of the second clock is fixed, thus allowing the I/O interface to interact with off-chip memory and other off-chip components, and to perform operations, such as "video display updating and disc drive reading and writing," which require a fixed frequency. [JXM-1 at 17:14-37.] The second clock and its connection to the I/O interface is illustrated in Figure 17 of the '336 patent, with the second clock labeled as the "crystal clock" 434. [*Id.* at Fig. 17.]

To achieve optimum CPU performance, the '336 patent's specification describes the variable speed CPU as being decoupled from the fixed speed I/O interface by connecting the variable speed clock to the CPU while separately connecting the independent fixed-speed crystal clock to the I/O interface. [JXM-1 at 17:32-34; Tr. (Subramanian) 1127:4-1129:22; RDX-4.13-14.] Unlike a fixed clock's speed that varies so little in response to the PVT parameters that it is effectively fixed, the frequency (*i.e.*, speed) of the claimed variable speed clock (ring oscillator) varies significantly and is determined by the PVT parameters. [JXM-1 at 16:59-60 ("The ring oscillator frequency is determined by the parameters of temperature, voltage, and process").] For

example, the '336 patent specification discloses that the speed of the variable speed clock will be 100 megahertz at room temperature, but will slow to 50 megahertz if the temperature rises to 70°C (*i.e.*, 158° F), and may vary by as much as a factor of four (*i.e.*, by as much as 400%) depending on all three PVT parameters. [*Id.* at 16:59-63, 17:21-22; RDX-4.93.]

Notably, the '336 patent never mentions a PLL or a VCO. As Complainants' expert conceded, the '336 patent does not relate to controlled oscillators or PLLs:

> [Q.] I'm trying to deal with what the patent discloses. The VCO is not disclosed?
> A. *The patent is not about VCO.*
> Q. And also we know that there's no disclosure in the patent about a PLL; isn't that right?
> A. *The patent is not about PLL.*

[Tr. (Oklobdzija) 816:11-18.] In fact, PLLs and VCOs existed long before the filing of the '336 patent. [*Id.* 817:2-5 (agreeing that "the PLL circuits have been around since the 1970s").]

C. The Products at Issue

1. Accused products

Complainants accuse many different categories of consumer electronic devices of infringing the '336 patent. The following is a summary of the accused products, by product category, for each remaining Respondent: Barnes & Noble (e-readers and tablet computers); Garmin (navigation devices); HTC (smartphones and tablet computers); Huawei (smartphones and tablet computers); LG (smartphones and mobile phones); Nintendo (portable handheld gaming devices); Novatel Wireless (mobile hotspots); Samsung (smartphones); and ZTE (smartphones, mobile phones, and wireless home phones).

2. Design and operation of relevant components

Each of Respondents' accused products includes a chip from one of three different chip families: Qualcomm; Texas Instruments ("TI") OMAP; and Samsung. [Tr. (Subramanian) 1140:1-13.] Complainants contend that these chips constitute the "integrated circuit" comprising

a CPU and a variable speed clock required by the asserted claims.[3] The design and operation of these chip families, to the extent relevant to the issues raised in the petition, are described below.

a. Qualcomm chips

Certain accused products use one of a number of different accused Qualcomm microprocessor chips. At a high level, there are similarities in how each accused Qualcomm chip generates and distributes clock signals. [redacted]

[RDX-4.39C (excerpt).] [redacted]

[3] The TI audio codec chips in Nintendo's accused products are not addressed here because TPL is no longer challenging the noninfringement findings regarding claims 1 and 11.

PUBLIC VERSION

[redacted]

Accordingly, there is no evidence in the record regarding the internal structure and operation of numerous PLLs used in many of the accused Qualcomm chips. [ID at 118-119.]

For the Qualcomm chips for which Complainants obtained discovery, the table below identifies the types of PLLs present in these chips:

[redacted]

[RDX-4.42C (excerpt); Tr. (Subramanian) 1147:17-1149:3; RX-611C at [redacted]; RX-628C at [redacted] RX-622C at [redacted]; RX-627C at [redacted]; RX-607C at [redacted].]

As illustrated in RDX-4.42C, many of the accused Qualcomm chips include [redacted]

PUBLIC VERSION

[redacted]

At the hearing, Respondents' expert, Dr. Subramanian, provided a detailed discussion about the structure and operation of each of the Qualcomm PLLs for which information is available. [*Id.* 1140:24-1182:23.] Dr. Subramanian's testimony identified the relevant structural and operational differences, as well as similarities, between these PLLs. [*Id.;* RDX-4.43C-4.70C.] In light of the ID's findings and the narrower scope of Complainants' petition, it is unnecessary to review each of these Qualcomm PLLs to dispose of the petition. For this reason, Respondents will only provide, as an example of the relevant technology, a brief discussion of the first Qualcomm PLL listed on RDX-4.42C.

[redacted]

[RDX-4.45C (excerpt); Tr. (Subramanian) 1150:13-1151:13; RX-618C at [redacted]; RX-

PUBLIC VERSION

621C at [redacted].] [redacted]

PUBLIC VERSION

[RX-621C at [redacted] (excerpt); Tr. (Subramanian) 1158:7-1159:2]

PUBLIC VERSION

[redacted]

PUBLIC VERSION

[redacted]

b. TI OMAP chips

The second set of chips used in some of the Respondents' accused products are Texas Instruments OMAP chips. The six accused OMAP chips come from [redacted] The accused [redacted]

At the hearing, Dr. Subramanian provided a detailed discussion about the structure and operation of the [redacted], including their [redacted] [Id. 1182:24-1190:16; RDX-4.71C-4.77C.] In light of the ID's findings and the narrower scope of Complainants' petition, Respondents will focus on the [redacted] as an example. [Tr. (Subramanian) 1184:22-1186:24; RDX 4.73C; RX-528C at LGE800ITC 85679, 85682-91.]

[RDX-4.72C (excerpt).] [redacted]

PUBLIC VERSION

[redacted]

PUBLIC VERSION

[redacted]

c. Samsung chips

Some of the accused [redacted] products incorporate microprocessor chips manufactured by [redacted] including the [redacted] chips. [RDX-4.81C; Tr. (Subramanian) 1195:4-19.]

PUBLIC VERSION

At the hearing, Dr. Subramanian provided a detailed discussion about the structure and operation of the [redacted] [*Id.* 1195:4-1201:23; RDX-4.81C-4.84C.] At a high level, there are similarities in how the [redacted] generate and distribute clock signals. [*Id.*] Given the ID's findings and the narrower scope of Complainants' petition, Respondents will focus on the [redacted] chip as an example.

[redacted]

[RDX-4.83C (excerpt).] [redacted]

PUBLIC VERSION

[redacted]

PUBLIC VERSION

[redacted]

PUBLIC VERSION

III. STANDARD OF REVIEW

Under Commission Rule 210.43(d)(2), the Commission may grant a petition for review of an initial determination if the petitioner demonstrates:

(i) That a finding or conclusion of material fact is clearly erroneous;

(ii) That a legal conclusion is erroneous, without governing precedent, rule or law, or constitutes and abuse of discretion; or

(iii) That the determination is one affecting Commission policy.

19 C.F.R. § 210.43(d)(2); *see also Certain Acid-Washed Denim Garments and Accessories*, Inv. No. 337-TA-324, Comm'n Notice, 1992 WL 738782 (Nov. 1992). Because Complainants' petition fails to establish any of these grounds, their petition should be denied.

IV. COMPLAINANTS DO NOT DISPUTE MOST OF THE ID'S FINDINGS AND RULINGS

As a preliminary matter, Complainants' petition for review is very narrow, as it challenges three separate and independent grounds of noninfringement in the ID with respect to only two asserted claims.[4] Importantly, the petition does ***not*** challenge a number of findings made in the ID, including:

- The finding that none of the Respondents infringe claims 1, 7, 9, 10, 11, 14, 15, and 16 of the '336 patent. [Pet. at 3 n. 1 ("In an attempt to streamline this Petition, Complainants have chosen to focus only on claims 6 and 13 of the '336 patent.").][5]
- The finding that the accused audio codec chips used in Nintendo's accused products lack a "central processing unit," as required by all asserted claims. [ID at 273-275.]
- The finding that there is no infringement under the Doctrine of Equivalents. [ID at 275.]

[4] As explained in Section VIII, *infra*, Complainants prematurely challenge a portion of the ALJ's RD on Remedy and Bond with respect to certain Respondents.

[5] Because Complainants have only alleged that Nintendo infringes claims 1 and 11 of the '336 patent, their decision to focus their petition on only claims 6 and 13 concedes that the ID correctly found no violation of Section 337 by Nintendo.

- The finding that there is no contributory infringement and no induced infringement. [ID at 280.]
- The finding that the products listed in Attachments B and C of Respondents' opening brief do not infringe any asserted claims of the '336 patent. [ID at 286-287.]

In addition to these undisputed findings, Complainants' petition does ***not*** contest the ALJ's claim constructions of any limitation, except for the limitation "an entire oscillator disposed upon said integrated circuit substrate" in claims 6 and 13. [*Compare generally* Pet. *with* ID at 13-17.] For example, Complainants do not dispute the ALJ's construction of the limitation "wherein said central processing unit operates *asynchronously* to said input/output interface" in claim 13. [Pet. at 45-47 (arguing that ALJ allegedly erred in applying his construction of this term to the evidence); *see also* ID at 245-259 (applying claim construction to facts).] Nor do Complainants challenge the interpretation of the term "external clock is operative at a frequency *independent* of a clock frequency of said oscillator" in claims 6 and 13, given that they stipulated to the adopted construction. [ID at 14 (indicating agreed-upon construction for this limitation); Pet. at 35-36 (summarizing agreed upon construction); *see also* ID at 245-259 (applying agreed-upon construction to facts).] And the "varying … as a function of" limitation in claims 6 and 13 do not implicate any claim construction, because Complainants did not advance any proposed interpretation of this term and the ALJ did not adopt a construction of this limitation. [ID at 13-16 (no construction of the term); Pet. at 26-35 (only arguing factual error with respect to this limitation).]

By failing to challenge these factual findings and claim constructions in their petition, Complainants have waived their rights to dispute these issues before the Commission or in a later appeal. 19 C.F.R. § 210.43(b)(2) ("Any issue not raised in a petition for review will be deemed to have been abandoned by the petitioning party and may be disregarded by the Commission in reviewing the initial determination"); *Broadcom Corp. v. Int'l Trade Comm'n*, 542 F.3d 894, 900-

901 (Fed. Cir. 2008) (finding waiver of an argument not raised in a petition of review to the Commission).

With these undisputed issues waived, the only challenges presented in the petition are whether (i) the ALJ correctly construed the "entire oscillator" limitation in claims 6 and 13 and properly applied the correct construction to the evidence; (ii) the ALJ correctly found no evidence of infringement of claims 6 and 13's "varying … as a function of" limitation; and (iii) the ALJ correctly found no infringement of claims 6 and 13's "off-chip external clock" limitation. Respondents address each of these issues below.

V. THE "ENTIRE OSCILLATOR" LIMITATION OF CLAIMS 6 AND 13

A. The ID correctly found that Complainants failed to show that many of the accused products include an oscillator or a ring oscillator

1. The petition mischaracterizes the ID's finding on this issue

Complainants' petition mischaracterizes the ID's findings with respect to the "oscillator" / "ring oscillator" claim limitations, and reflects a misunderstanding of the scope of ALJ's findings with respect to these claim limitations. According to the petition, the ALJ erred in concluding that Complainants relied on a "blanket assumption" that all of the accused chips include ring oscillators, and that the ALJ ignored undisputed evidence of "ring oscillators" in certain accused products. [Pet. at 7 (citing ID at 118-19).] However, the ID did not find that Complainants failed to produce evidence of a "ring oscillator" in ***all*** accused products. Rather, the ID states that the evidence is insufficient to establish" that ***certain*** accused chips include either an oscillator or a ring oscillator:

> Because Complainants bear the burden of proof, in order to prove that each of the Accused Products infringes, more is required than a blanket assumption based on Dr. Oklobdzija's general knowledge of digital system clocking to warrant reliance. Therefore, the Administrative Law Judge finds that ***the evidence is not sufficient to establish that chips listed above meet this element*** of the asserted claims.

[ID at 119; *see also* Sept. 12, 2013 Notice of Clarification Regarding Final Initial Determination (clarifying that the list of chips referenced on page 119 of the ID is located on page 88 of the ID).] Specifically, the ID found that Complainants failed to prove that the following 24 models of Qualcomm chips include an oscillator or ring oscillator:

[ID at 88.]

Although the ID limited its noninfringement findings with respect to the oscillator/ring oscillator limitations to the above-listed 24 models of Qualcomm chips, Complainants' petition misleadingly argues that these limitations are present in all accused chips by pointing for the most part to "ring oscillators" in chips other than the 24 chips identified by the ALJ. [*See* Pet. at 9-11 (discussing various other models of chips manufactured by Qualcomm, such as the [redacted] *id.* at 7-9, 12 (discussing chips developed by other manufacturers, including [redacted]).] Because the ID clearly states (particularly in view of the Notice of Clarification) that its noninfringement findings with respect to the oscillator/ring oscillator limitations are limited to the 24 Qualcomm chips listed above, Complainants' argument that the ALJ allegedly failed to consider evidence of ***other chips*** is irrelevant. Indeed, that Complainants had to resort to discussing other chips highlights that, as the ALJ correctly found, Complainants failed to provide any meaningful evidence as to these 24 chips.

2. Complainants failed to demonstrate that certain Qualcomm chips meet the "oscillator" and "ring oscillator" limitations.

Ample evidence not only supports, but also mandates, the ID's finding that Complainants failed to demonstrate that certain Qualcomm chips meet the "oscillator" and "ring oscillator" limitations. As the ID correctly notes, the testimony of Complainants' expert, Dr. Oklobdzija, is "incomplete and inconclusive with respect to whether all of the accused chips include the claimed ring oscillators or oscillators." [ID at 118.]

Although claims 6 and 13 of the '336 patent expressly require an "oscillator," Complainants fail to identify any particular oscillator for a large number of accused Qualcomm chips, and instead identify only a PLL on the chip. [ID at 37-38; JXM-1 at cls. 6, 13; Tr. (Subramanian) 1334:5-23; RDX-4.147C (identifying 24 Qualcomm chips for which Complainants have alleged only a PLL).] Attempting to overcome this failure of proof, Complainants' expert, Dr. Oklobdzija, made a blanket assumption that all PLLs necessarily contain a ring oscillator. [ID at 37-38; Tr. (Oklobdzija) 442:16-443:1 ("I'm 99 percent sure that everything that has a PLL has a ring oscillator... My confidence level is 99.999 percent high..."); *id.* at 459:23-460:8; *see also* Tr. (Subramanian) 1335:4-10 (summarizing Complainants' argument).] However, the evidence, including Dr. Oklobdzija's own pre-litigation writing, does not support his opinion or his confidence level.

The evidence shows that a PLL does not need to include an oscillator. [ID at 38, 85.] First, Respondents' expert, Dr. Subramanian, explained that one type of PLL, called a delay-locked loop ("DLL"), does not incorporate any oscillator. [ID at 118, 38, 85; Tr. (Subramanian) 1335:11-1336:3.] As illustrated below, a DLL instead uses a delay line to control the frequency and align the phase of the output signal with the phase of the reference signal:

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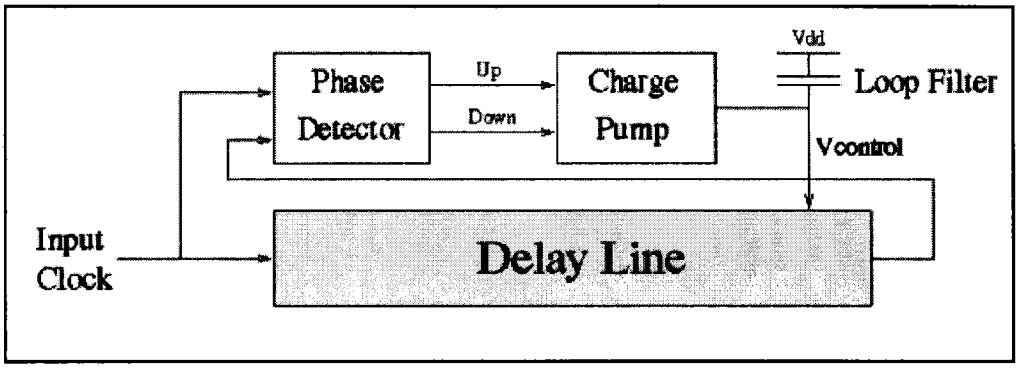


[Tr. (Subramanian) 1335:11-1336:3; RDX-4.145 (excerpt).] Second, Dr. Oklobdzija's own book on clocking expressly recognizes that a DLL is a type of PLL in which a voltage-controlled delay line replaces the controlled oscillator:

> The other type of PLL is delay-line based or delay-locked loop (DLL). As shown in Fig. 1.12, the VCO in the PLL is replaced by the voltage-controlled delay line (VCDL), which delays the external clock, feeding the clock driver, until the internal clock becomes aligned with the external clock, at which point the control voltage of the VCDL become steady and the loop stays in lock. An

[RX-2283 at Garmin 92907-08; ID at 118-119 (discussing same); *see also id.* at 38, 85-86.] Because a PLL need not include an "oscillator," Complainants cannot rely, as they do, on the mere presence of a PLL to satisfy claims 6 and 13.

Accordingly, the ALJ correctly found that "[g]iven the conflicting evidence, both from Dr. Subramanian and from Dr. Oklobdzija's own textbook, more was needed to be shown by Complainants besides Dr. Oklobdzija's sweeping generalization" that he was 99 percent sure the accused PLLs include a ring oscillator. [ID at 118-19.]

3. **Complainants' petition further highlights the complete lack of evidence of an "oscillator" in many accused Qualcomm chips**

As discussed above, the ID found that Complainants failed to demonstrate the presence of an oscillator / ring oscillator in 24 specific Qualcomm chips. Remarkably, Complainants' petition focuses on other chips that are not implicated by this finding. [*See* Pet. at 9-11 (discussing various other models of chips manufactured by Qualcomm, such as the [redacted]);

Pet. at 7-9, 12 (discussing chips developed by other manufacturers, including [redacted].] While the petition claims to provide "overwhelming" evidence that all of the accused chips include a ring oscillator, the petition only mentions 5 of the 24 chip models identified in the ID (shown in bold and underlined below).

[ID at 88; Pet. at 7-12.] Complainants' petition does not even mention the other 19 listed Qualcomm chips, much less identify any evidence that any of these chips includes an oscillator or ring oscillator. This is not surprising, because there is no such evidence in the record. Accordingly, the ID correctly found that Complainants failed to meet their burden with respect to these 19 chips. [ID at 118-19.]

With respect to the [redacted] chips, Complainants' petition includes numerous citations purporting to demonstrate that each of these chips includes a ring oscillator. [Pet. at 10-12 n.14.] Yet, none of the cited evidence even identifies the type of PLL in any of these chips, much less identifies an oscillator within the PLL. [*Id.*] For instance, the cited evidence does not support Complainants' contention that the [redacted] [*Id.* (citing CX-1220C at LGE800ITC 309550; CX-619C at QCHTCTPL 7709).] Similarly, none of the evidence cited for the [redacted] chips identifies the type of PLL or any purported oscillator within the PLL. [*Id.* (citing CX-591C ([redacted]) at NVTL_TPL853_0079980 for the [redacted], and RX-1033C; RDX-4.26C; Tr. 1136:3-15; CX515C for the [redacted]).] Given that

Complainants cannot even identify any evidence demonstrating an oscillator or ring oscillator within any of these chips, the ID's finding with respect to these chips is clearly correct.

Finally, while Complainants' petition includes citations for each of the remaining two chips (the [redacted]), the cited evidence fails to establish that either chip includes an oscillator or ring oscillator. For example, of the 12 citations relating to the [redacted] chip, only one even mentions the [redacted]—and that one citation is to Dr. Oklobdzija's unsupported testimony speculating about the type of PLL included in the chip. [Pet. at 11 fn. 14; Tr. (Oklobdzija) 352:7-353:1 ("As I said, this specification applies to three of them. ***I believe. Actually, I'm almost sure.*** [redacted]").] Similarly, while Complainants contend that the [redacted] chip is "from the same family" as the [redacted] chip, their only evidence is a cite to the unsupported testimony of Dr. Oklobdzija. [Pet. at 11 n. 14; Tr. (Oklobdzija) 446:6-447:7.][6] Given the lack of evidence of an oscillator in these chips, the ID correctly found that Complainants failed to meet their burden of proof.

B. The ALJ correctly construed the "entire oscillator" limitation of claims 6 and 13

Claims 6 and 13 require "an entire oscillator disposed upon said integrated circuit substrate." [JXM-1 at cls. 6 & 13.] In his *Markman* ruling, the ALJ construed this limitation to mean "an oscillator that is located entirely on the same semiconductor substrate as the central processing unit and does not rely on a control signal or an external crystal/ clock generator to

[6] Dr. Oklobdzija's testimony on this issue refers to demonstrative exhibit CDX-5C.15, which includes a red annotation indicating that the [redacted] is in the same family as the [redacted] chip. [Tr. (Oklobdzija) 446:6-447:7; CDX-5C.15.] The source document does not, however, include the red annotation, or any other indication that the [redacted] are in the same chip family, and of course demonstrative exhibit CDX-5C.15 is not itself evidence. [CDX-5C.15; CX-659C at [redacted]]

generate a clock signal." [Order No. 31 at 41; ID at 15.] Contrary to Complainants' criticisms, [Pet. at 13-21], the ALJ correctly construed this limitation.

The intrinsic evidence amply supports the ALJ's construction of the "entire oscillator" limitation. More specifically, the ALJ's construction (1) embodies the clear disclaimers of claim scope made by the applicants during the prosecution of the '336 patent to avoid otherwise invalidating prior art, (2) is consistent with the specification's teachings and its criticisms of the prior art, and (3) finds confirmation in the plain language of the claims. These unambiguous disclaimers and teachings in the intrinsic evidence mandate, as the ALJ found, that the claimed "entire oscillator" cannot rely on any off-chip crystal, off-chip clock generator, or control signal. In contrast, Complainants' proposed construction ignores these clear disclaimers and teachings, and fails to define what the claims mean in requiring an oscillator to be located "entirely" on the same substrate as the CPU. Because the applicants clearly and unambiguously disclaimed on-chip oscillators and clocks that rely on off-chip crystals, off-chip clock generators, or control signals, the ALJ's construction is entirely correct. Review of that construction is not warranted.

1. Overview of the claimed invention as relevant to the "entire oscillator" limitation

The '336 patent is directed to a variable-speed clock (the "entire oscillator") that controls the speed of a CPU and that is incorporated on the same integrated circuit substrate as the CPU. [ID at 7; Order No. 31 at 5-6; JXM-1 at cover & 16:54-17:10.] The variable-speed oscillator adjusts its frequency in real time based upon the microprocessor's physical and environmental characteristics, including temperature, voltage and semiconductor manufacturing process quality, to track the then-existing processing capabilities of the CPU. [JXM-1 at 16:54-17:10.] In other words, the on-chip oscillator's frequency varies together with the frequency of the CPU. [*Id.*]

The '336 patent issued as a divisional patent from a specification that describes several

different purported inventions. [ID at 5; Order No. 31 at 6; JXM-1 at cover ("Division of Ser. No. 389,334, Aug. 3, 1989, Pat. No. 5,440,749").] As a result, the '336 patent's "Summary of the Invention" section contains material that is largely irrelevant to the asserted claims, with only lines 27 through 35 of column 3 pertaining to the alleged invention. [JXM-1 at 3:27-35.] Similarly, the "Detailed Description of The Invention" includes much extraneous material, with the only parts describing the '336 patent's purported invention being found in the last 25 lines of column 16 and the first 37 lines of column 17, under the sub-headings "Optimal CPU Clock Scheme" and "Asynchronous/Synchronous CPU." [*Id.* at 16:43-17:37.]

In the parts of the specification that are relevant to the alleged invention claimed in the '336 patent, the specification explains that a high speed microprocessor must "operate over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing" that "all affect transistor gate propagation delays." [*Id.* at 16:44-48; ID at 7; Order No. 31 at 5.] These three parameters, "processing," "voltage" and "temperature," are referred to as "PVT" parameters. [ID at 7; Order No. 31 at 5.]

As the specification explains, traditional prior art microprocessor systems are designed with a single fixed speed clock for all parts of the system. [JXM-1 at 16:48-50, 17:12-13.] By design, this conventional fixed speed clock (which includes an off-chip crystal and on-chip components) always operates at a speed that is slow enough to ensure error-free operation during those times when worst case PVT parameter conditions may exist. [*Id.*] As a result, the traditional prior art microprocessor systems "must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse [sic] case conditions" to ensure that a user always experiences error-free operation. [*Id.* at 16:48-53.]

To avoid the constrained speed of the prior art and to always operate at or near its

maximum performance capabilities for the existing PVT parameter conditions, the '336 patent replaces the prior art's external fixed-speed crystal clock which controls the CPU's speed with an on-chip "ring counter variable speed system clock" (also referred to as a "ring oscillator variable speed system clock") that adjusts its speed in real time as a function of existing PVT parameters to match the CPU's maximum frequency capability under those parameters. [ID at 7; Order No. 31 at 5-6; JXM-1 at 3:26-34, 16:54-17:10, 17:19-22; Tr. (Subramanian) 1113:6-1115:17; RDX-4.6.] In other words, the oscillator's frequency varies together with the frequency of the CPU. [JXM-1 at 3:26-34, 16:60-17:2; Tr. (Subramanian) 1111:12-1112:11.]

Unlike a fixed clock's speed, the frequency of the claimed internal variable speed oscillator varies significantly as a function of PVT parameters. [JXM-1 at 16:59-60 ("The ring oscillator frequency is determined by the parameters of temperature, voltage, and process").] For example, the '336 patent's specification discloses that the speed of the variable speed clock will be 100 megahertz at room temperature, but will slow to 50 megahertz if the temperature rises to 70°C (*i.e.*, 158° F). [*Id.* at 16:59-63.] The oscillator's speed may vary, according to the patent, by as much as a factor of four (*i.e.*, by as much as 400%) depending on all three PVT parameters. [*Id.* at 17:21-22.]

According to the '336 patent, the "optimum performance" of the variable speed oscillator supposedly results from fabricating and locating the variable speed oscillator on the same semiconductor substrate as the CPU, so that the same PVT parameters affect both the oscillator and the CPU. [*Id.* at 16:57-58, 16:63-17:10.] For example, if the temperature of the substrate rises, then the processing speed capability of the CPU decreases. But because the oscillator and CPU are fabricated on the same substrate, this rise in temperature also causes the speed of the variable speed oscillator to decrease, so that the oscillator leads the CPU to operate at the slower

maximum speed at which it can operate. [*See id.*] As the specification explains, this ensures that the CPU "will always execute at the maximum frequency possible, but never too fast." [*Id.* at 16:67-17:2.]

Because certain devices which communicate with the CPU cannot tolerate a variable speed clock, the system requires a second clock that is independent of the variable speed oscillator. [ID at 7; Order No. 31 at 5-6; JXM-1 at 17:22-34.] The independent second clock is connected to the input/output (I/O) interface, as illustrated in Figure 17 of the '336 patent, with the second clock on Figure 17 being a conventional "crystal clock" 434:

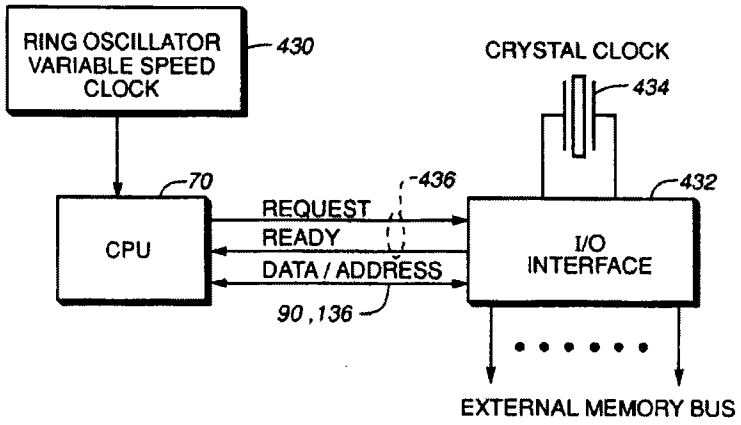


FIG._17

Each independent claim of the '336 patent (including claims 6 and 13) provides for a fixed-speed, independent second clock that is connected to an input/output ("I/O") interface. [ID at 7; Order No. 31 at 5-6; JXM-1 at 17:14-34.] The frequency of the second clock is fixed to allow the I/O interface to interact with off-chip memory and other off-chip components, and to perform operations that require a fixed frequency, such as "video display updating and disc drive reading and writing." [JXM-1 at 17:14-34.] By connecting the variable speed oscillator to the CPU while separately connecting the independent fixed speed clock to the I/O interface, the variable speed CPU is decoupled from the fixed speed I/O interface. [ID at 7; Order No. 31 at 6;

JXM-1 at 17:32-34.] This configuration optimizes the performance of the system by allowing the CPU to run as fast as possible under the current PVT conditions while maintaining the I/O interface 432 at a stable fixed speed. [JXM-1 at 17:32-34.]

2. **The ALJ's correct claim construction**

Following two rounds of claim construction briefing and an all-day *Markman* hearing, the ALJ correctly construed the claim phrase "an entire oscillator disposed upon said integrated circuit substrate" to mean:

> an oscillator that is located entirely on the same substrate as the central processing unit and does not rely on a control signal or an external crystal/clock generator to generate a clock signal.

[Order No. 31 at 40-41; *see also id.* at 37-40.] In so finding, the ALJ properly rejected Complainants' proposed construction, which merely required "an oscillator that is located entirely on the same semiconductor substrate as the central processing unit." [*Id.*]

3. **The intrinsic evidence supports the ALJ's correct construction**

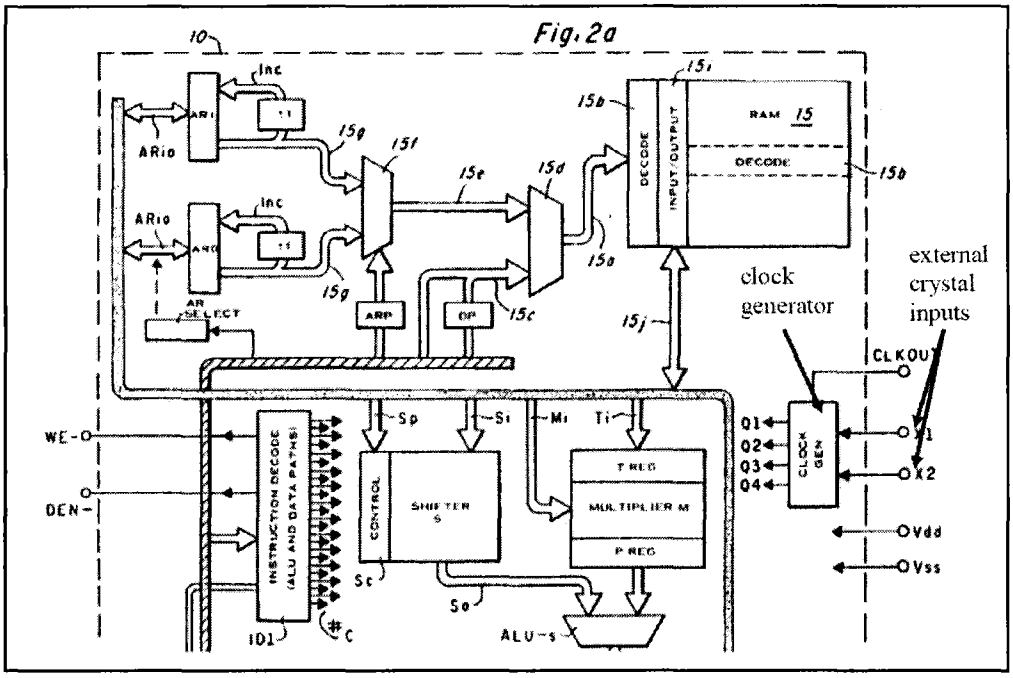
a. The '336 patent prosecution history expressly disclaims reliance on external crystals and frequency generators

i. The ALJ's construction correctly incorporated the clear prosecution disclaimers

As the ALJ correctly stated in his claim construction order, during prosecution of the '336 patent, the applicants repeatedly distinguished their purported invention from the prior art on the basis that their on-chip clock and on-chip oscillator do not rely on external crystals or external frequency generators. [Order No. 31 at 38-40.] In doing so, as the ALJ correctly found, the applicants clearly and unambiguously disclaimed any clock or oscillator, even when fabricated on the same substrate as the CPU, that relies on an external crystal or frequency generator like the prior art. [*Id.* at 39-40 (finding that "the essential point made by applicants to gain acceptance" of their claims, and their "unqualified statements in distinguishing" the prior art,

constituted a "clear disavowal" of claim scope).] The ALJ's claim construction recognizes and incorporates this key disclaimer. [*Id.*]

This disclaimer started with the applicants' attempt to overcome the Magar prior art. During prosecution, the PTO issued a non-final rejection based on U.S. Patent No. 4,503,500 to Magar ("Magar"), Figure 2a of which is reproduced below. [JXM-19 ('336 prosec. hist., April 3, 1997 rejection) at TPL85300002433-36.] In his rejection, the examiner asserted that the "CLOCK GEN" (clock generator) circuitry in Figure 2a of Magar was fabricated on the same microprocessor substrate 10 as the CPU, as required by the claims. [*Id.* at 2 (TPL8530002434).]



[JXM-15 (Magar) at Fig. 2a (annotations in red text added).]

In response, the applicants attempted to distinguish Magar on the basis that an external off-chip crystal (connected to the X1 and X2 inputs in the figure above) drove the clock:

> A review of the Magar reference shows that it is apparently no more pertinent than prior art acknowledged in the application, in that ***the clock disclosed in the Magar reference is in fact driven by a fixed frequency crystal, which is external to the Magar integrated circuit.***

[JXM-18 ('336 prosec. hist., July 7, 1997 Amend.) at 2 (TPL85300002426).]

The applicants also emphasized the following difference between their claimed variable speed clock and Magar's clock generator, which relies on the frequency of an external crystal:

> Contrary to the Examiner's assertion in the rejection that 'one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock vary together due to manufacturing variation, operating voltage and temperature of the IC [integrated circuit],' one of ordinary skill in the art should readily recognize that the speed of the CPU and clock ***do not*** vary together due to manufacturing variation, operating voltage, and temperature of the IC in the Magar processor . . . ***This is simply because the Magar microprocessor clock is frequency controlled by a crystal which is also external to the microprocessor.*** *Crystals are by design fixed frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature.* ***The Magar microprocessor in no way contemplates a variable speed clock as claimed.***

[*Id.* at 3-4 (first emphasis in original) (TPL85300002427-28).] Thus, in this first amendment, the applicants ***expressly and unambiguously disclaimed*** clocks and oscillators that rely on an external crystal ***for frequency control.***

Later in this same amendment, the applicants further emphasized that, even if the Magar crystal oscillator were located entirely on the same chip as the rest of the clock generator circuitry, Magar would ***still*** not practice the claimed invention because Magar's clock could not vary with the PVT parameters:

> ***[C]rystal oscillators have never***, to Applicants' knowledge, ***been fabricated on a single silicon substrate with a CPU***, for instance. ***Even if they were***, as previously mentioned, crystals are by design fixed-frequency devices whose oscillation frequency is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. ***The oscillation frequency of a crystal on the same substrate with the microprocessor would inherently not vary due to variations in manufacturing, operating voltage and temperature in the same way as the frequency capability of the microprocessor on the same underlying substrate, as claimed.***

[*Id.* at 4.] This express disclaimer could not be clearer: the claims exclude oscillators using

crystals ***to control frequency***. More specifically, an on-chip oscillator that does not vary as a function of the PVT parameters – such as an oscillator whose frequency is controlled by any crystal or control signal – is outside the scope of the claims.

Unconvinced, the PTO issued a second rejection based on Magar. In response, the applicants amended their claims to explicitly require that the "entire" oscillator/clock be on the same integrated circuit substrate as the CPU.[7] [JXM-16 ('336 prosec. hist., Feb. 10, 1998 Amend.) at 1-2 (TPL853_02954557-558).] Along with this amendment, the applicants again tried to distinguish Magar from the claimed invention by arguing that Magar's clock generator could not operate properly without the use of an external component such as a crystal. In doing so, the applicants directed the examiner to Magar's disclosure at 15:26-27, which states that "chip 10 includes a clock generator 17 which has two external pins X1 and X2 to which a crystal (or external generator) is connected." [*Id.* at 4 (TPL853_02954560); JXM-15 (Magar) at 15:26-27.] Because Magar does not disclose what components are included in the clock generator or how it uses the signal from the crystal, the only basis for applicants' distinction and disclaimer is Magar's reliance on the external crystal or clock generator, regardless of how the signal supplied by the external crystal or clock generator was used.

Further confirming the scope of this clear disclaimer, the applicants clearly rejected ***any reliance on an external crystal*** by telling the examiner:

> [W]hile most of Magar's clock (generator) circuitry is on the IC, ***the entire oscillator, which because it requires an external crystal, is not***.

[7] Prosecution claim 19 was amended to recite "an entire ring oscillator variable speed system clock in said single integrated circuit[;]" claim 73 was amended to recite "an entire oscillator disposed upon said integrated circuit substrate[;]" and claim 78 was amended to recite "an entire variable speed clock disposed upon said integrated circuit substrate." [JXM-16 ('336 prosec. hist., Feb. 10, 1998 Amend.) at 1-2 (underlined text indicating additions through the amendment).]

[JXM-16 ('336 prosec. hist., Feb. 10, 1998 Amend.) at 4 (TPL853_02954560).] Once again, the applicants expressly disclaimed clocks and oscillators that rely on an external crystal. But this time, they went further: they disclaimed reliance on an external crystal generally, not just for purposes of frequency control.

The applicants reinforced their disclaimers by then explaining and characterizing "the ***essential*** difference" between Magar's fixed-frequency clock and the variable speed clock shown in Figure 18 of the '336 patent:

> The signals PHASE 0, PHASE 1, PHASE 2 and PHASE 3 in Applicants' Fig. 18 are synonymous with Q1, Q2, Q3 and Q4 depicted in Magar Fig. 2a. The ***essential difference*** is that the ***frequency or rate of the PHASE 0, PHASE 1, PHASE 2 and PHASE 3 signals is determined by the processing and/or operating parameters of the integrated circuit*** containing the Fig. 18 circuit, ***while the frequency or rate of the Q1, Q2, Q3 and Q4 signals depicted in Magar Fig. 2a are determined by the fixed frequency of the external crystal*** connected to the circuit portion outputting the Q1, Q2, Q3 and Q4 signals shown in Magar Fig. 2a.

[*Id.*] By this statement, the applicants again expressly distinguished their claimed invention from Magar on the ground that their invention does not, while Magar does, rely on ***a fixed frequency external crystal to set the "frequency or rate" of the clock.***

The applicants concluded their argument about Magar by "specifically" distinguishing their claimed invention from an external crystal used for either ***frequency control*** or ***oscillation***:

> The Magar teaching . . . is specifically distinguished from the instant case in that it is both ***fixed frequency (being crystal based)*** and ***requires an external crystal or external frequency generator***.

[*Id.* at 5 (TPL853_02954561).]

Thus, the applicants distinguished the Magar reference ***both*** (1) because the ***frequency*** of Magar's on-chip clock was controlled by an external crystal, ***and*** (2) because the Magar on-chip clock relied on an external crystal to ***oscillate***. In light of these clear disavowals, the ALJ's construction correctly captures both disclaimers. *Krippelz v. Ford Motor Co.*, 667 F.3d 1261,

1267 (Fed. Cir. 2012) (affirming district court's construction imposing two limitations on the disputed claim term, because patent owner distinguished the prior art on two separate grounds).[8]

As the ALJ properly found, the disclaimers are clear: the applicants' purported invention requires an "entire" on-chip oscillator that does not rely on an external crystal or external frequency generator (or other external components). [Order No. 31 at 38-39.] Given these unambiguous disclaimers, the claimed "entire" oscillators cannot now encompass, as Complainants contend, any reliance on an external crystal or external frequency generator either for frequency control or oscillation, because binding precedent requires limiting the scope of a claim term where, as was the case here, the applicant relied on the limited scope during prosecution to obtain allowance of the patent. *Southwall Techs., Inc., v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995) ("Claims may not be construed one way in order to obtain their allowance and in a different way against accused infringers."); *Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319, 1325 (Fed. Cir. 2002) ("Explicit arguments made during prosecution to overcome prior art can lead to a narrow claim interpretation because '[t]he public has a right to rely on such definitive statements made during prosecution.'") (quoting *Digital Biometrics, Inc. v. Identix, Inc.*, 149 F.3d 1335, 1347 (Fed. Cir. 1998)); *Gillespie v. Dywidag Systs. Int'l, USA*, 501 F.3d 1285, 1291 (Fed. Cir. 2007) ("The patentee is held to what he declares during the prosecution of his patent."); *Computer Docking Station Corp. v. Dell, Inc.*, 519 F.3d 1366, 1379 (Fed. Cir. 2008) (holding that "the sum of the patentees' statements during prosecution would lead a competitor to believe that the patentee had disavowed coverage of laptops" and, thus, affirming

[8] Regardless of whether either or both of applicants' arguments distinguishing Magar ultimately were successful, or even necessary, in convincing the examiner to allow the claims, the public is entitled to rely on them. *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 979 (Fed. Cir. 1999).

the trial court's construction of the portable computer limitation); *Seachange Int'l, Inc. v. C-COR, Inc.*, 413 F.3d 1361, 1372-75 (Fed. Cir. 2005) ("Where an applicant argues that a claim possesses a feature that the prior art does not possess in order to overcome a prior art rejection, the argument may serve to narrow the scope of otherwise broad claim language." (citations omitted)); Order No. 31 at 39-40.[9]

ii. Complainants' criticisms of the ALJ's reliance on these clear disclaimers are misplaced

In scattershot fashion, Complainants' petition makes a number of unsupported assertions to avoid the necessary conclusion – reached by the ALJ – that the applicants' repeated, express disclaimers regarding Magar compel the ALJ's construction of the "entire oscillator" claim term. None of Complainants' assertions has merit.

First, ignoring the repeated express disclaimers concerning frequency control identified above, Complainants assert that there was no disclaimer because Magar lacks an on-chip oscillator. [Pet. at 16.] This assertion, however, flies in the face of Magar and the prosecution

[9] *See also Am. Piledriving Equip. v. Geoquip, Inc.*, 637 F. 3d 1324, 1336 (Fed. Cir. 2011) ("[A]n applicant's argument that a prior art reference is distinguishable on a particular ground can serve as a disclaimer of claim scope even if the applicant distinguishes the reference on other grounds as well."); *Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) ("The purpose of consulting the prosecution history in construing a claim is to 'exclude any interpretation that was disclaimed during prosecution.'" ; "Accordingly, 'where the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender.'") (citation omitted); *Microsoft Corp. v. Multi-Tech. Sys., Inc.*, 357 F.3d 1340, 1349 (Fed. Cir. 2004) (a court "cannot construe the claims to cover subject matter broader than that which the patentee itself regarded as comprising its invention and represented to the PTO"); *Springs Window Fashions LP v. Novo Indus., L.P.*, 323 F.3d 989, 993-96 (Fed. Cir. 2003) (rejecting patentee's attempt to narrow the scope of disclaimer, even though the examiner did not rely on the disclaimer to issue the claims); *N. Am. Container Inc. v. Plastipak Packaging Inc.*, 415 F.3d 1335, 1345-46 (Fed. Cir. 2005) (holding that "the applicant, through argument [that the prior-art inner walls are "slightly concave"] during the prosecution, disclaimed inner walls of the base portion having any concavity . . . [a]lthough the inner walls disclosed in the [prior art] may be viewed as entirely concave").

history. Indeed, as discussed above, the applicants first attempted to distinguish Magar's "CLOCK GEN" circuitry on the ground that Magar's *on-chip clock* is frequency controlled by an off-chip fixed-frequency crystal (just as is the case with the Respondents' accused products in this investigation). [JXM-18 ('336 prosec. hist., July 7, 1997 Amend.) at 2-4; JXM-15 (Magar) at Fig. 2a.] Complainants' assertion also ignores another key fact: Applicants next asserted that, even if the off-chip crystal in Magar were placed on the chip, Magar still would not anticipate the claimed invention because the invention does not encompass the use of a fixed-speed crystal (whether on or off chip) to control the frequency of the on-chip clock (which, again, is the case with Respondents' accused products). [*Id.* at 4.]

Worse yet, Complainants further ignore that the applicants next amended their claim by adding the word "entire" to the term "entire oscillator" and argued that: (1) Magar cannot anticipate the claims without an "entire" clock on the chip because, while the CLOCK GEN circuitry is on the chip, the fixed-speed external crystal is *not* on the chip (which is just like the accused products in this investigation); (2) their invention does not encompass the use of a fixed-frequency external crystal to set the "frequency or rate" of the clock (which, again, is the case here); and (3) their invention does not cover the use of an external crystal to either cause the clock to oscillate or to fix the frequency of the clock (which, once more, is the case here). [JXM-16 ('336 prosec. hist., Feb. 10, 1998 Amend.) at 1-2 (TPL853_02954557-558).]

Second, Complainants' petition asserts that the "disavowal" doctrine is "rarely applicable." [Pet. at 17.] This assertion is belied by the legion of Federal Circuit cases cited above. In any event, regardless of how frequently the doctrine is applied, the above-cited cases mandate its application where, as here, there are repeated express disclaimers, as the ALJ correctly found. [Order No. 31 at 38-40.]

Third, Complainants' petition attempts to create a strawman argument by asserting that the ALJ somehow "latched onto a single isolated phrase in the file history – 'does not utilize external components'" on which to base his construction. [Pet. at 17.] This argument is wrong. While the ALJ correctly cited this ***additional, consistent disclaimer*** in the file history, [Order No. 31 at 38-39], the ALJ also correctly identified, and relied upon, several of the other above-cited disclaimers, including the *applicants' assertions* that (1) the claimed invention does not utilize an external crystal, (2) Magar does not have an "entire oscillator" because it uses an off-chip crystal to cause oscillation, and (3) Magar is distinguishable ***both*** because it uses a fixed frequency crystal ***and*** because it requires an external crystal. [Order No. 31 at 38.] Furthermore, as established above, the file history is replete with additional express disclaimers that support the ALJ's construction.

Fourth, Complainants incorrectly assert in their petition that the "applicants never disclaimed the use of an external crystal/clock generator as a reference." [Pet. at 17.] To the contrary, as established above, the applicants repeatedly made such a clear disclaimer when they repeatedly distinguished Magar on the ground that the fixed-frequency off-chip crystal controls the frequency of the reference clock. [JXM-18 ('336 prosec. hist., July 7, 1997 Amend.) at 2-4; JXM-16 ('336 prosec. hist., Feb. 10, 1998 Amend.) at 1-5 (TPL853_02954557-561).]

Fifth, Complainants' petition tries to resurrect the argument that the applicants distinguished Magar solely because there is allegedly no on-chip clock in Magar and because Magar's clock supposedly was the off-chip fixed-speed crystal which generated the oscillation. [Pet. at 17-19.] While this is one of the arguments that applicants made during prosecution (which resulted in disclaiming the use of an off-chip crystal to cause oscillation), Complainants' argument ignores the applicants' *additional arguments* and express disclaimers to secure their

patent, including: (1) that the components of the Magar clock are both on-chip (the CLOCK GEN circuitry) and off-chip (the fixed speed crystal) and, therefore, that the "entire" clock is not on the chip; (2) that, according to the applicants, even if Magar's off-chip crystal were placed on the chip, Magar still would not anticipate the claimed invention because the invention does not encompass the use of a fixed-speed crystal (whether on or off chip) to control the frequency of the on-chip clock, and (3) the applicants' subsequent repeated statements that the claimed invention does not encompass the use of an external fixed-frequency crystal to set or control the frequency of an on-chip oscillator. [JXM-18 ('336 prosec. hist., July 7, 1997 Amend.) at 2-4; JXM-16 ('336 prosec. hist., Feb. 10, 1998 Amend.)at 1-5 (TPL853_02954557-561).]

Finally, Complainants' petition mischaracterizes the arguments that applicants made when they amended their claims to add the word "entire" to the term "entire oscillator." [Pet. at 19.] As established above, the applicants did not at that time (as Complainants now contend) limit their argument to disclaiming the use of an external crystal to cause oscillation; they instead also clearly and repeatedly disclaimed the use of an external crystal to set or control the frequency of the oscillator. [JXM-16 ('336 prosec. hist., Feb. 10, 1998 Amend.) at 1-5 (TPL853_02954557-561).]

In short, the arguments advanced in Complainants' petition concerning the applicants' disclaimers related to Magar are unavailing. Contrary to Complainants' arguments, the ALJ's construction embodies the applicants' clear disclaimers with respect to the Magar reference because the construction requires that the "entire" oscillator "does not rely on … an external crystal/clock generator to generate a clock signal." [Order No. 31 at 41.] In contrast, Complainants' proposed construction ignores the applicants' disclaimers and cannot, therefore, be correct. *See Abbott Labs. v. Sandoz, Inc.*, 566 F.3d 1282, 1289 (Fed. Cir. 2009) (*en banc*) ("'the

prosecution history can often inform the meaning of the claim language by demonstrating . . . whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be.'") (quoting *Phillips v. AWH Corp.*, 415 F.3d 1303, 1317 (Fed. Cir. 2005) (*en banc*)). As such, the petition provides no basis to disturb the ALJ's construction of the "entire oscillator" limitations of claims 6 and 13.

b. The '336 patent's prosecution history also clearly disclaims reliance on control signals

As the ALJ correctly found, in addition to disclaiming reliance on an external crystal or clock generator, the applicants repeatedly, clearly, and unambiguously disclaimed reliance on control signals to control the oscillator. [Order No. 31 at 39-40.]

The first of these disclaimers occurred in response to the examiner's rejection of the claims in light of U.S. Patent No. 4,670,837 to Sheets ("Sheets"). [RXM-21.] The applicants distinguished their purported invention from microprocessors that rely on frequency control information from an external clock source:

> ***The present invention*** does not similarly rely upon provision of frequency control information to an external clock, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit ***obviates the need for provision of the type of frequency control information described by Sheets . . . Sheets' system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention***.

[JXM-17 ('336 prosec. hist., April 11, 1996 Amend.) at 8 (TPL853_02954574).] Because the applicants referred to the "present invention" in this statement, the disclaimer applies to all claims. *See, e.g.*, *Ballard Med. Prods. v. Allegiance Healthcare Corp.*, 268 F.3d 1352, 1360-62 (Fed. Cir. 2001).

In response to a subsequent rejection, the applicants went even further and disclaimed the use of *controlled* oscillators altogether, regardless of whether the control is on-chip or not:

> Even if the examiner is correct that the variable clock in Sheets is in the same circuit as the microprocessor of system 100, ***that still does not give the claimed subject matter.*** In Sheets, ***a command input is required to change the clock speed.***

[JXM-18 ('336 prosec. hist., July 7, 1997 Amend.) at 4 (TPL853_00002428).] Thus, according to the applicants, simply having a CPU clock on the chip is not enough to meet the claimed invention because ***controlling*** the on-chip ring oscillator's speed using a command ***signal*** "does not give the claimed subject matter." [*Id.*] Indeed, in that same amendment, the applicants left no doubt that, unlike "all cited references," the on-chip oscillator of their purported invention is completely free of inputs and extra components:

> ***Crucial to the present invention*** is that . . . when fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together. ***This differs from all cited references in that . . . the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so.***

[*Id.* at 5 (TPL853_00002429).][10] This prosecution statement confirms the applicants' clear disclaimer of any reliance on control signals (inputs). Hence, the ALJ's construction correctly includes, and Complainants' construction incorrectly ignores, the requirement that the oscillator "does not rely on a control signal . . . to generate a clock signal." *See Am. Piledriving Equip.*, 637 F. 3d at 1336; *Seachange Int'l, Inc.*, 413 F.3d at 1372-75; *Elkay Mfg. Co.*, 192 F.3d at 979.

Complainants again miss the mark regarding the applicants' disclaimer of the use of control signals because their petition simply ignores the full scope of the applicants' disclaimers. In particular, Complainants' petition wholly disregards a key fact: as discussed above, the applicants clearly stated (twice) that even an on-chip variable speed clock does not meet the

[10] When a patentee uses the term "crucial to" or "in the present invention," this use has a special effect on the scope of the claim. *See Microsoft Corp. v. Multi-Tech Sys., Inc.*, 357 F.3d 1340, 1351-52 (Fed. Cir. 2004) (construing claim to require a feature that was "central to the functioning of the claimed invention").

requirements of the claim if a control signal is required to change the frequency of the clock, because the frequency of the claimed variable speed clock instead is determined by the PVT parameters. [JXM-18 ('336 prosec. hist., July 7, 1997 Amend.) at 4-5.] This unrebutted clear disavowal of claim scope not only supports the ALJ's construction, it compels it.

c. The claim language also supports the ALJ's construction

Complainants' petition asserts – without explanation – that "nothing in [the claim] language suggests that CPU/system clock can never use a 'control signal' or an 'external crystal/clock generator.'" [Pet. at 15.] To the contrary, the claim language itself precludes the use of a control signal or an external crystal to fix the frequency of the claimed "entire oscillator."

Claims 6 and 13 expressly require that the "entire oscillator" vary in the same way as the CPU as changes occur in the PVT parameters:

> A microprocessor system comprising: ... an ***entire oscillator*** disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit ***at a clock rate*** and being constructed of a second plurality of electronic devices, ***thus varying the processing frequency*** of said first plurality of electronic devices [*i.e.*, the CPU] ***and the clock rate*** of said second plurality of electronic devices ***in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate*** ...

[JXM-1 at cls. 6, 13.]

Unlike the ***claimed*** "entire oscillator" whose frequency (recited in these claims as the "clock rate") varies because it is determined by the PVT parameters, an oscillator whose frequency is determined by an external crystal is fixed. As a result, that frequency does not (and cannot) vary with changes in the PVT parameters, as is expressly required by each of the asserted claims. [JXM-1, claims 6, 13.] Thus, contrary to Complainants' unsupported assertion, the claim language itself dictates that an oscillator whose frequency is determined by an external

crystal or clock generator falls outside the scope of the claims. *See Phillips*, 415 F.3d at 1314 (explaining that "the context in which a term is used in the asserted claim can be highly instructive" to claim construction).

d. The specification further supports the ALJ's construction

Complainants' petition similarly asserts that the specification "does ***not*** support the additional limitations the ALJ included." [Pet. at 15 (emphasis in original).] But, the ALJ did not "add" any limitation. Rather, the ALJ's construction mirrors the clear-cut teaching of the intrinsic evidence, including the specification, of what the "entire oscillator" is.

The title of the '336 patent is "High Performance Microprocessor Having a ***Variable Speed System Clock.***" Consistent with this title, the specification criticizes prior art solutions that clocked a CPU with a fixed clock, such as, for example, a clock whose frequency is controlled by an external crystal:

> Traditional CPU designs are done so that with the worse [sic] case of the three parameters, the circuit will function ***at the rated clock speed. The result are designs that must be clocked a factor of two slower than their maximum theoretical performance***, so they will operate properly in worse [sic] case conditions.

[JXM-1 at 16:48-53; *see also id.* at 17:12-33.]

Rejecting the prior art fixed-speed clock approach (which is the approach used in the Respondents' accused products), the '336 patent discloses a clock that is completely on the same semiconductor substrate as the CPU and whose speed freely varies with the PVT parameters of the substrate. As the specification explains, the frequency of the allegedly inventive variable speed oscillator is, unlike prior art fixed-speed clocks, determined by the PVT parameters, so that the CPU can always operate at its maximum possible frequency:

> ***The ring oscillator frequency is determined by the parameters of temperature, voltage, and process***. At room temperature, the frequency will be in the neighborhood of 100 MHZ. At 70 degrees Centigrade, the speed will be

> 50 MHZ. ... ***By deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast.***

[*Id.* at 16:54-17:2.] In other words, by insulating its frequency from any outside influence, the "ring oscillator variable speed clock" can vary and drive the CPU to execute at the fastest speed possible. [*Id.* at 17:14-34.] Because the CPU must still communicate with the outside world, the patent discloses the use of an I/O interface which is clocked by an off-chip, fixed-speed crystal clock. [*Id.*] By decoupling the speed of these two clocks and allowing the frequency of the on-chip "ring oscillator variable speed system clock" to vary with the PVT parameters while the I/O interface relies on an off-chip, fixed-speed crystal oscillator, the patent allegedly achieves "optimum performance" under any PVT parameters. [*Id.*]

The only fair reading of the specification leads to only one conclusion: the invention of the '336 patent involved a variable speed system clock that varies with PVT parameters, rather than the prior art's fixed speed clocks which did not vary with the PVT parameters because an external crystal or control signals controlled these fixed speed clocks. Thus, contrary to Complainants' assertion in its petition, the '336 patent specification does not "merely teach[] that the ***system clock*** that clocks the CPU must be ***on the same chip*** as the CPU." [Pet. at 16 (emphasis in original).] Indeed, such architectures were well known in the prior art long before the '336 patent. For example, the Talbot prior art patent that is addressed in the file history discloses a phase-locked loop ("PLL") structure containing an on-chip "oscillator" or "clock." [JXM-13 (U.S. Patent No. 4,689,581 ("Talbot")), 3:1-4 ("As is clear from Fig. 1, all of the components of the timing apparatus 4 are on the single silicon chip and the timing apparatus 4 has been designed such that it does not require any components external to chip 1."), Fig. 1; *see also* RXM-17 (U.S. Patent No. 3,967,104 (issued in June 1976 and cited on the front cover the '336 patent)) at 1:8-12, 12:5-19 and Fig. 4a (disclosing 2-phase ring oscillator system clock on

same single chip as processor).]

In short, the specification criticizes the use of prior art fixed-frequency clocks, such as clocks that include an on-chip oscillator or clock whose frequency is controlled by an external crystal. Instead, the '336 patent proposes the purportedly novel variable speed clock that is dependent on PVT parameters to set the clock's frequency in order to allegedly overcome the perceived deficiencies of the prior art fixed-frequency clocks. The ALJ's construction correctly reflects these express teachings and disclaimers. *Chicago Bd. Options Exch. Inc. v. Int'l Secs. Exch. LLC*, 677 F.3d 1361, 1372 (Fed. Cir. 2012) (finding that "the specification goes well beyond expressing the patentee's preference" and that "its repeated derogatory statements…may be viewed as a disavowal of that subject matter from the scope of the Patents claims."); *SciMed Life Sys. v. Advanced Cardiovascular Sys.*, 242 F.3d 1337, 1341 (Fed. Cir. 2001) (holding "[w]here the specification makes clear that the invention does not include a particular feature, that feature is deemed to be outside the reach of the claims of the patent...."); *Phillips*, 415 F.3d at 1314 (the specification is the "single best guide to the meaning of a disputed term").

Disregarding these central teachings in the specification, Complainants incorrectly assert that nothing in the specification conflicts with an external crystal controlling the frequency of the on-chip oscillator. [Pet. at 16.] However, as established above, utilizing an off-chip crystal to control the frequency of the claimed oscillator is directly contrary to the specification's express teaching that "***[t]he ring oscillator frequency is determined by the parameters of temperature, voltage, and process***." [JXM-1 at 16:54-17:2.] This is particularly true in light of the fact, also established above, that the specification criticizes prior art microprocessors that use a fixed clock to set the frequency of the CPU. [*Id.* at 16:48-53.] Thus, Complainants' analysis of the specification is both incomplete and incorrect.

4. **The district court claim constructions support the ALJ's construction**

Complainants' petition twice cites the claim construction of this claim term issued by the United States District Court for the Northern District of California (Judge Grewal) in litigation between Complainant TPL and respondent HTC. [Pet. at 15 n.15, 21.] This citation is remarkable for at least two reasons, neither of which suggests that the ALJ committed any error in construing this claim term.

First, while Complainants chose to cite Judge Grewal's construction, they fail to mention a prior claim construction issued by the United States District Court for the Eastern District of Texas (Judge Ward). Judge Ward's construction was considered by the ALJ during the *Markman* process in this investigation. [Order No. 31 at 27-29.] Judge Ward construed the claim phrase "entire ring oscillator variable speed system clock in said single integrated circuit" as recited in claim 1 to mean "a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not directly rely on a command input control signal or an external crystal/clock generator to generate a clock signal." [*Id.* at 27.] As with the ALJ's construction, Judge Ward's construction precludes reliance on either a control signal or an external crystal/clock generator to generate a clock signal. [*Id.*] Further, in reaching this construction, Judge Ward explained: "The Court agrees with the defendants that the applicant disclaimed the use of an input control signal and an external crystal/clock generator to generate a clock signal." [*Id.*] This is in accord with the ALJ's findings and conclusion. And contrary to Complainants' current protestations of error, Complainant TPL initially asked the Court in the currently pending HTC District Court litigation to adopt Judge Ward's construction of this claim term. [*Id.* at 28.]

Second, although Complainants assert that the ALJ's claim construction errs by precluding the claimed "entire oscillator" from relying on an external crystal/clock generator to

generate a clock signal, Judge Grewal's claim construction similarly states that the "entire oscillator" of claims 6 and 13 "are properly understood to exclude any external clock used to generate the signal used to clock the CPU." [Pet. at Ex. 2 p. 2.] Thus, the constructions of the ALJ and Judge Grewal are in accord on this issue. While Judge Grewal's claim construction order does not also include a "control signal" limitation, there is no discussion of such a potential limitation in the order and, therefore, there is no basis to address the assessment of what, if any, consideration Judge Grewal gave to that limitation.

In short, there is nothing in either District Court claim construction that points to any alleged error by the ALJ. Rather, if anything, they confirm that the ALJ's construction is correct.

5. **The Accused Products do not practice the "entire oscillator" limitations even under Complainants' construction**

In a single two-sentence paragraph, Complainants' petition asserts that "[o]verwhelming evidence" establishes that this claim limitation is met under Complainants' incorrect construction of the claim term. [Pet. at 21.] Not true. Specifically, even if Complainants' construction of the "entire oscillator" limitation were adopted – which, as established above, it should not be – the accused products still do not practice this limitation for many of the reasons set forth in the ID.

For example, claims 6 and 13 require "an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator ***clocking*** said central processing unit." [JXM-1 at cls. 6, 13.] Thus, regardless of the construction of the "entire oscillator" limitation, the claim language requires that the ***oscillator*** must clock the CPU. In contrast, the controlled oscillators within the accused PLLs are not, by themselves, clocks that provide clocking signals to the CPU. Rather, as established in the ID, the oscillators within the accused PLLs require and rely on an external crystal/clock generator to operate. [ID at 119-122.] Based on the testimony of both sides' experts and the testifying engineers who developed the

accused products, the ID determined that the PLLs in the accused products "***require, and thus rely on***" control signals to generate a clock signal for the CPU. [ID at 119 (citing Tr. (Subramanian) at 1316-32, Tr. (Haroun) at 178-205, Tr. (Kekre) at 228-239, Tr. (Oklobdzija) at 834.] Dr. Oklobdzija's own textbook confirms that a controlled oscillator, if any, in a PLL "generates the internal clock by virtue of a control voltage [*i.e.* control signal] created in response to the external reference." [ID at 120; RX-2283 at Garmin 92907.] The clock signal that is generated is thus a product of both a control signal provided by the PLL and a reference frequency of the external crystal/clock. [ID at 120-121.] Accordingly, as the ID correctly found, "the distributed clocking of all the Accused Products relies on an external crystal." [ID at 121; *see also* ID at 41-56, 58-60, 68-73, 75-82 (summarizing Respondents' arguments and evidence demonstrating that oscillators in the accused PLLs require an external crystal to generate clocking signals).]

In contrast to the accused products' reliance on an external crystal or clock generator, Complainants' proposed construction of the "entire oscillator" limitation requires that the claimed "oscillator" be "located entirely on the same semiconductor substrate as the central processing unit." [Pet. at 21.] Because the accused PLLs use and require an external off-chip crystal/clock generator, the accused "entire oscillators" in the accused products are not located entirely on the same substrate as the accused CPU. Rather, it is undisputed that part of the accused oscillator (*i.e.*, the external crystal or external clock generator) resides off-chip.

C. The ALJ correctly found that the accused products do not meet the "entire oscillator" limitation

1. Review should *not* be granted in response to Complainants' perfunctory assertion that the accused products infringe under the ALJ's claim construction

Complainants summarily assert that they "presented substantial evidence at trial to prove"

infringement of claims 6 and 13 under the ALJ's construction of the "entire oscillator" limitation. [Pet. at 22-23.] However, rather than identify any such evidence or make any argument as to how any such evidence demonstrates error on the part of the ID, Complainants instead make the following remarkable assertion:

> Complainants showed that each of the Accused Products has a ring oscillator that "generates a clock signal" without relying on any "control signal" or "external crystal/clock generator." For purposes of this Petition for Review, **it is not necessary to burden the Commission with that evidence, which is discussed in detail in Complainants' post-hearing briefing.** Complainants can review the evidence of infringement – even under the ALJ's incorrect construction of "entire oscillator" – if the Commission grants review of the ID.

[Pet. at 23.]

Complainants' ***admitted*** failure to present any evidence, facts, or arguments to support their naked assertion that they demonstrated infringement under the ALJ's claim construction fails to establish a basis for Commission review of this issue. Specifically, Commission Rule 210.43(b)(2) requires that "[t]he petition for review must set forth a concise statement of the facts material to the consideration of the stated issues, and must present a concise argument providing the reasons that review by the Commission is necessary or appropriate to resolve an important issue of fact, law, or policy." 19 C.F.R. § 210.43(b)(2). Complainants failed to do this, and their request for review should therefore be disregarded.

Moreover, "petitions for review may not incorporate statements, issues, or arguments by reference." *Id.* Yet, this is exactly what Complainants are effectively doing by vaguely referring to unspecified portions of their post-hearing briefs for support.

Furthermore, the Commission Rules provide that "[a]ny issue not raised in a petition for review will be deemed to have been abandoned by the petitioning party and may be disregarded by the Commission in reviewing the initial determination . . . and any argument not relied on in a

petition for review will be deemed to have been abandoned and may be disregarded by the Commission." *Id.* Having failed to present any evidence or argument to support their position, Complainants have waived their opportunity for review before the Commission or in a later appeal. *See id.*; *see also Broadcom*, 542 F.3d at 900-901 (finding waiver of an argument not raised in a petition of review to the Commission).

For these reasons, the Commission should disregard Complainants' challenge to the ID's exhaustive and well-reasoned conclusion that Respondents' accused products do not meet the "entire oscillator" limitation under the ALJ's correct construction. Furthermore, even if the Commission does not simply disregard Complainants' request for review due to their failure to comply with the Commission's Rules, Complainants' petition fails to present any evidence or argument sufficient to warrant review of this issue.

2. **The ALJ correctly found noninfringement under his proper construction of the "entire oscillator" limitation**

a. Complainants waived any infringement argument under the ALJ's correct application of his claim construction

Complainants' challenge to the finding of noninfringement under the ALJ's construction is narrow: Complainants only assert that the ALJ allegedly "mischaracterized" his own construction of the "entire oscillator" limitation and then allegedly applied that "mischaracterized" and "changed" construction to the accused products. [Pet. at 22-26.]

Significantly, Complainants do ***not*** argue that the accused products infringe if the Commission concludes either that (1) the ALJ did not "mischaracterize" his claim construction or (2) any alleged "change" that the ALJ supposedly made to his construction is correct. As such, Complainants have waived any argument that the accused products infringe under the ALJ's application of his claim construction if the Commission finds that the ALJ neither misapplied the construction nor applied an incorrect construction. *See* 19 C.F.R. § 210.43(b)(2);

Broadcom, 542 F.3d at 900-901.

b. Complainants' arguments are each without merit

Complainants' assertion that the ALJ "mischaracterized" his claim construction and then improperly applied that "mischaracterized" and "changed" construction to the accused products is incorrect for three reasons. [Pet. at 22-26.] First, the ALJ did not mischaracterize his construction. Rather, it is Complainants who fundamentally mischaracterize the ALJ's findings and the facts. The ALJ instead correctly applied his construction to the evidence in a detailed manner and correctly concluded from his analysis that none of the accused products practice the "entire oscillator" limitation. Second, while the ALJ did not change his construction as Complainants assert, the supposed "change" cited by Complainants is in fact a requirement of the claims. Third, Complainants' petition ignores – and leaves unchallenged – the majority of the ALJ's factual findings that lead to the necessary conclusion that the "entire oscillator" limitation is not met under the ALJ's claim construction, even under Complainants' own narrow interpretation of the ALJ's construction. Respondents discuss each of these reasons in further detail below.

i. Contrary to Complainants' mischaracterizations, the ALJ correctly found that setting the frequency of a clock is an inseparable part of clock signal generation

Complainants assert that the ALJ "***equated*** the concept of 'frequency adjustment' with 'clock generation.'" [Pet. at 23; *see also id* at 24 ("equating 'setting a clock's frequency' with 'generating a clock signal' is fundamentally incorrect").] Complainants, however, misrepresent the ALJ's analysis and findings.

When evaluating the "entire oscillator" limitation in the context of the accused products, the ALJ correctly found that setting a clock's frequency is an ***inseparable part of*** generating a clock signal. But contrary to Complainants' suggestion, the ALJ did not conclude that setting the

frequency of a clock comprises the entirety of generating a clock signal. As the ALJ correctly found, based in large part on the testimony of Complainants' own expert (Dr. Oklobdzija) and his textbook on this subject, as well as the confirming testimony of Respondents' expert (Dr. Subramanian), setting the frequency of a clock through the use of an external crystal and control signals is integral to the generation of the clock signal:

> What Dr. Oklobdzija and his fellow authors said in their book coincides with Respondents' argument that the process of setting the frequency of a clock signal and generating ***a clock signal are inseparable, because a clock signal must have a frequency, since its sole purpose is to provide a frequency for timing the operation of device*****s** (*See* RBr. at 70-71 (citing Tr. (Oklobdzija) at 1088)) . . . Dr. Oklobdzija testified that "a clock is a control" and exerts control through repeated, periodic "start, stop, start, stop, and . . . do[es] it a billion times a second." (Tr. (Oklobdzija) at 413(sic) [at 1089].) ***This periodicity is the frequency of the clock signal. In order for a clock signal to carry out its objective, it must have a frequency, which the PLL circuitry sets in reaction to a reference signal from an external crystal or clock generator. The external reference signal is integral to the generation of a clock signal,*** and by acknowledging that the PLL sets the frequency of the VCO in reaction to a reference clock signal from an external crystal or clock generator, Dr. Oklobdzija concedes that the PLL and its components rely on an external crystal/clock to generate a clock signal. [¶] What Dr. Oklobdzija and his fellow authors describe in their book is also consistent with Dr. Subramanian's testimony. (Tr. (Subramanian) at 1304-16) . . .

[ID at 121-122; *see also* ID at 123-124 ("Frequency – and the regulation thereof, which is a form of control – are incidental to clock generation, as Dr. Oklobdzija and his co-authors describe in their textbook, as discussed above."); Tr. (Oklobdzija) at 1089:2-7 ("Q. And the periodicity of start, stop, start, stop, that's frequency; right? A. That is frequency."), 1089:13-1090:5 ("The role of the PLL is to *control the frequency* of the VCO or *set it* in the desired range"), 1091:4-5 ("And that control signal controls the frequency or adjusts the frequency of the VCO.").]

In addition to the above-cited testimony of both sides' experts, Dr. Oklobdzija's own textbook supports, as the ALJ notes, the finding that setting the frequency of a clock through the use of an external crystal and control signals is "inseparable" from and "integral to" the

generation of the clock signal. [ID at 120-122.] This textbook (RX-2283) states that a clock system usually is divided into two distinct categories: ***clock generation*** and clock distribution. [RX-2283 at Garmin 92904; ID at 120.] The textbook teaches that an oscillator, if any, in a PLL ***generates*** a clock signal *in response to* the oscillator's receipt of a control voltage which is in turn created in response to an external reference signal received from an external crystal. [RX-2283 at Garmin 92907; ID at 120.] As the ALJ correctly concluded from the teaching of Dr. Oklobdzija's textbook, "[t]he clock signal that is generated is a product of a control signal provided by the PLL and the reference frequency of the external crystal/clock." [ID at 121.] In short, as the ALJ accurately found, setting the frequency of a clock is not only part of generating a clock signal—it is integral to the generation of a clock signal.

Notwithstanding the clear-cut evidence provided by Dr. Oklobdzija and Dr. Subramanian and the express teachings of Dr. Oklobdzija's textbook, Complainants attempt to pry open a hole for their infringement argument by asserting that "[f]requency is a ***characteristic*** of a clock signal – it is not the same as a clock signal." [Pet. at 24 (emphasis in original).] However, Complainants never even attempt to explain how clock signal generation can be separated or somehow distinguished from setting the frequency of the clock. They cannot, as the ALJ found in the above-quoted passage from the ID. [ID at 121-122.] Nor do Complainants attempt to explain what, if anything, would remain of a clock signal if, as they contend, the frequency of the signal (*i.e.*, its periodicity) somehow could be segregated from the "rest" of the signal. Thus, although Complainants proclaim that "[t]he clock signal and its frequency are distinct concepts," [Pet. at 25], they never explain how this is true or what, if anything, a clock signal could possibly be once stripped of its frequency.

Indeed, Complainants' own cited evidence confirms that the frequency of the clock signal

is part and parcel of what is generated by the oscillator. [Pet. at 24 (quoting Dr. Subramanian (at MTr. 35:8-36:15) as stating that "a clock signal is a signal that is, essentially, a periodic signal . . . these pulses coming at a regular interval spaced out over time . . . And so we could figure out the frequency by counting how many times it oscillates between zero and one in a given second"); *see also* Pet. at 25 (quoting Dr. Oklobdzija's testimony (at Tr. 1092:17-1093:19) that a "dead" oscillator "doesn't generate any frequency," and that the frequency must first be "generated" before it can be regulated, without explaining how the frequency is initially generated apart from the process of generating the clock signal).]

Struggling to find any ground for argument, Complainants also cite the unremarkable fact that (unlike the clocks in the accused products) some clocks are designed to generate clock signals with different frequencies. [Pet. at 24-25.] But this fact does nothing to separate the "clock signal" from its "frequency," because regardless of the frequency of the clock signal, the signal has a frequency and the signal, including its frequency, are generated together.

Complainants' final effort to find separation between the generation of a clock signal and its frequency fares no better. Specifically, Complainants point to the fact that both the specification and the claims separately recite the "clocks" and "oscillators," on the one hand, and their "frequency" or "rate," on the other hand. [Pet. at 25-26.] But the distinction there is between the physical component (the clock or oscillator) and what it generates (a clock signal having a frequency or rate). While this distinction is correct, it is wholly irrelevant to the issue at hand, namely whether the generation of the "clock signal" of the ALJ's claim construction can be segregated from generating its frequency. As established above, and as the ALJ correctly found, it cannot.

The "entire oscillator" limitation requires that the on-chip oscillator "***not*** rely on a control

signal or an external crystal/clock generator to generate a clock signal." [Order No. 31 at 41.] As established by the evidence presented to the ALJ, all of the accused products rely on control signals and either on an external crystal or an external clock generator to generate the frequency of the oscillator. As the ALJ correctly found, this is an integral part of generating the clock signal.[11] [ID at 119-124.]

ii. Complainants also mischaracterize the ALJ's findings regarding control signals

The petition asserts that the ALJ applied his construction in a manner that would preclude reliance on a control signal for "any purpose," rather than, as the claim construction states, precluding reliance on a control signal to generate a clock signal. [Pet. at 22.] Other than repeating their false distinction addressed above between generating a clock signal and its frequency, Complainants cite no instance of the ALJ actually relying on any control signal that does anything other than generating a clock signal. [*Id.*] Thus, there is no error.

iii. The alleged "change" in the ALJ's claim construction is in fact a claim requirement

Complainants contend, incorrectly, that the ALJ effectively revised his construction to read: "an oscillator that is located entirely on the same substrate as the central processing unit

[11] Complainants' argument regarding frequency control suffers from the further defective assumption that a clock signal is "generated" once and that thereafter the "frequency" of that once-generated signal is "regulated." [Pet. at 24-26.] However, the process of generating a clock signal and its frequency is not a singular event that occurs once during the existence of the signal. Rather, the clock signal and its frequency is being generated the entire time that it exists. [*See* Tr. (Oklobdzija) at 1089:2-4 (explaining that a clock signal starts and stops a billion times a second); ID at 119-120.] In this sense, the signal is similar to electricity produced by a generator: the electricity is not generated *only* in the split second when the generator first starts to run. Rather, the generator *continuously* generates the electricity. In the same way, the process of generating the clock signal and its frequency does not occur only in the split second when the VCO first starts. Rather, the clock signal is being generated during the entire time that the PLL is outputting the clock signal to the CPU. Thus, the purported distinction between a one-time clock signal "generation" and its subsequent "regulation" is false.

and does not rely on a control signal or an external crystal/clock generator ***to set or adjust the frequency*** of a clock signal." [Pet. at 23 (emphasis in original).] While the ALJ made no such change to his construction, it is in fact correct that the claimed "entire oscillator" ***cannot*** rely on a control signal or an external crystal/clock generator to set or adjust the frequency of a clock signal, because the applicants, as established above, expressly disclaimed such an oscillator during the prosecution of the '336 patent. *See* Part V.B, *supra*. Thus, even if the ALJ had made such a change to his construction (which he did not), that change would have been correct.

iv. Complainants ignore the ALJ's unchallenged findings that the accused products rely on external crystals and control signals to cause the on-chip oscillators to oscillate

Complainants' challenge to the ALJ's application of his construction of the "entire oscillator" limitation to the accused products is narrow and only attacks the part of the ALJ's analysis directed to generating and controlling the frequency of the clock signal. [Pet. at 22-26.] This singular focus ***entirely ignores*** the ALJ's further findings that control signals and external crystals in the accused products cause the on-chip oscillator to oscillate. [ID at 125-132 (detailed findings that the oscillators in the accused products do not oscillate without the required control signal),122 ("Beyond that, Dr. Subramanian additionally testified that there are control signals within the accused PLLs themselves that are used to control the oscillation of the oscillators"), 124 ("The evidence shows that the oscillators in all of the Accused Products rely on control signals from with the PLL (Tr. (Subramanian) at 1316-32), and on an external crystal/clock generator to generate a clock signal (Tr. (Subramanian) at 1304-1316)"), 124 ("The fact remains, all of the 'entire oscillators' in the Accused Products rely on control signals and external crystal/clock generators to generate clock signals").]

Complainants do not challenge ***any*** of these separate findings, nor do Complainants

disagree that one aspect of generating a clock signal in the accused products is causing the oscillators to oscillate. [Pet. at 6.] Accordingly, these unchallenged findings – which do not turn in any way on the distinction between generating a clock signal and its frequency that Complainants falsely assert underlie the ALJ's findings – establish that the accused products do not practice the "entire oscillator" limitation because the products ***do*** "rely on a control signal or an external crystal/clock generator to generate a clock signal." [Order No. 31 at 41.]

For all of these reasons, Complainants have not shown any legal error or clear error of fact that justify review or disturbance of the ALJ's correct construction and correct findings.

VI. THE "VARYING" LIMITATION OF CLAIMS 6 AND 13

Claims 6 and 13 require the claimed oscillator's frequency to vary as a function of variations in fabrication process, voltage or temperature ("PVT"):

> ***varying*** the ***processing frequency*** of said first plurality of electronic devices [*i.e.*, the CPU] and ***the clock rate*** of said second plurality of electronic devices [*i.e.*, the entire oscillator] in the same way ***as a function of*** parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said ***processing frequency*** to track said ***clock rate*** in response to parameter variation.

[JXM-1 at cls. 6 & 13.] Because the parties did not dispute the meaning of the phrase "varying … as a function of," the ALJ did not construe this term.[12] Accordingly, Complainants' petition is not challenging a legal issue with respect to this term, but is instead attacking the ALJ's factual findings for this limitation.

In their petition, Complainants abandoned the numerous infringement theories about

[12] During the *Markman* process, the parties disputed the meaning of the phrase "varying … in the same way" in claims 6 and 13, with Complainants arguing that this phrase did not need construction. [Order No. 31 at 57-67.] In his *Markman* order, the ALJ adopted Complainants' position by giving this phrase its plain and ordinary meaning. [*Id.* at 67-68.] Although claim phrases "varying … in the same way" and "varying … as a function of" share the same word "varying," they are different and involve distinct issues. Complainants' petition only seeks review of the ALJ's factual ruling on the phrase "varying … as a function of."

frequency variations that they presented at the hearing (including the concept of "jitter," discussion of PVT in various technical documents, the DVFS feature and the so-called "dead band" phenomenon) in favor of a single theory: binning. [Pet. at 26-35.] Complainants argue that the processes used to fabricate semiconductor chips can give rise to differences in processing frequency *capability* from chip to chip, and that such differences necessarily result in the performance variations required by the claim language. [*Id.* at 26-30.] For the reasons set forth below in Part VI.A., *infra*, Complainants are wrong.

As a second angle of attack, Complainants emphasize the disjunctive in claims 6 and 13 with respect to the types of parameter variations listed in the claims (*i.e.*, "one or more fabrication or operational parameters"), and contend that the ALJ erred by failing to conclude that fabrication variation alone suffices to satisfy their burden of proof even if this variation does not occur or affect the chip's operation. [*Id.* at 30-34.] As discussed in Part VI.B., *infra*, Complainants are wrong again.

A. Complainants' argument based on binning is misplaced

1. Binning relates to maximum processing frequency *capability*

To see the flaw in Complainants' argument, it is important to understand at the outset what "binning" is. Because semiconductor fabrication is an imprecise process, a chip manufacturer "cannot fabricate them exactly to the [sic] specs." [Tr. (Oklobdzija) 300:12-13.] As a result of these fabrication variances, chips will exhibit different characteristics, including different processing frequency capabilities. [*Id.* 300:14-16; Tr. (Subramanian) 1264:5-9.] In the consumer electronics device industry, a chip with a higher maximum processing frequency capability (*e.g.*, 1.2 GHz) can potentially command a higher price than a chip with a lower maximum processing frequency capability (*e.g.*, 1.0 GHz). [Tr. (Subramanian) 1265:4-18; *see also* Tr. (Oklobdzija) 300:17-22.] Since processing frequency capability differs from chip to

chip, the chip manufacturers – which are all overseas[13] – use a standard industry practice called "binning" to sort chips with higher processing frequency capability from chips with lower capability. [Tr. (Subramanian) 1264:11-18; RDX-4.108.]

To perform binning, the manufacturers "use a giant tester, a high-precision tester, to test what's the maximum frequency capability, or at least some indicator thereof, of a given chip." [Tr. (Subramanian) 1264:19-23; *see also id.* 1266:12-14 ("Well, testers are big machines that are used to test chips or test various things.").] In this binning process, the testing equipment does not measure the processing frequency capability of the CPU or any clocking circuit associated with the CPU; the testers instead assess the "maximum possible operating capability" of "test circuits that will be placed on the sides of a chip that allow you to figure out a representative [sic] of how the chip works." [*Id.* 1266:14-23.] Based on the results of these characterization tests, the manufacturers then physically place the chips into different buckets, or "bins," noting "[t]his one is fast, this one is slow." [Tr. (Oklobdzija) 879:8-880:18.] After proper packaging, the chip supplier can potentially sell the chip in the "fast" bin for a higher price than the chip in the "slow" bin depending on the fixed clock rate set by the manufacturer. [*Id.* 881:1-6; Tr. (Subramanian) 1265:4-10.]

Critically, the binning process sorts individual chips based on the *maximum* processing frequency at which a chip is *capable* of operating and has nothing to do with the *actual*

[13] The binning process, by Dr. Oklobdzija's own admission, occurs exclusively overseas. [Tr. (Oklobdzija) 879:3-20.] It does not take place at the time of importation or even when the chips are in this country. Complainants' reliance on the overseas binning process is legally insufficient to show a violation of Section 337. *See Certain Electronic Devices with Image Processing Sys.*, Inv. No. 337-TA-724, Comm'n Op., 2012 WL 3246515 (Dec. 21, 2011) ("We also interpret the phrase 'articles that – infringe' to reference the status of the articles *at the time of importation.* Thus, infringement, direct or indirect, must be based on the articles as imported to satisfy the requirements of section.").

frequency and clock rate at which a chip operates. [Tr. (Subramanian) 1264:5-1265:10.] In other words, the binning process only relates to a chip's *maximum* processing frequency *capability*, not its actual processing frequency when it operates. [*Id.* 1264:19-1265:18; *see also id.* 1271:21-25 ("[P]rocessing frequency capability is the maximum frequency at which you can run a part.... Processing frequency is the frequency at which you're running the part.").] Even Complainants' expert agreed, recognizing that "binning ... comes when you are selecting chips of different *capabilities*, meaning VCO and the CPU are slower or faster and you bin them in different things." [Tr. (Oklobdzija) 1030:18-21; *see also id.* 300:20-21 ("So we'll sell them [the chips] out according to their *ability* to run.").] Based on the undisputed evidence, the ALJ correctly found that "binning is a reflection that variations exist in the performance *capabilities* of microprocessors." [ID at 209.]

2. **Maximum processing frequency *capability* is irrelevant to claims 6 and 13 and does not reflect the actual processing frequency or clock rate in the accused products**

While a chip may end up in one bin or another based on binning tests, variation in the chip's maximum processing frequency *capability* is not what claims 6 and 13 require. Nor is the *maximum* processing frequency capability the *actual* processing frequency at which the chip operates in the accused products. Because Complainants' focus on binning alone concerns only processing frequency *capability*, which is irrelevant to claims 6 and 13, their argument fails.

First, claims 6 and 13 require that both (1) the *actual, or operational*, processing frequency of the claimed CPU, not its *maximum* possible frequency capability, and (2) the *actual* clock rate of the oscillator, not its *maximum* possible clock rate, vary as a function of one or more PVT parameters. [Tr. (Subramanian) 1272:5-8 ("to prove the claims, besides all the other requirements of the claims, the clock in question has to move with PVT, which in turn affects the actual processing frequency"); *see also* JXM-1 at cls. 6 & 13 ("*varying* ... the clock rate of said

second plurality of electronic devices in the same way *as a function* of [PVT] . . . thereby enabling said processing frequency to track the clock rate *in response to* [PVT]").][14] If the inventors wanted to claim variation in the maximum processing frequency, they knew how to do so, as shown by claims 1 and 11. [JXM-1 at cls. 1 & 11 (requiring variation in "a processing frequency capability of said central processing unit" separately from variation in the "speed of said ring oscillator variable speed system clock"); *see also* ID at 210 ("Processing frequency capability is the maximum frequency at which a part can run, but that is not the actual frequency at which the part operates.").] Rather than requiring variation in "processing frequency *capability*" of the CPU, claims 6 and 13 call for variation in the CPU's *actual* operating speed by reciting "said central processing unit operating at a processing frequency" and "thus varying the processing frequency." [JXM-1 at cls. 6 & 13 (Reexam. Cert. at 2:15-23 and 3:31-39); Tr. (Subramanian) 1271:20-25 (explaining that processing frequency capability is the maximum frequency at which a part can run, while the speed at which the part actually runs is its processing frequency).] Contrary to Complainants' position that claims 6 and 13 do not require the frequency of the CPU to vary during operation, [Pet. at 27], the claims require exactly that.

By ignoring this fact, Complainants repeat the same analytical error that their expert committed during the hearing, and which the ALJ properly rejected. [ID at 210 ("But Dr. Oklobdzija, in his analysis, focuses on the clock's capability rather than its actual speed.").] For this reason, Complainants cannot establish infringement by showing variations in the *maximum* possible processing frequency, or processing frequency *capability*, even if "the processing frequency *capability* is indeed dependent on PVT" as the experts agree. [ID at 211 ("Succinctly

[14] According to Dr. Oklobdzija, because the CPU operates at a processing frequency determined in part by the rate, or speed, of the clock signal output by the oscillator, the actual processing frequency of the CPU is dependent on the actual speed of the oscillator.

put, a part's processing frequency capability may change with PVT, but its actual speed, or processing frequency, remains constant."); *see also* Tr. (Subramanian) 1121:18-25, 1213:15-20, 1272:1-8.] To satisfy the "varying" limitation in claims 6 and 13, Complainants must show that the *actual* processing frequency and the *actual* clock rate vary as a function of PVT, and they have not done so. [ID at 210-211.]

Second, when integrated into the accused devices, the chips provided by [redacted] do not operate at their maximum processing frequency capability. Instead, each chip is set at a fixed processing frequency based on worst-case scenario parameters and well below the maximum frequency capability identified by the binning process. [Tr. (Subramanian) 1265:22-23 (explaining that each chip is set at a fixed frequency based on worst-case scenario parameters), 1266:1-9 (explaining, *inter alia*, that "it turns out it depends on the customer -- to fix the frequency at a value below the worst case").] Hence, at the time the chips are integrated into mobile products overseas, they run at a fixed frequency. [*Id.* 1266:5-8 ("And just as importantly with respect to this court, all of that, it is a *fixed-frequency chip* when it crosses the border and enters the United States.").] And when these accused mobile products are imported, their chips also operate at a fixed processing frequency, not at the theoretical maximum processing frequency capability identified by the binning process. [*Id.; see also id.* 1267:8-10 ("from that point on, it's a fixed-frequency chip, and when it enters the U.S., it's fixed-frequency").] The binning process, therefore, does not affect the operational processing frequency of the chip (or its entire oscillator, if any) as integrated in the accused devices.

Because binning only characterizes a chip's maximum processing frequency *capability* without shedding any light on the oscillator's *actual* operating processing frequency, binning does not, and cannot, provide evidence relevant to claims 6 or 13. The ALJ understood this key

point and correctly found that binning is not evidence relevant to the asserted claims:

> As for Dr. Oklobdzija's assertion that binning is evidence of variations due to manufacturing process, the Administrative Law Judge concludes that while binning is a reflection that variations exist in the performance capabilities of microprocessors, this does not constitute evidence that any of the Accused Products meet the 'varying' limitations of the asserted claims.

[ID at 209 (internal citation omitted).] Therefore, the ALJ's correct finding that binning is irrelevant to claims 6 and 13 does not warrant review.

3. Complainants' other evidence regarding maximum processing capability is equally irrelevant

Because the claims focus on *actual* processing frequency (*i.e.*, clock rate), rather than processing frequency *capability*, Complainants' heavy reliance on Dr. Subramanian's testimony about binning and on the book chapter by Boning & Nassif is misplaced. [Pet. at 28-29.]

The testimony of Dr. Subramanian that Complainants' petition so prominently quotes and cites actually reinforces the key point found by the ALJ: binning is irrelevant to the infringement analysis at hand. [*See id.*] In this testimony, Dr. Subramanian was very specific that fabrication processes cause variations in the chip's processing frequency capability, *i.e.*, its *maximum* achievable processing frequency. [*Id.* (quoting Tr. (Subramanian) 1122:1-1123:7 (discussing the effect of process on an integrated circuit's "maximum achievable performance"); citing *id.* 1121:18-25 (also discussing "maximum achievable performance"); quoting *id.* 1263:23-1265:18 (explaining binning)).] Dr. Subramanian's testimony about binning was therefore not addressing a chip's actual processing frequency, much less a PLL's actual fixed clock frequency.

The same point is true for the chapter authored by Messrs. Boning and Nassif on which Complainants rely. [Pet. at 29.] Not only is this chapter "a theoretical paper using statistical modeling," [ID at 205], but it relates to variations in *maximum possible* speed related to PVT parameters. [CX-154; RDX-4.104; Tr. (Subramanian) 1253:19-1255:6 (explaining book

chapter).] Variations in processing frequency capability do *not*, however, necessarily translate into variation in actual processing frequency or clock speed. [*Id.* 1254:12-16.] Again, this distinction is critical because variation in actual processing frequency and actual clock speed is what the asserted claims require. [*Id.*]

Overlooking this critical distinction, Dr. Oklobdzija "ignor[ed] the circuits that basically prevent that variation from doing anything." [*Id.* 1254:16-1255:4.] This circuit is the PLL. [*Id.* 1255:10-12, 1273:13-17 ("The reason it's flat is we use PLLs to prevent processing frequency from varying with processing frequency capability. And as a corresponding result, processing frequency does not vary with PVT.").] By its very nature and design, a PLL outputs a very stable and fixed frequency. [*Id.* 1213:5-10; RDX-4.94; ID at 194.] To achieve this stability, the PLL precisely controls and fixes its components' output frequency by continuously comparing this output against an accurate and fixed reference signal provided by an external crystal or clock generator. [*Id.* 1212:23-1213:14; RDX-4.94.] The PLL's ability to provide a fixed and stable processing frequency and clock speed is analogous to a car's cruise control, which maintains a car's speed regardless of environmental conditions. [Tr. (Subramanian) 1214:14-19; RDX-4.95.] For example, a cruise control set to run at 55 miles per hour will maintain this fixed speed regardless of whether the car is going uphill, downhill, or on a flat surface. [*Id.* 1214:21-25.] Like a cruise control, the PLL compensates for any PVT effects on its transistors and circuitry, thus resulting in a fixed speed processing frequency and a fixed-speed clock like the fixed-speed prior art discussed in the patent. [*Id.* 1213:21-25.]

Third party witnesses, including a subpoenaed TI witness and one of the named inventors, corroborated Dr. Subramanian's explanation about the PLL's function. [redacted], a third party witness from [redacted] who testified pursuant to a subpoena from

Complainants, confirmed this key feature of PLLs when he stated that [redacted] [Tr. ([redacted]) 195:17-24.] Leaving no possible doubt, [redacted] further testified that [redacted] [*Id.* 201:24-202:3.] As he also emphasized, [redacted] [*Id.* 202:4-5.] And because of this desire for a stable frequency, [redacted] [*Id.* 203:5-12.]

Consistent with Dr. Subramanian and [redacted] named inventor Russell Fish also confirmed that a PLL, a fixed-speed clock, is fundamentally inconsistent with the variable-speed clock of the '336 patent:

> Q. And just to confirm, if one were to time their CPU using a PLL-based frequency synthesizer as we've defined it, that would defeat the purpose of the '336 patent. Correct?
> A. That is correct.

[RX-167C (Fish Depo.) at 237:5-14; *see also id.* 231:12-232:7 (confirming that using a PLL to clock a CPU "would defeat the purpose of the variable speed timing described in the '336 patent" because the purpose of the PLL is "to not vary").]

In disregarding the PLL and its effect on processing frequency and clock rate, Complainants and their expert fail to recognize that, although PVT parameters affect individual transistors' maximum speed, the PLL prevents PVT variation from influencing either the actual speed of the PLL and its incorporated oscillator (if any) or the actual processing frequency of the CPU. [ID at 211 ("While the oscillators in the PLLs of the Accused Products are capable of variable frequencies in response to PVT factors, nevertheless, they are constrained to provide

fixed clocking signals to the CPU and the claimed first and second plurality of electronic devices."); *see also* Tr. (Subramanian) 1214:7-17.] To accomplish this, the PLL generates a fixed-speed clock signal with a frequency *below* the chip's maximum processing frequency capability. [*Id.* 1295:7-24.] Not only is the actual clock rate in operation below the chip's maximum processing capability, but the PLL fixes the processing frequency at a point below the *worst case* conditions. [*Id.* 1265:22-23, 1266:5-9.] For example, [redacted] [Tr. (Subramanian) 1262:16-1263:7; Tr. (Oklobdzija) 877:6-878:2.] It is at this lower fixed-speed, not at its maximum processing capability, that the chip will operate regardless of binning or any other variation in PVT.

The ID understood the flaw in Dr. Oklobdzija's disregard for the PLL and rebuked Complainants for their improper use of binning as evidence of infringement. [ID at 209 ("Once again, Dr. Oklobdzija and Complainants apply the 'varying' limitation in a hermetic fashion as though an oscillator having a power source is the claimed 'entire oscillator' and it does not matter that the frequency of the oscillators in the Accused Products are fixed, both internally and externally.").] Because the accused products use a PLL to ensure that the actual clock rate of the alleged oscillators does not vary with PVT, the ID correctly concluded that "this argument [regarding binning] is found to be erroneous." [*Id.*] Therefore, the ID correctly rejected Complainants' arguments.[15]

[15] The petition also suggests that claims 6 and 13 are met because the CPU's processing frequency and the oscillator's clock rate always vary "in the same way." [Pet. at 30.] Complainants again conflate two separate and distinct claim requirements. These claims, by their plain language, require at least three things: (i) that the CPU's processing frequency must vary as a function of one or more PVT parameters; (ii) that the oscillator's clock rate must vary as a function of one or more PVT parameters, and (iii) that the CPU's processing frequency and

B. The claimed speed/frequency variation must occur during chip operation

In his carefully crafted and thorough ID, the ALJ found that Complainants did not show that any accused products satisfy the "varying" limitations of the asserted claims. [ID at 189-213.] Having had the opportunity to observe the live testimony of both sides' experts, he found that Complainants' expert lacks credibility, while finding Respondents' expert "to be verifiable and reliable." [ID at 189-192 (discussing Dr. Oklobdzija's inconsistent testimony and noting that the testimony "raises genuine questions about the degree of Dr. Oklobdzija's independence and about his sincerity and veracity") and 201 ("The Administrative Law Judge finds Dr. Subramanian's testimony to be verifiable and reliable.").] The credibility gap between the two experts was readily apparent when contrasting Dr. Subramanian's testimony and the unrebutted empirical evidence on the "varying" limitations against the "a priori opinions of Dr. Oklobdzija" about the alleged variations in the accused chips. [*Id.* 192-193.] Notably, the ALJ's ruling on the "varying" limitations did not merely rest on Complainants' failure of proof; he found that "Respondents' evidence, irrespective of the failure of Complainants' evidence to show otherwise, affirmatively shows that none of the Accused Products infringes any of the asserted claims with respect to the 'varying' limitations." [*Id.* at 196.] This finding, as well as the underlying evidence, confirms that Complainants' petition is without merit.

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the oscillator's clock rate must vary in the same way. [JXM-1 at cls. 6 & 13.] To meet their burden for infringement, Complainants must show that every limitation is present in the accused products. *Revolution Eyewear, Inc. v. Aspex Eyewear, Inc.*, 563 F.3d 1358, 1369 (Fed. Cir. 2009) ("Literal infringement requires that the accused device literally embodies every limitation of the claim."). Thus, Complainants must show not only "varying … in the same way," but also that PVT causes the variation in the CPU's processing frequency and in the oscillator's clock rate. However, as established above, neither the oscillator's clock rate nor the processing frequency of the CPU vary with PVT. Accordingly, by focusing on only part of the claim limitation and ignoring other explicit claim requirements, Complainants fall far short of meeting this burden.

Unable to overcome Respondents' compelling empirical evidence,[16] Complainants argue that this evidence and the ALJ's related findings are allegedly irrelevant to the "fabrication" parameter of claims 6 and 13. Complainants perform this misleading legerdemain by first re-characterizing the empirical evidence, Dr. Subramanian's testimony, and the ALJ's findings as being related to the PLL's "operations." [*E.g.,* Pet. at 34 ("But these tests are utterly irrelevant to 'varying' based on semiconductor fabrication parameters, and the Commission can ignore this entire section for the ID for purposes of this Petition." (emphasis omitted)); *see also id.* at 30-34.] Seizing on the claims' distinction between the "fabrication" parameter and "operational" parameters, Complainants then argue that reliance on fabrication parameters somehow gives them leave to disregard all evidence related to the chips' operation. [*Id.* at 33 ("Dr. Subramanian's testing and testimony that the 'operational frequencies of the chips' are fixed is irrelevant; claims 6 and 13 do not require 'varying' based on 'operational parameters.'" (emphasis omitted)).] The Commission should not be misled by this plainly incorrect argument.

1. The limitation "as a function of [fabrication] parameter variation" in claims 6 and 13 must occur during operation

Complainants use a lot of color coding, italics, and bolding to argue that any variations related to fabrication process satisfy claims 6 and 13, even if these variations "do[] ***not*** cause changes to the frequency of the chip ***during operation.***" [*Id.* at 32 (emphases in original); *see also id.* at 27 (arguing that fabrication "does ***not*** result in changes in the frequency or the clock rate of the "entire oscillator" ***during operation*** – nor do claims 6 and 13 require operational varying" (emphasis in original)), 34 ("***not*** within the same chip ***during operation***" (emphasis in

[16] As the ID noted, Complainants did not offer their own empirical measurements, preferring to make "criticisms of the methodology by which Dr. Subramanian derived the data." [ID at 193.] The ID carefully considered these criticisms and methodically rejected each of them. [*Id.* at 196-204.] Complainants' decision not to challenge these findings confirms that the ALJ was correct in his assessment.

original)).]

Complainants' multi-color highlights and flurry of emphases advance a misleading word play that conflates "operational" with "operation." "Operational," as used in claims 6 and 13, is a simple adjective that describes certain types of parameters, like voltage, that are associated with the functioning of the chips. This adjective does not by itself exclude consideration of the chips' operation with respect to other parameters. To the contrary, the claims and the specification, as discussed below, require that the claimed variation in the processing frequency of the CPU and in the oscillator's clock rate must occur during the chip's operation.

The plain language of the claims, stripped of Complainants' distracting colors and emphases, makes clear that the claimed variation in the oscillator's frequency and the CPU's clock rate must occur during the operation of the chip. This requirement is apparent from the use of "processing frequency" and "clock rate" in the claim language to indicate actual speed in operation: "varying the *processing frequency* of said first plurality of electronic devices and the *clock rate* of said second plurality of electronic devices in the same way as a function of [PVT] ... thereby enabling said *processing frequency* to track said *clock rate* in response to said parameter variation." [JXM-1 at cls. 6 & 13; *see also* Tr. (Subramanian) 1272:1-8 ("to prove the claims, besides all the other requirements of the claims, the clock in question has to move with PVT, which in turn affects the *actual* processing frequency").] If there is any doubt left, the other parts of the claims would dispel it, because the varying "processing frequency" in this disputed limitation refers back to the CPU's "operating" frequency: "said central processing unit operating at a *processing frequency* and being constructed of a first plurality of electronic devices." [JXM-1 at cls. 6 & 13 (first clause).] And comparison with other claims, including previously-asserted claims 1 and 11 which use the distinct term "processing frequency

capability" instead of the term "processing frequency" used in claims 6 and 13, shows that the claimed variations in processing frequency and clock rate refer to actual changes that occur during operation rather than to the theoretical capacity of the chips. [*Compare* cls. 6 & 13 (using "processing frequency") *with* cls. 1 & 11 (using "processing frequency capability").]

Complainants' own petition admits that the two terms "processing frequency" and "clock rate" refer to the frequency of the CPU and entire oscillator *during operation*. As Complainants recognize, the claimed "processing frequency" of the CPU is the actual speed at which the CPU operates. [Pet. at 31 ("The CPU has a 'processing frequency' which is *the speed at which it runs*." (color highlights omitted)).] If the claimed variations did not need to occur during operation as Complainants posit, the claim language would have no need to use a term referring to "the speed at which [the CPU] runs." Likewise, the oscillator's clock rate is the frequency that drives the CPU. [*Id.* ("The entire oscillator also has a 'clock rate,' which is the frequency of the clock signal that it provides to the CPU.").] If the actual operation of the clock is irrelevant to the claims as Complainants argue, then the entire oscillator would not need to provide any clock signal to the CPU. Hence, Complainants' own statements confirm that the claimed variations in frequency must occur during chip operation.

The specification of the '336 patent – especially the passage quoted by Complainants – further confirms this understanding of the claims and shows that processing frequency/clock rate variations occur during chip operation. Indeed, the two sentences quoted in Complainants' petition use the verb "operate" no less than three separate times to describe the effect of poor fabrication process on the CPU in microprocessor 50 and on the ring oscillator clock 430:

> For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor 50 will **operate** slower than normal. Since the microprocessor 50 ring oscillator clock 430 is made from the same transistors on the same die as the latches and gates, it too will **operate**

> slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic **to operate** properly.

[JXM-1 at 17:2-10 (quoted in Pet. at 32).] As this passage explains, poor fabrication process causes the microprocessor of the '336 patent to "operate slower than normal" and the ring oscillator clock to "operate slower (oscillating at a lower frequency)." [*Id.*] Other parts of the specification similarly discuss variations in clock speed during chip operations:

> The microprocessor 50 provides a dual-clock scheme as shown in FIG. 17, with the CPU 70 **operating** a synchronously to I/O interface 432 forming part of memory controller 118 (FIG. 2) and the I/O interface 432 **operating** synchronously with the external world of memory and I/O devices. The CPU 70 **executes** at the fastest speed possible using the adaptive ring counter 20 clock 430. *Speed may vary by a factor of four depending upon temperature, voltage, and process*. The external world must be synchronized to the microprocessor 50 for **operations** such as video display updating and disc drive reading and writing.

[*Id.* at 17:14-25.] As this passage indicates, PVT parameters cause variations in the actual operating speed of the '336 patent's microprocessor's CPU and the I/O interface as the chip performs operations such as video display and disc drive reading and writing. [*Id.*] Consequently, the written description, like the claim language, undercuts Complainants' misleading suggestion that frequency variations do not need to occur during operation.

Complainants cannot overcome their proof problem by relying on an alleged "permanent characteristic of different chips in the same fabrication batch." [Pet. at 27.] Nor can they create the illusion of clear error where there is none. [*Id.* at 33-34.]

2. Empirical evidence confirms that the processing frequency does not vary as a function of PVT

Complainants ginned up their false distinction between "operation" and "operational" to hide the devastating effect of Dr. Subramanian's empirical evidence and to compensate for their own failure to present any empirical evidence. Complainants had ample time before filing their complaint to perform measurements. They also had ample opportunity during discovery to run

these tests. In fact, they demanded and obtained samples of accused products from each Respondent and could have bought additional products on the open market if they needed more samples. Their own expert even wanted to perform such tests. [Tr. (Oklobdzija) 980:11-981:22.] With both the incentive and the opportunity to perform these tests, Complainants did not perform a single measurement.

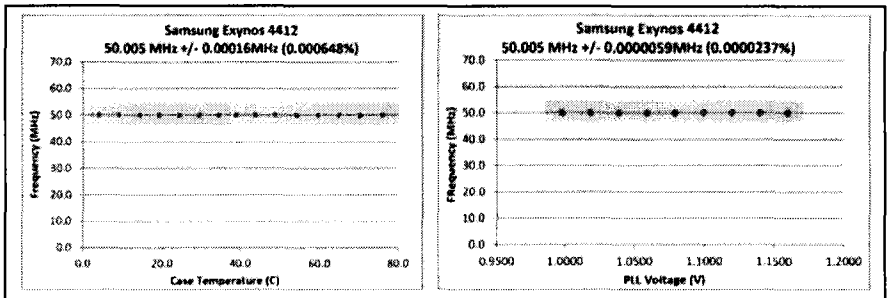
Their failure leaves Dr. Subramanian's measurements as the only empirical evidence in the record, and this evidence is fatal to Complainants' case as the ALJ recognized. [ID at 209 ("Dr. Subramanian's testimony and the testing it was based on empirically demonstrate that the operational frequencies of the chips, no matter their individual differences are fixed.").] By working with an engineer at a testing facility to measure PLL clock rate in a few accused chips,[17] [Tr. (Subramanian) 1252:1-14], Dr. Subramanian gathered evidence clearly demonstrating that PLLs do not vary as a function of parameters such as temperature, voltage, or fabrication process.

First, with respect to the accused Samsung Exynos 4412 chip, Dr. Subramanian empirically measured clock output frequency over a large temperature range, as well as over a substantial voltage range. [Tr. (Subramanian) 1215:6-23; RX-1179; RX-1181.][18] His results for

[17] Because Complainants bear the burden of proof on infringement, Respondents did not need to measure the frequency of each and every accused chip.

[18] For his empirical measurements on the accused Samsung Exynos 4412 and S5PC210 chips, Dr. Subramanian mounted the chips on a development board, which is available on the open market and which implements basic phone functionalities. [Tr. (Subramanian) 1215:6-17.] He then used a high-precision and well-calibrated Agilent 53131A frequency counter to characterize the frequency behavior of the Samsung chips as a function of temperature or voltage. [*Id.* 1215:17-1216:8, 1219:8-19 (discussing temperature measurement set-up), 1219:20-25 (same for voltage measurements); RDX-4.96 (showing development board).] In addition, the PLL's frequency output is subjected to a fixed ratio divider that provides a fixed fraction of the actual on-chip PLL frequency. [*Id.* 1216:22-1217:5; RDX-4.97.] Because of this fixed division ratio, the measured frequency would vary by the same amount as the PLL. [*Id.* 1217:6-9.]

this Samsung chip appear on RDX-4.97, where the plot on the left shows frequency as a function of temperature while the graph on the right depicts frequency as a function of voltage. [Tr. (Subramanian) 1216:17-21; RDX-4.97.]



Range	Clock Frequency over Range	Tolerance During Measurement
0°C -70°C in five degrees increments	50.005 MHz*	+/- 0.000648%
1.0V-1.16V in 0.02V increments	50.005 MHz*	+/- 0.0000237%

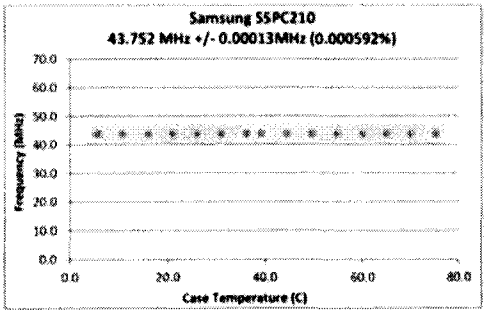
[RDX-4.97 (excerpt).] As Dr. Subramanian noted, "if you look at the data, you see that it is effectively flat." [Tr. (Subramanian) 1217:10-11; RDX-4.97.] "[T]he key point is, over a large range of testing, 0 to 70°C, and an almost 20 percent change in operating voltage, which is a large change in operating voltage, because these PLLs are driven with precision power sources, we see that the clock frequency basically doesn't move very much. ***It's extremely flat.***" [*Id.* 1217:17-24] This level of stability in frequency is in the same ballpark as what a crystal—which the patent calls "fixed"—would exhibit. [*Id.* 1217:25-1218:5; JXM-1 at 17:32-34.]

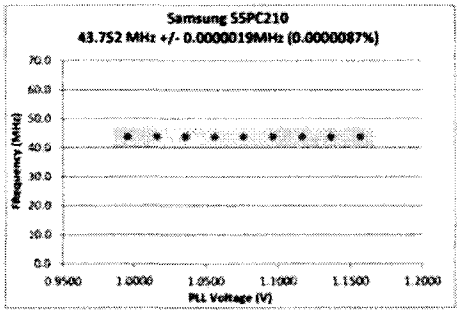
To further confirm the stability of the PLL's frequency despite changes in temperature or voltage, Dr. Subramanian also calculated the tolerance (*i.e.*, the variability associated with the measurements). [Tr. (Subramanian) 1218:8-10.] As shown in the table on RDX-4.97, "[t]he variation is tiny," being *less than* 0.001 percent. [*Id.* 1218:16-18; RDX-4.97.] The PLL thus outputs an extremely stable frequency that is, according to the patent, fixed.

Second, Dr. Subramanian empirically measured the PLL frequency of the accused

PUBLIC VERSION

Samsung S5PC210 chip as a function of voltage or temperature by using the same procedure and set-up used for the Exynos chip. [Tr. (Subramanian) 1218:22-1219:5, 1220:24-1221:4; RDX-4.98.] As with the Exynos chip, the data for the S5PC210 chip, as shown on RDX-4.99, shows ***no variation*** over a temperature range of 0 to 80 degrees Celsius or over a voltage range of 0.95V to 1.20V. [*Id.* 1220:10-1221:7; RX-1184C; RX-1186C; RDX-4.99.] The tolerance for the temperature measurement was a tiny +/- 0.000592%, while the tolerance for the voltage measurement was a minuscule +/- 0.0000087%. [*Id.*]



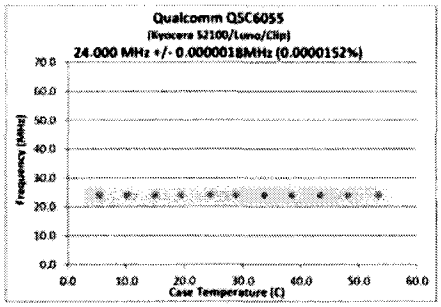


Range	Clock Frequency over Range	Tolerance During Measurement
0ºC -70ºC in five degrees increments	43.752 MHz*	+/- 0.000592%
1.0V-1.16V in 0.02V increments	43.752 MHz*	+/- 0.0000087%

[RDX-4.99 (excerpt).] As Dr. Subramanian noted, the data "shows that the frequency is essentially flat as a function of temperature" and "similarly, the frequency is essentially flat as a function of voltage." [Tr. (Subramanian) 1220:19-22.]

Third, his measurement on the accused Qualcomm QSC6055 chip used in an actual accused phone shows the same result: the clock frequency is flat as a function of temperature. [Tr. (Subramanian) 1221:8-1224:2; RDX-4.100.] Because this chip was inside an operating mobile phone, Dr. Subramanian measured the camera clock frequency as a proxy for the PLL's output, because this frequency originates from the same PLL associated with the ARM core. [*Id.*

1221:22-1222:4; RX-602C at LGE800ITC 1914-16, 1918.] The measured camera clock frequency—which is a fixed fraction of the actual on-chip PLL frequency—is again "incredibly flat" over the temperature range of 0-50 degrees Celsius, with a tolerance of +/- 0.000015%.[19] [Tr. (Subramanian) 1222:25-1223:8; RX-1187C; RX-1188C; RDX-4.100.]



Temperature Range	Clock Frequency over Temperature Range	Tolerance During Temperature Measurement
0ºC -50ºC in five degrees increments	24.000 MHz*	+/- 0.000015%

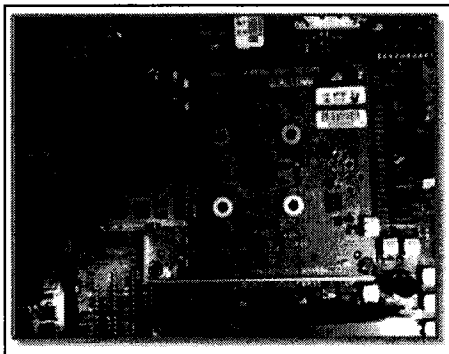
[RDX-4.100 (excerpt).]

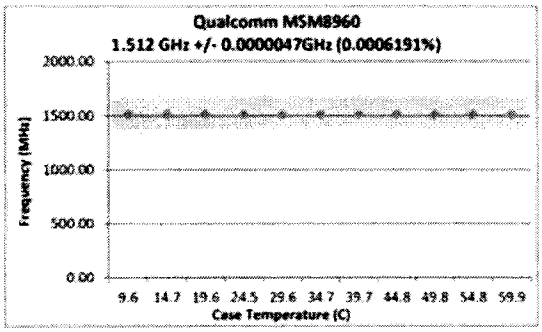
Finally, Dr. Subramanian measured the frequency output of the relevant PLL in the Qualcomm MSM8960 chip by using a development board from Qualcomm. [Tr. (Subramanian) 1224:3-1225:19; RDX-4.101.] This Qualcomm development board provides a terminated output that allows direct measurement of the PLL frequency without needing a fixed-ratio division as with the other chips. [*Id.* 1224:13-24.] As a result, he was able to measure the PLL's full 1.5 GHz frequency over a large temperature range from 0 to 50 degrees Celsius with a tolerance of +/- 0.000619%.[20] [*Id.* 1225:1-10; RX-1189; RX-1190.] As with the other measurement data,

[19] A different temperature range of 0-50 degrees Celsius was used for the phone, as compared to the tests for the other chips, to prevent battery damage. [Tr. (Subramanian) 1223:15-25.]

[20] A temperature range of 0-50 degrees Celsius was used for the Qualcomm chip because it was on a development board that required a larger oven than that used for the other chips and this oven's maximum temperature was 50 degrees Celsius. [Tr. (Subramanian) 1225:5-15.]

the PLL's output is "completely flat" and "incredibly stable over the temperature range that we could do." [*Id.* 1225:2-4.] In fact, the data shows that any possible fluctuation is "basically in the range of what the crystal can provide." [*Id.* 1225:18-19; *see also* RX-167C (Fish Depo.) at 145:21-24 (confirming that a crystal is "a fixed clock for all intents and purposes").]





Temperature Range	Clock Frequency over Temperature Range	Tolerance During Temperature Measurement
0ºC -50ºC in five degrees increments	1.512 GHz	+/- 0.000619%

[RDX-4.101 (excerpt).] As the empirical evidence clearly demonstrates, "the PLL does exactly what it should." [Tr. (Subramanian) 1226:14.] In particular, the PLL's output frequency "does not vary" and "is extremely stable." [*Id.* 1226:6-8.]

In contrast to the PLL's fixed frequency, the '336 patent teaches that its variable speed clock's frequency will change by as much as about 400% due to PVT during operation. [JXM-1 at 17:21-22 ("factor of four").] As another example, the patent also states that its clock's frequency changes by 200% with temperature, varying from 50 MHz at 70°C to 100 MHz at room temperature (~22°C). [JXM-1 at 16:60-63, 17:21-22; RDX-4.93.] Over this same temperature range, Dr. Subramanian's empirical measurements show no detectable variation. [RDX-4.97-101.] The data is unequivocal: the accused PLLs' frequencies do not vary as a function of fabrication process, voltage, or temperature.

PUBLIC VERSION

VII. THE "OFF-CHIP EXTERNAL CLOCK" LIMITATION OF CLAIMS 6 AND 13

A. The ID correctly found that the accused products do not meet the "external clock is operative at a frequency independent of a clock frequency of said oscillator" limitation of claims 6 and 13

Claims 6 and 13 both require that the clock for the on-chip input/output ("I/O") interface be off-chip and independent from the claimed oscillator. [JXM-1 at cls. 6 & 13 ("external clock is operative at a frequency independent of a clock frequency of said oscillator").] Based on the parties' agreement, the ALJ construed this limitation to mean "an external clock wherein a change in the frequency of either the external clock or oscillator does not affect the frequency of the other." [Order No. 31 at 11; ID at 14.] Having stipulated to this construction, Complainants do not challenge this construction in their petition. [Pet. at 35, 37-45.]

Instead, Complainants advance a new strained interpretation of the construction to suit their litigation needs, [*id.* at 35, 37-39], and jettison all of their prior contentions based on "internal" clock limitations found in other claims in favor of "external" clocks, in a futile effort to mask their proof problems. [*Id.* at 35, 39-45.] These arguments are specious and disregard the paramount problem with Complainants' case concerning this limitation: Complainants did not present adequate evidence, if any, on this limitation and thus failed to satisfy their burden of proof. Given this failure of proof, the ALJ found "that Complainants' evidence is not sufficient to establish that any of the Accused Products meet the 'second clock' or 'external clock' limitations of the asserted claims." [ID at 245.] The ALJ is correct.

1. Dr. Oklobdzija's conclusory testimony is insufficient

As a preliminary matter, Complainants' petition fails to confront their overwhelming failure of proof on the "independent" limitation. Complainants accused hundreds of products with different chips, and attempted to rely on dozens of separate I/O interfaces in each of these products or chips. [RBr. at Att. A (list of accused products at the conclusion of the hearing), and

Att. B-C (lists of products accused in Dr. Oklobdzija's expert report but for which Complainants failed to present evidence at the hearing).] Even in their post-hearing brief, Complainants still alleged that over 200 products infringe the asserted claims, with a plethora of I/O interfaces in each product that supposedly satisfy the "independent" limitation. [CBr. at Ex. A (final list of accused products).]

Having chosen quantity over quality, Complainants' proof on these products and their alleged "second clock"[21] were entirely conclusory, as the ID found: "The Administrative Law Judge further finds that Dr. Oklobdzija's testimony on infringement of the 'second/external clock' limitations is in other respects inadequate because it was essentially conclusory." [ID at 246.] The ALJ found, and Complainants' petition does not dispute, that "Complainants' technique was to elicit conclusory opinions from Dr. Oklobdzija and leave it to Respondents to try to ferret out his underlying reasoning." [*Id.* (also quoting Tr. (Oklobdzija) 704:7-705:2 to show inadequacy of testimony).] This approach of making a broad assertion about the ultimate issue without offering any explanation or evidence falls far short of Complainants' burden of proof. [ID at 247 ("That testimony overlooks the fact that the time to 'elaborate,' as Dr. Oklobdzija tauntingly put it, was during his direct examination, not cross, because it is Complainants who bear the burden of proving that the Accused Products infringe—Respondents do not bear the burden of proving that their products do not infringe.").] As the ALJ elaborated, "[f]or Complainants to base their proof of infringement on dogmatic tidbit statements of an expert, in the guise of an informed opinion based on a litany of documents without explaining the thought process by which, or

[21] During his analysis, Dr. Oklobdzija used the short-hand "second clock" to refer to the disputed limitations in all asserted claims, including the limitations requiring independent external clocks and "wherein… asynchronously." For the Commission's convenience, this brief will also use this short-hand convention wherever appropriate.

reasons why, he arrived at his conclusion is not sufficient to sustain that burden." [*Id.*]

Complainants' "shotgun" approach to proving this limitation was pervasive throughout the hearing. For example, despite hours of testimony about accused I/O interfaces, Dr. Oklobdzija failed to even once explain the alleged documentary evidence, tie the documents to the controlling claim construction, and establish how any of these I/O interfaces can meet the "independent" limitation. [ID at 247.] For most of the accused chips, Dr. Oklobdzija's only explanation about the "second clock" limitations consisted of conclusory statements affirming that he reviewed the schematics and decided that these limitations are met. [*E.g.* Tr. (Oklobdzija) 681:12-684:2 (providing conclusory statements for 8 separate products from two respondents), 686:11-693:19 (same for 21 separate products from five respondents), 702:22-704:18 (same for 17 products from Garmin), 730:22-732:6 (same for Samsung); *see also* ID at 247 (citing same passages as example of inadequate testimony).]

Rejecting this improper tactic, the ALJ correctly found that Complainants did not meet their burden on these limitations: "While Complainants say Dr. Oklobdzija analyzed hundreds of external and internal clocks (apparently meaning technical documents) that does not alleviate Complainants and their expert witness of their responsibility to provide information sufficient to carry Complainants' burden of proof by connecting the dots, *i.e.*, showing how the documents support his conclusions." [ID at 247.] Given these facts and the controlling law, the ALJ correctly found that Complainants and their expert failed to satisfy their burden of proof.[22] [*Id.*]

[22] It is notable that Complainants do not question, attack, or even challenge the ALJ's findings of failure of proof on the "second clock" limitations, as shown by their failure to cite or discuss these findings in their petition. [Pet. at 35-47 (discussing "independent" and "asynchronous" limitations).] Despite the opportunity to challenge the ALJ's specific findings by pointing to evidence to satisfy their burden of proof, Complainants offer no such evidence and thus confirm that the ALJ was correct in his findings. [*Id.*]

See Kim v. ConAgra Foods, Inc., 465 F.3d 1312, 1319-20 (Fed. Cir. 2006) (affirming JMOL of noninfringement because, beyond merely "conclusory testimony," the patentee's expert "presented no testimony based on the accused products themselves that supported a finding of infringement.").

On this basis alone, the Commission should reject Complainants' petition for review in its entirety.

2. **The Commission should reject Complainants' misinterpretation of the undisputed construction**

a. Complainants disregard the agreed-upon construction

According to Complainants, the ID misapplied the undisputed construction by "conclud[ing] that the first and second clocks are not independent or asynchronous because they share the same reference signal." [Pet. at 35; *see also id.* at 37-39.] However, it is Complainants, not the ALJ, who disregard the agreed-upon construction.

As an initial matter, the ALJ already considered and expressly rejected Complainants' allegations that Respondents supposedly attempted to import limitations into the adopted claim construction. [ID at 252-253 (summarizing Complainants' argument and citing CRBr. at 55).] After summarizing the allegations, the ALJ found that the arguments actually highlighted Complainants' own failure to apply the adopted construction:

> The Administrative Law Judge finds that one of the problems with this argument is that ***it raises the specter of Dr. Oklobdzija's and Complainants' own failure, since they did not provide evidence sufficient*** to demonstrate that a change in the frequency of the second (external) clock or the first clock does not affect the frequency of the other, given the construction adopted based on the parties' agreed claim constructions. (Order No. 31 at 11-12.) Complainants' argument on this point serves as a reminder of an important principle that pervades this Investigation, which is that Complainants have the burden of proof-in terms of production and persuasion-and the criticism Complainants level at Respondents here applies to them as well. ***According to Complainants' own critical standards, they have not discharged their burden of proof.***

[ID at 253.] In other words, Complainants' allegations demonstrate that they failed to satisfy their burden of proof.

A simple look at Complainants' argument illuminates their failure of proof. At the heart of Complainants' argument is the mistaken belief that "supplying an upstream reference signal to two clocks does not render them dependent on each other." [Pet. at 38.] To justify their position, Complainants throw around the words "dependent" and "independent." [*E.g., id.* at 38 ("In other words, the relevant question is whether the two clocks are ***dependent on each other*** for changes in frequency. Unrefuted evidence shows that the two clocks are ***not*** dependent on each other." (emphases in original)); *see also id.* at 38-39 (using the words "dependent" and "independent" twelve separate times over two pages).]

Complainants' argument, however, ignores the agreed-upon construction, which does *not* use the words "dependent" or "independent." The undisputed construction instead requires "an external clock wherein a change in the frequency of either the external clock or oscillator does not affect the frequency of the other." [Order No. 31 at 11; ID at 14.] Rather than re-use the word "independent" from the claim term, the agreed-upon construction specifies *how* two structures are independent – by requiring that a change in frequency of one does not affect the other's frequency. Despite Complainants' misuse of the undefined words "independent" and "dependent," it is too late for them to backtrack on this stipulated meaning.

Complainants' casual use of "independent" in their petition while ignoring the actual construction of the limitation mirrors the approach they and their expert took during the hearing. When referring to what he considered "second clocks," Complainants' expert testified that "[w]e have identified or established their independence, basically, by coming from two independent PLLs or ring oscillators within those PLLs." [Tr. (Oklobdzija) 702:2-5.] However,

Dr. Oklobdzija did not testify even once about the governing claim construction. That is why the ALJ found "that is not sufficient proof that the frequency of either the external clock or oscillator does not the affect the frequency of the other." [ID at 245; *see also id.* (finding that "Dr. Oklobdzija failed to address the parties' agreed claim construction").]

Complainants' petition does not cite to any adequate evidence, but instead offers a single testimonial citation that does not even address this issue. In the cited passage, Dr. Oklobdzija conclusorily stated that [redacted] chips were independent because [redacted] [Tr. (Oklobdzija) 1060:23-1061:18; Pet. at 38 (citing same).] This testimony is, however, irrelevant to claims 6 and 13, the only remaining asserted claims, because these claims require an "off-chip external clock" and the two ring oscillators discussed in this testimony [redacted]. [*Id.*] In other words, the testimony does not even relate to an off-chip external clock. But even if this testimony were relevant, it fails to apply the controlling construction, as it fails to explain how the change in the frequency of one oscillator "does not affect the frequency of the other." Dr. Oklobdzija simply concluded that they are independent without any analysis or explanation under the governing construction. Whether one concludes that the testimony is irrelevant or conclusory (or both), one thing is sure: this testimony does not save Complainants' argument.

Lacking evidence, the petition resorts to an analogy based solely on attorney arguments. [Pet. at 39.] Taking a simple analogy to cruise control that Dr. Subramanian used to explain the role of a PLL, Complainants stretch the analogy beyond its breaking point by injecting a ring oscillator, a reference frequency, and an external clock. [*Id.*] Complainants' analogy is a brand new, *post hoc* attorney argument, which is devoid of support in the evidentiary record. [*Id.*] Their analogy is not evidence. *See Johnston v. IVAC Corp.*, 885 F.2d 1574, 1581 (Fed. Cir.

1989) ("Attorneys' argument is no substitute for evidence."). Even if one were to accept Complainants' premise that two clocks sharing a reference frequency is analogous to two cars with cruise control set to the reference speed dictated by the speed limit, Complainants' own analogy supports Respondents' position. If the speed of two cars were dictated by the speed limit on the road, then the speed of both cars would change when the speed limit changes. This analogy, like the irrelevant citation to Dr. Oklobdzija's testimony, does not help Complainants' cause.

By contrast and as the ALJ recognized, Dr. Subramanian's analysis applied the governing claim construction, showing that the accused interfaces do not meet this limitation:

> Given the lack of particulars and specificity in Dr. Oklobdzija's summary conclusions, Respondents' expert witness, Dr. Subramanian, responded accordingly by pointing out that the I/O interface signals that Complainants rely on are neither independent nor asynchronous, illustrating this by focusing on the two most common I/O interfaces discussed during Dr. Oklobdzija's direct testimony-the USB and camera interfaces-as well as the LSI Logic B5503A chip.

[ID at 249-250.] In his testimony, Dr. Subramanian explained that two clock signals cannot meet the construction if they are derived from the same source, because a change in the frequency of the source clock affects the frequency of both downstream clocks. [Tr. (Subramanian) 1353:1-1354:5).] For example, if two separate PLLs use the same 20 MHz crystal oscillator as a reference clock, a change in the reference's frequency (such as switching to a 30 MHz crystal) will likewise cause the output frequency of both PLLs to change. [*Id.*] Rather than advancing a different interpretation, Dr. Subramanian simply applied the undisputed construction to the structure of the accused products and explained how these devices do not meet the construction.

Having heard the live testimony of both experts, the ALJ credited Dr. Subramanian's analysis and rejected Complainants' criticisms: "The Administrative Law Judge concludes, therefore, that Complainants' criticisms of Dr. Subramanian's analysis and his conclusions, do

not show that his reasoning is wrong or that his opinion is invalid. The Administrative Law Judge further finds that, vis-a-vis Dr. Oklobdzija's testimony, Dr. Subramanian's is more demonstrable by independent evidence." [ID at 252.] Neither the ALJ's findings nor his credibility determinations warrant review. *See Agfa Corp. v. Creo Prods. Inc.*, 451 F.3d 1366, 1379 (Fed. Cir. 2006) ("This court must defer heavily to the trial court's credibility determinations.... Credibility determinations by the trial judge can virtually never be clear error.").

b. Complainants' argument based on the "entire" limitations is specious

According to Complainants, the ID incorrectly "bootstraps the same theory the ID advances with respect to the 'entire' limitations" because it is the ring oscillator, not the PLL or a reference signal, that generates the clock signal. [Pet. at 40.] This point falters for two reasons.

First, in making this argument, Complainants presuppose that their theory about the generation of the clock signal is correct. The ID, however, considered this theory and thoroughly discredited it. [ID at 118-132.] And as discussed above, there is no merit to any of Complainants' bases for reviewing or disturbing the ID's correct finding on the "entire" limitation. [*See* Part V, *supra*, at pp. 20-57.] Without the support of this incorrect premise related to the "entire" limitation, Complainants' attack on this limitation must fail.

Second, even if Complainants could overcome the weight of the evidence on the "entire" limitation, they still have not shown how any accused products satisfy the agreed-upon construction of the "independent" limitation. [Order No. 31 at 74.] Other than conclusory attorney argument, Complainants offer no evidence to explain how generation of a clock signal by a ring oscillator necessarily means that a change in the oscillator's output frequency will not affect the frequency of the external clock. [Pet. at 40.] Nor is there any evidence to show why a

change in the frequency of the external clock will not affect the ring oscillator's clock signal even if the ring oscillator generates a clock signal on its own (which it does not). [*Id.* (providing no evidentiary citation).] Complainants offer attorney argument – but no evidence, no logic, and no reason – to support their conclusory statements. Their attorney argument is not evidence. *See Johnston,* 885 F.2d at 1581 ("Attorneys' argument is no substitute for evidence.").

3. **Complainants' eleventh-hour focus on "external" I/O clocks cannot remedy their failure of proof**

a. Commission precedent precludes infringement based on an "external clock" located on a different device

Complainants attempt to brush aside the ALJ's well-reasoned findings on this limitation by drawing a distinction between "internal" clocks (on the same chip as the PLL) and "external" clocks (not on the same chip), and then asking the Commission to ignore all of the ALJ's detailed findings pertaining to "internal" clocks. [Pet. at 35, 40-44.] By abandoning the camera interface and other "internal" I/O interfaces that were the focus of Complainants' prior allegations, Complainants now limit their case to a second "external" clock provided via the HDMI and USB interfaces because these are the only external clocks for which Complainants offered any evidence in their petition. [*Id.*]

Complainants' "external" clock theory is fundamentally flawed because it is based on HDMI and USB connections that require the use of a device *separate* from the accused products. This is apparent from the petition itself. As discussed in the petition, Dr. Oklobdzija testified that the HDMI clock is an "external clock that originates from the HDMI device, that could be a display or it could be something else that uses HDMI protocol." [Tr. (Oklobdzija) 706:10-707:7; Pet. at 42 (citing same).] As to USB, Complainants admit that they "accused an external USB clock originating from a connected peripheral." [Pet. at 43; *see also id.* (arguing that "the clock signal originates from *an unrelated device*").] In both instances, Complainants' "external clock"

theory requires that there must be a separate device connected to an accused product's USB or HDMI interface, with the device and the product exchanging data over a USB or HDMI cable.

The accused products, however, are not imported while tethered to a desktop or laptop computer for data transfer. [Tr. (Oklobdzija) 1086:18-23 ("I don't see desktop or notebook in your other hand."); *see also, e.g.*, RPX-37 (accused LG Lucid phone in its original small box).] Nor is any accused product imported while exchanging data with a television display or a Blu-Ray player via a HDMI cable, and Complainants have not offered any evidence to suggest otherwise. [*E.g.*, RPX-37 (showing nothing connected to phone as imported).] Because there is no USB or HDMI connection between any accused product and an external device at the time of importation, there is no "second clock" when the accused products enter the United States and thus no basis for a violation of Section 337 under this theory. *See Certain Electronic Devices with Image Processing Sys.*, Inv. No. 337-TA-724, Comm'n Op., 2012 WL 3246515 at *9 (Dec. 21, 2011) ("We also interpret the phrase 'articles that – infringe' to reference the status of the articles *at the time of importation*. Thus, infringement, direct or indirect, must be based on the articles *as imported* to satisfy the requirements of section.").

To avoid the impact of *Image Processing*, Complainants now argue that this Commission opinion does not apply to apparatus claims. [Pet. at 44.] Not so. The patents in *Image Processing* included apparatus and data format claims, in addition to method claims. *Image Processing*, Inv. No. 337-TA-724, 2012 WL 3246515 at *3-4. In fact, the Commission's analysis of infringement at the time of importation started with claim 11 of the '978 patent, which is a data format claim. *Id.* at *9-10. For this non-method claim, the Commission found that "Apple does not import an article that directly infringes claim 11" because "the data that S3G relies upon for infringement of claim 11 is created in the United States," *i.e.*, *after* the respondent

had imported the accused products. *Id.* at *9. Critically, this analysis did not depend on the statutory subject matter of the claim, but instead turned on whether the accused articles met every claim limitation at the time of importation. *Id.*

The Initial Determination in *Certain Video Game Systems,* which Complainants cite in an attempt to cabin *Image Processing*, is not persuasive. *See Certain Video Game Sys.*, Inv. No. 337-TA-770, Init. Determ., 2012 WL 4480570 at *10 (Aug. 31, 2012) (cited in Pet. at 44). Not only was this Initial Determination reversed and remanded, *Certain Video Game Sys.*, Inv. No. 337-TA-770, Comm'n Notice (Nov. 6, 2012), but it incorrectly assumed that *Image Processing* only involved method claims. *Certain Video Game Sys.*, Inv. No. 337-TA-770, 2012 WL 4480570 at *10 ("*Image Processing Systems*, however, involved method claims."). Contrary to this assumption, *Image Processing* implicates more than just method claims. *Image Processing*, Inv. No. 337-TA-724, 2012 WL 3246515 at *3-4 (reciting different types of claims, including apparatus claims). Because the ruling in *Video Games Systems* relied on an incorrect assumption and did not survive review, it is not persuasive authority.

The only applicable and controlling authority is *Image Processing* itself. This Commission opinion compels a finding of noninfringement because, as imported, none of the accused products is connected to an external device providing the claimed external clock signal through a USB or HDMI connection.[23] Because there is no "second clock" at the time of importation under Complainants' revised "external clock" theory, the Respondents "do[] not import an article that directly infringes" claims 6 and 13. *Image Processing*, Inv. No. 337-TA-

[23] Because Complainants did not seek review of indirect infringement, they waived their ability to prove a violation of Section 337 based on any alleged indirect infringement, including induced infringement, arising from any post-importation connection of the accused products to an external device via a USB or HDMI connection. *Broadcom*, 542 F.3d at 900-901 (finding waiver of an argument not raised in a petition of review to the Commission).

724, 2012 WL 3246515 at *9.

b. Complainants' argument about testing is a strawman

Unable to conjure an actual error in the ALJ's thorough analysis, Complainants raise another strawman by suggesting that the ALJ incorrectly required testing evidence from a technical expert to show infringement. [Pet. at 44-45.] Even a cursory review of the ID dispels this argument. [ID at 245-246.]

In his ID, the ALJ emphasized that there is a dearth of record evidence related to the "independent" limitation, and it is in large part because Dr. Oklobdzija "failed to address the parties' agreed claim construction." [ID at 245.] As the ID noted, whether "the frequency of either of those devices is affected by the frequency of the other was not covered by Dr. Oklobdzija's testimony; and whether or not they do cannot simply be inferred on the basis of the existing evidence." [*Id.* at 246.] Because Dr. Oklobdzija did not perform any test to satisfy the agreed-upon claim construction, the ALJ reasoned that Complainants' expert had no other evidence than his testimony. And despite hours of testimony superficially covering a multitude of clocks, Dr. Oklobdzija only presented conclusory assertions on this limitation. Hence, in the absence of independent test results, "the most he could have offered by way of expert testimony would have been conclusory, anyway." [*Id.*]

To be thorough, the ALJ further hypothesized that, even if Dr. Oklobdzija had performed tests, it is possible Respondents and Dr. Subramanian would have presented their own test results in response. [*Id.*] The ALJ was left to guess about what evidence would have been sufficient, given Complainants' failure to present evidence to make a *prima facie* case. [*Id.*] He was, however, sure that "there is a hole in the evidence, and the Administrative Law Judge concludes that Complainants' proof here is not sufficient to show that any of the Accused Products satisfies any of the 'second clock' or 'external clock' limitations." [*Id.*]

Given the gaping "hole[s] in the evidence" on this limitation, there is no basis to review the ALJ's well-reasoned and thorough ID finding that Complainants failed to prove the presence of this claim limitation in the accused products.

B. The ID correctly found that the accused products do not meet the "wherein ... asynchronous" limitation of claim 13

Claim 13 additionally requires that the clock for the on-chip input/output ("I/O") interface operates asynchronously to the entire oscillator. [JXM-1 at cl. 13.] Based on a careful consideration of the evidence and after thoroughly addressing Complainants' allegations regarding this limitation, the ALJ concluded that "the evidence does not support a finding that any of the Accused Products meet the 'asynchronous' requirement of claims 11, 13, and 16." [ID at 257; *see also id.* at 255-259 (discussing "asynchronous" limitation).]

Complainants' petition does *not* challenge the ALJ's claim construction of this limitation. Rather, the petition advances two arguments against the ID's factual findings. First, the petition alleges that, because "the ALJ did not understand" Dr. Oklobdzija's testimony about "asynchronous," the ALJ supposedly analyzed the wrong relationship and failed to understand that Dr. Oklobdzija's testimony discussed "universal principles applicable to PLLs." [Pet. at 45-46.] Second, the petition quotes a number of instances where the term "asynchronous" appears in cherry-picked technical documents to argue that the accused chips satisfy this limitation. Not only are these two arguments wrong, but they fail to satisfy the requirements of the undisputed claim construction. As a result, Complainants have shown no error that would justify review.

1. Complainants cannot satisfy the "no readily predictable phase relationship" requirement of the undisputed construction

The undisputed construction of this limitation precludes a predictable phase relationship between the CPU's timing controls and the I/O's timing controls: "the timing control of the central processing unit operates independently of and is not derived from the timing control of

the input/output interface such that there is no readily predictable phase relationship between them." [Order No. 31 at 74.] Complainants have not met their burden of showing that the accused products meet this requirement.

In their post-hearing brief and again in their petition, Complainants cite only a single piece of evidence—Dr. Oklobdzija's testimony about phase relationship. [CBr. at 44 (citing Tr. (Oklobdzija) 1026:14-1028:8); Pet. at 46 (same).] But their expert was addressing the *wrong* relationship; his testimony relates to the phase relationship between the phase of the received external reference clock signal and the phase of the PLL's output signal which is provided back to the PFD block by the PLL's feedback loop: [24]

> The phase relationship is how those edges of the clock fall together; okay? And that difference produces that error signal that drives PLL, because if there is a predictable phase relationship, there is no error signal, and you don't need PLL; the PLL has no purpose any more. The PLL is based on error, as those phases don't come together. That's why PLL works. If there is no error, the signal out of PLL is zero, and there is no purpose for the PLL.

[Tr. (Oklobdzija) 1026:23-1027:10.] In other words, Dr. Oklobdzija's cited testimony addresses the phase relationship *between a PLL's input and its output*. Confirming this fact is the testimony which came just before the excerpt cited by Complainants, where Dr. Oklobdzija acknowledged which relationship he was addressing:

> Yes, what Mr. Casasanta is talking about is a formula, the formula that establishes *the relationship of the output of the PLL with respect to reference*.

[Tr. (Oklobdzija) 1026:16-19.] By contrast, the "asynchronous" limitation requires a different phase relationship: as construed, these limitations prohibit readily predictable phase

[24] The Phase Frequency Detector ("PFD") block in a PLL performs a "phase checking" function by comparing the phase of the input reference signal from an external crystal/clock generator with the phase of the signal output by the PLL's feedback loop. [Tr. (Subramanian) 1152:11-1153:3.]

relationships *between the CPU's timing* interface *and the I/O interface's timing interface, i.e.,* between the CPU and the I/O interface. [Order No. 31 at 74.] Therefore, Dr. Oklobdzija's testimony, as well as Complainants' argument about this particular phase relationship, is simply irrelevant to the "asynchronous" limitation.

In light of this evidence, the ALJ agreed that Dr. Oklobdzija was addressing the wrong relationship:

> Complainants have not demonstrated how Dr. Oklobdzija's testimony shows that the timing control signals of the accused CPUs are not derived from the timing controls of input/output interface such that there is no readily predicable phase relationship between them. It does appear, as Respondents argue, that Dr. Oklobdzija was testifying about something else, the phase relationship between the PLL and the external clock.

[ID at 257-258.] The ALJ thus ruled "that the evidence does not support a finding that any of the Accused Products meet the 'asynchronous' requirement of claims 11, 13, and 16." [*Id.* at 257.]

Instead of acknowledging their failure of proof, Complainants raise the proverbial strawman by criticizing the ALJ for requiring a relationship between the phase of "a reference signal and the first or second clocks." [Pet. at 46.] The ALJ required no such thing. [ID at 256-258.] He simply recognized the obvious: Dr. Oklobdzija testified about a phase relationship that is different from what the undisputed construction requires. In fact, the ID even gave Complainants the benefit of the doubt, but found the evidence still wanting: "Insofar as Complainants contend that Dr. Oklobdzija was testifying about the phase relationship between the CPU and the input/output interface, they have not provided a sufficient explanation as to how they derive that conclusion from the testimony of Dr. Oklobdzija. It is certainly not from the portion of his testimony they cite in their brief, quoted above." [ID at 258.] The problem is therefore not in the ID; it rests with Complainants, who failed to offer adequate evidence to prove their case.

Finally, although admitting that Dr. Oklobdzija's testimony on this limitation only addressed one specific PLL in a single accused product, Complainants contend that his testimony "discusses universal principles applicable to PLLs." [Pet. at 46.] Yet, Dr. Oklobdzija never stated that his testimony on this point should extend to all types of PLLs. [Tr. (Oklobdzija) 1026:14-1027:10.] Although Complainants try to use attorney argument to compensate for their lack of evidence, attorney argument is simply not enough. *Johnston*, 885 F.2d at 1581 ("Attorneys' argument is no substitute for evidence.").

In sum, there is no evidence establishing, as the undisputed construction requires, that "there is no readily predictable phase relationship between" the entire oscillator and the off-chip external I/O clock. Therefore, Complainants did not meet their burden of proof and cannot justify review of the ID.

2. **Complainants' citations to the word "asynchronous" in documents cannot satisfy their burden**

Complainants argue that the mere presence of the word "asynchronous" (regardless of context) in various technical documents necessarily meets this disputed limitation. [Pet. at 46-47.] Their argument is meritless.

As a preliminary matter, by just pointing to the word "asynchronous" in technical documents, Complainants ignore the remainder of the claim term that the ALJ construed and that is at issue: "wherein said central processing unit operates asynchronously to said input/output interface." [Order No. 31 at 74; ID at 16-17.] While the word "asynchronous" is part of this claim language, it is, by itself and out of context, insufficient to satisfy Complainants' burden of proof.

More importantly, the word "asynchronous" in the quotes cited by Complainants appear without any context, and without any explanatory testimony or analysis other than attorney

argument. For instance, Complainants rely on an excerpt from a Qualcomm document that says [redacted] but their brief does not explain how that is relevant to the "asynchronous" limitation. [Pet. at 47 & n.29 (quoting CX-663C at [redacted]).] Although this excerpt contains the word "asynchronous," it sheds no light on whether the Qualcomm document uses the term in the same way as the patent. Nor is there any evidence—and certainly none from Complainants' expert—addressing how this excerpt satisfies the other requirements of the undisputed construction, such as the provision that the CPU's timing control must operate independently of the I/O interface's timing control or the provision that there is no phase relationship between these timing controls. [*Id.*] The other documentary excerpts that Complainants cite face the same flaw, because they are quoted without context and without any testimonial explication. More importantly, this same evidence was before the ALJ, who noted the deficiency and correctly found that the mere mention of "asynchronous" is not sufficient to satisfy the claim language. [ID at 258 ("The fact that the technical documents that Complainants cite in their reply brief mention the word 'asynchronous' does not mean that those documents are applying the term in the same way as expressed in the adopted construction.").]

With no actual testimonial support for these excerpts, Complainants' petition cites two passages of their expert's testimony. [Pet. at 47.] Neither cite, however, supports their position. In the first cite, Dr. Oklobdzija was not addressing any accused products or technical documents; he merely read the adopted construction into the record. [Tr. (Oklobdzija) 312:8-313:11 (cited in Pet. at 47).] In the second passage, Dr. Oklobdzija read into the record the same quotes from the [redacted] that Complainants include in their petition. [*Compare* Tr. (Oklobdzija) 488:21-489:15, *with* Pet. at 46-47 & n.28.] But at no time did Dr. Oklobdzija establish that the

manual from which he read uses the term "asynchronous" in the same way as the asserted claims. Nor did Dr. Oklobdzija testify about the other requirements of the undisputed construction, including (1) timing controls, (2) independence, (3) no derivation, and (4) no readily predictable phase relationship. [*Compare* Tr. (Oklobdzija) 488:21-489:15, *with* Order No. 31 at 74.] All that Dr. Oklobdzija does in the cited testimony is parrot the word "asynchronous" and then assume that the claim language is met. Faced with a similar statement about a [redacted] manual's use of the word "asynchronous," the ALJ found such conclusory testimony to be unpersuasive and legally insufficient. [ID at 259.] Because conclusory expert testimony is insufficient, this issue does not warrant review. *See ConAgra Foods, Inc.*, 465 F.3d at 1319-20.

As a last resort, Complainants criticize Respondents and the ALJ for failing to offer any "suggestion about what else the term [asynchronous] could mean in the context of clocking a microprocessor." [Pet. at 47.] This criticism is meritless for two reasons. First, it is Complainants, not Respondents, that bear the burden of proving that the limitation is met by presenting adequate testimony to explain the technical evidence and show how the accused products meet the construed limitation. As the ID noted, "Complainants have the ultimate burden of proof, and any unresolved questions on material issues redound to their detriment." [ID at 255.] Having failed to secure the necessary testimonial support, Complainants cannot shift the burden onto Respondents. Second, the *undisputed* construction does not relate to the term "asynchronous" alone and does not adopt the word's ordinary meaning. Instead, this construction, which the petition does not challenge, arose from clear and extensive prosecution disclaimers made by the patentee during the reexamination of the '336 patent to secure allowance of the claims with this language. [Order No. 31 at 74 (explaining reasoning for construction); *see also id.* at 69-73 (summarizing evidence supporting construction).]

Accordingly, there is no error here. There is simply Complainants' significant failure of proof that no amount of attorney argument and out-of-context documentary quotes can bridge.

3. **Complainants have not petitioned on or offered evidence addressing the "derived from the timing control of the input/output interface" requirement of the undisputed construction**

As construed, the "asynchronous" limitation requires that "the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them." [Order No. 31 at 74.] Complainants do not challenge this construction in their petition.

In his ID, the ALJ found that Complainants failed to prove up the construction's "derived from" provision, which requires that the CPU's timing control cannot be derived from the I/O interface's timing control: "Since Complainants have not connected Dr. Oklobdzija's testimony about PLLs to these documents, so as to explain how they, alone or in conjunction with other evidence, meet the 'derived from' aspect of the 'asynchronous' limitation, proof of infringement of claims 11, 13, and 16 is lacking with respect to this element." [ID at 259.]

Complainants do not address the construction's "derived from" requirement at all. Their post-hearing briefs and petition are devoid of analysis on that requirement. [CBr. at 81 and 166 (advancing only conclusory attorney statements); CRBr. at 60-62; Pet. at 45-47 (not even discussing evidence related to this requirement or even advancing any argument).] And Dr. Oklobdzija did not testify about this requirement. [Tr. 567:12-570:4 (precluding Dr. Oklobdzija from testifying "as to the ultimate issue" of infringement with respect to the "asynchronous" limitation); ID at 256 n. 22 (explaining same).]

Because Complainants have not petitioned on this issue or presented any evidence on the "derived from" requirement of the "asynchronous" limitation, they have not shown that any of the accused products meets the "asynchronous" limitation and thus cannot show any error.

PUBLIC VERSION

VIII. CEASE & DESIST ORDER

Although the ID correctly concluded that there has been no violation of Section 337 by any Respondents, the ALJ issued a separate Recommended Determination on Remedy and Bond ("RD") as required by 19 C.F.R. § 210.42(a)(1)(ii). The RD states, among other things, that if the Commission finds a violation "the Administrative Law Judge does not recommend that cease and desist orders issue" as to any Respondents. [RD at 9.]

Complainants' Petition improperly includes a request for Commission review of the RD (and specifically the recommendation that no cease and desist orders should issue). [Pet. at 47-49.] The Commission Rules, however, only permit Complainants to "request Commission review of an initial determination." 19 C.F.R. § 210.43(a)(1). Complainants' request for review of recommendations in the ALJ's RD is both premature and improper.

In accordance with Commission practice and consistent with the rules, Respondents understand that, if the Commission decides to review the Initial Determination then it may issue a notice setting deadlines for written submissions from the parties on the issues of remedy, the public interest and bonding. *See* 19 C.F.R. § 210.46. Accordingly, Respondents are not responding substantively to Complainants' petition as it concerns the ALJ's recommendation that no cease and desist orders should issue, and instead reserve their right to submit comments and respond to any comments that Complainants may properly file at the appropriate time if the Commission requests written submissions from the parties.

IX. CONCLUSION

For at least the reasons set forth above, Complainants have failed to establish any error of law or fact and have failed to raise any issue affecting Commission policy that warrant review. Accordingly, Respondents respectfully request that the Commission deny Complainants' petition for review and that the Commission adopt the ID as its final decision.

PUBLIC VERSION

Dated: October 17, 2013

Respectfully submitted,

/s/ Paul F. Brinkman
David Eiseman
Paul F. Brinkman
Michael James O'Connor
Pamela L. Van Dort
QUINN EMANUEL URQUHART & SULLIVAN, LLP
1299 Pennsylvania Ave. NW, Suite 825
Washington, DC 20004
Tel.: (202) 538-8000

Counsel for Respondent Barnes & Noble, Inc.

/s/ Timothy Bickham
Charles Schill
Timothy C. Bickham
Alice A. Kipel
STEPTOE & JOHNSON LLP
1330 Connecticut Avenue, NW
Washington, DC 20036
Telephone: (202) 429-3000

Counsel for Respondents Huawei Technologies Co., Ltd., Huawei Device Co., Ltd., Huawei Device USA Inc., and Futurewei Technologies, Inc.

/s/ Scott A. Elengold
Michael J. McKeon
Richard A. Sterba
Christian A. Chu
Scott A. Elengold
FISH & RICHARDSON P.C.
1425 K Street, N.W., 11th Floor
Washington, D.C. 20005
Telephone: (202) 783-5070

Attorneys for Respondents LG Electronics, Inc. and LG Electronics USA, Inc.

/s/ Eric C. Rusnak
Eric C. Rusnak
K&L GATES LLP
1601 K Street, NW
Washington, DC 20006-1600
Telephone: (202) 778-9000

Michael J. Bettinger
Timothy Walker
Curt Holbreich
Harold H. Davis, Jr.
Irene I. Yang
K&L GATES LLP
Four Embarcadero Center, 12th Floor
San Francisco, CA 94111
Telephone: (415) 882-8200

Michael J. Abernathy
Brian J. Arnold
K&L GATES LLP
70 West Madison Street, Suite 3100
Chicago, IL 60602-4207
Telephone: (312) 372-1121

Counsel for Respondent Novatel Wireless, Inc.

/s/ Aaron Wainscoat
Mark Fowler
Aaron Wainscoat
Carrie Williamson
Erik Fuehrer
DLA PIPER LLP (US)
2000 University Avenue
East Palo Alto, California 94303
Tel: 650-833-2000

Attorneys for Respondents Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc.

PUBLIC VERSION

/s/ Adam P. Seitz
Louis S. Mastriani
Sarah E. Hamblin
Daniel F. Smith
Dana L. Watts
ADDUCI, MASTRIANI & SCHAUMBERG, L.L.P.
1133 Connecticut Avenue, N.W., 12th Floor
Washington, DC 20036
Telephone: (202) 467-6300

Adam P. Seitz
Eric A. Buresh
Jason R. Mudd
ERISE IP, P.A.
6201 College Boulevard, Suite 300
Overland Park, KS 66211
Telephone: (913) 777-5600

Counsel for Respondents Garmin Ltd., Garmin International, Inc. and Garmin USA, Inc.

/s/ Jay H. Reiziss
Jay H. Reiziss
Michelle A. Miller
BRINKS HOFER GILSON & LIONE
1775 Pennsylvania Avenue, NW, Suite 900
Washington, D.C. 20006
(202) 296-6940 (phone)

William H. Frankel
Robert S. Mallin
Kori Anne Bagrowski
Hersh H. Mehta
BRINKS HOFER GILSON & LIONE
NBC Tower, Suite 3600
455 North Cityfront Plaza Drive
Chicago, IL 60611-5599
(312) 321-4200 (phone)

Attorneys for Respondents ZTE Corporation and ZTE (USA) Inc.

/s/ Stephen R. Smith
Stephen R. Smith
COOLEY LLP
11951 Freedom Drive
Reston, VA 20190
Tel.: 703.456.8000
Fax: 703.456.8100
Email: HTC-TPL@cooley.com

Kyle Chen
COOLEY LLP
3175 Hanover Street
Palo Alto, CA 94304
Tel: 650.843.5000
Fax: 650.849.7400
Email: HTC-TPL@cooley.com

Counsel for Respondents HTC Corp., HTC America, Inc., Nintendo Co., Ltd. and Nintendo of America Inc.

CERTIFICATE OF SERVICE

I, Matthew Salcedo, hereby certify that on October 28, 2013, a copy of the

[PUBLIC VERSION] RESPONDENTS' JOINT RESPONSE AND OPPOSITION TO COMPLAINANTS' PETITIONS FOR REVIEW OF THE FINAL INITIAL DETERMINATION

[PUBLIC VERSION] SUMMARY OF RESPONDENTS' JOINT RESPONSE AND OPPOSITION TO COMPLAINANTS' PETITIONS FOR REVIEW OF THE FINAL INITIAL DETERMINATION

was served on the following as indicated:

The Honorable Lisa R. Barton
Acting Secretary
U.S. International Trade Commission
500 E Street, S.W.
Washington, D.C. 20436

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The Honorable E. James Gildea
Chief Administrative Law Judge
U.S. International Trade Commission
500 E Street, S.W., Room 317
Washington, D.C. 20436
Email:
sarah.zimmerman@usitc.gov;
kenneth.schopfer@usitc.gov

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R. Whitney Winston
OFFICE OF UNFAIR IMPORT INVESTIGATIONS
U.S. International Trade Commission
500 E Street, S.W., Room 401
Washington, D.C. 20436
Email: Whitney.Winston@usitc.gov

☐ **Via Hand Delivery**
☐ **Via Overnight Courier**
☒ **Via Electronic mail**

For Complainants Technology Properties Limited, LLC and Phoenix Digital Solutions LLC:

James C. Otteson
AGILITY IP LAW, LLP
149 Commonwealth Drive
Menlo Park, CA 94025
Email: TPL853@agilityiplaw.com

☐ **Via Hand Delivery**
☐ **Via Overnight Courier**
☒ **Via Electronic mail**

Michelle G. Breit
James R. Farmer
OTTESON LAW GROUP
AGILITY IP LAW, LLP
14350 North 87th Street, Suite 190
Scottsdale, AZ 85260

For Complainant Patriot Scientific Corporation:

Charles T. Hoge
KIRBY NOONAN LANCE & HOGE LLP
350 Tenth Avenue, Suite 1300
San Diego, CA 92101
Email: choge@knlh.com

☐ **Via Hand Delivery**
☐ **Via Overnight Courier**
☒ **Via Electronic mail**

For Respondents Acer, Inc., Acer America Corporation, Amazon.com, and Novatel Wireless, Inc.:

Eric C. Rusnak
K&L GATES LLP
1601 K Street, NW
Washington, DC 20006-1600
Email: AcerAmazonNovatel_ITC853@klgates.com

☐ **Via Hand Delivery**
☐ **Via U.S. Mail**
☒ **Via Electronic mail**

For Respondent Barnes & Noble, Inc.:

Paul F. Brinkman
QUINN EMANUEL URQUHART &SULLIVAN, LLP
1299 Pennsylvania Avenue NW, Suite 825
Washington, DC 20004
Email: BN-853@quinnemanuel.com

☐ **Via Hand Delivery**
☐ **Via U.S. Mail**
☒ **Via Electronic mail**

For Respondents Garmin Ltd., Garmin International, Inc., and Garmin USA, Inc.:

Louis S. Mastriani
ADDUCI, MASTRIANI & SCHAUMBERG, LLP
1133 Connecticut Avenue, N.W., 12th Floor
Washington, DC 20036
Email: Garmin-853@adduci.com

☐ **Via Hand Delivery**
☐ **Via U.S. Mail**
☒ **Via Electronic mail**

Adam P. Seitz
Eric A. Buresh
Jason R. Mudd
ERISE, IP, P.A.
6201 College Boulevard, Suite 300
Overland Park, KS 66211
Email: Garmin_853@eriseIP.com

☒ **Via Electronic Mail**

For Respondents HTC Corporation, HTC America:

Stephen R. Smith
COOLEY LLP
11951 Freedom Drive
Reston, VA 20190
Email: HTC-TPL@cooley.com

☐ **Via Hand Delivery**
☐ **Via U.S. Mail**
☒ **Via Electronic mail**

For Respondents Huawei Technologies Co., Ltd., Huawei DeviceCo., Ltd., Huawei Device USA Inc., and Futurewei Technologies, Inc.:

Timothy C. Bickham
STEPTOE & JOHNSON LLP
1330 Connecticut Avenue, NW
Washington, DC 20036
Email: Huawei853@steptoe.com

☐ **Via Hand Delivery**
☐ **Via U.S. Mail**
☒ **Via Electronic mail**

For Respondents Kyocera Corporation, Kyocera Communications, Inc.:

M. Andrew Woodmansee
MORRISON &FOERSTER LLP
12531 High Bluff Drive
San Diego, CA 92130
Email: Kyocera-TPL-ITC@mofo.com

☐ **Via Hand Delivery**
☐ **Via U.S. Mail**
☒ **Via Electronic mail**

For Respondents LG Electronics, Inc., LG Electronics U.S.A., Inc.:

Scott Elengold
FISH & RICHARDSON P.C.
1425 K Street, N.W., Suite 1100
Washington, D.C. 20005
Email: LG-TPLITCService@fr.com

☐ **Via Hand Delivery**
☐ **Via U.S. Mail**
☒ **Via Electronic mail**

For Respondents Nintendo Co., Ltd., Nintendo of America, Inc.:

Stephen R. Smith
COOLEY LLP
11951 Freedom Drive
Reston, VA 20190
Email: Nintendo-TPL@cooley.com

☐ **Via Hand Delivery**
☐ **Via U.S. Mail**
☒ **Via Electronic mail**

For Respondents ZTE Corporation and ZTE (USA) Inc.:

Jay H. Reiziss
BRINKS HOFER GILSON & LIONE
1775 Pennsylvania Avenue, NW
Suite 900
Washington, DC 20006
Email: Brinks-853-ZTE@brinksgilson.com

☐ **Via Hand Delivery**
☐ **Via U.S. Mail**
☒ **Via Electronic mail**

/s/ Matthew Salcedo

Matthew Salcedo
Senior Paralegal
DLA Piper LLP (US)
2000 University Avenue
East Palo Alto, CA 94303
Telephone: 650-833-2000
Facsimile: 650-833-2001