(Counsel listed on signature page)

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

TECHNOLOGY PROPERTIES LIMITED LLC, et al.,

Plaintiffs,

v.

HUAWEI TECHNOLOGIES CO., LTD., HUAWEI DEVICE CO., LTD., HUAWEI DEVICE USA INC., FUTUREWEI TECHNOLOGIES, INC., HUAWEI TECHNOLOGIES USA INC.,

Defendants.

Case No. 3:12-cv-03865-VC (PSG)

PLAINITIFFS' MOTION FOR DE NOVO DETERMINATION OF DISPOSITIVE MATTER REFERRED TO MAGISTRATE JUDGE, OR, IN THE ALTERNATIVE, MOTION FOR RELIEF FROM NONDISPOSITIVE PRETRIAL ORDER OF MAGISTRATE JUDGE

DATE: **Nov. 19, 2015**
TIME: **10:00am**
PLACE: **Courtroom 4**
JUDGE: **Hon. Vince Chhabria**

TECHNOLOGY PROPERTIES LIMITED LLC, et al.,

Plaintiffs,

v.

ZTE CORPORATION and ZTE (USA) INC.,

Defendants.

Case No. 3:12-cv-03876-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al.,

Plaintiffs,

v.

SAMSUNG ELECTRONICS CO., LTD. and SAMSUNG ELECTRONICS AMERICA, INC.,

Defendants.

Case No. 3:12-cv-03877-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. LG ELECTRONICS, INC. and LG ELECTRONICS U.S.A., INC., Defendants.	Case No. 3:12-cv-03880-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. NINTENDO CO., LTD. and NINTENDO OF AMERICA, INC., Defendants.	Case No. 3:12-cv-03881-VC (PSG)

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NOTICE OF MOTION AND MOTION

TO THE COURT AND ALL COUNSEL OF RECORD:

NOTICE IS HEREBY GIVEN that on November 19, 2015, at 10:00 AM, or as soon thereafter as counsel may be heard in Courtroom 4 of the above-titled court, located at 450 Golden Gate Avenue San Francisco, CA 94102, Plaintiffs will and hereby do move the Court for a *de novo* determination of dispositive matter referred to magistrate judge, or, in the alternative, motion for relief from non-dispositive pretrial order of magistrate judge, pursuant to Civil L.R. 72.

This motion is based upon this notice, the accompanying memorandum of points and authorities, the accompanying declaration of Barry Bumgardner, all pleadings, papers and records on file in this action, including the record of the *Markman* hearing held in front of Judge Paul Grewal on September 18, 2015, and any oral argument presented at the hearing on this matter.

STATEMENT OF RELIEF

For the reasons set forth below, Plaintiffs seek a *de novo* review of the Report & Recommendation of Judge Grewal regarding his construction of the term "entire oscillator."

MEMORANDUM IN SUPPORT

I. INTRODUCTION

On September 22, 2015, Judge Grewal issued a "Claim Construction Report and Recommendation" (hereinafter the "R&R") construing the term "entire oscillator disposed upon said integrated circuit substrate" of U.S. Pat. No. 5,809,336 (the "'336 Patent"). See Ex. A[1] (Dkt. 104,[2] Report & Recommendation). Judge Grewal's R&R improperly finds disclaimer associated with the "entire oscillator" term where none exists, and, importantly, has the effect of granting summary judgment of non-infringement in favor of the Defendants in each of the above-styled

[1] All exhibits cited in this brief are attached to the accompanying Declaration of Barry J. Bumgardner in Support of Plaintiffs' Motion for De Novo Determination.

[2] Unless otherwise indicated, docket numbers refer to documents from *Technology Properties Ltd., et al. v. Samsung Electronics Co., Ltd.*, Case. No. 3:12-cv-3877.

cases. In addition, even if subject matter was disclaimed during the prosecution of the '336 Patent, the disclaimer certainly is not as broad as the one described in the R&R. As a result of the dispositive nature of this issue, Plaintiffs move for a *de novo* determination of the meaning of the "entire oscillator" term. Should the Court consider the R&R to be non-dispositive, Plaintiffs move in the alternative that the Court find that Judge Grewal's R&R was clearly erroneous.

In the parties' claim construction briefing, both Defendants (who submitted a joint claim construction brief) and Plaintiffs agreed principally on the meaning of the sole disputed term, an "entire oscillator disposed upon said integrated circuit" as "an oscillator that is located entirely on the same semiconductor substrate as the central processing unit." Plaintiffs argued this should have been the complete construction of the term. Defendants, on the other hand, argued that the construction should include additional language – "and does not rely on a control signal or an external crystal/clock generator to cause clock signal oscillation or control clock signal frequency" – to reflect subject matter that was "disclaimed" during the prosecution of the '336 Patent. Ultimately, Judge Grewal agreed with the parties as to what the "entire oscillator" was – "an oscillator that is located entirely on the same semiconductor substrate as the central processing unit", but came to his own conclusion as to the disclaimer, finding that the claimed "entire oscillator" was one "that does not require a control signal and whose frequency is not fixed by any external crystal." Plaintiffs object to Judge Grewal's claim construction.

II. PROCEDURAL POSTURE

Each of the above-styled cases (collectively, the "California Actions") is a civil action alleging infringement of the '336 Patent. The suits, originally filed on July 24, 2012, were stayed pending an investigation at the International Trade Commission (the "ITC Investigation"). The ITC Investigation concluded on March 21, 2014, after which the stay was lifted in the California Actions. In addition to the ITC Investigation and California Actions, a trial was held in the Northern District of California, with Plaintiff HTC Corp. seeking a declaratory judgment of non-infringement and Defendants (the Plaintiffs in the California Actions) pursuing a counterclaim of infringement. The trial, held in front of Judge Grewal, resulted in a jury finding of infringement of certain HTC products. While on appeal, Plaintiffs and HTC settled their

dispute. On October 17, 2014, the California Actions subject to the present motion were consolidated in front of Judge Grewal for pretrial matters. See Dkt. 16.

After the parties exchanged simultaneous opening and responsive claim construction briefs (See, Exs. B-E, Dkts. 94, 95, 96, and 97), a *Markman* hearing was held on September 18, 2015, in front of Judge Grewal. On September 22, Judge Grewal issued his R&R, providing a construction of the "entire oscillator" term. As a result of this ruling, Plaintiffs and four of the five Defendants (excepting Huawei) agreed to move to stay the underlying actions, with the exception of claim construction objections, and stipulated that under the construction recommended by Judge Grewal in the R&R, "all accused products of all [moving Defendants] do not infringe the asserted claims."[3] See Ex. F, Dkt. 105 ("Joint Motion to Stay").

III. OVERVIEW OF THE '336 PATENT

The '336 Patent issued on September 15, 1998 and is based on an application filed on August 3, 1989. See Ex. H, U.S. Pat. No. 5,809,336. While pending at the United States Patent and Trademark Office ("USPTO"), the patent examiner contested the patentability of the pending claims, issuing four rejections prior to ultimately granting the patent. Applicants responded by distinguishing the claims of the '336 Patent from the cited references. After adding the limitations of a then pending dependent claim regarding a second independent clock for clocking external devices at the behest of the patent examiner, the application was allowed. The '336 Patent has been involved in litigation both in this district and the Eastern District of Texas, as well as at the ITC. It has been the subject of six reexamination requests, resulting in two reexaminations certificates. In total, the '336 Patent has already overcome more than 600 prior art references that were raised against it during prosecution and/or reexamination.

The "entire oscillator" term has been construed several times. The constructions reached by the various tribunals that have looked at the issue are found in Plaintiffs' Opening *Markman*

[3] On Friday, October 2, 2015, Judge Grewal granted a contested motion staying Plaintiffs' case against Huawei. See Ex. G, *Technology Properties Ltd., et al. v. Huawei Technologies Co., Ltd. et al.*, Case. No. 3:12-cv-3865, Dkt. 104. In each of the above cases, Plaintiffs assert independent claims 6 and 13, along with dependent claims 7, 9, 14, and 15 (the "Asserted Claims").

Brief. See Ex. C at pp. 1-5 (presenting a summary of how other tribunals have treated the "entire oscillator" term). Notably, Judge Grewal's recommended construction of "entire oscillator" does not comport with any of these prior constructions, including the one issued by Judge Grewal in the HTC case.

IV. APPLICABLE LAW

A. Objecting to a Magistrate Judge's Order

A party may object to a magistrate judge's order. FED. R. CIV. P. 72. If the matter is non-dispositive, the district judge reviews the order to determine whether the magistrate's decision was clearly erroneous. *Id.* When the magistrate judge rules on a dispositive motion, the district judge must determine *de novo* any part of the magistrate's order that was objected to. *Id.* Although 28 USC § 636(b)(1)(A) contains a list of "dispositive" motions, the list is not all-inclusive. In the 9th Circuit, courts look to the effect of an order to determine if the matter is dispositive. *United States v. Rivera-Guerrero*, 377 F.3d 1064, 1068 (9th Cir. 2004).

B. Claim Construction Law

This Court is generally familiar with the various tenets of claim construction, so a general discussion of the applicable law is not included. Prosecution disavowal/disclaimer, however, is a more nuanced subject. While the words of a claim are normally given their customary and ordinary meaning, "there are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows [also referred to in cases as "disclaims"] the full scope of a claim term either in the specification or during prosecution." *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012), citing *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1580 (Fed. Cir. 1996). The standard for disavowal/disclaimer of claim scope is exacting. *Thorner*, 669 F.3d at 1366. "The patentee may demonstrate intent to deviate from the ordinary and accustomed meaning of a claim term by including in the specification expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope." *Id.*

Any disclaimers that are found must be the result of statements made by the patentee/applicant during the prosecution of the patent at issue. *North Am. Container Inc. v.*

Plastipak Packaging Inc., 415 F.3d 1335, 1345-46 (Fed. Cir. 2005). As stated by Defendants in their responsive brief:

> The focus must be on the arguments applicants made to distinguish [the prior art at issue], as those are what define the disclaimer. . . . As the Federal Circuit made clear in *North Am. Container*, for example, the scope of the disclaimers must be measured by *what the applicants said during prosecution*, not by what was necessary to distinguish the claims from the prior art. 415 F.3d at 1340-41.

Ex. D, Defendants' Responsive Claim Construction Brief, Dkt. 96 at 5 (emphasis in original). Thus, in determining what, if any disavowals/disclaimers were made by patentee/applicant during the prosecution of a patent, the analysis must look to the words used by patentee/applicant, as those words "define" the disclaimer. Notably, though, to qualify as disclaimer, these statements must be "clear and unmistakable" as the Federal Circuit has "consistently rejected prosecution statements too vague or ambiguous to qualify as a disavowal of claim scope." *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1325-26 (Fed. Cir. 2003).

V. ARGUMENT

These objections are made to Judge Grewal's R&R regarding construction of the claim term "an entire oscillator disposed upon a single integrated circuit." Judge Grewal construed the "entire oscillator" term as "an [oscillator] located entirely on the same semiconductor substrate as the [central processing unit] that does not require a control signal and whose frequency is not fixed by any external crystal." The basis of Judge Grewal's construction is his erroneous finding that Applicants made certain disclaimers during the prosecution of the '336 Patent. Based upon the erroneous finding of disclaimer, Judge Grewal improperly included negative limitations into the claim construction (*i.e.*, "that does not require a control signal and whose frequency is not fixed by any external crystal"). Because Judge Grewal's claim construction (if adopted) has the effect of being case dispositive, thus the Court should review it under a standard of *de novo* review. FED. R. CIV. P. 72(b)(3). Even if this Court determines that the issue is not properly classified as dispositive, Judge Grewal's R&R should be modified because it is clearly erroneous. FED. R. CIV. P. 72(a).

A. The R&R Issued by Judge Grewal is Case Dispositive and therefore the Construction of the Entire Oscillator Term is Subject to *De Novo* Review.

The clear impact of Judge Grewal's construction of the "entire oscillator" term is summary judgment of non-infringement in favor of Defendants, thus making this a dispositive issue requiring *de novo* review. The Federal Rules distinguish between the standard of review required for objections to a magistrate judge's order on dispositive and non-dispositive matters. When an objection to a magistrate judge's order is properly made, orders which are dispositive receive a *de novo* determination by the District Judge, who may accept, reject, or modify the magistrate judge's opinion. FED. R. CIV. P. 72(b). Those issues which are non-dispositive are entitled to review by the district judge under a "clearly erroneous" standard. FED. R. CIV. P. 72(a). While Rule 72 does not indicate which matters are dispositive, 28 U.S.C. § 636(b)(1)(A) lists several motions which are considered dispositive and entitled to *de novo* review. This list is not exhaustive. In the 9th Circuit, courts look to the effect of an order to determine if the matter is dispositive to a claim or defense of a party. *Rivera-Guerrero*, 377 F.3d at 1067-68. "[W]e do not simply look to the list of excepted pretrial matters in order to determine the magistrate judge's authority. Instead, we must look to the effect of the motion, in order to determine whether it is properly characterized as 'dispositive or non-dispositive of a claim or defense of a party.'" *Id.* at 1068, citing *Maisonville v. F2 Am., Inc.*, 902 F.2d 746 (9th Cir. 1990).

The plain effect of Judge Grewal's R&R is judgment of non-infringement in favor of Defendants. Three days after Judge Grewal's issued the R&R, the parties (with the exception of Huawei), filed a joint stipulation stating that "the parties hereby stipulate that all accused products of all Defendants in this Action do not infringe the asserted claims of U.S. Patent 5,809,336 under the Entire Oscillator Construction." Dkt. 105 at ¶4. It is indisputable that the effect of the R&R is dispositive, and Plaintiff's timely objection to the R&R requires *de novo* review by this Court.

This situation is not unusual, as claim construction rulings are frequently case dispositive. In fact, Northern District Patent L.R. 4-3(c) expressly recognizes the potentially dispositive nature of claim construction, requesting the parties to identify which of the claim terms whose

construction may be dispositive. In this particular instance, Defendants identified the "entire oscillator" construction as potentially dispositive. See Ex. I, Joint P.R. 4-3 statement, Dkt. 72 at 4. Evidencing this belief, Defendants directed a significant amount of their presentation at the *Markman* hearing toward non-infringement. During the "tutorial" phase of the *Markman* hearing, Defendants spent significant time discussing the nature of their own products, a subject which had nothing to do with claim construction and everything to do with non-infringement. During the "argument" phase of the *Markman* hearing, counsel for Defendants spoke at length about the importance of this claim term toward non-infringement. Defendants also harkened to non-infringement in their opening *Markman* brief, explicitly comparing the '336 Patent to accused products. Ex. B at 13-14. Having prevailed before Judge Grewal on the "entire oscillator" construction, Defendants effectively secured a judgement of non-infringement, which requires this Court to review Judge Grewal's determination *de novo*.

B. The Applicants Did Not Make the Alleged Disclaimers

Judge Grewal's construction of "entire oscillator" is based on a finding that the Applicants made certain "disclaimers" while distinguishing their invention from two prior art references: U.S. Pat. No. 4,503,500 ("Magar") and U.S. Pat. No. 4,670,837 ("Sheets").[4] R&R at 4. Plaintiffs dispute that any disclaimer actually occurred during Applicants' correspondence with the USPTO. Indeed, several courts (as well as Judge Grewal himself) have previously construed the "entire oscillator" term, and none of them found the sweeping disclaimer advocated by Judge Grewal in his R&R. This record begs the obvious question – how can there be "clear and unmistakable" disavowal of the broad scope advocated by Judge Grewal if several, experienced patent judges have reviewed the same record as Judge Grewal and reached a different conclusion? The answer is readily apparent – no clear and unmistakable disavowal exists in the patent prosecution, and Judge Grewal's finding of clear and unmistakable disclaimer is erroneous.

Applicants distinguished Magar and Sheets on the basis of existing claim limitations. But

[4] Plaintiffs refer to those who prosecuted the '336 Patent in the USPTO as "Applicants", as the entities that owned the application that became the '336 Patent were different entities than Plaintiffs.

even if some disclaimers exist (which Plaintiffs dispute), they are not as broad as those found by Judge Grewal. As discussed in detail below, even if one does find that Applicants did disclaim "something" during the prosecution of the '336 Patent, the subject matter actually disclaimed is far less than that described in the R&R. At most, the proper scope of disclaimer should be an oscillator "that does not require command, manual, or programmed inputs to change frequency and excluding external crystals/clocks to generate a clock signal."

1. Magar

Judge Grewal's construction includes the limitation that the oscillator of the '336 Patent cannot have a frequency that is "fixed by any external crystal." The R&R purports to justify this limitation by examining the arguments made to distinguish the present invention from Magar. The statements made by the Applicants, however, do not support the construction provided, particularly if examined in light of the Magar disclosure.

Magar, attached as Ex. J, was drawn to a specialized processor that would be optimized for performing certain arithmetic tasks. Ex. J, 6:34, et seq. In explaining the specialized processor, Magar describes a particular clocking scheme that involves an external crystal and a component called "CLOCK GEN," seen in the bottom right of Figure 2a. Ex. J, Fig 2a and 15:23-41. Figures 2 and 3 of Magar, along with column 15 of Magar, demonstrate how Magar utilizes the external crystal to generate a 20MHz clock signal. That clock signal drives the on-chip "CLOCK GEN" circuitry shown in Figure 2 and diagramed in Figure 3. Ex. J at Figs. 2a, 3, 15:23-41. After receiving the 20MHz signal via pins X1 and X2, the "CLOCK GEN" circuitry in Magar creates four quarter-cycle clocks seen in Q1-Q4, having a period of 200 nanoseconds (a 5MHz clock signal). *Id.* at 15:23-35. Importantly, there is no on-chip oscillator in Magar. Rather, the clock signal for the CPU is generated by the off-chip crystal. Stated differently, Magar is a one-oscillator system. This is critical to understanding the statements made to the USPTO.

As explained in Plaintiffs' responsive brief to Judge Grewal (see Ex. E at 2-9), the statements relied upon by Defendants in their briefing and Judge Grewal in the R&R do not support a finding of disclaimer. In fact, Applicants' statements during prosecution distinguish

Magar based on existing claim limitations, and clarify that (unlike Magar) the claimed invention does not rely on an external oscillator to generate a clock signal. The oscillator in the claimed invention is on-chip – and, thus, the clock signal is generated on-chip, while Magar's clock is off-chip, a difference specifically captured by the explicit language of the claim.

Judge Grewal, however, cites four sections of Applicants' responses to Magar to support his construction, alleging that the statements made to the USPTO require a finding of disclaimer. Yet, when examined closely, the statements do not create disclaimer individually, nor do they create disclaimer when taken as a whole.

Judge Grewal first cites the Applicants' argument to the USPTO as found in their July 7, 1997 Office Action Response. *See* R&R at 4, lns. 14-18, *see also* Ex. K, July 7, 1997 Office Action Response at 3-4. Judge Grewal alleges that this paragraph is an attempt to "distinguish Magar by emphasizing that the clock disclosed in Magar was fixed by a crystal that was external to the microprocessor, unlike their on-chip variable speed clock." R&R at 4. Judge Grewal is correct that it the Applicants argued that Magar used an external crystal, and that those crystals are fixed frequency. Further, Applicants state that the microprocessor clock is frequency controlled by a crystal. But, a "clock" is not the same thing as an oscillator. See Ex. K at 4, (explaining Applicants' position that all oscillators are clocks but not all clocks are oscillators). The statement above, made in reference to Magar, makes sense because Magar did not have an on-chip oscillator, rather it only contained the on-chip CLOCK GEN circuitry. Thus, the statement above does not support Judge Grewal's construction that the "entire oscillator" is not "fixed by any off-chip oscillator" simply because the Applicants did not disclaim any interaction between an off-chip oscillator and an on-chip oscillator.

Judge Grewal continues that "applicants also argued that the Magar clock could not practice the claimed invention because of its reliance on a crystal, which by its nature cannot vary its oscillation frequency." R&R at 4. In support of this argument, Judge Grewal cites to Applicants' argument found in the R&R at 4-5. See Ex. K at 4. But once again, the statement by the Applicants does not support Judge Grewal's construction. Specifically, there is no mention of an off-chip oscillator having any involvement with an on-chip oscillator. This makes sense

because Magar is a single-oscillator system. Applicants could not have disclaimed that the '336 Patent's oscillator's frequency "is not fixed by any external crystal" because there was no opportunity to do so, and they did not make such a clear, unambiguous statement at the USPTO.

Judge Grewal notes that the USPTO "issued a second rejection based on Magar, and the Applicants responded by emphasizing again that the claimed invention did not rely on an external crystal's fixed frequency to set the clock's frequency rate." R&R at 5. Judge Grewal cites the statement from the prosecution history found in the R&R at 5, lns. 8-10 for support. *See* Ex. L, February 10, 1998 Office Action Response at 4. But, the cited passage does not support the construction promoted by Judge Grewal. Although Applicants state that the frequency originates from an external crystal, they do not say anything about fixing a frequency of an on-chip oscillator.

Lastly, Judge Grewal states that "[t]he applicants also disclaimed the use of an external crystal to cause clock signal oscillation," citing a final passage from the prosecution history for support. See R&R at 5, citing Ex. L at 3. Here, as before, there is no oscillator on the Magar chip that can be controlled by the off-chip oscillator. Applicants clarify that the "clock generator" is not an entire oscillator in itself. They argue that Magar shows a crystal which is used to generate a clock, but say nothing of an off-chip oscillator fixing the frequency of an on-chip oscillator.

In the aggregate, the four statements relied upon by Judge Grewal do not and cannot support the disclaimer featured in Judge Grewal's construction. Indeed, Applicants' statements clearly distinguish the present invention from Magar on the basis of limitations already present in the claims at issue (*e.g.*, varying frequency as a "function of parameter variation in one or more fabrication or operational parameters," such as voltage or temperature). Applicants' statements could support a construction that states that the clock signal provided to the CPU does not originate from or is not generated by an external oscillator. As discussed above, there is only a single oscillator in Magar that supplies a clock signal to the CPU, as is there in the claims of the '336 Patent. But, the construction found in the R&R contemplates the interaction of an on-chip oscillator with an off-chip one. The interaction of two oscillators was never discussed with

respect to Magar, because the reference does not contemplate such an arrangement, just as the '336 Patent does not contemplate this arrangement. Yet, Judge Grewal found that, based on Applicants' words, such subject matter was disclaimed. This is clear error: the interaction of two oscillators cannot be disclaimed if Applicants' never mentioned this subject.

Finally, if any disclaimer with respect to Magar is appropriate, it is one that prohibits a clock signal being *generated* from an off-chip oscillator. Not only would a limitation of "not generated by an off-chip oscillator" be more consistent with the arguments presented to the USPTO, it would also be consistent with prior constructions provided by the ITC, Judge Ward in the Eastern District of Texas, and Judge Grewal himself in the HTC case. See Ex. B at 16, chart listing prior claim constructions.

2. Sheets

The second disclaimer found in Judge Grewal's "entire oscillator" construction concerns statements made by the Applicant in securing allowance of the '336 Patent over Sheets. Based on these statements, Judge Grewal found that the claimed "entire oscillator" term cannot "require a control signal." But, a close review of the statements made by Applicant reveals that the Applicants made no such disavowal. Further, even if Applicant did disclaim subject matter, the scope of the disclaimer is materially narrower than what was found by Judge Grewal.

Sheets (attached as Ex. M) describes a system in which a "microprocessor controls the clock frequency [of the microprocessor] based on the present rate of required microprocessor activity." Ex. M at Abstract. Thus, the goal of the invention described in Sheets is to save energy by running the microprocessor at a lower clock speed when high performance is not needed (and hence use less power). *Id.* Due to this variable speed processor, Sheets is unlike Magar, whose clock is generated by a fixed frequency crystal.

Sheets accomplishes this goal by having the microprocessor periodically determine its processing load. If the load is low, the microprocessor will reduce the clock frequency at which it is driven. *Id.* at 1:45-57. Sheets achieves this reduction in clock frequency by operating with a digital voltage controlled oscillator ("VCO"). *Id.* at 2:54-57. This oscillator generates the clock signal used by the microprocessor in Sheets. *Id.*

In simpler terms, the computer system in Sheets can speed up or slow down based on how much work it has to do. When the system runs faster, it consumes more power, but can process more data. When it runs slower, it consumes less power, but processes less data. The processor in Sheets makes the determination of how much work is queued up, then sets the VCO (which directly determines how fast/slow the system runs) accordingly.

The processor in Sheets causes the VCO to generate a clock speed at a particular frequency by writing a "digital word" to the VCO. *Id.* at 1:60-68. As used in Sheets, a "digital word" is simply a digital value (e.g., 234). Sheets makes clear that the processor writes the digital word to the VCO in the same manner as the word would be written to RAM. So, just as the processor can write/store data to memory, it can write digital data to the VCO. This digital word is stored by the VCO and then used to compute the clock rate output by the VCO.

Judge Grewal's R&R focuses on three paragraphs from the '336 Patent's file history regarding Sheets. See R&R at 5-6, citing Ex. N, at 8, Ex. O, at 4, and Ex. K at 5. These paragraphs are the (apparent) basis for Judge Grewal's finding of disclaimer and are the same passages cited by Defendants in their briefs. Relying on these paragraphs, Judge Grewal crafted a construction that excludes oscillators that "require a control signal" from the scope of the Asserted Claims, finding that Applicants disclaimed such material.

Plaintiffs disagree that these three paragraphs evidence any disclaimer, let alone a disclaimer of the scope found by Judge Grewal. As discussed in Plaintiff's responsive brief (see Ex. E at 9-14), Applicants' statements to the USPTO regarding Sheets evidence no more than the fact that Sheets does not meet the literal language of what became the Asserted Claims. The doctrine of prosecution disclaimer is meant to exclude subject matter that would otherwise be within the scope of the claims, but for the disclaimers. In Sheets, there is no disclosure of how Sheets' oscillator can vary other than by having a digital word written to it. Thus, the Sheets processor does not vary as a function of environmental or fabrication parameters, which is explicitly required by the Asserted Claims. For this reason, Applicants' comments should not be read to disclaim subject matter that would otherwise be within the scope of the claims.

As Defendants repeatedly state, disclaimers that originate in prosecution arise from the words used by Applicants. Assuming arguendo that Applicants disclaimed subject matter in arguing for the allowance of the Asserted Claims over Sheets, the disclaimer found by Judge Grewal goes far beyond what Applicants actually stated.

This disclaimer found by Judge Grewal is defective in two important aspects. First, it applies to "control signals" generally. The universe of what can be considered a "control signal" is large when compared to the specific inputs at issue in Sheets. Plaintiffs believe it is improper to saddle Plaintiffs with the difference in scope between Sheet's signals/inputs and general "control signals" because Applicants never discussed "control signals" in the abstract, instead specifically referring to "***Sheet's system for providing*** control signals."[5] That fact alone demonstrates that Judge Grewal's finding of disclaimer with respect to all "control signals" is not proper.

Second, Judge Grewal's construction prohibits the "entire oscillator" from "requiring" a "control signal" for ostensibly any purpose. Again, as the cited arguments make clear, whatever input/signals that were being disclaimed were only being used for the purposes of changing the frequency/clock speed of the "external clock" at issue. A control signal could possibly be used in conjunction with an oscillator for a number of reasons other than to control the speed of the oscillator. Again, if Applicants' words are to form the basis of the alleged disclaimers, the scope of the disclaimers must be commensurate with what was actually said. In this case, the scope of Applicants' comments is limited to using specific inputs for changing the frequency of an oscillator. Thus, finding disclaimer for the use of "control signals" for purposes other than changing the frequency of the oscillator goes well beyond Applicants' words and is improper.

A proper disclaimer should not be based on some judicially-created abstraction of Applicants' comments. Applicants' specific statements refer to command, programmed, or manual control inputs to change the frequency of the oscillator. To the extent any clear and

[5] Applicants did refer to "Sheets' system for providing clock control signals to an external clock . . . ." in the paragraph cited in the R&R on pp. 5-6. This reference to control signals was clearly limited to the ones discussed in Sheets and not to "control signals" generally.

unmistakable disclaimer was made, which Plaintiffs strongly dispute, it would necessarily relate to only this subject matter.

Turning now to the particular words used by Applicants in discussing Sheets, the first citation relied upon by Judge Grewal distinguishes Sheets from the Asserted Claims based on the "control information" found in Sheets. The discussion in this paragraph is not a generalized discussion of "control information." Rather, it is specific to the "control information" disclosed in Sheets (*i.e.*, the digital word written by the processor to the VCO).

In the second citation relied upon by Judge Grewal, Applicants characterize the digital word of Sheets as a "command input." If a disclaimer is to be found in this citation, it must be limited to an oscillator that requires "command inputs" to change the frequency. Again, these "command inputs" refer to the disclosure in Sheets of the microprocessor writing a digital value to the VCO. In this paragraph, Applicants did not mention "control signals."

Finally, in the third and last paragraph cited by Judge Grewal with respect to Sheets, Applicants state that the oscillator described in the Asserted Claims "does not require manual or programmed inputs . . . to [vary in frequency]." Again, there is no discussion of "control signals" in this portion of Applicant's response. Rather, on the topic of "inputs", the discussion is limited to "manual or programmed inputs." Thus, like the preceding citations, the statements made by Applicants are far more limited than the disclaimer found by Judge Grewal.

In summary, the R&R finds the term "entire oscillator" does not include oscillators that require a "control signal." This finding is based on Applicants statements in distinguishing over Sheets. But, Applicants' never made such a sweeping disclaimer in the prosecution history. At most, Applicants' statements distinguished the claimed oscillator as one that does not require "command, manual, and programmed inputs" to change its frequency. But even these statements are not clear and unmistakable disclaimers.

VI. CONCLUSION

As discussed above, Judge Grewal incorrectly found that Applicants disclaimed subject matter during the prosecution of the patent application that ultimately became the '336 Patent. During that prosecution, Applicants demonstrated that Magar and Sheets both fell outside the

explicit requirements of the then pending claims. With respect to Magar, the Asserted Claims require the "entire oscillator" to reside on the same chip as the CPU and to vary with the CPU as a function of certain environmental and process related variables. The quartz oscillator in Magar is neither on-chip nor can it vary like the claimed oscillator. The same goes for Sheets - it is an off-chip oscillator that is not disclosed as varying like the oscillator recited in the Asserted Claims. For these reasons, there is simply no cause to find that Applicants disclaimed subject matter that would otherwise be captured by the Asserted Claims.

Further, despite Plaintiffs' beliefs to the contrary, if Applicants did disclaim subject matter that would otherwise be covered by the Asserted Claims, the scope of such disclaimer is much narrower than that found by Judge Grewal. A review of the statements made by Applicants demonstrates as much. With respect to Magar, Applicants' statements all centered on the fact that the off-chip quartz oscillator in Magar could not generate a clock signal like the one described in the Asserted Claims. Thus, a disclaimer finding that the claimed oscillator does not include "external crystals/clocks to generate a clock signal" is more appropriate than the one found in the R&R. With respect to Sheets, Applicants merely discussed Sheet's use of "command, manual, and programmed inputs" to "change the frequency" of the oscillator in Sheets. Accordingly, if a disclaimer is to be found with respect to Sheets, it should only exclude oscillators "that require command, manual, or programmed inputs to change frequency."

Dated: October 6, 2015

Respectfully submitted,

/s/ Barry J. Bumgardner

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CERTIFICATE OF SERVICE

I hereby certify that, on October 6, 2015, I caused the foregoing document to be served on counsel of record via the Court's CM/ECF system.

Dated: October 6, 2015

By: */s/ Barry J. Bumgardner*
Barry J. Bumgardner

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

TECHNOLOGY PROPERTIES LIMITED LLC, et al.,

Plaintiffs,

v.

HUAWEI TECHNOLOGIES CO., LTD., HUAWEI DEVICE CO., LTD., HUAWEI DEVICE USA INC., FUTUREWEI TECHNOLOGIES, INC., HUAWEI TECHNOLOGIES USA INC.,

Defendants.

Case No. 3:12-cv-03865-VC (PSG)

DECLARATION OF BARRY J. BUMGARDNER IN SUPPORT OF PLAINTIFFS' MOTION FOR DE NOVO DETERMINATION

DATE: **Nov. 19, 2015**
TIME: **10:00am**
PLACE: **Courtroom 4**
JUDGE: **Hon. Vince Chhabria**

TECHNOLOGY PROPERTIES LIMITED LLC, et al.,

Plaintiffs,

v.

ZTE CORPORATION and ZTE (USA) INC.,

Defendants.

Case No. 3:12-cv-03876-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al.,

Plaintiffs,

v.

SAMSUNG ELECTRONICS CO., LTD. and SAMSUNG ELECTRONICS AMERICA, INC.,

Defendants.

Case No. 3:12-cv-03877-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. LG ELECTRONICS, INC. and LG ELECTRONICS U.S.A., INC., Defendants.	Case No. 3:12-cv-03880-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. NINTENDO CO., LTD. and NINTENDO OF AMERICA, INC., Defendants.	Case No. 3:12-cv-03881-VC (PSG)

I, Barry J. Bumgardner, submit this declaration in support of Plaintiffs' Motion for De Novo Determination, and declare as follows:

1. I am a partner at the law firm of Nelson Bumgardner, P.C., attorneys of record for Phoenix Digital Solutions LLC ("PDS"). If called as a witness, I could and would testify competently to the information set forth in this declaration.

2. Attached as **Exhibit A** is a true and correct copy of the claim construction report and recommendation in *Technology Properties Ltd. et al. v. Samsung Elecs. Co., Ltd., et al.*, No. 3:12-cv-03877, Dkt. No. 104 (N.D. Cal., June 15, 2007).

3. Attached as **Exhibit B** is a true and correct copy of the Defendants' opening claim construction brief in *Technology Properties Ltd. et al. v. Samsung Elecs. Co., Ltd., et al.*, No. 3:12-cv-03877, Dkt. No. 94.

4. Attached as **Exhibit C** is a true and correct copy of the Plaintiffs' opening claim construction brief in *Technology Properties Ltd. et al. v. Samsung Elecs. Co., Ltd., et al.*, No. 3:12-cv-03877, Dkt. No. 95.

5. Attached as **Exhibit D** is a true and correct copy of the Defendants' responsive claim construction brief in *Technology Properties Ltd. et al. v. Samsung Elecs. Co., Ltd., et al.*, No. 3:12-cv-03877, Dkt. No. 96.

6. Attached as **Exhibit E** is a true and correct copy of the Plaintiffs' responsive claim construction brief in *Technology Properties Ltd. et al. v. Samsung Elecs. Co., Ltd., et al.*, No. 3:12-cv-03877, Dkt. No. 97.

7. Attached as **Exhibit F** is a true and correct copy of the Joint Motion to Stay All Proceedings and Deadlines Pending Resolution of Objections to Claim Construction Report and Recommendation in is a true and correct copy of the Defendants' opening claim construction brief in *Technology Properties Ltd. et al. v. Samsung Elecs. Co., Ltd., et al.*, No. 3:12-cv-03877, Dkt. No. 105.

8. Attached as **Exhibit G** is a true and correct copy of Judge Grewal's Order Granting Stay in *Technology Properties Ltd. et al. v. Huawei Techs. Co., Ltd., et al.*, No. 3:12-cv-03865, Dkt. No. 104.

9. Attached as **Exhibit H** is a true and correct copy of U.S. Pat. No. 5,809,336 to Moore et al.

10. Attached as **Exhibit I** is a true and correct copy of Patent Local Rule 4-3 Joint Claim Construction and Prehearing Statement in *Technology Properties Ltd. et al. v. Samsung Elecs. Co., Ltd., et al.*, No. 3:12-cv-03877, Dkt. No. 72.

11. Attached as **Exhibit J** is a true and correct copy of U.S. Pat. No. 4,503,500 to Magar.

12. Attached as **Exhibit K** is a true and correct copy of an excerpt from the Patent File History of U.S. Pat. No. 5,809,336, specifically the Response to Office Action of July 7, 1997.

13. Attached as **Exhibit L** is a true and correct copy of an excerpt from the Patent File History of U.S. Pat. No. 5,809,336, specifically the Response to Office Action of February 10, 1998.

14. Attached as **Exhibit M** is a true and correct copy of U.S. Pat. No. 4,670,837 to

Sheets.

15. Attached as **Exhibit N** is a true and correct copy of an excerpt from the Patent File History of U.S. Pat. No. 5,809,336, specifically the Response to Office Action of April 15, 1996.

16. Attached as **Exhibit O** is a true and correct copy of an excerpt from the Patent File History of U.S. Pat. No. 5,809,336, specifically the Response to Office Action of January 13, 1997.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. This declaration is executed on October 6, 2015 in Fort Worth, Texas.

Dated: October 6, 2015

By: /s/ *Barry J. Bumgardner*
Barry J. Bumgardner

Exhibit "A"

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. HUAWEI TECHNOLOGIES CO., LTD., et al., Defendants.	Case No. 3:12-cv-03865-VC **CLAIM CONSTRUCTION REPORT AND RECOMMENDATION**
TECHNOLOGY PROPERTIES LIMITED LLC, ET AL., PLAINTIFFS, V. ZTE CORPORATION, et al., DEFENDANTS.	Case No. 3:12-cv-03876-VC
TECHNOLOGY PROPERTIES LIMITED LLC, ET AL., PLAINTIFFS, V. SAMSUNG ELECTRONICS CO., LTD., et al., DEFENDANTS.	Case No. 3:12-cv-03877-VC

TECHNOLOGY PROPERTIES LIMITED LLC, ET AL., PLAINTIFFS, V. LG ELECTRONICS, INC., et al., DEFENDANTS.	Case No. 3:12-cv-03880-VC
TECHNOLOGY PROPERTIES LIMITED LLC, ET AL., PLAINTIFFS, V. NINTENDO CO., LTD., et al., DEFENDANTS.	Case No. 3:12-cv-03881-VC

The parties to this patent infringement suit dispute the construction of just one claim term in U.S. Patent No. 5,809,336: "an entire oscillator disposed upon said integrated circuit substrate."[1] At issue is the impact of various statements made by the patent applicant to the examiner during the patent's prosecution. Because these statements would be understood by one of ordinary skill in the art as disclaiming certain scope of the disputed "entire oscillator" term, the court RECOMMENDS construction of the term to reflect this disclaimer, as follows: "an [oscillator] located entirely on the same semiconductor substrate as the [central processing unit] that does not require a control signal and whose frequency is not fixed by any external crystal."

I.

Consistent with the Supreme Court's admonition in 1886 that a patent claim not be "a nose of wax, which may be turned and twisted in any direction,"[2] the Federal Circuit has long held that a claim term must be understood as limited if the applicant argued as much during prosecution in

[1] *See* Docket No. 89 at 6-7.

[2] *White v. Dunbar*, 119 U.S. 47, 51 (1886).

order to overcome prior art.[3] "'[T]he prosecution history can often inform the meaning of the claim language by demonstrating . . . whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be.'"[4]

Plaintiff Technology Property Limited and Patriot Scientific brought these patent infringement suits for infringement of three patents: U.S Patent Nos. 5,440,749, 5,530,890 and 5,809,336. Only the '336 patents remains at issue; the others were dismissed by stipulation.[5] The '336 patent, titled "High Performance Microprocessor Having Variable Speed System Clock," was derived along with the others from a single patent application that was subject to nothing less than a ten-way restriction requirement. The result is that the '336 specification includes much discussion that is irrelevant to that which the '336 patent specifically claims.[6]

The '336 patent claims an invention that allows the frequency of a central processing unit, the brains of any computing device, to fluctuate based on local conditions. Traditional microprocessors use off-chip, fixed frequency clocks to regulate the CPU's frequency.[7] One result is that the clock needs to be set lower than the CPU's maximum possible frequency to ensure proper operation under worst-case conditions. The '336 patent solves this problem by placing a ring oscillator on the same silicon substrate as the CPU to act as the CPU's clock. Because the ring oscillator is on the same silicon substrate and is made of the same components as the CPU, it is subject to the same environmental conditions and thus will allow the CPU to operate at higher rates

[3] *See, e.g., Southwall Techs., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995); *see also Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319, 1325 (Fed. Cir. 2002) ("Explicit arguments made during prosecution to overcome prior art can lead to a narrow claim interpretation because '[t]he public has a right to rely on such definitive statements made during prosecution.'") (quoting *Digital Biometrics, Inc. v. Identix, Inc.*, 149 F.3d 1335, 1347 (Fed. Cir. 1998)).

[4] *Abbott Labs. v. Sandoz, Inc.*, 566 F.3d 1282, 1289 (Fed. Cir. 2009) (quoting *Phillips v. AWH Corp.*, 415 F.3d 1303, 1317 (Fed. Cir. 2005) (en banc)).

[5] *See* Docket No. 86; all docket references are to Case No. 3:12-cv-03865-VC.

[6] *See, e.g.*, Docket No. 28-3, Ex. C at 3:27-35, 16:43-17:37.

[7] *See* Docket No. 28-3, Ex. C at 16:48-50, 17:12-13.

during good conditions and lower rates during bad. As the specification explains, the microprocessor may "operate over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing" that "all affect transistor gate propagation delays."[8] Because other devices with which the microprocessor communicates, both on-chip and off-chip, cannot tolerate a variable speed clock, a second, conventional "crystal clock" is separately connected to the input/output interface.[9]

During the '336 patent's prosecution, the applicants made a variety of arguments to the examiner to overcome two key prior art references: U.S. Patent No. 4,503,500 ("Magar") and U.S. Patent No. 4,670,837 ("Sheets"). With respect to Magar, the examiner initially rejected the claims after noting that certain circuitry in Magar was fabricated on the same microprocessor substrate as the CPU, as required by the claims. The applicants then attempted to distinguish Magar by emphasizing that the clock disclosed in Magar was fixed by a crystal that was external to the microprocessor, unlike their on-chip variable speed clock:

> [O]ne of ordinary skill in the art should readily recognize that the speed of the CPU and clock *do not* vary together due to manufacturing variation, operating voltage, and temperature of the IC in the Magar processor . . . This is simply because the Magar microprocessor clock is frequency controlled by a crystal which is also external to the microprocessor. Crystals are by design fixed frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The Magar microprocessor in no way contemplates a variable speed clock as claimed.[10]

In the same amendment, the applicants also argued that the Magar clock could not practice the claimed invention because of its reliance on a crystal, which by its nature cannot vary its oscillation frequency:

> [C]rystal oscillators have never, to Applicants' knowledge, been fabricated on a single silicon substrate with a CPU, for instance. Even if they were, as previously mentioned, crystals are by design fixed-frequency devices whose oscillation

[8] Docket No. 28-3, Ex. C at 16:44-48.

[9] *See* Docket No. 28-3, Ex. C at 17:14-34, Fig. 17.

[10] Docket No. 90-7, Ex. D at 3-4.

> frequency is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The oscillation frequency of a crystal on the same substrate with the microprocessor would inherently not vary due to variations in manufacturing, operating voltage and temperature in the same way as the frequency capability of the microprocessor on the same underlying substrate, as claimed.[11]

The PTO nonetheless issued a second rejection based on Magar, and the applicants responded by emphasizing again that the claimed invention did not rely on an external crystal's fixed frequency to set the clock's frequency rate:

> The essential difference is that the frequency or rate of the . . . signals is determined by the processing and/or operating parameters of the integrated circuit containing the . . . circuit, while the frequency or rate of the . . . signals depicted in Magar . . . are determined by the fixed frequency of the external crystal.[12]

The applicants also disclaimed the use of an external crystal to cause clock signal oscillation:

> Magar's clock generator relies on an external crystal connected to terminals X1 and X2 to oscillate . . . . It is not an entire oscillator in itself. And with the crystal, the clock rate generated is also conventional in that it is a fixed, not a variable, frequency. The Magar clock is comparable in operation to the conventional crystal clock 434 depicted in Fig. 17 of the present application for controlling the I/O interface at a fixed rate frequency, and not at all like the clock on which the claims are based.[13]

The examiner similarly issued an initial rejection in view of Sheets. In response, the applicants distinguished their "present invention" from microprocessors that rely on frequency control information from an external source:

> The present invention does not similarly rely upon provision of frequency control information to an external clock, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, since the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance.

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[11] *Id.* at 4.

[12] *Id.* at 4.

[13] *Id.* at 3.

> Sheets' system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.[14]

Because the applicants referred to the "present invention" in this statement, their disclaimer applies to all claims.[15]

But that disclaimer, like the prior disclaimers, could not secure allowance. In response to a subsequent rejection, the applicants went even further and disclaimed the use of controlled inputs altogether, regardless whether the control is on-chip or not:

> Even if the examiner is correct that the variable clock in Sheets is in the same circuit as the microprocessor of system 100, that still does not give the claimed subject matter. In Sheets, a command input is required to change the clock speed. In the present invention, the clock speed varies correspondingly to variations in operating parameters . . . . No command input is necessary to change the clock frequency.[16]

Thus, according to applicants, controlling the on-chip oscillator's speed using a command signal "does not give the claimed subject matter."[17] Indeed, in a later amendment, the applicants left no doubt that, unlike "all cited references," the claimed oscillator is completely free of inputs and extra components:

> Crucial to the present invention is that . . . when fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together. This differs from all cited references in that . . . the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so.[18]

After overcoming these and other objections by the examiner, the '336 patent issued on September 15, 1998. The patent has been construed in three previous litigations, including

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[14] Docket No. 90-9, Ex. F at 8.

[15] *See, e.g., Ballard Med. Prods. v. Allegiance Healthcare Corp.*, 268 F.3d 1352, 1360-62 (Fed. Cir. 2001).

[16] Docket No. 90-10, Ex. G at 4.

[17] *Id.*

[18] Docket No. 90-7, Ex. D at 5.

one before the undersigned that resulted in a nine-day trial. In the Eastern District of Texas, Judge Ward construed the "entire ring oscillator" claim term in claim 1 to preclude reliance on either a control signal or an external crystal/clock generator to generate a clock signal.[19] In reaching this conclusion, Judge Ward explained: "The Court agrees with the defendants that the applicant disclaimed the use of an input control signal and an external crystal/clock generator to generate a clock signal."[20]

Similarly, in a United States International Trade Commission investigation, Judge Gildea construed "entire oscillator" as precluding reliance on either a control signal or an external crystal/clock generator to generate a clock signal.[21] Judge Gildea found that Plaintiffs clearly and unambiguously disclaimed any oscillator that relies on a control signal or an external crystal or frequency generator.[22] The Commission affirmed Judge Gildea's construction.[23]

Likewise, this court construed "ring oscillator" as "an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment,"[24] and instructed the jury that the term "entire oscillator" excludes any external clock used to generate the CPU clock signal.[25]

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[19] *See* Docket No. 90-15, Ex. L at 12.

[20] *Id.*

[21] *See* Docket No. 90-16, Ex. M at 40-41; Docket No. 90-17, Ex. N at 16-25.

[22] *See* Docket No. 90-20, Ex. Q at 39-40 (finding that "the essential point made by the applicants in seeking to gain acceptance" of their claims, and their "unqualified statements in distinguishing" the prior art, constituted a "clear disavowal" of claim scope).

[23] *See* Docket No. 90-17, Ex. N at 16-25.

[24] *See Acer, Inc. v. Tech. Properties Ltd.*, No. 5:08-CV-00877 PSG, 2013 WL 4515545, at *5 (N.D. Cal. Aug. 21, 2013).

[25] *See* Docket No. 90-13, Ex. J at 26; Docket No. 90-14, Ex. K at 2; *see also* Docket No. 90-18, Ex. O at 11, and n.24.

The parties to this litigation agree that the disputed term must be limited as "an [oscillator] that is located entirely on the same semiconductor substrate as the [central processing unit]."[26] Where they disagree is whether the term should further be limited to read as "an [oscillator] that is located entirely on the same semiconductor substrate as the [central processing unit] and does not rely on a control signal or an external crystal/clock generator to cause clock signal oscillation or control clock signal frequency."[27]

II.

This court has jurisdiction under 28 U.S.C. §§ 1331 and 1338. The presiding judge referred all pretrial matters to the undersigned pursuant to Fed. R. Civ. P. 72(a).[28]

"To construe a claim term, the trial court must determine the meaning of any disputed words from the perspective of one of ordinary skill in the pertinent art at the time of filing."[29] This requires a careful review of the intrinsic record comprised of the claim terms, written description and prosecution history of the patent.[30]

While claim terms "are generally given their ordinary and customary meaning,"[31] the claims themselves and the context in which the terms appear "provide substantial guidance as to the meaning of particular claim terms."[32] Indeed, a patent's specification "is always highly relevant

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[26] Docket No. 89 at 7.

[27] *Id.*

[28] *See* Docket No. 17.

[29] *Chamberlain Group, Inc. v. Lear Corp.*, 516 F.3d 1331, 1335 (Fed. Cir. 2008).

[30] *See id.* ("To construe a claim term, the trial court must determine the meaning of any disputed words from the perspective of one of ordinary skill in the pertinent art at the time of filing. Intrinsic evidence, that is the claims, written description, and the prosecution history of the patent, is a more reliable guide to the meaning of a claim term than are extrinsic sources like technical dictionaries, treatises, and expert testimony.") (citing *Phillips*, 415 F.3d at 1312).

[31] *Phillips*, 415 F.3d at 1312 (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)).

[32] *Phillips*, 415 F.3d at 1314

to the claim construction analysis."[33] Claims "must be read in view of the specification, of which they are part."[34]

Although the patent's prosecution history "lacks the clarity of the specification and thus is less useful for claim construction purposes," it "can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be."[35] The court also has the discretion to consider extrinsic evidence, including dictionaries, learned treatises and testimony from experts and inventors.[36] Such evidence, however, is "less significant than the intrinsic record in determining the legally operative meaning of claim language."[37] No extrinsic evidence is necessary to resolve the dispute here, however, because the intrinsic record is dispositive that the applicant disclaimed certain claim scope to convince the examiner to issue the patent.

III.

"[T]here is no principle of patent law that the scope of surrender of subject matter made during prosecution is limited to what is absolutely necessary to avoid a prior art reference that was the basis for an examiner's rejection."[38] Whether necessary or not to get the examiner to avoid Magar and Sheets, the applicant here surrendered subject matter that the definition of the "entire oscillator" term must account, albeit in language different than that proposed by either side.

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[33] *Phillips*, 415 F.3d at 1312-15.

[34] *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995); *see also Ultimax Cement Mfg. Corp v. CTS Cement Mfg. Corp.*, 587 F. 3d 1339, 1347 (Fed. Cir. 2009).

[35] *Phillips*, 415 F.3d at 1317 (internal quotations omitted).

[36] *See id.* ("Although we have emphasized the importance of intrinsic evidence in claim construction, we have also authorized district courts to rely on extrinsic evidence, which 'consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises.'") (quoting *Markman*, 52 F.3d at 980).

[37] *Phillips*, 415 F.3d at 1317 (citing *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 862 (Fed. Cir. 2004)) (internal quotations and additional citations omitted).

[38] *Norian Corp. v. Stryker Corp.*, 432 F.3d 1356, 1361 (Fed. Cir. 2005).

To avoid Magar, the applicants surrendered any oscillator that like Magar's is fixed by an off-chip crystal. Over and over again, the applicants insisted that its claims did not read on Magar because of this distinction. Whether styled by the applicants as an "essential difference" or "not at all like the clock on which the claims are based,"[39] Magar is distinct from the invention because it fixes the frequency of the CPU with a crystal oscillator that is not on the same silicon substrate. Having sold the Patent Office on this distinction, and told the world the same in the prosecution history, the applicants understood that they could not later claim anything else. The Federal Circuit has taught this lesson over and over again.[40]

[39] Docket No. 90-8, Ex. E at 3, 4.

[40] *See, e.g.*, *Southwall*, 54 F.3d at 1576 ("Claims may not be construed one way in order to obtain their allowance and in a different way against accused infringers."); *Rheox*, 276 F.3d at 1325 ("Explicit arguments made during prosecution to overcome prior art can lead to a narrow claim interpretation because '[t]he public has a right to rely on such definitive statements made during prosecution.'"); *Gillespie v. Dywidag Sys. Int'l, USA*, 501 F.3d 1285, 1291 (Fed. Cir. 2007) ("The patentee is held to what he declares during the prosecution of his patent."); *Computer Docking Station Corp. v. Dell, Inc.*, 519 F.3d 1366, 1379 (Fed. Cir. 2008) (holding that "the sum of the patentees' statements during prosecution would lead a competitor to believe that the patentee had disavowed coverage of laptops" and, thus, affirming. the trial court's construction of the portable computer limitation); *Seachange Int'l, Inc. v. C-COR, Inc.*, 413 F.3d 1361, 1372-75 (Fed. Cir. 2005) ("Where an applicant argues that a claim possesses a feature that the prior art does not possess in order to overcome a prior art rejection, the argument may serve to narrow the scope of otherwise broad claim language."); *see also Am. Piledriving Equip. v. Geoquip, Inc.*, 637 F. 3d 1324, 1336 (Fed. Cir. 2011) ("[A]n applicant's argument that a prior art reference is distinguishable on a particular ground can serve as a disclaimer of claim scope even if the applicant distinguishes the reference on other grounds as well."); *Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) ("The purpose of consulting the prosecution history in construing a claim is to 'exclude any interpretation that was disclaimed during prosecution.'"; "Accordingly, 'where the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender.'") (citations omitted); *Microsoft Corp. v. Multi-Tech. Sys., Inc.*, 357 F.3d 1340, 1349 (Fed. Cir. 2004) (a court "cannot construe the claims to cover subject matter broader than that which the patentee itself regarded as comprising its invention and represented to the PTO"); *Springs Window Fashions LP v. Novo Indus., L.P.*, 323 F.3d 989, 993-96 (Fed. Cir. 2003) (rejecting patentee's attempt to narrow the scope of disclaimer, even though the examiner did not rely on the disclaimer to issue the claims); *N. Am. Container Inc. v. Plastipak Packaging Inc.*, 415 F.3d 1335, 1345-46 (Fed. Cir. 2005) (holding that "the applicant, through argument [that the prior-art inner walls are 'slightly concave'] during the prosecution, disclaimed inner walls of the base portion having any concavity. . . . [a]lthough the inner walls disclosed in the [prior art] may be viewed as entirely concave").

The song remains much the same regarding Sheets. The applicants distinguished Sheets repeatedly on the ground that Sheets requires control signals, frequency control information or command inputs. In contrast, they characterize the invention upon relying upon or requiring any such signals, information or inputs.[41] Because applicants described this distinction as no less than "crucial," and applicable to the "present invention," their disclaimer applies to all claims.[42]

Plaintiffs principally argue that the distinctions drawn from Magar and Sheets are already expressly included in the patent claims themselves. It is true that the "on-chip/off-chip" distinction and the invention's variability depending on PVT are reflected in other limitations. But those other limitations do not get at the full range of distinctions drawn, especially the claimed invention's oscillator frequency not being fixed by any crystal off-chip and the oscillator not needing any control inputs. The Federal Circuit has been clear that claim construction must reflect all disclaimers, not merely a subset.[43]

The undersigned appreciates that the construction recommended differs from the constructions adopted in the Eastern District of Texas, the International Trade Commission and by the undersigned as presiding judge in *HTC*. It also must be noted that neither party urged this particular language. But putting aside any notion that this court is bound in this case by any prior construction, the recommended construction is consistent with the fundamental meaning of those earlier constructions. After multiple rounds of briefing by the parties and a lengthy hearing, the undersigned is convinced that the particular language urged recommended here best captures what actually happened at the patent office. In the universe of claim construction, that directive is ultimate prime.

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[41] *See* Docket No. 90-9, Ex. F at 8; *see also* Docket No. 90-10, Ex. G at 4.

[42] *See, e.g.*, *Ballard Med. Prods. v. Allegiance Healthcare Corp.*, 268 F.3d 1352, 1360-62 (Fed. Cir. 2001).

[43] *See Krippelz v. Ford Motor Co.*, 667 F.3d 1261, 1267 (Fed. Cir. 2012); *Am. Piledriving Equip. v. Geoquip, Inc.*, 637 F.3d 1324, 1336 (Fed. Cir. 2011); *Elkay v. Mgf. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 979 (Fed. Cir. 1999).

SO ORDERED.

Dated: September 22, 2015

PAUL S. GREWAL
United States Magistrate Judge

Exhibit "B"

(*Counsel listed on signature page*)

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. HUAWEI TECHNOLOGIES CO., LTD., et al., Defendants.	CASE NO. 3:12-cv-03865-VC (PSG) **DEFENDANTS' OPENING CLAIM CONSTRUCTION BRIEF** DATE: September 18, 2015 TIME: 10:00 AM PLACE: Courtroom 5, 4th Floor JUDGE: Hon. Paul S. Grewal

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. GARMIN LTD., et al., Defendants.	Case No. 3:12-cv-03870-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al. Plaintiffs v. ZTE CORPORATION, et al., Defendants.	Case No. 3:12-cv-03876-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. SAMSUNG ELECTRONICS CO., LTD., et al., Defendants.	CASE NO. 3:12-cv-03877-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. LG ELECTRONICS, INC., et al., Defendants.	Case No. 3:12-cv-03880-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. NINTENDO CO., LTD, et al. Defendants.	Case No. 3:12-cv-03881-VC (PSG)

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OTHER AUTHORITIES

Pursuant to Patent Local Rule 4-5 and the Court's Second Amended Case Management Order, Defendants Garmin International, Inc., Garmin USA, Inc., Huawei Technologies Co., Ltd., Huawei Device Co., Ltd., Huawei Device USA, Inc., Futurewei Technologies, Inc., Huawei Technologies USA, Inc., LG Electronics, Inc., LG Electronics U.S.A., Inc., Nintendo Co., Ltd., Nintendo of America Inc., Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., ZTE Corporation and ZTE (USA) Inc. (collectively, "Defendants") submit the following Opening Claim Construction Brief.

I. INTRODUCTION

The only patent remaining in the above-captioned cases is U.S. Patent No. 5,809,336 (the "'336 patent"). The parties dispute the construction of only one claim term – "an entire oscillator disposed upon said integrated circuit substrate" – which appears in each of the two asserted independent claims. As the Court is aware from prior litigation involving Plaintiffs and the '336 patent, this claim term (or variations thereof) has been the subject of previous claim construction orders issued by this Court, the Eastern District of Texas, and the International Trade Commission. As confirmed in differing ways by all of the prior claim construction orders, the correct construction of this claim term must reflect the clear and unambiguous disclaimers that the applicants made during the prosecution of the '336 patent in order to obtain the claims over otherwise invalidating prior art. As established in detail below, applicants' clear prosecution disclaimers mandate that the claimed "entire oscillator" cannot rely on any off-chip crystal, off-chip clock generator, or control signal to cause clock signal oscillation or control clock signal frequency. While the prosecution disclaimers alone require this result, the specification's teachings, its criticisms of the prior art, and the plain claim language further support this conclusion.

II. OVERVIEW OF U.S. PATENT NO. 5,809,336

The '336 patent is directed to a variable-speed clock (the "entire oscillator") that controls the speed of a CPU and that is incorporated on the same integrated circuit substrate as the CPU.

Ex. A ('336 patent) at cover & 16:54-17:10.[1] The variable-speed oscillator adjusts its frequency in real time based upon the microprocessor's physical and environmental characteristics, including temperature, voltage and semiconductor manufacturing process quality, to track the then-existing processing capabilities of the CPU. *Id.* at 16:54-17:10. In other words, the on-chip oscillator's frequency varies together with the frequency capability of the CPU. *Id.*

The '336 patent issued as a divisional patent from a specification that describes several different purported inventions. Ex. A at cover ("Division of Ser. No. 389,334, Aug. 3, 1989, Pat. No. 5,440,749"). As a result, the '336 patent's "Summary of the Invention" section contains material that is largely irrelevant to the asserted claims, with only lines 27 through 35 of column 3 pertaining to the alleged invention. *Id.* at 3:27-35. Similarly, the "Detailed Description of The Invention" includes much extraneous material, with the only parts describing the '336 patent's purported invention being found in the last 25 lines of column 16 and the first 37 lines of column 17, under the sub-headings "Optimal CPU Clock Scheme" and "Asynchronous/Synchronous CPU." *Id.* at 16:43-17:37.

In the parts of the specification that are relevant to the alleged invention claimed in the '336 patent, the specification explains that a high speed microprocessor must "operate over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing" that "all affect transistor gate propagation delays." Ex. A at 16:44-48. These three parameters, "processing," "voltage" and "temperature," are referred to as "PVT" parameters.

As the specification explains, traditional prior art microprocessor systems are designed with a single fixed speed clock for all parts of the system. Ex. A at 16:48-50, 17:12-13. By design, this conventional fixed speed clock (which includes an off-chip crystal and on-chip components) always operates at a speed that is slow enough to ensure error-free operation during those times when worst case PVT parameter conditions may exist. *Id.* As a result, the traditional prior art microprocessor systems "must be clocked a factor of two slower than their maximum

[1] All exhibits cited in this brief are attached to the accompanying Declaration of Aaron Wainscoat in Support of Defendants' Opening Claim Construction Brief.

theoretical performance, so they will operate properly in worse [sic] case conditions" to ensure that a user always experiences error-free operation. *Id.* at 16:48-53.

To avoid the constrained speed of the prior art and to always operate at or near its maximum performance capabilities for the existing PVT parameter conditions, the '336 patent replaces the prior art's external fixed-speed crystal clock which controls the CPU's speed with an on-chip "ring counter variable speed system clock" (also referred to as a "ring oscillator variable speed system clock") that adjusts its speed in real time as a function of existing PVT parameters to match the CPU's maximum frequency capability under those parameters. Ex. A at 3:26-34, 16:54-17:10, 17:19-22. In other words, the oscillator's frequency varies together with the frequency of the CPU. *Id.* at 3:26-34, 16:60-17:2.

Unlike a fixed clock's speed, the frequency of the claimed internal variable speed oscillator varies significantly as a function of PVT parameters. Ex. A at 16:59-60 ("The ring oscillator frequency is determined by the parameters of temperature, voltage, and process"). For example, the '336 patent's specification discloses that the speed of the variable speed clock will be 100 megahertz at room temperature, but will slow to 50 megahertz if the temperature rises to 70°C (*i.e.*, 158° F). *Id.* at 16:59-63. The oscillator's speed may vary, according to the patent, by as much as a factor of four (*i.e.*, by as much as 400%) depending on all three PVT parameters. *Id.* at 17:21-22.

According to the '336 patent, the "optimum performance" of the variable speed oscillator supposedly results from fabricating and locating the variable speed oscillator on the same semiconductor substrate as the CPU, so that the same PVT parameters affect both the oscillator and the CPU. Ex. A at 16:57-58, 16:63-17:10. For example, if the temperature of the substrate rises, then the processing speed capability of the CPU decreases. But because the oscillator and CPU are fabricated on the same substrate, this rise in temperature also causes the speed of the variable speed oscillator to decrease, so that the oscillator leads the CPU to a slower maximum speed at which it can operate properly. *See id.* As the specification explains, this ensures that the CPU "will always execute at the maximum frequency possible, but never too fast." *Id.* at 16:67-17:2.

Because certain devices which communicate with the CPU cannot tolerate a variable speed clock, the system requires a second clock that is independent of the variable speed oscillator. Ex. A at 17:22-34. The independent second clock is connected to the input/output (I/O) interface, as illustrated in Figure 17 of the '336 patent, with the second clock on Figure 17 being a conventional "crystal clock" 434:

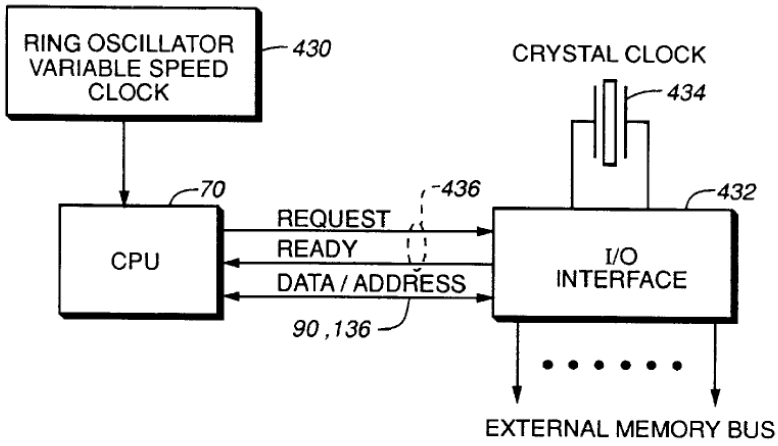


FIG._17

Each independent claim of the '336 patent (including asserted claims 6 and 13) provides for a fixed-speed, independent second clock that is connected to an input/output ("I/O") interface. Ex. A at 17:14-34. The frequency of the second clock is fixed to allow the I/O interface to interact with off-chip memory and other off-chip components, and to perform operations that require a fixed frequency, such as "video display updating and disc drive reading and writing." *Id.* at 17:14-34. By connecting the variable speed oscillator to the CPU while separately connecting the independent fixed speed clock to the I/O interface, the variable speed CPU is decoupled from the fixed speed I/O interface. *Id.* at 17:32-34. This configuration optimizes the performance of the system by allowing the CPU to run as fast as possible under the current PVT conditions while maintaining the I/O interface 432 at a stable fixed speed. *Id.* at 17:32-34.

III. CLAIM CONSTRUCTION LAW

When construing claim terms, the Federal Circuit emphasizes the importance of intrinsic evidence such as the language of the claims themselves, the specification, and the prosecution history. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-17 (Fed. Cir. 2005) (*en banc*). Claim

terms "are generally given their ordinary and customary meanings as understood by a person of ordinary skill in the art when read in the context of the specification and prosecution history." *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). There are two circumstances where a claim is not entitled to its plain and ordinary meaning: "1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution." *Id*. Courts may also consider "extrinsic evidence," which "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Phillips*, 415 F.3d at 1317 (quotation and citation omitted). However, such evidence is "less significant than the intrinsic record in determining the legally operative meaning of claim language." *Id*. (quotation and citation omitted).

Of particular importance here, the scope of a claim term must be limited if the applicant argued during prosecution that the claim has a limited scope in order to obtain the patent from the PTO. *Southwall Techs., Inc., v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995) ("Claims may not be construed one way in order to obtain their allowance and in a different way against accused infringers."); *Rheox, Inc. v. Entact, Inc*., 276 F.3d 1319, 1325 (Fed. Cir. 2002) ("Explicit arguments made during prosecution to overcome prior art can lead to a narrow claim interpretation because '[t]he public has a right to rely on such definitive statements made during prosecution'") (quoting *Digital Biometrics, Inc. v. Identix, Inc*., 149 F.3d 1335, 1347 (Fed. Cir. 1998)); *Abbott Labs. v. Sandoz, Inc.*, 566 F.3d 1282, 1289 (Fed. Cir. 2009) (*en banc*) ("'the prosecution history can often inform the meaning of the claim language by demonstrating . . . whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be.'") (quoting *Phillips*, 415 F.3d at 1317).

In short, "[t]he patentee is held to what he declares during the prosecution of his patent." *Gillespie v. Dywidag Systs. Int'l, USA*, 501 F.3d 1285, 1291 (Fed. Cir. 2007) (reversing district court's construction and determination of literal infringement because patentee's "construction was negated during prosecution."); *Computer Docking Station Corp. v. Dell, Inc*., 519 F.3d 1366, 1379 (Fed. Cir. 2008) (holding that "the sum of the patentees' statements during prosecution

would lead a competitor to believe that the patentee had disavowed" devices otherwise covered by the claim language). Thus, if an inventor defines a term or otherwise disclaims a meaning during prosecution, the inventor has acted as his own lexicographer and the term is limited to the scope of the definition or disclaimer. *Astrazeneca AB v. Mut. Pharm. Co., Inc*., 384 F.3d 1333, 1341-42 (Fed. Cir. 2004) (the inventor's reference to language in the specification as a "definition" constituted lexicography); *Schoenhaus v. Genesco, Inc*., 440 F.3d 1354, 1358-60 (Fed. Cir. 2006) (lexicography in file history by virtue of disclaimer of scope of claim term during prosecution).

IV. CLAIM CONSTRUCTION

The parties propose the following constructions of the term "an entire oscillator disposed upon said integrated circuit substrate," which is recited in asserted independent claims 6 and 13 of the '336 patent. Ex. A ('336 patent *Ex Parte* Reexamination Certificate) at 2:18-19, 3:34-35 (TPL853_00000053.)

Term	Defendants' Construction	Plaintiffs' Construction
an entire oscillator disposed upon said integrated circuit substrate	an oscillator that is located entirely on the same semiconductor substrate as the central processing unit and does not rely on a control signal or an external crystal/clock generator to cause clock signal oscillation or control clock signal frequency	An [oscillator] that is located entirely on the same semiconductor substrate as the [central processing unit].

The intrinsic evidence compels Defendants' construction because it embodies clear disclaimers of claim scope that the applicants made during the prosecution of the '336 patent to secure allowance of their claims over otherwise invalidating prior art. Defendants' construction is also consistent with the specification's teachings, its criticisms of the prior art, and the plain language of the claims. These unambiguous disclaimers and teachings in the intrinsic evidence mandate that the claimed "entire oscillator" cannot rely on any off-chip crystal, off-chip clock generator, or control signal to cause clock signal oscillation or control clock signal frequency. Defendants' construction incorporates these key disclaimers and teachings, while Plaintiffs' construction ignores them. Furthermore, as established below, by clearly incorporating these

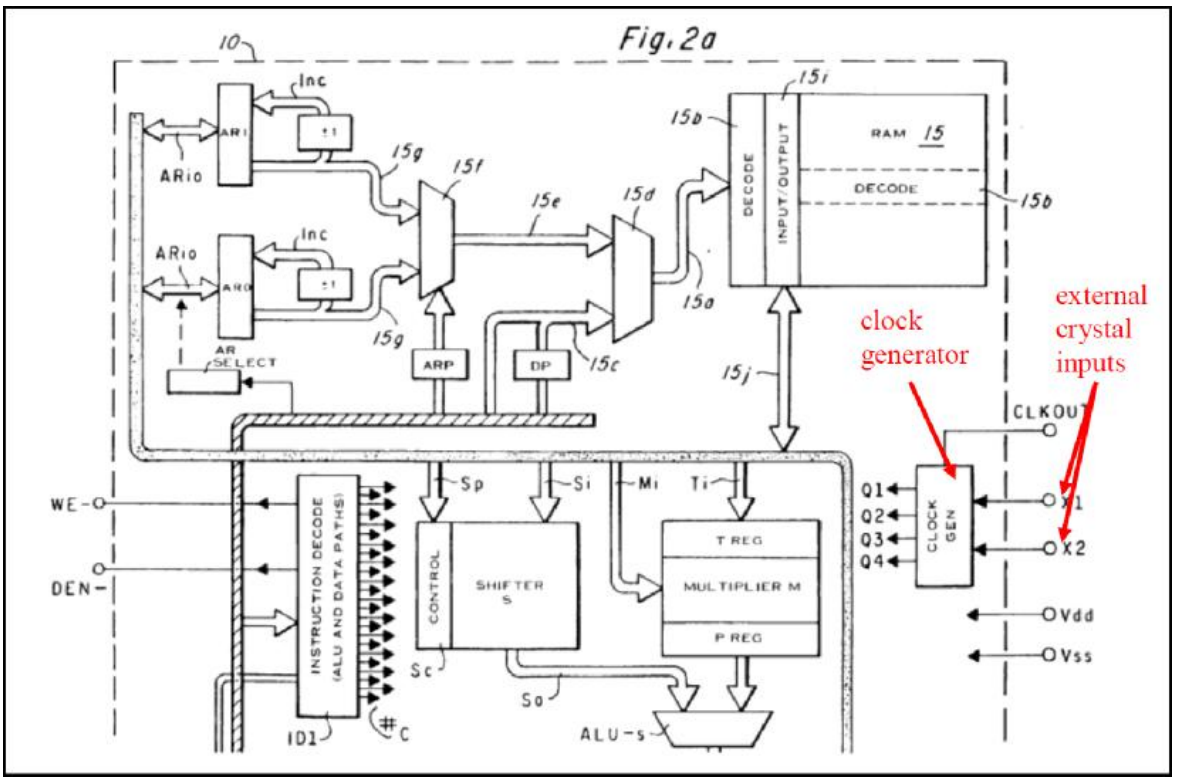
disclaimers into the construction, Defendants' construction avoids the ambiguity that was present in prior constructions of this term in prior litigations.

A. The '336 patent prosecution history compels Defendants' construction.

During prosecution of the '336 patent, the applicants repeatedly distinguished their purported invention from the prior art on the grounds that their on-chip oscillator does not rely on either an external crystal/clock generator or any control signal, to cause clock signal oscillation or control clock signal frequency. Applicants' prosecution history arguments constitute clear and unambiguous disclaimers that limit the scope of the "entire oscillator" limitation. Defendants' construction is correct because it recognizes and incorporates these key disclaimers, while Plaintiffs' construction wholly ignores them.

1. Applicants expressly disclaimed reliance on an external crystal or clock generator to control clock signal frequency or cause clock signal oscillation.

During prosecution, applicants expressly and repeatedly distinguished their purported invention from the prior art on the grounds that their on-chip oscillator does not rely on an external crystal or clock generator to cause clock signal oscillation or control clock signal frequency. More specifically, applicants argued that their on-chip oscillator does not rely on an external crystal or clock generator to (1) control the frequency of the clock signal, or (2) cause clock signal oscillation. These disclaimers began with applicants' attempt to overcome U.S. Patent No. 4,503,500 to Magar ("Magar"), Figure 2a of which is reproduced below. The examiner rejected the claims in view of Magar, correctly noting that the "CLOCK GEN" circuitry in Figure 2a was fabricated on the same microprocessor substrate 10 as the CPU, as is required by the claims.



Ex. B (Magar) at Fig. 2a (annotations in red added); Ex. C (April 3, 1997 Rejection) at 2 (TPL853_0002434). In response, applicants attempted to distinguish Magar on the basis that an external off-chip crystal (connected to the X1 and X2 inputs in the figure above) controlled the frequency of the clock:

> A review of the Magar reference shows that it is apparently no more pertinent than prior art acknowledged in the application, in that ***the clock disclosed in the Magar reference is in fact driven by a fixed frequency crystal, which is external to the Magar integrated circuit***.[2]

Ex. D (July 7, 1997 Amend.) at 2 (TPL853_00002426). Applicants then further emphasized the difference between their claimed on-chip variable speed clock and Magar's clock generator, which relies on the frequency of an external crystal:

> Contrary to the Examiner's assertion in the rejection that 'one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock vary together due to manufacturing variation, operating voltage and temperature of the IC [integrated circuit],' one of ordinary skill in the art should readily recognize that the speed of the CPU and clock ***do not*** vary together due to manufacturing variation, operating voltage, and

[2] Unless otherwise indicated, all emphasis in this brief is added by Defendants.

> temperature of the IC in the Magar processor . . . ***This is simply because the Magar microprocessor clock is frequency controlled by a crystal which is also external to the microprocessor.*** *Crystals are by design fixed frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature.* ***The Magar microprocessor in no way contemplates a variable speed clock as claimed.***

Id. at 3-4 (TPL853_00002427-28) (first emphasis in original). Thus, in this first amendment, applicants ***expressly and unambiguously disclaimed*** oscillators that rely on an external crystal ***for frequency control***.

Applicants then further argued in the same amendment that, even if the Magar crystal oscillator were located entirely on the same chip as the CPU, Magar would ***still*** not practice the claimed invention because Magar's clock could not vary with process, voltage and temperature ("PVT") parameters:

> ***[C]rystal oscillators have never***, to Applicants' knowledge, ***been fabricated on a single silicon substrate with a CPU***, for instance. ***Even if they were***, as previously mentioned, crystals are by design fixed-frequency devices whose oscillation frequency is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. ***The oscillation frequency of a crystal on the same substrate with the microprocessor would inherently not vary due to variations in manufacturing, operating voltage and temperature in the same way as the frequency capability of the microprocessor on the same underlying substrate, as claimed.***

Id. at 4 (TPL853_00002428). This express disclaimer could not be clearer: the claims exclude oscillators using crystals to ***control frequency*** of the clock signal. More specifically, an on-chip oscillator that does not vary as a function of the PVT parameters – such as an oscillator whose frequency is controlled by any crystal or control signal – is outside the scope of the claims.

Unconvinced, the PTO issued a second rejection based on Magar. In response, applicants amended their claims to explicitly require that the "entire" oscillator be on the same integrated circuit substrate as the CPU. Ex. E (Feb. 10, 1998 Amend.) at 1-2 (TPL853_02954557-58).[3] Along with this amendment, applicants again distinguished Magar on the ground that it relies on

[3] For example, prosecution claim 73, which ultimately issued as claim 6, was amended to recite "an entire oscillator disposed upon said integrated circuit substrate." Ex. E (Feb. 10, 1998 Amend.) at 1-2 (TPL853_02954557-58) (underlined text indicating addition through amendment).

an external crystal for frequency control, arguing that the "the ***essential*** difference" between Magar's fixed-frequency clock and the variable speed clock shown in Figure 18 of the '336 patent is that Magar's clock relies on a "fixed frequency of the external crystal" to set the "frequency or rate" of the clock:

> The signals PHASE 0, PHASE 1, PHASE 2 and PHASE 3 in Applicants' Fig. 18 are synonymous with Q1, Q2, Q3 and Q4 depicted in Magar Fig. 2a. The ***essential difference*** is that the ***frequency or rate of the PHASE 0, PHASE 1, PHASE 2 and PHASE 3 signals is determined by the processing and/or operating parameters of the integrated circuit*** containing the Fig. 18 circuit, ***while the frequency or rate of the Q1, Q2, Q3 and Q4 signals depicted in Magar Fig. 2a are determined by the fixed frequency of the external crystal*** connected to the circuit portion outputting the Q1, Q2, Q3 and Q4 signals shown in Magar Fig. 2a.

Id. at 4 (TPL853_02954560). By this statement, applicants again expressly distinguished their claimed invention from Magar on the ground that their invention does not, while Magar does, ***rely on a fixed frequency external crystal to control the "frequency or rate" of the clock***.

In addition to distinguishing Magar's clock from their purported invention based on the Magar clock's reliance on an external crystal for frequency control, applicants also distinguished Magar on the grounds that Magar's clock generator required an external crystal ***to cause clock signal oscillation***:

> Magar's clock generator ***relies on an external crystal*** connected to terminals X1 and X2 ***to oscillate***, as is conventional in microprocessor designs. It is not an entire oscillator in itself. And with the crystal, ***the clock rate generated is also conventional in that it is a fixed, not a variable, frequency***. The Magar clock is comparable in operation to the conventional crystal clock 434 depicted in Fig. 17 of the present application for controlling the I/O interface ***at a fixed rate frequency, and not at all like the clock on which the claims are based***, as has been previously stated.

Id. at 3 (TPL853_02954559).

Applicants concluded their argument about Magar by "specifically" distinguishing their claimed invention from an external crystal on the dual bases of ***frequency control*** and ***causing oscillation***:

> The Magar teaching . . . is specifically distinguished from the instant case in that it is both *fixed frequency* (*being crystal based*) and *requires an external crystal or external frequency generator*.

Id. at 5 (TPL853_02954561).

Thus, applicants distinguished Magar ***both*** (1) because the ***frequency*** of Magar's on-chip clock was controlled by an external crystal, ***and*** (2) because Magar's on-chip clock relied on an external crystal to ***cause oscillation***. In light of these clear disavowals, the correct construction of this claim term must capture both disclaimers. *Krippelz v. Ford Motor Co.*, 667 F.3d 1261,1267 (Fed. Cir. 2012) (affirming construction imposing two limitations on the disputed claim term, because patent owner distinguished the prior art on two separate grounds).[4]

The disclaimers are clear: Plaintiffs repeatedly told the Examiner and the public that their claimed "entire oscillator" does not rely on an external crystal or frequency generator to control the frequency of the clock signal or to cause clock signal oscillation. The claimed "entire oscillator" cannot cover what Plaintiffs disclaimed. *Southwall*, 54 F.3d at 1576 ("Claims may not be construed one way in order to obtain their allowance and in a different way against accused infringers."); *Rheox*, 276 F.3d at 1325 ("Explicit arguments made during prosecution to overcome prior art can lead to a narrow claim interpretation because '[t]he public has a right to rely on such definitive statements made during prosecution.'"); *Gillespie*, 501 F.3d at 1291 ("The patentee is held to what he declares during the prosecution of his patent."); *Computer Docking*, 519 F.3d at 1379 (holding that "the sum of the patentees' statements during prosecution would lead a competitor to believe that the patentee had disavowed coverage of laptops" and, thus, affirming the trial court's construction of the portable computer limitation); *Seachange Int'l, Inc. v. C-COR, Inc.*, 413 F.3d 1361, 1372-75 (Fed. Cir. 2005) ("Where an applicant argues that a claim possesses a feature that the prior art does not possess in order to overcome a prior art rejection, the argument may serve to narrow the scope of otherwise broad claim language.").[5]

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[4] Regardless of whether either or both of applicants' arguments distinguishing Magar ultimately were successful, or even necessary, in convincing the Examiner to allow the claims, the public is entitled to rely on them. *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 979 (Fed. Cir. 1999).

[5] *See also Am. Piledriving Equip. v. Geoquip, Inc.*, 637 F. 3d 1324, 1336 (Fed. Cir. 2011) ("[A]n applicant's argument that a prior art reference is distinguishable on a particular ground can serve as a disclaimer of claim scope even if the applicant distinguishes the reference on other grounds as well."); *Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) ("The purpose of consulting the prosecution history in construing a claim is to 'exclude any interpretation that was disclaimed during prosecution.'"; "Accordingly, 'where the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches

2. Applicants also clearly disclaimed reliance on control signals.

Applicants also repeatedly, clearly, and unambiguously disclaimed reliance on control signals to control the oscillator. The first of these disclaimers was made in response to a rejection by the Examiner in light of U.S. Patent No. 4,670,837 to Sheets ("Sheets"). Applicants distinguished their "present invention" from microprocessors that rely on frequency control information from an external source:

> ***The present invention*** does not similarly rely upon provision of frequency control information to an external clock, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit ***obviates the need for provision of the type of frequency control information described by Sheets***, since the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance. ***Sheets' system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention***.

Ex. F (April 11, 1996 Amend.) at 8 (TPL853_02954574). Because applicants referred to the "present invention" in this statement, their disclaimer applies to all claims. *See, e.g.*, *Ballard Med. Prods. v. Allegiance Healthcare Corp.*, 268 F.3d 1352, 1360-62 (Fed. Cir. 2001).

But that disclaimer, like the prior disclaimers, could not secure allowance. In response to a subsequent rejection, the applicants went even further and disclaimed the use of *controlled* oscillators altogether, regardless whether the control is on-chip or not:

> Even if the examiner is correct that the variable clock in Sheets is in the same circuit as the microprocessor of system 100, ***that still does not give the claimed subject matter***. ***In Sheets, a command input is required to change the clock speed.*** In the present invention, the clock speed varies

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and narrows the ordinary meaning of the claim congruent with the scope of the surrender.'") (citation omitted); *Microsoft Corp. v. Multi-Tech. Sys., Inc.*, 357 F.3d 1340, 1349 (Fed. Cir. 2004) (a court "cannot construe the claims to cover subject matter broader than that which the patentee itself regarded as comprising its invention and represented to the PTO"); *Springs Window Fashions LP v. Novo Indus., L.P.*, 323 F.3d 989, 993-96 (Fed. Cir. 2003) (rejecting patentee's attempt to narrow the scope of disclaimer, even though the examiner did not rely on the disclaimer to issue the claims); *N. Am. Container Inc. v. Plastipak Packaging Inc.*, 415 F.3d 1335, 1345-46 (Fed. Cir. 2005) (holding that "the applicant, through argument [that the prior-art inner walls are 'slightly concave'] during the prosecution, disclaimed inner walls of the base portion having any concavity . . . [a]lthough the inner walls disclosed in the [prior art] may be viewed as entirely concave").

> correspondingly to variations in operating parameters . . . ***No command input is necessary to change the clock frequency***.

Ex. G (January 8, 1997 Amend.) at 4 (TPL853_00002449). Thus, according to applicants, ***controlling*** the on-chip oscillator's speed using a command ***signal*** "does not give the claimed subject matter." *Id*. Indeed, in a later amendment, the applicants left no doubt that, unlike "all cited references," the claimed oscillator is completely free of inputs and extra components:

> ***Crucial to the present invention*** is that . . . when fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together. ***This differs from all cited references in that . . . the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so.***

Ex. D at 5 (TPL853_00002429).[6] Thus, applicants clearly stated that even an on-chip oscillator does not satisfy the claims if a control signal is required to change the frequency of the oscillator. *Id.* at 4-5 (TPL853_00002428-29). These repeated clear and unambiguous disavowals of claim scope not only support Defendants' construction; they compel it. *Southwall Techs.*, 54 F.3d at 1576; *Rheox*, 276 F.3d at 1325.

B. The '336 patent specification also supports Defendants' construction.

Defendants' construction also mirrors the clear-cut teaching in the specification of what the "entire oscillator" is. The title of the '336 patent is "High Performance Microprocessor Having a ***Variable Speed System Clock***." Consistent with this title, the specification criticizes prior art solutions that clocked a CPU with a fixed clock, such as, for example, a clock whose frequency is controlled by an external crystal:

> Traditional CPU designs are done so that with the worse [sic] case of the three parameters, the circuit will function at the rated clock speed. The result are designs that must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse [sic] case conditions.

Ex. A ('336 patent) at 16:48-53; *see also id.* at 17:12-33.

Rejecting the prior art fixed-speed clock approach (which is the approach used in the

[6] When a patentee uses terms such as "crucial to" and "in the present invention," this use has a special effect on the scope of the claim. *See Microsoft Corp.*, 357 F.3d at 1351-52 (construing claim to require a feature that was "central to the functioning of the claimed invention").

Defendants' accused products), the '336 patent discloses a variable-speed oscillator that is completely on the same semiconductor substrate as the CPU and whose speed freely varies with the PVT parameters of the substrate. As the specification explains, the frequency of the variable-speed oscillator is determined by the PVT parameters, so that the CPU can always operate at its maximum possible frequency:

> ***The ring oscillator frequency is determined by the parameters of temperature, voltage, and process***. At room temperature, the frequency will be in the neighborhood of 100 MHZ. At 70 degrees Centigrade, the speed will be 50 MHZ. ... ***By deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast***.

Ex. A at 16:54-17:2. In other words, by insulating the oscillator from any outside influence, the oscillator can vary and drive the CPU to execute at the fastest speed possible. *Id.* at 17:14-34.

Because the CPU must still communicate with the outside world, the patent discloses the use of an I/O interface which is clocked by an off-chip, fixed-speed crystal clock. *Id.* By decoupling the speed of these two clocks and allowing the frequency of the on-chip variable speed clock to vary with the PVT parameters while the I/O interface relies on an off-chip, fixed-speed crystal oscillator, the patent allegedly achieves "optimum performance" under any PVT parameters. *Id.*

Thus, according to the specification, the applicants chose to use a variable speed oscillator—which varies and is "determined by" PVT parameters—rather than the prior art's fixed speed clocks—which did not vary with the PVT parameters because their frequency was "fixed" by an external crystal or control signal. This was not simply a design choice. By disclosing that the applicants' free-running oscillator cures sub-optimal performance of the prior art's fixed speed clocks, the specification makes it clear that the applicants' oscillator is antithetical to the prior art's fixed-speed approach of allowing crystals, clocks, or signals to affect the oscillator's frequency.

In short, the specification disclaims the prior art's fixed-speed clocks (which rely on a crystal, clock, or signal to control the on-chip oscillator's frequency) in favor of a variable-speed oscillator (whose frequency is determined by PVT parameters) by claiming to overcome the

perceived deficiencies of the prior art fixed-frequency clocks. Defendants' construction correctly reflects these express teachings and disclaimers. *Chicago Bd. Options Exch. Inc. v. Int'l Secs. Exch. LLC*, 677 F.3d 1361, 1372 (Fed. Cir. 2012) (finding that "the specification goes well beyond expressing the patentee's preference" and that "its repeated derogatory statements...may be viewed as a disavowal of that subject matter from the scope of the Patents claims."); *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1341 (Fed. Cir. 2001) (holding "[w]here the specification makes clear that the invention does not include a particular feature, that feature is deemed to be outside the reach of the claims of the patent...."); *Phillips*, 415 F.3d at 1314 (the specification is the "single best guide to the meaning of a disputed term").

C. The claim language further supports Defendants' construction.

The claim language itself also precludes the use of a control signal or an external crystal to fix the frequency of the claimed "entire oscillator." In this regard, claims 6 and 13 expressly require that the "entire oscillator" vary in the same way as the CPU as changes occur in the PVT parameters:

> A microprocessor system comprising: ... an ***entire oscillator*** disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit ***at a clock rate*** and being constructed of a second plurality of electronic devices, ***thus varying the processing frequency*** of said first plurality of electronic devices [*i.e.*, the CPU] ***and the clock rate*** of said second plurality of electronic devices ***in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate*** ...

Ex. A ('336 patent) at claims 6, 13.

Unlike the ***claimed*** "entire oscillator" whose frequency (recited in these claims as the "clock rate") varies because it is determined by the PVT parameters, an oscillator whose frequency is determined by an external crystal is fixed.[7] As a result, that frequency does not (and cannot) vary with changes in the PVT parameters, as is expressly required by each of the asserted

[7] As applicants explained during prosecution, the meaning of "fixed" does not preclude small variations in oscillator frequency: "crystals are by design fixed-frequency devices whose oscillation frequency is designed to be ***tightly controlled*** and to ***vary minimally*** due to variations in manufacturing, operating voltage and temperature." Ex. D at 3-4 (TPL853_00002428).

claims. *Id.* Thus, the claim language itself dictates that an oscillator whose frequency is determined by an external crystal or clock generator falls outside the scope of the claims. *See Phillips*, 415 F.3d at 1314 (explaining that "the context in which a term is used in the asserted claim can be highly instructive" to claim construction).

D. Defendants' construction is consistent with all prior constructions of this term.

The "entire oscillator" claim terms of the '336 patent have been construed in three prior litigations. The table below lists the constructions adopted in each of these prior litigations:

NDCA Construction (Judge Grewal)	EDTX Construction (Judge Ward)	ITC Construction (ALJ Gildea)
The term "entire oscillator" (in claims 6 and 13) is properly understood to ***exclude any external clock used to generate the signal used to clock the CPU***. Ex. J (Dkt. No. 646 jury instructions) at 26; Ex. K (Dkt. No. 616 Order re Emergency Motion) at 2.	"a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and ***does not directly rely on a command input control signal or an external crystal/clock generator to generate a signal***." Ex. L (Dkt. No. 259) at 11-12 (Construing "entire ring oscillator" term in claim 1).	"an oscillator that is located entirely on the same substrate as the central processing unit and ***does not rely on a control signal or an external crystal/clock generator to generate a clock signal***." Ex. M (Order No. 31) at 40-41; Ex. N (Commission Opinion) at 16-25 (affirming construction).

As shown above, every Court that has construed the "entire oscillator" term has concluded that applicants' prosecution history disclaimers require the construction to exclude reliance on an external clock to "generate" a clock signal.

In the Eastern District of Texas, Judge Ward construed the "entire ring oscillator" claim term in claim 1 to preclude reliance on either a control signal or an external crystal/clock generator to generate a clock signal. Ex. L (Dkt. No. 259) at 12. In reaching this conclusion, Judge Ward explained: "The Court agrees with the defendants that the applicant disclaimed the use of an input control signal and an external crystal/clock generator to generate a clock signal." *Id.*

Similarly, in the United States International Trade Commission investigation,

Administrative Law Judge Gildea construed "entire oscillator" as precluding reliance on either a control signal or an external crystal/clock generator to generate a clock signal. Ex. M (Order No. 31) at 40-41; Ex. N (Commission Opinion) at 16-25. In a detailed opinion thoroughly analyzing the intrinsic evidence, ALJ Gildea found that Plaintiffs clearly and unambiguously disclaimed any oscillator that, even when fabricated on the same substrate as the CPU, relies on a control signal or an external crystal or frequency generator. Ex. Q (Initial Determination) at 39-40 (finding that "the essential point made by the applicants in seeking to gain acceptance" of their claims, and their "unqualified statements in distinguishing" the prior art, constituted a "clear disavowal" of claim scope). The Commission affirmed Judge Gildea's construction in its entirety, reasoning that the prosecution history resulted in disclaimer, and concluded that the claim language and the specification also independently support the ALJ's construction. Ex. N at 16-25.

Likewise, in the prior *HTC v. TPL* case, this Court instructed the jury that the term "entire oscillator" excludes any external clock used to generate the CPU clock signal. Ex. J (Dkt. No. 646 jury instructions) at 26; Ex. K (Dkt. No. 616 Order re Emergency Motion) at 2; *see also* Ex. O (Dkt. No. 585 (Order on HTC summary judgment motion) at 11, and n.24.

Thus, Defendants' proposed construction is consistent with each of the prior constructions as it reflects applicants' prosecution history disclaimers. Defendants' proposed construction also provides clarification as to what it means "to generate" a signal – a phrase that is used in all three prior constructions. Such clarification is necessary and appropriate, both because it more specifically articulates the applicants' disclaimers, and because it avoids potential future argument or confusion over what "to generate" means.

For example, in the ITC investigation, notwithstanding the Administrative Law Judge's construction – which was premised upon the applicants' disclaimers – TPL continued to argue that the process of generating a clock signal did not include setting the frequency of the signal. *See, e.g.*, Ex. Q (Initial Determination) at 108-110. As a result, this issue required further litigation, which led to the ALJ ultimately concluding that "the process of setting the frequency of a clock signal and generating a clock signal are inseparable, because a clock signal must have a frequency, since its sole purpose is to provide a frequency for timing the operation of devices."

Id. at 121-122. The Commission agreed. Ex. N at 29-30 ("We find that the ALJ's application of his construction of the 'entire oscillator' limitation to the Accused Products was correct, including in particular his discussion of the intricate relationship between the generation and frequency of a clock signal.").

And, in the *HTC* case, the jury expressed uncertainty as to the meaning of the word "generate" in the jury instructions and sought clarification of this term during deliberations. Ex. P (Trial Tr.) at 1641:21-1644:14. Defendants' proposed construction should avoid any such potential confusion and aid the jury in this case because it clarifies that the term "generate" includes both causing clock signal oscillation and controlling signal frequency, consistent with applicants' prosecution disclaimers.

Accordingly, because Defendants' construction (1) is mandated by the repeated clear and unambiguous prosecution history disclaimers, (2) is consistent with the specification's teachings and its criticisms of the prior art, (3) finds confirmation in the plain language of the claims, and (4) is consistent with and further clarifies each of the claim constructions adopted in prior litigation for entire oscillator claim terms, Defendants' construction should be adopted.

E. Plaintiffs' construction is incorrect.

Plaintiffs' construction merely requires that the claimed oscillator be "located entirely on the same semiconductor substrate as the [central processing unit]." That cannot be correct because the intrinsic evidence leaves no doubt that the applicants surrendered far more during prosecution to secure allowance of the '336 patent. As discussed above, the applicants repeatedly distinguished their claimed oscillator from prior art clocks on the basis that their oscillator does not rely on a crystal, generator, or control signal to cause clock signal oscillation or control clock signal frequency. Plaintiffs cannot reclaim what they surrendered because that would eviscerate the patent's public notice function, which "requires that a patentee be held to what he declares during the prosecution of his patent." *See Springs Window Fashions LP v. Novo Indus., L.P.*, 323

F.3d 989, 995 (Fed. Cir. 2003).[8]

That Plaintiffs' construction would cover architectures well-known in the prior art long before the '336 patent is a further indication that it is incorrect. *See Amhil Enters. Ltd. v. Wawa, Inc.*, 81 F.3d 1554, 1562 (Fed. Cir. 1996)(construing claim term to avoid prior art of record). For example, the Talbot[9] prior art patent that is addressed in the file history discloses a phase-locked loop ("PLL") structure containing an on-chip "oscillator" or "clock." Ex. H (U.S. Patent No. 4,689,581 ("Talbot")) at 3:1-4 ("As is clear from Fig. 1, all of the components of the timing apparatus 4 are on the single silicon chip and the timing apparatus 4 has been designed such that it does not require any components external to chip 1."), Fig. 1; *see also* Ex. I (U.S. Patent No. 3,967,104 (issued in June 1976 and cited on the front cover the '336 patent)) at 1:8-12, 12:5-19 and Fig. 4a (disclosing oscillator system clock on same single chip as processor). Plaintiffs' construction should be rejected for all of the foregoing reasons.

V. CONCLUSION

For the foregoing reasons, Defendants respectfully request that the Court adopt their proposed claim construction.

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[8] Plaintiffs' attempt to undo their disclaimers also contradicts their prior litigation position. In the HTC litigation, Plaintiffs proposed that the "entire oscillator" term be given Judge Ward's construction, which requires "an oscillator that is located entirely on the same semiconductor substrate as the CPU ***and does not directly rely on a command input control signal or an external crystal/clock generator to generate a clock signal***." *See* C.A. 5:08-cv-00882-PSG, D.I. 228 at 17-19.

[9] While the issue of whether Talbot disclosed a ring oscillator was contested in the HTC litigation (*see* C.A. 5:08-cv-00877-PSG, D.I. 357 at 9-12), this issue is irrelevant here because claims 6 and 13 of the '336 patent are not limited to ring oscillators.

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ATTESTATION

I, Aaron Wainscoat, am the ECF User whose ID and password are being used to file this Defendants' Opening Claim Construction Brief. In compliance with Civi Local Rule 5-1(i)(3), I hereby attest that the signatories listed above have read and approved the filing of this brief.

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Exhibit "C"

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UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. HUAWEI TECHNOLOGIES CO., LTD., HUAWEI DEVICE CO., LTD., HUAWEI DEVICE USA INC., FUTUREWEI TECHNOLOGIES, INC., HUAWEI TECHNOLOGIES USA INC., Defendants.	Case No. 3:12-cv-03865-VC (PSG) **PLAINITIFFS' OPENING CLAIM CONSTRUCTION BRIEF**
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. GARMIN LTD., GARMIN INTERNATIONAL, INC., and GARMIN USA, INC., Defendants.	Case No. 3:12-cv-03870-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. ZTE CORPORATION and ZTE (USA) INC., Defendants.	Case No. 3:12-cv-03876-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. SAMSUNG ELECTRONICS CO., LTD. and SAMSUNG ELECTRONICS AMERICA, INC., Defendants.	Case No. 3:12-cv-03877-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. LG ELECTRONICS, INC. and LG ELECTRONICS U.S.A., INC., Defendants.	Case No. 3:12-cv-03880-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. NINTENDO CO., LTD. and NINTENDO OF AMERICA, INC., Defendants.	Case No. 3:12-cv-03881-VC (PSG)

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I. INTRODUCTION

The sole phrase for claim construction is one the Court knows well – "an entire oscillator disposed upon said integrated circuit substrate."[1] Defendants' construction represents yet another attempt build a non-infringement position through misconstruing the prosecution history regarding the *entire oscillator* phrase. These same efforts have been previously rejected by this Court and other tribunals. As set forth below, this Court should adopt Plaintiffs' construction of the *entire oscillator* phrase, which is in accordance with the Court's previous construction and provides Plaintiffs the correct scope of the claims bargained for at the patent office.

II. FACTUAL BACKGROUND

The issues presented in this briefing have a lengthy history, much of which has unfolded in this Court. For the better part of a decade, parties have been arguing in various forums whether the term *entire oscillator* allows for the use of an external crystal or clock generator as a reference signal. These specific issues have been presented to this Court no fewer than four times, and each time this Court has held that the intrinsic record permits the use of an external crystal or clock generator as a reference signal and has rejected defendants' attempts to include unwarranted negative limitations in the *entire oscillator* construction.

In June 2007, a related phrase, "an entire ring oscillator variable speed system clock in said integrated circuit," was construed by the United States District Court for the Eastern District of Texas. See Ex. A to Declaration of Barry J. Bumgardner,[2] *Technology Properties Ltd. et al. v. Matsushita Elec. Indus. Co., Ltd., et al.*, No. 2:05-cv-494, Dkt. No. 259 (E.D. Tex., June 15, 2007) (the "Texas Markman Order"). In the Texas proceeding, the court analyzed the intrinsic record presently cited by Defendants in this case and found that the term meant "a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not directly rely on a command input control signal or an external crystal/clock

[1] The *entire oscillator* term appears in claims 6 and 13 of U.S. Patent No. 5,809,336 and is the only term in dispute for the ''336 Patent. The parties recently dismissed each other's claims involving the two other patents previously at issue in these cases: U.S. Patent Nos. 5,440,749 and 5,530,890. *See, e.g., Technology Properties Ltd. v. Samsung Electronics Co., Ltd.*, No. 3:12-cv-03877, Dkt. 91.

[2] Hereinafter referred to as "Bumgardner Decl."

generator to *generate* a clock signal." *Id.* at 11-12 (emphasis added). The court in Texas specifically considered (i) whether the prosecution history prohibited the use of a crystal or external clock, or whether the external clock could be used as a reference, and (ii) whether the prosecution history prohibited the use of control signals such as voltage and current control signals, or the more narrow "command input control signals." *Id.* The Texas court found that an external crystal/clock generator could not be used for *generating* a clock signal, but left open the possible use of an external crystal/clock generator for a *reference signal*. The Texas Markman Order specifically rejected defendant Matsushita's proposed construction that the "ring oscillator" could not "rely on a control signal or an external crystal/clock generator." Instead, the court adopted a narrower limitation which excluded "direct" reliance on "command input control signals" from the scope of the claim term. Lastly, the Texas court construed the term "ring oscillator" to mean "an oscillator having a multiple, odd number of inversions arranged in a loop." *Id.* at 11.

In 2012, Judge Ware of this District considered the phrase "entire ring oscillator variable speed system clock." *See* Bumgardner Decl. Ex. B, *HTC Corp. v. Technology Properties Ltd., et al.*, No. 3:08-cv-882, Dkt. No. 364 at 13-16 (N.D. Cal., June 12, 2012)[3] (the "Ware Markman Order"). In this proceeding, HTC, like the prior defendants in Texas, took the position that the "ring oscillator" could not "rely on a control signal or an external crystal/clock generator to generate a clock signal" and that the speed of the "oscillator" was "non-controllable." *See, e.g., Id.* and Bumgardner Decl. Ex. C, *HTC,* Dkt. No. 339 at 25 (TPL's Opening Claim Construction Brief).

Judge Ware evaluated the parties' respective positions and discussed the plain and ordinary meaning of a *ring oscillator*. Ware Markman Order at 13. Other than to state that "a person of ordinary skill in the art reading the patent would understand that Claim 1 claims a 'single integrate circuit,' fabricated so as to include a 'ring oscillator'", Judge Ware declined to further construe the *entire ring oscillator variable speed clock* without receiving additional briefing regarding statements made during prosecution. Ware Markman Order at 16. In other

[3] Subsequent citations to *HTC Corp. v. Technology Properties Ltd., et al.* will be made as "HTC Case."

words, the exacting standard for showing disavowal had not been met and the Court asked to hear more. Judge Ware ordered the supplemental briefing, subsequently retired, and the *HTC* matter was transferred to Judge Grewal.

In the supplemental briefing, the parties continued to debate the meaning of the *ring oscillator*. The supplemental briefing generally covered the disputed elements of *ring oscillator* rather than the meaning of the word *entire*. After evaluating the parties' positions and the prosecution history, Judge Grewal held that while the frequency of the *ring oscillator* is determined by the temperature, voltage, and process, the prosecution history of the patent did not "impose a prohibition on all types of control." Bumgardner Decl. Ex. D, *HTC*, Dkt. No. 509 (August 21, 2013 - Claim Construction Order) (the "Grewal Markman Order"). Thus, Judge Grewal declined to include "non-controllable" in the construction or to prohibit reliance on an external crystal oscillator in the construction of the term.

Meanwhile, at the ITC, an administrative law judge considered the meaning of *ring oscillator* and *entire oscillator* in a proceeding involving all of the Defendants to the present case. In the ITC, the Defendants advocated that the term *ring oscillator* could "not *rely* on a control signal or an external crystal/clock generator to *generate* a clock signal." See Bumgardner Decl. Ex. E, Commission Investigative Staff's Initial Markman Brief, Investigation No. 337-TA-853 at 7 (February 8, 2013). As in the Grewal Markman Order, the ITC ultimately held that the *ring oscillator* need not be "non-controllable" because there was no clear and unmistakable disavowal in the prosecution history. See Bumgardner Decl. Ex. F, Investigation No. 337-TA-853, Order No. 31, Construing the Terms of the Asserted Claims of the Patent at Issue at 18 (Apr. 18, 2013) (the "ITC Markman Order"). The ITC Markman Order further declined to add the temperature, voltage and process limitation because such limitations were already found in the claims. *Id.* The ITC did continue address the meaning of *entire* by construing the term *an entire ring oscillator variable speed system clock in said single integrated circuit*. Here, the ALJ disagreed with Judge Ward's construction. The ITC held that the term meant "a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the central processing unit and does not rely on a control signal or an external crystal/clock generator to

generate a clock signal." ITC Markman Order at 40 (emphasis added). This construction differed from Judge Ward's prior construction in that it modified the previous prohibition against relying on a "command input control signal" to be a prohibition against relying on a "control signal." The construction also removed the word *directly* before *rely*.

After the ITC ruling, HTC moved for summary judgement in its district court case. *See* Bumgardner Decl. Ex. G, *HTC*, Dkt. No. 457 (Plaintiffs' Motion for Summary Judgment of Non-Infringement). HTC argued that the *entire* portion of the *entire oscillator* term meant that there could be no involvement whatsoever of an external crystal in the function of the oscillator. The Court denied HTC's motion. Bumgardner Decl. Ex. H, *HTC*, Dkt. No. 585 at 11 (Summary Judgment Order). While the Court did agree that, as a result of prosecution history, the claims exclude "any external clock used to *generate* a signal" the Court recognized that there was some factual dispute as to whether the clock is generated on the chip and relies on the PLL (and, thus, the external crystal) to merely "buffer or fix" the frequency. *Id*. The Court called this a "classic factual question that requires a trial to answer." *Id.*

After the Court entered the HTC Summary Judgment Order, HTC moved on an emergency basis to attempt to again capture additional claim limitations in the jury instructions. Bumgardner Decl. Ex. I, *HTC*, Dkt. No. 590 (HTC Emergency Motion). TPL and Patriot opposed. Bumgardner Decl. Ex. J, *HTC*, Dkt. No. 596, (TPL Response to Emergency Motion). Specifically, HTC asked the Court to modify the jury instructions to indicate that (1) the *entire oscillator* term (and its kin) "are not satisfied by an accused system that uses any external clock to generate a signal" and (2) "an accused product can only infringe the '336 Patent if that product contains an on-chip oscillator or clock that is (a) self-generating and (b) does not rely on an input control to determine its frequency." Ex. I at 2. The Court held that the jury would be instructed that the term *entire oscillator* and its kin are properly understood to "exclude any external clock used to *generate* a signal," but once again declined to add a restriction with respect to control of the oscillator. Bumgardner Decl. Ex. K, *HTC*, Dkt. No. 607, (Emergency Motion Order) (emphasis added).

After trial, the Court considered a JMOL by HTC which once again touched on the issue of the *entire oscillator*. In its order denying HTC's JMOL, the Court explained that in considering HTC's emergency motion regarding jury instructions, the Court specifically considered HTC's request for additional claim construction and explained that the Emergency Motion Order modified the "external clock to generate a signal" language, while denying the self-generating/input control language. Bumgardner Decl. Ex. L, *HTC*, Dkt. No. 707 at 8-9 (Order Denying JMOL). The Court's JMOL Order demonstrated the Court's acute understanding of how the PLLs involved in the accused HTC products are used to regulate, not generate the *ring oscillator's* frequency. *Id.* at 11.

The *entire oscillator* issue is once again before this Court, as Defendants in this suit make yet another attempt to include some of the same negative limitations in the *entire oscillator* construction that have been previously rejected.

III. APPLICABLE LAW

This Court is well-versed in the general principles applicable to claim construction. *Sealant Systems Intern., Inc. v. TEK Global S.R.L.*, 2012 WL 3763794 at *1, (N.D. Cal. 2012) ("Seven years after the Federal Circuit's seminal *Phillips* decision, the cannons of claim construction are now well-known even if not perfectly understood by parties and courts alike.") However, the below discussion regarding disclaimer may be useful.

As Judge Ware observed in the Ware Markman Order, before a submission made by a patentee during reexamination can be regarded as a disavowal, the court must find "the allegedly disavowing statement is 'so clear as to show reasonable clarity and deliberateness, and so unmistakable as to show unambiguous evidence of disclaimer.'" Ware Markman Order at 16, quoting *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1325 (Fed. Cir. 2003) (citations omitted). Stated another way, the "disavowal" doctrine only applies where a disavowal is "clear and unmistakable." *See Cordis Corp. v. Medtronic AVE, Inc.*, 511 F.3d 1157, 1177 (Fed Cir. 2008) ("alleged disavowing actions or statements made during prosecution [must] be both clear and unmistakable"). *See also Hill-Rom Servs. v. Stryker Corp.*, 755 F.3d 1367, 1373 (Fed. Cir. 2014) ("Disavowal requires that "the specification [or prosecution history] make[] clear that the

invention does not include a particular feature,") (brackets in original); *Thorner v. Sony*, 669 F.3d 1362, 1367 (Fed. Cir. 2012) (stating that "the standard for disavowal of claim scope is [] exacting").

Additionally, the alleged disavowal must be made by the patentee, not the examiner. *Salazar v. Procter & Gamble Co.*, 414 F.3d 1342, 1347 (Fed. Cir. 2005) ("unilateral statements by an examiner do not give rise to a clear disavowal of claim scope by an applicant," as "the applicant has disavowed nothing"); *Univ. of Pittsburgh of Commonwealth Sys. of Higher Educ. v. Hedrick*, 573 F.3d 1290, 1296-97 (Fed. Cir. 2009) ("a wide chasm exists between the weak inference from the [interview] summary . . . and a clear and unmistakable disavowal as required to limit a claim term"). As the Federal Circuit has recognized, "[p]rosecution history ... cannot be used to limit the scope of a claim unless the *applicant* took a position before the PTO." *3M Innovative Props. Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1373 (Fed. Cir. 2003) (emphasis added). The reason for requiring the disclaimer to come from the *applicant* rather than the *examiner* is the recognition that sometimes the examiner and applicant are talking past one another. *See Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc*., 381 F.3d 1111, 1124 (Fed. Cir. 2004) (where an "examiner and applicant [are] talking past one another" and "the record finally reflects the examiner's acquiescence to the claim language chosen by the applicant, [t]his is not clear evidence of the patentee's disavowal of claim scope").

IV. ARGUMENT

The parties agree to the meaning of the term *oscillator*. Bumgardner Decl. Ex. M, Joint Claim Construction and Prehearing Statement, Ex. A - Agreed Terms, *Technology Properties Ltd., et al. v. Samsung Electronics Co., Ltd. et al.*, No. 3:12-cv-0877, Dkt. No. 72-1 at 5. The parties also agree to the meaning of *ring oscillator*, and other descriptions of the *oscillator*, such as the *oscillator . . . clocking*. *Id.* The sole dispute is whether the *entire oscillator* term should include narrowing limitations that this Court has previously rejected. The disputed language proposed by Defendants is italicized below:

Term	Plaintiffs' Construction	Defendants' Construction
an entire oscillator disposed upon said integrated circuit substrate	An [oscillator] that is located entirely on the same semiconductor substrate as the [central processing unit].	An [oscillator] that is located entirely on the same semiconductor substrate as the [central processing unit] *and does not rely on a control signal or an external crystal/clock generator to cause clock signal oscillation or control clock signal frequency.*

A. Plaintiffs' construction gives meaning to the claim language and is consistent with the Court's prior claim constructions.

Plaintiffs' construction utilizes the parties' agreed constructions of *oscillator* and *CPU*, and is the same as Defendants' construction except for the negative limitations Defendants seek to improperly include (discussed below). As an initial matter, the parties agree that an *oscillator* is a "circuit capable of maintaining an alternating output." The claim language at issue merely requires that the *entire oscillator* be "disposed upon said integrated circuit substrate." Plaintiffs' construction gives meaning to the claim language by requiring that the *oscillator* be "located entirely on the same semiconductor substrate as the [CPU]." Defendants do not dispute this part of Plaintiffs' construction.

As to the function of the *entire oscillator*, the claim requires that "said oscillator clocking said [CPU] at a clock rate . . . ." The parties are in agreement that (1) "clocking said [CPU]" means "providing a timing signal to said [CPU]; and (2) "oscillator … clocking" means "oscillator that generates the signal(s) used for timing the operation of the [CPU]." Thus, there is no dispute as to the function of the *entire oscillator* and its role in the claimed invention.

Plaintiffs' construction is also consistent with the Court's prior treatment of the phrase in the HTC case. Notably, the Court in the HTC case issued a jury instruction that the *entire oscillator* "exclude[s] any external clock used to generate the signal used to clock the CPU." *See* Bumgardner Decl. Ex. N, *HTC*, Dkt. No. 646 at 26 (Jury Instructions). Plaintiffs' construction is entirely consistent with this instruction because (i) Plaintiffs' construction of the *entire oscillator* already requires the oscillator to be "located entirely on the same semiconductor substrate as the [CPU]" and (ii) other, undisputed claim language already requires "said oscillator clocking said

[CPU] at a clock rate." *See* '336 Patent, Claim 6. Thus, Plaintiff's construction, when read in conjunction with the claim as a whole, already makes clear that an external clock may not generate the signal used to clock the CPU.

B. Defendants' construction improperly adds negative limitations and is inconsistent with the Court's prior constructions.

Defendants' construction improperly adds the negative limitations that the oscillator "*not rely on a control signal or an external crystal/clock generator to cause clock signal oscillation or control clock signal frequency.*" Adoption of this negative limitation would be a major departure from the Court's prior treatment of the *entire oscillator* phrase and must be rejected for several reasons.

A comparison of Defendants' proposed construction to that proffered previously by HTC is illustrative of Defendants attempt to read an even broader (in certain aspects) disclaimer in to the *entire oscillator* term.

Term	HTC's Proposed Construction[4]	Defendants' Construction
an entire oscillator disposed upon said integrated circuit substrate	A ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not *rely* on a control signal or an external crystal/clock generator to *generate* a clock signal, wherein the ring oscillator variable speed system clock is: (1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters in the environment	An [oscillator] that is located entirely on the same semiconductor substrate as the [central processing unit] and does not *rely* on a control signal or an external crystal/clock generator to *cause* clock signal oscillation or control clock signal frequency.

Both HTC and Defendants include the phrase "does not rely on a control signal or an external crystal/clock generator" in their constructions. HTC's construction goes on to limit the reliance on the actual generation of the clock signal ("to generate a clock signal"). Defendants,

[4] HTC's proposed construction corresponds to "providing an entire variable speed clock disposed upon said integrated circuit substrate" but the nature and importance of the arguments is the same.

on the other hand, broaden this concept using the term "cause" ("to cause clock signal oscillation"). Plaintiffs' respectfully submit that the concept of "causation" is significantly broader than the concept of "generation" as put forward by HTC. A common legal test for causation is the "but for" test. The test simply asks, "but for the existence of X, would Y have occurred?" If the answer is yes, then factor X is an actual cause of result Y. Under this type of analysis, any one of a number of control signals unrelated to the generation of a clock signal could possibly be found to "cause clock signal oscillation." For example, a general reset signal that is asserted on power-on and that holds many systems in a non-active state for some period of time could be a "control signal . . . that cause[s] clock signal oscillation" under Defendants' construction. Likewise, a signal that causes power to be applied to the clocking systems could be found to "cause clock signal oscillation or control clock signal frequency." Such concepts are far removed from the intrinsic record of the '336 Patent and are but one reason why Defendants' construction should be rejected.

Turning now to other aspects of Defendants' proposed construction, with respect to the external crystal/clock generator, the Defendants now propose that the *entire oscillator* cannot "*rely*" on those elements to "*cause* clock signal oscillation or control clock signal frequency." This is an unabashed attempt to exclude scenarios where an external crystal is used as a reference signal. Nothing in the prosecution history supports such a restriction. Presumably the Defendants will cite to the prosecution history surrounding Magar (U.S. Patent No. 4,503,500), arguing that the patentees disclaimed all use of an external crystal. But that characterization is incorrect. Magar relied upon an external crystal to *generate* the actual clock signal used by the CPU. As the Court is aware, such an argument is distinct from using an external crystal or clock generator as a *reference* to adjust the frequency of an already existing clock signal. *See, e.g.*, Ex. L at 10-11.

With respect to external control, Defendants now attempt to claim that the entire oscillator cannot rely on a control signal to *cause* clock signal oscillation or control clock signal frequency. The only potential support for such a limitation, however, is another strained and incorrect reading of the prosecution history. In years of prosecution and re-examination, the patentees did

not state that the *oscillator* could not be subject to any form of control. Instead, for example, in distinguishing the '336 Patent invention from U.S. Patent No. 4,670,837 ("Sheets"), the patentees pointed out that by placing the clock and the CPU on the same integrated circuit, the '336 patent:

> ***obviates the need*** for provision of the type of frequency control information described by Sheets.

Bumgardner Decl., Ex. O, '336 Patent, File History, Response to Office Action at 8 (April 15, 1996) (emphasis added). The '336 Patent prosecution history demonstrates that the patentees distinguished their invention from the prior art by pointing out that, unlike the prior art, the oscillator or variable speed clock in their invention varies in frequency (*i.e.*, is not fixed, for example, like an external crystal) and *does not require* external frequency control. Defendants' unsupported effort to expand this distinction beyond its clear meaning to impose a *prohibition* of any form of control should be rejected as unsupported and without merit. See Ex. D, HTC Markman Order at 10 (analyzing similar language in the file history).

Furthermore, with respect to Talbot (U.S. Patent No. 4,689,581), the statements in the prosecution history do not amount to disavowal because they are not clear and unmistakable limitations of the claim scope. A review of the prosecution history reveals that the only reference to "non-controllability" is inclusion of the single word "non-controllable" in a summary of an interview *prepared by the examiner*. Bumgardner Decl., Ex. P, U.S. Patent No. 6,598,148 Patent, Reexamination File History, Interview Summary at 4 (February 12, 2008).[5] In the short, three-sentence summary of the discussion of Talbot, the examiner provided no explanation regarding the meaning of the word. Moreover, rather than relying on "non-controllability," the examiner specifically stated he would "reconsider the current rejection [premised on Talbot] based on a forthcoming response" from the patent owner. Within 8 days of the interview (dated February 21, 2008, though filed February 26, 2008) TPL submitted the promised written response. Bumgardner Decl., Ex. Q, '148 Patent, Reexamination File History, Remarks/Arguments, (February 21, 2008). This written response explained that Talbot was distinguishable because "Talbot does not teach, disclose, or suggest the ring oscillator recited in claim 4." *Id.* at 11.

[5] U.S. Patent No. 6,598,148 (the "'148 Patent") shares a common specification with the '336 Patent and contains similar claim limitations.

Nowhere – and in no way – did TPL adopt the examiner's reference to "non-controllability." TPL, in fact, made no reference to that word at all.

Importantly, TPL acknowledged that "Talbot discusses a voltage-controlled oscillator (VCO)." *Id*. After that acknowledgment, TPL did not point to that feature as distinguishing Talbot from the claimed invention. Instead, TPL wrote: "but, [Talbot] does not teach or disclose a ring oscillator." *Id*. TPL, in other words, did not exclude or disclaim voltage controlled oscillators, as Defendants appear to assert; TPL, instead, pointed out that voltage controlled oscillators *which do not employ a ring oscillator*, such as in Talbot, do not satisfy the claimed "ring oscillator" limitation of the invention.

Of further importance, in an action dated June 25, 2008, the examiner expressly accepted the arguments contained in the written response, never mentioning the interview. Specifically, the examiner stated "Patent Owner's arguments, filed 2/26/08 with respect to the rejections [based on Talbot] have been fully considered and are persuasive. Therefore, the rejection … has been withdrawn." Bumgardner Decl., Ex. R, '148 Patent, Reexamination History, Detailed Action at 5. Thus, the examiner expressly relied on the patent owner's written arguments to overcome Talbot, and *not* the interview.

The law regarding disavowal is settled: Allegedly disavowing statements must be both "so clear as to show reasonable clarity and deliberateness, and so unmistakable as to show unambiguous evidence of disclaimer" for the Court to use the statement to limit the meaning of claim terms. *Omega Eng'g, Inc.*, 334 F.3d at 1325. Here, the alleged disavowing statement – "non-controllable" – remains unexplained in the file history and not adopted by the patentee. The term itself is ambiguous, and would require further construction. For example, the '336 Patent discloses that the ring oscillator frequency will vary with changes in voltage. '336 Patent, 17:21-22. This disclosure indicates, therefore, that the voltage provided to the ring oscillator is not fixed and can be changed or even controlled, rendering the meaning of "non-controllable" ambiguous. Where the meaning of purported disavowal is not apparent, there can be no "clear and unambiguous" disclaimer. On this basis alone, Defendants' proposed limitation should be rejected.

The portions of the prosecution history analyzed above are merely some examples of how past litigants have attempted to use the prosecution history of the'336 Patent to recast the plain meaning of the *entire oscillator* element and to include disclaimers that do not exist. Which portions of the record the current Defendants will rely upon will be clear from their claim construction brief (which is being filed concurrently with this document). Accordingly, Plaintiffs will conduct a thorough analysis of the specific arguments made by Defendants in their Response.

V. CONCLUSION

The *entire oscillator* term was properly construed by this Court in the HTC case. Plaintiffs recognize that Defendants were not parties to that case and have the right to make their own arguments as to the meaning of *entire oscillator*. But, given that HTC presented a construction similar to the one being proffered by Defendants and that the portions of the intrinsic record noted by Defendants as being relevant to the construction of this term largely overlap with those relied upon by HTC, Plaintiffs suspect that Defendants' arguments relating to the meaning of *entire oscillator*, and the supporting evidence, will be substantively the same. If this is the case, Plaintiffs believe that this Court prior analysis was the proper one as well as the resulting construction. Regardless of Defendants' specific arguments, however, prior litigants have been trying to read in negative limitations to the *entire oscillator* term for years and have been justifiably unsuccessful. Plaintiffs respectfully submit that this lack of success is due to the simple fact that the intrinsic record does not support such negative limitations. Accordingly, this Court should continue to reject such attempts.

Dated: August 4, 2015

Respectfully submitted,

/s/ Barry J. Bumgardner

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CERTIFICATE OF SERVICE

I hereby certify that, on August 4, 2015, I caused the foregoing document to be served on counsel of record via the Court's CM/ECF system.

Dated: August 4, 2015

By: */s/ Barry J. Bumgardner*
Barry J. Bumgardner

Exhibit “D”

(*Counsel listed on signature page*)

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. HUAWEI TECHNOLOGIES CO., LTD., et al., Defendants.	Case No. 3:12-cv-03865-VC (PSG) **DEFENDANTS' RESPONSIVE CLAIM CONSTRUCTION BRIEF** DATE: September 18, 2015 TIME: 10:00 AM PLACE: Courtroom 5, 4th Floor JUDGE: Hon. Paul S. Grewal

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. GARMIN LTD., et al., Defendants.	Case No. 3:12-cv-03870-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al. Plaintiffs v. ZTE CORPORATION, et al., Defendants.	Case No. 3:12-cv-03876-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. SAMSUNG ELECTRONICS CO., LTD., et al., Defendants.	Case No. 3:12-cv-03877-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. LG ELECTRONICS, INC., et al., Defendants.	Case No. 3:12-cv-03880-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. NINTENDO CO., LTD, et al. Defendants.	Case No. 3:12-cv-03881-VC (PSG)

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I. INTRODUCTION

The parties' opening briefs squarely frame the issues to be decided by the Court: (1) do applicants' prosecution history disclaimers limit the "entire oscillator" claim term; and (2) if so, what are those limits? The Court must decide these issues because the Federal Circuit requires that all disclaimers be fully embodied in the construction of this claim term. *See* Defendants' Opening Claim Construction Brief ("Def. Op. Br.") at 5-6. Plaintiffs do not dispute this.

The response to the first question is clear: the intrinsic evidence conclusively establishes that applicants' prosecution history disclaimers limit the scope of the "entire oscillator" claim term, and every court that has addressed this issue has so found. *Id*. at 7-13, 16-18. Nevertheless, Plaintiffs' proposed construction and their opening brief ignores *all* of Defendants' disclaiming arguments, even though Plaintiffs have seen Defendants successfully make these same arguments in the International Trade Commission. Plaintiffs' head-in-the-sand approach of studiously ignoring the file history forces Defendants to wait until the *Markman* hearing to respond to whatever Plaintiffs will say about the file history in their responsive brief.

The answer to the second question also is clear: during prosecution, applicants argued clearly, repeatedly, and unmistakably that their "entire oscillator," unlike the prior art, does not rely on an external crystal, clock generator, or control signal to cause clock signal oscillation or control clock signal frequency. Defendants' construction accurately captures applicants' disclaimers. Plaintiffs, however, ignore the disclaiming statements applicants made about the prior art references and instead resort to characterizing the references themselves. But Federal Circuit law is clear that the scope of the disclaimer is measured by what applicants said during prosecution, not by what the prior art says and not by what is necessary to distinguish the claims from the prior art.

As established in Defendants' opening brief, and as further confirmed below, Defendants' construction is consistent with all prior constructions of "entire oscillator," and Defendants' construction clarifies in plain English what it means "to generate" a signal. This is necessary to avoid the misapplication of this claim term and jury confusion that resulted in prior cases.

II. REPEATED AND UNAMBIGUOUS PROSECUTION HISTORY DISCLAIMERS MANDATE DEFENDANTS' CONSTRUCTION

As discussed above, and as established in detail in Defendants' opening brief, applicants repeatedly and unambiguously distinguished their purported invention from the prior art on several distinct grounds during prosecution of the '336 patent. Def. Op. Br. at 7-13. Specifically, applicants distinguished their on-chip oscillator from the prior art Magar reference on the grounds that their purported invention did not rely on an external crystal oscillator or clock generator to either (1) control the frequency of the clock or (2) cause clock signal oscillation. *Id*. at 7-11. Applicants further distinguished their on-chip oscillator from the Sheets prior art reference on the grounds that their purported invention did not rely on a control signal to cause clock signal oscillation or control the frequency of the clock signal. *Id*. at 11-13. The repeated arguments made by applicants during prosecution to distinguish the claims from the Magar and Sheets prior art constitute clear disclaimers that Federal Circuit law mandates must be reflected in the proper construction of this term. *Id*. at 5-6.

Plaintiffs' opening brief ignores applicants' prosecution history disclaimers, preventing Defendants from meaningfully responding until the *Markman* hearing. Meanwhile, Defendants establish below that the arguments in Plaintiffs' opening brief fail for the following reasons: (1) Plaintiffs ignore applicants' disclaimers over the prior art Magar reference; (2) Plaintiffs erroneously focus on the disclosure in Magar itself, as opposed to focusing (as must be the case) on the *distinguishing arguments* applicants actually made to avoid Magar; (3) Plaintiffs' arguments about the word "cause" in Defendants' construction lack merit; (4) Plaintiffs ignore applicants' disclaimers over the prior art Sheets reference; and (5) Plaintiffs rely on irrelevant portions of the prosecution history.

A. Plaintiffs Ignore Applicants' Disclaimers Over Magar

It is true, as Plaintiffs contend, that Defendants' construction "exclude[s] scenarios where an external crystal is used as a reference signal." Pl. Op. Br. at 9. However, Plaintiffs' narrow focus on reference signals is misplaced. As discussed below, applicants' clear and unambiguous disclaimers exclude use of an external crystal ***to control the frequency of the clock signal***. This

disclaimer applies equally to exclude use of a reference signal from an external crystal to control the frequency of the clock signal.

For convenience, reproduced below are *all six* of the arguments applicants made during prosecution to distinguish Magar on the ground that it uses a crystal to control the frequency of the clock signal that clocks the CPU:[1]

> A review of the Magar reference shows that it is apparently no more pertinent than prior art acknowledged in the application, in that ***the clock disclosed in the Magar reference is in fact driven by a fixed frequency crystal, which is external to the Magar integrated circuit***.[2]

Ex. D[3] (July 7, 1997 Amend.) at 2 (TPL85300002426).

> Contrary to the Examiner's assertion . . . one of ordinary skill in the art should readily recognize that the speed of the CPU and clock ***do not*** vary together due to manufacturing variation, operating voltage, and temperature of the IC in the Magar processor . . . ***This is simply because the Magar microprocessor clock is frequency controlled by a crystal which is also external to the microprocessor. Crystals are by design fixed frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The Magar microprocessor in no way contemplates a variable speed clock as claimed.***

Id. at 3-4 (TPL85300002427-28) (first emphasis in original).

> [C]rystal oscillators have never, to Applicants' knowledge, been fabricated on a single silicon substrate with a CPU, for instance. ***Even if they were***, as previously mentioned, ***crystals are by design fixed-frequency devices whose oscillation frequency is designed to be tightly controlled*** and to vary minimally due to variations in manufacturing, operating voltage and temperature. ***The oscillation frequency of a crystal on the same substrate with the microprocessor would inherently not vary due to variations in manufacturing, operating voltage and temperature in the same way as***

[1] At least a subset of these citations are prominently discussed in no fewer than 7 different publicly available papers filed in the ITC investigation: the Staff's opening *Markman* brief (23-25); the Staff's reply the *Markman* brief (12-14); the transcript of the ITC's *Markman* hearing (93-95, 108, 127, 128, 132, 142-85); ALJ Gildea's claim construction order (15-20); ALJ Gildea's Initial Determination (122-124); Respondents' Opposition to Complainants' Petition for Review (36-47); and the Commission's Opinion (14-25).

[2] Unless otherwise indicated, all emphasis in this brief is added by Defendants.

[3] Unless otherwise indicated, all exhibits cited in this brief are attached to the Declaration of Aaron Wainscoat in Support of Defendants' Opening Claim Construction Brief (Exs. A-Q) (Dkt. No. 94-1) and the Supplemental Declaration of Aaron Wainscoat in Support of Defendants' Responsive Claim Construction Briefs submitted herewith (Exs. R-U).

> ***the frequency capability of the microprocessor on the same underlying substrate, as claimed.***

Id. at 4 (TPL85300002428).

> The signals PHASE 0, PHASE 1, PHASE 2 and PHASE 3 in Applicants' Fig. 18 are synonymous with Q1, Q2, Q3 and Q4 depicted in Magar Fig. 2a. The ***essential difference*** is that the ***frequency or rate*** *of the PHASE 0, PHASE 1, PHASE 2 and PHASE 3 signals* ***is determined by the processing and/or operating parameters of the integrated circuit*** containing the Fig. 18 circuit, ***while the frequency or rate*** *of the Q1, Q2, Q3 and Q4 signals depicted in Magar Fig. 2a* ***are determined by the fixed frequency of the external crystal*** connected to the circuit portion outputting the Q1, Q2, Q3 and Q4 signals shown in Magar Fig. 2a.

Ex. E (Feb. 10, 1998 Amend.) at 4 (TPL853_02954560).

> Magar's clock generator *relies on an external crystal* connected to terminals X1 and X2 *to oscillate*, as is conventional in microprocessor designs. It is not an entire oscillator in itself. And with the crystal, ***the clock rate generated is also conventional in that it is a fixed, not a variable, frequency***. The Magar clock is comparable in operation to the conventional crystal clock 434 depicted in Fig. 17 of the present application for ***controlling*** the I/O interface ***at a fixed rate frequency, and not at all like the clock on which the claims are based***, as has been previously stated.

Id. at 3 (TPL853_02954559).

> The Magar teaching . . . is specifically distinguished from the instant case in that it is both ***fixed frequency*** (*being crystal based*) and *requires an external crystal or external frequency generator*.

Id. at 5 (TPL853_02954561).

Each of these ***six*** file history arguments distinguishes Magar from the claimed invention either by stating that the frequency of the Magar clock signal is crystal-controlled, or by stating that the Magar clock signal is "determined," "fixed," or "set" by the crystal – all of which mean precisely the same thing. Applicants left no doubt about what they viewed as the feature that distinguished Magar from the "entire oscillator" of their claimed invention: Magar used a clock signal whose frequency is controlled by an external crystal, whereas applicants' "entire oscillator" does not.

These repeated and unambiguous arguments expressly disclaim oscillators whose frequency is controlled, set, determined or fixed by an external crystal. *See North Am. Container*

Inc. v. Plastipak Packaging Inc., 415 F.3d 1335, 1345-46 (Fed. Cir. 2005) (holding that disclaimer of any concavity was the "inescapable consequence" of applicant's argument that the prior-art inner walls are "slightly concave").[4] The six file history excerpts quoted above certainly meet the Federal Circuit standard cited by Plaintiffs in their opening brief, namely that the disavowing statement be "so clear as to show reasonable clarity and deliberateness, and so unmistakable as to show unambiguous evidence of disclaimer." Pl. Op. Br. at 5 (quoting *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1325 (Fed. Cir. 2003) (citations omitted).

B. Plaintiffs Incorrectly Focus On The Magar Disclosure Itself, Rather Than On Applicants' Actual Disclaimers

Plaintiffs' opening brief ignores all six of applicants' disclaimers quoted above. Rather than confront what applicants actually told the Patent Office to distinguish Magar, Plaintiffs focus on Magar itself, arguing:

> Presumably the Defendants will cite to the prosecution history surrounding Magar (U.S. Patent No. 4,503,500), arguing that the patentees disclaimed all use of an external crystal. But that characterization is incorrect. Magar relied upon an external crystal *to generate* the actual clock signal used by the CPU. As the Court is aware, such an argument is distinct from using an external crystal or clock signal generator as a *reference* to adjust the frequency of an already existing clock signal.

Pl. Op. Br. at 9 (emphasis in original). This distinction is incorrect for several reasons.

First, this is legal error. The focus must be on the arguments applicants made to distinguish Magar, as those are what define the disclaimer. Instead, Plaintiffs focus on Magar itself – which runs counter to Federal Circuit disclaimer law. As the Federal Circuit made clear in *North Am. Container,* for example, the scope of the disclaimers must be measured by ***what the applicants said during prosecution***, not by what was necessary to distinguish the claims from the prior art. 415 F.3d at 1340-41.

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[4] *See also, Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) ("where the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender."); *Microsoft Corp. v. Multi-Tech. Sys., Inc.*, 357 F.3d 1340, 1349 (Fed. Cir. 2004) (a court "cannot construe the claims to cover subject matter broader than that which the patentee itself regarded as comprising its invention and represented to the PTO").

In *North Am. Container*, the applicant made the following arguments during prosecution to overcome two prior art patents, Jakobsen and Dechenne:

> The shape of the base as now defined in the claims differs from those of both the Dechenne patent, wherein the corresponding wall portions 3 are *slightly concave . . .* and the Jakobsen patent, wherein the entire re-entrant portion is clearly *concave in its entirety*. This is also generally true of all of the prior art known to the applicant and/or referred to by the examiner.

Id. at 1340. Nevertheless, after the patent issued, the patentees argued that there was no disclaimer over walls with some concavity, but rather only a disclaimer over walls that were entirely concave. *Id*. at 1344. The Federal Circuit rejected that argument for the following reasons:

> We are not persuaded by NAC's argument that the applicant intended only to distinguish his invention from the prior art on the basis that the inner walls in the prior art bottles are entirely concave. ***Although the inner walls disclosed in the Dechenne and Jakobsen patents may be viewed as entirely concave, that is not what the applicant argued during prosecution to gain allowance for his claims.*** The applicant stressed the difference in the extent of the concavity between the Dechenne and Jakobsen patents, noting that Dechenne is "slightly concave," whereas Jakobsen is "clearly concave in its entirety." Such a distinction would have been unnecessary if the only point that the applicant intended to make was that both prior art patents disclosed inner walls that are entirely concave.

Id. at 1345-46. The court made clear that the scope of the disclaimer is measured by the words used by the patentee and can be broader than what is necessary to overcome the prior art. This holding is in accord with well-established Federal Circuit precedent. *See, e.g.*, *Norian Corp. v. Stryker Corp.*, 432 F.3d 1356, 1361 (Fed. Cir. 2005) ("[T]here is no principle of patent law that the scope of surrender of subject matter made during prosecution is limited to what is absolutely necessary to avoid a prior art reference that was the basis for an examiner's rejection"); *Atofina v. Great Lakes Corp.*, 441 F.3d 991, 998 (Fed. Cir. 2006) ("[t]hat the applicants only needed to surrender nickel-chromium catalysts to avoid a prior art reference does not mean that its disclaimer was limited to that subject matter"); *Marctec LLC v. Johnson & Johnson*, 394 Fed. App'x 685, 687 (Fed. Cir. 2010) ("[l]imitations clearly adopted by the applicant during prosecution are not subject to negation during litigation, on the argument that the limitations were not really needed in order to overcome the reference"); *Saffran v. Johnson & Johnson*, 712 F.3d

549, 559 (Fed. Cir. 2013) (holding that arguments made to distinguish prior art "preformed chamber" constitute a disclaimer of not only the prior art "preformed chamber" but also a broader disclaimer of anything other than a "sheet.").

Here, as in *North Am. Container*, applicants disclaimed what they *actually argued* to overcome Magar, not just what was necessary to overcome Magar. By repeatedly arguing that, unlike their claims, Magar's clock signal frequency was controlled by an external crystal, they disclaimed the use of an external crystal to control clock signal frequency – regardless of whether that scope was necessary to avoid Magar. Indeed, applicants pointed to their argued distinction as being the "essential difference" between Magar and their claimed invention:

> The ***essential difference*** is that the frequency or rate of the [clock] signals [of the claimed invention] is determined by the processing and/or operating parameters of the integrated circuit containing [applicants] Fig 18 circuit, while the frequency or rate of the [clock] signals depicted in Magar Fig. 2a are determined by the fixed frequency of the external crystal connected to the circuit portion outputting the [clock] signals shown in Magar Fig. 2a.

Ex. E (Feb. 10, 1998 Amend.) at 4 (TPL853_02954560). Applicants did not distinguish Magar on the basis of whether the components necessary for Magar's oscillator to oscillate were on-chip or off-chip. Rather, they argued that Magar's clock frequency is controlled by the external signal while the frequency of the claimed "entire oscillator" is not.[5]

Second, while Plaintiffs acknowledge that "Magar relied on an external crystal to *generate*

[5] Notably, during the claim construction hearing in the ITC proceeding between the parties, Defendants specifically pointed out that Plaintiffs did not discuss applicants' disclaimer of oscillators whose frequency is controlled by an external crystal. Ex. S (ITC *Markman* Hearing Tr.) at 143:7-23. Defendants then presented a comprehensive discussion of the actual words used by applicants to disclaim frequency control, including those set forth above. *Id*. at 145:3 -156:3. When Plaintiffs were given the opportunity to explain why they felt those words were not disclaimers of frequency control, they chose not to do so and, instead, again focused on what Magar itself discloses and the disclaimer relating to causing oscillation. *Id*. at 205:6-214:6. This pattern repeated itself in the post-hearing briefing to the Commission. *See* Ex. T (Complainants' Petition for Review) at 16-21; Ex. U (Respondents' Response to Complainants' Petition for Review) at 30-40. The reason for this pattern of silence on this issue is clear: Plaintiffs have no credible factual basis to dispute that disclaimers over frequency control were made, and no credible legal basis to dispute that such disclaimers must be reflected in the proper claim construction.

the actual clock signal used by the CPU," Plaintiffs incorrectly argue that the construction of "entire oscillator" is limited to this distinction. As established above, applicants ***also*** argued that the "entire oscillator" is different from Magar because the clock signal *frequency* of Magar's oscillator was controlled by the external crystal. The applicants themselves acknowledged that these were two different (albeit closely related) arguments, and indicated that they were relying on both arguments when they told the examiner:

> The Magar teaching . . . is specifically distinguished from the instant case in that it is both *fixed frequency* (*being crystal based*) and *requires an external crystal or external frequency generator*.

Ex. E (Feb. 10, 1998 Amend.) at 4 (TPL853_02954560). Federal Circuit precedent is clear that when multiple disclaimers are made the Court's claim construction must capture ***all*** of the disclaimers. *Krippelz v. Ford Motor Co.*, 667 F.3d 1261,1267 (Fed. Cir. 2012); *Am. Piledriving Equip. v. Geoquip, Inc.*, 637 F. 3d 1324, 1336 (Fed. Cir. 2011). This is true even if one of the disclaimers was unnecessary. *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 979 (Fed. Cir. 1999).

Third, Plaintiffs' opening brief inaccurately suggests that generating a clock signal somehow is distinct from setting the clock signal's frequency. Not so. Every clock signal has a frequency from its inception. Thus, generating a clock signal and setting its frequency are part and parcel of the same act. Accordingly, as the ITC found, Plaintiffs' argued distinction between generating a clock signal and setting its frequency fails because the two concepts are inseparable:

> Furthermore, the ALJ found that "the process of setting the frequency of a clock signal and generating a clock signal are inseparable, because a clock signal must have a frequency, since it [sic] sole purpose is to provide a frequency for timing the operations of devices." *Id.* We affirm the ALJ's finding and analysis.

Ex. N, Commission Opinion at 28-30 (quoting ID at 121); Ex. Q, ID at 120-124 (finding, *inter alia*, that at its base, a clock is a periodic signal, that the periodicity is the frequency of the clock, and that frequency is "incidental to clock generation").

Finally, Plaintiffs mischaracterize Defendants' construction. Defendants do not contend that applicants disclaimed "all use of an external crystal." Pl. Op. Br. at 9. What Defendants

contend is that applicants disclaimed those uses of an external crystal to control the frequency of, or cause oscillation of, the claimed "entire oscillator," and only those uses are excluded by Defendants' construction.

C. Plaintiffs' Arguments About The Word "Cause" Lack Merit

As established in Defendants' opening brief and as discussed above, applicants also distinguished their purported invention from Magar on the grounds that Magar required an external crystal oscillator to cause clock signal oscillation. Def. Op. Br. at 10. These prosecution history arguments constitute a second independent disclaimer, which is properly reflected in Defendants' construction. Although Plaintiffs are less than unequivocal on this point, and although their proposed construction lacks this disclaimer, Plaintiffs do not appear to dispute that the "entire oscillator" may not use an external crystal or clock generator to cause clock signal oscillation. Pl. Op. Br. at 7-8. Instead, Plaintiffs focus on the use of the term "cause" in Defendants' construction. *Id.* at 8-9.

In this regard, Plaintiffs argue without support that the term "cause" in Defendants' construction is "significantly broader than the concept of 'generation.'" Pl. Op. Br. at 9. As an initial matter, Plaintiffs' argument is irrelevant because neither construction uses the term "to generate." Plaintiffs' argument is also incorrect because the definition of "generate" includes the word "cause": "to bring into existence; ***cause*** to be; produce." Ex. R, THE RANDOM HOUSE DICTIONARY OF THE ENGLISH LANGUAGE (2d ed. 1987). Defendants are not using the word "cause" to change the meaning of the word "generate." Rather, as explained in Defendants' opening brief, that word clarifies in plain English the meaning of the word "generate" to obviate the kind of jury confusion that occurred in the HTC trial, and in light of the post-*Markman* hearing arguments over the meaning of that word in the ITC proceedings. Def. Op. Br. at 17-18.

Plaintiffs' other assertions regarding the word "cause" also lack merit. Plaintiffs hypothesize that, under Defendants' construction, "a general reset signal that is asserted on power-on and that holds many systems in a non-active state for some period of time" could be a control signal that causes clock signal oscillation. Pl. Op. Br. at 9. But Plaintiffs never explain

how a signal that "that holds many systems in a *non-active state*" could possibly be said to *cause* oscillation. Plaintiffs then suggest that Defendants' construction could cover "a signal that causes power to be applied to the clocking systems." *Id*. This is incorrect. Defendants' construction does not exclude reliance on a power signal (or a power button, battery connection or any other such potential "but for" causes of clock signal oscillation). Defendants' construction only excludes what applicants disclaimed: reliance on an external crystal oscillator/clock generator or control signal that causes clock signal oscillation.

D. Plaintiffs Ignore Applicants' Disclaimers Over Sheets

As established in Defendants' opening brief, applicants distinguished their claimed invention from the Sheets prior art reference on the ground that Sheets required a control signal to generate a clock signal. Def. Op. Br. at 12-13. But just as Plaintiffs' brief ignores applicants' disclaiming statements about frequency control, their brief ignores all but one line of applicants' disclaiming statements about control signals and then quotes that single line out of context.

Specifically, Plaintiffs partially quote the file history as saying "obviates the need for provision of the type of frequency control information described by Sheets" and then argue that the quoted statement merely means that the use of control signals is not required in the claimed invention, not that they cannot be used. Pl. Op. Br. at 10. Plaintiffs' argument fails upon even a cursory review of what applicants argued to get around Sheets:

> ***Crucial to the present invention*** is that . . . when fabrication and environmental parameters vary, the oscillation or ***clock frequency*** and the frequency capability of the driven device ***will automatically vary*** *together*. ***This differs from all cited references in that*** . . . the oscillator or variable speed clock varies in frequency but ***does not require manual or programmed inputs*** or external or extra components ***to do so***.

Ex. D at 5 (TPL853_00002429).

> Even if the examiner is correct that the variable speed clock in Sheets is in the same circuit as the microprocessor of system 100, that still does not change the claimed subject matter. ***In Sheets, a command input is required to change the clock speed. In the present invention, the clock speed varies correspondingly to variations in operating parameters . . . No command input is necessary to change the clock frequency.***

Ex. G at 4 (TPL853_00002449). Thus, applicants told the Patent Office that their invention does not require control by programmed inputs, distinguished "all cited references" on that ground, and

then specifically distinguished Sheets on that very ground. In doing so, the applicants told the Patent Office that this feature is the reason why the "clock frequency and the frequency capability of the driven device will automatically vary together"—a feature they told the Patent Office is "[c]rucial to the present invention." The applicants' arguments leave no doubt that their invention does not rely on a control signal to change the clock frequency. *See Microsoft Corp. v. Multi-Tech Sys., Inc.*, 357 F.3d 1340, 1351-52 (Fed. Cir. 2004) (construing claim to require a feature that was "central to the functioning of the claimed invention"); *see also Ballard Med. Prods. v. Allegiance Healthcare Corp.*, 268 F.3d 1352, 1360-62 (Fed. Cir. 2001) (use of "present invention" signifies that disclaimer applies to all claims).

The applicants' disclaiming arguments also establish that their invention ***as claimed*** cannot rely on a control signal. As discussed above, applicants argued that their CPU frequency and clock speed vary together because the clock does not rely on inputs. The claims expressly require that the CPU frequency and clock speed vary together. Therefore, the claims cannot cover a clock that relies on inputs to change the clock speed because that is precisely what applicants disclaimed to get around Sheets.

Here, applicants' arguments regarding control inputs include a disclaimer of the use of a control signal to control the frequency of the clock signal, and not just that "the oscillator or variable speed clock in their invention varies in frequency." Pl. Op. Br. at 10. The claims are limited by both of these disclaimers. *See Saffran*, 712 F.3d at 559.[6]

E. Plaintiffs' Discussion Of Talbot Is Irrelevant

Plaintiffs' opening brief addresses the prosecution history discussion of the Talbot prior

[6] As explained by the Federal Circuit in *Saffran*:

> Saffran's arguments to the examiner presented two bases for distinguishing Gaskill: (i) that his device is a sheet, and (ii) that his device is not a pre-formed chamber. Even if, as Saffran suggests, the examiner had relied only on the latter, that would not annul the remainder of his statement. "Rather, as we have made clear, an applicant's argument that a prior art reference is distinguishable on a particular ground can serve as a disclaimer of claim scope even if the applicant distinguishes the reference on other grounds as well." *Andersen Corp. v. Fiber Composites, LLC*, 474 F.3d 1361, 1374 (Fed. Cir. 2007).

art reference. Pl. Op. Br. at 10-11. But that part of the prosecution history is irrelevant because it relates to the "ring oscillator" claim limitation, not the "entire oscillator" term at issue here. Defendants do not rely on any statements or arguments made in the prosecution history relating the Talbot reference to support their construction of the "entire oscillator" term or that there was a disclaimer as to that term, so this discussion is entirely irrelevant to the issue at hand.

To be sure, even if the prosecution history concerning Talbot were relevant, it could not undo applicants' disclaimers. Applicants made their disclaimers during the original prosecution of the '336 patent, while Talbot was cited during reexamination, and claims cannot be broadened during reexamination. 35 U.S.C. § 314 (pre-AIA) ("no proposed amended or new claim enlarging the scope of a claim of the patent shall be permitted."); *Hakim v. Cannon Avent Group Plc*., 479 F.3d 1313, 1317-18 (Fed. Cir. 2007) (prosecution disclaimer cannot be rescinded absent sufficiently clear statement).

III. PLAINTIFFS MISCHARACTERIZE THE PRIOR CONSTRUCTIONS

Plaintiffs' "Factual Background" section is rife with incorrect or misleading statements about prior construction of the "entire oscillator" term. For example, Plaintiffs baldly assert that "this Court has held that the intrinsic record permits the use of an external crystal or clock generator as a reference signal . . ." Pl. Op. Br. at 1. Plaintiffs cite no support for this "fact" – because there is none.

A. Plaintiffs Mischaracterize Judge Ward's Prior Construction

Plaintiffs argue that Judge Ward's construction "left open the possible use of an external crystal/clock generator for a *reference signal*." Pl. Op. Br. at 2 (emphasis in original). However, Judge Ward's order does not state or suggest that an external crystal/clock generator could be used as a reference signal. To the contrary, Judge Ward explained that the dispute before him was "whether the ring oscillator may rely on a control signal or an external crystal/clock generator." Ex. L at 11. And Judge Ward concluded that he "***agrees with the defendants*** that the applicant disclaimed the use of an input control signal and an external crystal/clock generator ***to generate a clock signal.***" *Id*. at 12 (emphasis added).

B. Plaintiffs Mischaracterize Judge Ware's Prior Construction

Plaintiffs next assert that Judge Ware "considered" the phrase "entire ring oscillator variable speed system clock." Pl. Op. Br. at 2. This is incorrect: Judge Ware construed the term "ring oscillator" – not "entire oscillator," or even "entire ring oscillator variable speed system clock." *See* Ex. B to Bumgardner Decl.; Pl. Op. Br. at 13. In addition to mischaracterizing the subject of Judge Ware's construction of "ring oscillator," Plaintiffs neglect to mention that the focus of Judge Ware's inquiry was whether the voltage controlled oscillator in the Talbot prior art reference was a ring oscillator – and not any other issue concerning frequency control or the meaning of "entire oscillator." *Id*. Furthermore, while Plaintiffs' opening brief implies that Judge Ware's call for additional briefing reflected a deficiency in the briefing of defendants (Pl. Op. Br. at 2-3), it was actually the sufficiency of *Plaintiffs*' position on "ring oscillator" with which Judge Ware was concerned:

> The Court has examined the Talbot patent. Although the component is, indeed, referred to as a "voltage-controlled oscillator," declarations and other extrinsic materials that have been tendered during the claim construction proceedings ***call into question the validity of the inventors' contention to the PTO and to this Court*** that the "ring oscillator" is different from the "voltage-controlled oscillator" disclosed in Talbot.

Id. at 16 (emphasis added).

C. Plaintiffs Focus On The Construction Of A Different Term, "Ring Oscillator"

Plaintiffs next address this Court's construction of "ring oscillator." Pl. Op. Br. at 3. The "ring oscillator" term is *a different term*, which does not appear in either of the two asserted independent claims in this case (claims 6 and 13). Those claims instead recite "an entire oscillator." Ex. A, '336 patent at claims 6, 13. In this litigation, the meaning of "ring oscillator" is not in dispute because the parties have agreed upon the construction of the term "ring oscillator" in the asserted dependent claims (claims 9 and 15). Dkt. No. 72 (JCCS), Ex. A at 5 (construing "ring oscillator" to mean "an [oscillator] having multiple, odd number of inversions arranged in a loop, wherein the [oscillator] is variable based on the temperature, voltage and process parameters in the environment").

D. Plaintiffs Mischaracterize The ITC's Claim Construction

Plaintiffs next engage in spin control in attempting to minimize their loss on this very issue in the ITC. Pl. Op. Br. at 3-4. Plaintiffs first focus (again without explanation as to relevance) on ALJ Gildea's construction of the "ring oscillator" term, as opposed to his construction of the "entire oscillator" term. And while Plaintiffs eventually acknowledge that ALJ Gildea rejected their construction at the ITC, Plaintiffs limit their discussion of claim construction in the ITC to solely ALJ Gildea's *Markman* order, ignoring the portions of his Initial Determination, as well as the Commission's affirmance of that decision, that directly bear on the claim construction issue before this Court.

For example, Plaintiffs ignore ALJ Gildea's flat rejection of Plaintiffs' position that controlling the frequency of a clock signal is separate from generating it in his Initial Determination:

> What Dr. Oklobdzija [Plaintiffs' expert] and his fellow authors said in their book coincides with Respondents' argument that ***the process of setting the frequency of a clock signal and generating the clock signal are inseparable***, because a clock signal must have a frequency, since its sole purpose is to provide a frequency for timing the operations of devices.
>
> …
>
> Frequency – and the regulation thereof, which is a form of control – are ***incidental to clock generation***.

Ex. Q (Initial Determination) at 121, 123 (emphasis added). Plaintiffs also ignore the Commission's affirmance of ALJ Gildea's finding on this issue. After citing many of the same statements by applicants discussed earlier in this brief, including as the final sentence the applicants' statement that the Magar patent "*is specifically distinguished from the instant case in that it is* ***both*** *fixed frequency (being crystal based)* ***and*** *requires an external crystal or external frequency generator,*" the Commission stated:

> The patent applicants' statement in the final sentence quoted above, in particular, shows that the applicants intended to disclaim, not only an external crystal/frequency generator, ***but also a fixed frequency, crystal controlled generator***. Thus, the "entire oscillator" limitation requires both that the circuitry required to generate and/or determine (adjust) the frequency of the oscillator's clock rate must be entirely on-chip.

Ex. N (Commission Opinion) at 24 (emphasis in original); *see also id.* at 29-30 ("We find that the ALJ's application of his construction of the 'entire oscillator' limitation to the Accused Products was correct, including in particular his discussion of the intricate relationship between the generation and frequency of a clock signal.").

E. Plaintiffs Mischaracterize HTC Litigation Events

Plaintiffs' opening brief next discusses this Court's treatment of HTC's summary judgment motion and subsequent Emergency Motion. Pl. Op. Br. at 4. As Plaintiffs acknowledge, in the Court's summary judgment order, "the Court did agree that, as a result of prosecution history, the claims exclude 'any external clock used to *generate* a clock signal.'" Pl. Op. Br. at 4 (emphasis in original); Ex. H to Bumgardner Decl. at 11 (summary judgment order). Significantly, the very next sentence of the Court's order (which Plaintiffs' brief ignores) states that "there remains a factual dispute whether HTC's products contain an on-chip ring oscillator that ***is self-generating*** and ***does not rely on an input control to determine its frequency***." Ex. H to Bumgardner Decl. at 11 (emphasis added). The existence of a factual issue concerning whether HTC's products include a self-generating oscillator and rely on an input control to determine frequency only would have been relevant if the Court's construction excluded such reliance. Thus, the Court's summary judgment order does not support Plaintiffs' current claim construction position.

In response to the summary judgment order, HTC brought an Emergency Motion. Pl. Op. Br. at 4. The Court ruled that the jury would be instructed that the "entire oscillator" term "is properly understood to exclude any external clock used to generate a signal." Ex. K to Bumgardner Decl. at 1. While, as Plaintiffs note, the Court did not grant HTC's additional request to further instruct the jury that the "entire oscillator" must be self-generating and cannot rely on an input control signal to determine its frequency, the Court did not state its reasons for declining to do so (or otherwise discuss those additional requests in its order). *Id.* Indeed, when the Court later addressed this issue in its JMOL Order, the Court noted only that the "Court chose not to adopt the second sentence of HTC's proposal . . . ." Ex. L to Bumgardner Decl. at 9. Notably, the Court did not explain why it chose not to do so.

IV. PLAINTIFFS' REMAINING ARGUMENTS ALSO LACK MERIT

Although Plaintiffs' construction does not incorporate any prosecution history disclaimer, Plaintiffs nonetheless make the remarkable assertion that their construction of the "entire oscillator" term is consistent with this Court's prior construction of that term. Pl. Op. Br. at 7. This assertion is surprising because the Court instructed the jury that the "entire oscillator" limitation is "properly understood to exclude any external clock used to generate a clock signal."

Plaintiffs contend that their construction is consistent with the Court's prior construction, because their construction requires that the oscillator be "located entirely on the same semiconductor substrate as the CPU," and because other claim language requires that the oscillator "generates the signal(s) used for timing the operation of the [CPU]." Pl. Op. Br. at 7. Thus, according to Plaintiffs, their construction "already makes clear that an external clock may not generate the signal used to clock the CPU." *Id.* at 8. Of course, there is no dispute that an external clock that generates the CPU clock signal cannot be the claimed "entire oscillator," because, among other reasons, such a clock would not be on the same semiconductor substrate as the CPU. However, unlike the Court's prior construction in the HTC case, which "exclude[s] any external clock used to generate the signal used to clock the CPU" (Ex. K. to Bumgardner Decl. at 1), Plaintiffs' current construction could be read to allow an on-chip oscillator that uses an external clock to generate the signal used to clock the CPU. As established above in Section II and in Defendants' opening brief (at 7-13), such a construction would be both incomplete and incorrect, because applicants clearly and unambiguously disclaimed on-chip oscillators that rely on a control signal or an external crystal/clock generator to cause clock signal oscillation or control clock signal frequency.

V. CONCLUSION

Federal Circuit law requires that the full extent of applicants' prosecution history disclaimers, including the frequency control disclaimers, be reflected in the construction of "entire oscillator." Defendants' construction must therefore be adopted.

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ATTESTATION

I, Aaron Wainscoat, am the ECF User whose ID and password are being used to file this Defendants' Responsive Claim Construction Brief. In compliance with Civil Local Rule 5-1(i)(3), I hereby attest that the signatories listed above have read and approved the filing of this brief.

Dated: August 18, 2015

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Exhibit “E”

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UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. HUAWEI TECHNOLOGIES CO., LTD., HUAWEI DEVICE CO., LTD., HUAWEI DEVICE USA INC., FUTUREWEI TECHNOLOGIES, INC., HUAWEI TECHNOLOGIES USA INC., Defendants.	Case No. 3:12-cv-03865-VC (PSG) **PLAINITIFFS' RESPONSIVE CLAIM CONSTRUCTION BRIEF**
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. GARMIN LTD., GARMIN INTERNATIONAL, INC., and GARMIN USA, INC., Defendants.	Case No. 3:12-cv-03870-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. ZTE CORPORATION and ZTE (USA) INC., Defendants.	Case No. 3:12-cv-03876-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. SAMSUNG ELECTRONICS CO., LTD. and SAMSUNG ELECTRONICS AMERICA, INC., Defendants.	Case No. 3:12-cv-03877-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. LG ELECTRONICS, INC. and LG ELECTRONICS U.S.A., INC., Defendants.	Case No. 3:12-cv-03880-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. NINTENDO CO., LTD. and NINTENDO OF AMERICA, INC., Defendants.	Case No. 3:12-cv-03881-VC (PSG)

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Cases:

I. INTRODUCTION

The intrinsic record does not evidence any clear and unambiguous surrender of claim scope regarding the "entire oscillator" phrase. Defendants' disclaimer position distorts statements made by applicants during prosecution and ignores the context in which they were made. As demonstrated herein, the prosecution history of the patent-in-suit merely reflects that applicants distinguished the claims at issue from the cited references on the basis of other claim limitations. Ultimately, Plaintiffs' construction accurately reflects the true, bargained-for meaning of the "entire oscillator" phrase.

II. ARGUMENT

A. Applicants did not make the disclaimers advanced by Defendants.

Applicants did not make the vague and broad disclaimers advanced by Defendants in their construction of "entire oscillator." To the contrary, in distinguishing over the references cited by Defendants, applicants successfully demonstrated that the references at issue did not satisfy the claim limitations of (i) an on-chip oscillator[1] (ii) whose frequency varied in the same way as the CPU as a function of processing variation, operating voltage, and temperature ("PVT factors").[2] Specifically, the cited references (Magar and Sheets) disclosed either an off-chip crystal or an off-chip oscillator to generate the signal used to clock the CPU. Not only did these references fail to disclose an on-chip oscillator, but the references' oscillators would not vary according to PVT factors in the same way as the CPU. Applicants' arguments for distinguishing the claims at issue from Magar and Sheets were clearly based on limitations present in the claims themselves,

[1] For example, claim 6 recites "a [CPU] *disposed upon an integrated circuit substrate*…" and "an entire oscillator *disposed upon said integrated substrate*…." See Ex. S to Declaration of Barry J. Bumgardner (hereinafter "Bumgardner Decl."), Re-examination Certificate of U.S. Pat. No. 5,809,336, 2:15-20. The parties agree that the "entire oscillator" must be "located entirely on the same semiconductor substrate as the [CPU]…."

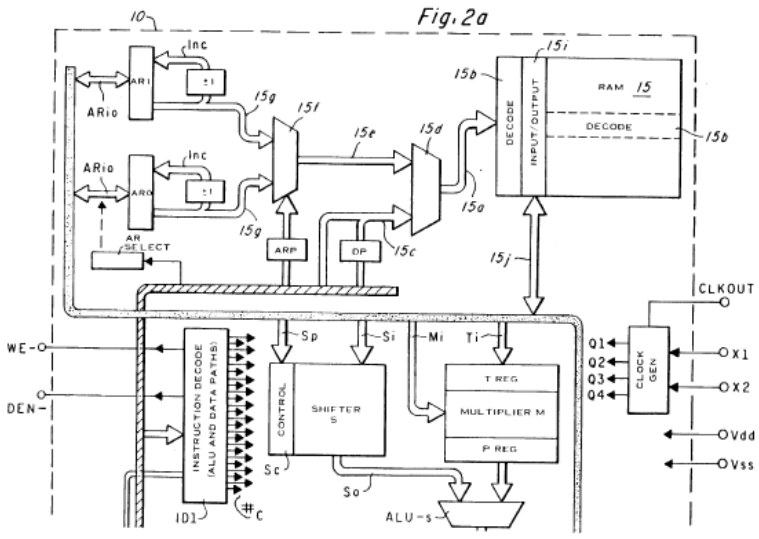
[2] For example, claim 6 recites "thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as *a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate*, thereby enabling said processing frequency to track said clock rate in response to said parameter variation…." Ex. S at 2:23-30.

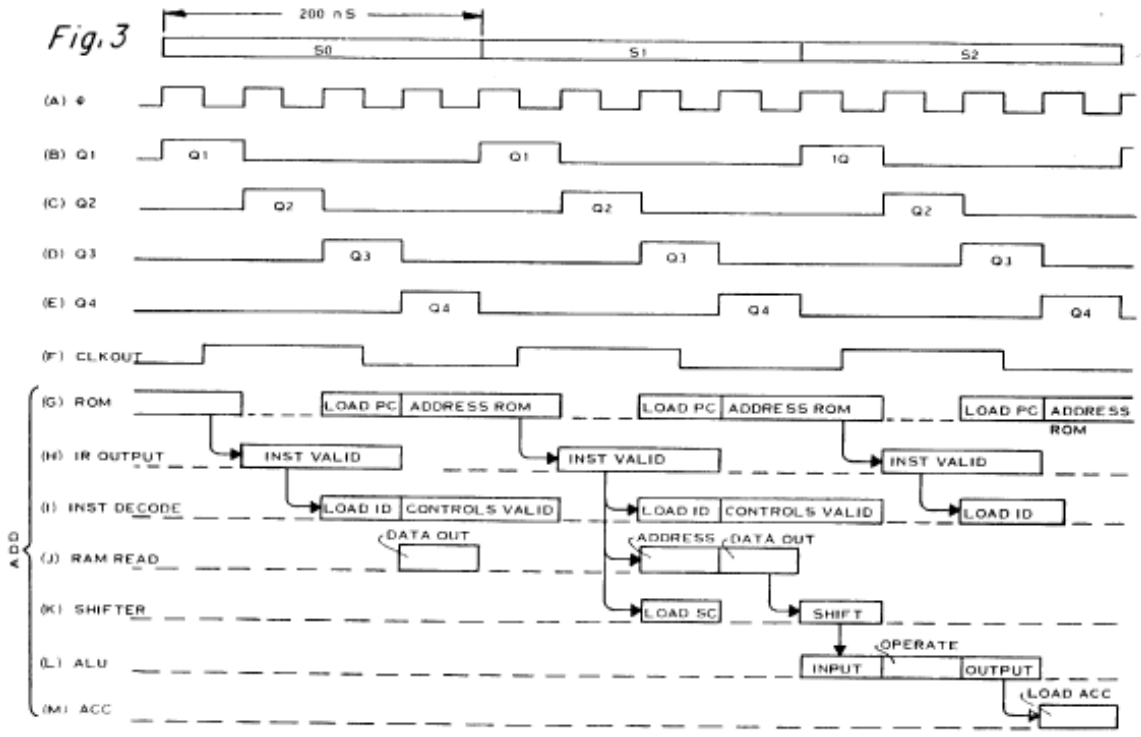
and no disclaimers were made. Without question, applicants never made any statements prohibiting the claimed on-chip oscillator that clocks the CPU from using an off-chip crystal as a reference signal, which is what Defendants seek to exclude by sleight of hand via their overly broad and vague claim construction.

1. U.S. Patent No. 4,503,500 to Magar ("Magar").

In distinguishing the claims at issue from Magar, Defendants allege that applicants disclaimed any use of an "external crystal / clock generator" to (1) "cause clock signal oscillation" or (2) "control clock signal frequency." This position, presented previously to this and other courts, is not supported by the intrinsic record. The record is clear that applicants distinguished Magar on the basis that Magar disclosed an ***external crystal*** used to ***generate*** the clock signal supplied to the CPU. Applicants further distinguished Magar on the basis that Magar's external crystal would not vary according to PVT factors.

Figures 2 and 3 of Magar demonstrate that Magar utilizes an external crystal to generate a 20MHz clock signal. That clock signal, which has a period of 50 nanoseconds, drives the on-chip "CLOCK GEN" circuitry shown below in Figure 2 and diagramed in Figure 3. Bumgardner Decl. Ex. T, U.S. Pat. No. 4,503,500 to Magar at Figs. 2a, 3, 15:23-41.





After receiving the 20MHz signal via pins X1 and X2, the "CLOCK GEN" circuitry in Magar divides the received signal from the crystal oscillator to create four quarter-cycle clocks seen in Q1-Q4. Ex. T at 15:23-35. These four, slower clock signals are each of a period of 200 nanoseconds (a 5MHz clock signal). In Magar, there is no on-chip oscillator that generates these 5MHz clock signals. Rather, the clock signal for the CPU is generated by the off-chip crystal.

In distinguishing their claims from Magar, applicants relied on limitations that are expressly included in the patent claims themselves. Specifically, applicants argued that, unlike their inventions, the oscillator detailed in Magar was not on-chip. Additionally, applicants explained that Magar's off-chip crystal and the speed of Magar's CPU would not vary together according to PVT factors. See Bumgardner Decl. Ex. U, '336 Patent, File History, Response to Office Action at 3-4 (July 7, 1997). As explained in applicants remarks, crystal oscillators do not vary (or vary minimally) due to PVT factors. Notably, both the on-chip/off-chip distinction and the PVT factor variability distinction relied upon by applicants are expressly present in the claims. Neither of these distinctions is directed to the meaning of the "entire oscillator" limitation.

In addition to the passages cited by Defendants – which when read properly show nothing more than applicants' explanation between generating a clock signal by an on-chip, electronic oscillator (as in the '336) and generating a clock signal by an off-chip crystal – applicants provided a clear, contextual meaning for their statements in the following passages:

> In making the rejection based on Magar, the examiner appears to be confusing the multiple uses and meanings of the technical term "clock." A clock is simply an electrical pulse relative to which events take place. **Conventionally, a CPU is driven by a clock that is *generated* by [a] crystal. The crystal might be connected directly to two pins on the CPU, as in Magar,** and be caused to oscillate by circuitry contained in the CPU with the aid of possible other external components . . .
>
> The present invention is unique in that it applies, and can only apply, in the circumstance *wh**ere the oscillator or variable speed clock is fabricated on the same substrate as the driven device*** . . . Thus in this example, the user designs the ring oscillator (clock) to oscillate at a frequency appropriate for the driven device when both the oscillator and the device are under specified fabrication and environmental parameters.

Id. at 4-5 (emphasis added). The critical difference explained by applicants in this passage is that the claimed oscillator used to generate clock signal is fabricated on the same chip as the CPU, and thus subject to the same PVT factors as the CPU. Nowhere in this explanation, or otherwise, do applicants state that the oscillator cannot utilize external reference signals (from fixed frequency sources or otherwise), such as in a PLL where an external crystal is used as a reference for the oscillator contained on the chip. This is consistent with Judge Grewal's previous finding that the prosecution history of the patent did not "impose a prohibition on all types of control." Bumgardner Decl. Ex. D, *HTC Corp. v. Technology Properties Ltd., et al.*, No. 3:08-cv-882, Dkt. No. 509 at 10 (August 21, 2013 - Claim Construction Order) (the "Grewal Markman Order").

After making the aforementioned argument to the examiner, the applicants again faced a rejection in light of Magar. Rather than abandon their previous arguments, applicants amended their claims to expressly require that the entire oscillator is present on the integrated circuit. This amendment clarifies the distinction that applicants were making over Magar, namely that circuitry sufficient to create a clock signal must be found on the same substrate as the CPU, thus making it subject to the same PVT factors of variability (*e.g.*, temperature). In explanation of

their amendment, applicants wrote:

> [T]he independent claims have been rewritten to specify that the ***entire*** ring oscillator variable speed system clock, variable speed clock or oscillator ***be provided in the integrated circuit***, in order to sharpen the distinction over the prior art . . . ***[T]he prior art circuits require an external crystal*** . . .
>
> ***Magar's clock generator relies on an external crystal connected to terminals X1 and X2 to oscillate***, as is conventional in microprocessor designs. It is not an entire oscillator in itself.

Bumgardner Decl. Ex. U, '336 Patent, File History, Response to Office Action at 3 (February 10, 1998).

The applicants correctly observed that Magar "requires" an external crystal to oscillate and generate a clock signal. *Id*. at 4 (Magar "***requires*** an external crystal"; Magar's "clock gen" block "lacks the crystal or external generator that it ***requires***"); *id*. at 5 (Magar "***requires*** an external crystal or external frequency generator"). Notably, applicants pointed out that the oscillator of the claims at issue must be on-chip. Thus, the file history is clear that the applicants made a critical distinction between Magar (and similar references) and the '336 invention: the oscillator that ***generates*** the CPU clock in Magar is an off-chip crystal, while the oscillator that ***generates*** the CPU clock in the '336 invention is an on-chip, electronic oscillator. The file history never discussed – much less disclaimed – the use of PLL circuitry (including an off-chip reference crystal) to adjust the frequency of a clock signal that was already ***generated*** by an on-chip oscillator.

Notably, the distinctions over Magar relied upon by the applicants are found in the claims themselves. Claim 6 expressly requires the "entire oscillator disposed upon said integrated circuit substrate and connected to said [CPU]." The parties' constructions are already in agreement that the "entire oscillator" is "located entirely on the same semiconductor substrate as the [CPU]." And claim 6 already requires PVT variability, reciting "varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated semiconductor substrate…." The point is that the claims themselves already contain the distinctions relied upon by applicants in

distinguishing Magar. There is no factual (or legal) basis for inserting the vague and broad disclaimers advocated by Defendants in the "entire oscillator" construction.

Defendants' citations to the prosecution history distort the statements actually made by applicants with regard to Magar. Regarding the first and second cited passages from the prosecution history (found on pages 8 and 9 of Defendants' Brief[3]), Defendants erroneously claim that "applicants ***expressly and unambiguously disclaimed*** oscillators that rely on an external crystal for ***frequency control.***" Defts' Brief at 9 (emphasis in original). This statement does not comport with what applicants actually said in the passages relied upon by Defendants. In the first passage cited by Defendants, applicants distinguished Magar on the basis that it used an external clock to drive the CPU:

> A review of the Magar reference shows that it is apparently no more pertinent than prior art acknowledged in the application, in that ***the clock disclosed in the Magar reference is in fact driven by a fixed frequency crystal, which is external to the Magar integrated circuit***.

Defts' Brief at 8 (emphasis in Defts' Brief). Nothing in this passage pertains to "frequency control," whatever Defendants' mean by this phrase. The clear distinction made by applicants is Magar's lack of an on-chip oscillator.

In the second passage cited by Defendants, applicants again distinguish Magar on the basis of Magar's use of an off-chip crystal:

> Contrary to the Examiner's assertion in the rejection that 'one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock vary together due to manufacturing variation, operating voltage and temperature of the IC [integrated circuit],' one of ordinary skill in the art should readily recognize that the speed of the CPU and clock ***do not*** vary together due to manufacturing variation, operating voltage, and temperature of the IC in the Magar processor . . . ***This is simply because the Magar microprocessor clock is frequency controlled by a crystal which is also external to the microprocessor***. Crystals are by design fixed frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in

[3] *Technology Properties Ltd. et al. v. Samsung Electronics, et al.*, No.3:12-cv-3877, Dkt. 94 (hereinafter "Defts' Brief).

> manufacturing, operating voltage and temperature. ***The Magar microprocessor in no way contemplates a variable speed clock as claimed***.

Defts' Brief at 8-9 (emphasis in Defts' Brief). The applicants' statement that "the Magar microprocessor clock is frequency controlled by a crystal which is also external to the microprocessor" merely points out that, unlike the claims at issue, the signal used to clock the on-chip CPU in Magar is provided by an external crystal. The portions of applicants' statements highlighted in Defendants' brief are certainly not a clear and unequivocal disclaimer pertaining to any notion of "frequency control" and cannot be extended to support Defendants' construction that the claimed oscillator does "not rely on a ***control signal*** or an external crystal clock to … ***control*** clock signal frequency." In fact, these passages say absolutely nothing about whether an on-chip oscillator (which clocks the on-chip CPU) could rely on an external crystal for "frequency control." There is simply no "unmistakable" disavowal present in these passages.

Defendants next cite to portions of the prosecution history where applicants correctly distinguish their claims from the Magar on the basis that crystals are not subject to PVT factors, such as temperature:

> ***[C]rystal oscillators have never***, to Applicants' knowledge, ***been fabricated on a single silicon substrate with a CPU***, for instance. ***Even if they were***, as previously mentioned, crystals are by design fixed-frequency devices whose oscillation frequency is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. ***The oscillation frequency of a crystal on the same substrate with the microprocessor would inherently not vary due to variations in manufacturing, operating voltage and temperature in the same way as the frequency capability of the microprocessor on the same underlying substrate, as claimed.***

Defts' Brief at 9 (emphasis in Defts' Brief). Defendants disingenuously misconstrue this passage as an "express disclaimer" that "the claims exclude oscillators using crystals to control frequency of the clock signal." *Id.* This alleged sweeping disclaimer is found nowhere in the cited passage. It is simply not there. What is stated in this prosecution history is that a crystal clock's frequency would not vary as a function of PVT like the "microprocessor on the same underlying substrate, ***as claimed***." And as set forth above, what is ***claimed*** is an "entire oscillator" whose frequency varies along with that of the CPU according to PVT factors.

In the next passage of prosecution history cited by Defendants, applicants again distinguish the claims' on-chip electronic oscillator from Magar's use of an external crystal. Defts' Brief at 10. Applicants pointed out that, in their inventions, the signals are subject to variation due to PVT factors while in Magar the signals are "determined by the fixed frequency of the external clock." Nothing in this passage remotely addresses the issue of whether the patent's "entire oscillator" may utilize an external crystal as a reference signal. Nor could this passage legally support a sweeping disclaimer as to "control of the 'frequency or rate' of the clock."

In the final passage of Magar cited by Defendants, applicants again distinguish their invention from Magar on the basis of Magar's use of an external crystal (i.e. lack of an on-chip oscillator), whose frequency is not subject to PVT factors:

> Magar's clock generator ***relies on an external crystal*** connected to terminals X1 and X2 to oscillate, as is conventional in microprocessor designs. It is not an entire oscillator in itself. And with the crystal, ***the clock rate generated is also conventional in that it is a fixed, not a variable, frequency***. The Magar clock is comparable in operation to the conventional crystal clock 434 depicted in Fig. 17 of the present application for controlling the I/O interface ***at a fixed rate frequency, and not at all like the clock on which the claims are based***, as has been previously stated.

Defts' Brief, p. 10 (emphasis in Defendants' Brief). Defendants cite this passage for the alleged disclaimer that the oscillator may not "rely on a control signal or an external crystal/clock generator to ***cause clock signal oscillation***…." But this passage makes no such disclaimer, let alone one that is clear, unambiguous and unmistakable. Applicants are merely pointing out that Magar does not disclose an on-chip oscillator.

It is not entirely clear why Defendants seek to use the language "cause clock signal oscillation," thereby deviating from this Court's jury instruction that the claims exclude "any external clock used to ***generate*** a signal." Plaintiffs strongly suspect that Defendants seek to replace "generate" with "cause clock signal oscillation" in order to lodge a non-infringement argument that goes beyond Judge Grewal's prohibition and has nothing to do with the differences between the claims at issue and Magar. In any event, there is no basis for including a vague and broad disclaimer relating to "causing clock signal oscillation" because the prosecution history

does not clearly and unmistakably include this prohibition. To the extent there is any disclaimer arising from Magar, Judge Grewal's HTC jury instruction (as well as the express claim language itself) accurately addresses the scope of the invention.

2. U.S. Patent No. 4,670,837 to Sheets ("Sheets").

Prior to facing a rejection under Magar, applicants faced a rejection based on Sheets. Like Magar, Sheets differed drastically from the claimed inventions of the '336 patent. Sheets did not contain an on-chip oscillator, and it relied upon a technique for adjusting the frequency of a voltage control oscillator by writing a "digital word" from the microprocessor to the voltage control oscillator indicative of the desired operating frequency as a means of adjusting the clock frequency.

Applicants wrote:

> The present invention does not similarly rely upon provision of frequency control information to an **external clock**, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. . . Sheets' system for providing clock control signals to an **external clock** is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.

Bumgardner Decl. Ex. V, '336 Patent, File History, Office Action Response at 8 (April 11, 1996).

In a subsequent amendment, the applicants noted that the Sheets clock "***required***" a "digital word" or "command input." By contrast, in the '336 inventions, "both the variable speed clock and the microprocessor ***are fabricated together in the same integrated circuit***. No command input is ***necessary*** to change the clock frequency." Bumgardner Decl. Ex. W, ''336 Patent, File History, Office Action Response at 4 (Jan. 7, 1997). Thus, the applicants distinguished Sheets on at least two bases: (1) unlike the '336 invention, Sheets lacked an on-chip clock/oscillator; and (2) the off-chip clock in Sheets ***required*** a "digital word"/"command input" to vary clock frequency (i.e. it did not vary according to PVT factors). These distinctions do not come close to constituting a disclaimer of any "control signal" for any purpose. Indeed, the analog voltage and/or current supplied to a ring oscillator in a PLL is nothing like the "digital

command word" in Sheets. For example, while a ring oscillator may need power to oscillate (*i.e.*, analog voltage/current), it does not have the ability to accept a "digital command word" – nor could it be "***required***" to do so. Further, as discussed above, nothing said in overcoming the Magar reference prevents the use of external reference signals.

The citations Defendants make to the prosecution history once again attempt to remove statements from the context under which they were made. The clear, contextual meaning of applicants' statements is a narrow distinction over the cited reference, not broad disclaimer as alleged by Defendants. In the first passage cited by Defendants, applicants distinguished Sheets on the basis that Sheets discloses an external clock that would not vary according to PVT factors:

> The present invention does not similarly rely upon provision of frequency control information ***to an external clock***, but instead contemplates providing a ring oscillator clock and the microprocessor ***within the same integrated circuit***. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, ***since the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance***. Sheets' system for providing clock control signals to ***an external clock*** is thus seen to be unrelated to the ***integral microprocessor/clock system of the present invention***.

Defts' Brief at 12 (emphasis added by Plaintiffs). Unlike Sheets, the claims at issue contain an on-chip electronic oscillator that naturally varies according to PVT factors. Sheets, on the other hand, apparently varied frequency according to a "digital word"/"command input." Remarkably, Defendants cite the above passage for the proposition that applicants clearly and unmistakably disclaimed all "reliance on control signals." There is no such broad disclaimer present in this passage.

In the second passage cited by Defendants, applicants again distinguished Sheets on the basis that the Sheets clock does not vary according to PVT factors:

> Even if the examiner is correct that the variable clock in Sheets is in the same circuit as the microprocessor of system 100, that still does not give the claimed subject matter. ***In Sheets, a command input is required to change the clock speed. In the present invention, the clock speed varies correspondingly to variations in operating parameters*** . . . No command input is necessary to

change the clock frequency.

Defts' Brief, pp. 12-13 (emphasis by Plaintiffs). Once again, applicants pointed out that Sheets does not disclose a clock (whether on-chip or off-chip) whose frequency varies according to PVT factors, a requirement of the claim. There is simply no broad disclaimer of all "reliance on control signals" present in this passage.

In the final passage cited by Defendants, applicants again distinguished Sheets on the basis of PVT variation, noting that the on-chip oscillator and on-chip CPU must both vary frequencies according to PVT factors:

> ***Crucial to the present invention is that . . . when fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together***. This differs from all cited references in that . . . the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so.

Defts' Brief at 13 (emphasis by Plaintiffs). Applicants noted that Sheets, on the other hand, required "manual or programmed inputs or external or extra components" to vary its oscillator. In this passage, there is no disclaimer of "reliance on control signals." These words appear nowhere in this passage.

At the end of the day, all of Defendants' accused products contain an on-chip, electronic oscillator that varies according to PVT factors. Defendants improperly seek to exclude the accused oscillators' use of an external crystal as a reference signal by seeking a vague, broad, and improper disclaimer as to "reliance on control signals." As set forth above, applicants' response to Sheets does not make any such disclaimer, as applicants relied on express claim limitations (on-chip vs. off-chip, PVT factor variation) to distinguish the reference. It cannot be disputed that there is no unmistakable disclaimer of the on-chip, electronic oscillator using on an off-chip crystal oscillator as a reference signal in applicants' response to Sheets. Applicants' remarks regarding Sheets contain no such disclaimer.

B. The specification does not support Defendants' disclaimer arguments.

Recognizing the weakness of their prosecution history arguments, Defendants next argue that "the specification disclaims the prior art's fixed-speed clocks (which rely on a crystal, clock,

or signal to control the on-chip oscillator's frequency)…." Defts' Brief, p. 14. Defendants' specification-based disclaimer argument, however, is factually inaccurate and the case law cited by Defendants do not support a finding of disclaimer.

First, Defendants misrepresent the specification by claiming that "the specification criticizes prior art solutions that clocked a CPU with a fixed clock, such as, for example, a clock whose frequency is controlled by an external crystal." *Id.* at 13 (citing '336 patent, 16:48-53 and 17:12-23). This argument is ***highly misleading***, as ***nowhere*** in the passages cited by Defendants does the specification discuss "a clock whose frequency is ***controlled*** by an external crystal." The passages cited by Defendants merely make reference to a "traditional CPU design," which as applicants pointed out in distinguishing Magar involves the use of an off-chip crystal to ***generate*** the actual clock signal for an on-chip CPU. The specification excerpts cited by Defendants do not discuss using an off-chip crystal to ***control*** an on-chip oscillator. Therefore, this passage cannot be read to support the sweeping disclaimer advocated by Defendants. Moreover, the fact that the patent was critical of using an off-chip crystal to generate the actual clock signal for the CPU is of no consequence to this claim construction proceeding as the claims themselves clearly exclude such a scenario from infringement (*i.e.*, the "entire oscillator" must be "located entirely on the same semiconductor substrate as the [CPU]").

Second, Defendants make another misleading statement - "[r]ejecting the prior art fixed-speed clock approach (***which is the approach used in the Defendants' accused products***), the '336 patent discloses a variable-speed oscillator that is completely on the same semiconductor substrate as the CPU and whose speed freely varies with the PVT parameters of the substrate." Defts' Brief at 13-14 (emphasis by Plaintiffs). Contrary to this assertion, Defendants' accused products employ a technique called "dynamic frequency scaling", whereby the frequency of the clock signal generated by an on-chip oscillator and supplied to the CPU is increased during periods of high activity (so that the accused device can quickly respond to user inputs and be perceived as "high performance"), and decreased during periods of low activity (to conserve battery life and reduce power consumption). This oscillator is on the same semiconductor as the CPU and does vary with PVT. What Defendants hope to accomplish is to exclude the oscillators'

use of an external crystal as a reference signal. But, this situation is not addressed by the patent specification, much less disclaimed.

Third, Defendants again overplay their hand by stating that "applicants chose to use a variable speed oscillator – which varies and is 'determined by' PVT parameters – rather than the ***prior art's fixed speed clocks – which did not vary with the PVT parameters because their frequency was 'fixed' by an external crystal or control signal***." *Id.* at 14 (emphasis by Plaintiffs). Again, this statement is misleading as the prior art contemplated by the specification did not involve an on-chip oscillator "whose frequency was 'fixed' by an external crystal or control signal." In the prior art contemplated by the patent, an off-chip crystal oscillator was the oscillator that clocked the CPU. Because using a crystal oscillator to "control" a different, on-chip oscillator was not discussed or contemplated by the specification, there can certainly be no disclaimer of this scenario.

These erroneous statements by Defendants are not sufficient to meet the high bar required to show clear and unmistakable disclaimer, and the cases cited by Defendants involved far different factual scenarios. For example, in *Chicago Bd. Options Exch. Inc. v. Int'l Secs. Exch. LLC*, the court found that the specification "goes well beyond expressing the patentee's preference" and that the patentee's "***repeated derogatory statements*** … may be viewed as a disavowal of that subject matter from the scope of the Patent's claims." 677 F3d 1361, 1372 (Fed. Cir. 2012). By contrast, the '336 patent does not clearly and unambiguously criticize (much less "repeatedly criticize") use of "a control signal or an external crystal/clock generator to cause clock signal oscillation or control clock signal frequency." In fact, this situation is completely unaddressed in the passages cited by Defendants. And while the patent specification does distinguish the invention from prior art systems (like Magar) that used an external crystal to generate the signal used to clock the CPU, this type of system is specifically excluded by virtue of limitations already present in the claims (i.e., the on-chip and PVT variation limitations).

Finally, Defendants claim that the *title* of the patent controls how the Court should interpret the patent. Yet Defendants cite to no law for this proposition. Indeed they cannot – "[i]t is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the

patentee is entitled the right to exclude.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citations omitted). Here, the claims do not state that there can be no use of an external element such as an off-chip crystal as a reference for the clock. The claims only require that an entire oscillator be disposed on the same integrated circuit as the CPU and vary according to PVT factors. This is entirely consistent with the specification passages cited by Defendants, and there is no basis for finding disclaimer going beyond the limitations expressly present in the claims.

C. The Claim Language Speaks for Itself

Defendants next argue that the presence of other elements within the claim should dictate the meaning of the *entire oscillator* term. They argue that if an entire oscillator clocks a CPU at a clock rate which varies in the same way as a function of parameter variation in one or more fabrication or operation parameters associated with the integrated circuit substrate, it cannot use an external crystal or clock generator as a reference, because such reference would not permit the oscillator to vary.

As an initial matter, the argument is technically incorrect. Even if an external crystal is used to later adjust the output of an oscillator, the fact is that the frequency output by the oscillator itself does vary as a function of parameter variation. The addition of other elements, such as an external crystal, to an infringing entire oscillator, does not change the fundamental nature of the oscillator itself.

Further, the claim language speaks for itself. Whether an accused oscillator satisfies the "entire oscillator" element of the claim and also meets other claim limitations (such as the parameter variation requirements) is not an issue for claim construction, but instead a factual argument for trial. Importing the parameter variation requirements into the entire oscillator claim element is unnecessary, renders the parameter variation language redundant, and is not properly handled in the claim construction phase.

D. Defendants' Construction is Not Consistent with Prior Constructions

As explained in Plaintiffs' opening brief, adoption of the negative limitations proposed by Defendants would be a major departure from this Court's prior treatment of the *entire oscillator*

phrase.

In the HTC case, this Court issued a jury instruction that the entire oscillator "exclude any external clock used to generate a signal," but declined to add a restriction with respect to control of the oscillator. The most notable difference between the HTC jury instruction and Defendants' proposed construction is that the HTC jury instruction restricted the entire oscillator from relying on an external crystal/clock generator to ***generate*** the signal used to clock the CPU, whereas Defendants seek to broaden that limitation by virtue of language that the external crystal/clock generator may not ***cause*** clock signal oscillation ***or control clock signal frequency.***

These departures from prior constructions are not trivial. First, Defendants, attempt to broaden the concept of generation to one of causation ("to cause clock signal oscillation"). As explained in their opening brief, Plaintiffs respectfully submit that the concept of "causation" can be viewed as significantly broader and much more uncertain than the concept of "generating" the actual signal used to clock the CPU. As set forth above, the intrinsic record does not support a disclaimer relating to "causation." Indeed, the prosecution history indicates that if there was any disclaimer, it was the use of an external crystal to generate the actual signal used to clock the CPU (a situation that Plaintiffs respectfully submit is already excluded by the claim language). Notably, like the HTC jury instruction, both the Texas construction and the ITC construction also use the term "generate a [clock] signal." Neither construction uses "cause clock signal oscillation."

Additionally, Defendants' proposal that the entire oscillator cannot rely on an external clock to "control clock signal frequency" has been considered and rejected previously by this Court. Applicants did not make any clear and unmistakable disclaimer in this regard, and as such there is simply no basis for including this negative limitation in the entire oscillator construction. Doing so would improperly restrict the scope of the claims. Notably, neither the Texas construction nor the ITC construction includes a broad prohibition relating to "controlling clock signal frequency."

E. Plaintiffs' Construction is Correct

Defendants argue that Plaintiffs' construction cannot be correct because it is too broad and covers prior art systems. They also contend that Plaintiffs surrendered claim scope when distinguishing over Magar and Sheets. These arguments lack merit.

First, Defendants' argument that Plaintiffs' "entire oscillator" construction covers prior art systems that allegedly disclosed an on-chip oscillator. Assuming arguendo that this is true, Defendants' argument obviously ignores the many other claim limitations that must be considered when assessing the scope of the claim. It is simply nonsense to cherry pick the claim term at issue and argue that its construction must be narrower by viewing the claim term in a vacuum and divorced from the claim as a whole. Using Defendants' logic, a construction of CPU would necessarily need to be narrower than what the parties agreed to because there were CPUs disclosed in the prior art. This approach makes little sense.

Second, Defendants' argument that Plaintiffs' construction cannot be correct because "the intrinsic evidence leaves no doubt that the applicants surrendered far more during prosecution to secure allowance of the '336 patent" simply misstates what actually happened during prosecution. As set forth above, Magar and Sheets were distinguished based on the "on-chip" claim requirement and the PVT variation requirement, which are express limitations in the asserted claims.

Finally, it cannot be overlooked that Plaintiffs' construction is included within Defendants' construction. There is no dispute that it is correct. The only question is whether Defendants have met their heavy burden of disclaimer. As set forth above, they have not.

III. CONCLUSION

For the foregoing reasons, Plaintiffs respectfully request that the court adopt their proposed construction.

Dated: August 18, 2015

Respectfully submitted,

/s/ Barry J. Bumgardner

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CERTIFICATE OF SERVICE

I hereby certify that, on August 18, 2015, I caused the foregoing document to be served on counsel of record via the Court's CM/ECF system.

Dated: August 18, 2015

By: */s/ Barry J. Bumgardner*
Barry J. Bumgardner

Exhibit “F”

(*Counsel listed on signature page*)

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. ZTE CORPORATION, et al., Defendants.	Case No. 3:12-cv-03876-VC (PSG) **JOINT MOTION TO STAY ALL PROCEEDINGS AND DEADLINES PENDING RESOLUTION OF OBJECTIONS TO CLAIM CONSTRUCTION REPORT AND RECOMMENDATION**
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. SAMSUNG ELECTRONICS CO., LTD., et al., Defendants.	Case No. 3:12-cv-03877-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. LG ELECTRONICS, INC., et al., Defendants.	Case No. 3:12-cv-03880-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. NINTENDO CO., LTD, et al. Defendants.	Case No. 3:12-cv-03881-VC (PSG)

Plaintiffs Technology Properties Limited LLC, Phoenix Digital Solutions LLC, and Patriot Scientific Corporation's (collectively, "Plaintiffs") and Defendants ZTE Corporation, ZTE (USA) Inc., Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., LG Electronics, Inc., LG Electronics U.S.A., Inc., Nintendo Co., Ltd., and Nintendo of America Inc. ("Defendants") (collectively, the "Parties") in the above-titled and numbered civil cases (collectively, "this Action"), respectfully move the Court to stay all deadlines and proceedings in this Action, except for the deadline for Plaintiffs to file their objections to the recently issued Claim Construction Report and Recommendation (or otherwise seek to alter the findings in Claim Construction Report and Recommendation). In support of the requested stay, the parties would show the Court:

1. Magistrate Grewal's Claim Construction Report and Recommendation (Dkt. Nos. (109) in case 3:12-cv-03876-VC, (104) in case 3:12-cv-03877-VC, (117) in case 3:12-cv-03880-VC, (106) in case 3:12-cv-03881-VC) issued September 22, 2015 (the "Claim Construction Report").

2. The Claim Construction Report construed the term "an entire oscillator disposed

upon said integrated circuit substrate" as "an [oscillator] located entirely on the same semiconductor substrate as the [central processing unit] that does not require a control signal and whose frequency is not fixed by any external crystal" (the "Entire Oscillator Construction").

3. Any objections to the Claim Construction Report are due October 6, 2015.

4. The parties hereby stipulate that all accused products of all Defendants in this Action do not infringe the asserted claims of U.S. Patent 5,809,336 under the Entire Oscillator Construction.

5. If Plaintiffs do not file an objection to the Claim Construction Report on or before October 6, 2015, or, if Plaintiffs timely file an objection to the Claim Construction Report and the Court does not reject or materially modify the construction of the term "an entire oscillator disposed upon said integrated circuit substrate", and thereby accepts the Entire Oscillator Construction, the Parties will within, three (3) business days of (a) Plaintiffs' failure to timely file an objection (*i.e.*, October 9, 2015) or (b) the Court's acceptance of the Entire Oscillator Construction, request the Court to enter final judgment of non-infringement in favor of Defendants in the form attached hereto as Exhibit A.

6. Close of fact discovery is currently set for October 8, 2015. Parties with the burden of proof are currently set to serve initial expert reports on November 6, 2015.

7. The parties have agreed to stay all proceedings and deadlines in this Action pending the Court's ruling on any objections to the Claim Construction Report.

8. A stay will prevent the time and resources of both the Court and the parties from being wasted should the Court overrule Plaintiffs' objections to the Claim Construction Report.

9. If the Court sustains Plaintiffs' objections and reconsiders the construction of the term "an entire oscillator disposed upon said integrated circuit substrate," the parties will jointly propose a revised scheduling order for the Court's consideration.

10. To be clear, this stipulation does not prevent any Defendant from filing objections to the Claim Construction Report, and no Defendant is required to file objections to the Claim Construction Report in order to preserve its appellate rights.

Therefore, the parties request that the Court grant this Motion, and enter an Order staying further proceedings and upcoming deadlines in this Action, except for the deadline for Plaintiffs to file their objections to the Claim Construction Report, until further order of the Court.

IT IS SO STIPULATED.

Dated: September 25, 2015

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ATTESTATION

I, Aaron Wainscoat, am the ECF User whose ID and password are being used to file this JOINT MOTION TO STAY ALL PROCEEDINGS AND DEADLINES PENDING RESOLUTION OF OBJECTIONS TO CLAIM CONSTRUCTION REPORT AND RECOMMENDATION. In compliance with Civil Local Rule 5-1(i)(3), I hereby attest that the signatories listed above have read and approved the filing of this brief.

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Exhibit “G”

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

TECHNOLOGY PROPERTIES LIMITED LLC, et al.,

Plaintiffs,

v.

HUAWEI TECHNOLOGIES CO., LTD., et al.,

Defendants.

Case No. 3:12-cv-03865-VC

ORDER GRANTING STAY

Plaintiffs ask the court to stay all deadlines and proceedings in this case[1] other than the deadline for Plaintiffs to seek relief and file objections to the undersigned's Claim Construction Report and Recommendation.[2] In light of that report, Plaintiffs offered Defendants in this and the related actions[3] a stipulation to a judgment of non-infringement should Judge Chhabria adopt the recommended construction of "an entire oscillator disposed upon said integrated circuit substrate" in U.S. Patent 5,809,336.[4]

[1] *See* Docket No. 100.

[2] *See* Docket No. 98.

[3] *See Technology Properties Limited, LLC et al. v. ZTE Corporation et al.*, Case No. 3:12-cv-03876-VC; *Technology Properties Limited LLC et al.v. Nintendo Co., Ltd et al.*, Case No. 3:12-cv-03881-VC; *Technology Properties Limited LLC et al.v. LG Electroncis, Inc. et al.*, Case No. 3:12-cv-03880-VC; *Technology Properties Limited LLC et al.v. Samsung Electronic Co., LTD et al.*, Case No. 3:12-cv-03877-VC.

[4] *See* Docket No. 100 at 1.

The other Defendants accepted the offer and agreed to stay;[5] Defendants here declined.[6] They say they have a right to pursue their claim that the '336 patent is invalid, and that a stay would unfairly delay their right to a ruling.[7]

With full appreciation of Defendants' interest in finally getting a resolution of a dispute between the parties that began in 2006, on balance a stay is warranted. With the related cases stayed, there is little or no reason to proceed here in a piecemeal fashion. As the court explained before, the primary goal of the referral to the undersigned is give the presiding judge a single package of items for final resolution if necessary. That goal is undermined by anything less than a complete stay.

Plaintiffs' motion is GRANTED.

SO ORDERED.

Dated: October 2, 2015

PAUL S. GREWAL
United States Magistrate Judge

[5] *See Technology Properties Limited, LLC et al. v. ZTE Corporation et al.*, Case No. 3:12-cv-03876-VC at Docket No. 111; *Technology Properties Limited LLC et al.v. Nintendo Co., Ltd et al.*, Case No. 3:12-cv-03881-VC at Docket No. 108; *Technology Properties Limited LLC et al.v. LG Electroncis, Inc. et al.*, Case No. 3:12-cv-03880-VC at Docket No. 119; *Technology Properties Limited LLC et al.v. Samsung Electronic Co., LTD et al.*, Case No. 3:12-cv-03877-VC at Docket No. 106.

[6] *See* Docket No. 100 at 1.

[7] *See* Docket No. 103 at 1.

Exhibit “H”

US005809336A

United States Patent [19]

Moore et al.

[11] **Patent Number: 5,809,336**

[45] **Date of Patent: Sep. 15, 1998**

[54] **HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK**

[75] Inventors: **Charles H. Moore**, Woodside; **Russell H. Fish, III**, Mt. View, both of Calif.

[73] Assignee: **Patriot Scientific Corporation**, San Diego, Calif.

[21] Appl. No.: **484,918**

[22] Filed: **Jun. 7, 1995**

Related U.S. Application Data

[62] Division of Ser. No. 389,334, Aug. 3, 1989, Pat. No. 5,440,749.

[51] **Int. Cl.**[6] **G06F 1/04**

[52] **U.S. Cl.** **395/845**

[58] **Field of Search** 395/500, 551, 395/555, 845

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,967,104	6/1976	Brantingham	364/709.09
3,980,993	9/1976	Bredart et al.	395/550
4,003,028	1/1977	Bennett et al.	395/742
4,042,972	8/1977	Gruner et al.	395/389
4,050,096	9/1977	Bennett	395/494
4,112,490	9/1978	Pohlman et al.	395/287
4,315,308	2/1982	Jackson	395/853
4,338,675	7/1982	Palmer	364/748
4,398,265	8/1983	Puhl et al.	395/882
4,453,229	6/1984	Schaire	395/250
4,503,500	3/1985	Magan	395/800
4,539,655	9/1985	Trussell et al.	395/280
4,553,201	11/1985	Pollack	395/183.22
4,627,082	12/1986	Pelgrom et al.	377/63
4,670,837	6/1987	Sheets	395/550
4,680,698	7/1987	Edwards et al.	395/800
4,761,763	8/1988	Hicks	395/286
5,414,862	5/1995	Suzuki et al.	395/750

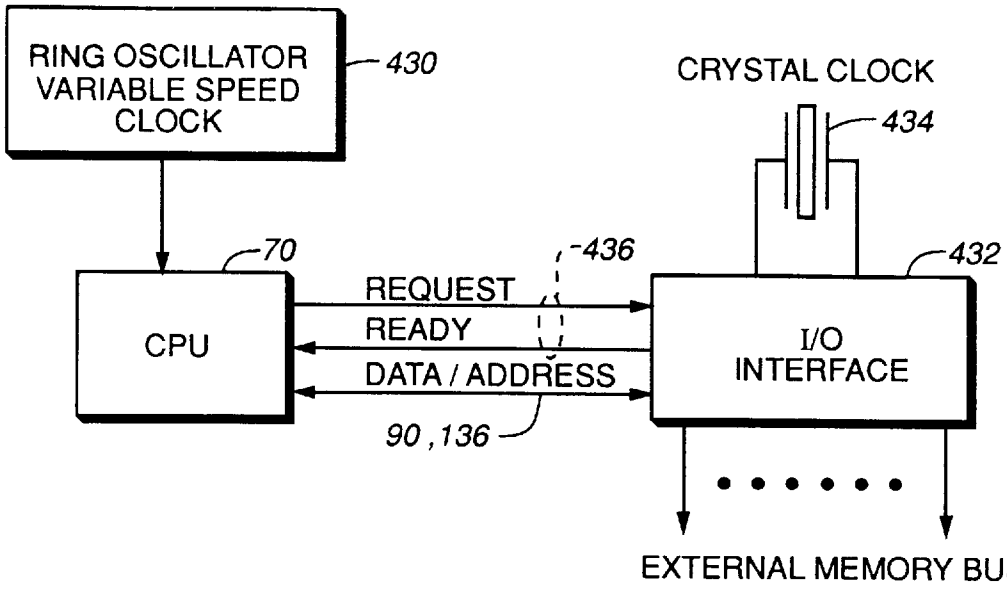
Primary Examiner—David Y. Eng

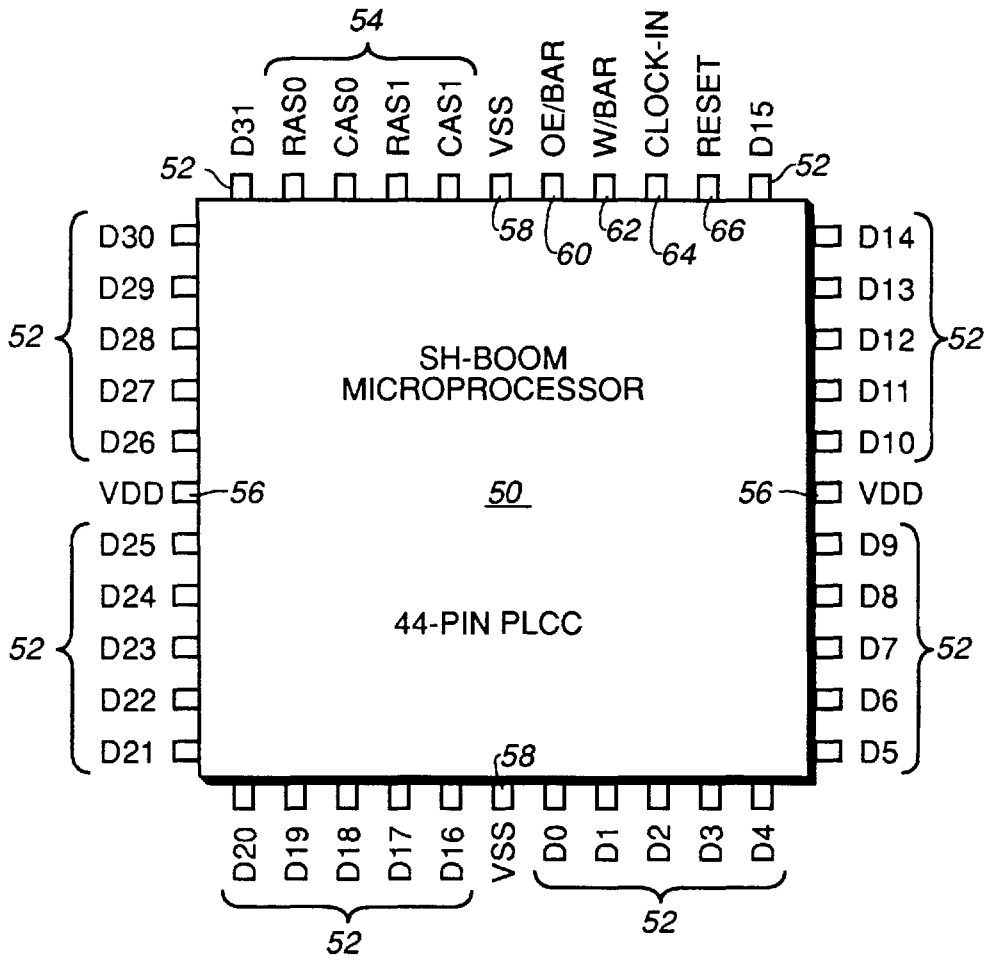
Attorney, Agent, or Firm—Cooley Godward LLP

[57] **ABSTRACT**

A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.

10 Claims, 19 Drawing Sheets

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CAS0
RAS1
CAS1
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OE/BAR
W/BAR
CLOCK-IN
RESET
D15
52
58
60
62
64
66
D30
D29
D28
D27
D26
VDD
56
SH-BOOM
MICROPROCESSOR
50
44-PIN PLCC
D14
D13
D12
D11
D10
D25
D24
D23
D22
D21
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D16
D0
D1
D2
D3
D4

FIG._1

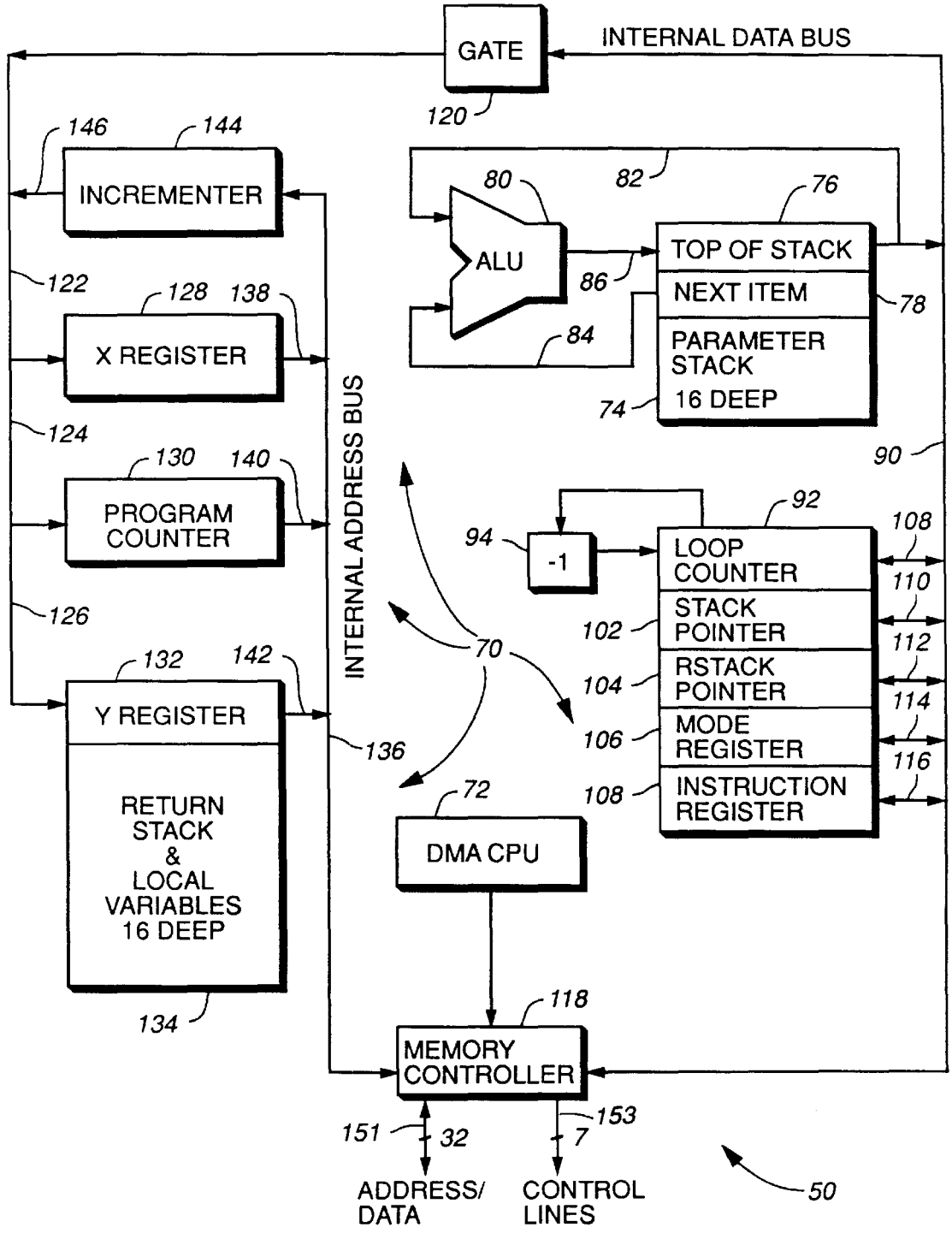
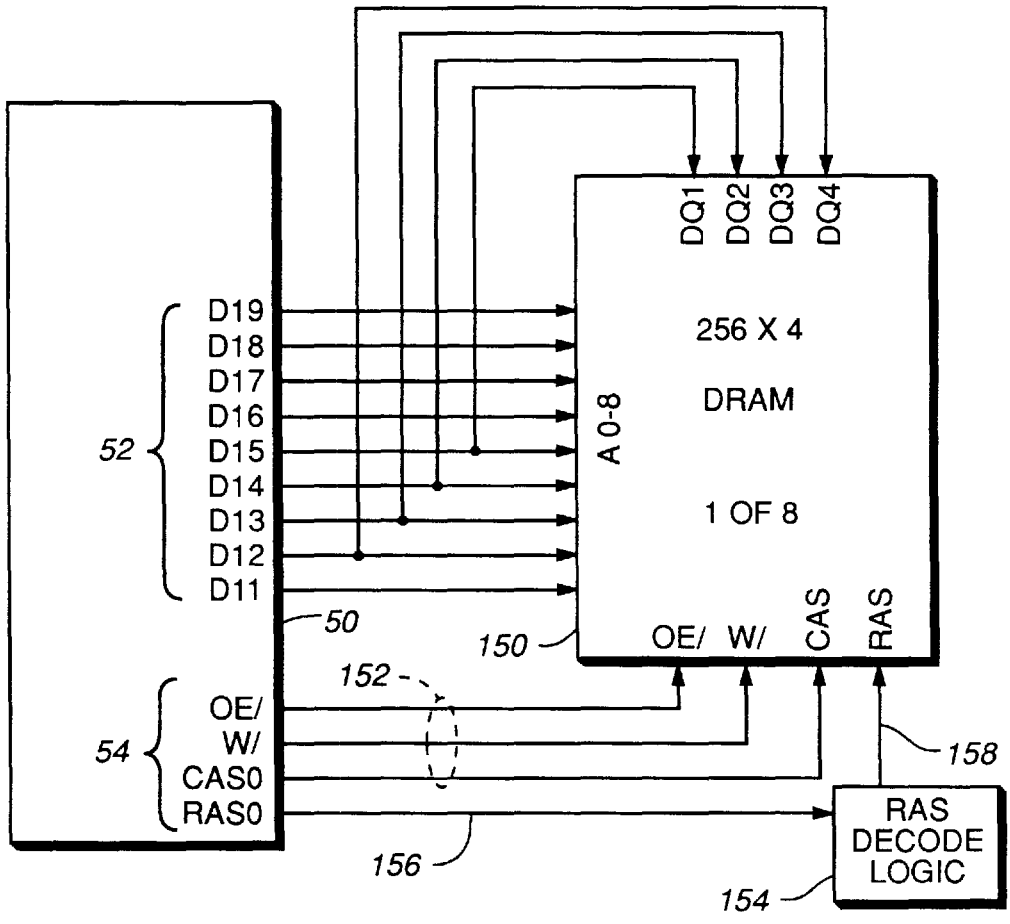

GATE
INTERNAL DATA BUS
120
146
144
INCREMENTER
80
82
76
ALU
TOP OF STACK
NEXT ITEM
PARAMETER STACK
16 DEEP
86
84
78
74
122
128
138
X REGISTER
124
130
140
PROGRAM COUNTER
126
INTERNAL ADDRESS BUS
90
92
94
-1
LOOP COUNTER
STACK POINTER
RSTACK POINTER
MODE REGISTER
INSTRUCTION REGISTER
108
110
112
114
116
102
104
106
108
70
132
142
Y REGISTER
RETURN STACK & LOCAL VARIABLES 16 DEEP
136
134
72
DMA CPU
118
MEMORY CONTROLLER
151
32
153
7
ADDRESS/ DATA
CONTROL LINES
50

FIG._2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DQ2
DQ3
DQ4
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A 0-8
OE/
W/
CAS
RAS
D19
D18
D17
D16
D15
D14
D13
D12
D11
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152
OE/
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156
158
RAS
DECODE
LOGIC
154

FIG._3

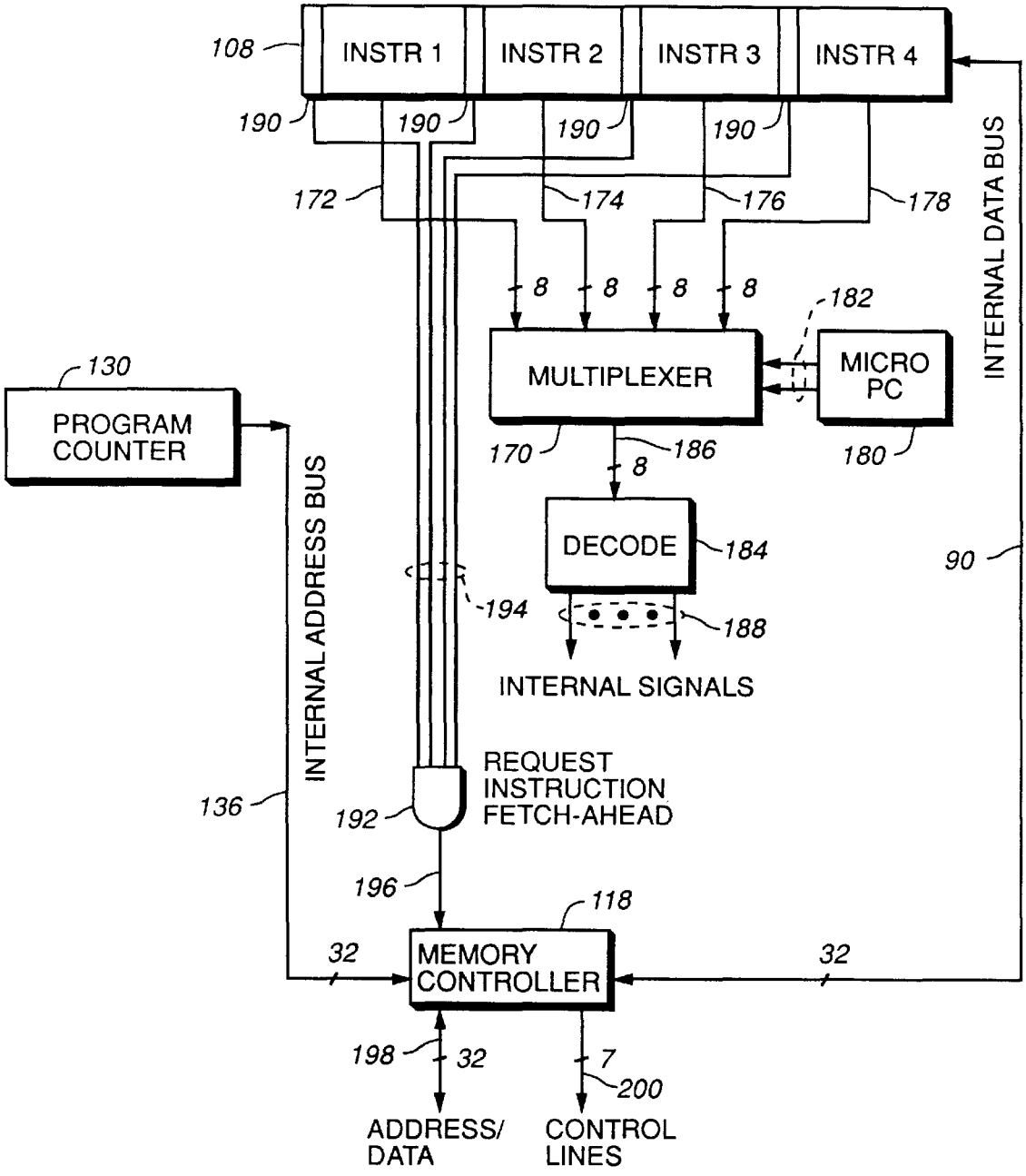
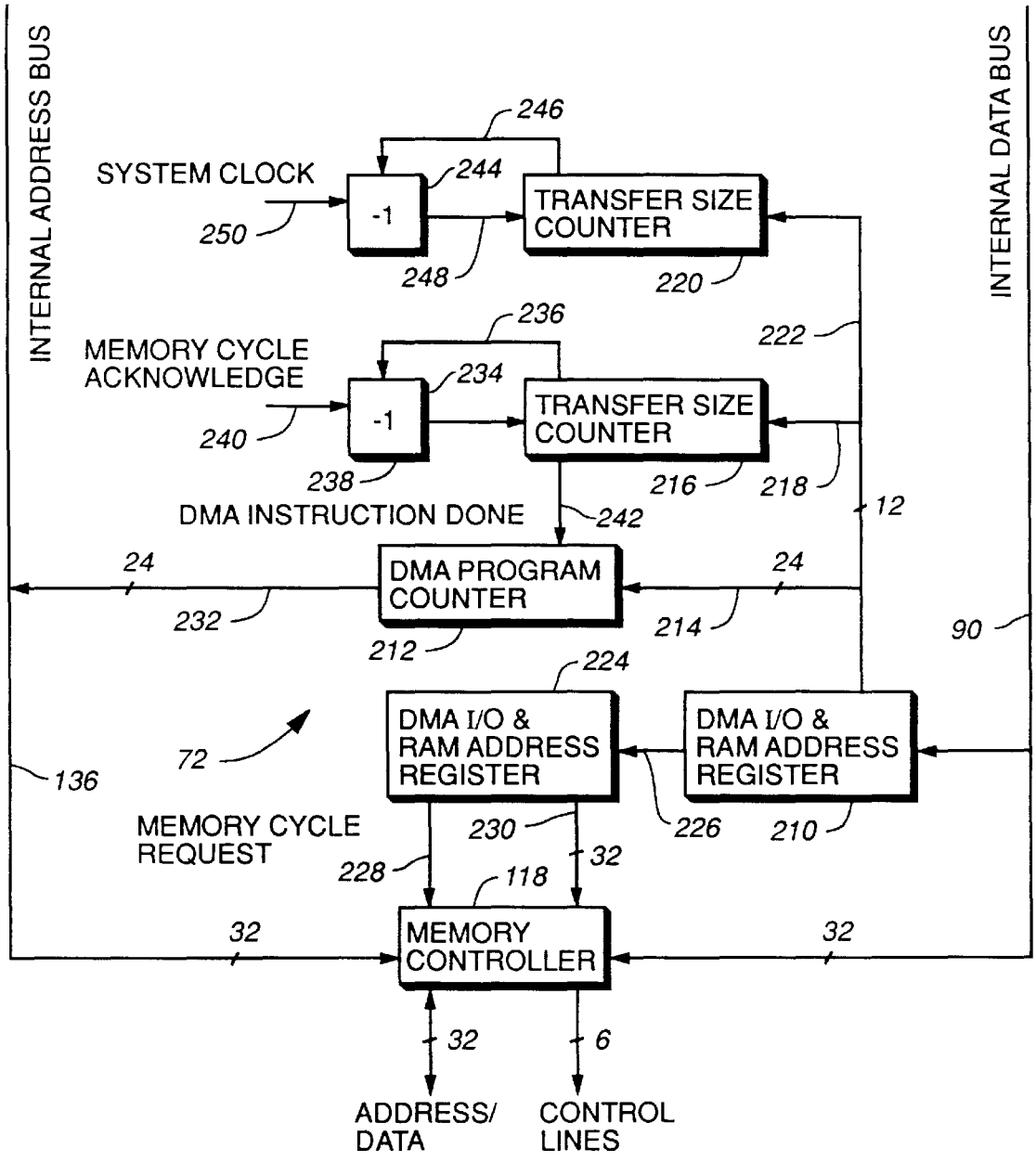

108
INSTR 1
INSTR 2
INSTR 3
INSTR 4
190
190
190
190
172
174
176
178
8
8
8
8
182
MULTIPLEXER
MICRO PC
180
170
186
8
130
PROGRAM COUNTER
DECODE
184
194
188
INTERNAL SIGNALS
INTERNAL ADDRESS BUS
INTERNAL DATA BUS
90
136
192
REQUEST INSTRUCTION FETCH-AHEAD
196
118
32
MEMORY CONTROLLER
32
198
32
7
200
ADDRESS/ DATA
CONTROL LINES

FIG._4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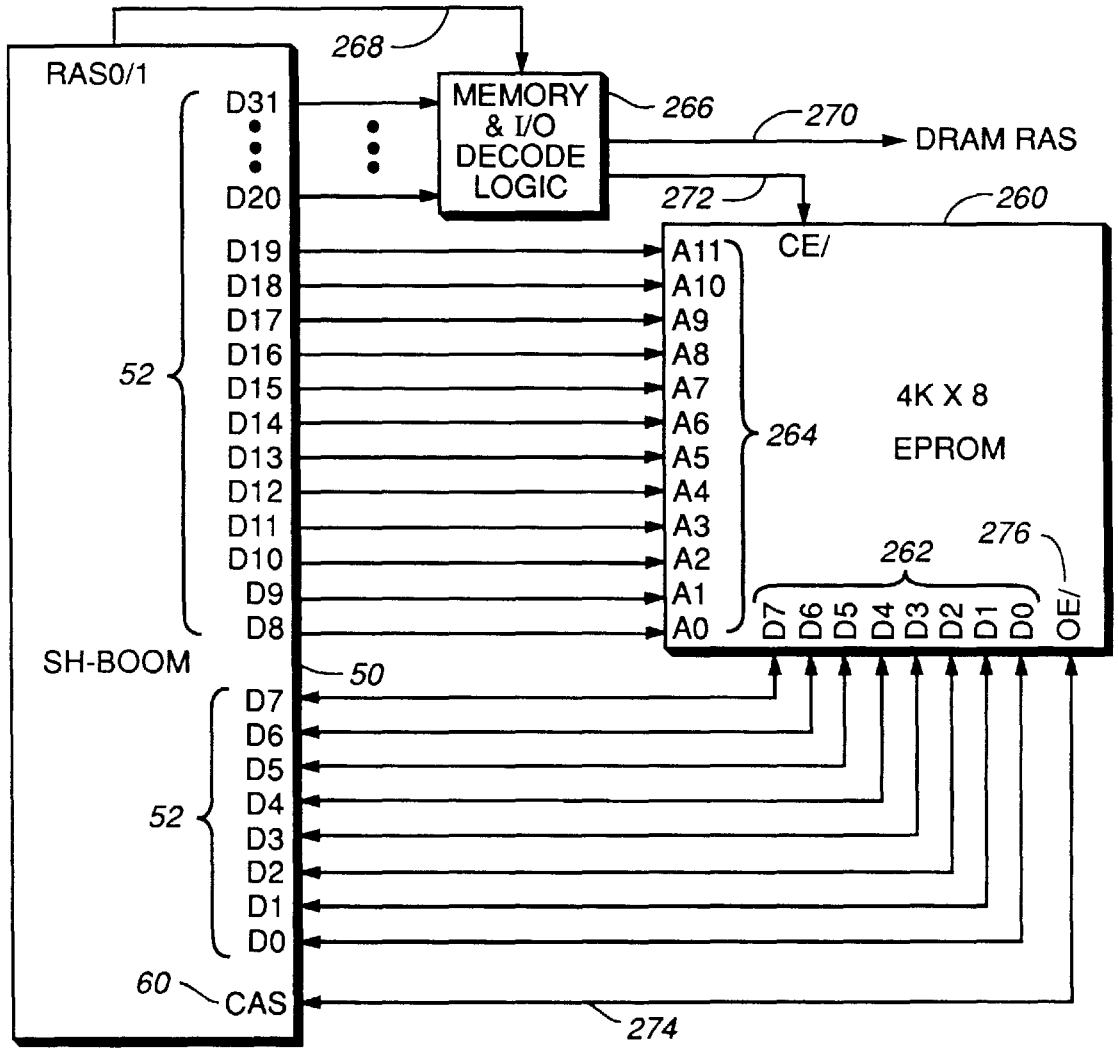
INTERNAL DATA BUS
SYSTEM CLOCK
250
-1
244
246
248
TRANSFER SIZE COUNTER
220
222
MEMORY CYCLE ACKNOWLEDGE
240
-1
234
236
238
TRANSFER SIZE COUNTER
216
218
12
DMA INSTRUCTION DONE
242
24
DMA PROGRAM COUNTER
24
232
212
214
90
224
DMA I/O & RAM ADDRESS REGISTER
DMA I/O & RAM ADDRESS REGISTER
72
136
MEMORY CYCLE REQUEST
230
226
210
228
32
118
32
MEMORY CONTROLLER
32
32
6
ADDRESS/ DATA
CONTROL LINES

FIG._5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RAS0/1
D31
D20
MEMORY & I/O DECODE LOGIC
266
270
DRAM RAS
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CE/
D19
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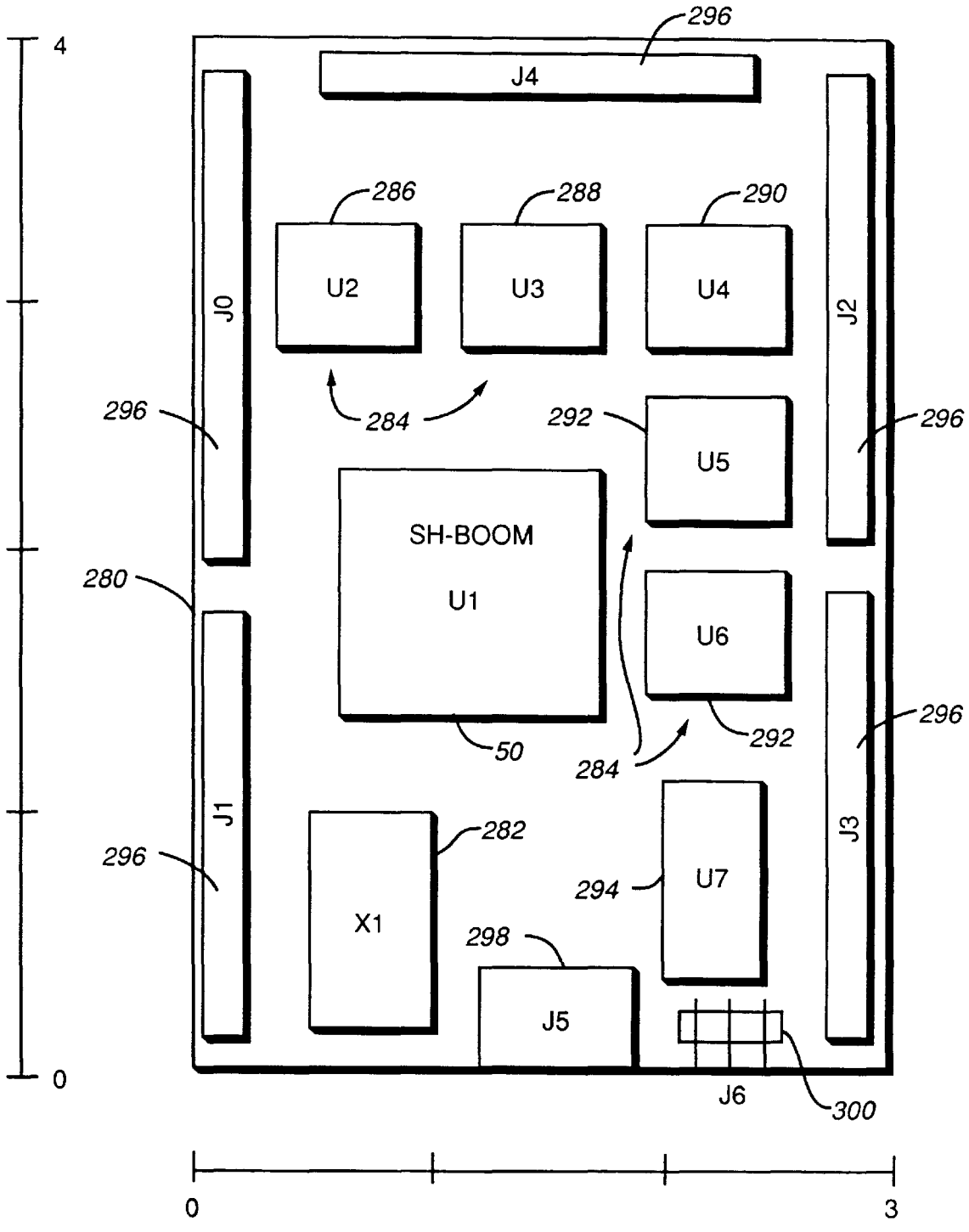
D17
D16
D15
D14
D13
D12
D11
D10
D9
D8
52
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
264
4K X 8
EPROM
262
276
D7
D6
D5
D4
D3
D2
D1
D0
OE/
SH-BOOM
50
52
60
CAS
274

FIG._6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J4
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288
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U2
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296
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SH-BOOM
U1
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U6
296
50
284
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U7
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J6
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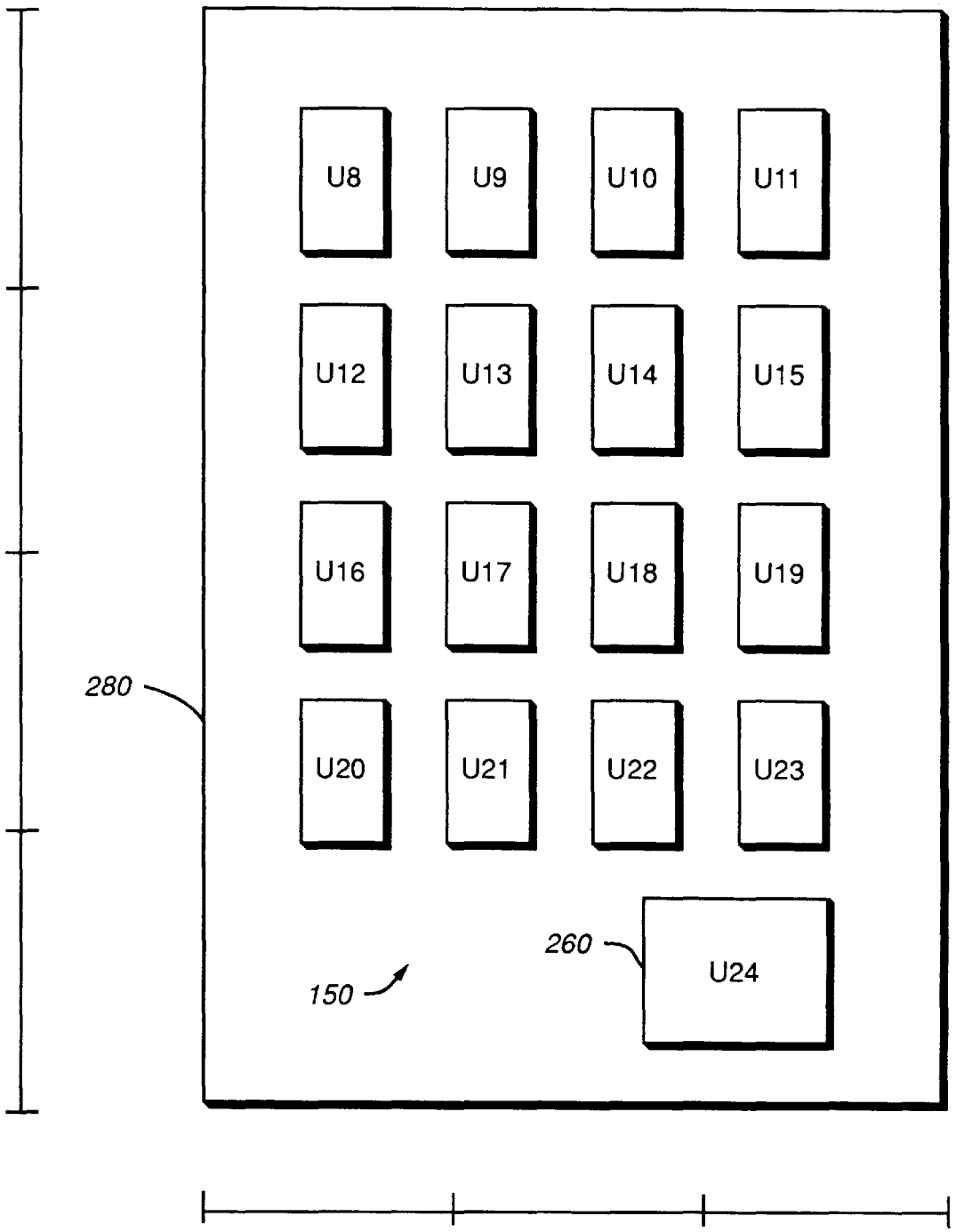
FIG._7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U12
U13
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U20
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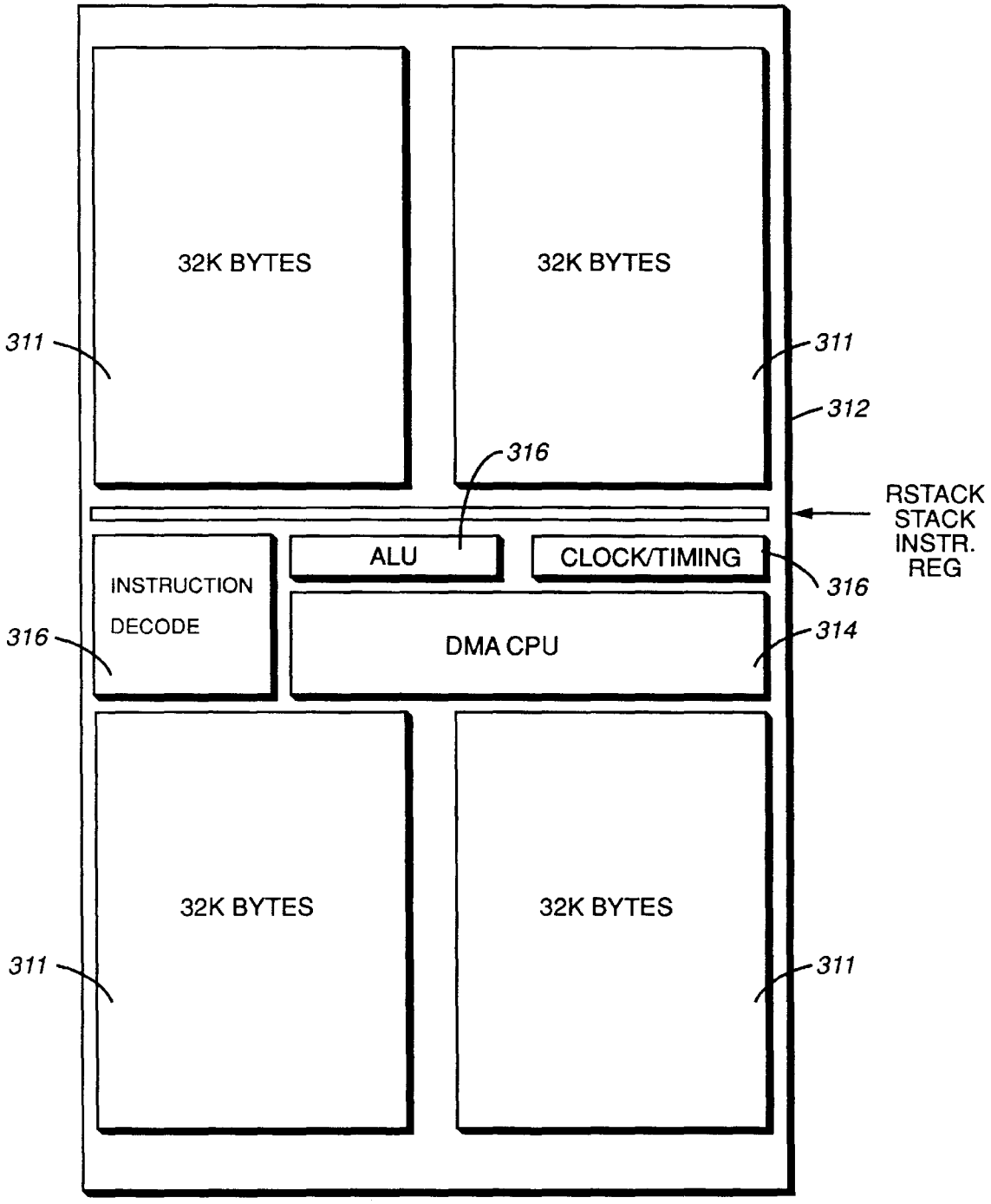
U23
U24
280
260
150

FIG._8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INSTR.
REG
ALU
CLOCK/TIMING
316
INSTRUCTION
DECODE
316
DMA CPU
314
32K BYTES
32K BYTES
311
311

FIG._9

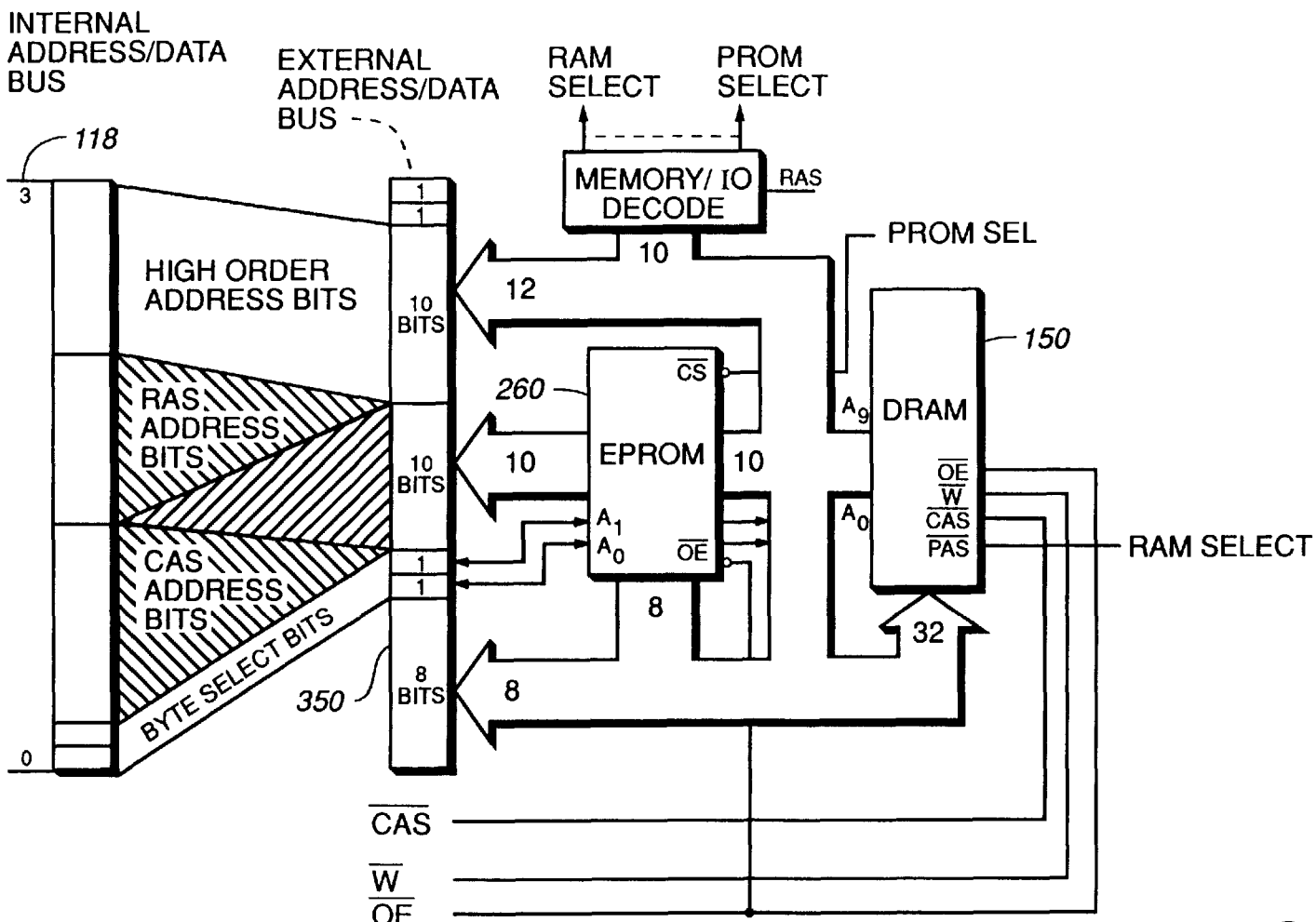
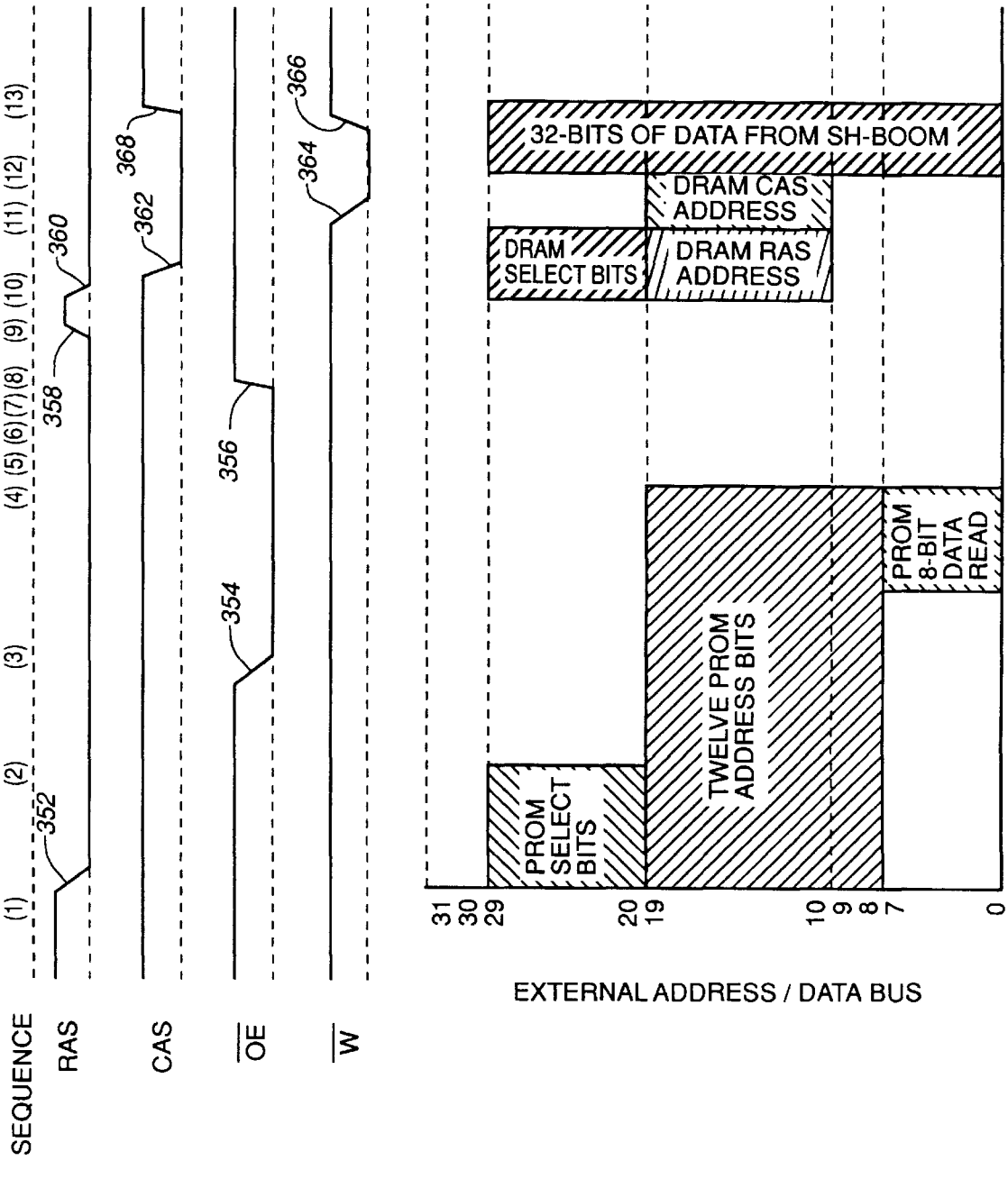

INTERNAL ADDRESS/DATA BUS
EXTERNAL ADDRESS/DATA BUS
RAM SELECT
PROM SELECT
118
3
0
HIGH ORDER ADDRESS BITS
RAS ADDRESS BITS
CAS ADDRESS BITS
BYTE SELECT BITS
10 BITS
10 BITS
8 BITS
350
MEMORY/ IO DECODE
RAS
10
12
PROM SEL
260
CS
EPROM
10
10
A1
A0
OE
8
8
150
A9
DRAM
A0
OE
W
CAS
PAS
RAM SELECT
32
CAS
W
OE

FIG._10

FIG._11


SEQUENCE
RAS
CAS
OE
W
(1)
(2)
(3)
(4) (5) (6) (7) (8)
(9) (10)
(11) (12)
(13)
352
354
356
358
360
362
364
366
368
32-BITS OF DATA FROM SH-BOOM
DRAM CAS ADDRESS
DRAM SELECT BITS
DRAM RAS ADDRESS
PROM SELECT BITS
TWELVE PROM ADDRESS BITS
PROM 8-BIT DATA READ
31 30 29
20 19
10 9 8 7
0
EXTERNAL ADDRESS / DATA BUS

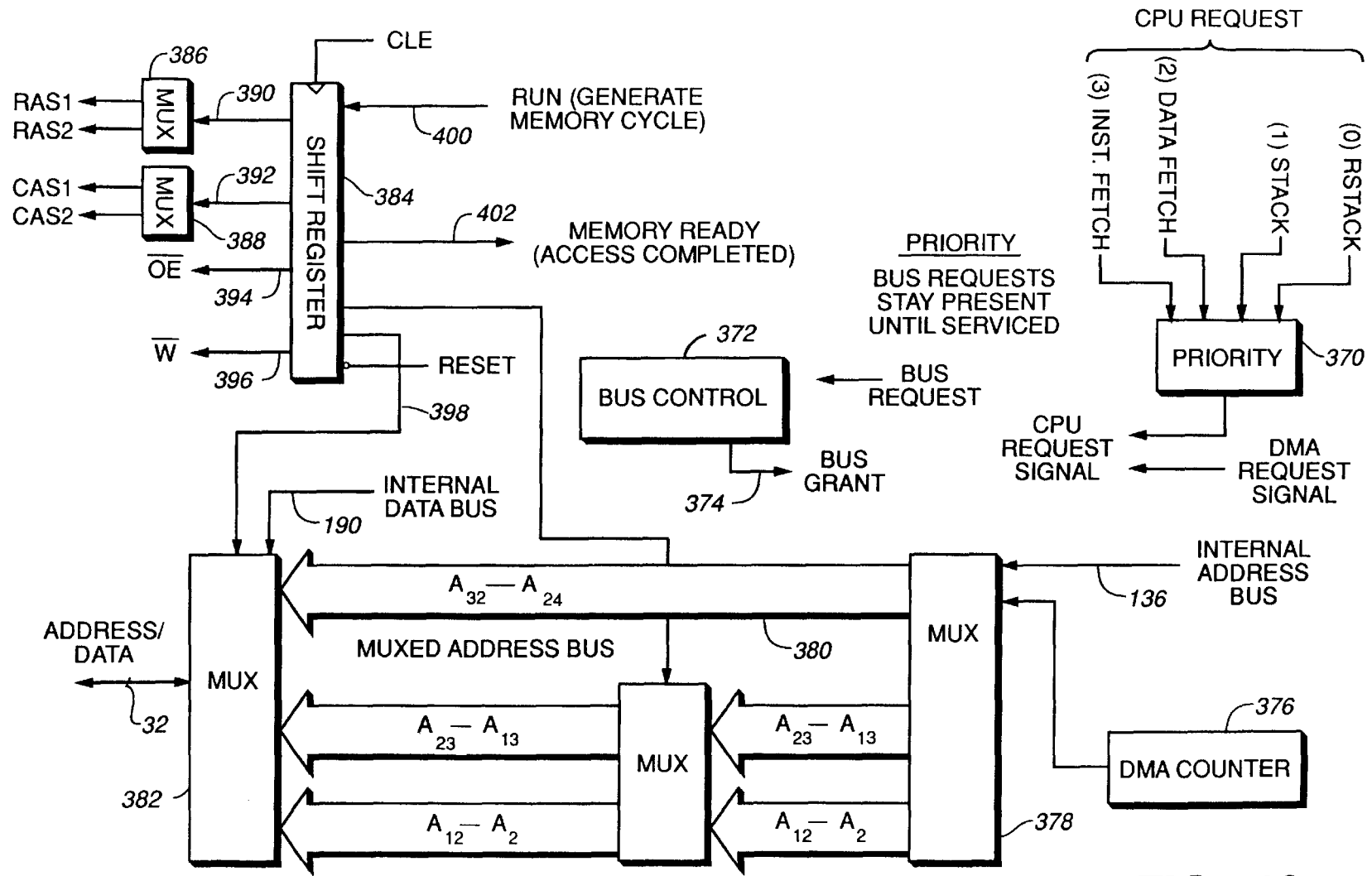

CPU REQUEST
(3) INST. FETCH
(2) DATA FETCH
(1) STACK
(0) RSTACK
PRIORITY
BUS REQUESTS STAY PRESENT UNTIL SERVICED
PRIORITY
370
CLE
386
RAS1
RAS2
MUX
390
SHIFT REGISTER
RUN (GENERATE MEMORY CYCLE)
400
CAS1
CAS2
MUX
392
384
388
402
MEMORY READY (ACCESS COMPLETED)
OE
394
W
396
RESET
398
372
BUS CONTROL
BUS REQUEST
BUS GRANT
374
CPU REQUEST SIGNAL
DMA REQUEST SIGNAL
INTERNAL DATA BUS
190
INTERNAL ADDRESS BUS
136
A32 — A24
MUXED ADDRESS BUS
380
ADDRESS/ DATA
32
MUX
MUX
MUX
A23 — A13
A23 — A13
A12 — A2
A12 — A2
376
DMA COUNTER
382
378

FIG._12

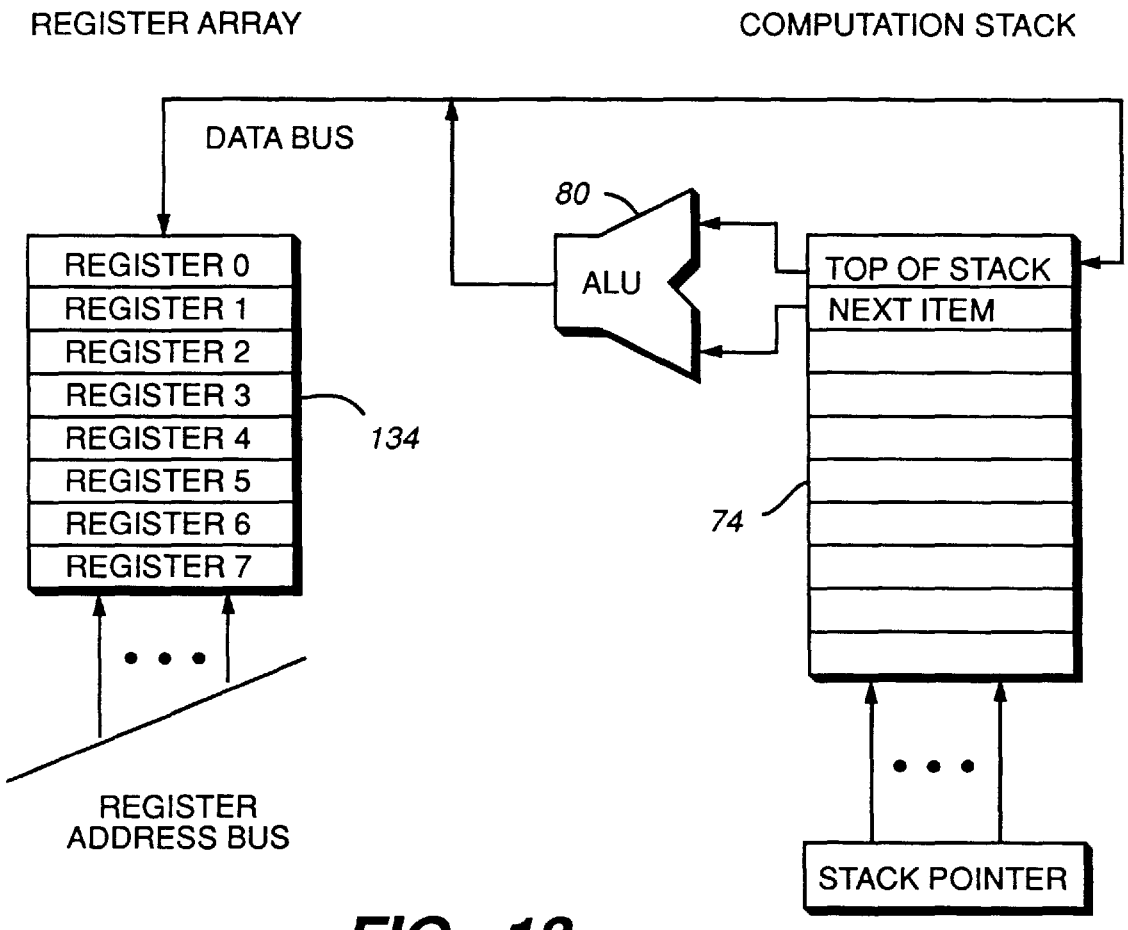

REGISTER ARRAY
COMPUTATION STACK
DATA BUS
80
ALU
REGISTER 0
REGISTER 1
REGISTER 2
REGISTER 3
REGISTER 4
REGISTER 5
REGISTER 6
REGISTER 7
134
TOP OF STACK
NEXT ITEM
74
REGISTER
ADDRESS BUS
STACK POINTER

FIG._13

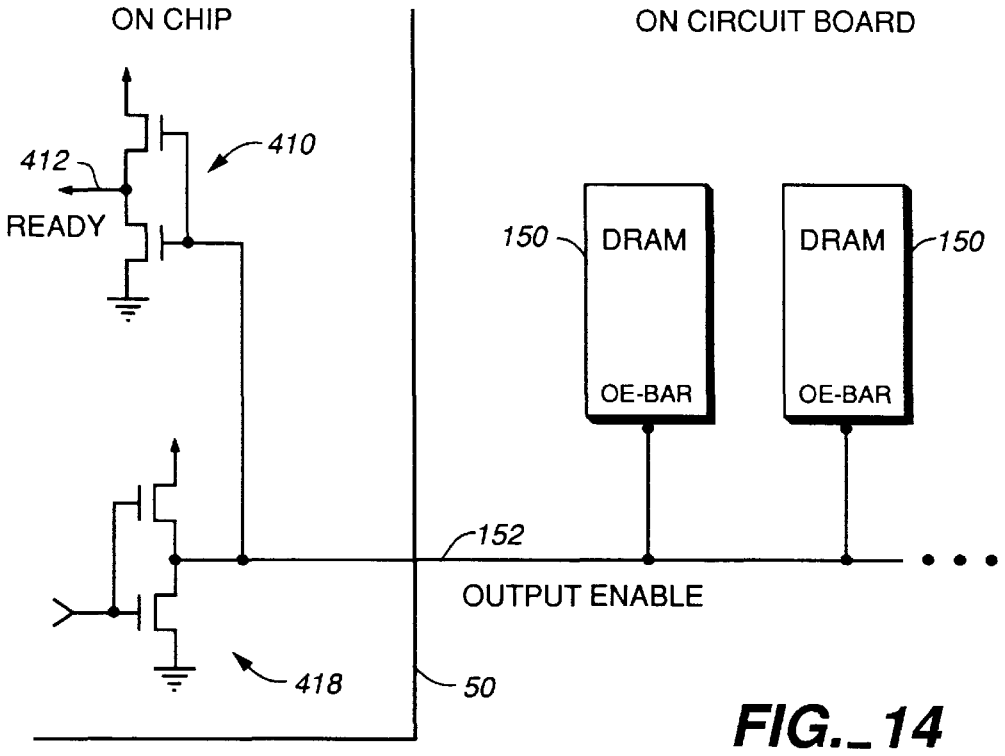

ON CHIP
ON CIRCUIT BOARD
412
410
READY
150
DRAM
OE-BAR
DRAM
150
OE-BAR
152
OUTPUT ENABLE
418
50

FIG._14

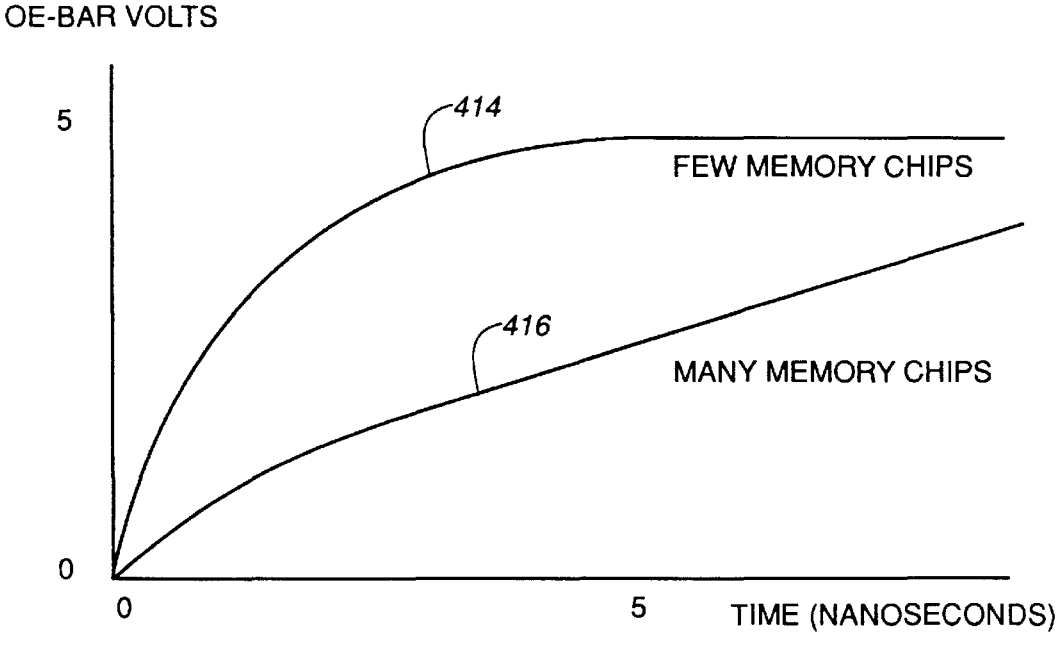

OE-BAR VOLTS
5
0
414
FEW MEMORY CHIPS
416
MANY MEMORY CHIPS
0
5
TIME (NANOSECONDS)

FIG._15

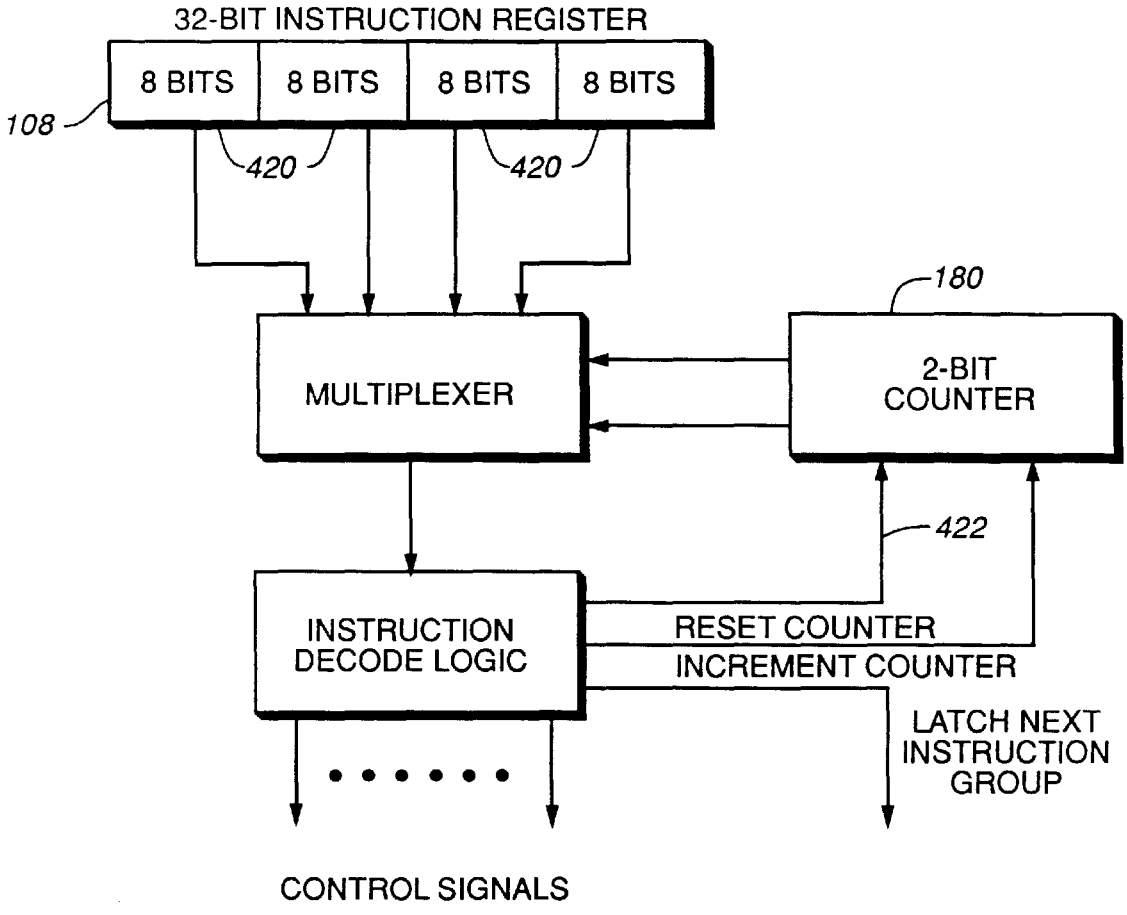

32-BIT INSTRUCTION REGISTER
8 BITS
8 BITS
8 BITS
8 BITS
108
420
420
180
MULTIPLEXER
2-BIT COUNTER
422
INSTRUCTION DECODE LOGIC
RESET COUNTER
INCREMENT COUNTER
LATCH NEXT INSTRUCTION GROUP
CONTROL SIGNALS

FIG._16

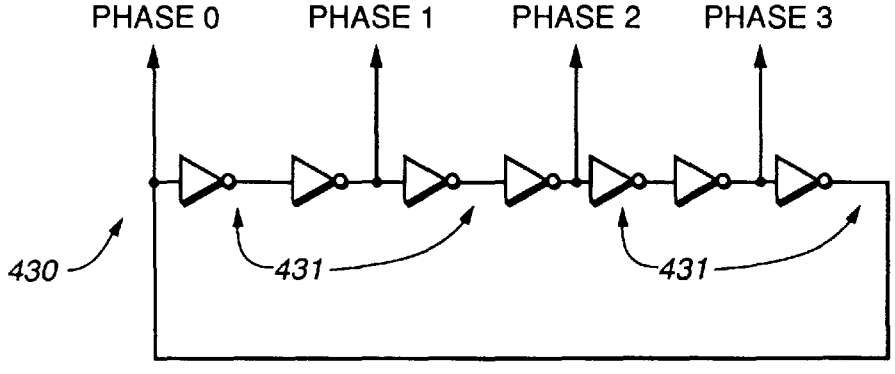

PHASE 0
PHASE 1
PHASE 2
PHASE 3
430
431
431

FIG._18

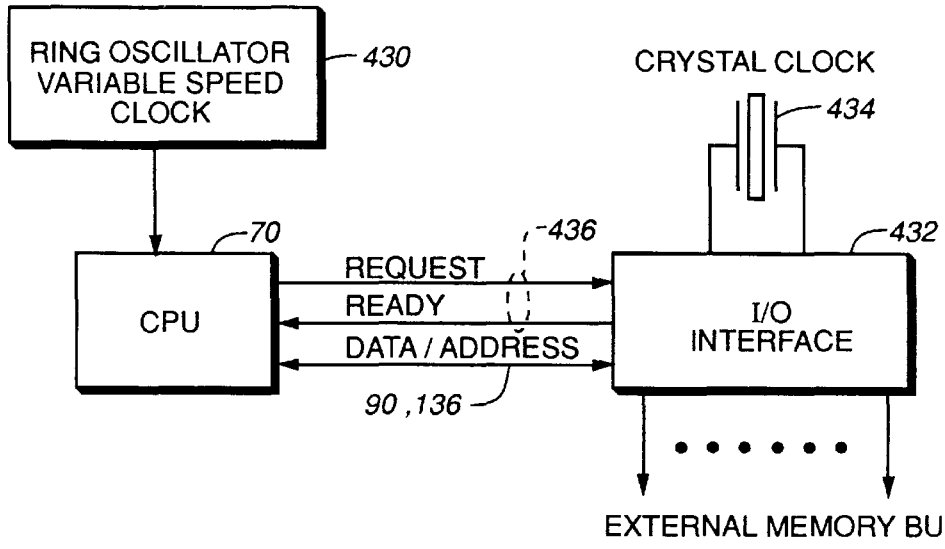

RING OSCILLATOR
VARIABLE SPEED
CLOCK
430
CRYSTAL CLOCK
434
70
436
432
CPU
REQUEST
READY
DATA / ADDRESS
I/O
INTERFACE
90 ,136
EXTERNAL MEMORY BUS

FIG._17

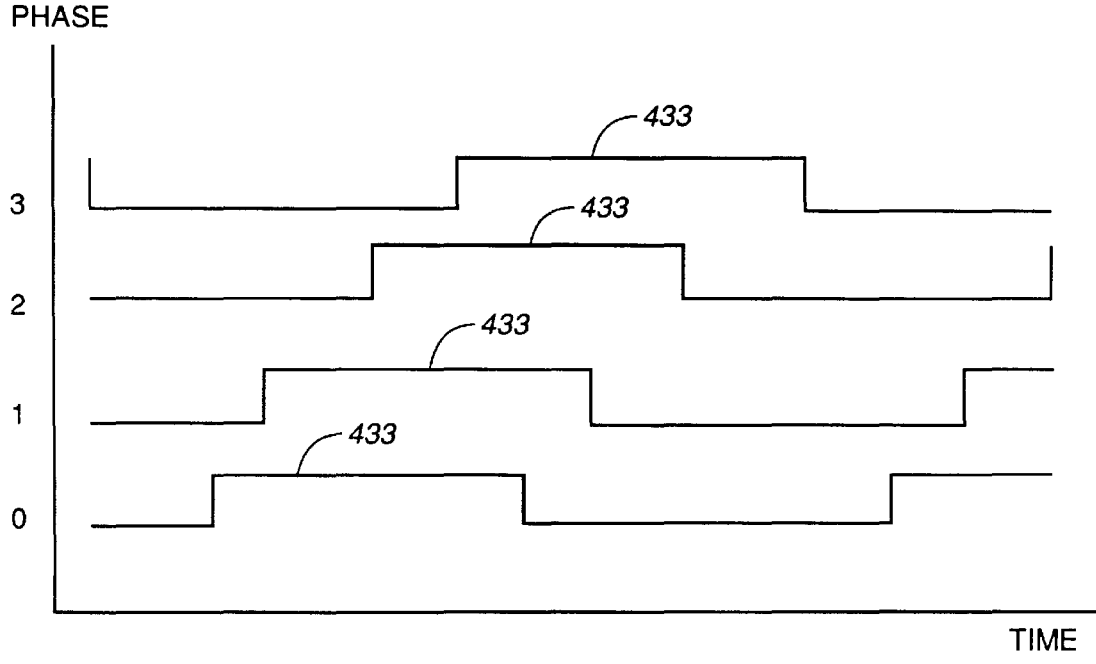

PHASE
3
2
1
0
433
433
433
433
TIME

FIG._19

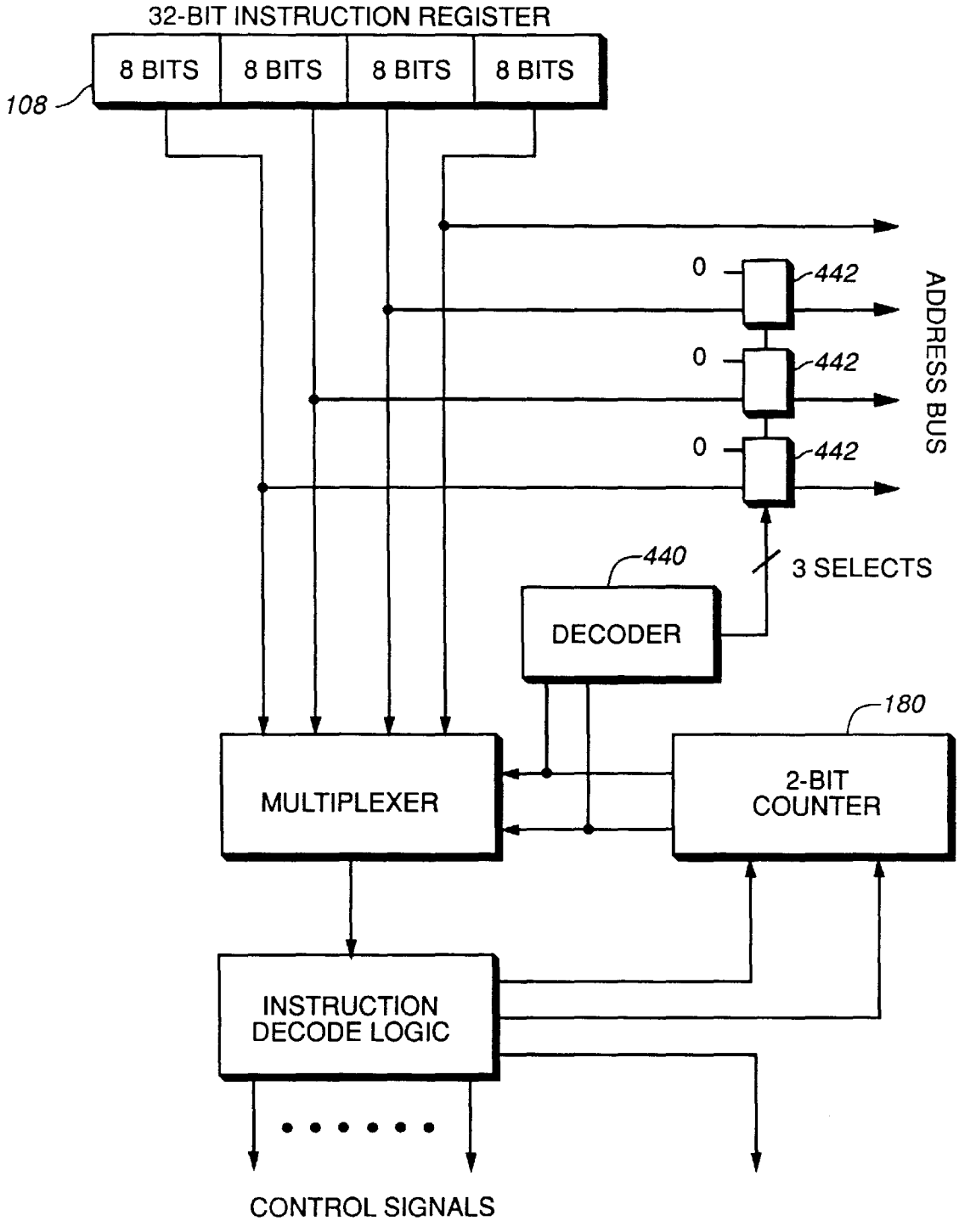

32-BIT INSTRUCTION REGISTER
8 BITS
8 BITS
8 BITS
8 BITS
108
0
442
0
442
0
442
ADDRESS BUS
440
3 SELECTS
DECODER
180
MULTIPLEXER
2-BIT COUNTER
INSTRUCTION DECODE LOGIC
CONTROL SIGNALS

FIG._20

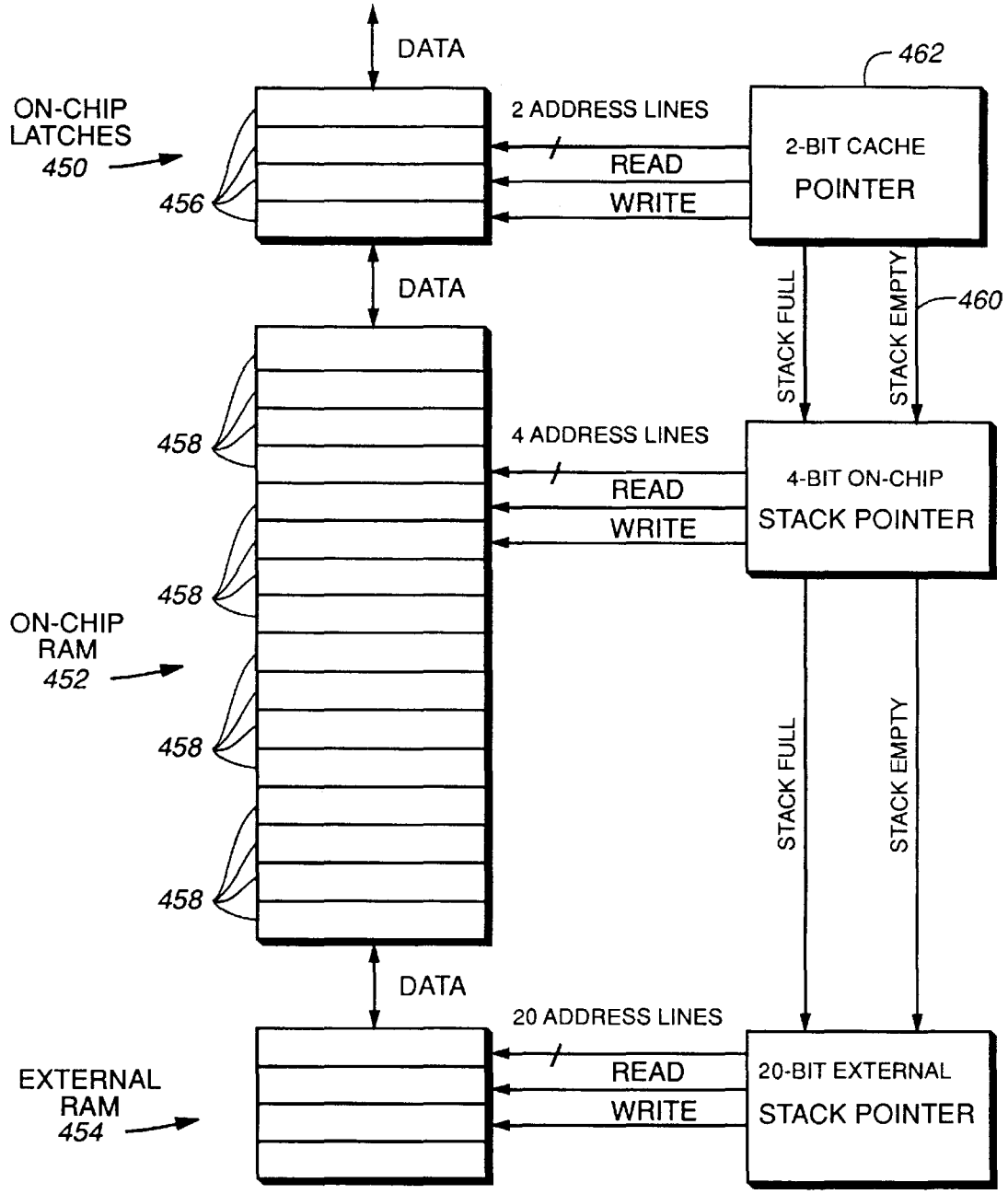

DATA
462
ON-CHIP
LATCHES
450
2 ADDRESS LINES
READ
WRITE
2-BIT CACHE
POINTER
456
DATA
STACK FULL
STACK EMPTY
460
458
4 ADDRESS LINES
READ
WRITE
4-BIT ON-CHIP
STACK POINTER
458
ON-CHIP
RAM
452
458
STACK FULL
STACK EMPTY
458
DATA
20 ADDRESS LINES
READ
WRITE
20-BIT EXTERNAL
STACK POINTER
EXTERNAL
RAM
454

FIG._21

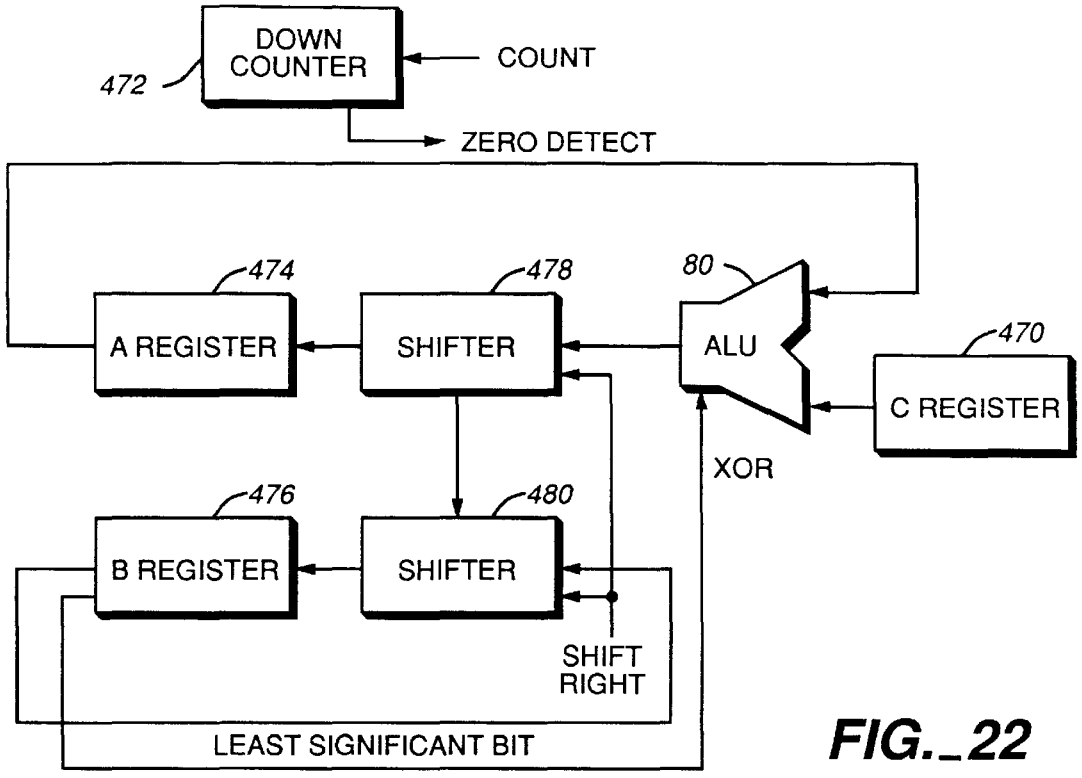

DOWN COUNTER
472
COUNT
ZERO DETECT
474
A REGISTER
478
SHIFTER
80
ALU
470
C REGISTER
XOR
476
B REGISTER
480
SHIFTER
SHIFT RIGHT
LEAST SIGNIFICANT BIT

FIG._22

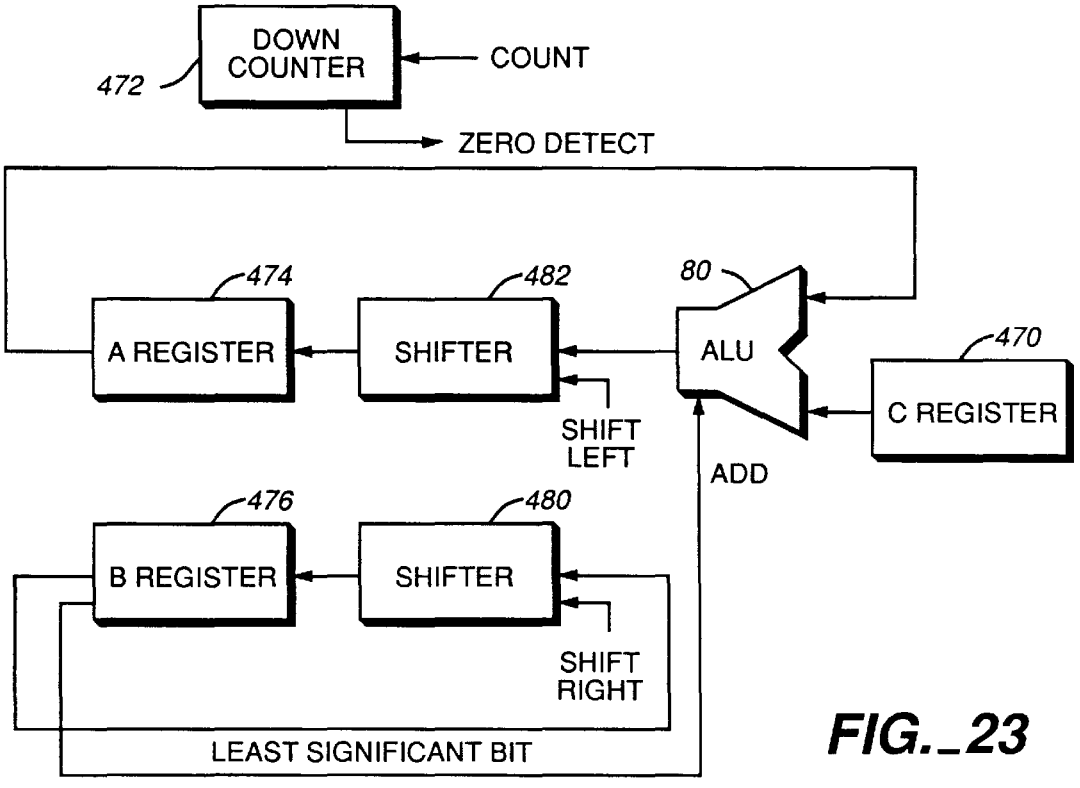

DOWN COUNTER
472
COUNT
ZERO DETECT
474
A REGISTER
482
SHIFTER
80
ALU
470
C REGISTER
SHIFT LEFT
ADD
476
B REGISTER
480
SHIFTER
SHIFT RIGHT
LEAST SIGNIFICANT BIT

FIG._23

HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a division of U.S. application Ser. No. 07/389,334, filed Aug. 3, 1989, now U.S. Pat. No. 5,440,749.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to a simplified, reduced instruction set computer (RISC) microprocessor. More particularly, it relates to such a microprocessor which is capable of performance levels of, for example, 20 million instructions per second (MIPS) at a price of, for example, 20 dollars.

2. Description of the Prior Art

Since the invention of the microprocessor, improvements in its design have taken two different approaches. In the first approach, a brute force gain in performance has been achieved through the provision of greater numbers of faster transistors in the microprocessor integrated circuit and an instruction set of increased complexity. This approach is exemplified by the Motorola 68000 and Intel 80X86 microprocessor families. The trend in this approach is to larger die sizes and packages, with hundreds of pinouts.

More recently, it has been perceived that performance gains can be achieved through comparative simplicity, both in the microprocessor integrated circuit itself and in its instruction set. This second approach provides RISC microprocessors, and is exemplified by the Sun SPARC and the Intel 8960 microprocessors. However, even with this approach as conventionally practiced, the packages for the microprocessor are large, in order to accommodate the large number of pinouts that continue to be employed. A need therefore remains for further simplification of high performance microprocessors.

With conventional high performance microprocessors, fast static memories are required for direct connection to the microprocessors in order to allow memory accesses that are fast enough to keep up with the microprocessors. Slower dynamic random access memories (DRAMs) are used with such microprocessors only in a hierarchical memory arrangement, with the static memories acting as a buffer between the microprocessors and the DRAMs. The necessity to use static memories increases cost of the resulting systems.

Conventional microprocessors provide direct memory accesses (DMA) for system peripheral units through DMA controllers, which may be located on the microprocessor integrated circuit, or provided separately. Such DMA controllers can provide routine handling of DMA requests and responses, but some processing by the main central processing unit (CPU) of the microprocessor is required.

SUMMARY OF THE INVENTION

Accordingly, it is an object of this invention to provide a microprocessor with a reduced pin count and cost compared to conventional microprocessors.

It is another object of the invention to provide a high performance microprocessor that can be directly connected to DRAMs without sacrificing microprocessor speed.

It is a further object of the invention to provide a high performance microprocessor in which DMA does not require use of the main CPU during DMA requests and responses and which provides very rapid DMA response with predictable response times.

The attainment of these and related objects may be achieved through use of the novel high performance, low cost microprocessor herein disclosed. In accordance with one aspect of the invention, a microprocessor system in accordance with this invention has a central processing unit, a dynamic random access memory and a bus connecting the central processing unit to the dynamic random access memory. There is a multiplexing means on the bus between the central processing unit and the dynamic random access memory. The multiplexing means is connected and configured to provide row addresses, column addresses and data on the bus.

In accordance with another aspect of the invention, the microprocessor system has a means connected to the bus for fetching instructions for the central processing unit on the bus. The means for fetching instructions is configured to fetch multiple sequential instructions in a single memory cycle. In a variation of this aspect of the invention, a programmable read only memory containing instructions for the central processing unit is connected to the bus. The means for fetching instructions includes means for assembling a plurality of instructions from the programmable read only memory and storing the plurality of instructions in the dynamic random access memory.

In another aspect of the invention, the microprocessor system includes a central processing unit, a direct memory access processing unit and a memory connected by a bus. The direct memory access processing unit includes means for fetching instructions for the central processing unit and for fetching instructions for the direct memory access processing unit on the bus.

In a further aspect of the invention, the microprocessor system, including the memory, is contained in an integrated circuit. The memory is a dynamic random access memory, and the means for fetching multiple instructions includes a column latch for receiving the multiple instructions.

In still another aspect of the invention, the microprocessor system additionally includes an instruction register for the multiple instructions connected to the means for fetching instructions. A means is connected to the instruction register for supplying the multiple instructions in succession from the instruction register. A counter is connected to control the means for supplying the multiple instructions to supply the multiple instructions in succession. A means for decoding the multiple instructions is connected to receive the multiple instructions in succession from the means for supplying the multiple instructions. The counter is connected to said means for decoding to receive incrementing and reset control signals from the means for decoding. The means for decoding is configured to supply the reset control signal to the counter and to supply a control signal to the means for fetching instructions in response to a SKIP instruction in the multiple instructions. In a modification of this aspect of the invention, the microprocessor system additionally has a loop counter connected to receive a decrement control signal from the means for decoding. The means for decoding is configured to supply the reset control signal to the counter and the decrement control signal to the loop counter in response to a MICROLOOP instruction in the multiple instructions. In a further modification to this aspect of the invention, the means for decoding is configured to control

the counter in response to an instruction utilizing a variable width operand. A means is connected to the counter to select the variable width operand in response to the counter.

In a still further aspect of the invention, the microprocessor system includes an arithmetic logic unit. A first push down stack is connected to the arithmetic logic unit. The first push down stack includes means for storing a top item connected to a first input of the arithmetic logic unit and means for storing a next item connected to a second input of the arithmetic logic unit. The arithmetic logic unit has an output connected to the means for storing a top item. The means for storing a top item is connected to provide an input to a register file. The register file desirably is a second push down stack, and the means for storing a top item and the register file are bidirectionally connected.

In another aspect of the invention, a data processing system has a microprocessor including a sensing circuit and a driver circuit, a memory, and an output enable line connected between the memory, the sensing circuit and the driver circuit. The sensing circuit is configured to provide a ready signal when the output enable line reaches a predetermined electrical level, such as a voltage. The microprocessor is configured so that the driver circuit provides an enabling signal on the output enable line responsive to the ready signal.

In a further aspect of the invention, the microprocessor system has a ring counter variable speed system clock connected to the central processing unit. The central processing unit and the ring counter variable speed system clock are provided in a single integrated circuit. An input/output interface is connected to exchange coupling control signals, addresses and data with the input/output interface. A second clock independent of the ring counter variable speed system clock is connected to the input/output interface.

In yet another aspect of the invention, a push down stack is connected to the arithmetic logic unit. The push down stack includes means for storing a top item connected to a first input of the arithmetic logic unit and means for storing a next item connected to a second input of the arithmetic logic unit. The arithmetic logic unit has an output connected to the means for storing a top item. The push down stack has a first plurality of stack elements configured as latches and a second plurality of stack elements configured as a random access memory. The first and second plurality of stack elements and the central processing unit are provided in a single integrated circuit. A third plurality of stack elements is configured as a random access memory external to the single integrated circuit. In this aspect of the invention, desirably a first pointer is connected to the first plurality of stack elements, a second pointer connected to the second plurality of stack elements, and a third pointer is connected to the third plurality of stack elements. The central processing unit is connected to pop items from the first plurality of stack elements. The first stack pointer is connected to the second stack pointer to pop a first plurality of items from the second plurality of stack elements when the first plurality of stack elements are empty from successive pop operations by the central processing unit. The second stack pointer is connected to the third stack pointer to pop a second plurality of items from the third plurality of stack elements when the second plurality of stack elements are empty from successive pop operations by the central processing unit.

In another aspect of the invention, a first register is connected to supply a first input to the arithmetic logic unit. A first shifter is connected between an output of the arithmetic logic unit and the first register. A second register is connected to receive a starting polynomial value. An output of the second register is connected to a second shifter. A least significant bit of the second register is connected to The arithmetic logic unit. A third register is connected to supply feedback terms of a polynomial to the arithmetic logic unit. A down counter, for counting down a number corresponding to digits of a polynomial to be generated, is connected to the arithmetic logic unit. The arithmetic logic unit is responsive to a polynomial instruction to carry out an exclusive OR of the contents of the first register with the contents of the third register if the least significant bit of the second register is a "ONE" and to pass the contents of the first register unaltered if the least significant bit of the second register is a "ZERO", until the down counter completes a count. The polynomial to be generated results in said first register.

In still another aspect of the invention, a result register is connected to supply a first input to the arithmetic logic unit. A first, left shifting shifter is connected between an output of the arithmetic logic unit and the result register. A multiplier register is connected to receive a multiplier in bit reversed form. An output of the multiplier register is connected to a second, right shifting shifter. A least significant bit of the multiplier register is connected to the arithmetic logic unit. A third register is connected to supply a multiplicand to said arithmetic logic unit. A down counter, for counting down a number corresponding to one less than the number of digits of the multiplier, is connected to the arithmetic logic unit. The arithmetic logic unit is responsive to a multiply instruction to add the contents of the result register with the contents of the third register, when the least significant bit of the multiplier register is a "ONE" and to pass the contents of the result register unaltered, until the down counter completes a count. The product results in the result register.

The attainment of the foregoing and related objects, advantages and features of the invention should be more readily apparent to those skilled in the art, after review of the following more detailed description of the invention, taken together with the drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an external, plan view of an integrated circuit package incorporating a microprocessor in accordance with the invention.

FIG. **2** is a block diagram of a microprocessor in accordance with the invention.

FIG. **3** is a block diagram of a portion of a data processing system incorporating the microprocessor of FIGS. **1** and **2**.

FIG. **4** is a more detailed block diagram of a portion of the microprocessor shown in FIG. **2**.

FIG. **5** is a more detailed block diagram of another portion of the microprocessor shown in FIG. **2**.

FIG. **6** is a block diagram of another portion of the data processing system shown in part in FIG. **3** and incorporating the microprocessor of FIGS. **1**–**2** and **4**–**5**.

FIGS. **7** and **8** are layout diagrams for the data processing system shown in part in FIGS. **3** and **6**.

FIG. **9** is a layout diagram of a second embodiment of a microprocessor in accordance with the invention in a data processing system on a single integrated circuit.

FIG. **10** is a more detailed block diagram of a portion of the data processing system of FIGS. **7** and **8**.

FIG. **11** is a timing diagram useful for understanding operation of the system portion shown in FIG. **12**.

FIG. **12** is another more detailed block diagram of a further portion of the data processing system of FIGS. **7** and **8**.

FIG. **13** is a more detailed block diagram of a portion of the microprocessor shown in FIG. **2**.

FIG. **14** is a more detailed block and schematic diagram of a portion of the system shown in FIGS. **3** and **7–8**.

FIG. **15** is a graph useful for understanding operation of the system portion shown in FIG. **14**.

FIG. **16** is a more detailed block diagram showing part of the system portion shown in FIG. **4**.

FIG. **17** is a more detailed block diagram of a portion of the microprocessor shown in FIG. **2**.

FIG. **18** is a more detailed block diagram of part of the microprocessor portion shown in FIG. **17**.

FIG. **19** is a set of waveform diagrams useful for understanding operation of the part of the microprocessor portion shown in FIG. **18**.

FIG. **20** is a more detailed block diagram showing another part of the system portion shown in FIG. **4**.

FIG. **21** is a more detailed block diagram showing another part of the system portion shown in FIG. **4**.

FIGS. **22** and **23** are more detailed block diagrams showing another part of the system portion shown in FIG. **4**.

DETAILED DESCRIPTION OF THE INVENTION

Overveiw

The microprocessor of this invention is desirably implemented as a 32-bit microprocessor optimized for:

HIGH EXECUTION SPEED, and

LOW SYSTEM COST.

In this embodiment, the microprocessor can be thought of as 20 MIPS for 20 dollars. Important distinguishing features of the microprocessor are:

Uses low-cost commodity DYNAMIC RAMS to run 20 MIPS

4 instruction fetch per memory cycle

On-chip fast page-mode memory management

Runs fast without external cache

Requires few interfacing chips

Crams 32-bit CPU in 44 pin SOJ package

The instruction set is organized so that most operations can be specified with 8-bit instructions. Two positive products of this philosophy are:

Programs are smaller,

Programs can execute much faster.

The bottleneck in most computer systems is the memory bus. The bus is used to fetch instructions and fetch and store data. The ability to fetch four instructions in a single memory bus cycle significantly increases the bus availability to handle data.

Turning now to the drawings, more particularly to FIG. **1**, there is shown a packaged 32-bit microprocessor **50** in a 44-pin plastic leadless chip carrier, shown approximately 100 times its actual size of about 0.8 inch on a side. The fact that the microprocessor **50** is provided as a 44-pin package represents a substantial departure from typical microprocessor packages, which usually have about 200 input/output (I/O) pins. The microprocessor **50** is rated at 20 million instructions per second (MIPS). Address and data lines **52**, also labelled D**0**–D**31**, are shared for addresses and data without speed penalty as a result of the manner in which the microprocessor **50** operates, as will be explained below.

DYNAMIC RAM

In addition to the low cost 44-pin package, another unusual aspect of the high performance microprocessor **50** is that it operates directly with dynamic random access memories (DRAMs), as shown by row address strobe (RAS) and column address strobe (CAS) I/O pins **54**. The other I/O pins for the microprocessor **50** include V_{DD} pins **56**, V_{SS} pins **58**, output enable pin **60**, write pin **62**, clock pin **64** and reset pin **66**.

All high speed computers require high speed and expensive memory to keep up. The highest speed static RAM memories cost as much as ten times as much as slower dynamic RAMs. This microprocessor has been optimized to use low-cost dynamic RAM in high-speed page-mode. Page-mode dynamic RAMs offer static RAM performance without the cost penalty. For example, low-cost 85 nsec. dynamic RAMs access at 25 nsec when operated in fast page-mode. Integrated fast page-mode control on the microprocessor chip simplifies system interfacing and results in a faster system.

Details of the microprocessor **50** are shown in FIG. **2**. The microprocessor **50** includes a main central processing unit (CPU) **70** and a separate direct memory access (DMA) CPU **72** in a single integrated circuit making up the microprocessor **50**. The main CPU **70** has a first **16** deep push down stack **74**, which has a top item register **76** and a next item register **78**, respectively connected to provide inputs to an arithmetic logic unit (ALU) **80** by lines **82** and **84**. An output of the ALU **80** is connected to the top item register **76** by line **86**. The output of the top item register at **82** is also connected by line **88** to an internal data bus **90**.

A loop counter **92** is connected to a decrementer **94** by lines **96** and **98**. The loop counter **92** is bidirectionally connected to the internal data bus **90** by line **100**. Stack pointer **102**, return stack pointer **104**, mode register **106** and instruction register **108** are also connected to the internal data bus **90** by lines **110**, **112**, **114** and **116**, respectively. The internal data bus **90** is connected to memory controller **118** and to gate **120**. The gate **120** provides inputs on lines **122**, **124**, and **126** to X register **128**, program counter **130** and Y register **132** of return push down stack **134**. The X register **128**, program counter **130** and Y register **132** provide outputs to internal address bus **136** on lines **138**, **140** and **142**. The internal address bus provides inputs to the memory controller **118** and to an incrementer **144**. The incrementer **144** provides inputs to the X register, program counter and Y register via lines **146**, **122**, **124** and **126**. The DMA CPU **72** provides inputs to the memory controller **118** on line **148**. The memory controller **118** is connected to a RAM (not shown) by address/data bus **150** and control lines **152**.

FIG. **2** shows that the microprocessor **50** has a simple architecture. Prior art RISC microprocessors are substantially more complex in design. For example, the SPARC RISC microprocessor has three times the gates of the microprocessor **50**, and the Intel 8960 RISC microprocessor has 20 times the gates of the microprocessor **50**. The speed of this microprocessor is in substantial part due to this simplicity. The architecture incorporates push down stacks and register write to achieve this simplicity.

The microprocessor **50** incorporates an I/O that has been tuned to make heavy use of resources provided on the integrated circuit chip. On chip latches allow use of the same I/O circuits to handle three different things: column addressing, row addressing and data, with a slight to non-existent speed penalty. This triple bus multiplexing results in fewer buffers to expand, fewer interconnection lines, fewer I/O pins and fewer internal buffers.

The provision of on-chip DRAM control gives a performance equal to that obtained with the use of static RAMs. As a result, memory is provided at ¼ the system cost of static RAM used in most RISC systems.

The microprocessor **50** fetches 4 instructions per memory cycle; the instructions are in an 8-bit format, and this is a 32-bit microprocessor. System speed is therefore 4 times the memory bus bandwidth. This ability enables the microprocessor to break the Von Neumann bottleneck of the speed of getting the next instruction. This mode of operation is possible because of the use of a push down stack and register array. The push down stack allows the use of implied addresses, rather than the prior art technique of explicit addresses for two sources and a destination.

Most instructions execute in 20 nanoseconds in the microprocessor **50**. The microprocessor can therefore execute instructions at 50 peak MIPS without pipeline delays. This is a function of the small number of gates in the microprocessor **50** and the high degree of parallelism in the architecture of the microprocessor.

FIG. **3** shows how column and row addresses are multiplexed on lines D**8**–D**14** of the microprocessor **50** for addressing DRAM **150** from I/O pins **52**. The DRAM **150** is one of eight, but only one DRAM **150** has been shown for clarity. As shown, the lines D**11**–D**18** are respectively connected to row address inputs A**0**–A**8** of the DRAM **150**. Additionally, lines D**12**–D**15** are connected to the data inputs DQ**1**–DQ**4** of the DRAM **150**. The output enable, write and column address strobe pins **54** are respectively connected to the output enable, write and column address strobe inputs of the DRAM **150** by lines **152**. The row address strobe pin **54** is connected through row address strobe decode logic **154** to the row address strobe input of the DRAM **150** by lines **156** and **158**.

D**0**–D**7** pins **52** (FIG. **1**) are idle when the microprocessor **50** is outputting multiplexed row and column addresses on D**11**–D**18** pins **52**. The D**0**–D**7** pins **52** can therefore simultaneously be used for I/O when right justified I/O is desired. Simultaneous addressing and I/O can therefore be carried out.

FIG. **4** shows how the microprocessor **50** is able to achieve performance equal to the use of static RAMS with DRAMs through multiple instruction fetch in a single clock cycle and instruction fetch-ahead. Instruction register **108** receives four 8-bit byte instruction words 1–4 on 32-bit internal data bus **90**. The four instruction byte 1–4 locations of the instruction register **108** are connected to multiplexer **170** by busses **172**, **174**, **176** and **178**, respectively. A microprogram counter **180** is connected to the multiplexer **170** by lines **182**. The multiplexer **170** is connected to decoder **184** by bus **186**. The decoder **184** provides internal signals to the rest of the microprocessor **50** on lines **188**.

Most significant bits **190** of each instruction byte 1–4 location are connected to a 4-input decoder **192** by lines **194**. The output of decoder **192** is connected to memory controller **118** by line **196**. Program counter **130** is connected to memory controller **118** by internal address bus **136**, and the instruction register **108** is connected to the memory controller **118** by the internal data bus **90**. Address/data bus **198** and control bus **200** are connected to the DRAMS **150** (FIG. **3**).

In operation, when the most significant bits **190** of remaining instructions 1–4 are "1" in a clock cycle of the microprocessor **50**, there are no memory reference instructions in the queue. The output of decoder **192** on line **196** requests an instruction fetch ahead by memory controller **118** without interference with other accesses. While the current instructions in instruction register **108** are executing, the memory controller **118** obtains the address of the next set of four instructions from program counter **130** and obtains that set of instructions. By the time the current set of instructions has completed execution, the next set of instructions is ready for loading into the instruction register.

Details of the DMA CPU **72** are provided in FIG. **5**. Internal data bus **90** is connected to memory controller **118** and to DMA instruction register **210**. The DMA instruction register **210** is connected to DMA program counter **212** by bus **214**, to transfer size counter **216** by bus **218** and to timed transfer interval counter **220** by bus **222**. The DMA instruction register **210** is also connected to DMA I/O and RAM address register **224** by line **226**. The DMA I/O and RAM address register **224** is connected to the memory controller **118** by memory cycle request line **228** and bus **230**. The DMA program counter **212** is connected to the internal address bus **136** by bus **232**. The transfer size counter **216** is connected to a DMA instruction done decrementer **234** by lines **236** and **238**. The decrementer **234** receives a control input on memory cycle acknowledge line **240**. When transfer size counter **216** has completed its count, it provides a control signal to DMA program counter **212** on line **242**. Timed transfer interval counter **220** is connected to decrementer **244** by lines **246** and **248**. The decrementer **244** receives a control input from a microprocessor system clock on line **250**.

The DMA CPU **72** controls itself and has the ability to fetch and execute instructions. It operates as a co-processor to the main CPU **70** (FIG. **2**) for time specific processing.

FIG. **6** shows how the microprocessor **50** is connected to an electrically programmable read only memory (EPROM) **260** by reconfiguring the data lines **52** so that some of the data lines **52** are input lines and some of them are output lines. Data lines **52** D**0**–D**7** provide data to and from corresponding data terminals **262** of the EPROM **260**. Data lines **52** D**9**–D**18** provide addresses to address terminals **264** of the EPROM **260**. Data lines **52** D**19**–D**31** provide inputs from the microprocessor **50** to memory and I/O decode logic **266**. RAS 0/1 control line **268** provides a control signal for determining whether the memory and I/O decode logic provides a DRAM RAS output on line **270** or a column enable output for the EPROM **260** on line **272**. Column address strobe terminal **60** of the microprocessor **50** provides an output enable signal on line **274** to the corresponding terminal **276** of the EPROM **260**.

FIGS. **7** and **8** show the front and back of a one card data processing system **280** incorporating the microprocessor **50**, MSM514258-10 type DRAMs **150** totalling 2 megabytes, a Motorola 50 MegaHertz crystal oscillator clock **282**, I/O circuits **284** and a 27256 type EPROM **260**. The I/O circuits **284** include a 74HC04 type high speed hex inverter circuit **286**, an IDT39C828 type 10-bit inverting buffer circuit **288**, an IDT39C822 type 10-bit inverting register circuit **290**, and two IDT39C823 type 9-bit non-inverting register circuits **292**. The card **280** is completed with a MAX12V type DC-DC converter circuit **294**, 34-pin dual AMP type headers **296**, a coaxial female power connector **298**, and a 3-pin AMP right angle header **300**. The card **280** is a low cost, imbeddable product that can be incorporated in larger systems or used as an internal development tool.

The microprocessor **50** is a very high performance (50 MHz) RISC influenced 32-bit CPU designed to work closely with dynamic RAM. Clock for clock, the microprocessor **50** approaches the theoretical performance limits possible with a single CPU configuration. Eventually, the microprocessor **50** and any other processor is limited by the bus bandwidth and the number of bus paths. The critical conduit is between the CPU and memory.

One solution to the bus bandwidth/bus path problem is to integrate a CPU directly onto the memory chips, giving every memory a direct bus the CPU. FIG. **9** shows another microprocessor **310** that is provided integrally with 1 mega-

bit of DRAM **311** in a single integrated circuit **312**. Until the present invention, this solution has not been practical, because most high performance CPUs require from 500,000 to 1,000,000 transistors and enormous die sizes just by themselves. The microprocessor **310** is equivalent to the microprocessor **50** in FIGS. **1–8**. The microprocessors **50** and **310** are the most transistor efficient high performance CPUs in existence, requiring fewer than 50,000 transistors for dual processors **70** and **72** (FIG. **2**) or **314** and **316** (less memory). The very high speed of the microprocessors **50** and **310** is to a certain extent a function of the small number of active devices. In essence, the less silicon gets in the way, the faster the electrons can get where they are going.

The microprocessor **310** is therefore the only CPU suitable for integration on the memory chip die **312**. Some simple modifications to the basic microprocessor **50** to take advantage of the proximity to the DRAM array **311** can also increase the microprocessor **50** clock speed by **50** percent, and probably more.

The microprocessor **310** core on board the DRAM die **312** provides most of the speed and functionality required for a large group of applications from automotive to peripheral control. However, the integrated CPU **310**/DRAM **311** concept has the potential to redefine significantly the way multiprocessor solutions can solve a spectrum of very compute intensive problems. The CPU **310**/DRAM **311** combination eliminates the Von Neumann bottleneck by distributing it across numerous CPU/DRAM chips **312**. The microprocessor **310** is a particularly good core for multiprocessing, since it was designed with the SDI targeting array in mind, and provisions were made for efficient interprocessor communications.

Traditional multiprocessor implementations have been very expensive in addition to being unable to exploit fully the available CPU horsepower. Multiprocessor systems have typically been built up from numerous board level or box level computers. The result is usually an immense amount of hardware with corresponding wiring, power consumption and communications problems. By the time the systems are interconnected, as much as 50 percent of the bus speed has been utilized just getting through the interfaces.

In addition, multiprocessor system software has been scarce. A multiprocessor system can easily be crippled by an inadequate load-sharing algorithm in the system software, which allows one CPU to do a great deal of work and the others to be idle. Great strides have been made recently in systems software, and even UNIX V.4 may be enhanced to support multiprocessing. Several commercial products from such manufacturers as DUAL Systems and UNISOFT do a credible job on 68030 type microprocessor systems now.

The microprocessor **310** architecture eliminates most of the interface friction, since up to 64 CPU **310**/RAM **311** processors should be able to intercommunicate without buffers or latches. Each chip **312** has about 40 MIPS raw speed, because placing the DRAM **311** next to the CPU **310** allows the microprocessor **310** instruction cycle to be cut in half, compared to the microprocessor **50**. A 64 chip array of these chips **312** is more powerful than any other existing computer. Such an array fits on a 3×5 card, cost less than a FAX machine, and draw about the same power as a small television.

Dramatic changes in price/performance always reshape existing applications and almost always create new ones. The introduction of microprocessors in the mid 1970s created video games, personal computers, automotive computers, electronically controlled appliances, and low cost computer peripherals.

The integrated circuit **312** will find applications in all of the above areas, plus create some new ones. A common generic parallel processing algorithm handles convolution/Fast Fourier Transform (FFT)/pattern recognition. Interesting product possibilities using the integrated circuit **312** include high speed reading machines, real-time speech recognition, spoken language translation, real-time robot vision, a product to identify people by their faces, and an automotive or aviation collision avoidance system.

A real time processor for enhancing high density television (HDTV) images, or compressing the HDTV information into a smaller bandwidth, would be very. feasible. The load sharing in HDTV could be very straightforward. Splitting up the task according to color and frame would require 6, 9 or 12 processors. Practical implementation might require 4 meg RAMs integrated with the microprocessor **310**.

The microprocessor **310** has the following specifications:

CONTROL LINES
4—POWER/GROUND
1—CLOCK
32—DATA I/O
4—SYSTEM CONTROL
EXTERNAL MEMORY FETCH
EXTERNAL MEMORY FETCH AUTOINCREMENT X
EXTERNAL MEMORY FETCH AUTOINCREMENT Y
EXTERNAL MEMORY WRITE
EXTERNAL MEMORY WRITE AUTOINCREMENT X
EXTERNAL MEMORY WRITE AUTOINCREMENT Y
EXTERNAL PROM FETCH
LOAD ALL X REGISTERS
LOAD ALL Y REGISTERS
LOAD ALL PC REGISTERS
EXCHANGE X AND Y
INSTRUCTION FETCH
ADD TO PC
ADD TO X
WRITE MAPPING REGISTER
READ MAPPING REGISTER
REGISTER CONFIGURATION
MICROPROCESSOR **310** CPU **316** CORE
COLUMN LATCH**1** (1024 BITS) 32×32 MUX
STACK POINTER (16 BITS)
COLUMN LATCH**2** (1024 BITS) 32×32 MUX
RSTACK POINTER (16 BITS)
PROGRAM COUNTER 32 BITS
X0 REGISTER 32 BITS (ACTIVATED ONLY FOR ON-CHIP ACCESSES)
Y0 REGISTER 32 BITS (ACTIVATED ONLY FOR ON-CHIP ACCESSES)
LOOP COUNTER 32 BITS
DMA CPU **314** CORE
DMA PROGRAM COUNTER 24 BITS
INSTRUCTION REGISTER 32 BITS
I/O & RAM ADDRESS REGISTER 32 BITS
TRANSFER SIZE COUNTER 12 BITS
INTERVAL COUNTER 12 BITS

To offer memory expansion for the basic chip **312**, an intelligent DRAM can be produced. This chip will be optimized for high speed operation with the integrated circuit **312** by having three on-chip address registers: Program Counter, X Register and Y register. As a result, to access the intelligent DRAM, no address is required, and a total access cycle could be as short as 10 nsec. Each

expansion DRAM would maintain its own copy of the three registers and would be identified by a code specifying its memory address. Incrementing and adding to the three registers will actually take place on the memory chips. A maximum of 64 intelligent DRAM peripherals would allow a large system to be created without sacrificing speed by introducing multiplexers or buffers.

There are certain differences between the microprocessor **310** and the microprocessor **50** that arise from providing the microprocessor **310** on the same die **312** with the DRAM **311**. Integrating the DRAM **311** allows architectural changes in the microprocessor **310** logic to take advantage of existing on-chip DRAM **311** circuitry. Row and column design is inherent in memory architecture. The DRAMs **311** access random bits in a memory array by first selecting a row of 1024 bits, storing them into a column latch, and then selecting one of the bits as the data to be read or written.

The time required to access the data is split between the row access and the column access. Selecting data already stored in a column latch is faster than selecting a random bit by at least a factor of six. The microprocessor **310** takes advantage of this high speed by creating a number of column latches and using them as caches and shift registers. Selecting a new row of information may be thought of as performing a 1024-bit read or write with the resulting immense bus bandwidth.

1. The microprocessor **50** treats its 32-bit instruction register **108** (see FIGS. **2** and **4**) as a cache for four 8-bit instructions. Since the DRAM **311** maintains a 1024-bit latch for the column bits, the microprocessor **310** treats the column latch as a cache for 128 8-bit instructions. Therefore, the next instruction will almost always be already present in the cache. Long loops within the cache are also possible and more useful than the 4 instruction loops in the microprocessor **50**.

2. The microprocessor **50** uses two 16×32-bit deep register arrays **74** and **134** (FIG. **2**) for the parameter stack and the return stack. The microprocessor **310** creates two other 1024-bit column latches to provide the equivalent of two 32×32-bit arrays, which can be accessed twice as fast as a register array.

3. The microprocessor **50** has a DMA capability which can be used for I/O to a video shift register. The microprocessor **310** uses yet another 1024-bit column latch as a long video shift register to drive a CRT display directly. For color displays, three on-chip shift registers could also be used. These shift registers can transfer pixels at a maximum of 100 MHz.

4. The microprocessor **50** accesses memory via an external 32-bit bus. Most of the memory **311** for the microprocessor **310** is on the same die **312**. External access to more memory is made using an 8-bit bus. The result is a smaller die, smaller package and lower power consumption than the microprocessor **50**.

5. The microprocessor **50** consumes about a third of its operating power charging and discharging the I/O pins and associated capacitances. The DRAMs **150** (FIG. **8**) connected to the microprocessor **50** dissipate most of their power in the I/O drivers. A microprocessor **310** system will consume about one-tenth the power of a microprocessor **50** system, since having the DRAM **311** next to the processor **310** eliminates most of the external capacitances to be charged and discharged.

6. Multiprocessing means splitting a computing task between numerous processors in order to speed up the solution. The popularity of multiprocessing is limited by the expense of current individual processors as well as the limited interprocessor communications ability. The microprocessor **310** is an excellent multiprocessor candidate, since the chip **312** is a monolithic computer complete with memory, rendering it low-cost and physically compact.

The shift registers implemented with the microprocessor **310** to perform video output can also be configured as interprocessor communication links. The INMOS transputer attempted a similar strategy, but at much lower speed and without the performance benefits inherent in the microprocessor **310** column latch architecture. Serial I/O is a prerequisite for many multiprocessor topologies because of the many neighbor processors which communicate. A cube has 6 neighbors. Each neighbor communicates using these lines:

DATA IN
CLOCK IN
READY FOR DATA
DATA OUT
DATA READY?
CLOCK OUT

A special start up sequence is used to initialize the on-chip DRAM **311** in each of the processors.

The microprocessor **310** column latch architecture allows neighbor processors to deliver information directly to internal registers or even instruction caches of other chips **312**. This technique is not used with existing processors, because it only improves performance in a tightly coupled DRAM system.

7. The microprocessor **50** architecture offers two types of looping structures: LOOP-IF-DONE and MICRO-LOOP. The former takes an 8-bit to 24-bit operand to describe the entry point to the loop address. The latter performs a loop entirely within the 4 instruction queue and the loop entry point is implied as the first instruction in the queue. Loops entirely within the queue run without external instruction fetches and execute up to three times as fast as the long loop construct. The microprocessor **310** retains both constructs with a few differences. The microprocessor **310** microloop functions in the same fashion as the microprocessor **50** operation, except the queue is 1024-bits or 128 8-bit instructions long. The microprocessor **310** microloop can therefore contain jumps, branches, calls and immediate operations not possible in the 4 8-bit instruction microprocessor **50** queue.

Microloops in the microprocessor **50** can only perform simple block move and compare functions. The larger microprocessor **310** queue allows entire digital signal processing or floating point algorithms to loop at high speed in the queue.

The microprocessor **50** offers four instructions to redirect execution:

CALL
BRANCH
BRANCH-IF-ZERO
LOOP-IF-NOT-DONE

These instructions take a variable length address operand 8, 16 or 24 bits long. The microprocessor **50** next address logic treats the three operands similarly by adding or subtracting them to the current program counter. For the microprocessor **310**, the 16 and 24-bit operands function in the same manner as the 16 and 24-bit operands in the microprocessor **50**. The 8-bit class operands are reserved to operate entirely within the instruction queue. Next address decisions can therefore be made quickly, because only 10 bits of addresses are affected, rather than 32. There is no carry or borrow generated past the 10 bits.

8. The microprocessor **310** CPU **316** resides on an already crowded DRAM die **312**. To keep chip size as small as

possible, the DMA processor **72** of the microprocessor **50** has been replaced with a more traditional DMA controller **314**. DMA is used with the microprocessor **310** to perform the following functions:

Video output to a CRT

Multiprocessor serial communications

8-bit parallel I/O

The DMA controller **314** can maintain both serial and parallel transfers simultaneously. The following DMA sources and destinations are supported by the microprocessor **310**:

DESCRIPTION	I/O	LINES
1. Video shift register	OUTPUT	1 to 3
2. Multiprocessor serial	BOTH	6 lines/channel
3. 8-bit parallel	BOTH	8 data, 4 control

The three sources use separate 1024-bit buffers and separate I/O pins. Therefore, all three may be active simultaneously without interference.

The microprocessor **310** can be implemented with either a single multiprocessor serial buffer or separate receive and sending buffers for each channel, allowing simultaneous bidirectional communications with six neighbors simultaneously.

FIGS. **10** and **11** provide details of the PROM DMA used in the microprocessor **50**. The microprocessor **50** executes faster than all but the fastest PROMs. PROMS are used in a microprocessor **50** system to store program segments and perhaps entire programs. The microprocessor **50** provides a feature on power-up to allow programs to be loaded from low-cost, slow speed PROMs into high speed DRAM for execution. The logic which performs this function is part of the DMA memory controller **118**. The operation is similar to DMA, but not identical, since four 8-bit bytes must be assembled on the microprocessor **50** chip, then written to the DRAM **150**.

The microprocessor **50** directly interfaces to DRAM **150** over a triple multiplexed data and address bus **350**, which carries RAS addresses, CAS addresses and data. The EPROM **260**, on the other hand, is read with non-multiplexed busses. The microprocessor **50** therefore has a special mode which unmultiplexes the data and address lines to read 8 bits of EPROM data. Four 8-bit bytes are read in this fashion. The multiplexed bus **350** is turned back on, and the data is written to the DRAM **150**.

When the microprocessor **50** detects a RESET condition, the processor stops the main CPU **70** and forces a mode **0** (PROM LOAD) instruction into the DMA CPU **72** instruction register. The DMA instruction directs the memory controller to read the EPROM **260** data at 8 times the normal access time for memory. Assuming a 50 MHz microprocessor **50**, this means an access time of 320 nsec. The instruction also indicates:

The selection address of the EPROM **260** to be loaded,

The number of 32-bit words to transfer,

The DRAM **150** address to transfer into.

The sequence of activities to transfer one 32-bit word from EPROM **260** to DRAM **150** are:

1. RAS goes low at **352**, latching the EPROM **260** select information from the high order address bits. The EPROM **260** is selected.
2. Twelve address bits (consisting of what is normally DRAM CAS addresses plus two byte select bits are placed on the bus **350** going to the EPROM **260** address pins. These signals will remain on the lines until the data from the EPROM **260** has been read into the microprocessor **50**. For the first byte, the byte select bits will be binary 00.
3. CAS goes low at **354**, enabling the EPROM **260** data onto the lower 8 bits of the external address/data bus **350**. NOTE: It is important to recognize that, during this part of the cycle, the lower 8 bits of the external data/address bus are functioning as inputs, but the rest of the bus is still acting as outputs.
4. The microprocessor **50** latches these eight least significant bits internally and shifts them 8 bits left to shift them to the next significant byte position.
5. Steps 2, 3 and 4 are repeated with byte address 01.
6. Steps 2, 3 and 4 are repeated with byte address 10.
7. Steps 2, 3 and 4 are repeated with byte address 11.
8. CAS goes high at **356**, taking the EPROM **260** off the data bus.
9. RAS goes high at **358**, indicating the end of the EPROM **260** access.
10. RAS goes low at **360**, latching the DRAM select information from the high order address bits. At the same time, the RAS address bits are latched into the DRAM **150**. The DRAM **150** is selected.
11. CAS goes low at **362**, latching the DRAM **150** CAS addresses.
12. The microprocessor **50** places the previously latched EPROM **260** 32-bit data onto the external address/data bus **350**. W goes low at **364**, writing the 32 bits into the DRAM **150**.
13. W goes high at **366**. CAS goes high at **368**. The process continues with the next word.

FIG. **12** shows details of the microprocessor **50** memory controller **118**. In operation, bus requests stay present until they are serviced. CPU **70** requests are prioritized at **370** in the order of: 1, Parameter Stack; 2, Return Stack; 3, Data Fetch; 4, Instruction Fetch. The resulting CPU request signal and a DMA request signal are supplied as bus requests to bus control **372**, which provides a bus grant signal at **374**. Internal address bus **136** and a DMA counter **376** provide inputs to a multiplexer **378**. Either a row address or a column address are provided as an output to multiplexed address bus **380** as an output from the multiplexer **378**. The multiplexed address bus **380** and the internal data bus **90** provide address and data inputs, respectively, to multiplexer **382**. Shift register **384** supplies row address strobe (RAS) **1** and **2** control signals to multiplexer **386** and column address strobe (CAS) **1** and **2** control signals to multiplexer **388** on lines **390** and **392**. The shift register **384** also supplies output enable (OE) and write (W) signals on lines **394** and **396** and a control signal on line **398** to multiplexer **382**. The shift register **384** receives a RUN signal on line **400** to generate a memory cycle and supplies a MEMORY READY signal on line **402** when an access is complete.

STACK/REGISTER ARCHITECTURE

Most microprocessors use on-chip registers for temporary storage of variables. The on-chip registers access data faster than off-chip RAM. A few microprocessors use an on-chip push down stack for temporary storage.

A stack has the advantage of faster operation compared to on-chip registers by avoiding the necessity to select source and destination registers. (A math or logic operation always uses the top two stack items as source and the top of stack as destination.) The stack's disadvantage is that it makes some operations clumsy. Some compiler activities in particular require on-chip registers for efficiency.

As shown in FIG. **13**, the microprocessor **50** provides both on-chip registers **134** and a stack **74** and reaps the benefits of both.

BENEFITS:

1. Stack math and logic is twice as fast as those available on an equivalent register only machine. Most programmers and optimizing compilers can take advantage of this feature.
2. Sixteen registers are available for on-chip storage of local variables which can transfer to the stack for computation. The accessing of variables is three to four times as fast as available on a strictly stack machine.

The combined stack **74**/register **134** architecture has not been used previously due to inadequate understanding by computer designers of optimizing compilers and the mix of transfer versus math/logic instructions.

ADAPTIVE MEMORY CONTROLLER

A microprocessor must be designed to work with small or large memory configurations. As more memory loads are added to the data, address, and control lines, the switching speed of the signals slows down. The microprocessor **50** multiplexes the address/data bus three ways, so timing between the phases is critical. A traditional approach to the problem allocates a wide margin of time between bus phases so that systems will work with small or large numbers of memory chips connected. A speed compromise of as much as 50% is required.

As shown in FIG. **14**, the microprocessor **50** uses a feedback technique to allow the processor to adjust memory bus timing to be fast with small loads and slower with large ones. The OUTPUT ENABLE (OE) line **152** from the microprocessor **50** is connected to all memories **150** on the circuit board. The loading on the output enable line **152** to the microprocessor **50** is directly related to the number of memories **150** connected. By monitoring how rapidly OE **152** goes high after a read, the microprocessor **50** is able to determine when the data hold time has been satisfied and place the next address on the bus.

The level of the OE line **152** is monitored by CMOS input buffer **410** which generates an internal READY signal on line **412** to the microprocessor's memory controller. Curves **414** and **416** of the FIG. **15** graph show the difference in rise time likely to be encountered from a lightly to heavily loaded memory system. When the OE line **152** has reached a predetermined level to generate the READY signal, driver **418** generates an OUTPUT ENABLE signal on OE line **152**.

SKIP WITHIN THE INSTRUCTION CACHE

The microprocessor **50** fetches four 8-bit instructions each memory cycle and stores them in a 32-bit instruction register **108**, as shown in FIG. **16**. A class of "test and skip" instructions can very rapidly execute a very fast jump operation within the four instruction cache.

SKIP CONDITIONS:

Always

ACC non-zero

ACC negative

Carry flag equal logic one

Never

ACC equal zero

ACC positive

Carry flag equal logic zero

The SKIP instruction can be located in any of the four byte positions **420** in the 32-bit instruction register **108**. If the test is successful, SKIP will jump over the remaining one, two, or three 8-bit instructions in the instruction register **108** and cause the next four-instruction group to be loaded into the register **108**. As shown, the SKIP operation is implemented by resetting the 2-bit microinstruction counter **180** to zero on line **422** and simultaneously latching the next instruction group into the register **108**. Any instructions following the SKIP in the instruction register are overwritten by the new instructions and not executed.

The advantage of SKIP is that optimizing compilers and smart programmers can often use it in place of the longer conditional JUMP instruction. SKIP also makes possible microloops which exit when the loop counts down or when the SKIP jumps to the next instruction group. The result in very fast code.

Other machines (such as the PDP-8 and Data General NOVA) provide the ability to skip a single instruction. The microprocessor **50** provides the ability to skip up to three instructions.

MICROLOOP IN THE INSTRUCTION CACHE

The microprocessor **50** provides the MICROLOOP instruction to execute repetitively from one to three instructions residing in the instruction register **108**. The microloop instruction works in conjunction with the LOOP COUNTER **92** (FIG. **2**) connected to the internal data bus **90**. To execute a microloop, the program stores a count in LOOP COUNTER **92**. MICROLOOP may be placed in the first, second, third, or last byte **420** of the instruction register **108**. If placed in the first position, execution will just create a delay equal to the number stored in LOOP COUNTER **92** times the machine cycle. If placed in the second, third, or last byte **420**, when the microloop instruction is executed, it will test the LOOP COUNT for zero. If zero, execution will continue with the next instruction. If not zero, the LOOP COUNTER **92** is decremented and the 2-bit microinstruction counter is cleared, causing the preceding instructions in the instruction register to be executed again.

Microloop is useful for block move and search operations. By executing a block move completely out of the instruction register **108**, the speed of the move is doubled, since all memory cycles are used by the move rather than being shared with instruction fetching. Such a hardware implementation of microloops is much faster than conventional software implementation of a comparable function.

OPTIMAL CPU CLOCK SCHEME

The designer of a high speed microprocessor must produce a product which operate over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing. Temperature, voltage, and process all affect transistor propagation delays. Traditional CPU designs are done so that with the worse case of the three parameters, the circuit will function at the rated clock speed. The result are designs that must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse case conditions.

The microprocessor **50** uses the technique shown in FIGS. **17–19** to generate the system clock and its required phases. Clock circuit **430** is the familiar "ring oscillator" used to test process performance. The clock is fabricated on the same silicon chip as the rest of the microprocessor **50**.

The ring oscillator frequency is determined by the parameters of temperature, voltage, and process. At room temperature, the frequency will be in the neighborhood of 100 MHZ. At 70 degrees Centigrade, the speed will be 50 MHZ. The ring oscillator **430** is useful as a system clock, with its stages **431** producing phase 0-phase 3 outputs **433** shown in FIG. **19**, because its performance tracks the parameters which similarly affect all other transistors on the same silicon die. By deriving system timing from the ring

oscillator **430**, CPU **70** will always execute at the maximum frequency possible, but never too fast. For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor **50** will operate slower than normal. Since the microprocessor **50** ring oscillator clock **430** is made from the same transistors on the same die as the latches and gates, it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.

ASYNCHRONOUS/SYNCHRONOUS CPU

Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor **50** provides a dual-clock scheme as shown in FIG. **17**, with the CPU **70** operating a synchronously to I/O interface **432** forming part of memory controller **118** (FIG. **2**) and the I/O interface **432** operating synchronously with the external world of memory and I/O devices. The CPU **70** executes at the fastest speed possible using the adaptive ring counter clock **430**. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor **50** for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface **432**, speed of which is controlled by a conventional crystal clock **434**. The interface **432** processes requests for memory accesses from the microprocessor **50** and acknowledges the presence of I/O data. The microprocessor **50** fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. By decoupling the variable speed of the CPU **70** from the fixed speed of the I/O interface **432**, optimum performance can be achieved by each. Recoupling between the CPU **70** and the interface **432** is accomplished with handshake signals on lines **436**, with data/addresses passing on bus **90**, **136**.

ASYNCHRONOUS/SYNCHRONOUS CPU IMBEDDED ON A DRAM CHIP

System performance is enhanced even more when the DRAM **311** and CPU **314** (FIG. **9**) are located on the same die. The proximity of the transistors means that DRAM **311** and CPU **314** parameters will closely follow each other. At room temperature, not only would the CPU **314** execute at 100 MHZ, but the DRAM **311** would access fast enough to keep up. The synchronization performed by the I/O interface **432** would be for DMA and reading and writing I/O ports. In some systems (such as calculators) no I/O synchronization at all would be required, and the I/O clock would be tied to the ring counter clock.

VARIABLE WIDTH OPERANDS

Many microprocessors provide variable width operands. The microprocessor **50** handles operands of 8, 16, or 24 bits using the same op-code. FIG. **20** shows the 32-bit instruction register **108** and the 2-bit microinstruction register **180** which selects the 8-bit instruction. Two classes of microprocessor **50** instructions can be greater than 8-bits, JUMP class and IMMEDIATE. A JUMP or IMMEDIATE op-code is 8-bits, but the operand can be 8, 16, or 24 bits long. This magic is possible because operands must be right justified in the instruction register. This means that the least significant bit of the operand is always located in the least significant bit of the instruction register. The microinstruction counter **180** selects which 8-bit instruction to execute. If a JUMP or IMMEDIATE instruction is decoded, the state of the 2-bit microinstruction counter selects the required 8, 16, or 24 bit operand onto the address or data bus. The unselected 8-bit bytes are loaded with zeros by operation of decoder **440** and gates **442**. The advantage of this technique is the saving of a number of op-codes required to specify the different operand sizes in other microprocessors.

TRIPLE STACK CACHE

Computer performance is directly related to the system memory bandwidth. The faster the memories, the faster the computer. Fast memories are expensive, so techniques have been developed to move a small amount of high-speed memory around to the memory addresses where it is needed. A large amount of slow memory is constantly updated by the fast memory, giving the appearance of a large fast memory array. A common implementation of the technique is known as a high-speed memory cache. The cache may be thought of as fast acting shock absorber smoothing out the bumps in memory access. When more memory is required than the shock can absorb, it bottoms out and slow speed memory is accessed. Most memory operations can be handled by the shock absorber itself.

The microprocessor **50** architecture has the ALU **80** (FIG. **2**) directly coupled to the top two stack locations **76** and **78**. The access time of the stack **74** therefore directly affects the execution speed of the processor. The microprocessor **50** stack architecture is particularly suitable to a triple cache technique, shown in FIG. **21** which offers the appearance of a large stack memory operating at the speed of on-chip latches **450**. Latches **450** are the fastest form of memory device built on the chip, delivering data in as little as 3 nsec. However latches **450** require large numbers of transistors to construct. On-chip RAM **452** requires fewer transistors than latches, but is slower by a factor of five (15 nsec access). Off-chip RAM **150** is the slowest storage of all. The microprocessor **50** organizes the stack memory hierarchy as three interconnected stacks **450**, **452** and **454**. The latch stack **450** is the fastest and most frequently used. The on-chip RAM stack **452** is next. The off-chip RAM stack **454** is slowest. The stack modulation determines the effective access time of the stack. If a group of stack operations never push or pull more than four consecutive items on the stack, operations will be entirely performed in the 3 nsec latch stack. When the four latches **456** are filled, the data in the bottom of the latch stack **450** is written to the top of the on-chip RAM stack **452**. When the sixteen locations **458** in the on-chip RAM stack **452** are filled, the data in the bottom of the on-chip RAM stack **452** is written to the top of the off-chip RAM stack **454**. When popping data off a full stack **450**, four pops will be performed before stack empty line **460** from the latch stack pointer **462** transfers data from the on-chip RAM stack **452**. By waiting for the latch stack **450** to empty before performing the slower on-chip RAM access, the high effective speed of the latches **456** are made available to the processor. The same approach is employed with the on-chip RAM stack **452** and the off-chip RAM stack **454**.

POLYNOMIAL GENERATION INSTRUCTION

Polynomials are useful for error correction, encryption, data compression, and fractal generation. A polynomial is generated by a sequence of shift and exclusive OR operations. Special chips are provided for this purpose in the prior art.

The microprocessor **50** is able to generate polynomials at high speed without external hardware by slightly modifying how the ALU **80** works. As shown in FIG. **21**, a polynomial is generated by loading the "order" (also known as the feedback terms) into C Register **470**. The value thirty one (resulting in 32 iterations) is loaded into DOWN COUNTER **472**. A register **474** is loaded with zero. B register **476** is loaded with the starting polynomial value. When the POLY

instruction executes, C register **470** is exclusively ORed with A register **474** if the least significant bit of B register **476** is a one. Otherwise, the contents of the A register **474** passes through the ALU **80** unaltered. The combination of A and B is then shifted right (divided by 2) with shifters **478** and **480**. The operation automatically repeats the specified number of iterations, and the resulting polynomial is left in A register **474**.

FAST MULTIPLY

Most microprocessors offer a 16×16 or 32×32 bit multiply instruction. Multiply when performed sequentially takes one shift/add per bit, or 32 cycles for 32 bit data. The microprocessor **50** provides a high speed multiply which allows multiplication by small numbers using only a small number of cycles. FIG. **23** shows the logic used to implement the high speed algorithm. To perform a multiply, the size of the multiplier less one is placed in the DOWN COUNTER **472**. For a four bit multiplier, the number three would be stored in the DOWN COUNTER **472**. Zero is loaded into the A register **474**. The multiplier is written bit reversed into the B Register **476**. For example, a bit reversed five (binary 0101) would be written into B as 1010. The multiplicand is written into the C register **470**. Executing the FAST MULT instruction will leave the result in the A Register **474**, when the count has been completed. The fast multiply instruction is important because many applications scale one number by a much smaller number. The difference in speed between multiplying a 32×32 bit and a 32×4 bit is a factor of 8. If the least significant bit of the multiplier is a "ONE", the contents of the A register **474** and the C register **470** are added. If the least significant bit of the multiplier is a "ZERO", the contents of the A register are passed through the ALU **80** unaltered. The output of the ALU **80** is shifted left by shifter **482** in each iteration. The contents of the B register **476** are shifted right by the shifter **480** in each iteration.

INSTRUCTION EXECUTION PHILOSOPHY

The microprocessor **50** uses high speed D latches in most of the speed critical areas. Slower on-chip RAM is used as secondary storage.

The microprocessor **50** philosophy of instruction execution is to create a hierarchy of speed as follows:

Logic and D latch transfers	1 cycle	20 nsec
Math	2 cycles	40 nsec
Fetch/store on-chip RAM	2 cycles	40 nsec
Fetch/store in current RAS page	4 cycles	80 nsec
Fetch/store with RAS cycle	11 cycles	220 nsec

With a 50 MHZ clock, many operations can be performed in 20 nsec. and almost everything else in 40 nsec.

To maximize speed, certain techniques in processor design have been used. They include:

Eliminating arithmetic operations on addresses,

Fetching up to four instructions per memory cycle,

Pipelineless instruction decoding

Generating results before they are needed,

Use of three level stack caching.

PIPELINE PHILOSOPHY

Computer instructions are usually broken down into sequential pieces, for example: fetch, decode, register read, execute, and store. Each piece will require a single machine cycle. In most Reduced Instruction Set Computer (RISC) chips, instruction require from three to six cycles.

RISC instructions are very parallel. For example, each of 70 different instructions in the SPARC (SUN Computer's RISC chip) has five cycles. Using a technique called "pipelining", the different phases of consecutive instructions can be overlapped.

To understand pipelining, think of building five residential homes. Each home will require in sequence, a foundation, framing, plumbing and wiring, roofing, and interior finish. Assume that each activity takes one week. To build one house will take five weeks.

But what if you want to build an entire subdivision? You have only one of each work crew, but when the foundation men finish on the first house, you immediately start them on the second one, and so on. At the end of five weeks, the first home is complete, but you also have five foundations. If you have kept the framing, plumbing, roofing, and interior guys all busy, from five weeks on, a new house will be completed each week.

This is the way a RISC chip like SPARC appears to execute an instruction in a single machine cycle. In reality, a RISC chip is executing one fifth of five instructions each machine cycle. And if five instructions stay in sequence, an instruction will be completed each machine cycle.

The problems with a pipeline are keeping the pipe full with instructions. Each time an out of sequence instruction such as a BRANCH or CALL occurs, the pipe must be refilled with the next sequence. The resulting dead time to refill the pipeline can become substantial when many IF/THEN/ELSE statements or subroutines are encountered.

THE PIPELINE APPROACH

The microprocessor **50** has no pipeline as such. The approach of this microprocessor to speed is to overlap instruction fetching with execution of the previously fetched instruction(s). Beyond that, over half the instructions (the most common ones) execute entirely in a single machine cycle of 20 nsec. This is possible because:

1. Instruction decoding resolves in 2.5 nsec.
2. Incremented/decremented and some math values are calculated before they are needed, requiring only a latching signal to execute.
3. Slower memory is hidden from high speed operations by high-speed D latches which access in 4 nsec.

The disadvantage for this microprocessor is a more complex chip design process. The advantage for the chip user is faster ultimate throughput since pipeline stalls cannot exist. Pipeline synchronization with availability flag bits and other such pipeline handling is not required by this microprocessor.

For example, in some RISC machines an instruction which tests a status flag may have to wait for up to four cycles for the flag set by the previous instruction to be available to be tested. Hardware and software debugging is also somewhat easier because the user doesn't have to visualize five instructions simultaneously in the pipe.

OVERLAPPING INSTRUCTION FETCH/EXECUTE

The slowest procedure the microprocessor **50** performs is to access memory. Memory is accessed when data is read or written. Memory is also read when instructions are fetched. The microprocessor **50** is able to hide fetch of the next instruction behind the execution of the previously fetched instruction(s). The microprocessor **50** fetches instructions in 4-byte instruction groups. An instruction group may contain from one to four instructions. The amount of time required to execute the instruction group ranges from 4 cycles for simple instructions to 64 cycles for a multiply.

When a new instruction group is fetched, the microprocessor instruction decoder looks at the most significant bit of all four of the bytes. The most significant bit of an instruction determines if a memory access is required. For example, CALL, FETCH, and STORE all require a memory access to

execute. If all four bytes have nonzero most significant bits, the microprocessor initiates the memory fetch of the next sequential 4-byte instruction group. When the last instruction in the group finishes executing, the next 4-byte instruction group is ready and waiting on the data bus needing only to be latched into the instruction register. If the 4-byte instruction group required four or more cycles to execute and the next sequential access was a column address strobe (CAS) cycle, the instruction fetch was completely overlapped with execution.

INTERNAL ARCHITECTURE

The microprocessor **50** architecture consists of the following:

PARAMETER STACK	<---> ALU* <--->	Y REGISTER RETURN STACK
<---32 BITS---> 16 DEEP Used for math and logic.		<---32 BITS---> 16 DEEP Used for subroutine and interrupt return addresses as well as local variables.
Push down stack. Can overflow into off-chip RAM.		Push down stack. Can overflow into off-chip RAM. Can also be accessed relative to top of stack.
LOOP COUNTER	(32-bits, can decrement by 1) Used by class of test and loop instructions.	
X REGISTER	(32-bits, can increment or decrement by 4). Used to point to RAM locations.	
PROGRAM COUNTER	(32-bits, increments by 4). Points to 4-byte instruction groups in RAM.	
INSTRUCTION REG	(32-Bits). Holds 4-byte instruction groups while they are being decoded and executed.	

MODE - A register with mode and status bits.

MODE-BITS:

- Slow down memory accesses by 8 if "1". Run full speed if "0". (Provided for access to slow EPROM.)
- Divide the system clock by 1023 if "1" to reduce power consumption. Run full speed if "0". (On-chip counters slow down if this bit is set.)
- Enable external interrupt 1.
- Enable external interrupt 2.
- Enable external interrupt 3.
- Enable external interrupt 4.
- Enable external interrupt 5.
- Enable external interrupt 6.
- Enable external interrupt 7.

ON-CHIP MEMORY LOCATIONS:

MODE-BITS	
DMA-POINTER	
DMA-COUNTER	
STACK-POINTER	- Pointer into Parameter Stack.
STACK-DEPTH	- Depth of on-chip Parameter Stack
RSTACK-POINTER	- Pointer into Return Stack
RSTACK-DEPTH	- Depth of on-chip Return Stack

*Math and logic operations use the TOP item and NEXT to top Parameter Stack items as the operands. The result is pushed onto the Parameter Stack. *Return addresses from subroutines are placed on the Return Stack. The Y REGISTER is used as a pointer to RAM locations. Since the Y REGISTER is the top item of the Return Stack, nesting of indices is straightforward.

ADDRESSING MODE HIGH POINTS

The data bus is 32-bits wide. All memory fetches and stores are 32-bits. Memory bus addresses are 30 bits. The least significant 2 bits are used to select one-of-four bytes in some addressing modes. The Program Counter, X Register, and Y Register are implemented as D latches with their outputs going to the memory address bus and the bus incrementer/decrementer. Incrementing one of these registers can happen quickly, because the incremented value has already rippled through the inc/dec logic and need only be clocked into the latch. Branches and Calls are made to 32-bit word boundaries.

INSTRUCTION SET

32-BIT INSTRUCTION FORMAT

The thirty two bit instructions are CALL, BRANCH, BRANCH-IF-ZERO, and LOOP-IF-NOT-DONE. These instructions require the calculation of an effective address. In many computers, the effective address is calculated by adding or subtracting an operand with the current Program Counter. This math operation requires from four to seven machine cycles to perform and can definitely bog down machine execution. The microprocessor's strategy is to perform the required math operation at assembly or linking time and do a much simpler "Increment to next page" or "Decrement to previous page" operation at run time. As a result, the microprocessor branches execute in a single cycle.

24-BIT OPERAND FORM:

Byte 1	Byte 2	Byte 3	Byte 4
WWWWWW XX -	YYYYYYYY -	YYYYYYYY -	YYYYYYYY

With a 24-bit operand, the current page is considered to be defined by the most significant 6 bits of the Program Counter.

16-BIT OPERAND FORM: QQQQQQQQ-WWWWWW XX-YYYYYYYY-YYYYYYYY With a 16-bit operand, the current page is considered to be defined by the most significant 14 bits of the Program Counter.

8-BIT OPERAND FORM: QQQQQQQQ-QQQQQQQQ-WWWWWW XX-YYYYYYYY With an 8-bit operand, the current page is considered to be defined by the most significant 22 bits of the Program Counter.

QQQQQQQQ—Any 8-bit instruction.

WWWWWW—Instruction op-code.

XX—Select how the address bits will be used:

00—Make all high-order bits zero. (Page zero addressing)

01—Increment the high-order bits. (Use next page)

10—Decrement the high-order bits. (Use previous page)

11—Leave the high-order bits unchanged. (Use current page)

YYYYYYYY—The address operand field. This field is always shifted left two bits (to generate a word rather than byte address) and loaded into the Program Counter. The microprocessor instruction decoder figures out the width of the operand field by the location of the instruction op-code in the four bytes.

The compiler or assembler will normally use the shortest operand required to reach the desired address so that the leading bytes can be used to hold other instructions. The effective address is calculated by combining:

The current Program Counter,

The 8, 16, or 24 bit address operand in the instruction, Using one of the four allowed addressing modes.

EXAMPLES OF EFFECTIVE ADDRESS CALCULATION

Example 1

Byte 1	Byte 2	Byte 3	Byte 4
QQQQQQQQ	QQQQQQQQ	00000011	10011000

The "QQQQQQQQs" in Byte 1 and 2 indicate space in the 4-byte memory fetch which could be hold two other

instructions to be executed prior to the CALL instruction. Byte 3 indicates a CALL instruction (six zeros) in the current page (indicated by the 11 bits). Byte 4 indicates that the hexadecimal number **98** will be forced into the Program Counter bits **2** through **10**. (Remember, a CALL or BRANCH always goes to a word boundary so the two least significant bits are always set to zero). The effect of this instruction would be to CALL a subroutine at WORD location HEX 98 in the current page. The most significant 22 bits of the Program Counter define the current page and will be unchanged.

Example 2

Byte 1	Byte 2	Byte 3	Byte 4
000001	01	00000001	00000000	00000000

If we assume that the Program Counter was HEX 0000 0156 which is binary:

00000000 00000000 00000001 01010110=OLD PROGRAM COUNTER.

Byte 1 indicates a BRANCH instruction op code (000001) and "01" indicates select the next page. Byte 2,3, and 4 are the address operand. These 24-bits will be shifted to the left two places to define a WORD address. HEX 0156 shifted left two places is HEX 0558. Since this is a 24-bit operand instruction, the most significant 6 bits of the Program Counter define the current page. These six bits will be incremented to select the next page. Executing this instruction will cause the Program Counter to be loaded with HEX 0400 0558 which is binary:

00000100 00000000 00000101 01011000=NEW PROGRAM COUNTER.

INSTRUCTIONS

CALL-LONG

0000 00XX-YYYYYYYY-YYYYYYYY-YYYYYYYY

Load the Program Counter with the effective WORD address specified. Push the current PC contents onto the RETURN STACK.

OTHER EFFECTS: CARRY or modes, no effect. May cause Return Stack to force an external memory cycle if on-chip Return Stack is full.

BRANCH

0000 01XX-YYYYYYYY-YYYYYYYY-YYYYYYYY

Load the Program Counter with the effective WORD address specified.

OTHER EFFECTS: NONE

BRANCH-IF-ZERO

0000 10XX-YYYYYYYY-YYYYYYYY-YYYYYYYY

Test the TOP value on the Parameter Stack. If the value is equal to zero, load the Program Counter with the effective WORD address specified. If the TOP value is not equal to zero, increment the Program Counter and fetch and execute the next instruction.

OTHER EFFECTS: NONE

LOOP-IF-NOT-DONE

0000 11YY-(XXXX XXXX)-(XXXX XXXX)-(XXXX XXXX)

If the LOOP COUNTER is not zero, load the Program Counter with the effective WORD address specified. If the LOOP COUNTER is zero, decrement the LOOP COUNTER, increment the Program Counter and fetch and execute the next instruction.

OTHER EFFECTS: NONE

8-BIT INSTRUCTIONS PHILOSOPHY

Most of the work in the microprocessor **50** is done by the 8-bit instructions. Eight bit instructions are possible with the microprocessor because of the extensive use of implied stack addressing. Many 32-bit architectures use 8-bits to specify the operation to perform but use an additional 24-bits to specify two sources and a destination.

For math and logic operations, the microprocessor **50** exploits the inherent advantage of a stack by designating the source operand(s) as the top stack item and the next stack item. The math or logic operation is performed, the operands are popped from the stack, and the result is pushed back on the stack. The result is a very efficient utilization of instruction bits as well as registers. A comparable situation exists between Hewlett Packard calculators (which use a stack) and Texas Instrument calculators which don't. The identical operation on an HP will require one half to one third the keystrokes of the TI.

The availability of 8-bit instructions also allows another architectural innovation, the fetching of four instructions in a single 32-bit memory cycle. The advantages of fetching multiple instructions are:

Increased execution speed even with slow memories,

Similar performance to the Harvard (separate data and instruction busses) without the expense,

Opportunities to optimize groups of instructions,

The capability to perform loops within this mini-cache.

The microloops inside the four instruction group are effective for searches and block moves.

SKIP INSTRUCTIONS

The microprocessor **50** fetches instructions in 32-bit chunks called 4-byte instruction groups. These four bytes may contain four 8-bit instructions or some mix of 8-bit and 16 or 24-bit instructions. SKIP instructions in the microprocessor skip any remaining instructions in a 4-byte instruction group and cause a memory fetch to get the next 4-byte instruction group. Conditional SKIPs when combined with 3-byte BRANCHES will create conditional BRANCHES. SKIPs may also be used in situations when no use can be made of the remaining bytes in a 4-instruction group. A SKIP executes in a single cycle, whereas a group of three NOPs would take three cycles.

SKIP-ALWAYS—Skip any remaining instructions in this 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group.

SKIP-IF-ZERO—If the TOP item of the Parameter Stack is zero, skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is not zero, execute the next sequential instruction.

SKIP-IF-POSITIVE—If the TOP item of the Parameter Stack has a the most significant bit (the sign bit) equal to "0", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is not "0", execute the next sequential instruction.

SKIP-IF-NO-CARRY—If the CARRY flag from a SHIFT or arithmetic operation is not equal to "1", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the CARRY is equal to "1", execute the next sequential instruction.

SKIP-NEVER (NOP) execute the next sequential instruction. (Delay one machine cycle).

SKIP-IF-NOT-ZERO—If the TOP item on the Parameter Stack is not equal to "0", skip any remaining instructions

in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is equal "0", execute the next sequential instruction.

SKIP-IF-NEGATIVE—If the TOP item on the Parameter Stack has its most significant bit (sign bit) set to "1", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item has its most significant bit set to "0", execute the next sequential instruction.

SKIP-IF-CARRY—If the CARRY flag is set to "1" as a result of SHIFT or arithmetic operation, skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the CARRY flag is "0", execute the next sequential instruction.

MICROLOOPS

Microloops are a unique feature of the microprocessor architecture which allows controlled looping within a 4-byte instruction group. A microloop instruction tests the LOOP COUNTER for "0" and may perform an additional test. If the LOOP COUNTER is not "0" and the test is met, instruction execution continues with the first instruction in the 4-byte instruction group, and the LOOP COUNTER is decremented. A microloop instruction will usually be the last byte in a 4-byte instruction group, but it can be any byte. If the LOOP COUNTER is "0" or the test is not met, instruction execution continues with the next instruction. If the microloop is the last byte in the 4-byte instruction group, the most significant 30-bits of the Program Counter are incremented and the next 4-byte instruction group is fetched from memory. On a termination of the loop on LOOP COUNTER equal to "0", the LOOP COUNTER will remain at "0". Microloops allow short iterative work such as moves and searches to be performed without slowing down to fetch instructions from memory.

EXAMPLE

Byte 1	Byte 2
FETCH-VIA-X-AUTO-INCREMENT	STORE-VIA-Y-AUTOINCREMENT
Byte 3	Byte 4
ULOOP-UNTIL-DONE	QQQQQQQQ

This example will perform a block move. To initiate the transfer, X will be loaded with the starting address of the source. Y will be loaded with the starting address of the destination. The LOOP COUNTER will be loaded with the number of 32-bit words to move. The microloop will FETCH and STORE and count down the LOOP COUNTER until it reaches zero. QQQQQQQQ indicates any instruction can follow.

MICROLOOP INSTRUCTIONS

ULOOP-UNTIL-DONE—If the LOOP COUNTER is not "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0", continue execution with the next instruction.

ULOOP-IF-ZERO—If the LOOP COUNTER is not "0" and the TOP item on the Parameter Stack is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

ULOOP-IF-POSITIVE—If the LOOP COUNTER is not "0" and the most significant bit (sign bit) is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

ULOOP-IF-NOT-CARRY-CLEAR—If the LOOP COUNTER is not "0" and the floating point exponents found in TOP and NEXT are not aligned, continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the exponents are aligned, continue execution with the next instruction. This instruction is specifically designed for combination with special SHIFT instructions to align two floating point numbers.

ULOOP-NEVER—(DECREMENT-LOOP-COUNTER) Decrement the LOOP COUNTER. Continue execution with the next instruction.

ULOOP-IF-NOT-ZERO—If the LOOP COUNTER is not "0" and the TOP item of the Parameter Stack is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

ULOOP-IF-NEGATIVE—If the LOOP COUNTER is not "0" and the most significant bit (sign bit) of the TOP item of the Parameter Stack is "1", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the most significant bit of the Parameter Stack is "0", continue execution with the next instruction.

ULOOP-IF-CARRY-SET—If the LOOP COUNTER is not "0" and the exponents of the floating point numbers found in TOP and NEXT are not aligned, continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the exponents are aligned, continue execution with the next instruction.

RETURN FROM SUBROUTINE OR INTERRUPT

Subroutine calls and interrupt acknowledgements cause a redirection of normal program execution. In both cases, the current Program Counter is pushed onto the Return Stack, so the microprocessor can return to its place in the program after executing the subroutine or interrupt service routine.

NOTE: When a CALL to subroutine or interrupt is acknowledged the Program Counter has already been incremented and is pointing to the 4-byte instruction group following the 4-byte group currently being executed. The instruction decoding logic allows the microprocessor to perform a test and execute a return conditional on the outcome of the test in a single cycle. A RETURN pops an address from the Return Stack and stores it to the Program Counter.

RETURN INSTRUCTIONS

RETURN-ALWAYS—Pop the top item from the Return Stack and transfer it to the Program Counter.

RETURN-IF-ZERO—If the TOP item on the Parameter Stack is "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-POSITIVE—If the most significant bit (sign bit) of the TOP item on the Parameter Stack is a "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-CARRY-CLEAR—If the exponents of the floating point numbers found in TOP and NEXT are not aligned, pop the top item from the Return Stack and

transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-NEVER (NOP)—Execute the next instruction.

RETURN-IF-NOT-ZERO—If the TOP item on the Parameter Stack is not "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-NEGATIVE—If the most significant bit (sign bit) of the TOP item on the Parameter Stack is a "1", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-CARRY-SET—If the exponents of the floating point numbers found in TOP and NEXT are aligned, pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

HANDLING MEMORY FROM DYNAMIC RAM

The microprocessor **50**, like any RISC type architecture, is optimized to handle as many operations as possible on-chip for maximum speed. External memory operations take from 80 nsec. to 220 nsec. compared with on-chip memory speeds of from 4 nsec. to 30 nsec. There are times when external memory must be accessed.

External memory is accessed using three registers:

X-REGISTER—A 30-bit memory pointer which can be used for memory access and simultaneously incremented or decremented.

Y-REGISTER—A 30-bit memory pointer which can be used for memory access and simultaneously incremented or decremented.

PROGRAM-COUNTER—A 30-bit memory pointer normally used to point to 4-byte instruction groups. External memory may be accessed at addresses relative to the PC. The operands are sometimes called "Immediate" or "Literal" in other computers. When used as memory pointer, the PC is also incremented after each operation.

MEMORY LOAD & STORE INSTRUCTIONS

FETCH-VIA-X—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. X is unchanged.

FETCH-VIA-Y—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. Y is unchanged.

FETCH-VIA-X-AUTOINCREMENT—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of X to point to the next 32-bit word address.

FETCH-VIA-Y-AUTOINCREMENT—Fetch the 32-bit memory content pointed to by Y and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of Y to point to the next 32-bit word address.

FETCH-VIA-X-AUTODECREMENT—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. After fetching, decrement the most significant 30 bits of X to point to the previous 32-bit word address.

FETCH-VIA-Y-AUTODECREMENT—Fetch the 32-bit memory content pointed to by Y and push it onto the Parameter Stack. After fetching, decrement the most significant 30 bits of Y to point to the previous 32-bit word address.

STORE-VIA-X—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. X is unchanged.

STORE-VIA-Y—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. Y is unchanged.

STORE-VIA-X-AUTOINCREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. After storing, increment the most significant 30 bits of X to point to the next 32-bit word address.

STORE-VIA-Y-AUTOINCREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. After storing, increment the most significant 30 bits of Y to point to the next 32-bit word address.

STORE-VIA-X-AUTODECREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. After storing, decrement the most significant 30 bits of X to point to the previous 32-bit word address.

STORE-VIA-Y-AUTODECREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. After storing, decrement the most significant 30 bits of Y to point to the previous 32-bit word address.

FETCH-VIA-PC—Fetch the 32-bit memory content pointed to by the Program Counter and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of the Program Counter to point to the next 32-bit word address.

*NOTE When this instruction executes, the PC is pointing to the memory location following the instruction. The effect is of loading a 32-bit immediate operand. This is an 8-bit instruction and therefore will be combined with other 8-bit instructions in a 4-byte instruction fetch. It is possible to have from one to four FETCH-VIA-PC instructions in a 4-byte instruction fetch. The PC increments after each execution of FETCH-VIA-PC, so it is possible to push four immediate operands on the stack. The four operands would be the found in the four memory locations following the instruction.

BYTE-FETCH-VIA-X—Fetch the 32-bit memory content pointed to by the most significant 30 bits of X. Using the two least significant bits of X, select one of four bytes from the 32-bit memory fetch, right justify the byte in a 32-bit field and push the selected byte preceded by leading zeros onto the Parameter Stack.

BYTE-STORE-VIA-X—Fetch the 32-bit memory content pointed to by the most significant 30 bits of X. Pop the TOP item from the Parameter Stack. Using the two least significant bits of X place the least significant byte into the 32-bit memory data and write the 32-bit entity back to the location pointed to by the most significant 30 bits of X.

OTHER EFFECTS OF MEMORY ACCESS INSTRUCTIONS:

Any FETCH instruction will push a value on the Parameter Stack **74**. If the on-chip stack is full, the stack will overflow into off-chip memory stack resulting in an additional memory cycle. Any STORE instruction will pop a value from the Parameter Stack **74**. If the on-chip stack is empty, a memory cycle will be generated to fetch a value from off-chip memory stack.

HANDLING ON-CHIP VARIABLES

High-level languages often allow the creation of LOCAL VARIABLES. These variables are used by a particular procedure and discarded. In cases of nested procedures, layers of these variables must be maintained. On-chip storage is up to five times faster than off-chip RAM, so a means of keeping local variables on-chip can make operations run faster. The microprocessor **50** provides the capability for both on-chip storage of local variables and nesting of multiple levels of variables through the Return Stack.

The Return Stack **134** is implemented as 16 on-chip RAM locations. The most common use for the Return Stack **134** is storage of return addresses from subroutines and interrupt calls. The microprocessor allows these 16 locations to also be used as addressable registers. The 16 locations may be read and written by two instructions which indicate a Return Stack relative address from 0–15. When high-level procedures are nested, the current procedure variables push the previous procedure variables further down the Return Stack **134**. Eventually, the Return Stack will automatically overflow into off-chip RAM.

ON-CHIP VARIABLE INSTRUCTIONS

READ-LOCAL-VARIABLE XXXX—Read the XXXXth location relative to the top of the Return Stack. (XXXX is a binary number from 0000–1111). Push the item read onto the Parameter Stack.

OTHER EFFECTS: If the Parameter Stack is full, the push operation will cause a memory cycle to be generated as one item of the stack is automatically stored to external RAM. The logic which selects the location performs a modulo **16** subtraction. If four local variables have been pushed onto the Return Stack, and an instruction attempts to READ the fifth item, unknown data will be returned.

WRITE-LOCAL-VARIABLE XXXX—Pop the TOP item of the Parameter Stack and write it into the XXXXth location relative to the top of the Return Stack. (XXXX is a binary number from 0000–1111.)

OTHER EFFECTS: If the Parameter Stack is empty, the pop operation will cause a memory cycle to be generated to fetch the Parameter Stack item from external RAM. The logic which selects the location performs a modulo **16** subtraction. If four local variables have been pushed onto the Return Stack, and an instruction attempts to WRITE to the fifth item, it is possible to clobber return addresses or wreak other havoc.

REGISTER AND FLIP-FLOP TRANSFER AND PUSH INSTRUCTIONS

DROP—Pop the TOP item from the Parameter Stack and discard it.

SWAP—Exchange the data in the TOP Parameter Stack location with the data in the NEXT Parameter Stack location.

DUP—Duplicate the TOP item on the Parameter Stack and push it onto the Parameter Stack.

PUSH-LOOP-COUNTER—Push the value in LOOP COUNTER onto the Parameter Stack.

POP-RSTACK-PUSH-TO-STACK—Pop the top item from the Return Stack and push it onto the Parameter Stack.

PUSH-X-REG—Push the value in the X Register onto the Parameter Stack.

PUSH-STACK-POINTER—Push the value of the Parameter Stack pointer onto the Parameter Stack.

PUSH-RSTACK-POINTER—Push the value of the Return Stack pointer onto the Return Stack.

PUSH-MODE-BITS—Push the value of the MODE REGISTER onto the Parameter Stack.

PUSH-INPUT—Read the 10 dedicated input bits and push the value (right justified and padded with leading zeros) onto the Parameter Stack.

SET-LOOP-COUNTER—Pop the TOP value from the Parameter Stack and store it into LOOP COUNTER.

POP-STACK-PUSH-TO-RSTACK—Pop the TOP item from the Parameter Stack and push it onto the Return Stack.

SET-X-REG—Pop the TOP item from the Parameter Stack and store it into the X Register.

SET-STACK-POINTER—Pop the TOP item from the Parameter Stack and store it into the Stack Pointer.

SET-RSTACK-POINTER—Pop the TOP item from the Parameter

Stack and store it into the Return Stack Pointer.

SET-MODE-BITS—Pop the TOP value from the Parameter Stack and store it into the MODE BITS.

SET-OUTPUT—Pop the TOP item from the Parameter Stack and output it to the 10 dedicated output bits.

OTHER EFFECTS: Instructions which push or pop the Parameter Stack or Return Stack may cause a memory cycle as the stacks overflow back and forth between on-chip and off-chip memory.

LOADING A SHORT LITERAL

A special case of register transfer instruction is used to push an 8-bit literal onto the Parameter Stack. This instruction requires that the 8-bits to be pushed reside in the last byte of a 4-byte instruction group. The instruction op-code loading the literal may reside in ANY of the other three bytes in the instruction group.

EXAMPLE

BYTE 1 LOAD-SHORT-LITERAL BYTE 4 00001111	BYTE 2 QQQQQQQQ	BYTE 3 QQQQQQQQ

In this example, QQQQQQQQ indicates any other 8-bit instruction. When Byte 1 is executed, binary 00001111(HEX 0f) from Byte 4 will be pushed (right justified and padded by leading zeros) onto the Parameter Stack. Then the instructions in Byte 2 and Byte 3 will execute. The microprocessor instruction decoder knows not to execute Byte 4. It is possible to push three identical 8-bit values as follows:

BYTE 1 LOAD-SHORT-LITERAL BYTE 3 LOAD-SHORT-LITERAL SHORT-LITERAL-INSTRUCTION	BYTE 2 LOAD-SHORT-LITERAL BYTE 4 00001111

LOAD-SHORT-LITERAL—Push the 8-bit value found in Byte 4 of the current 4-byte instruction group onto the Parameter Stack.

LOGIC INSTRUCTIONS

Logical and math operations used the stack for the source of one or two operands and as the destination for results. The stack organization is a particularly convenient arrangement for evaluating expressions. TOP indicates the top value on the Parameter Stack **74**. NEXT indicates the next to top value on the Parameter Stack **74**.

AND—Pop TOP and NEXT from the Parameter Stack, perform the logical AND operation on these two operands, and push the result onto the Parameter Stack.

OR—Pop TOP and NEXT from the Parameter Stack, perform the logical OR operation on these two operands, and push the result onto the Parameter Stack.

XOR—Pop TOP and NEXT from the Parameter Stack, perform the logical exclusive OR on these two operands, and push the result onto the Parameter Stack.

BIT-CLEAR—Pop TOP and NEXT from the Parameter Stack, toggle all bits in NEXT, perform the logical AND operation on TOP, and push the result onto the Parameter Stack. (Another way of understanding this instruction is thinking of it as clearing all bits in TOP that are set in NEXT.)

MATH INSTRUCTIONS

Math instruction pop the TOP item and NEXT to top item of the Parameter Stack **74** to use as the operands. The results are pushed back on the Parameter Stack. The CARRY flag is used to latch the "33rd bit" of the ALU result.

ADD—Pop the TOP item and NEXT to top item from the Parameter Stack, add the values together and push the result back on the Parameter Stack. The CARRY flag may be changed.

ADD-WITH-CARRY—Pop the TOP item and the NEXT to top item from the Parameter Stack, add the values together. If the CARRY flag is "1" increment the result. Push the ultimate result back on the Parameter Stack. The CARRY flag may be changed.

ADD-X—Pop the TOP item from the Parameter Stack and read the third item from the top of the Parameter Stack. Add the values together and push the result back on the Parameter Stack. The CARRY flag may be changed.

SUB—Pop the TOP item and NEXT to top item from the Parameter Stack, Subtract NEXT from TOP and push the result back on the Parameter Stack. The CARRY flag may be changed.

SUB-WITH-CARRY—Pop the TOP item and NEXT to top item from the Parameter Stack. Subtract NEXT from TOP. If the CARRY flag is "1" increment the result. Push the ultimate result back on the Parameter Stack. The CARRY flag may be changed.

SUB-X—

SIGNED-MULT-STEP—

UNSIGNED-MULT-STEP—

SIGNED-FAST-MULT—

FAST-MULT-STEP—

UNSIGNED-DIV-STEP—

GENERATE-POLYNOMIAL—

ROUND—

COMPARE—Pop the TOP item and NEXT to top item from the Parameter Stack. Subtract NEXT from TOP. If the result has the most significant bit equal to "0" (the result is positive), push the result onto the Parameter Stack. If the result has the most significant bit equal to "1" (the result is negative), push the old value of TOP onto the Parameter Stack. The CARRY flag may be affected.

SHIFT/ROTATE

SHIFT-LEFT—Shift the TOP Parameter Stack item left one bit. The CARRY flag is shifted into the least significant bit of TOP.

SHIFT-RIGHT—Shift the TOP Parameter Stack item right one bit. The least significant bit of TOP is shifted into the CARRY flag. Zero is shifted into the most significant bit of TOP.

DOUBLE-SHIFT-LEFT—Treating the TOP item of the Parameter Stack as the most significant word of a 64-bit number and the NEXT stack item as the least significant word, shift the combined 64-bit entity left one bit. The CARRY flag is shifted into the least significant bit of NEXT.

DOUBLE-SHIFT-RIGHT—Treating the TOP item of the Parameter Stack as the most significant word of a 64-bit number and the NEXT stack item as the least significant word, shift the combined 64-bit entity right one bit. The least significant bit of NEXT is shifted into the CARRY flag. Zero is shifted into the most significant bit of TOP.

OTHER INSTRUCTIONS

FLUSH-STACK—Empty all on-chip Parameter Stack locations into off-chip RAM. (This instruction is useful for multitasking applications). This instruction accesses a counter which holds the depth of the on-chip stack and can require from none to 16 external memory cycles.

FLUSH-RSTACK—Empty all on-chip Return Stack locations into off-chip RAM. (This instruction is useful for multitasking applications). This instruction accesses a counter which holds the depth of the on-chip Return Stack and can require from none to 16 external memory cycles.

It should further be apparent to those skilled in the art that various changes in form and details of the invention as shown and described may be made. It is intended that such changes be included within the spirit and scope of the claims appended hereto.

What is claimed is:

1. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.

2. The microprocessor system of claim **1** in which said second clock is a fixed frequency clock.

3. In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:

providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;

using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;

providing an on chip input/output interface for the microprocessor integrated circuit; and

clocking the input/output interface with a second clock independent of the ring oscillator system clock.

4. The method of claim **3** in which the second clock is a fixed frequency clock.

5. The method of claim **3** further including the step of:

transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.

6. A microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and

the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;

an on-chip input/output interface, connected between said said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

7. The microprocessor system of claim **6** wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

8. The microprocessor system of claim **6** wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.

9. The microprocessor system of claim **6** wherein said oscillator comprises a ring oscillator.

10. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

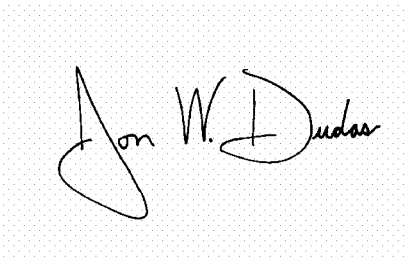
PATENT NO. : 5,809,336
APPLICATION NO. : 08/484918
DATED : September 15, 1998
INVENTOR(S) : Moore et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 34,
Line 25, delete "oscillator" and insert --variable speed clock--.

Signed and Sealed this

Twenty-second Day of May, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office

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(12) EX PARTE REEXAMINATION CERTIFICATE (7235th)

United States Patent
Moore et al.

(10) **Number: US 5,809,336 C1**
(45) **Certificate Issued: Dec. 15, 2009**

(54) **HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK**

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(73) Assignee: **Patriot Scientific Corporation**, San Diego, CA (US)

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(51) **Int. Cl.**

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G06F 7/78	(2006.01)
G06F 9/30	(2006.01)
G06F 9/32	(2006.01)
G06F 15/76	(2006.01)
G06F 15/78	(2006.01)
G06F 7/52	(2006.01)
G06F 9/38	(2006.01)
G06F 7/58	(2006.01)

(52) **U.S. Cl.** **710/25**; 711/E12.02; 712/E9.016; 712/E9.028; 712/E9.046; 712/E9.055; 712/E9.057; 712/E9.058; 712/E9.062; 712/E9.078; 712/E9.08; 712/E9.081

(58) **Field of Classification Search** ..... None
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,603,934	A	9/1971	Heath, Jr. et al.
3,696,414	A	10/1972	Allen et al.
3,849,765	A	11/1974	Hamano
3,878,513	A	4/1975	Werner
3,919,695	A	11/1975	Gooding
3,924,245	A	12/1975	Eaton et al.

(Continued)

FOREIGN PATENT DOCUMENTS

EP	0 200 797	A1	11/1986
EP	0 208 287		1/1987
EP	113 516	B1	6/1988

(Continued)

OTHER PUBLICATIONS

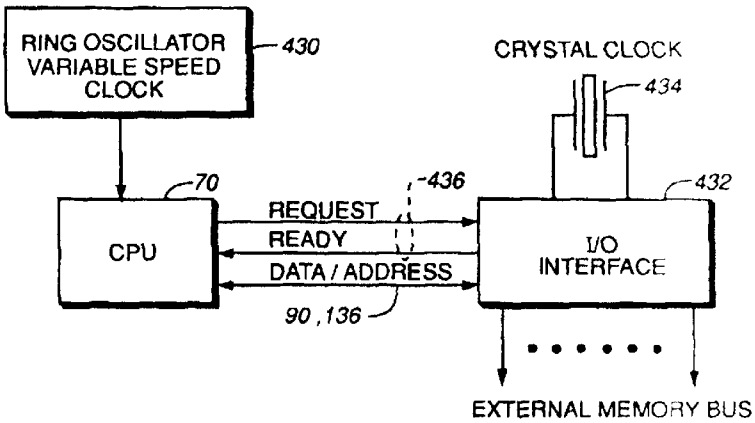
Memorandum Opinion and Order filed Jun. 15, 2007 in 2:05–CV–494 (TJW).
Plaintiffs Technology Property Limited's and Patriot Scientific Corporation's Claim Construction Brief filed Mar. 19, 2007 in 2:05–CV–494 (TJW).

(Continued)

Primary Examiner—Sam Rimell

(57) **ABSTRACT**

A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.



U.S. PATENT DOCUMENTS

3,967,104	A	6/1976	Brantingham et al.
3,968,501	A	7/1976	Gilbert
3,976,977	A	8/1976	Porter et al.
3,980,993	A	9/1976	Bredart et al.
4,003,028	A	1/1977	Bennett et al.
4,003,033	A	1/1977	O'Keefe et al.
4,037,090	A	7/1977	Raymond, Jr.
4,042,972	A	8/1977	Gruner et al.
4,050,058	A	9/1977	Garlic
4,050,096	A	9/1977	Bennett et al.
4,067,058	A	1/1978	Brandstaetter et al.
4,067,059	A	1/1978	Derchak
4,075,691	A	2/1978	Davis et al.
4,079,455	A	3/1978	Ozga
4,107,773	A	8/1978	Gilbreath et al.
4,110,822	A	8/1978	Porter et al.
4,112,490	A	9/1978	Pohlman et al.
4,125,871	A	11/1978	Martin
4,128,873	A	12/1978	Lamiaux
4,144,562	A	3/1979	Cooper
4,217,637	A	8/1980	Faulkner et al.
4,223,380	A	9/1980	Antonaccio et al.
4,223,880	A	9/1980	Brems
4,224,676	A	9/1980	Appelt
4,236,152	A	11/1980	Masuzawa et al.
4,242,735	A	12/1980	Sexton
4,253,785	A	3/1981	Bronstein
4,255,785	A	3/1981	Chamberlin
4,292,668	A	9/1981	Miller et al.
4,295,193	A	10/1981	Pomerene
4,305,045	A	12/1981	Metz et al.
4,315,305	A	2/1982	Siemon
4,315,308	A	2/1982	Jackson
4,317,227	A	2/1982	Skerlos
4,320,467	A	3/1982	Glass
4,321,706	A	3/1982	Craft
4,328,557	A	5/1982	Gastinel
4,334,268	A	6/1982	Boney et al.
4,335,447	A	6/1982	Jerrim
4,338,675	A	7/1982	Palmer et al.
4,348,720	A	9/1982	Blahut et al.
4,348,743	A	9/1982	Dozier
4,354,228	A	10/1982	Moore et al.
4,358,728	A	11/1982	Hashimoto
4,361,869	A	11/1982	Johnson et al.
4,364,112	A	12/1982	Onodera et al.
4,376,977	A	3/1983	Bruinshorst
4,382,279	A	5/1983	Ugon
4,390,946	A	6/1983	Lane
4,396,979	A	8/1983	Mor et al.
4,398,263	A	8/1983	Ito
4,398,265	A	8/1983	Puhl et al.
4,402,042	A	8/1983	Guttag
4,403,303	A	9/1983	Howes et al.
4,412,283	A	10/1983	Mor et al.
4,425,628	A	1/1984	Bedard et al.
4,449,201	A	5/1984	Clark
4,450,519	A	5/1984	Guttag et al.
4,462,073	A	7/1984	Grondalski
4,463,421	A	7/1984	Laws
4,467,810	A	8/1984	Vollmann
4,471,426	A	9/1984	McDonough
4,472,789	A	9/1984	Sibley
4,488,217	A	12/1984	Binder et al.
4,494,021	A	1/1985	Bell et al.
4,509,115	A	4/1985	Manton et al.
4,538,239	A	8/1985	Magar
4,539,655	A	9/1985	Trussell et al.
4,541,045	A	9/1985	Kromer, III
4,541,111	A	9/1985	Takashima et al.
4,553,201	A	11/1985	Pollack et al.
4,556,063	A	12/1985	Thompson et al.
4,562,537	A	12/1985	Barnett et al.
4,566,063	A	1/1986	Zolnowsky
4,577,282	A	3/1986	Caudel et al.
4,607,332	A	8/1986	Goldberg
4,616,338	A	10/1986	Helen et al.
4,626,798	A	12/1986	Fried
4,626,985	A	12/1986	Briggs
4,626,988	A	12/1986	George
4,627,082	A	12/1986	Pelgrom et al.
4,630,195	A	12/1986	Hester et al.
4,630,934	A	12/1986	Arber
4,641,246	A	2/1987	Halbert et al.
4,649,471	A	3/1987	Briggs et al.
4,660,155	A	4/1987	Thaden et al.
4,660,180	A	4/1987	Tanimura et al.
4,665,495	A	5/1987	Thaden
4,670,837	A	6/1987	Sheets
4,679,166	A	7/1987	Berger et al.
4,680,698	A	7/1987	Edwards et al.
4,689,581	A	8/1987	Talbot
4,691,124	A	9/1987	Ledzius et al.
4,698,750	A	10/1987	Wilkie et al.
4,701,884	A	10/1987	Aoki et al.
4,704,678	A	11/1987	May
4,708,490	A	11/1987	Arber
4,709,329	A	11/1987	Hecker
4,710,648	A	12/1987	Hanamura et al.
4,713,749	A	12/1987	Magar et al.
4,714,994	A	12/1987	Oklobdzija
4,720,812	A	1/1988	Kao et al.
4,724,517	A	2/1988	May
4,739,475	A	4/1988	Mensch, Jr.
4,750,111	A	6/1988	Crosby, Jr. et al.
4,758,948	A	7/1988	May et al.
4,760,521	A	7/1988	Rehwald et al.
4,761,763	A	8/1988	Hicks
4,763,297	A	8/1988	Uhlenhoff
4,766,567	A	8/1988	Kato
4,772,888	A	9/1988	Kimura
4,777,591	A	10/1988	Chang et al.
4,780,814	A	10/1988	Hayek
4,783,734	A	11/1988	May et al.
4,787,032	A	11/1988	Culley
4,794,526	A	12/1988	May et al.
4,797,850	A	1/1989	Amitai
4,803,621	A	2/1989	Kelly
4,805,091	A	2/1989	Thiel et al.
4,809,169	A	2/1989	Sfarti et al.
4,809,269	A	2/1989	Gulick
4,811,208	A	3/1989	Myers et al.
4,816,989	A	3/1989	Finn et al.
4,816,996	A	3/1989	Hill et al.
4,819,151	A	4/1989	May
4,833,599	A	5/1989	Colwell et al.
4,835,738	A	5/1989	Niehaus et al.
4,837,563	A	6/1989	Mansfield et al.
4,837,682	A	6/1989	Culler
4,853,841	A	8/1989	Richter
4,860,198	A	8/1989	Takenaka
4,868,735	A	9/1989	Moller et al.
4,870,562	A	9/1989	Kimoto et al.
4,872,003	A	10/1989	Yoshida
4,882,710	A	11/1989	Hashimoto et al.
4,890,225	A	12/1989	Ellis, Jr. et al.
4,899,275	A	2/1990	Sachs et al.
4,907,225	A	3/1990	Gulick et al.
4,910,703	A	3/1990	Ikeda et al.
4,912,632	A	3/1990	Gach et al.
4,914,578	A	4/1990	MacGregor et al.

4,926,323	A	5/1990	Baror et al.
4,931,748	A	6/1990	McDermott et al.
4,931,986	A	6/1990	Daniel et al.
4,933,835	A	6/1990	Sachs
4,942,553	A	7/1990	Dalrymple et al.
4,956,811	A	9/1990	Kajigaya et al.
4,959,782	A	9/1990	Tulpule et al.
4,967,326	A	10/1990	May
4,967,352	A	10/1990	Keida et al.
4,967,398	A	10/1990	Jamoua et al.
4,974,157	A	11/1990	Winfield et al.
4,979,102	A	12/1990	Tokuume
4,980,821	A	12/1990	Koopman et al.
4,988,892	A	1/1991	Needle
4,989,113	A	1/1991	Asal
4,989,133	A	1/1991	May et al.
4,989,135	A	1/1991	Miki
4,990,847	A	2/1991	Ishimaru et al.
5,008,816	A	4/1991	Fogg, Jr. et al.
5,013,985	A	5/1991	Itoh et al.
5,021,991	A	6/1991	MacGregor et al.
5,022,395	A	6/1991	Russie
5,023,689	A	6/1991	Sugawara
5,031,092	A	7/1991	Edwards et al.
5,036,300	A	7/1991	Nicolai
5,036,460	A	7/1991	Takahira et al.
5,047,921	A	9/1991	Kinter et al.
5,053,952	A	10/1991	Koopman, Jr. et al.
5,068,781	A	11/1991	Gillett, Jr. et al.
5,070,451	A	12/1991	Moore et al.
5,081,574	A	1/1992	Larsen et al.
5,091,846	A	2/1992	Sachs et al.
5,097,437	A	3/1992	Larson et al.
5,103,499	A	4/1992	Miner et al.
5,109,495	A	4/1992	Fite et al.
5,121,502	A	6/1992	Rau et al.
5,127,091	A	6/1992	Boufarah et al.
5,127,092	A	6/1992	Gupta et al.
5,134,701	A	7/1992	Mueller et al.
5,146,592	A	9/1992	Pfeiffer et al.
5,148,385	A	9/1992	Frazier
5,157,772	A	10/1992	Watanabe
5,179,689	A	1/1993	Leach et al.
5,179,734	A	1/1993	Candy et al.
5,226,147	A	7/1993	Fujishima et al.
5,237,699	A	8/1993	Little et al.
5,239,631	A	8/1993	Boury et al.
5,241,636	A	8/1993	Kohn
5,261,057	A	11/1993	Coyle et al.
5,261,082	A	11/1993	Ito et al.
5,261,109	A	11/1993	Cadambi et al.
5,325,513	A	6/1994	Tanaka et al.
5,339,448	A	8/1994	Tanaka et al.
5,353,417	A	10/1994	Fuoco et al.
5,353,427	A	10/1994	Fujishima et al.
5,379,438	A	1/1995	Bell et al.
5,410,654	A	4/1995	Foster et al.
5,410,682	A	4/1995	Sites et al.
5,414,862	A	5/1995	Suzuki et al.
5,421,000	A	5/1995	Fortino et al.
5,440,749	A	8/1995	Moore et al.
5,459,846	A	10/1995	Hyatt
5,511,209	A	4/1996	Mensch, Jr.
5,530,890	A	6/1996	Moore et al.
5,537,565	A	7/1996	Hyatt
5,604,915	A	2/1997	Moore et al.
5,659,703	A	8/1997	Moore et al.
5,784,584	A	7/1998	Moore et al.
6,598,148	B1	7/2003	Moore et al.

FOREIGN PATENT DOCUMENTS

EP	0288649		11/1988
JP	58-25710	A	2/1983
JP	61-127228	A	6/1984
JP	61-138356	A	6/1986
JP	62-145413		6/1987
JP	05-189383		7/1998

OTHER PUBLICATIONS

Defendants' Brief Regarding Construction of Disputed Claim Terms of the 336 and 148 Patents filed Apr. 2, 2007 in 2:05–CV–494 (TJW).

Defendants' Brief Regarding Construction of Disputed Claim Terms of the 584 Patent filed Apr. 2, 2007 in 2:05–CV–494 (TJW).

Plaintiffs' Claim Construction Reply Brief filed Apr. 9, 2007 in 2:05–CV–494 (TJW).

Defendants' Unopposed Motion for Leave to File a Sur–Reply Brief Regarding Claim Construction filed Apr. 19, 2007 in 2:05–CV–494 (TJW).

Defendants' Sur–Reply Brief Regarding Construction of Disputed Claim Terms of the 336 Patent filed Apr. 29, 2007 in 2:05–CV–494 (TJW).

Declaration of Roger L. Cook in Support of Plaintiffs Technology Property Limited's and Patriot Scientific Corporations's Claim Construction Brief filed Mar. 19, 2007 in 2:05–CV–00494 (TJW).

Supplemental Declaration of Roger L. Cook in Support of Plaintiffs Technology Property Limited's and Patriot Scientific Corporations's Claim Construction Brief filed Apr. 9, 2007 in 2:05–CV–00494 (TJW).

Declaration of David J. Lender filed Apr. 2, 2007 in 2:05–CV–00494 (TJW).

Supplemental Declaration of Alvin M. Despain in Support of Plaintiffs' Reply Claim Construction Brief filed Apr. 9, 2007 in 2:05–CV–0049 (TJW).

Declaration of Alvin M. Despain in Support of Plaintiffs' Claim Construction Brief filed Mar. 19, 2007 in 2:05–CV–00494 (TJW).

Nakamura et al., "Microprocessors—Special Purpose," 1987 IEEE International Solid–State Circuits Conference, Feb. 26, 1987.

Transputer Reference Manual, INMOS Limited 1988.

Horwitz et al., "A 20–MIPS Peak, 32–bit Microprocessor with On–Chip Cache," *IEEE Journal of Solid State Circuits*, SC–22(5):790–799 (Oct. 1987).

Submicron Systems Architecture Project, Caltech Computer Science Technical Report, Nov. 1, 1991.

Stevens, C. W., "The Transputer," *IEEE*, pp. 292–300 (1985).

Bosshart et al., "A 533K–Transistor LISP Processor Chip", *IEEE Journal of Solid State Circuits*, SC–22(5): 808–819 (Oct. 1987).

Jguppi et al., "A 20 Mips Sustained 32b CMOS with 64b Data Bus," *IEEE Int'l Solid State Circuits Conf.*, pp. 84–86 (1989).

May, D., "The Influence of VLSI Technology on Computer Architecture," pp. 247–256.

"Motorola MC68HC11A8 HCMOS Single–Chip Microcomputer," table of contents and introduction (1985).

"Motorola MC146805H2, advance information," pp. 1–12.

"MC68332 32–Bit Microcontroller System Integration User's Manual Preliminary Edition, Revision 0.8," (1989).

The Ring Oscillator VCO Schematic.

"INMOS T800 Transputer Data Sheet," (Apr. 1987).
"INMOS T414 Transputer Preliminary Data Sheet," (Feb. 1987).
"INMOS T212 Transputer Preliminary Data Sheet," (Aug. 1987).
"INMOS M212 Disk Processor Product Overview," (Oct. 1987).
Budinich et al., eds. *International Conference on the Impact of Digital Microelectronics & Microprocessors on Particle Physics*, pp. 204–213 (1988).
INMOS Presentation given at Jun. 15, 1988 Workshop on Computer Architecture.
Moore, P., "INMOS Technical Note 15: IMS B005 Design of a Disk Controller board with drives," Dec. 3, 1986.
Matthys R. J., *Crystal Oscillator Circuits*, pp. 25–64 (1983).
Elliot et al., eds. *Scientific Applications of Multiprocessors* Prentice Hall (1988).
Transputer Reference Manual, Cover page, Introduction and pp. 73and 96, INMOS Limited (1988).
"INMOS IMS T414 Transputer," (Jun. 1987).
"INMOS IMS T414 Engineering Data," pp. 107–163.
"INMOS Engineering Data, IMS T414M Transputer, Extended Temperature," (Aug. 1987).
"SM550 High Speed CMOS 4–bit Microcomputer SM–550 Series," (1982) document in Japanese.
"MC88100 RISC Microprocessor User's Manual," Motorola (1989).
Mead et al., eds., *Introduction of VLSI Systems*, Addison Wesley Publishers, (1980).
Moelands, A. P. M., "Serial I/O with the MA B8400 series microcomputers," *Electronic Components and Applications*, 3(1):38–46 (1980).
Stanley, R. C., "Microprocessors in brief," *IBM J. Res. Develop.*, 29(2):110–118 (Mar. 1985).
"MC68332 User's Manual," Motorola (1995).
"TMS370 Microcontroller Family User's Guide," Texas Instruments (1996).
"INMOS Preliminary Data IMS T800 transputer," (Apr. 1987).
"INMOS Engineering Data IMS T212 transputer Preliminary," (Aug. 1987).
"INMOS Product Overview IMS M212 disc processor," (Oct. 1987).
"MN18882 LSI User's Manual," (document in Japanese).
"MN1880 (MN18882) Instruction Manual," (document in Japanese).
"MN188166 User's Manual," (document in Japanese).
Paker, Y., *Multi–Processor Systems*, pp. 1–23 (1983).
"HP Sacajawea External Reference Specification Preliminary Version 1.1," (Jan. 14, 1987).
"Data sheet MOS Integrated Circuit uPD75008," NEC (1989).
Product Brochure by Motorola for MC146805H2.
Shyam, M., "Hardware External Reference Specification for Enhanced Champion/Paladin," Revision of Nov. 11, 1986.
Fish deposition transcript, vols. 1 and 2, held Jun. 25, 2007 and Jun. 26, 2007 in case No. 2–05CV–494 (TJW).
Exhibit 4 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); memo of Sep. 12, 1992 Fish to Higgins re: ShBoom Patents.
Exhibit 5 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Sep. 11, 1992 Higgins to Falk re: patent application for High Performance Low Cost Microprocessor.
Exhibit 6 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Sep. 30, 1992 Higgins to Falk re: patent application for High Performance Low Cost Microprocessor.
Exhibit 8 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Mostek 1981 3870/F8 Microcomputer Data Book (1981).
Exhibit 9 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); "IC Master 1980", pp. 2016–2040, published by Fairchild (1980).
Exhibit 10 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of May 12, 1992, Fish to Higgens.
Exhibit 12 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Agreement executed Jan. 3, 1989 between PTA Inc. and Chuck Moore, dba Computer Cowboys.
Exhibit 13 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Oki japan MSH–Boom 96000 Schematic (Jul. 13, 1989).
Exhibit 14 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Assignment of U.S. Appl. No. 07/389,334 from Fish to Fish Family Trust.
Exhibit 15 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Stock Purchase and Technology Transfer Agreement between Fish Family Trust, Helmut Falk, and Nanotronics Corporation (Aug. 16, 1991).
Exhibit 16 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); fax of Jul. 16, 2004Mmarshall to Suanders and Heptig w/ attached Jul. 15, 2004 memo from Beatie re: Fish and Moore.
Exhibit 17 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Fax of Jul. 29, 2004, Heptig to Marshall with attached executed agreement.
Exhibit 18 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Plaintiffs' Second Amended Complaint filed Sep. 22, 2006 in 3:06–CV–00815.
Exhibit 19 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Settlement Agreement between Patriot Scientific Corporation, Fish, and the trustee of Fish Family Trust.
Exhibit 21 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Comparisons of RISC Chips (Dec. 11, 1988).
Exhibit 22 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); VL86C010 An Affordable 32–bit RISC Microprocessor System, VLSI Technology, Inc.
Exhibit 23 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); VY86Cxxx ARM 32–Bit CMOS product literature, EDN (Nov. 21, 1991).
Exhibit 24 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Apr. 26, 1989 Ireland to Fish w/ copy of Apr. 17, 1989 article in Electronic News titled "35ns 256K Device, VLSI Debuts SRAM Designed With Hitachi,".
Exhibit 28 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Introduction to RISC Technology, LSI Logic Corporation (Apr. 1988).
Exhibit 29 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); "SH–Boom Patent Documentation," (Jun. 21, 1989).
Exhibit 30 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); "Sh–Boom Licensing Strategy," (Jan. 19, 1990).

Exhibit 31 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); "Transputer Includes Multiprocessing protocol," Jan. 2, 1991.
Exhibit 32 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); article titled "INMOS details next Transputer," (Apr. 18, 1991).
Exhibit 33 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Articles from Electronic World News.
Exhibit 35 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); INMOS Preliminary Data IMS T414 transputer.
Exhibit 36 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Comparison of Intel 80960 and Sh–Boom Microprocessors (1989).
Exhibit 37 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Memo of Jul. 13, 1989, Fish to Chu w/ attached comparison of MIPS 2000 to Sh–Boom.
Exhibit 38 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); fax of Jun. 10, 1992 Fish to Higgins w/ attached document titled State of the Prior Art ShBoom Microprocessor.
Exhibit 39 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Apr. 12, 1989 Time and Responsibility Schedule.
Exhibit 40 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); handwritten note.
Exhibit 41 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); memo of Jun. 1989 to PT Acquisitions, Inc. re: fees due for searches conducted.
Exhibit 42 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); memo of Jun. 28, 1992 Fish to Higgins re: Dialog Patents re: ShBoom.
Exhibit 43 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Aug. 6, 1998 Haerr to Turner transmitting documents.
Exhibit 44 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Declaration of Moore re: U.S. Appl. No. 08/484,918.
Exhibit 45 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); fax of Nov. 3, 1989, Leckrone to Fish with attached draft license agreement between PT Acquisitions and Oki Electric Industries.
Exhibit 46 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Nov. 29, 1989 Fish to Slater re: Japanese "borrowing" Sh–Boom 50 MHz RISC Chip.
Exhibit 47 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Dec. 29, 1989 Leckrone to Fish re: ShBoom project.
Exhibit 48 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Jul. 16, 1990 Fish to Leckron re: attorney client relationship and conflict of interest.
Exhibit 49 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Jul. 24, 1990 Leckrone to Fish re: letter of Jul. 16, 1990 (EX 48).
Exhibit 50 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Aug. 27, 1990 Moore to Fish re: ShBoom confidentiality.
Exhibit51 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); PT Acquisitions / Alliance Semiconductor Corp. Manufacturing Agreement (Jul. 20 1990).
Exhibit 52 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Feb. 6, 1990 to PT Acquisitions from Dun & Bradstreet Receivable Recovery Systems re: final notice for payment of account.
National Semiconductor HPC16400/HPC36400/HPC46400 High–Performance microControllers with HDLC Controller product literature.
NEC Data Sheet Mos Integrated Circuit uPD7225 Programmable LCD Controller/Driver. Part Nos. uPD7225G00, uPD7225G01, uPD7225GB–3B7.
NEC Electronics Inc. High–End, 8–Bit, Single–Chip CMOS Microcomputers product literature.
NEC Electronics Inc. uPD78C10/C11/C14 8–Bit, Single–Chip CMOS Microcomputers with A/D Converter product literature.
NEC Electronics Inc. Microcomputer Products Single–Chip Products Data Book vol. 1 of 2 cover page.
NEC Electronics Inc. Microcomputer Products Microprocessors, Peripherals, & DSP Products Data Book vol. 2 of 2 cover page.
NEC Electronics Inc. MOS Integrated Circuit uPD70208H, 70216H Data Sheet, V40HL, V50HL, 16/8; 16–Bit Microprocessor.
NEC Electronics Inc. MOS Integrated Circuit uPD7225 Programmable LCD Controller/Driver.
Signetics Microprocessor Data manual cover page.
Signetics Microprocessor Products Data manual, 8×330 Floppy Disk Formatter/Controller product specification.
Signetics Microprocessor Products Data manual, SC96AH Series Single–Chip 16–Bit Microcontrollers preliminary specification.
Realtime DSP; The TMS320C30 Course, Revision 3 (educational document re programming Digital Signal Processor microprocessor).
Texas Instruments TMS320C30 Digital Signal Processor product literature.
Texas Instruments TMS320C30 Digital Signal Processor product literature.
Texas Instruments TMS34010 Graphics System Processor product literature.
Texas Instruments TMS320 DSP Designer's Notebok, Using a TMS320C30 Serial Port as an Asynchronous RS–232 Port Application Brief: SPRA240.
UK application 8233733 as filed Nov. 26, 1982.
Office Action of Jan. 31, 2000 in U.S. Appl. No. 09/124,623.
TPL Infringement Contention for the TLCS–900/L Series.
TPL Infringement Contention for Toshiba Microcontroller.
TPL Infringement Contention for Toshiba TC35273.
Duell, C. H., "Everything that can be invented has been invented," 2 pages downloaded from http://www.tplgroup.net/patents/index.php.
Alliacense Product Report, NEC Microcontroller, UPD789473, B Bit Microcontroller, pp. 1–38.
Mostek Corp., Advertisement, EDN, Nov. 20, 1976.
Guttag, K.M., "The TMS34010: An Embedded Microprocessor," *IEEE Micro*, 8(3):39–52 (May 1988).
"8–Bit Single–Chip Microprocessor Data Book," Hitachi America Ltd., Table of Contents and pp. 251–279) Jul. 1985).
Request for Reexamination of U.S. Patent 6,598,148 as filed Sep. 21, 2006.
Office action of Nov. 22, 2006 in application No. 90/008,227.
Toshiba TLCS–42, 47, 470 User's Manual Published in Apr. 1986.
Fukui et al., "High Speed CMOS 4–bit Microcomputer SM550 Series," published 1982, 1983.

Intel 80386 Programmer's Reference Manual, published by Intel (1986).
Fairchild Microcomputers, F8/3870, F6800, Bit Slice, IC Master 1980, pp. 1, 2016–2040 (1980).
Mostek Corp., "Mostek 1981 3870/F8 Microcomputer Data Book", Feb. 1981, pp. III–76 through III–77, III–100 through III–129, and VI–1 through VI–31.
IBM Systems Reference Library, IBM System/360 Model 67 Functional Characteristics, File No. S360–01, Form A27–2719–0, published by IBM (1967).
Anderson, D.W., The IBM System/360 Model 91: Machine Philosophy and Instruction Handling, IBM Journal, (1967).
GE–625/ 635 Programming Reference Manual, revised Jan. 1966.
Clipper™ 32–Bit Microprocessor, Introductions to the Cliper Architecture, published by Fairchild in 1986.
Simpson et al., "The IBM RT PC Romp processor and memory management unit architecture," *IBM systems Journal*, 26(4):346–360.
M68300 Family MC68332 User's Manual, published by Motorola, Inc. in 1995.
Ditzel et al., "The Hardware Architecture of the Crisp Microprocessor," AT & T Information Systems, ACM, pp. 309–319 and table of contents (1987).
i860 64–Bit Microprocessor, published by Intel Corporation Feb. 1989.
Rau et al., "The Cydra 5 Departmental Supercomputer, Design Philosophies, Decisions, and Trade–offs," *IEEE* pp. 12–36 (1989).
Datasheet for Intel 4004 Single Chip 4–Bit 9–Channel Microprocessor, pp. 8–15 to 8–23.
Intel MCS–4 Micro Computer Set (Nov. 1971).
Intel 8008 8–Bit Parallel Central Processor Unit published by Intel (Nov. 1972).
iAPX 386 High Performance 32–Bit Microprocessor Product Review, published by Intel (Apr. 1984).
Intel 80386 Programmer's Reference Manual, published in Intel (1986).
Motorola MC68020 32–Bit Microprocessor User's Manual (1984).
Thornton, J. E., "Design of a Computer, The Control Data 6600," published by Advanced Design Laboratory (1970).
6400/6500/6600 Computer Reference Manual, published by Control Data® (1965, 1966, 1967).
Grishman, R., "Assembly Language Programming for the Control Data 6600 and Cyber Series Algorithmics".
Hennessy et al., "MIPS: A Microprocessor Architecture," *IEEE*, pp. 17–22 (1982).
Hennessy et al., "Hardware/software tradeoff for increased performance," *Proceedings of the Symposium on Architectural Support for Programming Languages and Operating Systems*, pp. 2–11, ACM, Apr. 1982.
Hennessy et al., "MIPS: A VLSI Processor Architecture, Technical Report 223," Computer Systems Laboratory, Department of Electrical Engineering and Computer Science, Standford University Nov. 1981.
Gross et al., "Measurement and evaluation of MIPS architecture and processor," *ACM Trans. Computer Systems*, pp. 229–257 Aug. 1988.
Bit Sparc Integer Unit B5000 Datasheet attached to a presentation by Anant Agrawal in 1989.
Sequin et al., "Design and Implementation of RISC1," pp. 276–298 from *VLSI Architecture*, B. Randell and P.C. Treleaven, editors, Prentice Hall, 1983.
Ungar et al., "Architecture of SOAR: Smalltalk on a RISC," *Proceedings of the 11th Annual International Symposium on Computer Architecture ISCA '84*. ACM Press, New York, NY, pp. 188–197 (1984).
Cray–I Computer System Hardware Reference Manual, Publication No. 2240004, Rev C, Nov. 4, 1997.
Acorn Computers, Ltd., Acorn RISC Machine CPU Software Manual, Issue 1.00 Oct. 1985.
Patterson et al., "Architecture of a VLSI Instruction Cache for A RISC," *ACM*, pp. 108–116 (1983).
Patterson, D. A., "Reduced Instruction Set Computers" *Communication of the ACM*, 28(1):8–21, Jan. 1985.
Patterson, D. A., "RISC watch", pp. 11–19 (Mar. 1984).
Sherburne, R. W., "Processor Design Tradeoffs in VLSI," U.C. Berkeley, May 1984. PhD Dissertation.
Excerpt from A Seymour Cray Perspective http://research.Microsoft.com/users/gbell/craytalk/std001.htm (Slide 1).
Excerpt from A Seymour Cray Perspective htpp.//research.microsoft.com/users/gbell/craytalk/std029.htm (Slide 29).
RISC Roots: CDC 6600 (1965).
http://www.bitsavers.org/pdf/tdc/6x00/.
Simpson, R.O., "The IBM RT Personal computer," *BYTE*, 11(11):43–78 (Oct. 1986).
Ryan, D.P., "Intel's 80960: An Architecture Optimized for Embedded Control," *IEEE, Micro,* published in Jun. 1988.
Waters, F., "IBM RT Personal Computer Technology," IBM Corp. 1986.
Alliacense Product Report, USP 5784584, TLCS–900/H1 Series TMP92C820, Toshiba Microcontroller TMP92C820 / TLCS–900/H1 Series 16–bit Microcontroller, pp. 1–9, filed Aug. 14, 2006 in 2:05–CV–00494–TJW.
Alliacense Product Report, NEC Microcomputer, USP 5784584, V850E2 32 Bit Microcontroller, pp. 1–8 (2006).
"8 bit Dual 1–chip Microcomputer MN1890 Series User's Manual," translation of original Japanese language document, by Matsushita Electric Industrial Co., Ltd. Semiconductor Sales Division.
Sibigtroth, J. M., "Motorola's MC68HC11: Definition and Design of a VLSI Microprocessor," *IEEE Micro* 4(1):54–65 (1984).
"Specification Sheet, MN18882 (Book)," translation of the Japanese language original, Code No. MIG0175, Matsushita Electronics Industry Corporation, Microcomputer Products Division, Oct. 2, 1990.
"DS5000 Soft Microcontroller User's Guide Preliminary V 1.0," Dallas Semiconductor.
MN188166 User's Manual, Japanese language document with English translation.
Alliacense Product Report—Preliminary Review, USP 5,440,749; GPS Car Navigation Main Processor.
Alliacense Product Report—Preliminary Review, USP 5,440,749; GSP Navigation System GPS Chipset.
Alliacense Product Report—Preliminary Review, USP 5,440,749; GPS Navigation System Main Microprocessor.
Alliacense Product Report—Preliminary Review, USP 5,440,749; Kyocera Digital Camera Finecam S3R Image Processor.
Alliacense Product Report—Preliminary Review, USP 5,440,749; PDA/Mobile Navigation, GPS Processor.
Motorola MC68020 32–bit Microprocessor User's Manual, 2nd Edition, Rev. 1, Prentice–Hall, 1985.
Barron et al., "The Transputer," *Electronics*, pp. 109–115 (1983).

Burroughs Corporation, "Burroughs B7700 Systems Reference Manual," 1973.
Fiasconaro, J., "Microarchitecture of the HP9000 Series 500 CPU," *Microarchitecture of VLSI Computers, NATO ASI Series No. 96*, Antognetti, eds., pp. 55–81.
MacGregor et al., "The Motorola MC68020," *IEEE Micro*, 4(4):103–118 (1984).
Best et al., "An Advanced–Architecture CMOS/SOS Microprocessor", IEEE Micro, vol. 2, No. 3, vol. 2, No. 3 (Jul. 1982), pp. 10–26.
Technology Properties Limited (TPL), Moore Microprocessor Patent (MMP) Portfolio, downloaded from <<www.tpl-group.net/patents/index.php>> downloaded on Aug. 3, 2006, 3 pages total.
Acorn's RISC Leapfrog, Acorn User special issue, Jun. 1987; 59: 149–153.
Agrawal, et al., "Design Considerations for a Bipolar Implementation of SPARC," Compcon Spring apos;88. Thirty–Third IEEE Computer Society International Conference, Digest of Papers, Feb. 29–Mar. 3, 1988, pp. 6–9.
Agrawal, "An 80 MHz Bipolar ECL Implementation of SPARC," Sun Microsystems, Inc., Jun. 25, 1989, 40 pages total.
ARM Datasheet, Part No. 1 85250 0360 0, Issue No. 1 (Mar. 17, 1987).
Atmel SPARC Instruction Set, "Assembly Language Syntax," Rev. 4168C–AERO–08/01, 2002.
Bagula, "A 5V Self–Adaptive Microcomputer with 16Kb of #2 Program Storage and Security," IEEE International Solid–State Circuit Conference, 1983, pp. 34–35.
Bayko, Great Microprocessors of the Past and Present (V 11.7.0), downloaded from: <<http://web.archive.org/web/20010107210400/http://bwrc.eecs.berkeley.edu/CIC/Archive/cup_history.html>>, Feb. 2007, 60 pages total.
Books Review: Operating Systems A Systematic View, William S. Davis, Addison–Wesley Publishing Company, Inc., 1987; 26(4):453–454.
Bourke, "Character Synchronization During Overrun Conditions," Delphion, IBM Technical Disclosure Bulletin, Dec. 1977.
Burroughs Corporation, "Burroughs B5500 Information Processing System Reference Manual," 1973.
CAL Run Fortran Guide, University of California, Computer Center, Berkeley, 292 pages total, (Sep. 1974).
CDC 6000 Computer Systems—Cobol Instant 6000, Version 3; Control Data Publication No. 60327600A (Apr. 1971).
CDC 6000 Computer Systems, 7600 Computer Systems: Fortran Extended Instant 6000 Version 3, 7600 Version 1; Control Publication No. 60305900A (May 1971).
CDC 6000 Computer Systems/7600 Computer Systems: Fortran Extended Reference Manual, 6000 Version 3, 7600 Version 1; Control Data Publication No. 60329100, Revision D (1972).
CDC 6000 Series Computer System, 6642 Distributive Data Path Operation and Programming Reference Manual; Control Data Publication No. 60376300C (Mar. 1979).
CDC 6000 Series Computer Systems—Chippewa Operating System Documentation, vol. I, Preliminary Edition (updated May 1966).
CDC 6000 Series Computer Systems—Chippewa Operating System Documentation, vol. II, Preliminary Edition, Peripheral Packages and Overlays (Oct. 1965).
CDC 6000 Series Computer Systems—Chippewa Operating System Documentation, vol. III, Preliminary Edition, DSD—The Systems Display, (Nov. 1965).
CDC 6000 Series Computer Systems Ascent General Information Manual; Control Data Publication No. 60135400 (Feb. 66).
CDC 6000 Series Computer Systems Chippewa Operating System Reference Manual; Control Data Publication No. 60134400 (Dec. 1965).
CDC 6000 Series Computer Systems Hardware Reference Manual; Control Data Publication No. 60100000 (Aug. 1978).
CDC 6000 Series Computer Systems/ 7600 Computer System: 6000 Compass Version 2, 7600 Versions 1 & 2 Reference Manual; Control Data Publication No. 60279900, Revision D, (1970, 1971, 1972).
CDC 6000 Series Computer Systems: Chippewa Operating System Fortran Reference Manual; Control Data Publication No. 60132700A (May 1966).
CDC 6000 Series Computer Systems: Peripheral Equipment Reference Manual; Control Data Publication No. 60156100, Revision J (Mar. 1970).
CDC 6000 Series Computer Systems: Site Preparation and Installation Manual; Control Data Publication No. 60142400, Revision B (Sep. 1965).
CDC 6000 Series Computer Systems: Fortran Extended General Information, Control Data Publication No. 60176400 (Oct. 1966).
CDC 6000 Series Fortran Extended 4.0, Internal Maintenance Specifications , (1971).
CDC 6000 Series Introduction and Peripheral Processors Training Manual, Second Edition, Control Data Publication No. 60250400 (Nov. 1968).
CDC 6400 Central Processor, Control Data Publication No. 60257200 (Feb. 1967).
CDC 6400/6500/6600 Ascent–to–Compass Translator; Control Data Publication No. 60191000 (Mar. 1967).
CDC 6400/6500/6600 Computer System Input/Output Specification; Control Data Publication No. 60045100 (Sep. 1967).
CDC 6400/6500/6600 Computer System Instant SMM; Control Data Publication No. 60299500 (Nov. 1969).
CDC 6400/6500/6600/ Computer Systems Compass Reference Manual; Data 60190900, Revision B (Mar. 1969).
CDC 6400/6500/6600 Computer Systems Reference Manual; Control Data Publication No. 60100000, Revision K (Aug. 1970).
CDC 6400/6500/6600 Extended Core Storage Systems Reference Manual; Control Data Publication No. 60225100, (Feb. 1968).
CDC 6400/6500/6600 Jovial General Information Manual; Control Data Publication No. 60252100A (Mar. 1969).
CDC 6400/6500/6600 Computer Systems: Ascent/Asper Reference Manual; Control Data Publication No. 60172700 (Jul. 1966).
CDC 6400/6600 Fortan Conversion Guide; Data Publication No. 60175500 (Aug. 1966).
CDC 6400/6600 Systems Bulletin (Oct. 10, 1968), 84 pages.
CDC 6400/6600, Export/Import 8231 Reference Manual; Data Publication No. 60189100 (Apr. 1967).
CDC 6600 Central Processor vol. 1; Control & Memory; Data Control Publication Nol. 021067 (Mar. 1967).
CDC 6600 Central Processor, vol. 2, Functional Units; Control Data Publication No. 60239700 (Mar. 1967).

CDC 6600 Chassis Tabs; Control Data Publication No. 63016700A (Apr. 1965).
CDC 6600 Chassis Tabs; Control Data Publication No. 63019800 (Mar. 1965).
CDC 6600 Chippewa Operating System; Control Data Publication No. 60124500, Revision C (Apr. 1965).
CDC 6600 Computer System 6601 A–J, 6613A/B/C, 6604A/B/C, 6614–A/B/C/ Central Processor (including Functional Units) vol. 1, Diagrams & Circuit Description; Control Data Publication No. 60119300BT (Jan. 1968).
CDC 6600 Computer System 6601 A–J, 6613A/B/C, 6604A/B/C/, 6614–A/B/C Peripheral and Control Processor/Central Memory/Clock/Extended Core Storage Coupler (Std Opt 10102 and/or Spec Opt 60080)/Power Wiring, vol. 2, Diagrams & Circuit Descriptions; Control Data Publication No. 60119300BT (Jan. 1968).
CDC 6600 Computer System Operating System/Reference Manual, SIPROS66, 1st ed.; Control Data Publication No. 60101800A (1965).
CDC 6600 Computer System Programming System/Reference Manual, vol. 1. Ascent; Control Data Publication No. 601016008 (1965).
CDC 6600 Computer System Programming System/Reference Manual, vol. 2, Asper; Control Data Publication No. 60107008 (1965).
CDC 6600 Computer System Programming vol. 3, Fortran 66; Control Data Publication No. 60101500B (1965).
CDC 6600 Computer Training Manual vol. 2, Preliminary Edition, Section 7.2 Shift Functional Units, 164 pages.
CDC 6600 Data Channel Equipment 6602–B/6612–A, 6603–B, 6622–A, 6681–B, 6682–A6683–A, S.O. 60022, 60028, 60029, Diagrams & Circuit Description' Control Data Publication No. 60125000, Revision G (Jun. 1966).
CDC 6600 Training Manual; Control Data Publication No. 60147400, Revision A (Jun. 1965).
CDC 6603—A/B/C Disk File Controller Reference Manual; Control Data Publication No. 60334000 (1970).
CDC 6638 Disk File Subsystem Training Supplement; Control Data Publication 602500800A (Oct. 1968).
CDC 6638 Disk File System Standard Option 10037–A, 6639–A/B File Controller—Diagrams and Circuit Description/Maintenance/Maintenance Aids/Parts List/Wire Lists/Chassis Tabs; Control Data No. 60227300, Revision H (Mar. 1974).
CDC 6639—A/B Disk File Controller Reference Manual; Control Data Publication No. 60334100E (Aug. 1973).
CDC 6639 Disk Controller Training Manual Test Edition (Sep. 1967), 28 pages.
CDC APL Version 2 Reference Manual, CDC Operating Systems :NOS; Control Data Publication No. 60454000F (Nov. 1980).
CDC Basic Version 3 Reference Manual: NOS 1 & NOS/BE 1; Control Data Publication No. 19983900G (Oct. 1980).
CDC Chippewa Operating System, Document Class ERS, System No. E012, Version 1.1; External Reference Specifications—Chippewa Operating System, (Jun. 1966).
CDC Chippewa Operating System, Document Class SIR, System No. E012, Version 1.0, (Mar. 3, 1966).
CDC Chippewa Operating System, Document Class SIR, System No. E012, Version 1.1, (Mar. 3, 1966).
CDC Cobol Version 4 Instant Manual, Cyber 170 Series, Cyber 70 Models 72, 73, 74, 6000 Series; Control Data Publication No. 60497000A (Feb. 1976).
CDC Cobol Version 5 Instant Manual, Operating Systems: NOS 1/BE 1; Control Data Publication No. 60497300B (Feb. 198).
CDC Codes/Control Data 6400/6500/6600 Computer Systems; Control Data Publication No. 60141900, Revision C (1966, 1967).
CDC Codes/Control Data 6400/6500/6600/6700 Computer Systems; Control Data Publication No. 60141900, Revision D (1966, 1967).
CDC Codes/Control Data 6600; Control Data Publication No. 60141900, Revision A (May 1965).
CDC Compass Version3 Instant, Operating Systems: NOS 1, NOS 2, NOS/BE 1, Scope 2; Control Data Publication No. 60492800D (Jun. 1982).
CDC Course No. FH4010–1C, NOS Analysis, Student Handbook, Revision C (Apr. 1980).
CDC Course No. FH4010–4C NOS Analysis, Study Dump (Apr. 1980).
CDC Cyber 170 Models 720, 730, 740, 750 and 760 Model 176 (Level B/C) Computer Systems, Codes; Control Data Publication No. 60456920C, (Jun. 1981).
CDC Cyber 70 Computer Systems Models 72, 73, 74, 6000 Computer Systems: Fortran Reference Manual Models 72, 73, 74 Version 2.3, 6000 Version 2.3; Control Data Publication No. 19980400, Revision F (Jul. 1972).
CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems—ALGOL Reference Manual, Cyber 70 Series Version 4, 6000 Series Version 4, 7600 Series Version 4; Control Data Publication No. 60384700A (Aug. 1973).
CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems: Cobol Instant Models 72, 73, 74 Version 4, Model 76 Version 1, 6000 Version 4; Control Data Publication No. 60328400A (Dec. 1971).
CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems: Fortran Extended Instant Models 72, 73, 74 Version 4, Model 76 Version 2, 7600 Version 2, 6000 Version 4; Control Data Publication No. 60357900A (Nov. 1971).
CDC Cyber 70 Computer Systems Models 72, 73, 74, 76 7600 Computer System, 6000 Computer Systems: Fortran Extended Reference Manual Models 72, 73, 74 Version 4, Model 76 Version 2, 6000 Version 4; Control Data Publication No. 60306600A (Oct. 1971).
CDC Cyber 70 Series 6000 Series Computer Systems: APL *Cyber Reference Manual; Control Data Publication No. 19980400B (Jul. 1973).
CDC Cyber 70 Series Computer Systems 72, 73, 74, 6000 Series Computer Systems—Kornos 2.1 Workshop Reference Manual; Control Data Publication No. 97404700D (1976).
CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, Krono 2.1 Operator Guide; Control Data Guide; Control Data Publication 60407700A (Jun. 1973).
CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, Kronos 2.1 Installation Handbook; Control Data Publication No. 60407500A (Jun. 1973).
CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, Kronos 2.1 Time–Sharing User's Reference Manual; Control Data Publication No. 60407600B (May 1974).

CDC Cyber 70/ Model 76 Computer System, 7600 Computer System: Fortran Run, Version 2 Reference Manual; Control Data 60360700C (May 1974).
CDC Cyber Interactive Debug Version 1 Guide for Users of Fortran Extended Version 4, CDC Operating Systems: NOS 1, NOS/ BE1, Control Data Publication No. 60482700A (Feb. 1979).
CDC Cyber Interactive Debug Version 1 Guide for Users of Fortran Version 5, Operating Systems: NOS 1, NOS/ BE 1; Control Data Publication No. 6048100C (Sep. 1984).
CDC Cyber Interactive Debug Version 1 Reference Manual, NOS 1, NOS 2, NOS/ BE 1; Data Control Publication No. 60481400D (Jun. 1984).
CDC Cyber Loader Version 1 Instant, CDC Operating System NOS1, NOS/ BE 1; Control Data Publication No. 60449800C (Aug. 1979).
CDC Disk Storage Subsystem—Operation and Programming Manual; Control Data Publication No. 60383900, Version T (1972–1980).
CDC Fortran Extended 2.0, Document Class ERS, System No. C012, (Dec. 1966).
CDC Fortran Extended 2.0, Document Class IMS, Internal Maintenance Specifications—64/65/6600 V Fortran Extended Version 2 (Mar. 1969).
CDC Fortran Extended Version 4 Instant Manual, Operating Systems: NOS 1, NOS/BE, 1 Scope 2; Control Data Publication No. 60497900B (Jun. 1981).
CDC Fortran Extended, Sales Technical Memorandum (May 1967).
CDC Fortran Version 5 Instant, CDC Operating System: NOS 1, NOS/ BE 1, Scope 2; Control Data Publication No. 60483900A (Jan. 1981).
CDC GED Fortran Extended 1.0, Product No. C012, Dept. No. 254, Project No. 4P63FTN (Aug. 1967).
CDC Instant 6400/3500/6500 Simula; Control Data Publication No. 60235100, Revision A (Feb. 1969).
CDC Instant 6400/6500/6600 Compass; Control Data Publication No. 60191900, Revision A (1968).
CDC Instant Fortran 2.3 (6000 Series); Data Publication No. 60189500D (May 1969).
CDC Internal Maintenance Specification; Fortran V5.; Control Data Publication No. 77987506A.
CDC Internal Maintenance Specification; Fortran V5.; Control Data Publication No. 77987506A.
CDC Kronos 2.1 Reference Manual vol. 1 of 2; Control Data Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems; Control Data Publication No. 60407000D (Jun. 1975).
CDC Kronos 2.1 Time–Sharing User's Reference Manual, Cyber 70 Series Models 72, 73, 74, 6000 Series Computer Systems; Control Data Publication No. 60407600D (Jun. 1975).
CDC Model dd 60A Computer Control Console/Customer Engineering Manual; Control Data Publication No. 82100010 (Mar. 1965).
CDC Model dd60b Computer Control Console/Customer Engineering Manual/ Control Data Publication No. 82103500 (Feb. 1967).
CDC Network Products: Network Access Method Version 1, Network Definition Language Reference Manual; Control Data Publication No. 60480000J (May 1981).
CDC Network Products: Network Terminal User's Instant—Operating System NOS 1; Control Data Publication No. 60456270C, (Oct. 1980).
CDC NOS 2 Operations Handbook; Control Data Publication No. 60459310, (Aug. 1994).
CDC NOS Version 1 Applications Programmer's Instant, CDC Computer Systems; Cyber 170 Series, Cyber 70 Models, 71, 72, 73, 74, 6000 Series; Control Data Publication No. 60436000H (Jan. 1980).
CDC NOS Version 1 Internal Maintenance Specification vol. 1 of 3; Control Data Publication No. 60454300B (Aug. 1979).
CDC NOS Version 1 Internal Maintenance Specification vol. 2 of 3; Control Data Publication No. 60454300B (Aug. 1979).
CDC NOS Version 1 Internal Maintenance Specification vol. 3 of 3; Control Data Publication No. 60454300B (Aug. 1979).
CDC NOS Version 1 Operator's Guide, CDC Computer Systems: Cyber 170 Series, Cyber 70 Model 71, 72, 73, 74, 6000 Series (Dec. 1980).
CDC NOS Version 1 Reference Manual vol. 1 of 2, CDC Computer Systems: Cyber 170 Series, Cyber 70 Models 71,72, 73, 74, 6000 Series; Control Data Publication No. 60435400J (1979).
CDC NOS Version 1 Reference Manual vol. 2 of 2, CDC Computer Systems: Cyber 170 Series, Cyber 70 Models 71, 72, 73, 74, 6000 Series; Control Data Publication No. 60445300E (1977).
CDC NOS Version 1 System Maintenance Reference Manual; Control Data Publication No. 60455380H (Apr. 1981).
CDC NOS Version 2 Analysis Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60459300D (Oct. 84).
CDC NOS Version 2 Analysis Handbook; Control Data Publication No. 60459300U (Jul. 1994).
CDC NOS Version 2 Installation Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60459320E_(Mar. 1985).
CDC NOS Version 2 Operation/Analysis Handbook, Cyber 170, Cyber 70 Models 71, 72, 73, 74 6000, Control Data Publication No. 60459310C (Oct. 1983).
CDC NOS Version 2 System Maintenance Reference Manual, Cyber 170, Cyber 70 Models 71, 72, 73 74, 6000; Control Data Publication No. 60459300C (Oct. 1983).
CDC NOS/BE Version 1 Diagnostic Handbook, Cyber 180; Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publicaton No. 60494400–V (1986).
CDC NOS/BE Version 1 Installation Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60494300AB (Dec. 1988).
CDC NOS/BE Version 1 Reference Manual, Cyber 170 Series, Cyber 70 Models 71, 72, 73, 74, 6000 Series; Control Data Publication No. 60493800M 1981.
CDC Outline of Reports on Feasibility Study of 64/6600 Fortran Ver 3.0 and Conversational Fortran, Fortran Study Project, Product No. X010, Dept. No. 254, Project No. 4P63, (Jun. 1966).
CDC Pascal Version 1 Reference Manual, Operating Systems: NOS 2; Control Data Publication No. 60497700 (Sep. 1983).
CDC Pascal Version 1 Reference Manual, Operating Systems: NOS 2; Control Data Publication No. 60497700A (Dec. 1982).

CDC PL/1 Version 1 Instant, CDC Operating Systems: NOS 1, NOS/ BE1, Control Data Publication No. 60483700A (Nov. 1979).
CDC Simscript 11.5 Instant, Control Data Publication No. 84000450B (Sep. 1978).
CDC Sort/Merge Version 4 and 1 Instant, Operating Systems: NOS 1, NOS/BE 1, Scope 2; Control Data Publication No. 60497600C (Jan. 1981).
CDC Sort/Merge Vision 5 Reference Manual, Operating Systems: NOS 2, NOS/ BE 1; Control Data Publication No. 60484800C (Feb. 1984).
CDC SYMPL Version 1 Instant, NOS 1, NOS/BE 1, Scope 2; Control Data Publication No. 60482600A (May 1978).
CDC SYMPL Version 1 Users Guide, Operating Systems: NOS 1, NOS/BE 1, Scope 2; Control Data Publication No. 60499800B (Apr. 1978).
CDC Update Instant, Cyber 170 Series, Cyber 70 Series, 6000 Series, 7600 Computer Systems; Control Data Publication No. 60450000A (Nov. 75).
CDC Update Reference Manual Operating Systems: Scope 3.4, Kronos 2.1; Control Data Publication No. 60342500, Revision H (1971–1976).
CDC Xedit Version 3 Reference Manual, Operating System: NOS 1; Control Data Publication No. 60455730B (Aug. 1979).
Chippewa Laboratories Fortran Compiler Run, Preliminary Edition, CDC 6000 Series Computer Systems, (Apr. 1966).
Cho et al., WAM 3.6: A 40K Cache Memory and Memory Management Unit, ISSCC '86, Feb. 19, 1986.
Cordell, II et al., "Advanced Interactive Executive Program Development Enviornment," IBM Systems Journal, 1987; 26(4):381–382.
Crawford, "The i486 Executing Instructions in One Clock Cycle," IEEE Micro, pp. 28–36 (Feb. 1990).
Disk Routines and Overlays, Chippewa Operating System, CDC Development Division—Applications, (Nov. 1965).
Dowsing et al., "Computer Architecture: A First Course, Chapter 6: Architecture and the Designer," Van Nostrand Reinhold (UK) Co. Ltd., pp. 126–139.
Evans et al., "An Experimental 512–bit Nonvolatile Memory with Ferroelectric Storage Cell," IEEE Journal of Solid–State Circuits, 23(5):1171–1175.
Field Maintenance Print Set, KA780–01–01 Rev. A.
Fisher et al., "Very Long Instruction Word Architectures and the ELI–512," ACM pp. 140–150 (1983).
Furber, VSLI RISC Architecture and Organization, Chapter 3: Commercial VLSI RISC, pp. 124–129, Marcel Dekker, Inc., 1989.
GB Patent Application 8233733, INMOS, Ltd. Microcomputer, filed Nov. 26, 1962.
GE 600 Series, publication.
Gershon, Preface, IBM Systems Journal 26(4):324–325.
Green et al., "A Perspective on Advanced Peer–to–Peer Networking," IBM Systems Journal, 1987; 26(4):414–428.
Grimes et al., "64–bit Processor, The Intel i860 64–Bit Processor: A General–Purpose CPU with 3D Graphics Capabilities", published by Intel, p. 85 (Jul. 1989).
Hansen, "A RISC Microprocessor with Integral MMU and Cache Interface," ICCD '86, pp. 145–148, 1986.
Hennessy et al., "Hardware/software Tradeoff for Increased Performance," Technical Report No. 22.8, Computer Systems Laboratory, Feb. 1983, 24 pages.
Hennessy et al., "The MIPS Machine", COMPCON, IEEE, Spring 1982, pp. 2–7.
Hennessy, "Performance Issues in VLSI Processor Design," IEEE on VLSI in Computers, pp. 153–156 (1983).
Hinton, 80960—Next Generation, Compcon Spring 89, IEEE, 13–18 (1989).
Hollingsworth et al., "The Fairchild Clipper: Instruction Set Architecture and Processor Implementation," Report No. UCB/CSD 87/329, Computer Science Division (EECS), University of California Berkeley, California, (Feb. 11, 1987).
HP 9000 Instrument Controllers, Technical Specifications Guide, Oct. 1989.pdf.
HP 9000 Series Computer Systems, HP–UX Reference 09000–090004, Preliminary Nov. 1982.
Hughes, "Off–Chip Module Clock Controller", Delphion, IBM Technical Disclosure Bulletin, Sep. 1989.
Hunter, "Introduction to the Clipper Architecture," IEEE Micro, pp. 6–26 (Aug. 1987).
IBM RT PC, BYTE 1986 Extra Edition, Inside The IBM PCs, pp. 60–78.
INMOS Limited, IMS T424 Transputer Reference Manual, 1984.
Intel 388Tm DX Microprocessor 32–Bit CHMOS Microprocessor With Integrated Memory Management (1995).
Intel 80960CA User's Manual published by Intel (1989).
Intel Architecture Optimization Manual, Order No. 242816–003, published by Intel (1997).
Intel Architecture Software Developer's Manual, vol. 1; Basic Architecture, published by Intel (1997).
Intel 8080A/8080A–1/8080A–2, 8–Bit N–Channel Microprocessor, Order No. 231453–001, Its Respective Manufacturer (Nov. 1986).
Johnson et al., "A Variable Delay Line PLL for CPU–Coprocessor Synchronization," IEEE Journal of Solid–State Circuits, 23(5): 1218–1223, Oct. 1988.
Katevenis et al., "Reduced Instruction Set Computer Architecture for VLSI," Doctoral Dissertation, Oct. 1983.
Katevenis et al., "The RISC II Micro–Architecture," Journal of VLSI and Computer Systems, 1(2):138–152 (1984).
Kipp, "Micron Technology Inc. Reports Financial Results," Business Wire, New York, Sep. 26, 1988.
Kohn et al., "Introducing Intel i860 64–Bit Microprocessor," Intel Corporation, IEEE Micro (Aug. 1989).
Koopman, "RTX 4000," Proceedings of 1989 Rochester Forth Conference, pp. 84–86.
Koopman, "The WISC Concept: A proposal for a writable instruction set computer," BYTE, pp. 187–193. (Apr. 1987).
Koopman, Jr. et al. "MVP Microcoded CPU/16 Architecture," Proceedings of 1986 Rochester Forth Conference, pp. 277–280.
Koopman, Jr. et al., "WISC Technologies, Inc., Writable Instruction Set, Stack Oriented Computers: The WISC Concept," 1987 Rochester Forth Conference, Journal of Forth Application and Research, 5(1):49–71.
Koopman, Jr., Slack Computers: the new wave, 1989.
Loucks et al., "Advanced interactive Executive (AIX) Operating System Overview," IBM Systems Journal, 1987; 26(4):326–345.
Matick, "Self–Clocked Cache," Delphion, IBM Technical Disclosure Bulletin, Apr. 1985.
Miller, Frequency Modulated Ring Oscillator for a Mode Regulated Substrate Bias Generator, Delphion, IBM Technical Disclosure Bulletin, Sep. 1989.
Mills et al, "Box Structured Information Systems," IBM Systems Journal, 1987; 26(4):395–413.

MMP Portfolio, News Release: Roland Becomes 50th Licensee, Setting a Major Milestone in Moore Microprocessor Patent Licensing Program, 3 pages (May 1, 2009).

Moussouris et al., "A CMOS RISC Processor Integrated System Functions," Proceedings of 31st IEEE Computer Society International Conference, Cathedral Hill Hotel, San Francisco, CA Mar. 3–6, 1986, pp .126–131, 1986.

Olson, Semiconductor Die with Wiring Skirt (Packaging Structure), Delphion, IBM Technical Disclosure Bulletin, Jul. 1978.

O'Neil, "Pipeline Memory System for Drams", Delphion, IBM Technical Disclosure Bulletin, May 1989.

Patterson et al., "RISC I: A Reduced Instruction Set VLSI Computer," Proceedings of the 8th annual symposium on Computer Architecture on Computer Architecture, Miinneapolis, Minnesota, pp. 443–457 (May 1981).

Pountain, "The Archimedea A310," BYTE, 1987.

Przybyiski et al., "Organization and VLSI Implementation of MIPS," Technical Report CSL–TR–84–259, Apr. 1984.

Przybyiski, "The Design Verification and Testing of MIPS", 1984 Conference on Advanced Research in VLSI, pp. 100–109.

Roche et al., "Method of Assuring a Two–Cycle Start, Zero Cycle Stop, Non–Chopping on Chip Clock Control Throughout a VLSI Clock System," Delphion, IBM Technical Disclosure Bulletin, Sep. 1989.

Rowen et al., "A Pipelined 32b NMOS Microprocessors and Microcontrollers," IEEE International Solids–State Circuits Conference, pp. 180–181, 1984.

Rubinfeld et al., "The CVAX CPU, A CMOS VAX Microprocessor Chip", International Conference on Computer Design, Oct. 1987.

Sanamrad et al., "A Hardware System Analysis Processor," IEEE, Aug. 1987, pp. 73–80.

Shih, "Microprogramming Heritage of RISC Design," Proceedings of the 23rd annual workshop and symposium on Microprogramming and microarchitecture, pp. 275–280 (1990).

Sultan et al., "Implementing System–36 Advanced Peer–to–Peer Networking," IBM Systems Journal, 1987; 26(4):429–452.

Thornton, J. E., "Considerations in Computer Design Leading Up To the Control Data 6600," Control Data Chippewa Laboratory (1970).

VAX 11/780 Architecture Handbook vol. 1, 1977–1978, 2–7 and G–8.

VAX 8800 System Technical Description vol. 2, EK–KA881–TD–PRE, Section 6, Instruction Box (IBOX), Preliminary Edition (Jul. 1986).

VAX Maintenance Handbook; VAX–11/780, EK–VAXV2–HB–002, 1983 Edition.

VL86C010 RISC Family Data Manual, Application Specific Logic Product Division, 1987.

Waters et al., "AIX Usability Enhancements and Human Factors," IBM Systems Journal, 1987; 26(4):383–394.

Williams, "Chip Set Tackles Laptop Design Issues, Offers Flat–Panel VGA Control," Computer Design, Oct. 15, 1988; 27(19):21–22.

IEEE Std 796–1983, Microcomputer System Bus, pp. 9–46 (Dec. 1983).

Mead & Conway, Introduction to VLSI Systems, pp. 1–429 (1980).

EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

ONLY THOSE PARAGRAPHS OF THE SPECIFICATION AFFECTED BY AMENDMENT ARE PRINTED HEREIN.

Column 17, lines 12–37:

Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor **50** provides a dual-clock scheme as shown in FIG. **17**, with the CPU **70** operating **[**a synchronously**]** *asynchronously* to I/O interface **432** forming part of memory controller **118** (FIG. **2**) and the I/O interface **432** operating synchronously with the external world of memory and I/O devices. The CPU **70** executes at the fastest speed possible using the adaptive ring counter clock **430**. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor **50** for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface **432**, speed of which is controlled by a conventional crystal clock **434**. The interface **432** processes requests for memory accesses from the microprocessor **50** and acknowledges the presence of I/O data. The microprocessor **50** fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. By decoupling the variable speed of the CPU **70** from the fixed speed of the I/O interface **432**, optimum performance can be achieved by each. Recoupling between the CPU **70** and the interface **432** is accomplished with handshake signals on lines **436**, with data/addresses passing on bus **90**, **136**.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

Claims **3**–**5** and **8** are cancelled.

Claims **1**, **6** and **10** are determined to be patentable as amended.

Claims **2**, **7** and **9**, dependent on an amended claim, are determined to be patentable.

New claims **11**–**16** are added and determined to be patentable.

1. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, *wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.*

6. A microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an *off-chip* external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an *off-chip* external clock, independent of said oscillator, connected to said input/output interface wherein said *off-chip* external clock is operative at a frequency independent of a clock frequency of said oscillator *and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.*

10. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an **[**on chip**]** *on-chip* input/output interface between said central processing unit and an *off-chip* external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an *off-chip* external clock wherein said *off-chip* external clock is operative at a frequency independent of a clock frequency of said variable speed clock *and wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock.*

11. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein said central processing unit operates asynchronously to said input/output interface.

12. The microprocessor system of claim 11, in which said second clock is a fixed frequency clock.

13. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;

an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and further wherein said central processing unit operates asynchronously to said input/output interface.

14. The microprocessor system of claim 13 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

15. The microprocessor system of claim 13 wherein said oscillator comprises a ring oscillator.

16. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock, wherein said central processing unit operates asychronously to said input/output interface.

* * * * *

US005809336C2

(12) EX PARTE REEXAMINATION CERTIFICATE (7887th)

United States Patent
Moore et al.

(10) **Number: US 5,809,336 C2**
(45) **Certificate Issued: Nov. 23, 2010**

(54) **HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK**

(75) Inventors: **Charles H. Moore**, 410 Star Hill Rd., Woodside, CA (US) 94062; **Russell H. Fish, III**, Mt. View, CA (US)

(73) Assignee: **Charles H. Moore**, Incline Village, NV (US)

Reexamination Request:
No. 90/009,457, Aug. 24, 2009

Reexamination Certificate for:

Patent No.:	**5,809,336**
Issued:	**Sep. 15, 1998**
Appl. No.:	**08/484,918**
Filed:	**Jun. 7, 1995**

Reexamination Certificate C1 5,809,336 issued Dec. 15, 2009

Certificate of Correction issued May 22, 2007.

Related U.S. Application Data

(62) Division of application No. 07/389,334, filed on Aug. 3, 1989, now Pat. No. 5,440,749.

(51) **Int. Cl.**

G06F 7/76	(2006.01)
G06F 7/48	(2006.01)
G06F 12/08	(2006.01)
G06F 7/78	(2006.01)
G06F 9/30	(2006.01)
G06F 9/32	(2006.01)
G06F 15/76	(2006.01)
G06F 15/78	(2006.01)
G06F 7/52	(2006.01)
G06F 9/38	(2006.01)
G06F 7/58	(2006.01)

(52) **U.S. Cl.** **710/25**; 711/E12.02; 712/E9.016; 712/E9.028; 712/E9.046; 712/E9.055; 712/E9.057; 712/E9.058; 712/E9.062; 712/E9.078; 712/E9.08; 712/E9.081

(58) **Field of Classification Search** ..... None
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,348,743	A	9/1982	Dozier
4,691,124	A	9/1987	Ledzius et al.
4,766,567	A	8/1988	Kato
4,853,841	A	8/1989	Richter
4,931,748	A	6/1990	McDermott et al.
5,809,336	A	9/1998	Moore et al.

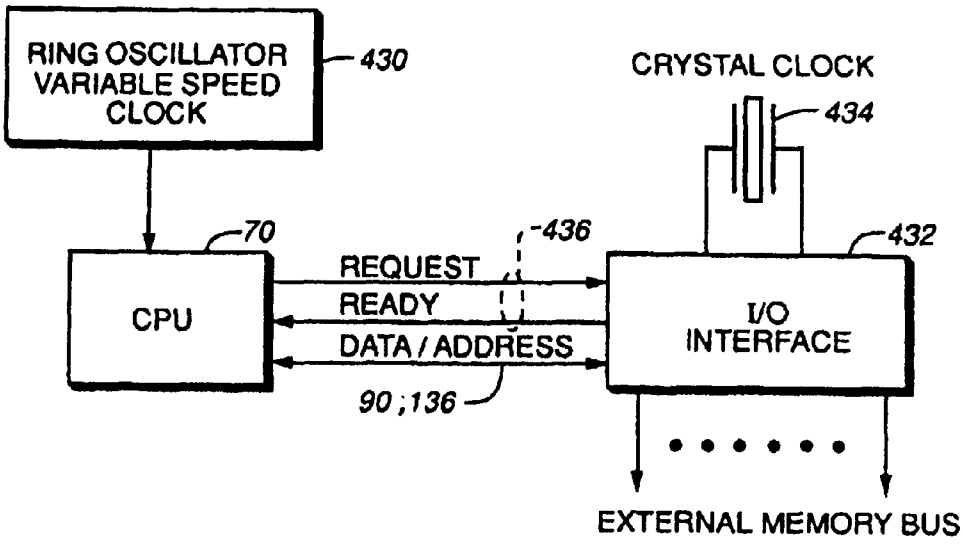
OTHER PUBLICATIONS

U.S. Patent No. 5,809,336, as certified by Ex Parte Reexamination Certificate (7235th) U.S. 5,809,336 C1, issued Dec. 15, 2009, 51 pages.
In re Recreative Technologies Corp., 83 F.3d 1394, 38 USPQ 2.d 1776 (Fed. Cir. 1996), 6 pages.

Primary Examiner—B. James Peikari

(57) **ABSTRACT**

A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and the ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.



EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

NO AMENDMENTS HAVE BEEN MADE TO THE PATENT

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claims **1**, **2**, **6**, **7** and **9-16** is confirmed.

Claims **3-5** and **8** were previously cancelled.

* * * * *

Exhibit “I”

(Counsel listed on signature page)

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN JOSE DIVISION

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. BARNES & NOBLE, INC., Defendants.	Case No. 3:12-cv-03863-VC (PSG) **PATENT LOCAL RULE 4-3 JOINT CLAIM CONSTRUCTION AND PREHEARING STATEMENT**
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. HUAWEI TECHNOLOGIES CO., LTD., HUAWEI DEVICE CO., LTD., HUAWEI DEVICE USA INC., FUTUREWEI TECHNOLOGIES, INC., HUAWEI TECHNOLOGIES USA INC., Defendants.	Case No. 3:12-cv-03865-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. GARMIN LTD., GARMIN INTERNATIONAL, INC., and GARMIN USA, INC., Defendants.	Case No. 3:12-cv-03870-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. ZTE CORPORATION and ZTE (USA) INC., Defendants.	Case No. 3:12-cv-03876-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. SAMSUNG ELECTRONICS CO., LTD. and SAMSUNG ELECTRONICS AMERICA, INC., Defendants.	Case No. 3:12-cv-03877-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. LG ELECTRONICS, INC. and LG ELECTRONICS U.S.A., INC., Defendants.	Case No. 3:12-cv-03880-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. NINTENDO CO., LTD. and NINTENDO OF AMERICA, INC., Defendants.	Case No. 3:12-cv-03881-VC (PSG)

Pursuant to the Court's Order Granting Defendants' Unopposed Motion to Modify Case Schedule, and to maximize the efficiency to the Court, the parties from all eight above-captioned related actions, Plaintiffs Phoenix Digital Solutions LLC, Patriot Scientific Corporation, and Technology Properties Limited LLC (collectively, "Plaintiffs"), and Defendants Barnes & Noble, Inc., Huawei Technologies Co., Ltd., Huawei Device Co., Ltd., Huawei Device USA Inc., Futurewei Technologies, Inc., Huawei Technologies USA Inc., Garmin International, Inc., Garmin USA, Inc., ZTE Corporation, ZTE (USA) Inc., Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., LG Electronics, Inc., LG Electronics U.S.A., Inc., Nintendo Co., Ltd., and Nintendo of America, Inc. (collectively, "Defendants") hereby submit the following Joint Claim Construction and Prehearing Statement pursuant to Patent Local Rule 4-3.

I. AGREED CLAIM CONSTRUCTION TERMS (Patent Local Rule 4-3(a))

Exhibit A sets forth a list of claim terms and their respective constructions that have been agreed upon by all the parties in the related actions.

II. DISPUTED CLAIM CONSTRUCTION TERMS (Patent Local Rule 4-3(b))

Exhibit B is a chart that sets forth disputed claim terms from U.S. Patent Nos. 5,440,749, 5,530,890, and 5,809,336, and the respective constructions proposed by each party. All three patents are at issue in the above-captioned related actions.

The proposed identification of evidence for each disputed claim term provided by plaintiffs Phoenix Digital Solutions LLC, Patriot Scientific Corporation and Technology Properties Limited LLC is attached hereto as Exhibit C.

The proposed identification of evidence for each disputed claim term provided by Defendants is attached hereto as Exhibit D.

III. IDENTIFICATION OF MOST SIGNIFICANT CLAIM TERMS (Patent Local Rule 4-3(c))

The Court has ordered the parties in all eight actions to identify the ten claim terms most significant to the resolution of the issues in the case. The parties have accordingly identified the following claim terms as being most significant to the resolution of the issues in that case at this time, including identification of which terms are believed to be case or claim dispositive:

1. instruction register ('749/'890 Patents)

2. means . . . for fetching instructions for said central processing unit integrated circuit on said bus from said memory, said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle ('749 Patent)

3. push down stack connected to said arithmetic logic unit ('749 Patent) / push down stack . . . connected to provide inputs to said arithmetic logic unit ('890 Patent)

4. address/data bus ('890 Patent)

5. an internal data bus, said internal data bus being bidirectionally connected to a [ ] ('890 Patent)

6. incrementer / decrementer ('890 Patent)

7. return push down stack ('890 Patent)

8. separate direct memory access central processing unit ('890 Patent)

9. X register / Y register ('890 Patent)

10. an entire oscillator disposed upon said integrated circuit substrate ('336 Patent)

Defendants believe that the construction of each of the above terms may be dispositive as to the claims in which those terms appear. Plaintiffs agree that the "means . . . for fetching" term listed as item 2 is claim dispositive for the claim in which it appears.

IV. ANTICIPATED LENGTH OF CLAIM CONSTRUCTION HEARING (Patent Local Rule 4-3(d))

The claim construction hearing has been scheduled for February 26, 2016 at 10:00 a.m. The technology tutorial has been scheduled for February 19, 2016 at 10:00 a.m.

Plaintiffs expect that the length of the claim construction hearing should be no more than 3 hours total (1.5 hours per side) and expect that the length for the tutorial should be no more than 1 hour (30 minutes per side).

Defendants request that Court provide the parties a full day, with equal time for each side, for the claim construction hearing. Although the Court has previously considered certain terms of

the Asserted Patents in a prior case, the present Defendants have not previously presented their positions, the majority of the terms listed in Section III have not been previously construed by the Court, and the asserted '749 and '890 Patents were not part of the trial in the prior case (indeed only one term from the previously tried '336 Patent is presented for construction here). For similar reasons, Defendants request that the Court provide two hours (one hour per side) for the technology tutorial.

V. WITNESSES FOR THE CLAIM CONSTRUCTION HEARING (Patent Local Rule 4-3(e))

Plaintiffs and Defendants do not currently plan to call any fact or expert witnesses to testify live at the claim construction hearing. However, to the extent that Plaintiffs or Defendants later decide that expert testimony is necessary and offer such testimony, then the parties agree that the other side may submit rebuttal expert testimony.

Respectfully submitted,

[SIGNATURE BLOCKS ON NEXT PAGE]

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ATTESTATION PER GENERAL ORDER 45

I, Barry J. Bumgardner, am the ECF User whose ID and password are being used to file this Stipulation. In compliance with General Order 45, X.B., I hereby attest that the counsel listed above have concurred with this filing.

Dated: June 23, 2015

Exhibit “J”

United States Patent [19]

Magar

[11] **Patent Number: 4,503,500**

[45] **Date of Patent: Mar. 5, 1985**

[54] **MICROCOMPUTER WITH BUS INTERCHANGE MODULE**

[75] Inventor: **Surendar S. Magar**, Houston, Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **619,650**

[22] Filed: **Jun. 15, 1984**

Related U.S. Application Data

[63] Continuation of Ser. No. 347,860, Feb. 11, 1982.

[51] **Int. Cl.**³ **G06F 3/00**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** 364/200, 900

[56] **References Cited**

U.S. PATENT DOCUMENTS

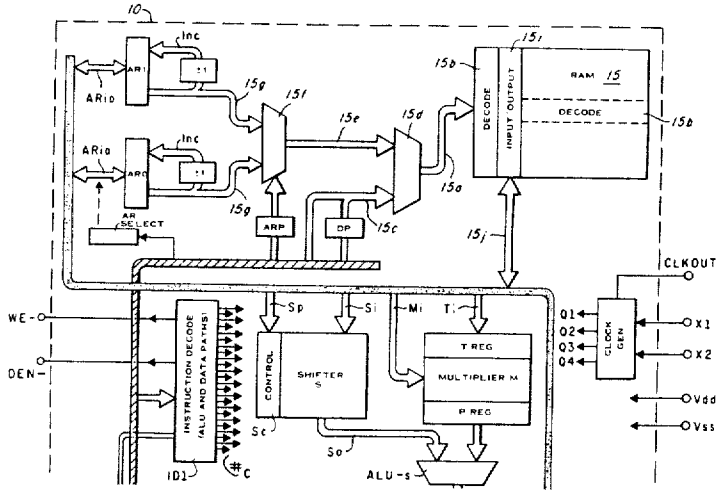
4,309,754	1/1982	Dinwiddie, Jr.	364/200
4,339,793	7/1982	Marenin	364/200
4,348,743	9/1982	Dozier	364/900
4,378,589	3/1983	Finnegan et al.	364/200

Primary Examiner—Gareth D. Shaw
Assistant Examiner—Ronni S. Malamud
Attorney, Agent, or Firm—John G. Graham

[57] **ABSTRACT**

A system for real-time digital signal processing employs a single-chip microcomputer device having separate on-chip program ROM and data RAM, with separate address and data paths for program and data. An external program address bus allows off-chip program fetch in an expansion mode, with the opcode returned by an external data bus. A bus interchange module allows transfer between the separate internal program and data busses in special circumstances. The internal busses are 16-bit, while the ALU and accumulator are 32-bit. A multiplier circuit produces a single state 16×16 multiply function separate from the ALU, with 32-bit output to the ALU. One input to the ALU passes through a 0-to-15 bit shifter with sign extension.

9 Claims, 15 Drawing Figures



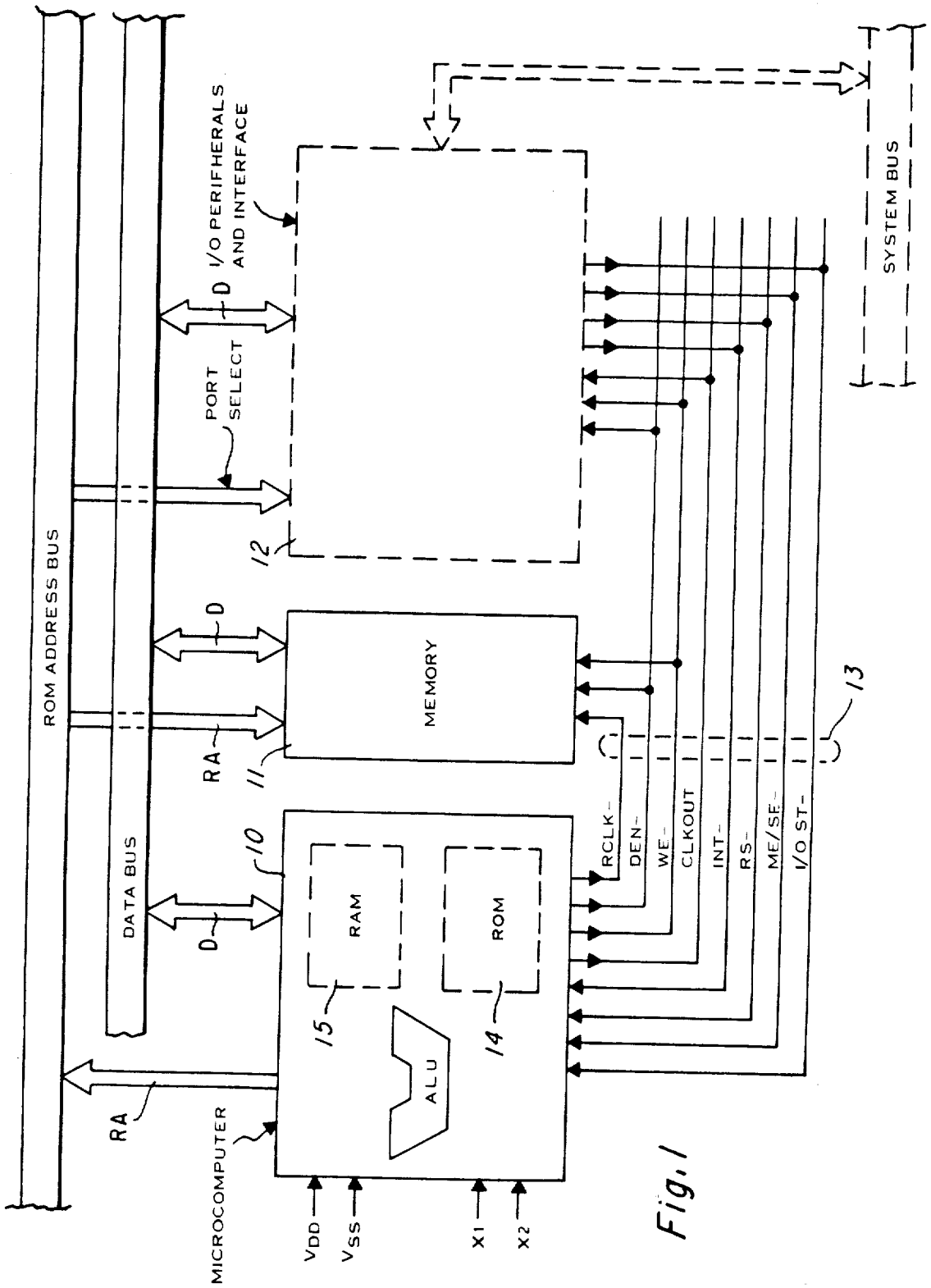

ROM ADDRESS BUS
DATA BUS
I/O PERIFHERALS AND INTERFACE
PORT SELECT
SYSTEM BUS
MEMORY
RAM
ROM
ALU
MICROCOMPUTER
RA
D
RCLK-
DEN-
WE-
CLKOUT
INT-
RS-
ME/SE-
I/O ST-
VDD
VSS
X1
X2
10
11
12
13
14
15

Fig. 1

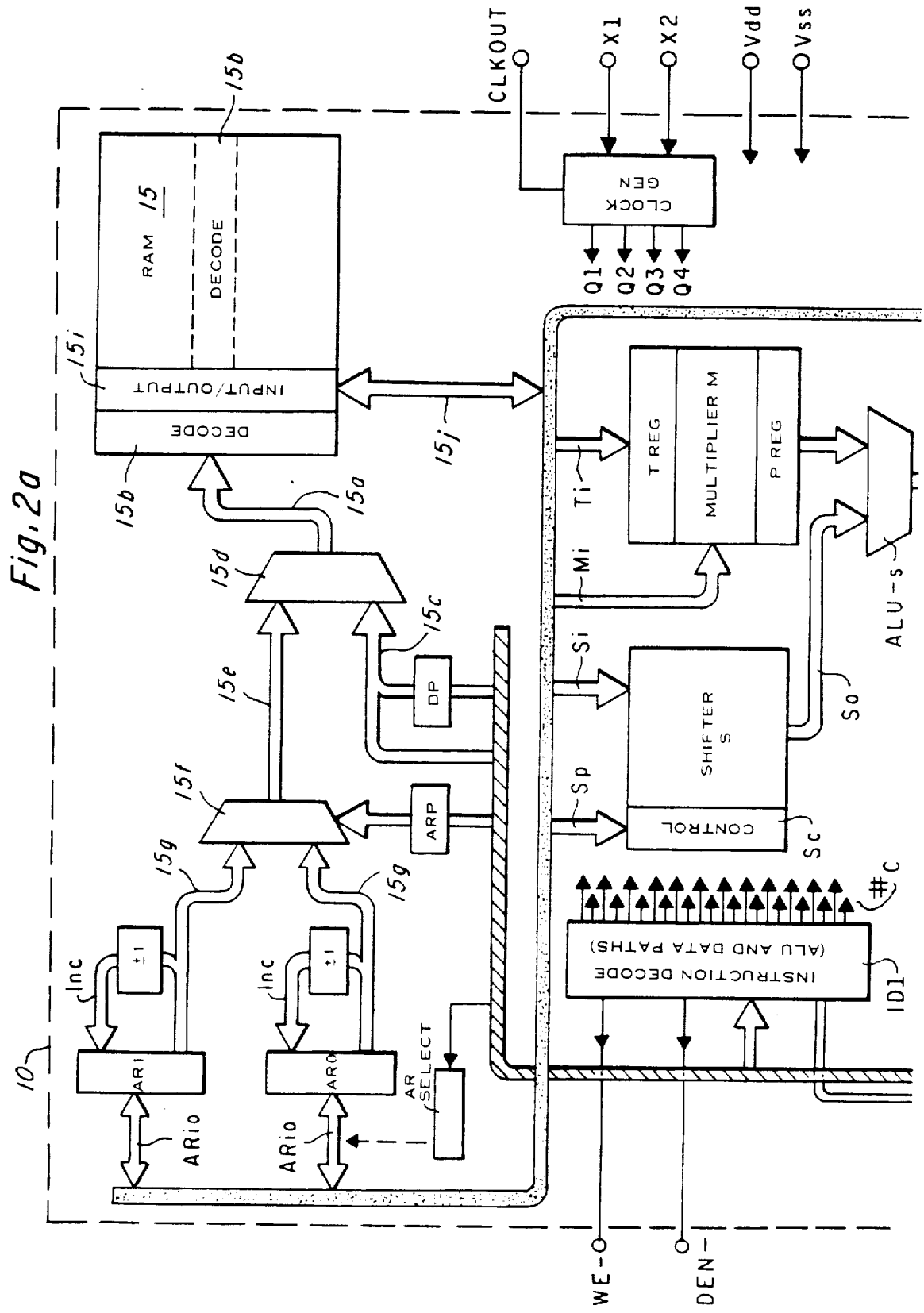


Fig. 2a
CLKOUT
X1
X2
Vdd
Vss
CLOCK GEN
Q1
Q2
Q3
Q4
15b
RAM 15
DECODE
15i
INPUT/OUTPUT
DECODE
15b
15a
15j
T REG
MULTIPLIER M
P REG
Ti
Mi
ALU-s
15d
15c
15e
DP
Si
SHIFTER S
So
15f
ARP
Sp
CONTROL
Sc
15g
15g
#c
INSTRUCTION DECODE (ALU AND DATA PATHS)
ID1
Inc
±1
Inc
±1
10
AR1
AR0
AR SELECT
AR1o
AR0o
WE-
DEN-

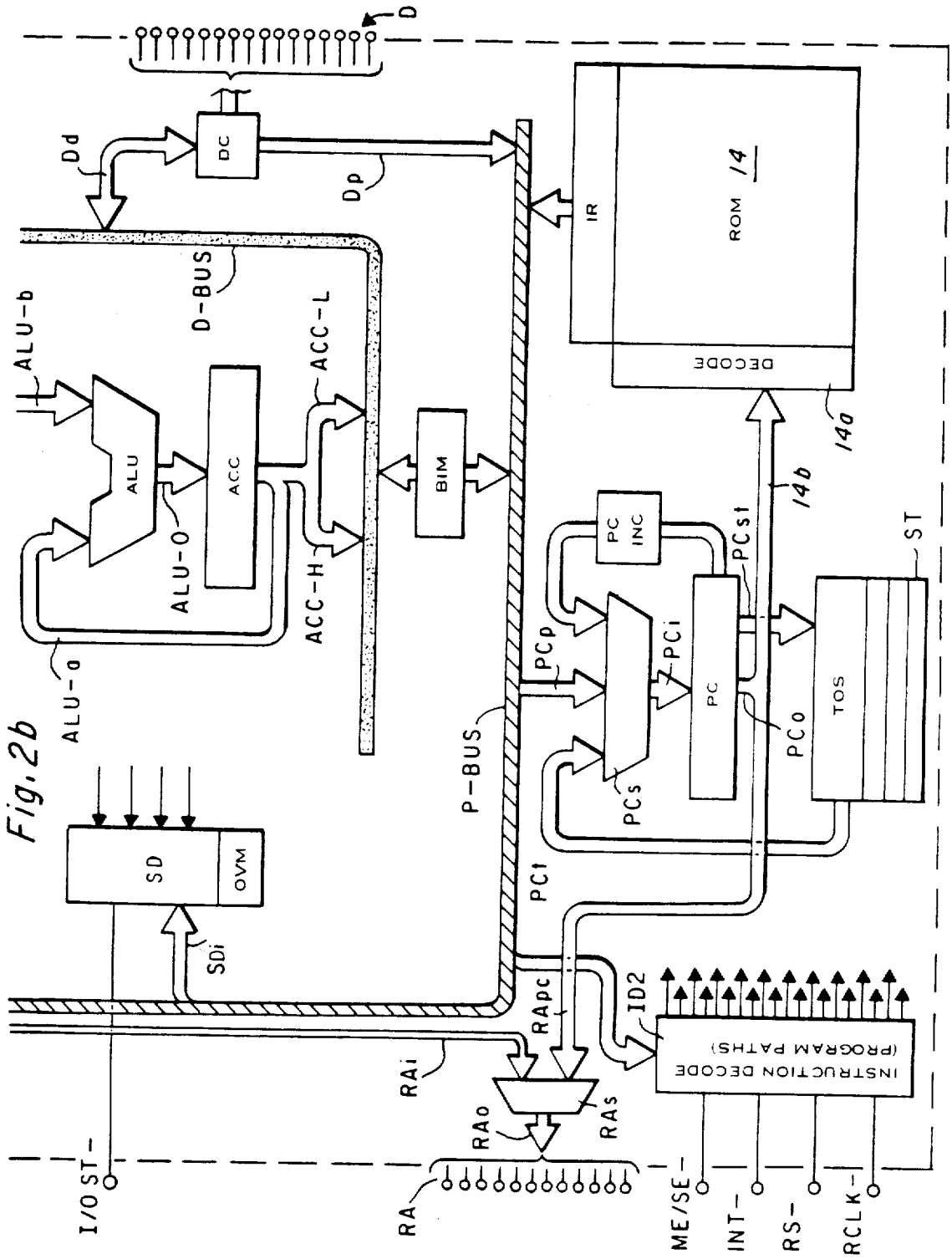

D
Dd
DC
Dp
IR
ROM 14
DECODE
14a
14b
D-BUS
ALU-b
ALU
ACC
ACC-L
ACC-H
ALU-o
ALU-0
BIM
PC INC
PCst
ST
PCp
PCi
PC
PCo
TOS
PCs
P-BUS
PC1
SD
OVM
SDi
RApc
ID2
INSTRUCTION DECODE
(PROGRAM PATHS)
RAi
RAo
RAs
RA
I/O ST-
ME/SE-
INT-
RS-
RCLK-

Fig. 2b

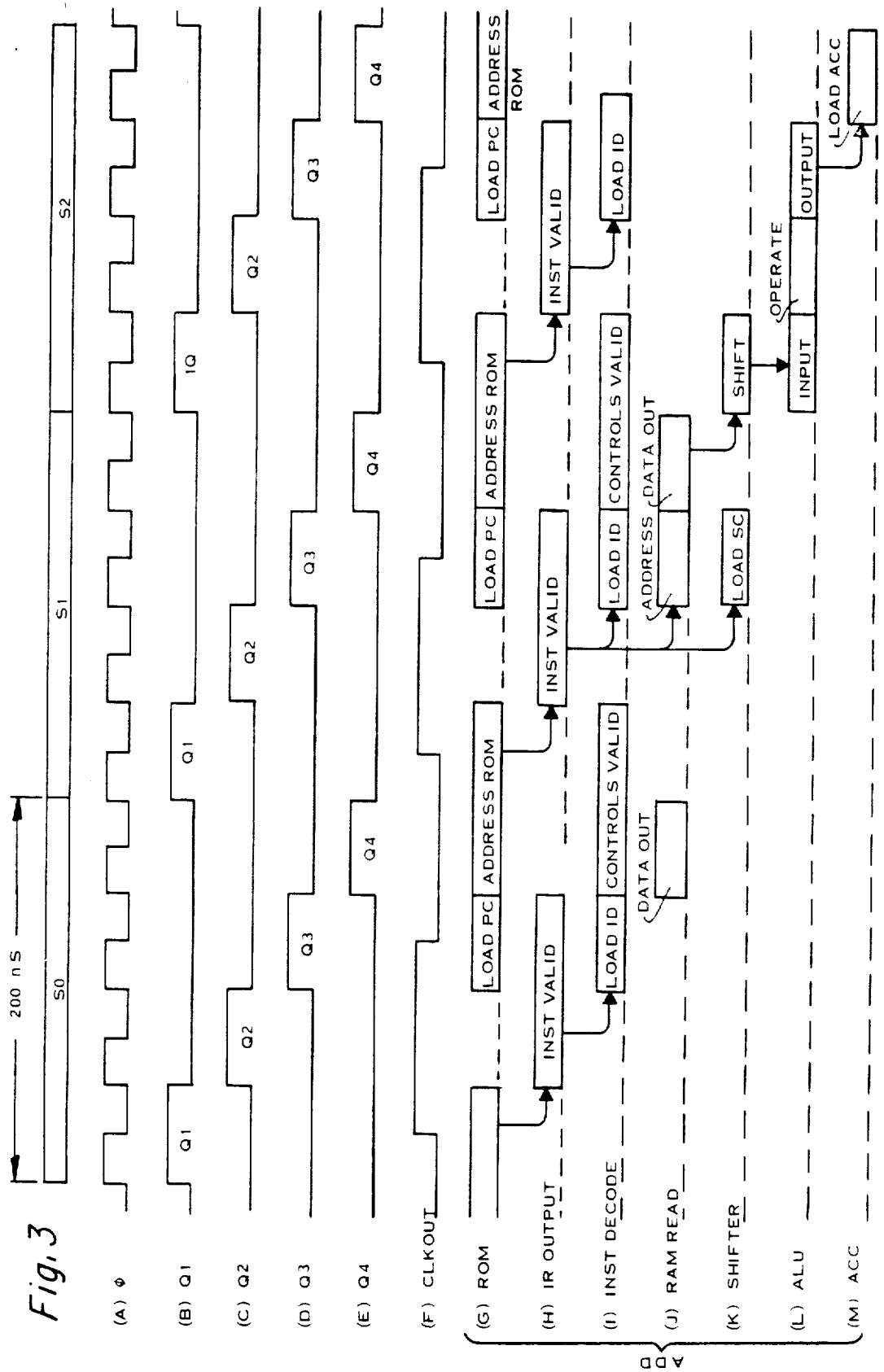

200 nS
S0
S1
S2
(A) Φ
(B) Q1
(C) Q2
(D) Q3
(E) Q4
(F) CLKOUT
(G) ROM
(H) IR OUTPUT
(I) INST DECODE
(J) RAM READ
(K) SHIFTER
(L) ALU
(M) ACC
LOAD PC
ADDRESS ROM
INST VALID
LOAD ID
CONTROLS VALID
DATA OUT
LOAD SC
SHIFT
OPERATE
INPUT
OUTPUT
LOAD ACC

Fig. 3

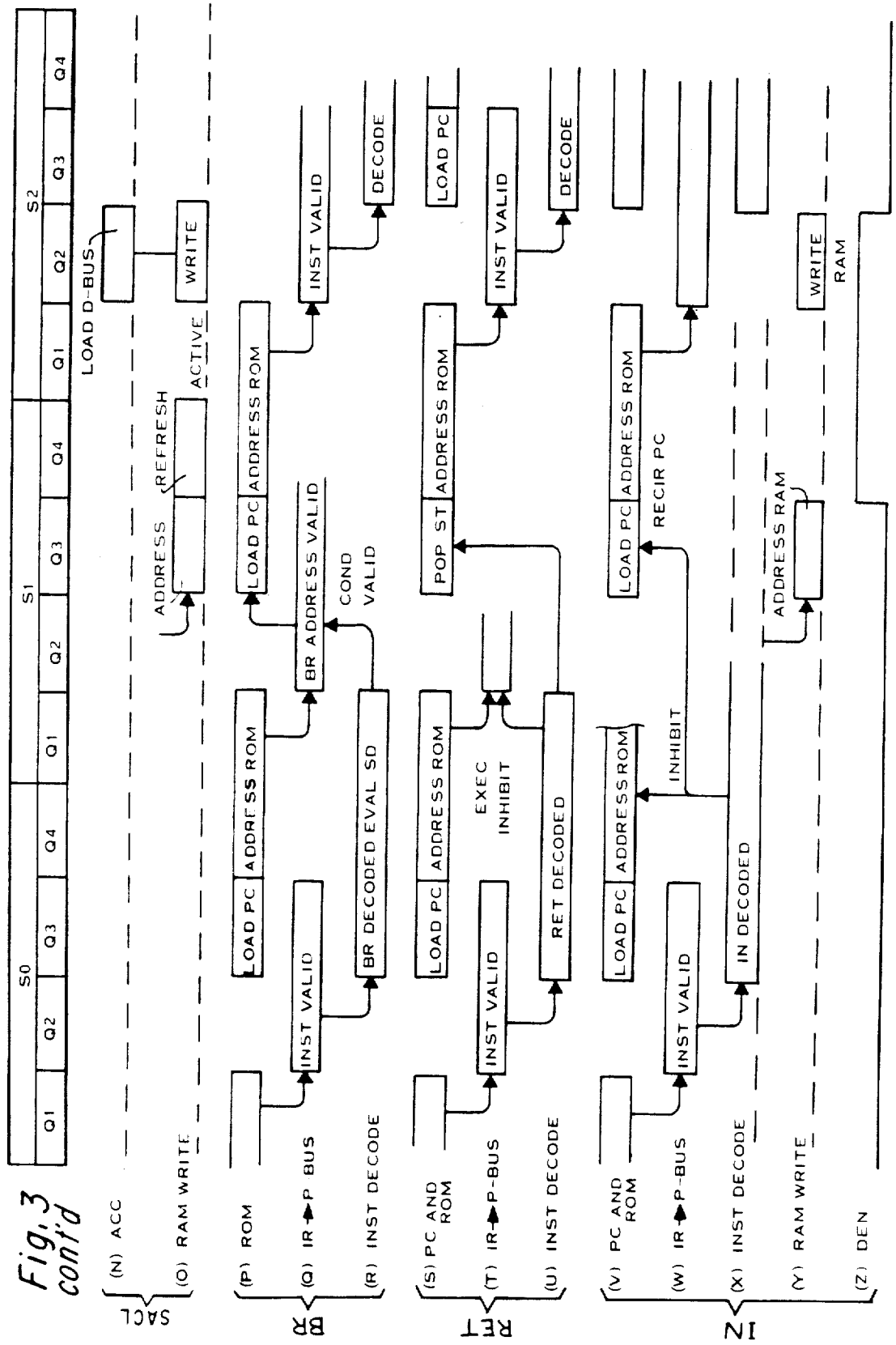

S0
S1
S2
Q1
Q2
Q3
Q4
LOAD D-BUS
ADDRESS
REFRESH
ACTIVE
WRITE
(N) ACC
(O) RAM WRITE
SACL
LOAD PC
ADDRESS ROM
INST VALID
DECODE
BR ADDRESS VALID
COND VALID
(P) ROM
(Q) IR→P BUS
(R) INST DECODE
BR DECODED EVAL SD
POP ST
EXEC INHIBIT
RET DECODED
(S) PC AND ROM
(T) IR→P-BUS
(U) INST DECODE
RET
RECIR PC
INHIBIT
(V) PC AND ROM
(W) IR→P-BUS
(X) INST DECODE
IN DECODED
ADDRESS RAM
(Y) RAM WRITE
WRITE RAM
(Z) DEN
IN

Fig. 3 cont'd

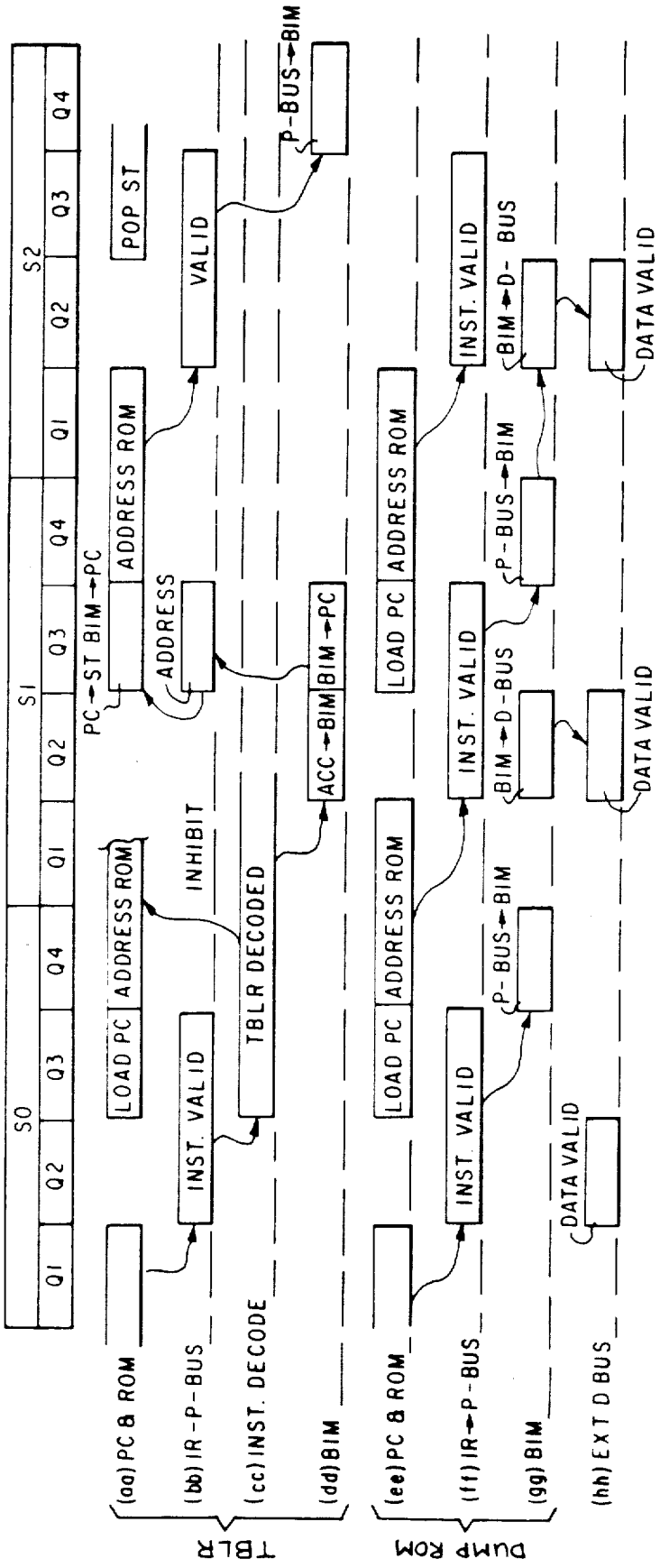

S0
S1
S2
Q1
Q2
Q3
Q4
(aa) PC & ROM
(bb) IR-P-BUS
(cc) INST. DECODE
(dd) BIM
TBLR
LOAD PC
ADDRESS ROM
INST. VALID
TBLR DECODED
INHIBIT
PC→ST BIM→PC
ADDRESS
VALID
POP ST
P-BUS→BIM
ACC→BIM
BIM→PC
(ee) PC & ROM
(ff) IR→P-BUS
(gg) BIM
(hh) EXT D BUS
DUMP ROM
BIM→D-BUS
DATA VALID
P-BUS→BIM

Fig. 3 (cont'd)

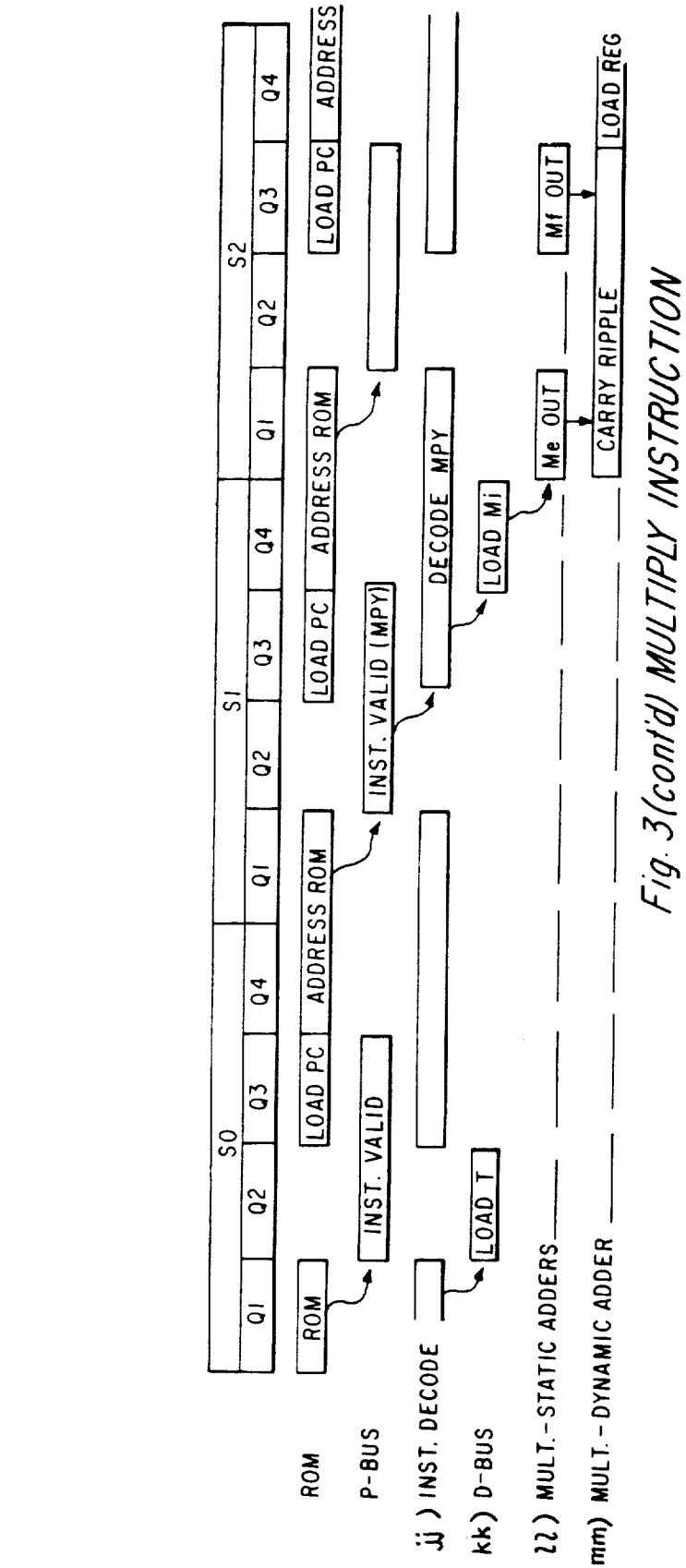


Fig. 3(cont'd) MULTIPLY INSTRUCTION

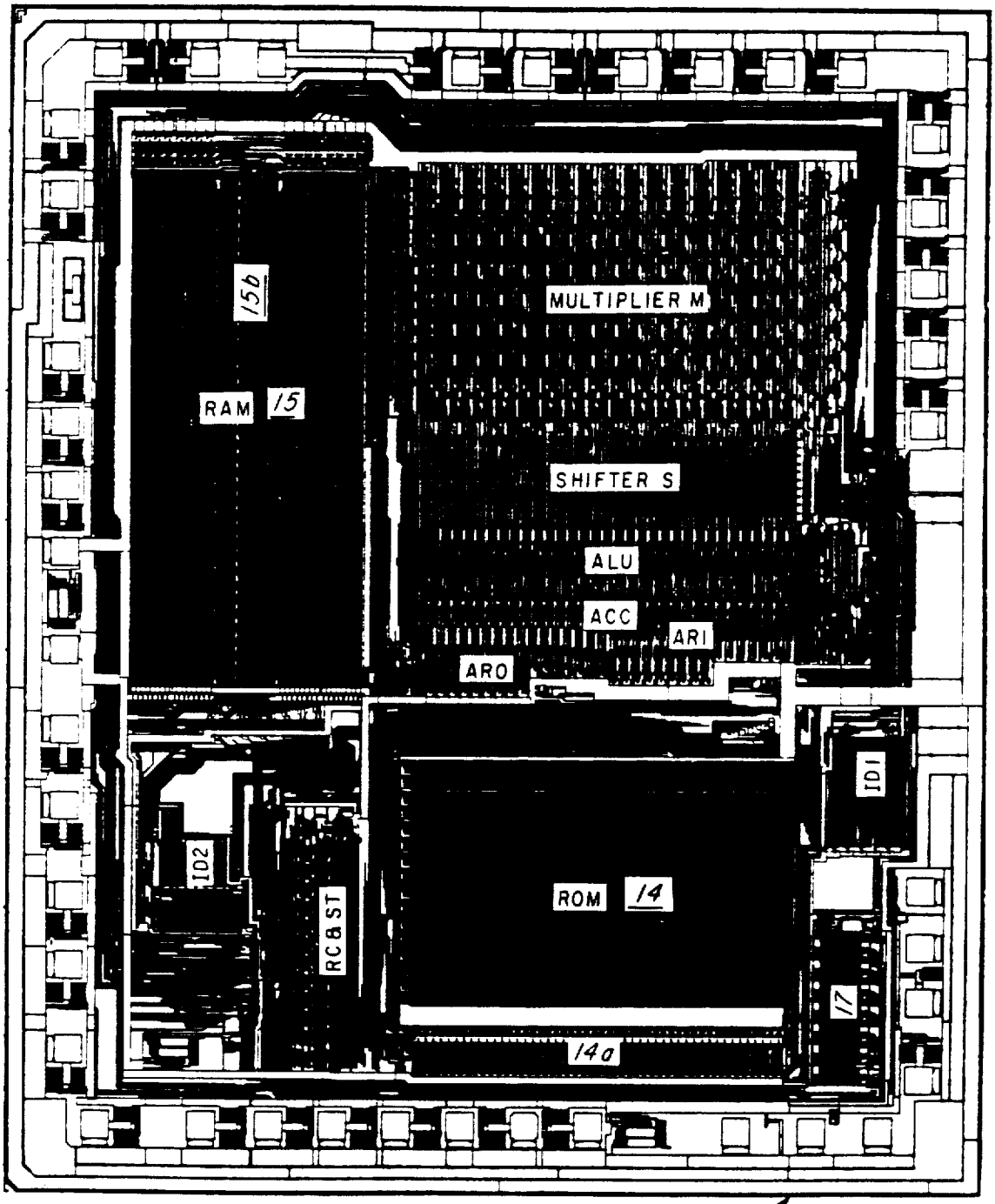

15b
MULTIPLIER M
RAM 15
SHIFTER S
ALU
ACC
ARI
ARO
ID1
ID2
RC & ST
ROM 14
17
14a

Fig. 4

10

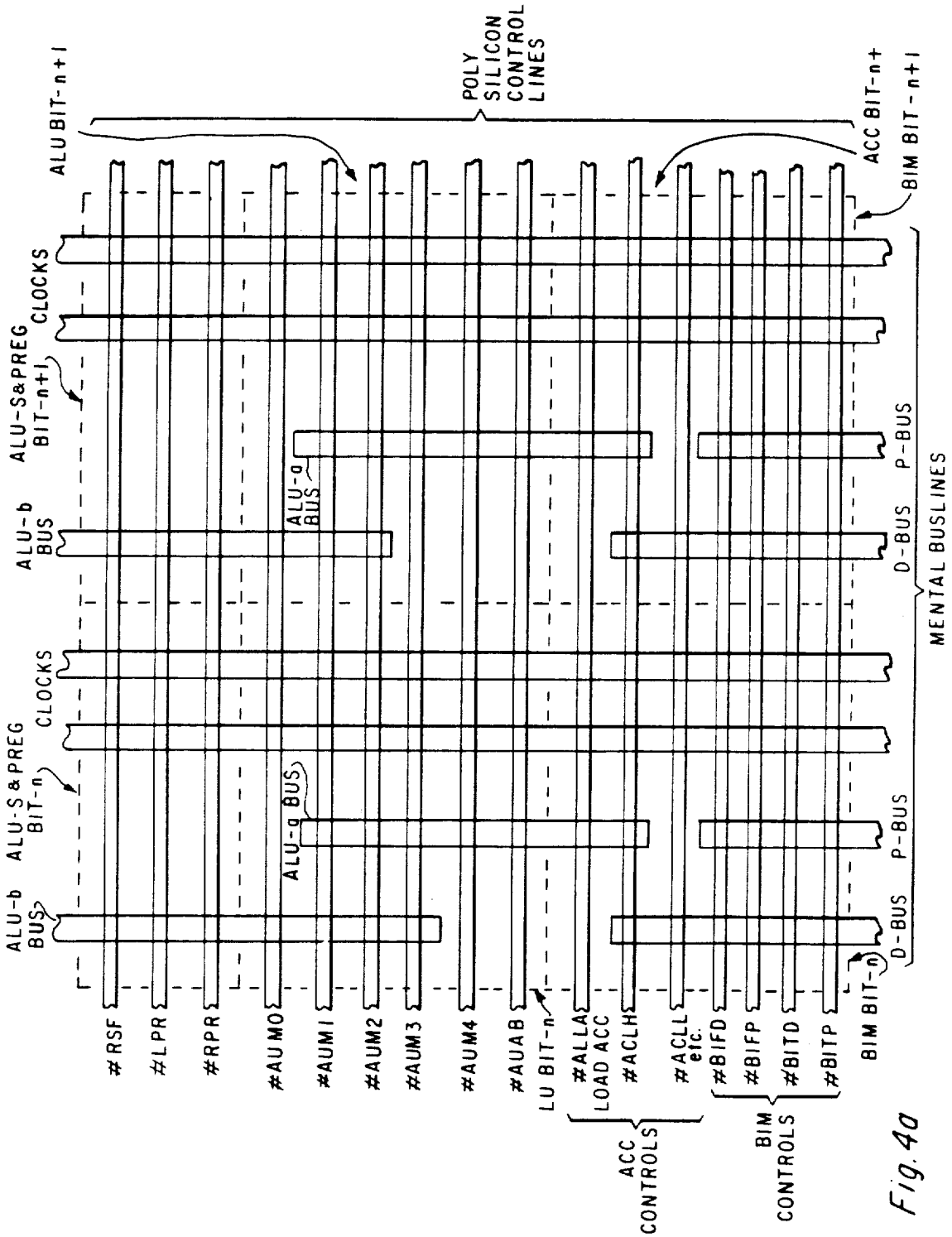

ALU BIT-n+1
POLY SILICON CONTROL LINES
ACC BIT-n+
BIM BIT-n+1
ALU-S&PREG CLOCKS
ALU-S&PREG BIT-n+1
ALU-b BUS
ALU-a BUS
D-BUS P-BUS
MENTAL BUSLINES
ALU-S&PREG CLOCKS
ALU-S&PREG BIT-n
ALU-b BUS
ALU-a BUS
D-BUS P-BUS
#RSF
#LPR
#RPR
#AUMO
#AUM1
#AUM2
#AUM3
#AUM4
#AUAB
LU BIT-n
#ALLA LOAD ACC
#ACLH
#ACLL etc.
ACC CONTROLS
#BIFD
#BIFP
#BITD
#BITP
BIM CONTROLS
BIM BIT-n

Fig. 4a

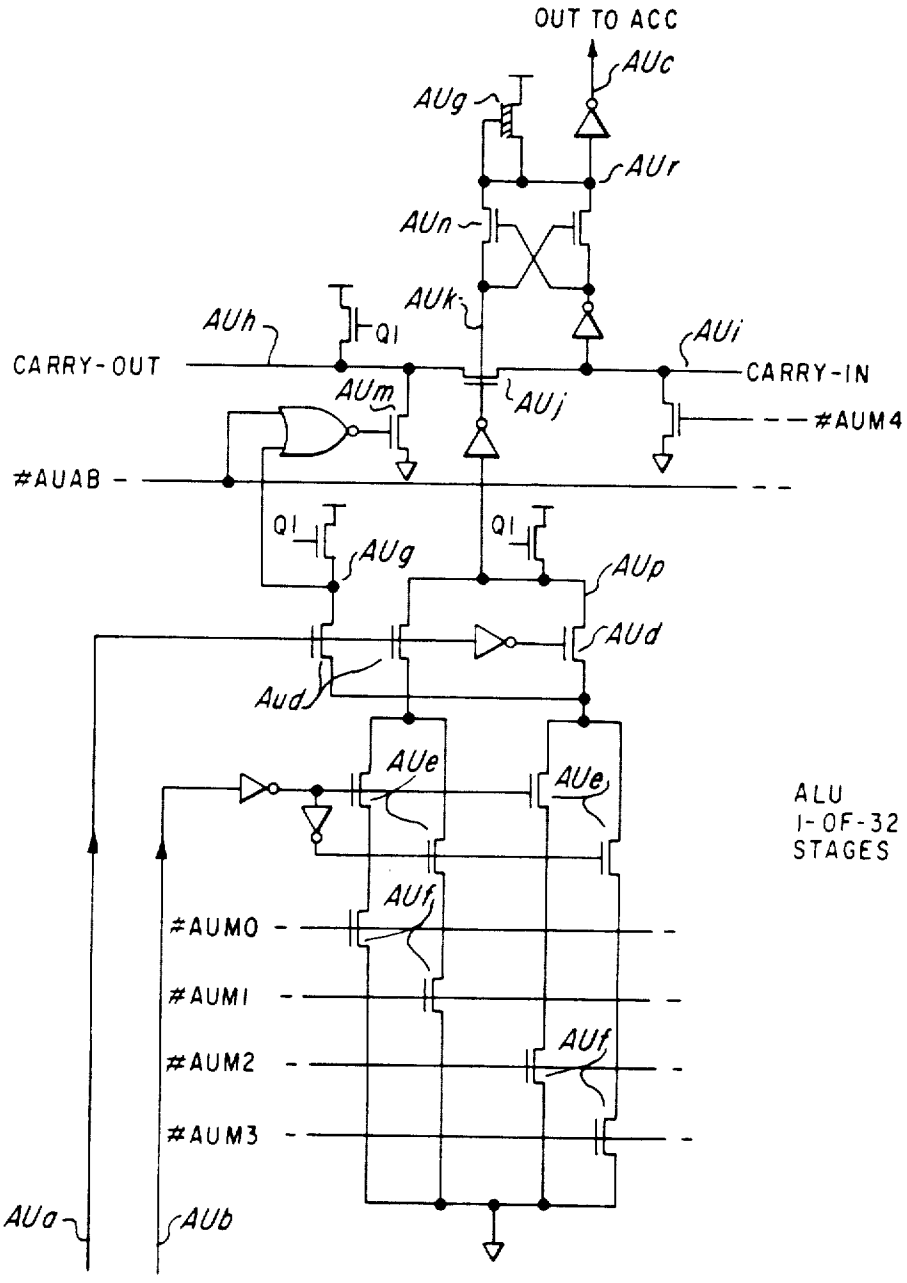

OUT TO ACC
AUc
AUg
AUr
AUn
AUk
AUh
Q1
AUi
CARRY-OUT
AUm
AUj
CARRY-IN
#AUM4
#AUAB
Q1
Q1
AUg
AUp
AUd
Aud
AUe
AUe
ALU
1-OF-32
STAGES
AUf
#AUM0
#AUM1
AUf
#AUM2
#AUM3
AUa
AUb

Fig. 5a

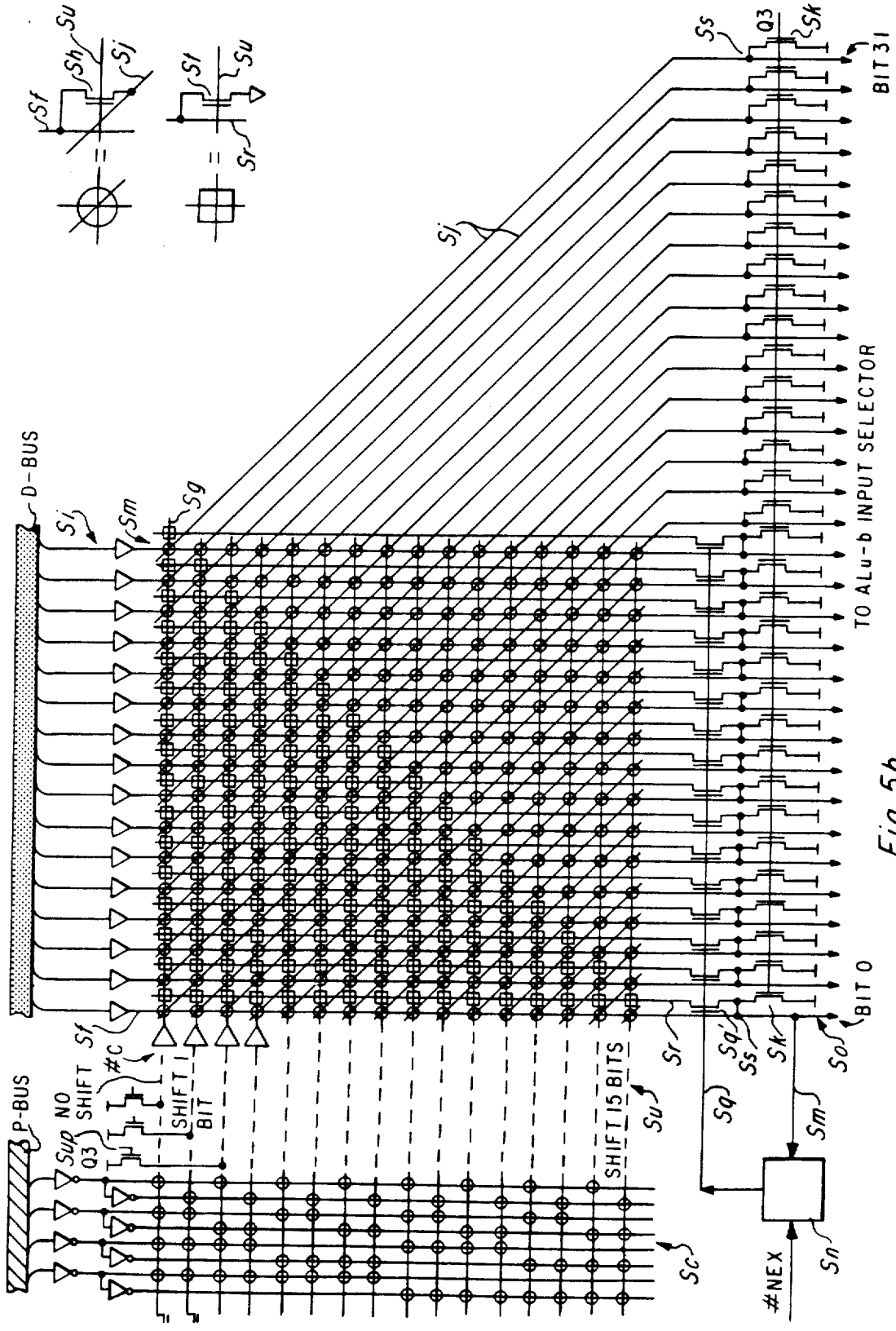
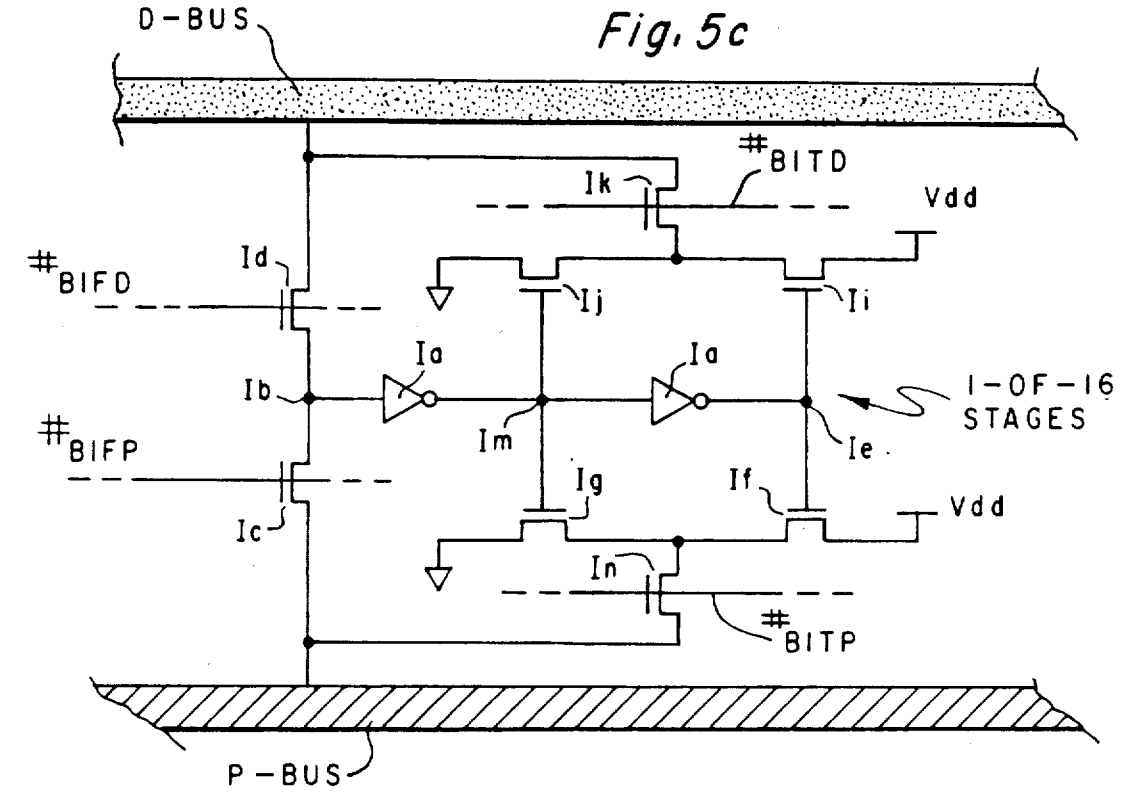

Su
Sh
Sj
Sf
Sl
Su
Sr
Sj
Ss
Q3
Sk
BIT 31
TO ALu-b INPUT SELECTOR
D-BUS
Sj
Sm
Sg
Sf
#C
SHIFT 1 BIT
SHIFT 15 BITS
Su
Sr
Sq'
Ss
Sk
So
BIT 0
P-BUS
Sup
NO SHIFT
Q3
Sq
Sm
Sc
#NEX
Sn

Fig. 5b

Fig. 5c


D-BUS
#BITD
Ik
Vdd
#BIFD
Id
Ij
Ii
Ia
Ia
Ib
I-OF-16
STAGES
#BIFP
Im
Ie
Ig
If
Vdd
Ic
In
#BITP
P-BUS

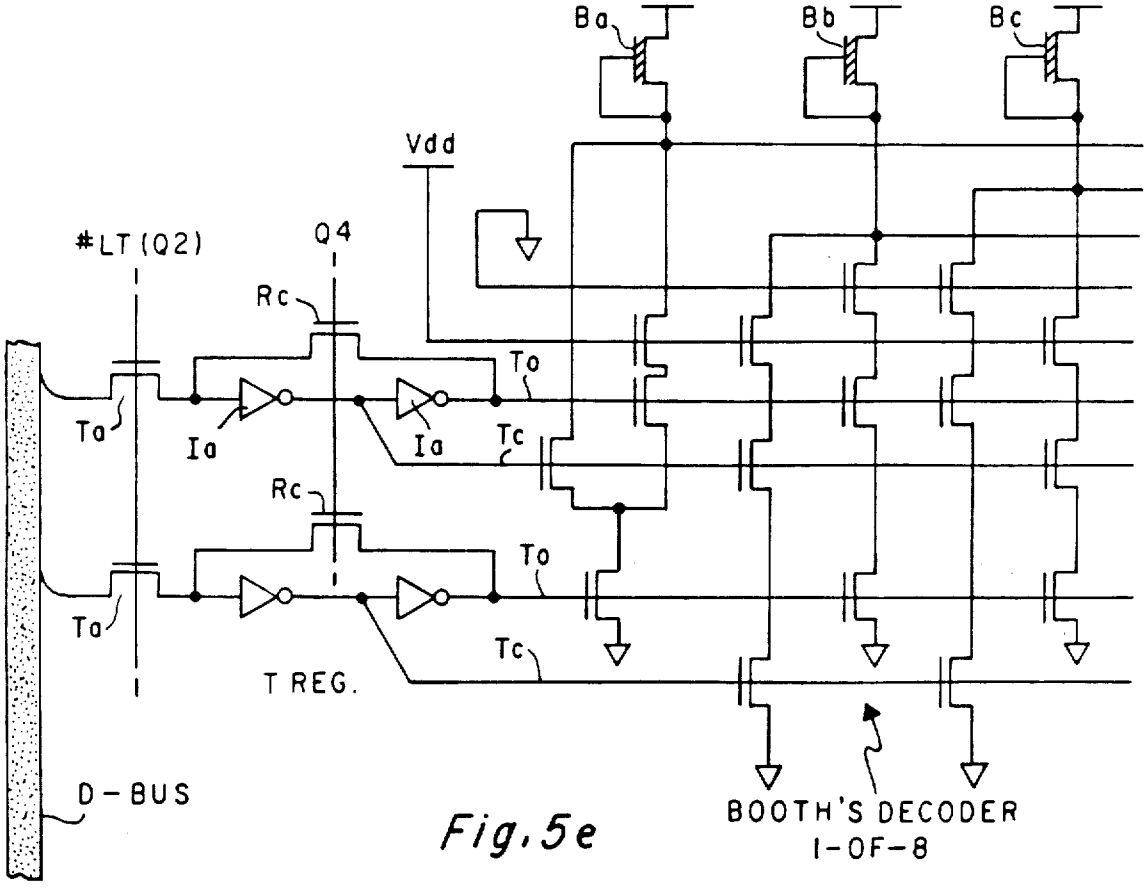

Ba
Bb
Bc
Vdd
#LT(Q2)
Q4
Rc
To
Ta
Ia
Ia
Tc
Rc
To
Ta
Tc
T REG.
D-BUS
BOOTH'S DECODER
I-OF-8

Fig. 5e

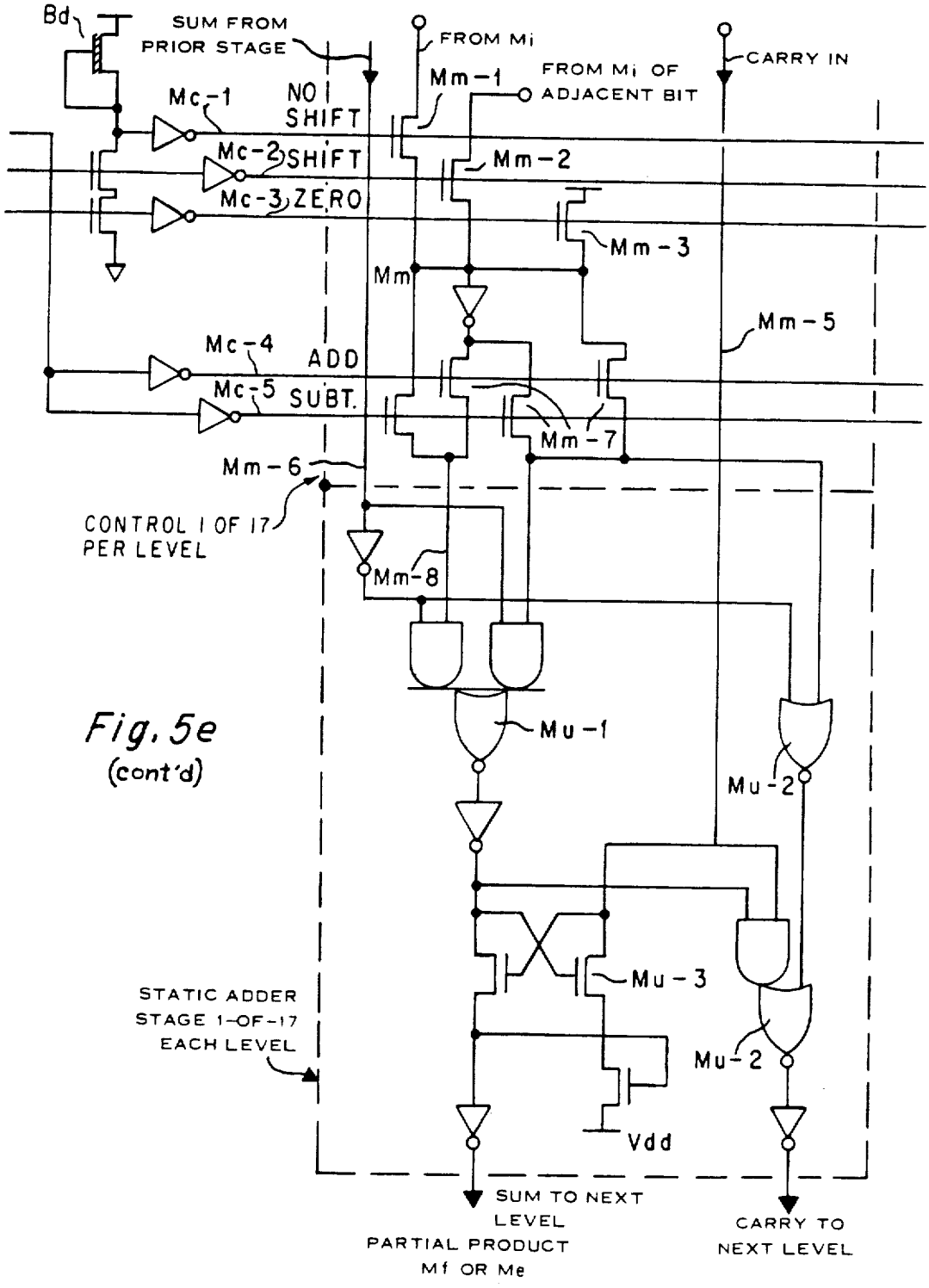

Bd
SUM FROM PRIOR STAGE
FROM Mi
FROM Mi OF ADJACENT BIT
CARRY IN
Mm-1
Mc-1
NO SHIFT
Mc-2 SHIFT
Mc-3 ZERO
Mm-2
Mm-3
Mm
Mm-5
Mc-4
ADD
Mc-5 SUBT.
Mm-7
Mm-6
CONTROL 1 OF 17 PER LEVEL
Mm-8
Mu-1
Mu-2
Mu-3
Mu-2
STATIC ADDER STAGE 1-OF-17 EACH LEVEL
Vdd
SUM TO NEXT LEVEL PARTIAL PRODUCT Mf OR Me
CARRY TO NEXT LEVEL

Fig. 5e (cont'd)

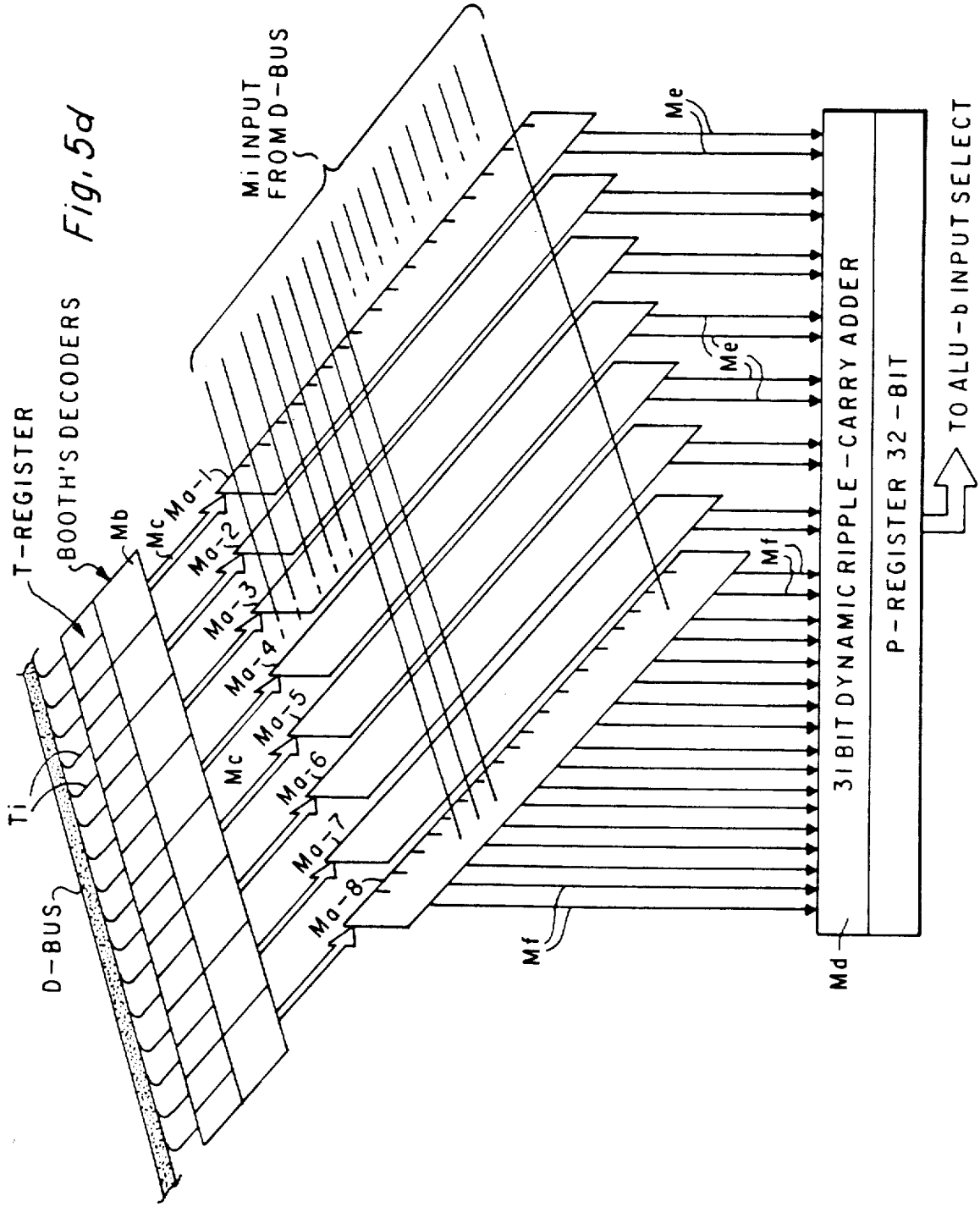


Fig. 5d
Mi INPUT FROM D-BUS
Me
Me
Mf
T-REGISTER
BOOTH'S DECODERS
Mb
Mc Mo-1
Mo-2
Mo-3
Mo-4
Mc Mo-5
Mo-6
Mo-7
Mo-8
Ti
D-BUS
Mf
31 BIT DYNAMIC RIPPLE-CARRY ADDER
P-REGISTER 32-BIT
Md
TO ALU-b INPUT SELECT

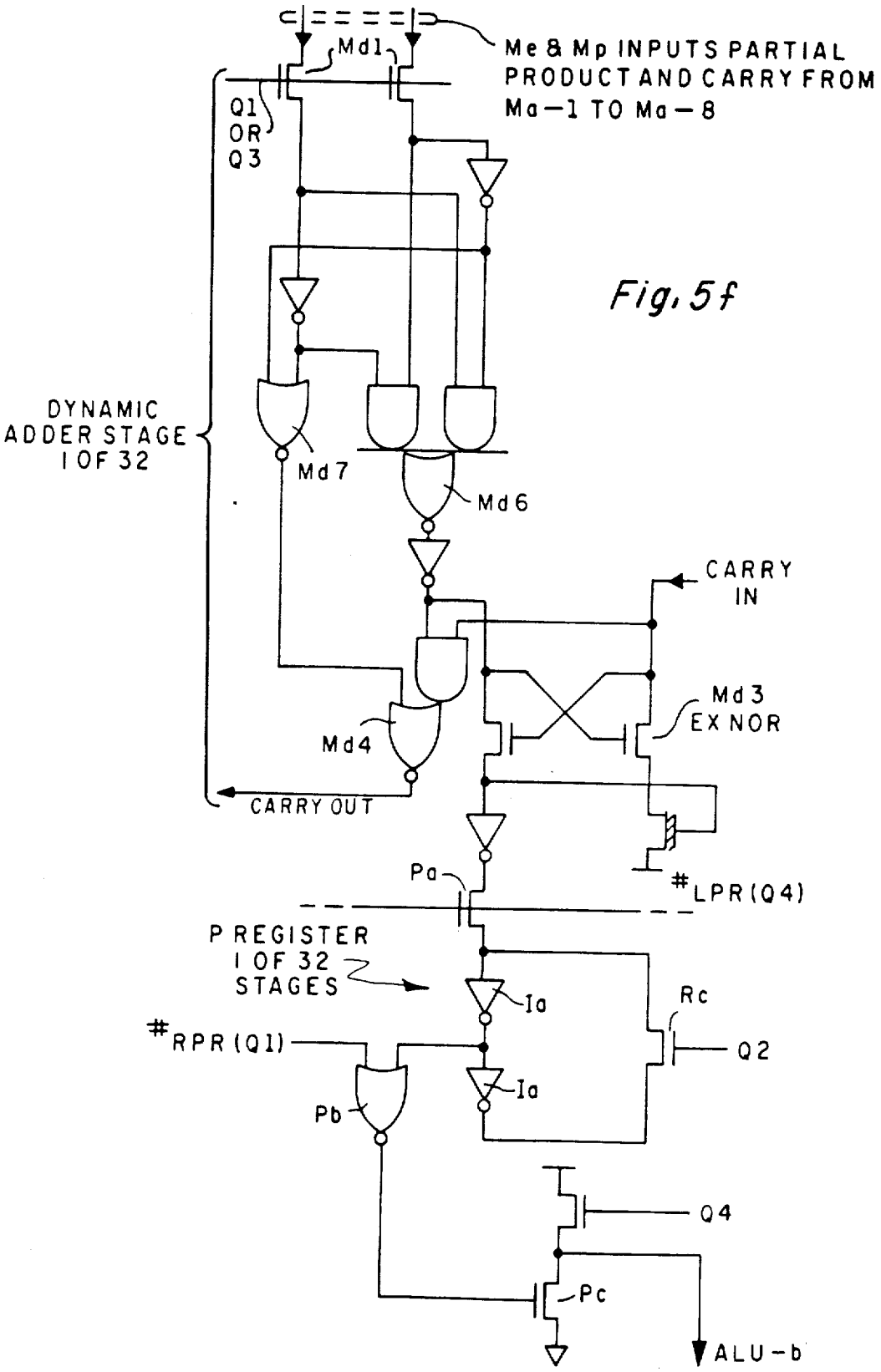

Me & Mp INPUTS PARTIAL PRODUCT AND CARRY FROM Ma−1 TO Ma−8
Md1
Q1 OR Q3
DYNAMIC ADDER STAGE 1 OF 32
Md7
Md6
CARRY IN
Md3 EX NOR
Md4
CARRY OUT
Pa
#LPR(Q4)
P REGISTER 1 OF 32 STAGES
Ia
Rc
#RPR(Q1)
Q2
Ia
Pb
Q4
Pc
ALU−b

Fig. 5f

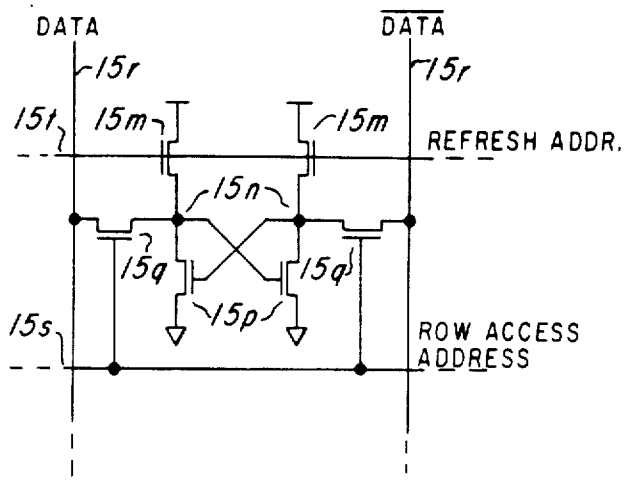

DATA
DATA
15r
15r
15t
15m
15m
REFRESH ADDR.
15n
15q
15q
15p
15s
ROW ACCESS ADDRESS

Fig. 5g

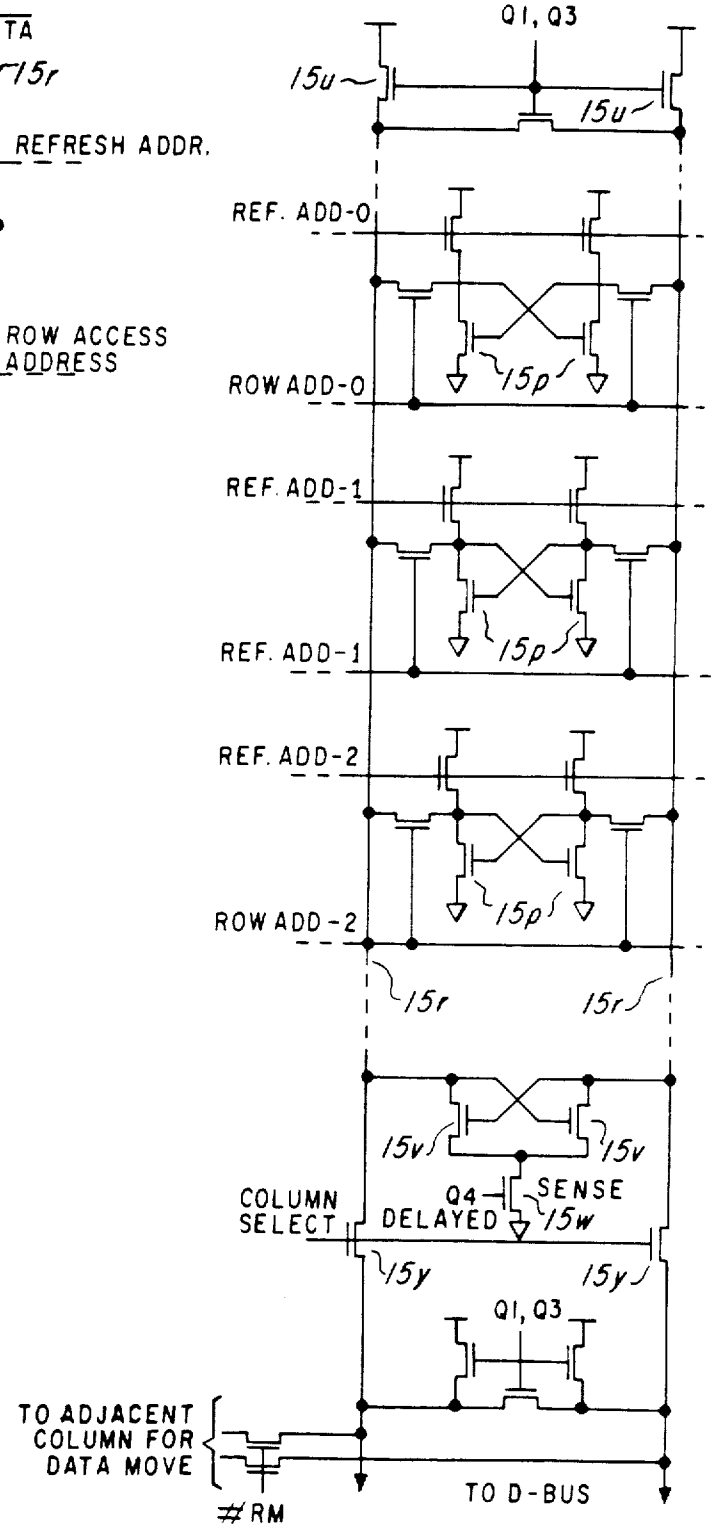

Q1, Q3
15u
15u
REF. ADD-0
15p
ROW ADD-0
REF. ADD-1
15p
REF. ADD-1
REF. ADD-2
15p
ROW ADD-2
15r
15r
15v
15v
COLUMN SELECT
Q4 DELAYED
SENSE
15w
15y
15y
Q1, Q3
TO ADJACENT COLUMN FOR DATA MOVE
TO D-BUS
#RM

Fig. 5h

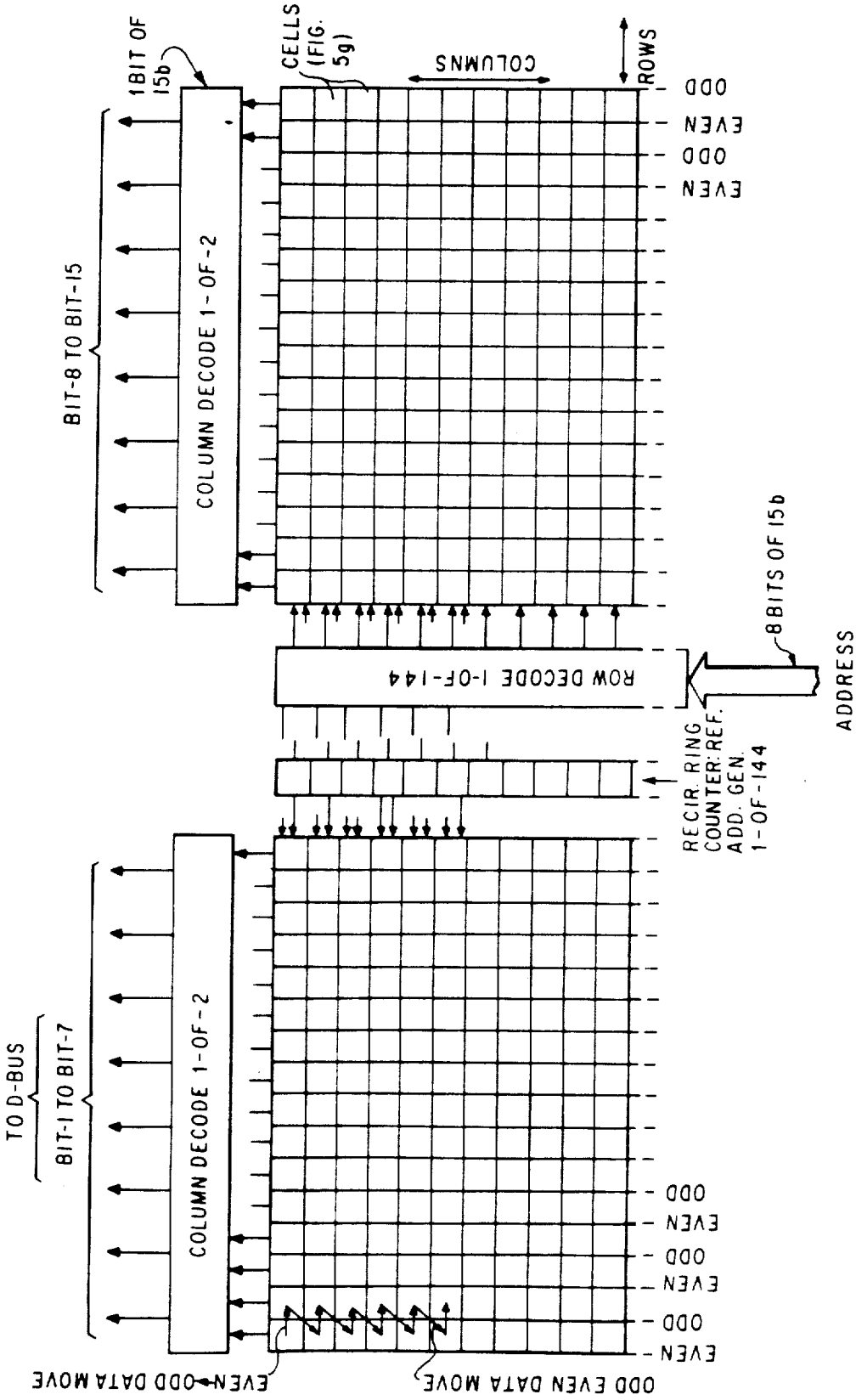

1 BIT OF 15b
CELLS (FIG. 5g)
COLUMNS
ROWS
ODD
EVEN
ODD
EVEN
BIT-8 TO BIT-15
COLUMN DECODE 1-OF-2
8 BITS OF 15b
ADDRESS
ROW DECODE 1-OF-144
RECIR. RING COUNTER: REF. ADD. GEN. 1-OF-144
TO D-BUS
BIT-1 TO BIT-7
COLUMN DECODE 1-OF-2
ODD
EVEN
ODD
EVEN
ODD
EVEN
EVEN-ODD DATA MOVE
ODD EVEN DATA MOVE

Fig. 5i

MICROCOMPUTER WITH BUS INTERCHANGE MODULE

This is a continuation of application Ser. No. 347,860, filed Feb. 11, 1982.

BACKGROUND OF THE INVENTION

This invention relates to integrated semiconductor devices and systems, and more particularly to a high-speed, miniaturized, electronic digital signal processing system in single-chip microcomputer form.

A microprocessor device is a central processing unit or CPU for a digital processor which is usually contained in a single semiconductor integrated circuit or "chip" fabricated by "MOS/LSI" technology, as shown in U.S. Pat. No. 3,757,306 issued to Gary W. Boone and assigned to Texas Instruments. The Boone patent shows a single-chip 8-bit CPU including a parallel ALU, registers for data and addresses, an instruction register and a control decoder, all interconnected using the Von Neuman architecture and employing a bidirectional parallel bus for data, address and instructions. U.S. Pat. No. 4,074,351, issued to Gary W. Boone and Michael J. Cochran, assigned to Texas Instruments, shows a single-chip "microcomputer" type device which contains a 4-bit parallel ALU and its control circuitry, with on-chip ROM for program storage and on-chip RAM for data storage, constructed in the Harvard architecture. The term microprocessor usually refers to a device employing external memory for program and data storage, while the term microcomputer refers to a device with on-chip ROM and RAM for program and data storage; the terms are also used interchangably, however, and are not intended as restrictive as to this invention.

Subsequent to 1971 when U.S. Pat. Nos. 3,757,306 and 4,074,351 were originally filed, many improvements have been made in microprocessors and microcomputers to increase the speed and capability of these devices and reduce the cost of manufacture, providing more circuitry and functions in less space, i.e., smaller chip size. Improved VLSI semiconductor processing and photolithographic techniques allow narrower line widths and higher resolution, providing added circuit density and higher speed, but circuit and system improvements also contribute to the goals of increased performance with smaller chip size. Some of these improvements in microcomputers are disclosed in the following U.S. Patents, all assigned to Texas Instruments: U.S. Pat. No. 3,991,305 issued to Edward R. Caudel and Joseph H. Raymond Jr.; U.S. Pat. No. 4,156,927 issued to David J. McElroy and Graham S. Tubbs; U.S. Pat. No. 3,934,233 issued to R. J. Fisher and G. D. Rogers; U.S. Pat. No. 3,921,142 issued to J. D. Bryant and G. A. Hartsell; U.S. Pat. No. 3,900,722 issued to M. J. Cochran and C. P. Grant; U.S. Pat. No. 3,932,846 issued to C. W. Brixely et al; U.S. Pat. No. 3,939,335 issued to G. L. Brantingham, L. H. Phillips and L. T. Novak; U.S. Pat. No. 4,125,901 issued to S. P. Hamilton, L. L. Miles, et al; U.S. Pat. No. 4,158,432 issued to M. G. VanBavel; U.S. Pat. No. 3,757,308 and U.S. Pat. No. 3,984,816. The devices described in these patents have been of the Harvard architecture and of the 4-bit type, particularly adapted for calculator or controller applications.

Additional examples of microprocessor and microcomputer devices in the evolutation of this technology are described in publications. In Electronics, Sept. 25, 1972, pp. 31–32, a 4-bit P-channel MOS microcomputer with on-chip ROM and RAM is shown which is similar to U.S. Pat. No. 3,991,305. Two of the most widely used 8-bit microprocessors like that of U.S. Pat. No. 3,757,306 are described in Electronics, Apr. 18, 1974 at pp. 88–95 (the Motorola 6800) and pp. 95–100 (the Intel 8080). A microcomputer version of the 6800 is described in Electronics, Feb. 2, 1978 at pp. 95–103. Likewise, a single-chip microcomputer version of the 8080 is shown in Electronics, Nov. 25, 1976 at pp. 99–105. Another single-chip microcomputer, the Mostek 3872, is shown in Electronics, May 11, 1978, at p. 105–110 and an improved version of the 6800 is disclosed in ELectronics, Sept. 17, 1979 at pp. 122–125. Sixteen-bit microprocessors based on minicomputer instruction sets evolved such as the part number TMS9900 described in a book entitled "9900 Family Systems Design", published in 1978 by Texas Instruments Incorporated, P.O. Box 1443, M/S 6404, Houston, Tex. 77001, Library of Congress Catalog No. 78-058005. The 8086, a 16-bit microprocessor evolving from the 8080, is described in Electronics, Feb. 16, 1978, pp. 99–104, while a 16-bit microprocessor identified as the 68000 (based on the 6800) is described in Electronic Design, Sept. 1, 1978 at pp. 100–107, and in IEEE Computer, Vol. 12. No. 2, pp. 43–52 (1979).

These prior 8-bit and 16-bit microprocessors and microcomputers have been general-purpose processors of the Von Neuman architecture with multiplexed address/data busses, and usually have been microcoded as described in U.S. patent application Ser. No. 209,915, filed Nov. 24, 1980 by Guttag, McDonough and Laws (now U.S. Pat. No. 4,402,043, or Ser. No. 253,624, filed Apr. 13, 1981, by Hayn, McDonough and Bellay, both assigned to Texas Instruments, and at pp. 28–34, IEEE Spectrum, March 1979, by McKevitt and Bayliss, or Proceedings 11th Annual Microprogramming Workshop, December, 1979 by Stintter and Tredenick. Microcoding, originally described by Wilkes in 1951, employs a control ROM to store microinstruction sequences entered by instruction words; the programmer works in a higher level machine code, so the number of assembly language code statements is supposedly reduced, and thus programming cost is reduced.

In contrast, a special-purpose high-speed microcomputer device according to the embodiment of the invention described herein departs from these contemporary microprocessor devices in several major respects in order to achieve substantial speed and performance advantages. This device is a non-microcoded processor of modified Harvard architecture.

It is the principal object of this invention to provide improved features of a microcomputer device and system, particularly one adapted for real-time digital signal processing. Another object is to provide a high-speed microcomputer of enhanced capabilities.

SUMMARY OF THE INVENTION

In accordance with one embodiment, features of the invention are included in a system for real-time digital signal processing employing a single-chip microcomputer device having separate on-chip program ROM and data RAM, with separate address and data paths for program and data. An external program address bus allows off-chip program fetch in an expansion mode, with the opcode returned by an external data bus. A bus interchange module allows transfer between the sepa-

rate internal program and data busses in special circumstances. The internal busses are 16-bit, while the ALU and accumulator are 32-bit. A multiplier circuit produces a single state 16×16 multiply function separate from the ALU, with 32-bit output to the ALU. One input to the ALU passes through a 0-to-15 bit shifter with sign extension.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as other features and advantages thereof, will be best understood by reference to the detailed description which follows, read in conjunction with the accompanying drawings, wherein;

FIG. **1** is an electrical diagram in block form of a microcomputer system employing features of the invention;

FIG. **2** is an electrical diagram in block form of an MOS/LSI microcomputer device (including a CPU or central processor unit) employed in the system of FIG. **1** and utilizing features of the invention;

FIGS. *3a–3mm* are timing diagrams showing voltage or event vs. time in the operation of the microcomputer of FIG. **2**;

FIGS. **4** and *4a* are greatly enlarged plan views of a semiconductor chip containing the microcomputer of FIG. **2**, showing the physical layout of the various parts of the device;

FIGS. *5a–5i* are electrical schematic diagram of particular circuits in the microcomputer device of FIG. **2**.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENT

Microprocessor System

The microcomputer device to be described herein is primarily used for signal processing, but concepts thereof may be used in processor devices of various configurations, and these devices may be used in many different systems; in one embodiment the microcomputer is used in a system shown in generalized form in FIG. **1**. The system may be, for example, a voice communication system, a speech analysis system, a small "personal" or "home" computer, a single-board general purpose microcomputer, a word processing system, a computer terminal having local processing capability with display and typewriter keyboard, or any one of many applications of various types. The system includes a single-chip MOS/LSI central processing unit or microcomputer **10** which will be described in detail, along with a program or data memory **11** and input/output or I/O devices **12**. Usually the I/O devices **12** for the typical system include analog-to-digital and/or digital-to-analog converters, a modem, a keyboard, a CRT display, a disc drive, etc. Often the I/O **12** includes coupling to a general purpose processor; that is the microcomputer **10** is an attached processor in a larger system with interface via the I/O **12**. The microcomputer **10**, program data memory **11** and I/O **12** communicate with one another by two multibit, parallel address and data busses, D and RA, along with a control bus **13**. The microcomputer **10** has suitable supply voltage and crystal-input terminals; for example, the device employs a single +5 V Vcc supply and ground or Vss, and a crystal is connected to terminals X1 and X2 of the device **10** to control certain system timing. The microcomputer **10** is a very high speed device with a crystal input of 20 MHZ, providing an instruction execution rate of five million per second, in one embodiment.

The microcomputer device **10** is a general purpose microcomputer specifically aimed at serving a large class of serial signal processing problems such as digital filtering, signal handling for telecommunications modems (modulation, demodulation), data compression for linear predictive code (LPC) speech signals, fast Fourier transforms, and in general for virtually all computation intensive analog system functions, including detection, signal generation, mixing, phase tracking, angle measurement, feedback control, clock recovery, correlation, convolution, etc. It is suitable for applications which have computational requirements similar to those for control and signal processing, such as coordinate transformation, solution of linear differential equations with constant coefficients, averaging, etc. The device **10** is usually interfaced via I/O **12** to a general purpose processor such as a 99000, an 8600 or a 68000, to construct processing systems as will be explained.

It is understood that, even though described in the context of a microcomputer in the preferred embodiment, with an on-chip program ROM **14** and data RAM **15**, nevertheless, some concepts of the invention may be used in a single-chip microprocessor with all off-chip program memory and/or data memory instead of the on-chip memory illustrated. Indeed, modes of operation are provided which disable the on-chip memory. Also, a microcomputer is shown having two separate external program address and data busses instead of the multiplexed, bidirectional busses which are now common, but some features herein disclosed are applicable where busses are multiplexed. The advantage of separating the busses and separating program and data memory space is speed.

In general terms, the system of FIG. **1** functions in the following manner: the microcomputer **10** fetches an instruction word internally by accessing the ROM **14** or externally by sending out an address on the ROM address bus RA to the memory **11** (and RCLK-on control bus **13**). If external, the instruction word is received back via the data bus D from the addressed location in the memory **11**. This instruction is executed in the next machine cycle (of length of 200 ns defined by a 20 MHz clock or crystal X1, X2) while a new instruction is being fetched; execution of an instruction may include accessing the on-chip RAM **15** for an operand, or writing a result into data RAM **15**, and an arithmetic or logic operation in ALU.

In the example to be described in detail, a 12-bit instruction address applied internally to ROM **14** or externally to the RA bus directly addresses 2^{12} or 4K words of program instruction or constants in ROM **14** and memory **11**. When reading from memory **11**, a DEN– (data bus enable bar) command is asserted on control bus **13**. It is also possible to write into the memory **11**, and for this purpose a WE– (write enable bar) command is asserted by the device **10** on one of the control bus lines **13**; the memory **11** may contain read/write memory devices in some or all of the address space, so the WE– command permits a write function.

The I/O devices **12** are addressed as ports; this interface to external devices **12** is accomplished using the address and data busses RA and D and control bus **13**, but the I/O devices **12** do not occupy locations in the logical address space like the memory **11**. This is in contrast to conventional memory-mapped I/O.

Data input/output via I/O or peripherals **12** employs a 3-bit field from the bus RA to select one of eight 16-bit ports in peripheral circuitry **12**. The selected 16-bit port is then accessed for read or write via the bus D. This operation uses one of the two instructions IN or OUT, on the control bus **13**, WE− is active for write or OUT, or DEN− is active for read or IN. A ROM clock RCLK− is active on control bus **13** on every machine cycle except when either DEN− or WE− is active; that is, the memory **11** is activated by RCLK− for possible instruction word access from off-chip in each machine cycle, but if accessing peripheral **12** using DEN− or WE− then the RCLK− does not occur.

A reset signal RS− on the control bus **13** clears the program counter and address bus RA (resets to zero), sets the data bus D in a high impedance state, and the memory controls DEN−, WE− and RCLK− in an inactive (high) state. All address and temporary data registers within the microcomputer **10** are cleared by a reset routine in the ROM **14**, but the internal RAM is not cleared. In this manner, the peripheral circuitry **12** (such as a main processor) can assert control, or initiate a start-up or power-on sequence.

An interrupt signal INT− on the control bus **13** causes the microcomputer **10** to halt execution (saving the current ROM address) and go to an interrupt vector address, unless interrupts are masked by the program.

The ME/SE− line in the control bus **13** defines the memory expansion mode or systems emulator mode for the microcomputer **10**. When this pin is held high (at +Vcc), the microcomputer executes from on-chip ROM and off-chip memory **11**, but when low (Vss) the chip is in the systems emulator mode and execution is only from the memory **11** which is PROM, EPROM or RAM so the program can be easily changed.

The Microcomputer Chip

The internal architecture of the microcomputer **10** is shown in a detailed block diagram in FIG. **2**. This device is a single-chip semiconductor integrated circuit mounted in a standard dual-in-line package or a chip carrier. Sixteen pins or terminals of the package are needed for the 16-bit data bus D, twelve to sixteen are used for the address bus RA (depending upon memory size) and the remaining terminals are used for the power supply Vcc and Vss, the crystal X1, X2, and the control bus **13**.

In addition to the program and data memory **14** and **15**, the microcomputer **10** contains a central processing unit or CPU for the system of FIG. **1**, and this CPU includes a 32-bit arithmetic logic unit or ALU, a 32-bit accumulator Acc to hold operands and results, multiplier M separate from the ALU, a shifter S which is one input to the ALU, status or flag decode SD, and an instruction decoder ID1 which receives part of the current instruction word and generates the control bits for the CPU and data memory portions of the device **10**.

The program memory **14** has associated with it a program counter PC to hold the instruction address used to access the ROM **14** or sent out on bus RA to the memory **11**, an instruction register IR to receive the instruction word from ROM **14**, a stack ST to save program memory addresses, and an instruction decoder ID2 which receives part of the current instruction word and generates control bits for the program memory portion of the microcomputer.

Associated with the data memory **15** are two auxiliary address registers AR0 and AR1 for the data memory **15**, a page register ARP to select between the registers AR0 and AR1 as the data memory address, and a data page buffer DP to hold certain bits of the data memory address.

The CPU is oriented around two internal busses, a 12-bit program bus (P-Bus) and a 16-bit data bus (D-Bus). Program access and data access can thus occur simultaneously, and the address spaces are separate. A bus interchange module BIM permits loading the program counter PC from Acc, for example, or accessing ROM **14** for constants via P-Bus, BIM and D-Bus.

The two major requirements for a signal processing microcomputer are high speed arithmetic and flexibility. Performance is achieved by using separate, principally on-chip program and data memories **14** and **15**, a large single accumulator Acc and a parallel multiplier M. A special purpose operation, data move, is defined within the data memory **15** which further enhances the performance in convolution operations. Flexibility has been achieved by defining an instruction set as will be described with reference to Table A, incorporating memory expansion and a single lever of interrupt.

The device can be configured with, for example, less than 2K or 2^{11} words of on-chip program memory **14** and the architecture allows for memory expansion up to 4K or 2^{12} words by the addition of external program memory in the memory **11**. In addition, a separate mode allows the device **10** to be configured as a system emulation device; in this "system emulator" mode, the entire 4K memory space is external and the ROM **14** is not used.

The CPU

The arithmetic logic unit or ALU consists of thirty-two parallel stages, each separate stage performing an arithmetic or logic function on its two input bits and producing a one-bit output and carry/borrow. The ALU has two 32-bit data inputs ALU-a and ALU-b, and a 32-bit data output ALU-o to accumulator Acc. The ALU-a input is always from the accumulator Acc and the ALU-b input is always either from the shifter S or from a 32-bit product register P in the multiplier M. The particular function performed on data passing through the ALU is defined by the current instruction word in IR which is applied by the program bus P-Bus to an instruction decoder ID1. The source of the ALU-b input is defined by an input select circuit ALU-s which selects from these two alternatives, based upon the contents of the current instruction word, i.e., the outputs #C of the decoder ID1. The shifter S receives a 16-bit input Si from D-Bus and produces a 32-bit output So which is the input Si shifted from zero to fifteen places to the left. Left-shifted data is zero-filled, i.e., all right-hand bit positions are filled with zeros when data is shifted out to the left. A unique feature is that the high-order bit is sign extended during shift operations. The ALU operates in twos-complement. The shifter S includes a shift control Sc loaded with a four-bit value from P-Bus via lines Sp so an arithmetic instruction can directly define the number of bits shifted in the path from D-Bus to the ALU-b input.

In this description, the LSB is considered to be on the right and the MSB on the left, so left-shift is toward more significant bits. Bit-0 is the MSB and bit-15 is the LSB. Data is always in signed 2's complement in this architecture.

The multiplier M is a 16×16 multiplier using carry feed-forward, constructed in partly dynamic and partly

static logic, to implement Booth's algorithm. One input to the multiplier M is the T register which is a 16-bit register for temporary storage of the multiplicand received from D-Bus via lines Ti. The other 16-bit input is via lines Mi from the D-Bus; this multiplier input may be from the data memory **15** or may be a 13-bit multiply-immediate value derived directly from the instruction word (loaded right-justified and sign-extended).

The ALU always receives the contents of the accumulator Acc as its ALU-a input, and always stores its output in Acc, i.e., Acc is always the destination and the primary operand. The unit will add, subtract and perform the logic operations of And, Or and Exclusive Or. The logic operation results are between the lower half of Acc (bits **16–31**) and a 16-bit value from the data memory **15**. Due to passing the data memory value through the shifter S (with zero shift), the operand for the logical operation result of the MSBs (bits **0–15**) is zero. The final 32-bit result reaching the accumulator is thus in two parts: Bits **0–15** will be Acc bits **0–15** Anded (or Or'ed, etc) with zero; bits **16–31** of the result will be Acc bits **16–31** Anded (etc.) with the data memory value. The accumulator Acc output, in addition to the 32-bit ALU-a input, includes high and low 16-bit outputs Acc-H (bits **0–15**) and Acc-L (bits **16–31**); separate instructions "store accumulator high" SACH and SACL "store accumulator low" are provided for storing high and low-order Acc bits in the data memory **15**.

The status decoder SD monitors the Acc whenever an instruction which updates Acc is executed. Four bits of SD are OV, L, G and Z. Accumulator overflow (or underflow) is indicated by the OV bit, Acc contents less than zero is indicated by the L bit, Acc greater than zero indicated by the G bit, and Acc equal zero indicated by the Z bit. Upon interrupt the OV bit is saved in an overflow flag register, but the other bits are available only up to the time the next accumulator instruction is executed.

The accumulator overflow mode is a single-bit mode register OVM (included in SD), directly under program control, to allow for saturated results in signal processing computations. When the overflow mode OVM is reset, overflow results are loaded via ALU-o into the accumulator Acc from the ALU without modification. When the overflow mode is set, overflow results are set to the largest, or smallest, representable value of the ALU and loaded into the accumulator Acc. The largest or smallest value is determined by the sign of the overflow bit. This allows a saturated Acc result in signal processing applications, modeling the saturation process of analog signals.

A separate status bit in SD monitors the condition of the currently used auxiliary register AR0 or AR1 and detects the all-zero condition of the least significant nine bits of the current auxiliary register (i.e. loop counter portion). This bit is used for a branch instruction conditioned on non-zero for the auxiliary register (BARNZ), "branch on auxiliary register non-zero."

The input/output status bit (I/O ST−) is an external pin which is part of the control bus **13** and provides "branch on I/O zero" instruction (BIOZ) to interrogate the condition of peripheral circuits **12**. A zero level on the I/O ST− pin will cause a branch when sampled by the BIOZ instruction.

The bus interchange module BIM exchanges the low-order twelve bits of the 16-bit value on the D-Bus with the twelve bits on the P-Bus. This operation is not available to the programmer as an instruction, but instead is needed as an inherent operation in instructions such as table look up (TBLR A).

PROGRAM MEMORY ADDRESSING

The program memory **14** is a ROM which is partitioned to produce a 16-bit output to instruction register IR, and this ROM employs a decoder **14***a* which selects one 16-bit instruction word based on an 11-bit or 12-bit address on input lines **14***b*. In the example embodiment, the ROM **14** contains less than 2K words, so an 11-bit address can be used, but the on-chip program memory could be expanded to 4K with a 12-bit address. The circuit of the ROM **14** is especially adapted for fast access as will be explained. The address input **14***b* is received from the program counter PC which is a 12-bit register containing the address of the instruction following the one being executed. That is, at the time when the control bits #C are valid at the outputs of the instruction decoders ID1 and ID2 for one instruction, PC contains the address of the next instruction; an address in PC goes into decoder **14***a* and the next instruction is read from ROM **14** into IR, and the program counter PC is incremented via PCinc in preparation for another instruction fetch. That is, PC is self incrementing under control of a #C control bit from ID2. The output PCo from the program counter PC is also applied via lines RApc and selector RAs (and output buffers not shown) to the external RA bus via output lines RAo and twelve output pins of the microcomputer device. The RA bus (RA0 through RA11) contains the PC output via RApc when the selector RAs is in one mode, or contains the input RAi when executing I/O instructions IN and OUT. Whenever the address in PC is above the highest address in ROM **14**, off-chip program addressing to memory **11** is assumed; however, the device is designed to operate principally with the on-chip ROM, so for many uses of the device off-chip fetches for program instructions would never be needed. The program counter PC may be loaded via input PCi and selector PCs from the P-Bus for branch or call instructions, or loaded from the accumulator Acc via Acc-L, D-Bus, BIM, P-Bus, PCp and PCi in a "call accumulator" CALLA instruction.

The register stack ST is used for saving the contents of PC during subroutine and interrupt calls. In the illustrated embodiment, the stack ST contains four 12-bit registers constructed as a first-in, last-out push-down stack, although a larger or smaller number of registers could be used. The current contents of PC are saved by "pushing" onto the top-of-stack register TOS via lines PCst. Succesive CALL instructions will keep pushing the current contents of PC onto TOS as the prior contents are shifted down, so up to four nested subroutines can be accomodated A subroutine is terminated by execution of a return instruction RET which "pops" the stack, returning the contents of TOS to PC via lines PCt, selector PCs and input PCi, allowing the program to continue from the point it had reached prior to the last call or interrupt. When TOS is popped, the addresses in lower registers of ST move up one position. Each subroutine, initiated by a call instruction or an interrupt, must be terminated by a RET instruction.

In an example embodiment, the ROM **14** contains 1536 words, so the remainder of the 4K program address space, 2560 words, is off-chip in the memory **11**. When the memory expansion control pin ME/SE− is high, at logic 1, the device interprets any program address in PC in the 0-to-1535 range as being an on-chip

address for the ROM **14**, and any address in the 1536–4095 range as being an off-chip address so that the PC contents are sent out via RApc and RAo to the RA bus. An output strobe RCLK— generated by the decoder ID2 for every machine state enables the external memory **11** (except when IN or OUT instructions are being executed). When off-chip program memory **11** is accessed, the instruction word read from memory **11** is applied to the external bus D and thus to the internal P-Bus via input/output control DC and lines Dp; this is a 16-bit instruction and, like the output of ROM **14** via IR, it is loaded into decoders ID1 and ID2 for execution, or loaded into PC via PCp, or otherwise used just as an on-chip instruction fetch.

When the ME/SE— pin is at zero the device enters the system emulator mode wherein the entire 4K program address space is off-chip, so all PC addresses are applied to the RA bus via RApc and RAo. This mode is necessary when a user is developing systems or programs, prior to arriving at a final version of code for the ROM **14**. That is, the microcomputer **10** can operate with no code permanently programmed into the ROM so that new programs (stored in RAM or EPROM in the memory **11**) can be tested and debugged, then when the final code is extablished the chips **10** are produced in large volume with this code mask-programmed into the ROM **14**.

In either mode, the first two program addresses 0000 and 0001 are used for the reset function. When the reset pin RS— is brought low, an address of all zeros is forced into the program counter PC, as will be explained. Also, the third address is reserved for an interrupt vector; when the INT— pin is brought low, an address of 0002 is forced into PC to begin an interrupt routine.

DATA MEMORY ADDRESSING

The data memory **15** in the example embodiment contains 144 16-bit words, and so an 8-bit address is needed on address input **15***a* to the RAM address decoder **15***b*. However, the RAM **15** may be constructed with up to 512 words, requiring a 9-bit address, so the addressing arrangement will be described in terms of address bits which are unused in some embodiments. Each 128 word block of the RAM **15** is considered to be a page, so a 7-bit address field in an instruction word from program memory **14** on P-Bus via input **15***c* is used to directly address up to 128 words of data memory **15**. Two auxiliary registers AR0 and AR1 are employed in the example embodiment; however, up to eight of these 16-bit registers may be used, with the particular one currently being used as the source of the address for the RAM **15** being defined by the auxiliary register pointer ARP. With two registers AR0 and AR1, the pointer ARP is only one bit, but for an embodiment with eight auxiliary registers the pointer ARP is a 3-bit register. The 16-bit auxiliary registers AR0 and AR1 are under control of store, load or modify auxiliary register instructions SAR, LAR, and MAR as will be described. Nine-bit addresses from the low-order parts of the auxiliary registers may be applied to the address input **15***a* via selector **15***d*, , lines **15***e*, selector **15***f*, and lines **15***g*. When one of the auxiliary registers is to be the source of the RAM address, the selector **15***d* uses the value on lines **15***e* as the address input **15***a*, whereas if the P-Bus is to be the source of the RAM address the selector **15***d* uses a 7-bit address from input **15***c* and a 1-bit (expandable to 3-bit or 4-bit) page address from the data page register DP. The selector **15***f* is controlled by the pointer ARP which is loaded from P-Bus as defined by an instruction. The auxiliary registers are used for indirect addressing wherein an instruction need not contain a complete address for RAM **15** but instead merely specifies that an auxiliary register is to be used for this address; such instructions can also specify increment or decrement for the auxiliary register selected, in which case the nine LSBs of AR0 or AR1 are changed by +1 or −1 via paths Inc. The auxiliary registers may be thus used as loop counters. The auxiliary registers are accessed by the D-Bus vis lines ARio so these registers may be used as miscellaneous working registers, or may be initially loaded to begin a loop count.

The data memory **15** is accessed via the D-Bus and an input/output circuit **15***i*, via lines **15***j*. Construction of the data memory is such that a data move wholly within the RAM **15** is permitted, according to an important feature of the microcomputer **10**. Under instruction control, the data at one address can be moved to the next higher location in one machine cycle without using the ALU or D-Bus. Thus during an add, for example, the accessed data can be also moved to the next higher address. INPUT/OUTPUT FUNCTIONS

Input and output of data from the microcomputer chip **10** uses the data bus D and two of the lines of the control bus **13**, these being data enable bar (DE—) and write enable bar (WE—). Two instructions, IN and OUT, are employed for the data input and output functions. The external data bus D is coupled to the internal data bus D-Bus by the input/output control and data buffers DC. The output buffers in D1 are tri-state, so the output to data bus D is always placed in a high impedence state except when IN or OUT is being executed; to this end, one of the controls #C from the instruction decode ID1 sets the output buffers in high impdence state whenever IN or OUT is not decoded. When the instruction IN is present, the control DC activates sixteen input buffers, so the external data bus D is coupled to the internal D-Bus via DC and lines Dd for data input. When the OUT instruction is decoded, a control #C from ID1 activates output buffers in DC so the internal D-Bus is coupled via Dd and DC to the external bus D.

Execution of an IN instruction will also generate a data enable DEN— strobe on line **13***a* from ID1, and will couple the D-Bus to the RAM **15** via **15***i* and **15***j*, so the data from external will be entered into on-chip data memory. The intended uses of the microcomputer as a signal processor require hundreds or thousands of accesses to RAM **15** for every off-chip reference. That is, a value will be fetched from off-chip then convolution or like operations performed using this new value and other data in the RAM **15**, so thousands of instruction executions will transpire before another off-chip reference is needed. For this reason, the architecture favors internal data manipulation over off-chip data access.

Execution of an OUT instruction causes generation of an off-chip write enable WE— strobe on line **13***b* from ID1 and outputs data from RAM **15** via **15***i* and **15***j*, D-Bus, lines Dd and buffer DC to the external bus D. Referring to FIG. **1**, this data may be written into one of the ports (selected by the 3-bit RAi value) in the peripherals **12**.

Implicit in both the IN and OUT instructions is a 3-bit port address on lines RAi from ID1. This address is multiplexed onto the three LSBs (RA9–RA11) of the external address bus RA via selector RAs. Up to eight

peripherals may thus be addressed. The remaining high order bits of the RA bus outputs are held at logic zero during these instructions.

THE INSTRUCTION SET

The microcomputer **10** of FIGS. **1** and **2** executes the instruction set of Table A. The Table shows in the first column in mneumonic or assembly language name of each instruction used in writing source code, followed in the second column by the object code in binary which is the form the code appears in the ROM **14** and in the instruction register IR. This binary code is decoded in ID1 and ID2 to generate all of the controls #C to execute the desired operation by accessing various busses and registers and setting the functions of the ALU. The Table also gives the number of cycles or machine states employed by the microcomputer in executing the instruction; note that all instructions except branches, calls, table look-up and input/output are executed in one state time. The microcomputer is not microcoded; the standard ALU instructions are executed in one state. The Table also shows the number of instruction words needed to execute each instruction; it is important to note that only branches and call direct require two instruction words. The right-hand column is a brief description of the operation for each instruction.

Most of the instructions of Table A show the low-order eight bits (bits **8–15**) as "IAAAAAAA", which is the direct or indirect RAM **15** address for one operand. If the "I" bit, bit-**8**, is 0, the direct addressing mode is used, so the "A" field of the instruction word, bits **9–15**, is employed as a direct address connected from IR through P-Bus, lines **15***c* and selector **15***d* to address input **15***a*. In this direct addressing mode, the auxiliary registers AR0–AR1 are not used.

For the instructions containing "IAAAAAA", the indirect addressing mode is specified by a 1 in the I field, bit-**8**, of these instructions. The input address on lines **15***a* for the RAM **15** will in this case be obtained from one of the auxiliary registers AR0 or AR1, and bit **15** will select which one. If bit-**15** is 0, AR0 is used; if bit-**15** is 1, AR1 is used. Thus bit-**15** coupled from IR via P-Bus controls the selector **15***f* (and can be loaded into the ARP register). Since the number of auxiliary registers is expandable to eight, bits **13–15** of these indirect-address instructions are reserved for use with a 3-bit selector **15***f* and ARP register to define one-of-eight in the indirect addressing mode. Bit-**10** to bit-**12** are controls in indirect addressing: bit-**10** causes the addressed auxiliary register to be incremented if 1, or no change if 0; bit-**11** causes the addressed AR to be decremented if 1 or no change if 0; bit-**12** if 0 causes bit-**15** to be loaded into ARP after execution of the current instruction, or if 1 leaves the ARP unchanged.

The shift code SSSS used in many instructions of Table A is a four-bit field loaded into shift control Sc via Sp to define the number of spaces (zero to fifteen) that the data coming from the RAM **15** via D-bus is left shifted as it passes through the shifter S on the way to the ALU-b input.

Although not material to the structure described herein, assembly language formats using the instruction set of Table A employ "A" to designate direct addressing and "@" to designate indirect. Thus, "ADD S,A" means add contents of memory location defined by the A field of the instruction word. "ADD A@" means add using contents of the data memory location addressed by the auxiliary register AR0 or AR1 selected by the existing contents of ARP. ADD S@+ means add using current contents of ARP to define AR then increment this auxiliary register for loop counting. ADD S@ is the same as previous except decrement by 1. ADD S@,AR is same as previous except ARP is loaded with the value of bit-**15** to define a new auxiliary register for subsequent operations.

The descriptions given in the right-hand column of Table A assume direct addressing. For indirect addressing, the above explanation applies.

The ADD instruction thus adds the 16-bit contents of RAM **15** (at location OAAAAAAA for direct, or the contents at the locations in RAM **15** selected by the chosen AR if indirect), shifted SSSS spaces left, to the 32-bit contents of the Acc, and stores the result in the Acc. ADDH does the same except only the high-order half of Acc is the source of one operand and destination of the result, and no shift is performed.

The subtract instructions SUB and SUBH subtract the addressed RAM **15** data from the accumulator and store the result in Acc, but are otherwise the same as add. The load instruction LAC loads Acc with the 16-bit data addressed by IAAAAAAA which is left-shifted by SSSS bits. Only ADD, SUB and LAC specify a shift.

There are four instructions associated with the auxiliary registers: SAR, LAR, LARK and MAR. Store auxiliary register SAR causes the contents of one of the auxiliary registers defined by RRR to be stored in the memory location IAAAAAAA; the load AR instruction LAR is the reverse of SAR. With the LARK instruction a constant K from IR (bits **8–15**) is loaded into the AR defined by RRR; this 8-bit constant K is right-justified and MSBs set to zero in the 16-bit auxiliary register. The modify auxiliary instruction MAR causes one auxiliary register to be modified by bits-**10** to **12** as above, but no add or memory **15** access is implemented. The MAR code is operative only in the indirect mode, I=1; in direct mode this instruction results in no-op.

The input/output instructions are written in assembly language as "IN PA, A" or "OUT PA, A", where PA is the 3-bit port address PPP output on bits **9–11** of the RA bus (generated from the decoder ID1 and coupled via lines RAi). IN enables DEN− and disables RCLK−, while OUT enables WE− and disables RCLK−. The peripheral devices **12** decode RA9–RA11 to select one of eight 16-bit ports or locations for read or write via the bus D. These instructions use two machine states so that the data input pins of bus D are free on the second state to allow external fetch of the next instruction from memory **11** instead of ROM **14**.

The store accumulator instructions SACL and SACH, written as "SACL X,A" in assembly, cause the low or high order bits of Acc to be left-shifted XXX places and stored in the data memory **15** at the location defined direct or indirect by IAAAAAAA. The X field is not fully implemented in the example embodiment; for SACL only X=0 is allowed and for SACH only X=0, X=1 and X=4 are allowed. This shift is implemented in the accumulator circuitry itself rather than in the shifter S.

The arithmetic and logic instructions without shift code are ADDH, ADDS, SUBH, SUBS, SUBC, ZALH, ZALS, EXOR, AND, OR and LACK. These are all written as ADDH A, for example, in assembly language. ADDH causes the 16-bit data from the defined location in RAM **15** to be added to the high-order

half of Acc and stored in the high-order half of Acc; actually the data from RAM **15** is left shifted sixteen bits in shifter S as it goes from D-Bus to the ALU-b input. The ADDS instruction means that the sign extension is suppressed in the shifter S; the data from RAM **15** defined by A is treated as a 16-bit positive number instead of a signed 2's complement integer. SUBH and SUBS correspond to ADDH and ADDS except subtract is performed in the ALU.

The conditional subtract instruction SUBC is used in divide operations. The contents of the defined location in RAM **15** are subtracted from the contents of Acc and left-shifted fifteen bits, producing an ALU output ALU-o which, if equal to zero is left-shifted by one bit and a +1 is added, with the result stored in Acc. If the ALU output is not equal to zero then it is left-shifted by one-bit and stored in Acc (the +1 is not added). SUBC is a two-cycle instruction that assumes the accumulator is not used in the following instruction. If the following operation involves Acc then a NO OP instruction should be inserted after SUBC.

The "xero accumulator load high" instruction ZALH fetches the 16-bit word at the addressed location in the RAM and loads it into the high-order half of Acc (bits **0–15**); the Acc has been zeroed, so the low-order bits **16–31** reamin zero. The shifter S is in the data path from D-Bus via ALU to Acc, so a 16-bit shift is performed in ZALH to move the data to the high-order half. The ZALS instruction fetches a word from RAM and loads it into the low-order half of the zeroed Acc, with sign extension suppressed in the shifter S.

The logic operations EXOR, AND and OR are performed in 32-bit format, even though the operand fetched is sixteen bits. For EXOR, the high-order half of Acc is Exclusive Or'ed with zeros, concatenated with Exclusive Or of the fetched data with the low-order half of Acc, both halves of the result being stored in Acc. The same applies to OR and AND.

The load accumulator instruction LACK causes an 8-bit constant contained in the eight LSB's of the instruction word to be loaded into the eight LSB's of Acc, right justified; the upper twenty-four bits of Acc are zeroed. To accomplish this operation, the instruction word on P-Bus from IR (after ID1 and ID2 are loaded, of course), is coupled to the D-Bus by BIM, and thence to the ALU-b via shifter S (with no shift). The ALU performs "pass ALU-b" or add zeros to b, leaving the constant in Acc.

The data shift or data move instruction DSHT causes the contents of the defined location in the RAM **15** to be moved to the defined location plus one. This is accomplished internal to the RAM **15** without using the ALU or data bus D-Bus. The operation cannot cross a page boundry, however.

The "load T" instructions are used to set up multiply operations. LT causes the T register to be loaded from RAM **15** with the value defined by IAAAAAAA. The "load T with data move" instruction LTD employs an operation like DSHT in the RAM; the T register is loaded with the contents of the RAM **15** location defined by IAAAAAAA, then this same value is shifted to location IAAAAAAA+1, and also the contents of Acc is added in ALU to the contents of the P register with the result going to Acc. The LTA instruction is the same as LTD but without data move; the T register is loaded from RAM **15** and the P register is added to Acc, with result to Acc.

The multiply instruction MPY causes the 16-bit contents of T register to be multiplied in multiplier M (not using ALU) by the value from RAM **15** on the input Mi from D-Bus, with the 32-bit result going to the P register. The "multiply constant" instruction MPYK causes the 16-bit contents of T register to be multiplied by a 13-bit constant C from the opcode in IR; the 32-bit result stays in P register. For MPYK, the constant is connected from IR to Mi via P-Bus, BIM and D-Bus.

The "load data page" instructions LDPK and LDP cause the data page register DP to be loaded with up to eight bits from the opcode itself or from the defined location in RAM **15**. In the embodiment shown, the DP register is only one bit, but in other embodiments with a larger RAM **15** the DP register contains up to eight bits. The page address remains the same until a new load page instruction occurs.

The load status and store status instructions LST and SST are used in call subroutine or interrupts to save the contents of the status circuits SD, or restore status SD. These instructions are used instead of hard wired circuits for performing this function.

The disable and enable interrupt instructions DINT and EINT are used to mask or unmask the interrupt capability, i.e., these instructions reset or set a latch which determines whether or not the microcomputer **10** responds to the INT− pin.

An absolute value instruction ABS functions to assure that the accumulator contains only an absolute valve, i.e., if Acc is less than zero, the absolute value of Acc is loaded into Acc, but if Acc is greater than zero there is no change. Similarly, the zero accumulator instruction ZAC clears Acc.

The overflow mode instructions RAMV and SAMV cause the overflow mode latch OVM in the status decode SD to be set to 1 or reset to 0. When set, the ALU output is set to its maximum or minimum before loading into Acc upon overflow. This simulates the effect of saturating an amplifier in an analog circuit, and is useful in signal processing.

Three P register instructions PAC, HPAC and SPAC are used in manipulating data after a multiply MPY or MPYK. PAC loads the accumulator with the contents of the P register by passing the 32-bit data through the ALU without performing any operation to modify the data; actually the ALU-a input is zeroed and an ADD is executed. The APAC instruction adds the contents of the P register to the contents of Acc, with the result going to Acc. Similarly, the SPAC subtracts the contents of P register from Acc, result to Acc.

The subroutine instructions are CALL, CALLA and RET. CALL is a two-word instruction; the first word is the opcode and the second is the absolute address of the first instruction in the subroutine. When CALL is decoded in ID2, PC is incremented to fetch the next instruction word which is the address, then the incremented contents of PC are pushed to stack ST. The subroutine ends in return RET which causes the address on TOS to be popped and loaded into PC. To save status, SST must be used before CALL, and LST inserted after RET. The CALLA instruction is unique for a Harvard architecture machine; this uses the contents of Acc as the subroutine address rather than using the next location addressed by PC+1. The low-order bits of Acc are transferred via Acc-L and BIM to the P-Bus and thus via PCp to the program counter PC. The incremented PC is saved in CALLA by pushing to ST just as in a CALL.

The table look up instructions TBLR and TBLW also employ the Acc as an address source. These instructions require three states to execute. The RAM **15** location defined by IAAAAAAA is transferred via D-Bus and BIM to P-Bus, and thus via PCp to PC, from whence this address is applied via RApc to the external RA bus, or to ROM **14**.

The branch instructions all require two words, the first being the opcode and the second at PC+1 being the address. The low-order bits **8–15** of the opcodes are unused. Unconditional branch B loads the word at PC+1 into PC as the next address. BARNZ is conditional upon whether or not a loop counter, one of the auxiliary registers defined by ARP, is not-zero. BV causes a branch if the overflow bit OV in the status decode SD is a 1. BIOZ causes a branch if the IO bit from I/O ST– is a 1 in the status decoder SD. The six instructions BLZ, BLEZ, BGZ, BGEZ, BNZ and BZ are all dependent upon the defined condition in SD reflecting the condition in Acc.

SYSTEM TIMING

Referring to FIGS. *3a–3ii*, the timing of the system of FIG. **1** and the CPU chip of FIG. **2** is illustrated in a sequence of voltage vs. time waveforms or event vs. time diagrams. The chip **10** includes a clock generator **17** which has two external pins X1 and X2 to which a crystal (or external generator) is connected. The basic crystal frequency is up to 20 MHz and is represented by a clock **0** of FIG. *3a*. This clock **0** has a period of 50 ns, minimum, and is used to generate four quarter-cycle clocks Q1, Q2, Q3 and Q4 seen in FIGS. *3b–3e*, providing the basic internal timing for the microcomputer chip **10**. A set of four quarter cycle clocks Q1 to Q4 defines one machine state time of 200 ns, minimum; the states are referred to as S0, S1, S2, in FIG. **3**. The clock generator **17** produces an output CLKOUT, FIG. *3f*, on one of the control bus lines **13**. CLKOUT has the same period as Q1, but 50% duty cycle and beginning at the midpoint of Q1. This output is used for timing or synchronizing external elements of the system of FIG. **1**.

Internally, the microcomputer **10** executes one instruction per state time for most types of instructions, so five million instructions per second are executed. Of course, some instructions such as input/output, branch, call or table look-up require two or three state times. Assuming a sequence of single-state instructions such as add, load, store, etc., a new address is loaded into PC during each Q3 as seen in FIG. *3g*, then the ROM **14** is addressed during Q4 and Q1 so an instruction word output is produced from IR onto P-Bus starting in the next Q2 and continuing through Q3, as seen in FIG. *3h*. The ROM **14** access time is thus about 100 ns. If an external instruction fetch from memory **11** is used, the same access time applies. The instruction decoders ID1 and ID2 receive the instruction word from P-Bus during Q3 as seen in FIG. *3i*, and most of the decoder outputs #C are valid during Q1, although some fast controls are available in Q4. For direct addressing of the RAM, the address on bit-**9** to bit-**15** of P-Bus is immediately gated into the RAM decoder **15***b* when P-Bus becomes valid, but in either direct or indirect the RAM address is valid by the beginning of Q3 as seen in FIG. *3j*. For RAM read, the data output via **15***j* to D-Bus is valid on Q4, FIG. *3j*, and this data passes through the shifter S, FIG. *3k*, and is available as an ALU input during Q1, FIG. *3l*. The ALU controls #C are valid in Q2 and ALU output ALU-o is available during Q3. The accumulator Acc is loaded from ALU in Q4, FIG. *3m*.

It is thus seen that an ADD instruction, for example, for which fetch began at Q3 of the S0 state in FIGS. *3a–3m*, will be completed, i.e., the result loaded into Acc, in Q4 of state S2. There is substantial overlap of instruction execution. A new instruction fetch begins during Q3 of each state time, so execution of two more instructions have begun before one is finished.

Not shown in FIGS. *3a–3m* is the write-RAM function. The RAM **15** is always written into during Q2. Addressing the RAM is always during Q3, however. Thus, an instruction such as "store accumulator low" SACL is illustrated in FIGS. *3n* and *3o*. The RAM address is received from the instruction register via P-Bus on Q3 of S1 (assuming the SACL instruction was fetched beginning at Q3 of S0), and the write will not occur until Q2 of state S2. During the read slot, Q4 of S1, a refresh occurs for the addressed row of the RAM, then the same address stays until Q2 of state S2 for the write. The D-Bus is loaded from Acc during this same Q2, see FIG. *3n*.

If the accumulator must perform the saturate function in the overflow mode, i.e., OVM set to **1**, this will be performed after the load accumulator function of FIGS. *3m*. That is, for the ADD instruction of FIGS. *3a–3m*, the Acc is saturated during Q1 if the next state S3, so that when the accumulator is accessed by the following instruction it will be available to load the D-Bus on Q2.

When an instruction uses the data move function within the RAM **15**, the move operation occurs during Q1 as illustrated in FIG. *3o*. Also, if the increment loop counter function is performed for the auxiliary registers AR0 or AR1, the increment (or decrement) is executed in Q1. The T register, auxiliary registers AR0 or AR1, ARP latch, DP register and stack ST registers are each loaded during Q2 of any state time if these functions are included in the current instruction.

The bus interchange module BIM always executes a transfer from D-Bus to P-Bus beginning in Q2, if this function is defined by the instruction. The transfer from P-Bus to D-Bus by BIM is begun during Q4. The D-Bus is precharged on Q3 of every cycle, so no data can carry over on D-Bus through Q3 of any state, nor can data be loaded to or from D-Bus during Q3.

The program counter PC is incremented by the PCinc path during Q3 of each state time. That is, the load PC function of FIG. *3g* is the incremented value just generated.

Execution of a branch instruction is illustrated in FIGS. *3p–3r*. If the instruction loaded into the decoders ID1 and ID2 during Q3 of state S0 is a branch, the status decode SD bits from the previous instruction are valid during Q1 of S1 so the decision of branch or not is made at this point. Meanwhile, of course, another instruction fetch has begun so if the branch condition is met the instruction delivered to P-Bus during Q2 of S1 is used as the next address; if the condition is not met, however, this instruction is discarded. Assuming the condition is met, the branch address is loaded from IR via P-Bus to PC during Q3 of S1, and the new instruction delivered to IR and P-Bus in Q2 of S2 then decoded and executed beginning at Q3 of S2, FIG. *3r*.

A CALL instruction is executed in the same time sequence as a branch, seen in FIGS. *3p–3r*, except no SD evaluation is needed, and PC+1 is pushed to stack ST during Q3 of S1.

A return instruction RET is a two cycle instruction as illustrated in FIGS. 3*s*–3*u*. If the instruction loaded into the decoders ID1 and ID2 during Q3 of state S0 is RET, the instruction fetch which began with PC+1 and load PC in Q3 of S) is discarded and a pop stack function is performed in Q3 of S1 so the next instruction fetch is to the return address. The instruction fetched during Q4 of S1 is then decoded and executed beginning at Q3 of S2.

Input (or output) instructions are executed in two cycles as illustrated in FIGS. 3*v*–3*x*. Assume the opcode loaded into the decoder ID2 in Q3 of S0 is IN. The instruction fetched beginning at Q3 of S0 is not used; execution is inhibited by the decode of IN. The contents of PC at Q3 of S1 are saved until Q3 of S2 for the next instruction fetch; that is, PC is recirculated back to PC by the increment path, but no increment is performed. The controls #C produced from decode of IN are available for two states. The RAM address is loaded from P-Bus on Q3 of S1, seen in FIG. 3*y*, and the data input reaches D-Bus on Q4 of S1 and is written into RAM **15** during Q2 of S2. The DEN− control is active from Q4 of S1 through Q2 of S2 for the IN function. An OUT instruction is executed like IN except the RAM **15** is read during Q4 of S1 and the WE− control is active instead of DEN−.

A table look up instruction is executed as shown in FIGS. 3*aa*–3*cc*. The TBLR opcode is decoded beginning at Q3 of S0 and causes the Acc to be loaded via D-Bus to BIM in Q2 of S1, then PC is loaded via P-Bus from BIM in Q3 of S1 so the content of Acc is used as the next instruction fetch address. Meanwhile, execution of the instruction fetched beginning at Q3 of S0 is inhibited by preventing a ROM read control #RR from loading IR with the ROM **14** output, at Q2 of S1. The incremented contents of PC from Q3 of S0 are pushed to ST during Q3 of S1, then popped at Q3 of S2 as the next instruction address. The data fetched from ROM **14** (or memory **11**) using the address from Acc during Q4/S1 to Q1/S2 is loaded onto P-Bus during Q2 of S2 where it remains until Q4 of S2 at which time the BIM accepts the data from P-Bus and then transfers it to D-Bus on Q2 of S3, the next state. The destination address for RAM **15** loaded into decoder **15***b* from P-Bus by Q3 of S1 and remains for two states, so the RAM write occurring at Q2 of S3 will use the RAM address defined in the original TBLR opcode.

One of the problems inherent in manufacturing microcomputer devices is that of testing the parts to determine whether or not all of the elements are functional. In many microcomputers, the instruction words read from the internal ROM are not available on external busses and so the ROM cannot be checked in any way other than by executing all possible functions, which can be lengthy. The device of FIG. **2** allows the ROM **14** to be read out one word at a time using the interchange module as illustrated in FIGS. 3*ee*–3*hh*. A test mode, not part of the instruction set of Table A, is entered by holding the I/O ST− pin at above Vdd, for example **10**V, and holding RS− low, producing an input to the decoders ID1 and ID2 causing a ROM output function in which the ROM **14** is accessed every cycle and PC incremented as seen in FIG. 3*ee*. The P-Bus receives the ROM output, FIG. 3*ff*, but the opcodes are not loaded into the decoders ID1, ID2. Instead, the BIM accepts the opcodes from P-Bus on Q4 of each cycle and transfers to D-Bus on the next Q2, as seen in FIG. 3*hh*.

THE CHIP LAYOUT

In FIG. **4**, the microcomputer **10** of FIGS. **1** and **2** is illustrated in chip layout form. This is a top view of an MOS/LSI chip which is about 150 mils on a side. A major part of the area of the chip **10** is occupied by the memory including the ROM **14** and RAM **15** with their address decoders, and by the 16×16 multiplier M. The ROM **14** has associated with it an X address decoder **14**X and a separate Y address decoder **14***y* for instruction word output; twelve address bits are used to define one of up to 4096 16-bit words in the ROM **14**, although in this example only 1536 are on-chip.

The RAM **15** has an X address decoder **15***b*–*x* which selects 1-of-72 row lines, and a Y address decoder **15***b*–*y* and sense amplifiers **15***s* which select 1-of-2 column lines, so only eight bits are needed for the RAM select in this embodiment (eight bits could accomodate a 256 byte RAM).

The busses RA and D have twelve or sixteen bonding pads on the chip (total of twenty-eight) for connection to external, and the areas of the chip around these bonding pads seen in FIG. **4** are occupied by the buffers used for the ports. It will be noted that the RA bus is only used for output, so only output buffers are needed for this port, while the D-Bus requires tri-state output buffers as well as input buffers.

The multiplier M, shifter S, ALU, accumulator Acc and auxiliary registers AR0, AR1 on the chip **10** of FIG. **4** comprise a 32-bit wide "strip" which is an array of rows (parallel to control lines #C) and columns (parallel to metal bus lines such as D-Bus and P-Bus and ALU and register bits) containing all of the 16-bit and 32-bit registers, ALU bits, and the like circuitry associated with the D-Bus and related control lines #C. As set forth in U.S. Pat. No. 4,402,044 issued to McDonough and Guttag, assigned to Texas Instruments, an important feature is that the 32-bit ALU and its associated 32-bit Acc registers, the two 16-bit AR registers, the shifter S, and the bus interchange BIM as described above are laid out on the MOS/LSI chip **10** in a regular strip pattern as seen in FIG. **4**. Other circuitry connected to the D-Bus and the ALU-b input and having controls #C shared by sixteen or thirty-two bits may also be in the strip, such as AR and BIM. The Acc and the ALU each contain thirty-two bits or stages which are laid out in a regular pattern like memory cells, the bits arrayed and aligned horizontally and vertically as seen in FIG. **4**. D-Bus and P-Bus of FIG. **2** are each sixteen parallel metal strips on top of the cells of the ALU and registers, and all of the dozens of control lines #C are horizontal polysilicon lines typically used as the control gates for transistors in the ALU and its associated registers and like circuitry. This layout arrangement is advantageous because the multiplier ALU and registers, and perpendicular control lines #C and metal busses fit in an array with virtually none of the wasted space used merely for routing conductors in conventional contruction of microprocessors. Metal bus lines such as P-Bus and D-Bus and control lines #C are in large part routed over functional regions or cells of the chip in the strip rather than over unused silicon, and many 90 degree turns are produced inherently at functional cells rather than in conductor routing. In the prior devices, the controls, the registers, the ALU, etc. where islands of circuitry connected by busses or conductors. The enlarged view of FIG. **4***a* shows a small part of the strip, two-bits wide, illustrating the metal bus

lines and the polysilicon control lines #C for an N-channel silicon gate MOS device made generally by a single-level polysilicon process according to U.S. Pat. No. 4,055,444, assigned to Texas Instruments. Various contacts (not shown) would be made within each register bit or stage from metal to silicon or to polysilicon. It is significant to note that many of the connecting lines from registers to busses illustrated in FIG. **2** are not physically lines or elongated conductors at all but instead are merely metal-to-silicon or metal-to-poly contact areas along the metal bus lines of FIG. **4***a*. That is, routing of 16-bit or 32-bit sets of parallel conductors is minimized by the strip feature, and the size of the chip **10** is reduced. All busses are not needed in any one part of the strip, and thus the pitch or maximum width of cells of the strip is minimized since the the metal-to-metal spacing is a critical limiting factor in bit density.

The internal program of the microcomputer **10** may be modified at the gate level mask in making the chip. The macro code or program in the ROM **14** is defined by a single mask in the manufacturing process as set forth for example in U.S. Pat. Nos. 3,541,543, 4,208,726 or 4,230,504, assigned to Texas Instruments. By rewriting this user or macrocode, keeping the instruction set defined by **ID1** and ID2 the same, a wide variety of different functions and operations are available.

ARITHMETIC LOGIC UNIT

A detailed schematic diagram of one bit of the 32-bit ALU is shown in FIG. **5***a*. The ALU operates under control of six of the #C commands from the instruction decode **ID1**, these commands being labelled #AUM-**0**–#AUM**4** (valid on Q2) and #AUAB (valid on Q1). The ALU-a input, inverted, is on line AUa and the ALU-b input inverted, is on line AUb, both being valid on Q1, one from Acc and the other from the shifter S or P register. The ALU output is at line AUc, valid on Q4, representing one of the inverted 32-bit parallel output ALU-o to Acc. Table B shows the function produced by operation of the ALU for various combinations of the six #C commands. This ALU is generally the same as U.S. Pat. No. 4,422,143, issued to Karl M. Guttag, assigned to Texas Instruments. Propagate and generate nodes AUp and AUg are precharged on Q1 and conditionally discharged by transistors AUd controlled by the ALU-a input, transistor AUe controlled by the ALU-b input and its complement, and transistors AUf controlled by the #AUM0–#AUM3 commands, according to the functions of Table B. A carry-out node AUh and a carry-in node AUi for each bit are coupled by a propagate-carry transistor AUj controlled by a line AUk which is the propagate node AUp inverted. The carry-out node AUh is precharged on Q1 and conditionally discharged via transistor AUm which is controlled by a NOR gate having the generate node AUg as one input and the absolute value command #AUAB as the other, so if #AUAB is 1 the transistor AUm is off and carry-out bar is always 1, meaning no carry or absolute value. If #AUAB is 0, the generate signal on AUg controls. The inverted propagate signal on AUk is one input to an Exclusive Nor circuit AUn with static load AUq; the inverted carry-in bar of line AUi is the other input to the Exclusive NOR, resulting in an output AUr which inverted is the ALU output AUc. The carry-in bar node AUi is made unconditionally 0 when control #AUM4 is high for logic functions OR, AND and EXOR, so this input to circuit AUn is unconditionally 1, but for ADD, SUB, etc., the control #AUM4 is 0 and the carry-in from the node AUu of the next low-order bit of the ALU controls.

THE SHIFTER S

Referring to FIG. **5***b*, the shifter S includes a 16-bit input Si, a shift matrix Sm, a shift controller Sc, and a 32-bit output So going to the ALU-b input. The input Si is connected to receive the D-Bus at all times and to drive lines Sf in the matrix Sm through high level buffers. If no shift is to be performed, a line Sg is high, turning on all sixteen of the transistors Sh for this line, so the 16-bit data on lines Sf will appear on the sixteen right-most output lines So via diagonal lines Sj. All of the lines Sf are precharged on Q3 via thirty-two transistors Sk then conditionally discharged by the input Si. The sign bit is extended by detecting the MSB bit-**0** of the input Si by the line Sm. A gate Sn also receives a #NEX not extend command from **ID1** (one of the controls #C) to kill the sign extension for certain instructions of Table A. Based on the incoming sign bit Sm and #NEX, the gate Sn generates an extend command on line Sq to transistors Sq'. The transistors Sq' in series with lines Sr conditionally discharge the nodes Ss on lines Sf through transistors St. The control Sc is a 1-of-16 decoder or selector which receives the bits **4**–**7** of the instruction word from the P-Bus on 4-bit input Sp during Q3 and activates one of the sixteen lines Su; the lines Su are precharged in Q3 via transistors Sup and conditionally discharged during Q4 via transistors Sud and Sc'. The controls for the shifter S consist of the 4-bit value on Sp (the SSSS field of the ADD instruction, for example) defining the number of positions of left shift, and controls on lines #C for negating sign extension, etc. Since the data is usually in two's complement, the sign bit is extended to all bits to the left of the most significant data bit. The sign bit is 0 for positive and 1 for negative. If the shift is to be seven bits, for example, the seventh line Su stays high on Q4 and all others go low. This turns on all transistors Sh and St in the seventh row and all other transistors Sh and St are off. The 16-bit data coming in on lines Si thus moved via transistors Sh and lines Sj to a position on lines So seven bits to the left of the zero shift (right-most) position, and zero-filled to the right due to the prcharge Sk. To the left, the sign bit will stay 0 is the bit-**0** is low, but if bit-0 is 1 then Sq is high, transistors Sq are on, allowing all bits to the left to discharge.

BUS INTERCHANGE MODULE

The bus interchange module BIM, shown in detail in FIG. **5***c*, consists of sixteen identical stages, only one of which is illustrated. Each stage has two clocked inverters Ia, with no feedback loop since data is not held in BIM longer than about half a state time. Input node Ib is connected to the respective bit of P-Bus via one of sixteen transistors Ic driven by a control bit #BIFP valid on Q4. The D-Bus is connected to the input node Ib via transistors Id driven by the control bit #BIFD (Bus Interchange From D) from decoder **ID1** valid on Q2. The output node Ie is connected to the P-Bus by a push-pull stage including transistors If and Ig, and a transistor Ih driven by a control bit #TP, valid during Q2 and Q3. Likewise, output node Ie is coupled to the D-Bus via a push-pull stage having driver transistors Ii and Ij, and a transistor Ik driven by a control bit #BITD valid on Q2 and Q4. The transistors Ig and Ij are driven by node Im at the output of the first inverter Ia, providing a push-pull output. Data is transferred

from D-Bus to nodes Ib, Im, Ie on Q2, and then from these nodes to P-Bus on Q4. Similarly, data is transferred from P-Bus to nodes Ib, Im, Ie on Q4, and then from these nodes to D-Bus on Q4 on the next Q2.

THE MULTIPLIER

Referring to FIG. 5*d*, a schematic representation of the multiplier M and its T and P registers is shown, and corresponding detailed circuit diagrams are shown in FIGS. 5*e*, 5*f*. The 16-bit output of the T register is applied to a set of eight Booth's decoders Mb which produce eight sets of outputs Mc, each set including five functions: shift or no shift, and add, subtract or zero. A set of eight banks of 17-it static carry-feed-forward adders Ma-1 to Ma-8 receive the Mc inputs when the T register is loaded, and so a significant part of the multiplication function is initiated before the MPY instruction is executed. The adders Ma-1 to Ma-8 are static in that no clock Q1–Q4 is needed to cause them to operate. Each stage of each level or bank includes a control section Mm responsive to the decoder outputs Me, and the control section feeds an adder. Level Ma-2 uses half adders and levels Mc-3 to Mc-8 use full adders. The first level Mc-1 does not need an adder because there is no partial product from the prior stage, so it has only the control section. When the MPY instruction is decoded, on Q4 the second operand is applied to the static adders from D-Bus by 16-bit input Mi. As each level of the eight levels of adders Ma-1 to Ma-8 calculates the sum, the partial product is fed forward via lines Mf to the next higher level, except for the two LSBs of each level which are fed to the dynamic adders Md via lines Me. When the static adder array settles, the 17-bit output Mg from the level Ma-8 plus the seven lower level 2-bit LSB outputs Me, is applied to a carry-ripple adder MD(31-stages) to perform the final carry evaluation, producing a 31-bit product in two's complement notation. The 31-bits are sign extended to obtain a 32-bit product in the product register P.

Booth's 2-bits algorithm reduces the number of adder stages to about half the number otherwise required. When performing multiply in the classic pencil and paper method, the right or LS digit of one operand is multiplied by the other operand to produce a partial product, then the next digit is multiplied to produce another partial product which is shifted one digit with respect to the first. Booth's algorithm gave a method of multiplying in binary which allowed two bits to be treated each time, instead of one. Thus, level Ma-1 multiplies the two LSBs of T reg times all bits of D-Bus, producing a partial product Me and Mf. The second level Ma-2 multiplies the next two bits of T reg to D-Bus, adds the partial product Mf from Ma-1, and generates a new partial product Mf and two more bits Me because this operation shifts two bits each level.

In FIG. 5*e*, one of the eight decoders Mb is shown, along with two bits of the T register. The T register stage consists of two inverters Ia with a recirculate transistor Rc clocked in Q4. The stage is loaded via transistor Ta by a #LT command from ID1 occurring on Q2 during an LT instruction. The outputs of two stages of the T register and complements are applied by lines To and Tc to one Booth decoder Mb. The decoder consists of four logic circuits, each having a static load Ba, Bb, Bc or Bd and a pattern of transistors Be with the lines To and Tc applied to the gates. Two of the terms have 1 or 0 fixed in the gates by lines Bf. Outputs Mc-1 and Mc-2 represent no-shift and shift commands and come from the logic stages Be and Bd. Outputs Mc-4 and Mc-5 are true and complement outputs from load Ba of the first of the logic circuits, and these represent add and subtract commands. The output Me-3 from Bb is the zero command.

The first level Ma-1 of the static adders is simpler than the higher levels in that only the D-Bus input Mi and the inputs Mc are involved, with no partial product. Two stages of this first level are seen in FIG. 5*g*, along with two of the seventeen stages of level Ma-2 and level Ma-3. The control sections Mm are all the same on all levels. Note that no elements are clocked.

The decoders Mb and control sections Mm with controls Mc define the Booth's two-bits at a time algorithm which reduces circuitry and increases speed by a factor of two. When two bits are interrogated successively, the only operations required are add, subtract, do nothing or shift by one bit. Considering the input from T as one operand, and from D-Bus as the other, the following table describes the function

Ti + 1	Ti	(Ti − 1)	Function	Partial Product
0	0	(0)	Do nothing	K + O
0	0	(1)	Add D	K + D
0	1	(0)	Add D	K + D
0	1	(1)	Shift D & Add	K + 2D
1	0	(0)	Shift D & Add	K − 2D
1	0	(1)	Subtract D	K − D
1	1	(0)	Subtract D	K − D
1	1	(1)	Do nothing	K + O

An example of multiplication using Booth's two bit algorithm is as follows:

D = 001101 (= 13 decimal)
T = 100111(0) (= −25 decimal)

	Ti+1	Ti	(Ti−1)
000000000000 — — —	1	1	(0) → K − D
111111(10011) — — —	0	1	(1) → K + 2D
000(001101)0 — — —	1	0	(0) → K − 2D
1(110011)0			
111010111011			

(= −325 decimal)

In the control sections Mm the inputs Mi from the D-Bus are controlled by a transistor Mm-1 and control Mc-1, not shift. The Mi input for the adjacent bit is gated in by transistor Mm-2 and the Mc-2 shift command, providing the "2D" function as just described. The zero is provided by transistor Mm-3 and zero control Mc-3 which results in mode Mm-4 being connected to Vcc (zero in two's complement). The carry-in from

the prior stage is on line Mm-5, and the partial product from the prior stage is on line Mm-6. The add or subtract control is provided by transistors Mm-7 controlled by the Mc-4 and Mc-5 add and subtract commands. The full adder includes logic gate Mn-1 receiving the outputs of the control section, as well as gates Mn-2 and the exclusive Nor Mn-3, producing a sum on line Mn-4 and a carry on line Mn-5. Speed is increased by using carry feed forward instead of carry ripple on the same level. Level Ma-1 has no partial product or sum Mm-6 from the prior stage, nor carry-in Mn-5, so the adder is not needed, only the control, producing a sum (a difference) at mode Mn-8 and no carry. The second level Ma-2 is a half adder since no carry feed forward is received from Ma-1.

One of the adder stages of the 31-stage ripple-through carry adder is shown in FIG. 5*f*, along with one stage of the P register. The adder stage receives two inputs Me, gated on Q1 or Q3 by transistors Md1. The six LSBs of adder Md have their inputs gated in on Q1 because the static array levels Ma-1, Ma-2 and Ma-3 will have settled and outputs Me will be valid at this point, so the add and ripple through in Md can begin, although the outputs Mf are not yet valid. Thus, the more significant bits are gated on Q3 at transistors Md1. A carry input Md2 from the next lower-significant stage is applied to one input of an exclusive NOR circuit Md3, and to a carrry output gate Md4 which produces a carry output Md5 to the next higher stage. A propagate term is generated from the inputs Me and the carry-in by logic gate Md6, and a carry generate term by a logic gate Md7 with Md4. The same output Md8 is connected by line Md9 to the input of the P register stage, gated by #LPR (load P Reg) from ID1 on Q4 by transistor Pa. The P register stage consists of pair of inverters Ia and recirculate transistor Rc gated on Q2. The output is applied to the ALU-b input on Q1 by gate Pb with #NRPR (not read P Reg) from ID1 as one input, along with an inverter Pc. Transistor Pd precharges the ALU-b input on Q4.

The timing of the multiplier operation is illustrated in FIGS. 3*jj* to 3*mm*. On Q2 of So, the register is loaded and outputs Mc from the Booth's decoder become valid. The Mi inputs from D-Bus are valid at Q4 of S1, assuming the MPY instruction is valid in decoder ID1 at Q3 of S1. The lower bits of the dynamic adder Md are loaded with Me on Q1 of S2, via Md1, and the carry begins to ripple through the lower of the 31-bits, then this continues in Q3 of S2 through the output Mf of the upper levels, so P register is loaded on Q4 of S2 via Pa, where the data remains until loaded to ALU-b on Q1 of a succeeding cycle.

THE RAM

The cell used in the RAM 15 is a pseudo-static 6-transistor cell as seen in FIG. 5*g*. This cell differs from the traditional 6-transistor static cell in that refresh transistors 15*m* are used in place of polysilicon resisters or depletion transistors used as load impedences. The implanted resistors or depletion devices are larger and interpose process complexities. The storage nodes 15*n* are connected through cross-coupled driver transistors 15*p* to ground; one transistor 15*p* is on and the other off, storing a 1 or 0. Read or write is through access transistors 15*q* to data and data bar lines 15*r*, with gates of the transistors 15*q* driven by a row address line 15*s*. Refresh is accomplished when the refresh line 15*t* is pulsed high allowing the node 15*n* which is at 1 to be charged back up to a level near Vdd, while the 0 node 15*n* will conduct the pulse of current to ground through the on transistor 15*p*. The row address on 15*s* is delayed slightly from the refresh line 15*t* so that both won't begin at the same time. In the timing sequence of the FIGS. 3*a*–3*e*, particularly FIGS. 3*j* and 3*o*, the cell of FIG. 5*j* is read in Q4 of any cycle, or written into on Q2.

Referring to FIG. 5*k*, several of the cells of FIG. 5*g* are shown in a column. The data and data bar lines 15*r* are precharged to Vdd-Vt on Q1 and Q3 by transistors 15*u*. The refresh address on lines 15*t*-0, 15*t*-1 and 15*t*-2, etc., occur in sequence, one-at-a-time, generated by a ring counter; for example, if the RAM 15 is partitioned in 64 rows, then a 64 bit ring counter generates one refresh address bit each state time, refreshing the entire array once each 64 states. The refresh pulse occurs on a line 15*t* during Q3, while transistors 15*u* precharge and equallize the data and data bar lines. A row address on a line 15*s* might begin to come up to 1 during the later part of Q3 since read access is in Q4, so the sizes of the transistors are such that nodes 15*n* will not be both forced to Vdd-Vt when transistors 15*m* and 15*q* are all turned on. The on transistor in the pair 15*p* will hold the 0 node lower than the 1 node. After the refresh pulse on 15*t* goes low, for a cell addressed for both read and refresh in Q3, the delayed Q3 address line stays high momentarily to assure that the zero-going line 15*r* will discharge at least slightly through 15*q* and 15*p* for the 0 side. Then a bistable sense circuit including cross-coupled transistors 15*v* is activated by transistor 15*w* having Q4 on its gate (delayed slightly to make sure Q3 has gone to zero). This flips the data and data bar lines to full logic level, after which the column access transistors 15*y* are activated for the addressed column and data can be read out onto the D-bus. Internal shift is implemented by lines 15*x* connecting nodes 15*z* to adjacent column lines 15*r* via transistors 15*z* activated by a RAM move command #RM from decoder ID1, occuring on Q4. The data is held until Q2 of the next cycle (after Q1 precharge of all data and data bar lines 15*r*) before being applied to the adjacent column for this move operation. Meanwhile, the row address may be incremented by 1; i.e., the next higher line 15*t*-1, etc., goes high so on Q2 the data is written into the next higher location.

The sixteen bits of the RAM 15 are arranged as seen in FIG. 5*i*, with column lines (data and data bar lines) 15*r* running vertical and row lines 15*s* horizontal. The RAM is only 32-columns wide, so the column select 15*y* is merely one-of-two, even or odd. There are in this embodiment 144 row lines 15*s*. The LSB of the address 15*b* to the RAM is the column address, even or odd. To implement the data move operation, on even columns the LSB of the address buffer is complemented, but for odd columns the LSB of the address buffer is complemented and also the row decoder output on line 15*s* is incremented.

TABLE A

THE INSTRUCTION SET

Source Code	Object Code-Binary	No. of Cycles	No. of Words	DESCRIPTION
ADD	0000SSSSIAAAAAAA	1	1	Add word at RAM address A (shifted S places to left) to Acc; Result to Acc
SUB	0001SSSSIAAAAAAA	1	1	Subtract word at address A (shifted S places to left) from ACC; Result to Acc
LAC	0010SSSSIAAAAAAA	1	1	Load Acc with word at address A (shifted S places to left)
SAR	00110RRRIAAAAAAA	1	1	Store contents of Aux Reg number R at location defined by A
LAR	00111RRRIAAAAAAA	1	1	Load Aux Reg R with value at location A
IN	01000PPPIAAAAAAA	2	1	Input value on external data bus, store in A
OUT	01001PPPIAAAAAAA	2	1	Output value at address A to ext data bus
SACL	01010XXXIAAAAAAA	1	1	Store low order Acc bits in location A, shifted X places left
SACH	01011XXXIAAAAAAA	1	1	Store high order Acc bits in location A, shifted X places left
ADDH	01100000IAAAAAAA	1	1	Add value at address A to high order Acc bits; result to Acc; no shift
ADDS	01100001IAAAAAAA	1	1	Add Acc to value at address A sign extension suppressed
SUBH	01100010IAAAAAAA	1	1	Subtract value at address A from high order Acc bits; result to Acc; no shift
SUBS	01100AAIAAAAAAA	1	1	Subtract with sign extension suppressed
SUBC	01100100IAAAAAAA	2	1	Conditional subtract for divide; left shift ALu output and conditional +1
ZALH	01100101IAAAAAAA	1	1	Zero Accumulator and Load High under half of Acc with addressed data
ZALS	01100110IAAAAAAA	1	1	Zero Accumlator and Load with sign Extension Suppressed
TBLR	01100111IAAAAAAA	3	1	Table Read; read data from program memory using Acc as address; store in RAM
MAR	01101000IAAAAAAA	1	1	Modify Auxiliary Registers
DSHT	01101001IAAAAAAA	1	1	Data Shift; value defined by A shifted to A+1
LT	01101010IAAAAAAA	1	1	Load T Reg with value defined by A
LTD	01101011IAAAAAAA	1	1	Load T Reg with value A; shift A to A+1; Acc+Preg Acc
LTA	01101100IAAAAAAA	1	1	Load T Reg with value defined by A; Acc+Preg Acc
MPY	01101101IAAAAAAA	1	1	Multiply T times value defined by A, result to P Reg
LDPK	01101110DDDDDDDD	1	1	Load page reg for data memory with 8-bit constant D
LDP	01101111IAAAAAAA	1	1	Load DP reg with value whose address is at A
LARK	01110RRRDDDDDDDD	1	1	Load Auxiliary Register R with 8-bit constant D; MSB's Zero
EXOR	01111000IAAAAAAA	1	1	Exclusive OR Acc with value defined by A; result to LSBs of Acc; zero MSB's
AND	01111001IAAAAAAA	1	1	AND LSB's of Acc with value defined by A; result to LSB's of Acc; (zero)-(MSB's)
OR	01111010IAAAAAAA	1	1	OR LSB's of Acc with value defined by A; result to Acc; (zero)-(MSB's of Acc)
LST	01111011IAAAAAAA	1	1	Load Status with 16-bit value found at location A in RAM
SST	01111100IAAAAAAA	1	1	Store Status in location defined by 8-bit address A in RAM
TBLW	01111101IAAAAAAA	3	1	Table Write; write the value at Ram address to program memory address in Acc
LACK	01111110DDDDDDDD	1	1	Load Accumulator with 8-bit constant from instruction word
NOOP	0111111110000000	1	1	No-operation
DINT	0111111110000000	1	1	Disenable Interrupt-masks interrupt input INT
EINT	0111111110000010	1	1	Enable Interrupt-unmasks interrupt input INT
ABS	0111111110001000	1	1	Absolute Value operation; if Acc 0, Acc Acc; else Acc Acc
ZAC	0111111110001001	1	1	Clear Accumulator; zeros Acc
RAMV	0111111110001010	1	1	Reset Overflow Mode
SAMV	0111111110001011	1	1	Set Overflow Mode
CALLA	0111111100001100	2	1	Call subroutine indirect
RET	0111111110001101	2	1	Return from Subroutine
PAC	0111111110001110	1	1	Load accumulator with contents of P Reg
APAC	0111111110001111	1	1	Add accumulator to contents of P Reg; Result to Acc
SPAC	0111111110010000	1	1	Subtract contents of P reg from Accumulator; Result to Acc
MPYK	100CCCCCCCCCCCC	1	1	Multiply by constant C
BARNZ	11110100XXXXXXXX	2	2	Branch if Loop Counter Not Zero, to location defined PC+1
BV	11110101XXXXXXXX	2	2	Branch if Overflow Bit in ST is 1
BIOZ	11110110XXXXXXXX	2	2	Branch if IO Bit in ST (from IO pin) is 1
CALL	11111000XXXXXXXX	2	2	Call Subroutine
B	11111001XXXXXXXX	2	2	Unconditional Branch to location W at PC+1
BLZ	11111010XXXXXXX	2	2	Branch if Acc is less than zero
BLEZ	11111011XXXXXXXX	2	2	Branch if Acc is less than or equal to zero
BGZ	11111100XXXXXXXX	2	2	Branch if Acc is greater than zero
BGEZ	11111101XXXXXXXX	2	2	Branch if Acc is greater than or equal to zero
BNZ	11111110XXXXXXXX	2	2	Branch if Acc is not zero
BZ	11111111XXXXXXXX	2	2	Branch if Acc is equal to zero

TABLE B

ALU FUNCTIONS

	Control Code						Propagate	Generate	
	#AUM0	#AUM1	#AUM2	#AUM3	#AUM4	#AUMB	Node	Node	Output
Add	0	1	1	0	0	0	A+B	AB	$A+B+C_{in}$
Subtract	1	0	0	1	0	0	A+B	AB	$A+B+C_{in}$
Load Acc	0	1	0	1	1	0	B	X	B+1=B
Exclusive Or	1	0	0	1	1	0	A+B	X	A+B+1=A+B
Or	1	0	0	1	1	0	AB (=A+B)	X	A+B+1=A+B
And	0	1	1	1	1	0	A+AB	X	(A+AB)+1=A+B=A
Abs. Value	0	0	1	1	0	1	A	0	$A+C_{in}$

What is claimed is:

1. A microcomputer formed in a single integrated circuit comprising:

an arithmetic/logic unit having data input and data output;

a data memory having an address input and having data input/output means;

data bus means coupled to the data input and data output of the arithmetic/logic unit and coupled to the data input/output means of the data memory, the data bus means transferring multi-bit data;

a program memory having an address input and having an instruction output, the program memory storing instruction words;

program address means having an input and including incrementing means; said program address means having an output connected to said address input of the program memory means;

control means for generating controls in response to instruction words; the controls defining operation of the arithmetic/logic unit, transfer of multi-bit data to and from the data bus means, and operation of said program address means;

program bus means coupling said instruction output to an input of said control means, and to said input of said program address means, the program bus means transferring multi-bit information;

timing means for establishing repetitive operating cycles wherein during one of said operating cycles multi-bit data is transferred from the data memory to the data input of the arithmetic/logic unit via said data bus means, the program address means applies an address to the address input of the program memory, and the control means receives an instruction word from the instruction output via said program bus means;

bus interchange means within said integrated circuit and coupled to said data bus means and to said program bus means for

(a) transferring said multi-bit data from the data bus means to the program bus means and for transferring said multi-bit data from the program bus means to said input of said program address means, both during one of said operating cycles, and

(b) transferring said multibit information from said instruction output of said program memory to said program bus means and transferring said multibit information from said program bus means to said data bus means, both during one of said operating cycles,

(c) all said transferring being in response to controls received from said control means generated from a single one of said instruction words.

2. A device according to claim **1** wherein:

after transferring said multi-bit data and multi-bit information in response to said single one of said instruction words via said bus interchange means,

multi-bit information from the program bus means is valid on said data bus means during one part of said one of said operating cycles and

multi-bit data from the data bus means is valid on said program bus means during another part of a different one of said operating cycles.

3. A device according to claim **2** wherein the bus interchange means receives said multi-bit data from the data bus means only during said one part for transfer to the program bus means, and receives said multi-bit information from the program bus means during said another part for transfer to the data bus means.

4. A device according to claim **1** wherein the data output of the arithmetic/logic unit is coupled to an accumulator and an output of the accumulator is coupled to the data bus means.

5. A device according to claim **4** wherein an output of the accumulator is coupled to a data input of the arithmetic/logic unit.

6. A microcomputer formed in a single integrated circuit comprising:

an arithmetic/logic unit having data input and data output;

a data memory having an address input and having data input/output means;

data bus means coupled to the data input and data output of the arithmetic/logic unit and coupled to the data input/output means of the data memory, the data bus means transferring multi-bit data;

a program memory having an address input and having an instruction output, the program memory storing instruction words;

program address means having an input and including incrementing means; said program address having an output connected to said address input of the program memory means;

program bus means separate from the data bus means and coupled to said instruction output and to said input of said program address means, the program bus means transferring multi-bit information;

control means having an input coupled to receive instruction words from said program bus means, said control means generating sets of controls in response to the instruction words; the sets of controls defining operation of the arithmetic/logic unit, transfer of multi-bit data to and from the data bus means, transfer of multibit information to and from the program bus means, and operation of said program address means;

timing means for establishing repetitive operating cycles wherein during one of said operating cycle multi-bit data is transferred from the data memory to the data input of the arithmetic/logic unit via said data bus means, the program address means applies an address to the address input of the program memory, and the control means receives an instruction word from the instruction output via said program bus means;

bus interchange means within said integrated circuit and coupled to said data bus means and to said program bus means, the bus interchange means including:

(a) means for transferring said multi-bit data from the data bus means to the program bus means and for transferring said multi-bit information from the program bus means to said data bus means,

(b) said means for transferring and said control means operating in response to one of said instructions words to transfer multi-bit data from the data bus means via said bus interchannge means to said input of the program address means, in one of said operating cycles,

(c) said means for transferring and said control means operating in response to a given instruction word to transfer multi-bit information from said instruction output of said program memory via said bus interchange means to said data bus means, in one of said operating cycles.

7. A microcomputer according to claim **6** wherein said one instruction word is the same as said given instruction word.

8. A microcomputer according to claim 6 including address and data bus means external to said integrated circuit and coupled to said address bus means and to said data bus means, and program and data memory means external to said integrated circuit coupled to said address and data bus means.

9. A microcomputer according to claim 8 wherein said address and data bus means external to the integrated circuit include an address bus and a data bus.

* * * * *

Exhibit “K”

#12D

TURNER, B

NANO-001/05US
N0765-2008

7/30/97

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on July 3, 1997.

Date: 7-3-97 By: Patricia K. Parry
Patricia K. Parry

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	Examiner: D. Eng
Charles H. Moore et al.	
Serial No. 08/484,918	Art Unit: 2315
Filed: June 7, 1995	
For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK	AMENDMENT Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Amendment is being submitted in response to the Office Action dated **April** 3, 1997 in the above-identified patent application.

IN THE CLAIMS

Please amend claim 73 as follows:

73 (Twice Amended). A microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and [including] being constructed of a second plurality of electronic devices, thus varying the [operating characteristics] processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of [transistors] electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said

integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation.

REMARKS

The above changes to the language of claim 73 clarify that claim and eliminate an inadvertent lack of antecedent basis problem in the former wording of the claim.

Claims 19-21, 65-67 and 72-79 were rejected under 35 U.S.C. § 103 as unpatentable over Magar, U.S. Patent 4,503,500. Shortly before issuing the Office Action, the Examiner had called to indicate that certain claims were allowable over the prior art, but when the undersigned attorney returned the Examiner's call, it was indicated that new prior art had been found and that a new action would be forthcoming. It is assumed that the Magar reference relied on is that new prior art. A review of the Magar reference shows that it is apparently no more pertinent than prior art acknowledged in the application, in that the clock disclosed in the Magar reference is in fact driven by a fixed frequency crystal, which is external to the Magar integrated circuit.

The clock gen circuit shown at the lower right hand edge of Fig. 2a in the Magar patent is of the same general type as shown at 434 in Fig. 17 of the present application, but depicted differently in that it shows the clock gen circuit portion which is on the semiconductor substrate, while Fig. 17 shows the external crystal at 434, connected to I/O interface 432 in the present invention. The crystal clock 434 is thus used in the invention for synchronizing I/O timing with the outside world, while the ring counter variable speed clock 430 also shown in Figure 17 is used for generating on-chip clock signals. The clock 430 is an example of the oscillator recited in the claims, the clock rate of which varies in the same way as a function of one or more device parameters associated with the integrated circuit substrate.

The definitive statement that the clock gen circuit in Fig. 2a in the Magar patent is equivalent to the "conventional crystal clock" 434 in Fig. 17 of the present application is at col. 15, lines 26-41 of Magar:

> "The chip 10 includes a clock generator 17 which has two external pins X1 and X2 to which a crystal (or external generator) is connected. The basic crystal frequency is up to 20 MHz and is represented by a clock 0 of Fig. 3a. This clock 0 has a period of 50 ns, minimum, and is used to generate for quarter-cycle clocks Q1, Q2, Q3 and Q4, seen in FIGS. 3b-3e, providing the basic internal timing for the microcomputer chip 10. A set of four quarter cycle clocks Q1 to Q4 defines one machine state of time of 200 ns., minimum; the states are referred to as SO, S1, S2 in FIG 3. The clock generator produces an output CLKOUT, Fig. 3f, on one of the control bus lines 13. CLKOUT has the same period as

Q1, but 50% duty cycle and beginning at the midpoint of Q1. This output is used for timing or synchronizing external components of the system of FIG. 1."

This description in Magar should be contrasted with the following detailed description of an embodiment of the present invention, as shown in Fig. 17, at explained at page **32,** lines **3-29:**

"Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor 50 provides a dual-clock scheme as shown in Figure 17, with the CPU 70 operating asynchronously to I/O interface **432** forming part of memory controller 118 (Figure **2)** and the I/O interface **432** operating synchronously with the external world of memory and I/O devices. The CPU 70 executes at the fastest speed possible using the adaptive ring counter clock **430.** Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor 50 for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface **432,** speed of which is controlled by a conventional crystal clock **434.** The interface **432** processes requests for memory accesses from the microprocessor 50 and acknowledges the presence of I/O data. The microprocessor 50 fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. By decoupling the variable speed of the CPU 70 from the fixed speed of the I/O interface **432,** optimum performance can be achieved by each. Recoupling between the CPU 70 and the interface **432** is accomplished with handshake signals on lines **436,** with data/addresses passing on bus **90,** 136."

From these two quotations, it is clear that the element in Fig. 17 missing from Fig. 2a in Magar is the ring counter variable speed clock 430, and that Magar is merely representative of the "most microprocessors" acknowledged as prior art in the above description from the present application, which prior art microprocessors use a "conventional crystal clock." Because the variable speed clock is a primary point of departure from the prior art, independent claims 19, 65, **73** and 78 all recite a system including a variable speed clock or a method including using a variable speed clock. In light of the prior art, of which Magar is a good example, Applicants are entitled to claims of this scope. Dependent claims 20, 66, 74 and 79 further recite a second clock, exemplified by the crystal clock **434** in Fig. 17.

Contrary to the Examiner's assertion in the rejection that "one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock vary together due to manufacturing variation, operating voltage and temperature of the IC", one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock *do not* vary together due to manufacturing variation, operating voltage and temperature of the IC in the Magar microprocessor, as taught in the above quotation from the reference. This is simply because the Magar microprocessor clock is

frequency controlled by a crystal which is also external to the microprocessor. Crystals are by design fixed-frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The Magar microprocessor in no way contemplates a variable speed clock as claimed.

In making the rejection based on Magar, the examiner appears to be confusing the multiple uses and meanings of the technical term "clock." A clock is simply an electrical pulse relative to which events take place. Conventionally, a CPU is driven by a clock that is generated by an crystal. The crystal might be connected directly to two pins on the CPU, as in Magar, and be caused to oscillate by circuitry contained in the CPU with the aid of possibly other external components. Alternatively, the crystal may be contained in a package with the oscillation circuitry, the packaged component thus called an oscillator, and connected to one pin on the CPU as in Edwards et al., U.S. Patent 4,680,698.

While an oscillator may be a clock, a clock is not usually an oscillator. An oscillator must exist someplace in the circuit from which a periodic clock is derived. In both cases, the crystal (or the entire oscillator in the second case) is external to the CPU, and the output of the oscillator circuitry is a "clock." This clock is typically modified to produce additional required clock signals for the system. The many clock signals are sometimes created by circuitry called a "clock generator." For example, see Magar, Fig. 2a. The "clock gen" connects to a crystal at external pins X1 and X2 and generates clock signals for the system Q1, Q2, Q3, Q4 and CLKOUT. Other cited reference have similar examples, see Palmer, U.S. Patent 4,338,675, Fig. 1, item 24; Pohlman et al., U.S. Patent 4, 112,490 Fig. 1, item 22. All these systems operate at a frequency determined by the external crystal. The single, fixed, oscillation frequency of the crystal is determined by how the device is manufactured, i.e., how the crystal is cut and trimmed, and other factors. Crystals are used precisely for this purpose; they oscillate at a given frequency within a tolerance determined by their manufacture. Because of the cutting and trimming required, and that the crystal slice is typically suspended by two wires to allow it to freely oscillate, crystal oscillators have never, to Applicants' knowledge, been fabricated on a single silicon substrate with a CPU, for instance. Even if they were, as previously mentioned, crystals are by design fixed-frequency devices whose oscillation frequency is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The oscillation frequency of a crystal on the same substrate with the microprocessor would inherently not vary due to variations in manufacturing, operating voltage and temperature in the same way as the frequency capability of the microprocessor on the same underlying substrate, as claimed.

Note that the term clock can refer to many different signals since the definition is broad, and that it can also refer to the oscillator that is required to generate the clock. While a crystal-controlled oscillator typically operates at a single speed, the circuitry around the crystal may be

designed so that the output of the entire oscillator circuit can be varied. Many mechanisms can be used to control the output of a variable-frequency oscillator, including manual inputs, program-controlled inputs, temperature sensors, or other devices. Non-crystal controlled oscillators are also possible, and when they are designed as variable-frequency oscillators they are typically also controlled by manual inputs, program-controlled inputs, temperature sensors and other devices.

The present invention is unique in that it applies, and can only apply, in the circumstance where the oscillator or variable speed clock is fabricated on the same substrate as the driven device. The example given is a non-crystal controlled circuit, a ring oscillator. **A** ring oscillator will oscillate at a frequency determined by its fabrication and design and the operating environment. Thus in this example, the user designs the ring oscillator (clock) to oscillate at a frequency appropriate for the driven device when both the oscillator and the device are under specified fabrication and environmental parameters. Crucial to the present invention is that since both the oscillator or variable speed clock and driven device are on the same substrate, when the fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together. This differs from all cited references in that the oscillator or variable speed clock and the driven device are on the same substrate, and that the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so. Like the cited references, the driven device might additionally contain clock generation circuitry to produce variations on the clock output of the oscillator or variable speed clock for the other circuitry on the device.

The remaining Bennett et al., Brantingham, Pollack, Gruner et al.and Suzuki et al. references, cited but not applied in a rejection, have been reviewed and found not pertinent to the invention as claimed.

Based on the above remarks, the rejection under 35 USC § 103 is believed to be overcome. All of the claims in the application are believed to be patentable over the prior art. This application is believed to be in condition for allowance, and allowance is solicited.

Respectfully submitted,

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Exhibit “L”

PATENT

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N0765-2008

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Date: 2/6/98 By: Patricia K. Carry
Patricia K. Parry

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Charles H. Moore et al.

Serial No. 08/484,918

Filed: June 7, 1995

For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

Examiner: D. Eng

Art Unit: 2784

AMENDMENT

Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Amendment is being submitted in response to the Office Action dated October 16, 1997 in the above-identified patent application.

IN THE CLAIMS

Please amend claims 19, 65, 73 and 78 as follows:

19(Three Times Amended). A microprocessor system, comprising a single integrated circuit including a central processing unit and [a] an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit.

Sub 72 65(Three Times Amended). In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:

providing [a] an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor; and

using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock.

Sub 73 73(Three Times Amended). **A** microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation.

Sub 74 78(Twice Amended). In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of

providing said central processing unit upon [a] an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing [a] an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors; and

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way

relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate.

REMARKS

Claims 19-21, 65-67 and 72-79 were rejected under 35 U.S.C. § 103 as unpatentable over Magar, U.S. Patent 4,503,500, in view of newly cited Pelgrom et al., U.S. Patent 4,627,082. In response, the independent claims have been rewritten to specify that the entire ring oscillator variable speed system clock, variable speed clock or oscillator be provided in the integrated circuit, in order to sharpen the distinction over the prior art. Because the prior art does not provide an entire ring oscillator variable speed system clock, variable speed clock or oscillator in the integrated circuit, in that the prior art circuits require an external crystal, the prior art fails to teach or suggest the invention as now claimed. This rejection is believed to be overcome by these changes to the claims and these remarks.

Shortly before this Office Action was mailed, Mr. George Shaw, the Assignee's technical representative, and the undersigned attorney had a phone interview with the Examiner regarding this and another of Assignee's cases. Technical distinctions of the present case over the Magar reference previously cited were discussed, as well as the benefits of the invention. Below is recited the pertinent points of that discussion, as well as rebuttal to the new Pelgrom reference.

First, the Examiner states "Pelgrom teaches that electronic components would exhibit same characteristics if they are manufactured by the same process technology", and applicant agrees that this is well known in the art. The Examiner states that, "Since Pelgrom's [Magar's?] microprocessor is made of electronic components, it would have obvious, from the teaching of Pelgrom, to a person of ordinary skill in the art to have the components of Magar' microprocessor and clock (oscillator) make of the same process for ensuring processing frequency of the cpu to track the clock rate in response to the parameter variations." Applicant agrees that the processing frequency capability of the CPU would track the clock rate capability of the clock generator, as this is controlled by the laws of physics on which the Pelgrom reference is based. However, there would be no "tracking" of the clock rate produced by the Magar clock generator, because the entire circuit is not provided on the integrated circuit. Magar's clock generator relies on an external crystal connected to terminals X1 and X2 to oscillate, as is conventional in microprocessor designs. It is not an entire oscillator in itself. And with the crystal, the clock rate generated is also conventional in that it is at a fixed, not a variable, frequency. The Magar clock is comparable in operation to the conventional crystal clock 434 depicted in Fig. 17 of the present application for controlling the I/O interface at a fixed rate frequency, arid not at all **like** the clock on which the claims are based, as has been previously stated.

The Examiner also states that "applicants contend that Magar's clock is external to the IC." This is not the case. The "clock gen" part of the oscillator circuit is clearly on the IC, but not the crystal. Applicants note that the crystal is external, connected to X1 and X2, as Magar cites at column 15, lines 26-27,

"The chip 10 includes a clock generator 17 which has two external pins X1 and X2 to which a crystal (or external generator) is connected."

Thus while most of Magar's clock (generator) circuitry is on the IC, the entire oscillator, which because it requires an external crystal, is not.

"The Examiner further states that applicants imply a "correspondence" in application between Applicant's clock 434 and Magar's clock. This is not the case. Applicants only state that the two clocks are "of the same general type" or are "equivalent" at the circuit level, in that they both use an external crystal to fix the clock rate. They are both of conventional design and not the subject of the claims in the instant case. Clearly, either type could be used to drive a CPU, as Magar depicts the conventional case and Applicant depicts a unique design which provides a variable clock frequency or rate.

Applicant's prior comments apparently did not make clear the distinction between an oscillator and a clock as it applies to the Magar reference. As a self-contained on-chip circuit, Magar's clock gen is distinguished from an oscillator in at least that it lacks the crystal or external generator that it requires. Thus Magar's circuit is not an entirely on-chip oscillator as contemplated in the present case, it is only a clock.

As mentioned in Applicant's previous remarks, the term clock is sometimes used interchangeably with oscillator, even inappropriately, leading to confusion. And, adding to the confusion, in the instant case, 430 is both an oscillator and a clock in the conventional senses. It is an oscillator in that it oscillates without external components (unlike the Magar reference). An example of such an oscillator circuit which does not utililze external components is given in Fig. 18 of the present application. It is also a clock in Magar reference sense in that it produces the various required timing signals needed of the CPU. The signals PHASE 0, PHASE 1, PHASE 2, and PHASE 3 in Applicant's Fig 18 are synonymous with Q1, Q2, Q3, and Q4 depicted in Magar Fig. 2a. The essential difference is that the frequency or rate of the PHASE 0, PHASE 1, PHASE 2, and PHASE 3 signals is determined by the processing and/or operating parameters of the integrated circuit containing the Fig. 18 circuit, while the frequency or rate of the Q1, Q2, Q3, and Q4 signals depicted in Magar Fig. 2a are determined by the fixed frequency of the external crystal connected to the circuit portion outputting the Q1, Q2, Q3, and Q4 signals shown in Magar Fig. 2a.

To summarize, the Pelgrom reference teaches well known art as one of the fundamental principles on which IC are designed. If components did not vary in a similar manner circuit performance could not be predicted and ICs could not be designed. This does not negate

patentability in the present case because it is not the fundamental principle that is claimed but the combination in light of the fundamental principle of enumerated heretofore uncombined circuits to produce a result not obtained with the prior art that is the subject of the claims in the instant case. The Magar teaching is well known in the art as a conventional crystal controlled oscillator. It is specifically distinguished from the instant case in that it is both fixed-frequency (being crystal based) and requires an external crystal or external frequency generator.

Based on the above changes to the claims and remarks, the rejection under 35 USC § 103 is believed to be overcome. All of the claims in the application are believed to be patentable over the prior art. This application is believed to be in condition for allowance, and allowance is solicited.

Respectfully submitted,

COOLEY GODWARD LLP

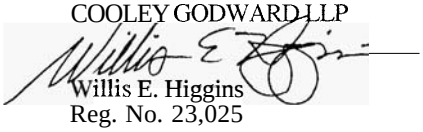

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Exhibit “M”

United States Patent [19]

Sheets

[11] **Patent Number: 4,670,837**

[45] **Date of Patent: Jun. 2, 1987**

[54] **ELECTRICAL SYSTEM HAVING VARIABLE-FREQUENCY CLOCK**

[75] Inventor: **Laurence L. Sheets**, St. Charles, Ill.

[73] Assignees: **American Telephone and Telegraph Company; AT&T Bell Laboratories**, both of Murray Hill, N.J.

[21] Appl. No.: **624,469**

[22] Filed: **Jun. 25, 1984**

[51] **Int. Cl.**[4] **H03K 5/04**

[52] **U.S. Cl.** **364/200**; 328/38.1

[58] **Field of Search** 364/200, 900; 328/62, 328/38; 365/222

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,453,601	7/1969	Bogert et al.	364/200
3,656,123	4/1972	Carnevale et al.	340/172.5
3,775,696	11/1973	Garth	331/57
3,922,526	11/1975	Cochran	235/152
4,037,090	7/1977	Raymond, Jr.	364/200
4,191,998	3/1980	Carmody	364/200
4,241,418	12/1980	Stanley	364/900
4,331,924	5/1982	Elliot et al.	328/38
4,414,637	11/1983	Stanley	364/569
4,438,490	3/1984	Wilder, Jr.	364/200
4,447,870	5/1984	Tague et al.	364/200
4,463,440	7/1984	Nishiura et al.	364/900

FOREIGN PATENT DOCUMENTS

0098653	6/1983	European Pat. Off. .
2248170	4/1974	Fed. Rep. of Germany .

Primary Examiner—Gareth D. Shaw
Assistant Examiner—Randy W. Lacasse
Attorney, Agent, or Firm—Ross T. Watland

[57] **ABSTRACT**

The microprocessor unit of a system implemented using metal-oxide-silicon (MOS) technology, is driven by a variable-frequency clock. The microprocessor controls the clock frequency based on the present rate of required microprocessor activity. By driving the microprocessor unit at a lower clock frequency when such activity rate is low, the energy dissipated by the microprocessor unit is reduced due to the MOS power-frequency characteristic.

7 Claims, 6 Drawing Figures

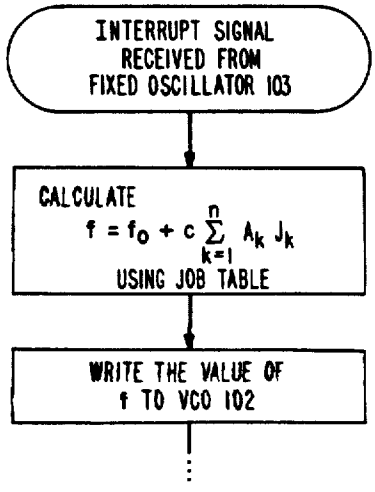


FIG. 1

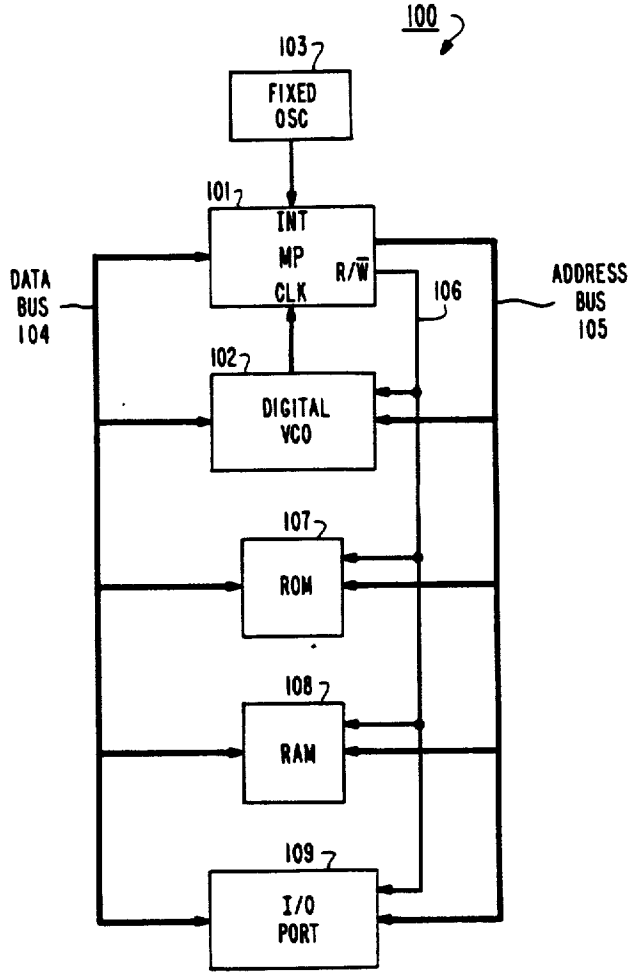

100
103
FIXED OSC
101
INT
MP
CLK
R/W
106
DATA BUS 104
ADDRESS BUS 105
102
DIGITAL VCO
107
ROM
108
RAM
109
I/O PORT

FIG. 2

JOB TABLE

JOB TYPE	NO. OF JOBS TO BE DONE
1	J_1
2	J_2
.	.
.	.
.	.
.	.
.	.
.	.
.	.
n	J_n

FIG. 3

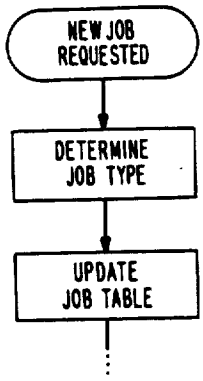


FIG. 4

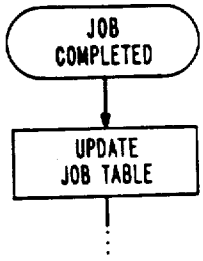
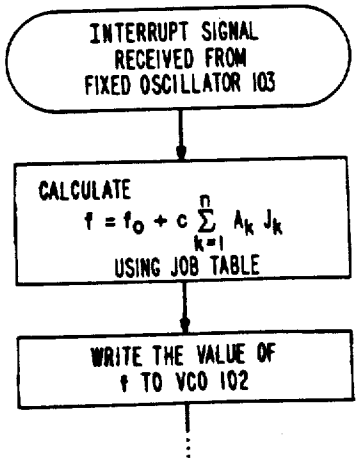


FIG. 5



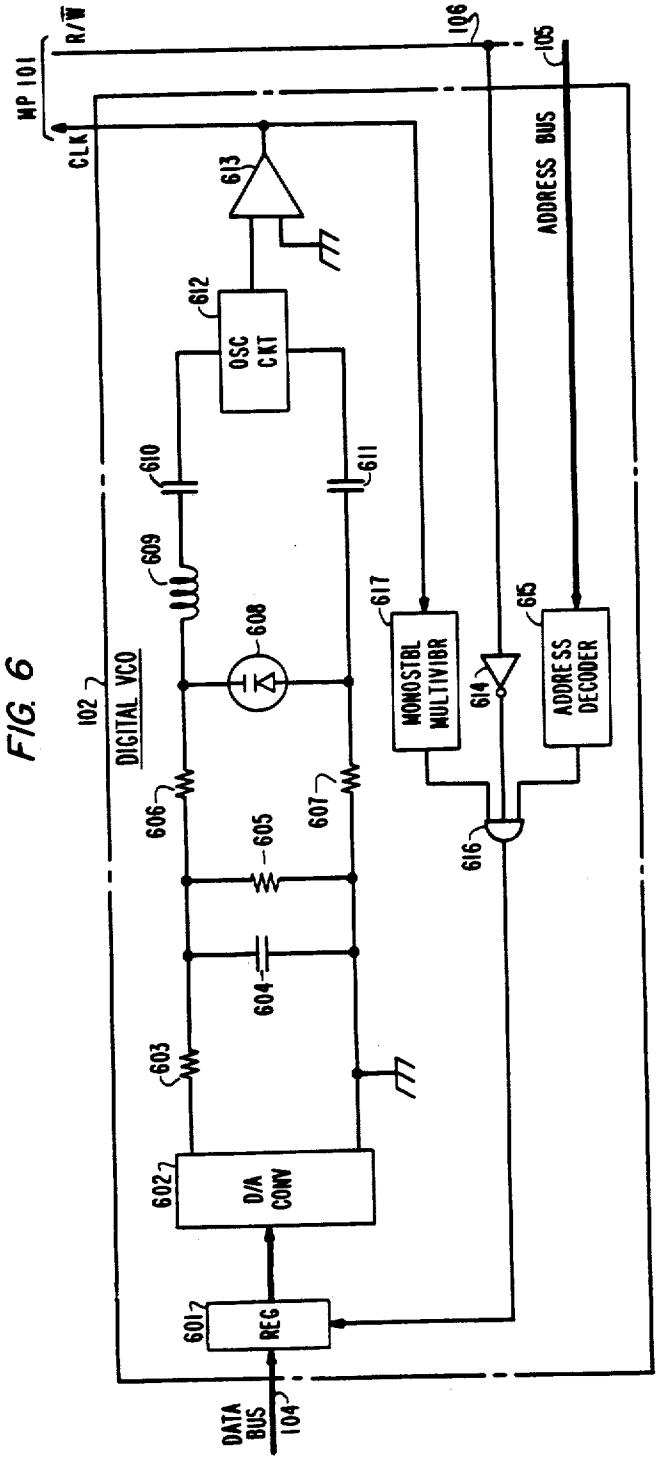

R/W
106
105
MP 101
CLK
613
ADDRESS BUS
612
OSC CKT
610
611
609
608
617
615
MONOSTBL MULTIVIBR
614
ADDRESS DECODER
102
DIGITAL VCO
606
605
607
616
604
603
602
D/A CONV
601
REG
DATA BUS
104

FIG. 6

ELECTRICAL SYSTEM HAVING VARIABLE-FREQUENCY CLOCK

TECHNICAL FIELD

This invention relates to clocked, electrical systems, and, more particularly, to microprocessor-based systems implemented using metal-oxide-silicon (MOS) technology.

BACKGROUND OF THE INVENTION

One very important aspect of the continuing evolution of silicon technology is the proliferation of microprocessors throughout our society. Because of the significant reductions in their size and cost, such processors can be economically used in many applications where the use of computers could not otherwise be justified. Even in applications where larger computers, e.g., minicomputers, have traditionally been used, the advantages of distributed processing have been obtained by using a number of microprocessors to perform the functions previously performed by a single larger processor. For example, many of the control functions previously performed by the central control unit in stored program controlled switching systems are being performed in more modern systems by a number of microprocessors which are distributed toward the system periphery and which communicate with each other to control system operation.

One countervailing factor to weigh against the established advantages of distributed processing is the large amount of power typically required to keep such distributed control processors continuously energized. This factor will become even more important as the cost of energy continues to increase. The power dissipation of microprocessors also becomes important when they are used in portable, battery-powered personal computers. In these applications and others, the ma9nitude of power required to operate microprocessor-based systems is a problem which diminishes the otherwise overall attractiveness of such systems.

SUMMARY OF THE INVENTION

The aforementioned problem is advantageously solved and a technical advance is achieved in accordance with the principles of the invention in both an electrical system driven by a variable-frequency clock and an associated system operation method which reduce the magnitude of energy required by the electrical system by determining the processing load presented to the system and then reducing the clock frequency at which the system is driven, during times when the processing load is reduced. The amount of the saving is dependent on the power-frequency characteristic associated with the particular technology with which the electrical system is implemented.

BRIEF DESCRIPTION OF THE DRAWING

A more complete understanding of the present invention may be obtained from a consideration of the following description when read in conjunction with the drawing in which:

FIG. **1** is a block diagram of a microprocessor-based system illustrating the principles of the present invention;

FIGS. **2** through **5** are diagrams illustrating a method of monitoring the processing load and computing the required clock frequency to reduce the magnitude of energy required by the system of FIG. **1**; and

FIG. **6** is a circuit diagram of a digital, voltage-controlled oscillator included in the system of FIG. **1**.

DETAILED DESCRIPTION

FIG. **1** is a block diagram of an exemplary microprocessor-based system **100** illustrating the principles of the present invention. The system is controlled by a microprocessor **101** which communicates with associated devices via a data bus **104** and an address bus **105**. For example, microprocessor **101** reads information from a read only memory (ROM) **107** via data bus **104** by transmitting a logic one signal from a control terminal $R/\overline{W}$ via a conductor **106** and transmitting on address bus **105**, an address defining both ROM **107** and the particular location of ROM **107** to be read. ROM **107** is typically used to store information such as programs to be executed by microprocessor **101** or fixed data. Microprocessor **101** reads information in like manner from a random access memory (RAM) **108**, used to store variable data, or from an input/output (I/O) port **109**, used to interface with various external devices (not shown), e.g., devices being operated under the control of microprocessor **101**. In addition, microprocessor **101** also writes information via data bus **104** to RAM **108** or I/O port **109** by transmitting a logic zero signal from control terminal $R/\overline{W}$ on conductor **106** and transmitting the appropriate address on address bus **105**.

The portion of system **100** described thus far is well known. Various other control or status signals are typically conveyed between microprocessor **101** and its associated devices to achieve correct system operation. However, since such signals are not relevant to the present invention and tend to vary depending upon the particular family of devices used in a given implementation, they are not further described herein. Microprocessor **101** and its associated devices are energized by means of a DC power source (not shown), e.g., a battery or, alternatively, a DC power supply driven from a commercial AC source. The present invention is directed to reducing the amount of energy drawn by system **100** from such a DC source. In addition to energy savings, an enhancement of long-term system reliability is also obtained.

Microprocessor-based systems such as system **100** are typically implemented using metal-oxide-silicon (MOS) technology. The magnitude of power consumed by a MOS device at a given voltage is substantially directly proportional to the frequency at which the device is operated. In the case of microprocessor **101**, which is a relatively complex MOS device, the duration of each execution cycle is defined by the signal received at a CLK terminal. In accordance with the present exemplary embodiment of the invention, a digital, voltage-controlled oscillator (VCO) **102** transmits the cycle-defining clock signal. Upon determining the amount of processing required at any given time, microprocessor **101** computes an operating frequency that is sufficient to meet the offered processing load. Microprocessor **101**, which communicates with VCO **102** via data bus **104**, address bus **105** and conductor **106** in the same manner as with RAM **108** or I/O port **109**, writes a digital word defined by the computed frequency via data bus **104** to VCO **102**. VCO **102** gradually adjusts the frequency of the clock signal transmitted to microprocessor **101** to the computed frequency in response to the digital word. Reducing the clock frequency reduces

the power consumed by microprocessor **101** and, by reducing the required access rate to the associated devices, i.e., ROM **107**, RAM **108**, and I/O port **109**, also reduces the power consumed by those devices. The power reduction is substantially directly proportional to the reduction of the clock frequency. For example, a frequency reduction from 20 megahertz to 10 megahertz will result in a saving of approximately 50%.

In system **100**, the timing of real-time events is controlled by microprocessor **101** in response to interrupt signals received at an INT terminal from a fixed-frequency oscillator **103**. For example, microprocessor **101** repeats the process of computing the required frequency based on the processing load and writing a digital word to digital VCO **102** at regular intervals as defined by the interrupt signals from fixed oscillator **103**.

In the present embodiment, microprocessor **101** determines its processing load to control the VCO **102** clock frequency at any given time by using a linear regression. All possible processing jobs expected for microprocessor **101** in a particular application, are categorized according to complexity, i.e., the number of execution cycles required for completion, into n job types, where n is a positive integer greater than one. Associated with each job type is a predetermined weighting factor A_k which defines the complexity of that job type with respect to other job types. Microprocessor **101** maintains a job table (FIG. **2**) in RAM **108**. The job table lists for each job type the number, J_k, of jobs of that type presently required. As shown in FIG. **3**, when each processing job is requested, the associated job type is determined and the job table is updated by incrementing J_k by one. Jobs may be requested in a number of ways. For example, certain jobs may be required at regular intervals as defined by the interrupt signals from fixed oscillator **103**. Other jobs may be requested in response to information received from external devices and read via I/O port **109**. After each processing job is completed, the job table is updated by decrementing J_k by one for the associated job type (FIG. **4**). Thus the job table in RAM **108** is kept current at all times. As shown in FIG. **5**, each time that microprocessor **101** receives an interrupt signal from fixed oscillator **103**, microprocessor **101** reads each of the J_k values in the job table and computes the required clock frequency, f, according to

$$f = f_0 + c \sum_{k=1}^{n} A_k J_k,$$

where f_o is the lowest desired frequency and c is an appropriate scale factor. (Alternatively, the A_k weighting factors could be properly scaled to eliminate the need for the scale factor c.) A digital word defined by the computed value of f is then written to VCO **102**.

In the present embodiment, di9ital VCO **102** is implemented as an LC oscillator (FIG. **6**). When microprocessor **101** computes a new clock frequency, it transmits a digital word defined by that frequency via data bus **104** to a register **601**. Microprocessor **101** also transmits an address on address bus **105** to an address decoder **615**. Address decoder **615** responds to the particular address defining VCO **102** by transmitting a logic one signal to an AND gate **616**. Microprocessor **101** transmits a logic zero signal on conductor **106** from its $R/\overline{W}$ terminal to an inverter **614**, which in turn transmits a logic one signal to AND gate **616**. When a monostable multivibrator **617** transmits a logic one signal to a third input terminal of AND gate **616**, AND gate **616** responds by transmitting a logic one signal to register **601** which then stores the digital word from data bus **104**. A D/A converter **602** generates an analog control voltage in response to the digital word in register **601**. The analog control voltage is filtered by a low-pass filter comprised of resistors **603** and **605** and a capacitor **604**, the values of which determine a filter time constant such that the control voltage transmitted varies slowly with respect to the minimum required clock frequency. The resistor **605** is connected across capacitor **604** as a discharging means. The control voltage is then applied via a pair of decoupling resistors **606** and **607** to a varicap diode **608**, having a capacitance that varies from 25 to 100 picofarads with applied voltage. The combination of the variable capacitance of the varicap diode **608** and the inductance of an inductor **609**, e.g., 2.5 microhenries, is coupled via a pair of coupling capacitors **610** and **611** to an oscillator circuit **612**. Oscillator circuit **612**, which is implemented in the present embodiment as an amplifier circuit, transmits a sinusoidal signal at the frequency determined by the combination of varicap diode **608** and inductor **609**. The sinusoidal signal transmitted by circuit **612** is applied to one input terminal of comparator **613**, which has its other input terminal 9rounded. Accordingly, comparator **613** transmits a square wave at the determined frequency. The square wave is transmitted to both the CLK terminal of microprocessor **101** to define its execution cycle and to monostable multivibrator **617** which responds by transmitting a logic one signal to AND gate **616** as described above. Monostable multivibrator **617** transmits a pulse of predetermined duration on the leading edge of the square wave generated by comparator **613** and is included to assure that each data word on data bus **104** is stable before AND gate transmits a logic one signal to store that data word in register **601**.

In this embodiment, the relationship between the clock frequency computed by microprocessor **101** and the digital word transmitted to VCO **102** is predetermined based on the characteristic of VCO **102**. Accordingly, when microprocessor **101** computes a given clock frequency, it transmits a digital word to VCO **102** according to the predetermined relationship such that VCO **102** generates the given clock frequency in response to that digital word.

It is to be understood that the above-described embodiment is merely illustrative of the principles of the present invention and that other embodiments may be devised by those skilled in the art without departing from the spirit and scope of the invention. For example, the LC oscillator implementation of digital VCO **102** may be replaced by a switched RC oscillator where resistors of differing resistance are switched in and out of the circuit to vary the frequency in response to the digital words received by the D/A converter. Rather than computing the frequency based on the processing backlog, the activity on data bus **104** and address bus **105** could be monitored and then used as a basis for determining the required frequency. Instead of using a continuously variable-frequency clock, selections can be made from a small number of discrete frequencies. For example, in a battery-powered personal computer with an operating system which includes a sleep state, the microprocessor CPU could be operated at a low frequency sufficient to keep any dynamic logic re-

freshed, e.g., 500 kilohertz, when the operating system is in the sleep state, and the frequency could then be increased to a nominal operating frequency, e.g., 10 megahertz, when wakeup occurs. In some applications, the desired clock frequency could be determined based on historical activity records rather than in real time. For example, the operating frequency of the distributed microprocessors used for control in a telephone switching system could be adjusted based on calling patterns observed during different times of the day or during different days of the week as a way of reducing the energy requirements of the system. It is to be recognized that any of a number of microprocessor families can be advantageously used in such systems. One specific example is the Motorola 68000 microprocessor and its associated devices. Furthermore, the invention is applicable to clocked, electrical systems other than microprocessor-based systems where power consumption is a function of clock frequency as, for example, in gate arrays.

What is claimed is:

1. In an electrical system driven by a variable-frequency clock to perform processing jobs, a method of operating said system under control of a processor to increase efficiency in power consumption comprising:

determining the processing load of said system based on all requested but uncompleted processing jobs and

adjusting the frequency of said clock basewd on the determined processing load, where each of said processing jobs is one of n types, n being a positive integer greater than one, said method further comprising

maintaining data that define a number, J_K, of jobs of type K for each integer K from one through n, to be performed by said system,

wherein said determining step further comprises reading said data and

wherein said adjusting step further comprises adjusting the frequency, f, of said clock according to

$$f = f_0 + C \sum_{K=1} A_K J_K,$$

wehrein f0 is a minimum frequency, A_K is a weighting factor associated with jobs of type K, and C is a predetermined scale factor.

2. A method in accordance with claim 1 further comprising

repeating at regular intevals said determining step and said adjusting step.

3. A method in accordance with claim 1 wherein said maintianing step further comprises

incrementing said number, J_k, by one as each job of type k is requested and

decremeting said number, J_k, by one as each job of type k is completed.

4. An electrical system comprising:

variable-frequency clock means for transmitting a clock signal of variable frequency,

electrical means for performing processing jobs at an operating frequency defined by the frequency of said clock signal, said electrical means comprising a processor

means for repetitively determining the processing load of said electrical means based on all requested but uncompleted processing jobs and

means coupled to said variable-frequency clock means for adjusting the frequency of said clock signal basedon the processing load determined by said determining means, wherein

each of said processing jobs is one of n types, n being a positive integer greater than one, said system further comprises

means for maintaining data that define a number, J_K, of jobs of type K, for each integer K from one through n, to be performed by said system,

wherein said determining means further comprises means for reading said data

wherein said adjusting means further comprises means for calculating an operating frequency, f, according to

$$f = f_0 + C \sum_{K=1} A_K J_K,$$

wherein f_0 is a minimum frequency, A_K is a weighting factor associated with jobs of type K, and C is a predetermined scale factor and

means for transmitting a digital word defined by said calculated operating frequency, f, to said variable-frequency clock means,

wherein said variable-frequency clock means is responsive to said digital word for generating said clock signal at said calculating operating frequency, f.

5. An electrical system in accordance with claim 4 wherein said variable-frequency clock means further comprises

converter means for generating an analog control voltage in response to said digital word and

oscillator means coupled to said converter means for generating said clock signal at a frequncy defined by said analog control voltage.

6. An electrical system in accordance with claim 5 further comprising

low-pass filter means interposed between said converter means and said oscillato means for filtering said analog control voltage.

7. An electrical system in accordance with claim 4 wherein said electrical means is implemented in metal-oxide-silicon technology.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 4,670,837

DATED : June 2, 1987

INVENTOR(S) : Laurence L. Sheets

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

IN THE CLAIMS

Column 5, line 30, "basewd" should be "based",
Column 5, line 47, "wehrein" should be "where",
Column 5, line 52, "intevals" should be "intervals",
Column 5, line 56, "maintianing" should be "maintaining";
Column 6, line 1, "decremeting" should be "decrementing",
Column 6, line 15, "basedon" should be "based on",
Column 6, line 48, "frequncy" should be "frequency",
Column 6, line 53, "oscillato" should be "oscillator".

Signed and Sealed this

Seventeenth Day of July, 1990

Attest:

Attesting Officer

HARRY F. MANBECK, JR.

Commissioner of Patents and Trademarks

Exhibit “N”

39-.702 GP 2315

PATENT

NANO-001/05US
N0765-2008

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of)

Charles H. Moore et al.

Serial No. 08/484,918

Filed: June 7, 1995

For: HIGH PERFORMANCE, LOW COST MICROPROCESSOR

Examiner: D. Eng

Art Unit: 2315

AMENDMENT

Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Amendment is being submitted in response to the first Office Action in the above-identified patent application.

IN THE SPECIFICATION

At page 1, line 1, please change the title from "HIGH PERFORMANCE, LOW COST MICROPROCESSOR" to --HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK--.

Please rewrite the Abstract as follows:

--A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.--

IN THE CLAIMS

Please amend claims 19-20 and 65-66 as follows:

19(Amended). A microprocessor system, comprising a single integrated circuit a central processing unit and a ring [counter] oscillator variable speed system clock connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring [counter] oscillator variable speed system clock [being provided in a single integrated circuit] each including a plurality of electronic devices of like type, said central processing unit operating at a variable processing frequency dependent upon a variable speed of said ring oscillator variable speed system clock.

20(Amended). The microprocessor system of Claim 19 additionally comprising an input/output interface connected to exchange coupling control signals, address and data with said [input/output interface] central processing unit, and a second clock independent of said ring [counter] oscillator variable speed system clock connected to said input/output interface.

65(Amended). In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:

[which comprises fabricating] providing a ring [counter] oscillator system clock having a plurality of transistors within the integrated circuit, said plurality of transistors having operating characteristics disposed to vary similarly to operating characteristics of transistors included within the microprocessor; [and the microprocessor each having a plurality of transistors having operating characteristics which vary in the same way with variations in their fabrication,] and

using the ring [counter] oscillator system clock for clocking the microprocessor, said central processing unit operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock.

66(Amended). The method of Claim 65 additionally comprising the steps of:

providing an input/output interface for the microprocessor integrated circuit, [and]

clocking the input/output interface with a second clock independent of the ring [counter] oscillator system clock, and

buffering information within said input/output interface received from said microprocessor integrated circuit.

Please add the following new claims 71-79:

71. The microprocessor system of claim 20 further including system memory coupled to said input/output interface, said system memory being synchronized to said second clock and operating synchronously with respect to said ring oscillator variable speed system clock.

72. The method of claim 65 further including the steps of

transferring information to and from said microprocessor in synchrony with said ring oscillator system clock, and

buffering said information to facilitate transfer of said information to and from system memory synchronously with respect to said ring oscillator system clock.

73. A microprocessor system comprising:

a central processing unit disposed upon a substrate, said central processing unit operating at a processing frequency and including a first plurality of transistors;

an oscillator disposed upon said substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and including a second plurality of transistors designed such that operating characteristics of said first plurality and said second plurality of transistors vary in the same way as a function of parameter variation in one or more operational parameters associated with said substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation)

74. The microprocessor system of claim 73 wherein said one or more parameters are included within the set consisting of: operating temperature of said substrate, operating voltage of said substrate, and fabrication process of said substrate.

75. The microprocessor system of claim 73 further comprising:

an input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, address and data with said central processing unit;

an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

76. The microprocessor system of claim 75 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.

77. The microprocessor system of claim 73 wherein said oscillator comprises a ring oscillator.

78. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon a substrate, said central processing unit including a first plurality of transistors and being operative at a processing frequency;

clocking said central processing unit at a clock rate using an oscillator disposed upon said substrate, said oscillator being provided so as to include a second plurality of transistors with said central processing unit being clocked by said oscillator at a variable frequency dependent upon variation in one or more operational parameters associated with said substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more operational parameters associated with said substrate.

79. The method of claim 78 further comprising the steps of

connecting an input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, address and data between said input/output interface and said central processing unit;

clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

REMARKS

This amendment responds to the first office action. Claims 19-20 and 65-66 have been amended, and new claims 71-79 have been added.

The Examiner has requested that applicants update the status of the parent application. Applicants note that the parent application Serial No. 07/389,334 has issued as U.S. Pat. No. 5,440,749. Also pursuant to the Examiner's request, a new title and new abstract more aptly descriptive of the invention have been provided.

The Examiner has rejected claims 19-21 and 65-67 under 35 U.S.C. § 112 as being indefinite. With respect to the apparatus claims, the Examiner asserted that there exists no functional relationship and interconnection between the claimed components. Similarly, the Examiner asserted that a functional relationship does not exist between the steps of the method claims, and that it is unclear what the steps try to accomplish.

Applicants note that the present invention is directed to a microprocessor system including a central processing unit and a ring oscillator variable speed system clock connected thereto. In accordance with the claimed invention, the central processing unit and the ring oscillator variable speed system clock are provided in a single integrated circuit. This allows, for example, the central processing unit to track variations in the speed of the ring oscillator variable speed system clock, since the elements of each are disposed in the same integrated circuit. By this amendment the term "ring counter" has been replaced with "ring oscillator", in order to more particularly identify the ring oscillator (FIG. 18) incorporated within a preferred implementation of the microprocessor system of the invention.

Although applicants submit that the "functional relationship" between the claimed central processing unit and system clock connected thereto is inherently clear, the apparatus and method claims have been amended in an effort to accommodate the Examiner's concerns with respect to 35 **U.S.C.** §112. For example, claim 19 now recites a "functional relationship" in that it is made explicit that the ring oscillator variable speed system clock is disposed to clock the central processing unit. Moreover, the central processing unit and ring oscillator variable speed system clock are described as "each including a plurality of electronic devices of like type". This allows the central processing unit to operate at a

variable processing frequency which depends upon a variable speed of the ring oscillator variable speed system clock. See, for example, the specification at page 31, line *33* to page 32, line 1:

> By deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast. For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor 50 will operate slower than normal. Since the microprocessor 50 *ring oscillator clock 430 is made from the same transistors on the same die as the latches and gates,* it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.

Method claim 65 has been similarly amended, and now recites the step of:

> fabricating a ring oscillator system clock having a plurality of transistors, said plurality of transistors having operating characteristics disposed to vary similarly to operating characteristics of transistors included within the microprocessor ... .

The method claims thus now prescribe a technique for clocking a microprocessor using a ring oscillator system clock comprised of transistors having similar operating characteristics as those within the microprocessor. This advantageously allows the processing frequency of the microprocessor to track the clock rate of the ring oscillator system clock.

The Examiner has rejected claims 19 and *65* under *35* U.S.C. § 103 as being unpatentable over Sheets. The Examiner stated that Sheets teaches a microprocessor system having a microprocessor and a variable speed clock generator. Although admitting that Sheets does not disclose that his clock is implemented using a ring oscillator, the Examiner opined that a "counter is a basis component of [a] clock generator". It was further asserted that choosing the counter to be of the ring type is merely a matter of design choice.

Applicants again observe that the present invention is directed to a system and method for clocking a central processing unit disposed *within the same integrated circuit* as a ring oscillator variable speed system clock. This allows, for example, the central processing unit to track variations in the speed of the ring oscillator variable speed system clock, since the elements of each are disposed in the same integrated circuit. That is, the operational speed of the microprocessor and ring oscillator clock are designed to vary similarly as a function of variation in temperature, processing and other parameters affecting circuit performance.

The system of Sheets effects microprocessor clocking in a way which is entirely dissimilar from that of the present invention, and in fact teaches away from Applicants' clocking scheme. In particular, Sheets describes the use of discrete, commercially available microprocessor chips, e.g., the Motorola 68000 (col. 5, line 16), driven by a separate clock (VCO 12 of FIG. 1). As is well known, such microprocessor chips include terminals or pins, such as the CLK and INT terminals of microprocessor (FIG. 1), for receiving inputs from external devices like the VCO 12 and fixed oscillator 103. Because the VCO 12 is not integral with the microprocessor 101, Sheets has proposed a technique for adjusting the frequency of VCO 12 in accordance with a desired operating frequency of the microprocessor 101. Specifically, a digital word indicative of this desired operating frequency is written by microprocessor 101 to VCO 12 by way of data bus 104 as a means of adjusting clock frequency.

The present invention does not similarly rely upon provision of frequency control information to an external clock, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, since the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance. Sheets' system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.

Although the foregoing clearly indicates the existence of a patentable distinction between the system of Sheets and the present invention, claims 19 and 65 have nonetheless been amended to advance prosecution of the application. Specifically, claims 19 and 65 now explicitly recite that the ring oscillator and microprocessor are provided within the same integrated circuit. Moreover, these claims further state that the plurality of transistors included within the ring oscillator clock have operating characteristics which vary similarly to operating characteristics of transistors included within the microprocessor, thereby enabling the processing frequency of the microprocessor to track the speed of the ring oscillator clock:

> …The CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process.
> (page 32, lines 10-13)

Neither of these aspects of the present invention are suggested by Sheets. As discussed above, Sheets describes the use of commercially available microprocessor chips, and depicts the microprocessor 101 as being coupled to a separate clock (i.e, VCO 12) by way of a data bus 104 and address bus 105. Moreover, the VCO 12 clearly is not comprised of transistors having operating characteristics disposed to vary similarly to those of transistors within the microprocessor 101. Rather, the VCO 12 is seen to be comprised of an LC oscillator (col. 3, line 58 and FIG. 6), which clearly is not adapted to mimic variation in the speed of transistors within the microprocessor 101. Accordingly, applicant respectfully submits that amended claims 19 and 65 are patentable over Sheets, and requests that the rejection thereof under 35 U.S.C. § 103 be withdrawn.

Since Schaire does not supplement the lack of teaching within Sheets with respect to amended claims 19 and 65, it is also respectfully submitted that pending claims 20-21 and 66-67 are patentable over Sheets in view of Schaire. Further with regard to pending claims 20 and 66, it is observed that Schaire provides no indication that bus interface unit 10 is clocked by a signal from a clock different from that used to clock the host microprocessor. That is, the origin of high-speed clock signal 230 (FIG. 1) provided to bus interface unit 10 does not appear to be described. Hence, Schaire fails to teach the claimed provision of separate, independent clock signals to an input/output interface buffer and microprocessor. Accordingly, applicant respectfully requests that the outstanding rejection of claims 20-21 and 66-67 under 35 U.S.C. § 103 be withdrawn.

By this amendment new claims 71-79 have also been added to more particularly identify the invention which appears to be available for protection. In this regard new claims 71-72 point out that information is transferred to and from the microprocessor in synchrony with the ring oscillator system clock, and that this information is buffered to facilitate transfer thereof to and from system memory synchronously with respect to the ring oscillator system clock. New claims 73-79 explicitly recite that the central processing unit and ring oscillator include first and second pluralities of transistors, respectively, and that the

operating characteristics of these transistors vary in the same way as a function of variation in operational parameters (e.g., operating temperature) of the substrate. This advantageously allows a processing frequency of the central processing unit to track a clock rate of the ring oscillator as a function of substrate parameter variation.

Accordingly, in view of the above remarks, it is submitted that this application is now ready for allowance. Early notice to this effect is solicited.

If in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned at (415) 843-5000.

Respectfully submitted,

COOLEY GODWARD CASTRO
HUDDLESON & TATUM

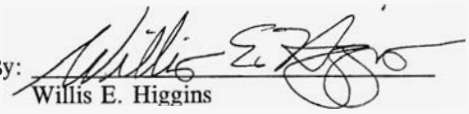
By: 
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Exhibit “O”

71477 U.S. PTO
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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficientpostage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on January 8, 1997.

Date: 1-8-97 By: Patricia K. Parus

IN THE UNITED STATES PATENT AMI) TRADEMARK OFFICE

In re application of

Charles H. Moore et al.

Serial No. 08/484,918

Filed: June 7, 1995

For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

Examiner: D. Eng

Art Unit: 2315

AMENDMENT

Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Amendment is being submitted in response to the Final Rejection dated July 8, 1996 in the above-identified patent application.

IN THE CLAIMS

Please amend claims 19, 65, 66, 71, 72, 73, 74 and 78 as follows;

19(Twice Amended). A microprocessor system, comprising a single integrated sircuit including a central processing unit and a ring oscillator variable speed system clock connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices [of like type] correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit [operating at a variable processing frequency dependent upon a variable speed of] and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said integrated circuit.

65(Twice Amended). In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of

providing a ring oscillator system clock [having a plurality] constructed of [transistors] electronic devices within the integrated circuit, said [plurality of transistors] electronic devices having operating characteristics [disposed to] which will, because said ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary [similarly to] together with operating characteristics of [transistors] electronic devices included within the microprocessor; and

using the ring oscillator system clock for clocking the microprocessor, said [central processing unit] microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock.

66(Twice Amended). The method of Claim 65 additionally comprising the steps of:

providing an input/output interface for the microprocessor integrated circuit, and

clocking the input/output interface with a second clock independent of the ring oscillator system clock[, and

buffering information within said input/output interface received from said microprocessor integrated circuit].

72(Amended). The method of claim 65 further including the [steps] step of

transferring information to and from said microprocessor in synchrony with said ring oscillator system clock[, and

buffering said information to facilitate transfer of said information to and from system memory synchronously with respect to said ring oscillator system clock].

73(Amended). A microprocessor system comprising:

a central processing unit disposed upon [a] an integrated circuit substrate, said central processing unit operating at a processing frequency and [including] constructed of a first plurality of [transistors] electronic devices;

an oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and including a second plurality of [transistors] electronic devices, thus varying the [designed such that] operating characteristics of said first plurality and said second plurality of transistors [vary] in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate thereby enabling said processing frequency to track said clock rate in response to said parameter variation

~~74~~(Amended). The microprocessor system of claim ~~73~~ wherein said one or more operational parameters [are included within the set consisting of:] include operating temperature of said substrate[,] or operating voltage of said substrate[, and fabrication process of said substrate].

~~78~~(Amended). In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon [a] an integrated circuit substrate, said central processing unit [including] being constructed of a first plurality of transistors and being operative at a processing frequency;

providing a variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors; and

clocking said central processing unit at a clock rate using [an oscillator, disposed upon said substrate, said oscillator being provided so as include a second plurality of transistors] variable speed clock with said central processing unit being clocked by said [oscillator] variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate.

Cancel claim 71.

REMARKS

Appreciation is expressed for the courteous and helpful telephone interview granted by the Examiner on January 7 and 8, 1997, with the undersigned attorney and Mr. George Shaw, representing the assignee of the application. The above changes to the claims are based on the discussion in the interview. Proposed changes to claims 19, 65 and 73 were sent by facsmile to the Examiner on January 7 to facilitate the further discussion on January 8. On January 8, the Examiner agreed that these changes merited further consideration of the application and appeared to overcome the prior art of record. The following remarks in part summarize the discussion in the interview and respond to specific points in the Final Rejection.

In the interview, the fact that operating characteristics of electronic devices in an integrated circuit will track one another depending on variations in the manufacturing process used to make the integrated circuit was discussed. This fact is described at page 31, line 1 through page 32, line 1 of this application, in the context of the microprocessor system of this invention. This fact is utilized in the present invention to provide a variable speed clock for the microprocessor, with the

clock speed varying in the same way as variations in the operating characteristics of the electronic devices making up the microprocessor. This allows the microprocessor to operate at its fastest safe operating speed, given its manufacturing process or changes in its operating temperature or voltage. In contrast, prior art microprocessor systems are given a rated speed based on possible worst case operating conditions and an external clock is used to drive them no faster than the rated speed. Under other than worst case operating conditions, the prior art microprocessors are actually capable of operating at a faster clock speed than their rated speed.

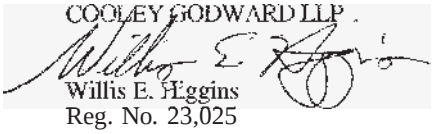
The above changes to the claims have been made to bring out the above distinction over the prior art more clearly. It is believed that they overcome the rejection of claims 19-21, 65-67 and 71-79 under 35 USC § 112, define statutory subject matter, i.e, a system implemented as a single integrated circuit having defined characteristics or a process, as well as distinguishing over the prior art of record.

In the rejection under 35 USC § 103, the Examiner contends that the Sheets reference "clearly indicates in lines 46-48 of column 2 that the system 100 shown in Figure 1 is fabricated *on* a ***single chip*** using MOS technology." Specific issue is taken with the inclusion of the italicized language in this characterization of the reference. Sheets does not say that the system 100 is on a single chip, only that it is implemented in MOS technology. At column 5, lines 15-17, a specific example of the Motorola 68000 microprocessor is given. That microprocessor is driven by an external clock that provides a clock signal to a designated pin of the microprocessor integrated circuit package. Applicants are aware of no prior art teaching or suggesting a variable speed oscillator in the same integrated circuit with a microprocessor and clocking the microprocessor with a clock speed that varies correspondingly with changes in operating characteristics of electronic devices making up the microprocessor, as a result of being in the same integrated circuit as the microprocessor, as claimed. Even if the Examiner is correct that the variable clock in Sheets is in the same integrated circuit as the microprocessor of system 100, that still does not give the claimed subject matter. In Sheets, a command input is required to change the clock speed. In the present invention, the clock speed varies correspondingly to variations in operating parameters of the electronic devices of the microprocessor because both the variable speed clock and the microprocessor are fabricated together in the same integrated circuit. No command input is necessary to change the clock frequency. The rejection under 35 USC § 103 is believed to be overcome.

All of the claims in the application are believed to be patentable over the prior art. This application is believed to be in condition for allowance, and allowance is solicited.

Respectfully submitted,

COOLEY GODWARD LLP



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