(Counsel listed on signature page)

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. HUAWEI TECHNOLOGIES CO., LTD., HUAWEI DEVICE CO., LTD., HUAWEI DEVICE USA INC., FUTUREWEI TECHNOLOGIES, INC., HUAWEI TECHNOLOGIES USA INC., Defendants.	Case No. 3:12-cv-03865-VC (PSG) **PLAINITIFFS' RESPONSIVE CLAIM CONSTRUCTION BRIEF**
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. GARMIN LTD., GARMIN INTERNATIONAL, INC., and GARMIN USA, INC., Defendants.	Case No. 3:12-cv-03870-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. ZTE CORPORATION and ZTE (USA) INC., Defendants.	Case No. 3:12-cv-03876-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. SAMSUNG ELECTRONICS CO., LTD. and SAMSUNG ELECTRONICS AMERICA, INC., Defendants.	Case No. 3:12-cv-03877-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. LG ELECTRONICS, INC. and LG ELECTRONICS U.S.A., INC., Defendants.	Case No. 3:12-cv-03880-VC (PSG)
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I. INTRODUCTION

The intrinsic record does not evidence any clear and unambiguous surrender of claim scope regarding the "entire oscillator" phrase. Defendants' disclaimer position distorts statements made by applicants during prosecution and ignores the context in which they were made. As demonstrated herein, the prosecution history of the patent-in-suit merely reflects that applicants distinguished the claims at issue from the cited references on the basis of other claim limitations. Ultimately, Plaintiffs' construction accurately reflects the true, bargained-for meaning of the "entire oscillator" phrase.

II. ARGUMENT

A. Applicants did not make the disclaimers advanced by Defendants.

Applicants did not make the vague and broad disclaimers advanced by Defendants in their construction of "entire oscillator." To the contrary, in distinguishing over the references cited by Defendants, applicants successfully demonstrated that the references at issue did not satisfy the claim limitations of (i) an on-chip oscillator[1] (ii) whose frequency varied in the same way as the CPU as a function of processing variation, operating voltage, and temperature ("PVT factors").[2] Specifically, the cited references (Magar and Sheets) disclosed either an off-chip crystal or an off-chip oscillator to generate the signal used to clock the CPU. Not only did these references fail to disclose an on-chip oscillator, but the references' oscillators would not vary according to PVT factors in the same way as the CPU. Applicants' arguments for distinguishing the claims at issue from Magar and Sheets were clearly based on limitations present in the claims themselves,

[1] For example, claim 6 recites "a [CPU] *disposed upon an integrated circuit substrate*…" and "an entire oscillator *disposed upon said integrated substrate*…." See Ex. S to Declaration of Barry J. Bumgardner (hereinafter "Bumgardner Decl."), Re-examination Certificate of U.S. Pat. No. 5,809,336, 2:15-20. The parties agree that the "entire oscillator" must be "located entirely on the same semiconductor substrate as the [CPU]…."

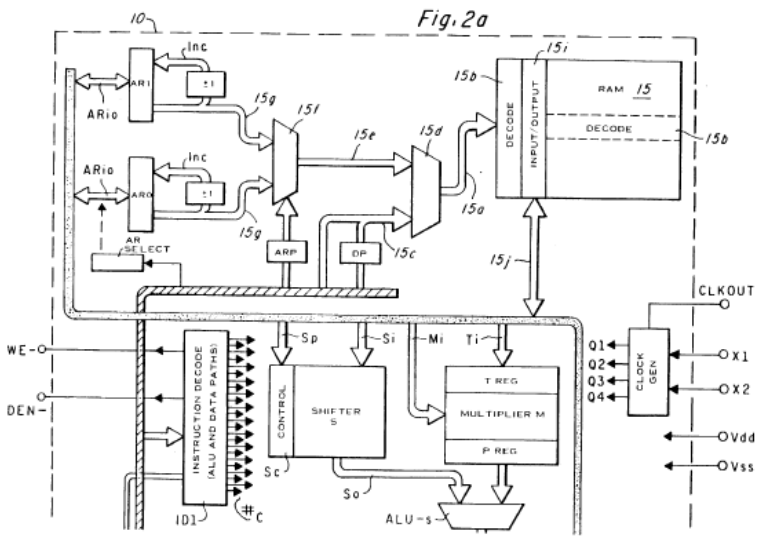
[2] For example, claim 6 recites "thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as *a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate*, thereby enabling said processing frequency to track said clock rate in response to said parameter variation…." Ex. S at 2:23-30.

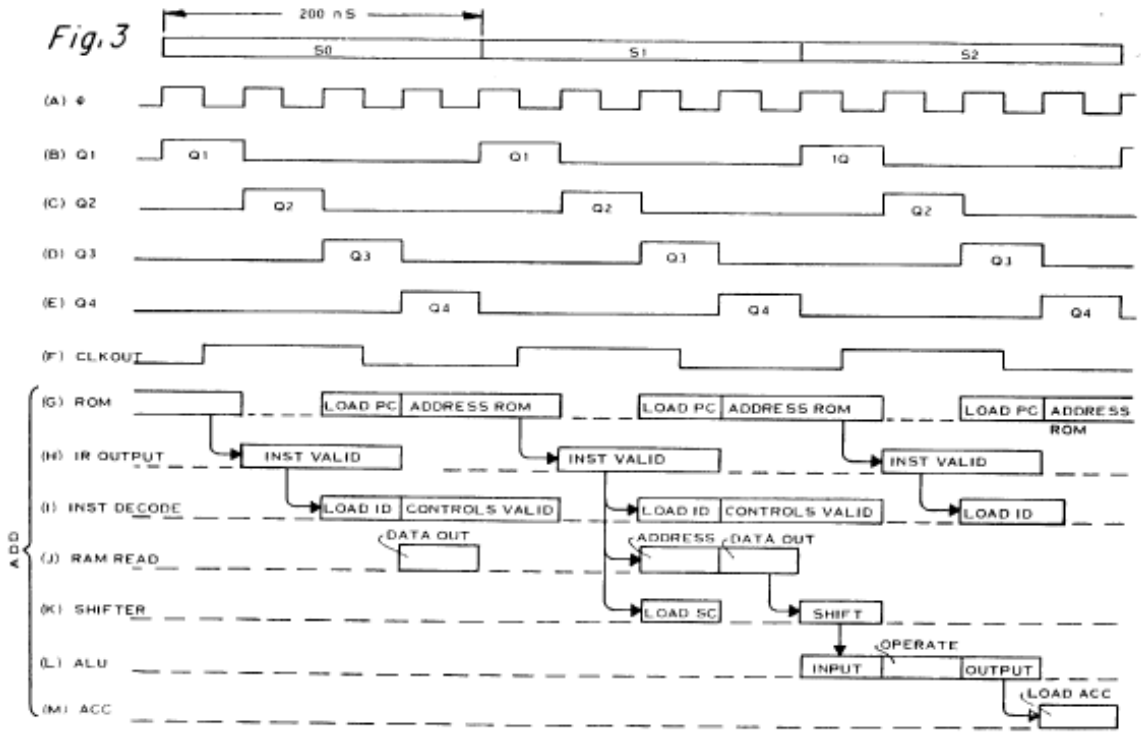
and no disclaimers were made. Without question, applicants never made any statements prohibiting the claimed on-chip oscillator that clocks the CPU from using an off-chip crystal as a reference signal, which is what Defendants seek to exclude by sleight of hand via their overly broad and vague claim construction.

1. U.S. Patent No. 4,503,500 to Magar ("Magar").

In distinguishing the claims at issue from Magar, Defendants allege that applicants disclaimed any use of an "external crystal / clock generator" to (1) "cause clock signal oscillation" or (2) "control clock signal frequency." This position, presented previously to this and other courts, is not supported by the intrinsic record. The record is clear that applicants distinguished Magar on the basis that Magar disclosed an ***external crystal*** used to ***generate*** the clock signal supplied to the CPU. Applicants further distinguished Magar on the basis that Magar's external crystal would not vary according to PVT factors.

Figures 2 and 3 of Magar demonstrate that Magar utilizes an external crystal to generate a 20MHz clock signal. That clock signal, which has a period of 50 nanoseconds, drives the on-chip "CLOCK GEN" circuitry shown below in Figure 2 and diagramed in Figure 3. Bumgardner Decl. Ex. T, U.S. Pat. No. 4,503,500 to Magar at Figs. 2a, 3, 15:23-41.





After receiving the 20MHz signal via pins X1 and X2, the "CLOCK GEN" circuitry in Magar divides the received signal from the crystal oscillator to create four quarter-cycle clocks seen in Q1-Q4. Ex. T at 15:23-35. These four, slower clock signals are each of a period of 200 nanoseconds (a 5MHz clock signal). In Magar, there is no on-chip oscillator that generates these 5MHz clock signals. Rather, the clock signal for the CPU is generated by the off-chip crystal.

In distinguishing their claims from Magar, applicants relied on limitations that are expressly included in the patent claims themselves. Specifically, applicants argued that, unlike their inventions, the oscillator detailed in Magar was not on-chip. Additionally, applicants explained that Magar's off-chip crystal and the speed of Magar's CPU would not vary together according to PVT factors. See Bumgardner Decl. Ex. U, '336 Patent, File History, Response to Office Action at 3-4 (July 7, 1997). As explained in applicants remarks, crystal oscillators do not vary (or vary minimally) due to PVT factors. Notably, both the on-chip/off-chip distinction and the PVT factor variability distinction relied upon by applicants are expressly present in the claims. Neither of these distinctions is directed to the meaning of the "entire oscillator" limitation.

In addition to the passages cited by Defendants – which when read properly show nothing more than applicants' explanation between generating a clock signal by an on-chip, electronic oscillator (as in the '336) and generating a clock signal by an off-chip crystal – applicants provided a clear, contextual meaning for their statements in the following passages:

> In making the rejection based on Magar, the examiner appears to be confusing the multiple uses and meanings of the technical term "clock." A clock is simply an electrical pulse relative to which events take place. **Conventionally, a CPU is driven by a clock that is *generated* by [a] crystal. The crystal might be connected directly to two pins on the CPU, as in Magar,** and be caused to oscillate by circuitry contained in the CPU with the aid of possible other external components . . .
>
> The present invention is unique in that it applies, and can only apply, in the circumstance *wh**ere the oscillator or variable speed clock is fabricated on the same substrate as the driven device*** . . . Thus in this example, the user designs the ring oscillator (clock) to oscillate at a frequency appropriate for the driven device when both the oscillator and the device are under specified fabrication and environmental parameters.

Id. at 4-5 (emphasis added). The critical difference explained by applicants in this passage is that the claimed oscillator used to generate clock signal is fabricated on the same chip as the CPU, and thus subject to the same PVT factors as the CPU. Nowhere in this explanation, or otherwise, do applicants state that the oscillator cannot utilize external reference signals (from fixed frequency sources or otherwise), such as in a PLL where an external crystal is used as a reference for the oscillator contained on the chip. This is consistent with Judge Grewal's previous finding that the prosecution history of the patent did not "impose a prohibition on all types of control." Bumgardner Decl. Ex. D, *HTC Corp. v. Technology Properties Ltd., et al.*, No. 3:08-cv-882, Dkt. No. 509 at 10 (August 21, 2013 - Claim Construction Order) (the "Grewal Markman Order").

After making the aforementioned argument to the examiner, the applicants again faced a rejection in light of Magar. Rather than abandon their previous arguments, applicants amended their claims to expressly require that the entire oscillator is present on the integrated circuit. This amendment clarifies the distinction that applicants were making over Magar, namely that circuitry sufficient to create a clock signal must be found on the same substrate as the CPU, thus making it subject to the same PVT factors of variability (*e.g.*, temperature). In explanation of

their amendment, applicants wrote:

> [T]he independent claims have been rewritten to specify that the ***entire*** ring oscillator variable speed system clock, variable speed clock or oscillator ***be provided in the integrated circuit***, in order to sharpen the distinction over the prior art . . . ***[T]he prior art circuits require an external crystal*** . . .
>
> ***Magar's clock generator relies on an external crystal connected to terminals X1 and X2 to oscillate***, as is conventional in microprocessor designs. It is not an entire oscillator in itself.

Bumgardner Decl. Ex. U, '336 Patent, File History, Response to Office Action at 3 (February 10, 1998).

The applicants correctly observed that Magar "requires" an external crystal to oscillate and generate a clock signal. *Id*. at 4 (Magar "***requires*** an external crystal"; Magar's "clock gen" block "lacks the crystal or external generator that it ***requires***"); *id*. at 5 (Magar "***requires*** an external crystal or external frequency generator"). Notably, applicants pointed out that the oscillator of the claims at issue must be on-chip. Thus, the file history is clear that the applicants made a critical distinction between Magar (and similar references) and the '336 invention: the oscillator that ***generates*** the CPU clock in Magar is an off-chip crystal, while the oscillator that ***generates*** the CPU clock in the '336 invention is an on-chip, electronic oscillator. The file history never discussed – much less disclaimed – the use of PLL circuitry (including an off-chip reference crystal) to adjust the frequency of a clock signal that was already ***generated*** by an on-chip oscillator.

Notably, the distinctions over Magar relied upon by the applicants are found in the claims themselves. Claim 6 expressly requires the "entire oscillator disposed upon said integrated circuit substrate and connected to said [CPU]." The parties' constructions are already in agreement that the "entire oscillator" is "located entirely on the same semiconductor substrate as the [CPU]." And claim 6 already requires PVT variability, reciting "varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated semiconductor substrate…." The point is that the claims themselves already contain the distinctions relied upon by applicants in

distinguishing Magar. There is no factual (or legal) basis for inserting the vague and broad disclaimers advocated by Defendants in the "entire oscillator" construction.

Defendants' citations to the prosecution history distort the statements actually made by applicants with regard to Magar. Regarding the first and second cited passages from the prosecution history (found on pages 8 and 9 of Defendants' Brief[3]), Defendants erroneously claim that "applicants ***expressly and unambiguously disclaimed*** oscillators that rely on an external crystal for ***frequency control.***" Defts' Brief at 9 (emphasis in original). This statement does not comport with what applicants actually said in the passages relied upon by Defendants. In the first passage cited by Defendants, applicants distinguished Magar on the basis that it used an external clock to drive the CPU:

> A review of the Magar reference shows that it is apparently no more pertinent than prior art acknowledged in the application, in that ***the clock disclosed in the Magar reference is in fact driven by a fixed frequency crystal, which is external to the Magar integrated circuit***.

Defts' Brief at 8 (emphasis in Defts' Brief). Nothing in this passage pertains to "frequency control," whatever Defendants' mean by this phrase. The clear distinction made by applicants is Magar's lack of an on-chip oscillator.

In the second passage cited by Defendants, applicants again distinguish Magar on the basis of Magar's use of an off-chip crystal:

> Contrary to the Examiner's assertion in the rejection that 'one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock vary together due to manufacturing variation, operating voltage and temperature of the IC [integrated circuit],' one of ordinary skill in the art should readily recognize that the speed of the CPU and clock ***do not*** vary together due to manufacturing variation, operating voltage, and temperature of the IC in the Magar processor . . . ***This is simply because the Magar microprocessor clock is frequency controlled by a crystal which is also external to the microprocessor***. Crystals are by design fixed frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in

[3] *Technology Properties Ltd. et al. v. Samsung Electronics, et al.*, No.3:12-cv-3877, Dkt. 94 (hereinafter "Defts' Brief).

> manufacturing, operating voltage and temperature. ***The Magar microprocessor in no way contemplates a variable speed clock as claimed***.

Defts' Brief at 8-9 (emphasis in Defts' Brief). The applicants' statement that "the Magar microprocessor clock is frequency controlled by a crystal which is also external to the microprocessor" merely points out that, unlike the claims at issue, the signal used to clock the on-chip CPU in Magar is provided by an external crystal. The portions of applicants' statements highlighted in Defendants' brief are certainly not a clear and unequivocal disclaimer pertaining to any notion of "frequency control" and cannot be extended to support Defendants' construction that the claimed oscillator does "not rely on a ***control signal*** or an external crystal clock to … ***control*** clock signal frequency." In fact, these passages say absolutely nothing about whether an on-chip oscillator (which clocks the on-chip CPU) could rely on an external crystal for "frequency control." There is simply no "unmistakable" disavowal present in these passages.

Defendants next cite to portions of the prosecution history where applicants correctly distinguish their claims from the Magar on the basis that crystals are not subject to PVT factors, such as temperature:

> ***[C]rystal oscillators have never***, to Applicants' knowledge, ***been fabricated on a single silicon substrate with a CPU***, for instance. ***Even if they were***, as previously mentioned, crystals are by design fixed-frequency devices whose oscillation frequency is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. ***The oscillation frequency of a crystal on the same substrate with the microprocessor would inherently not vary due to variations in manufacturing, operating voltage and temperature in the same way as the frequency capability of the microprocessor on the same underlying substrate, as claimed.***

Defts' Brief at 9 (emphasis in Defts' Brief). Defendants disingenuously misconstrue this passage as an "express disclaimer" that "the claims exclude oscillators using crystals to control frequency of the clock signal." *Id.* This alleged sweeping disclaimer is found nowhere in the cited passage. It is simply not there. What is stated in this prosecution history is that a crystal clock's frequency would not vary as a function of PVT like the "microprocessor on the same underlying substrate, ***as claimed***." And as set forth above, what is ***claimed*** is an "entire oscillator" whose frequency varies along with that of the CPU according to PVT factors.

In the next passage of prosecution history cited by Defendants, applicants again distinguish the claims' on-chip electronic oscillator from Magar's use of an external crystal. Defts' Brief at 10. Applicants pointed out that, in their inventions, the signals are subject to variation due to PVT factors while in Magar the signals are "determined by the fixed frequency of the external clock." Nothing in this passage remotely addresses the issue of whether the patent's "entire oscillator" may utilize an external crystal as a reference signal. Nor could this passage legally support a sweeping disclaimer as to "control of the 'frequency or rate' of the clock."

In the final passage of Magar cited by Defendants, applicants again distinguish their invention from Magar on the basis of Magar's use of an external crystal (i.e. lack of an on-chip oscillator), whose frequency is not subject to PVT factors:

> Magar's clock generator ***relies on an external crystal*** connected to terminals X1 and X2 to oscillate, as is conventional in microprocessor designs. It is not an entire oscillator in itself. And with the crystal, ***the clock rate generated is also conventional in that it is a fixed, not a variable, frequency***. The Magar clock is comparable in operation to the conventional crystal clock 434 depicted in Fig. 17 of the present application for controlling the I/O interface ***at a fixed rate frequency, and not at all like the clock on which the claims are based***, as has been previously stated.

Defts' Brief, p. 10 (emphasis in Defendants' Brief). Defendants cite this passage for the alleged disclaimer that the oscillator may not "rely on a control signal or an external crystal/clock generator to ***cause clock signal oscillation***…." But this passage makes no such disclaimer, let alone one that is clear, unambiguous and unmistakable. Applicants are merely pointing out that Magar does not disclose an on-chip oscillator.

It is not entirely clear why Defendants seek to use the language "cause clock signal oscillation," thereby deviating from this Court's jury instruction that the claims exclude "any external clock used to ***generate*** a signal." Plaintiffs strongly suspect that Defendants seek to replace "generate" with "cause clock signal oscillation" in order to lodge a non-infringement argument that goes beyond Judge Grewal's prohibition and has nothing to do with the differences between the claims at issue and Magar. In any event, there is no basis for including a vague and broad disclaimer relating to "causing clock signal oscillation" because the prosecution history

does not clearly and unmistakably include this prohibition. To the extent there is any disclaimer arising from Magar, Judge Grewal's HTC jury instruction (as well as the express claim language itself) accurately addresses the scope of the invention.

2. U.S. Patent No. 4,670,837 to Sheets ("Sheets").

Prior to facing a rejection under Magar, applicants faced a rejection based on Sheets. Like Magar, Sheets differed drastically from the claimed inventions of the '336 patent. Sheets did not contain an on-chip oscillator, and it relied upon a technique for adjusting the frequency of a voltage control oscillator by writing a "digital word" from the microprocessor to the voltage control oscillator indicative of the desired operating frequency as a means of adjusting the clock frequency.

Applicants wrote:

> The present invention does not similarly rely upon provision of frequency control information to an **external clock**, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. . . Sheets' system for providing clock control signals to an **external clock** is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.

Bumgardner Decl. Ex. V, '336 Patent, File History, Office Action Response at 8 (April 11, 1996).

In a subsequent amendment, the applicants noted that the Sheets clock "***required***" a "digital word" or "command input." By contrast, in the '336 inventions, "both the variable speed clock and the microprocessor ***are fabricated together in the same integrated circuit***. No command input is ***necessary*** to change the clock frequency." Bumgardner Decl. Ex. W, ''336 Patent, File History, Office Action Response at 4 (Jan. 7, 1997). Thus, the applicants distinguished Sheets on at least two bases: (1) unlike the '336 invention, Sheets lacked an on-chip clock/oscillator; and (2) the off-chip clock in Sheets ***required*** a "digital word"/"command input" to vary clock frequency (i.e. it did not vary according to PVT factors). These distinctions do not come close to constituting a disclaimer of any "control signal" for any purpose. Indeed, the analog voltage and/or current supplied to a ring oscillator in a PLL is nothing like the "digital

command word" in Sheets. For example, while a ring oscillator may need power to oscillate (*i.e.*, analog voltage/current), it does not have the ability to accept a "digital command word" – nor could it be "***required***" to do so. Further, as discussed above, nothing said in overcoming the Magar reference prevents the use of external reference signals.

The citations Defendants make to the prosecution history once again attempt to remove statements from the context under which they were made. The clear, contextual meaning of applicants' statements is a narrow distinction over the cited reference, not broad disclaimer as alleged by Defendants. In the first passage cited by Defendants, applicants distinguished Sheets on the basis that Sheets discloses an external clock that would not vary according to PVT factors:

> The present invention does not similarly rely upon provision of frequency control information ***to an external clock***, but instead contemplates providing a ring oscillator clock and the microprocessor ***within the same integrated circuit***. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, ***since the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance***. Sheets' system for providing clock control signals to ***an external clock*** is thus seen to be unrelated to the ***integral microprocessor/clock system of the present invention***.

Defts' Brief at 12 (emphasis added by Plaintiffs). Unlike Sheets, the claims at issue contain an on-chip electronic oscillator that naturally varies according to PVT factors. Sheets, on the other hand, apparently varied frequency according to a "digital word"/"command input." Remarkably, Defendants cite the above passage for the proposition that applicants clearly and unmistakably disclaimed all "reliance on control signals." There is no such broad disclaimer present in this passage.

In the second passage cited by Defendants, applicants again distinguished Sheets on the basis that the Sheets clock does not vary according to PVT factors:

> Even if the examiner is correct that the variable clock in Sheets is in the same circuit as the microprocessor of system 100, that still does not give the claimed subject matter. ***In Sheets, a command input is required to change the clock speed. In the present invention, the clock speed varies correspondingly to variations in operating parameters*** . . . No command input is necessary to

> change the clock frequency.

Defts' Brief, pp. 12-13 (emphasis by Plaintiffs). Once again, applicants pointed out that Sheets does not disclose a clock (whether on-chip or off-chip) whose frequency varies according to PVT factors, a requirement of the claim. There is simply no broad disclaimer of all "reliance on control signals" present in this passage.

In the final passage cited by Defendants, applicants again distinguished Sheets on the basis of PVT variation, noting that the on-chip oscillator and on-chip CPU must both vary frequencies according to PVT factors:

> ***Crucial to the present invention is that . . . when fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together***. This differs from all cited references in that . . . the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so.

Defts' Brief at 13 (emphasis by Plaintiffs). Applicants noted that Sheets, on the other hand, required "manual or programmed inputs or external or extra components" to vary its oscillator. In this passage, there is no disclaimer of "reliance on control signals." These words appear nowhere in this passage.

At the end of the day, all of Defendants' accused products contain an on-chip, electronic oscillator that varies according to PVT factors. Defendants improperly seek to exclude the accused oscillators' use of an external crystal as a reference signal by seeking a vague, broad, and improper disclaimer as to "reliance on control signals." As set forth above, applicants' response to Sheets does not make any such disclaimer, as applicants relied on express claim limitations (on-chip vs. off-chip, PVT factor variation) to distinguish the reference. It cannot be disputed that there is no unmistakable disclaimer of the on-chip, electronic oscillator using on an off-chip crystal oscillator as a reference signal in applicants' response to Sheets. Applicants' remarks regarding Sheets contain no such disclaimer.

B. The specification does not support Defendants' disclaimer arguments.

Recognizing the weakness of their prosecution history arguments, Defendants next argue that "the specification disclaims the prior art's fixed-speed clocks (which rely on a crystal, clock,

or signal to control the on-chip oscillator's frequency)…." Defts' Brief, p. 14. Defendants' specification-based disclaimer argument, however, is factually inaccurate and the case law cited by Defendants do not support a finding of disclaimer.

First, Defendants misrepresent the specification by claiming that "the specification criticizes prior art solutions that clocked a CPU with a fixed clock, such as, for example, a clock whose frequency is controlled by an external crystal." *Id.* at 13 (citing '336 patent, 16:48-53 and 17:12-23). This argument is ***highly misleading***, as ***nowhere*** in the passages cited by Defendants does the specification discuss "a clock whose frequency is ***controlled*** by an external crystal." The passages cited by Defendants merely make reference to a "traditional CPU design," which as applicants pointed out in distinguishing Magar involves the use of an off-chip crystal to ***generate*** the actual clock signal for an on-chip CPU. The specification excerpts cited by Defendants do not discuss using an off-chip crystal to ***control*** an on-chip oscillator. Therefore, this passage cannot be read to support the sweeping disclaimer advocated by Defendants. Moreover, the fact that the patent was critical of using an off-chip crystal to generate the actual clock signal for the CPU is of no consequence to this claim construction proceeding as the claims themselves clearly exclude such a scenario from infringement (*i.e.*, the "entire oscillator" must be "located entirely on the same semiconductor substrate as the [CPU]").

Second, Defendants make another misleading statement - "[r]ejecting the prior art fixed-speed clock approach (***which is the approach used in the Defendants' accused products***), the '336 patent discloses a variable-speed oscillator that is completely on the same semiconductor substrate as the CPU and whose speed freely varies with the PVT parameters of the substrate." Defts' Brief at 13-14 (emphasis by Plaintiffs). Contrary to this assertion, Defendants' accused products employ a technique called "dynamic frequency scaling", whereby the frequency of the clock signal generated by an on-chip oscillator and supplied to the CPU is increased during periods of high activity (so that the accused device can quickly respond to user inputs and be perceived as "high performance"), and decreased during periods of low activity (to conserve battery life and reduce power consumption). This oscillator is on the same semiconductor as the CPU and does vary with PVT. What Defendants hope to accomplish is to exclude the oscillators'

use of an external crystal as a reference signal. But, this situation is not addressed by the patent specification, much less disclaimed.

Third, Defendants again overplay their hand by stating that "applicants chose to use a variable speed oscillator – which varies and is 'determined by' PVT parameters – rather than the ***prior art's fixed speed clocks – which did not vary with the PVT parameters because their frequency was 'fixed' by an external crystal or control signal***." *Id.* at 14 (emphasis by Plaintiffs). Again, this statement is misleading as the prior art contemplated by the specification did not involve an on-chip oscillator "whose frequency was 'fixed' by an external crystal or control signal." In the prior art contemplated by the patent, an off-chip crystal oscillator was the oscillator that clocked the CPU. Because using a crystal oscillator to "control" a different, on-chip oscillator was not discussed or contemplated by the specification, there can certainly be no disclaimer of this scenario.

These erroneous statements by Defendants are not sufficient to meet the high bar required to show clear and unmistakable disclaimer, and the cases cited by Defendants involved far different factual scenarios. For example, in *Chicago Bd. Options Exch. Inc. v. Int'l Secs. Exch. LLC*, the court found that the specification "goes well beyond expressing the patentee's preference" and that the patentee's "***repeated derogatory statements*** … may be viewed as a disavowal of that subject matter from the scope of the Patent's claims." 677 F3d 1361, 1372 (Fed. Cir. 2012). By contrast, the '336 patent does not clearly and unambiguously criticize (much less "repeatedly criticize") use of "a control signal or an external crystal/clock generator to cause clock signal oscillation or control clock signal frequency." In fact, this situation is completely unaddressed in the passages cited by Defendants. And while the patent specification does distinguish the invention from prior art systems (like Magar) that used an external crystal to generate the signal used to clock the CPU, this type of system is specifically excluded by virtue of limitations already present in the claims (i.e., the on-chip and PVT variation limitations).

Finally, Defendants claim that the *title* of the patent controls how the Court should interpret the patent. Yet Defendants cite to no law for this proposition. Indeed they cannot – "[i]t is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the

patentee is entitled the right to exclude.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citations omitted). Here, the claims do not state that there can be no use of an external element such as an off-chip crystal as a reference for the clock. The claims only require that an entire oscillator be disposed on the same integrated circuit as the CPU and vary according to PVT factors. This is entirely consistent with the specification passages cited by Defendants, and there is no basis for finding disclaimer going beyond the limitations expressly present in the claims.

C. The Claim Language Speaks for Itself

Defendants next argue that the presence of other elements within the claim should dictate the meaning of the *entire oscillator* term. They argue that if an entire oscillator clocks a CPU at a clock rate which varies in the same way as a function of parameter variation in one or more fabrication or operation parameters associated with the integrated circuit substrate, it cannot use an external crystal or clock generator as a reference, because such reference would not permit the oscillator to vary.

As an initial matter, the argument is technically incorrect. Even if an external crystal is used to later adjust the output of an oscillator, the fact is that the frequency output by the oscillator itself does vary as a function of parameter variation. The addition of other elements, such as an external crystal, to an infringing entire oscillator, does not change the fundamental nature of the oscillator itself.

Further, the claim language speaks for itself. Whether an accused oscillator satisfies the "entire oscillator" element of the claim and also meets other claim limitations (such as the parameter variation requirements) is not an issue for claim construction, but instead a factual argument for trial. Importing the parameter variation requirements into the entire oscillator claim element is unnecessary, renders the parameter variation language redundant, and is not properly handled in the claim construction phase.

D. Defendants' Construction is Not Consistent with Prior Constructions

As explained in Plaintiffs' opening brief, adoption of the negative limitations proposed by Defendants would be a major departure from this Court's prior treatment of the *entire oscillator*

phrase.

In the HTC case, this Court issued a jury instruction that the entire oscillator "exclude any external clock used to generate a signal," but declined to add a restriction with respect to control of the oscillator. The most notable difference between the HTC jury instruction and Defendants' proposed construction is that the HTC jury instruction restricted the entire oscillator from relying on an external crystal/clock generator to ***generate*** the signal used to clock the CPU, whereas Defendants seek to broaden that limitation by virtue of language that the external crystal/clock generator may not ***cause*** clock signal oscillation ***or control clock signal frequency.***

These departures from prior constructions are not trivial. First, Defendants, attempt to broaden the concept of generation to one of causation ("to cause clock signal oscillation"). As explained in their opening brief, Plaintiffs respectfully submit that the concept of "causation" can be viewed as significantly broader and much more uncertain than the concept of "generating" the actual signal used to clock the CPU. As set forth above, the intrinsic record does not support a disclaimer relating to "causation." Indeed, the prosecution history indicates that if there was any disclaimer, it was the use of an external crystal to generate the actual signal used to clock the CPU (a situation that Plaintiffs respectfully submit is already excluded by the claim language). Notably, like the HTC jury instruction, both the Texas construction and the ITC construction also use the term "generate a [clock] signal." Neither construction uses "cause clock signal oscillation."

Additionally, Defendants' proposal that the entire oscillator cannot rely on an external clock to "control clock signal frequency" has been considered and rejected previously by this Court. Applicants did not make any clear and unmistakable disclaimer in this regard, and as such there is simply no basis for including this negative limitation in the entire oscillator construction. Doing so would improperly restrict the scope of the claims. Notably, neither the Texas construction nor the ITC construction includes a broad prohibition relating to "controlling clock signal frequency."

E. Plaintiffs' Construction is Correct

Defendants argue that Plaintiffs' construction cannot be correct because it is too broad and covers prior art systems. They also contend that Plaintiffs surrendered claim scope when distinguishing over Magar and Sheets. These arguments lack merit.

First, Defendants' argument that Plaintiffs' "entire oscillator" construction covers prior art systems that allegedly disclosed an on-chip oscillator. Assuming arguendo that this is true, Defendants' argument obviously ignores the many other claim limitations that must be considered when assessing the scope of the claim. It is simply nonsense to cherry pick the claim term at issue and argue that its construction must be narrower by viewing the claim term in a vacuum and divorced from the claim as a whole. Using Defendants' logic, a construction of CPU would necessarily need to be narrower than what the parties agreed to because there were CPUs disclosed in the prior art. This approach makes little sense.

Second, Defendants' argument that Plaintiffs' construction cannot be correct because "the intrinsic evidence leaves no doubt that the applicants surrendered far more during prosecution to secure allowance of the '336 patent" simply misstates what actually happened during prosecution. As set forth above, Magar and Sheets were distinguished based on the "on-chip" claim requirement and the PVT variation requirement, which are express limitations in the asserted claims.

Finally, it cannot be overlooked that Plaintiffs' construction is included within Defendants' construction. There is no dispute that it is correct. The only question is whether Defendants have met their heavy burden of disclaimer. As set forth above, they have not.

III. CONCLUSION

For the foregoing reasons, Plaintiffs respectfully request that the court adopt their proposed construction.

Dated: August 18, 2015

Respectfully submitted,

/s/ Barry J. Bumgardner

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CERTIFICATE OF SERVICE

I hereby certify that, on August 18, 2015, I caused the foregoing document to be served on counsel of record via the Court's CM/ECF system.

Dated: August 18, 2015

By: */s/ Barry J. Bumgardner*
Barry J. Bumgardner

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

TECHNOLOGY PROPERTIES LIMITED LLC, et al.,

Plaintiffs,

v.

HUAWEI TECHNOLOGIES CO., LTD., HUAWEI DEVICE CO., LTD., HUAWEI DEVICE USA INC., FUTUREWEI TECHNOLOGIES, INC., HUAWEI TECHNOLOGIES USA INC.,

Defendants.

Case No. 3:12-cv-03865-VC (PSG)

DECLARATION OF BARRY J. BUMGARDNER IN SUPPORT OF PLAINTIFFS' RESPONSIVE CLAIM CONSTRUCTION BRIEF

TECHNOLOGY PROPERTIES LIMITED LLC, et al.,

Plaintiffs,

v.

GARMIN LTD., GARMIN INTERNATIONAL, INC., and GARMIN USA, INC.,

Defendants.

Case No. 3:12-cv-03870-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. ZTE CORPORATION and ZTE (USA) INC., Defendants.	Case No. 3:12-cv-03876-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. SAMSUNG ELECTRONICS CO., LTD. and SAMSUNG ELECTRONICS AMERICA, INC., Defendants.	Case No. 3:12-cv-03877-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. LG ELECTRONICS, INC. and LG ELECTRONICS U.S.A., INC., Defendants.	Case No. 3:12-cv-03880-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. NINTENDO CO., LTD. and NINTENDO OF AMERICA, INC., Defendants.	Case No. 3:12-cv-03881-VC (PSG)

I, Barry J. Bumgardner, submit this declaration in support of Plaintiffs' Opening Claim Construction Brief, and declare as follows:

1. I am a partner at the law firm of Nelson Bumgardner, P.C., attorneys of record for Phoenix Digital Solutions LLC ("PDS"). If called as a witness, I could and would testify competently to the information set forth in this declaration.

2. Attached as **Exhibit S** is a true and correct copy of the re-examination certificate of U.S. Pat. No. 5,809,336C1.

3. Attached as **Exhibit T** is a true and correct copy of U.S. Pat. No. 4,503,500 to Magar.

4. Attached as **Exhibit U** is a true and correct copy of an excerpt from the Patent File History of U.S. Pat. No. 5,809,336, specifically the Response to Office Action of July 7, 1997.

5. Attached as **Exhibit V** is a true and correct copy of an excerpt from the Patent File History of U.S. Pat. No. 5,809,336, specifically the Response to Office Action of April 15, 1996.

6. Attached as **Exhibit W** is a true and correct copy of an excerpt from the Patent File History of U.S. Pat. No. 5,809,336, specifically the Response to Office Action of January 8, 1997.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. This declaration is executed on August 18, 2015 in Fort Worth, Texas.

Dated: August 18, 2015

By: /s/ *Barry J. Bumgardner*
Barry J. Bumgardner

Exhibit “S”

US005809336C1

(12) EX PARTE REEXAMINATION CERTIFICATE (7235th)

United States Patent

Moore et al.

(10) Number: US 5,809,336 C1
(45) Certificate Issued: Dec. 15, 2009

(54) **HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK**

(75) Inventors: **Charles H. Moore**, Woodside, CA (US); **Russell H. Fish, III**, Mt. View, CA (US)

(73) Assignee: **Patriot Scientific Corporation**, San Diego, CA (US)

Reexamination Request:
No. 90/008,306, Oct. 19, 2006
No. 90/008,237, Nov. 17, 2006
No. 90/008,474, Jan. 30, 2007

Reexamination Certificate for:
Patent No.: **5,809,336**
Issued: **Sep. 15, 1998**
Appl. No.: **08/484,918**
Filed: **Jun. 7, 1995**

Certificate of Correction issued May 22, 2007.

Related U.S. Application Data

(62) Division of application No. 07/389,334, filed on Aug. 3, 1989, now Pat. No. 5,440,749.

(51) **Int. Cl.**

G06F 7/76	(2006.01)
G06F 7/48	(2006.01)
G06F 12/08	(2006.01)
G06F 7/78	(2006.01)
G06F 9/30	(2006.01)
G06F 9/32	(2006.01)
G06F 15/76	(2006.01)
G06F 15/78	(2006.01)
G06F 7/52	(2006.01)
G06F 9/38	(2006.01)
G06F 7/58	(2006.01)

(52) **U.S. Cl.** **710/25**; 711/E12.02; 712/E9.016; 712/E9.028; 712/E9.046; 712/E9.055; 712/E9.057; 712/E9.058; 712/E9.062; 712/E9.078; 712/E9.08; 712/E9.081

(58) **Field of Classification Search** ..... None
See application file for complete search history.

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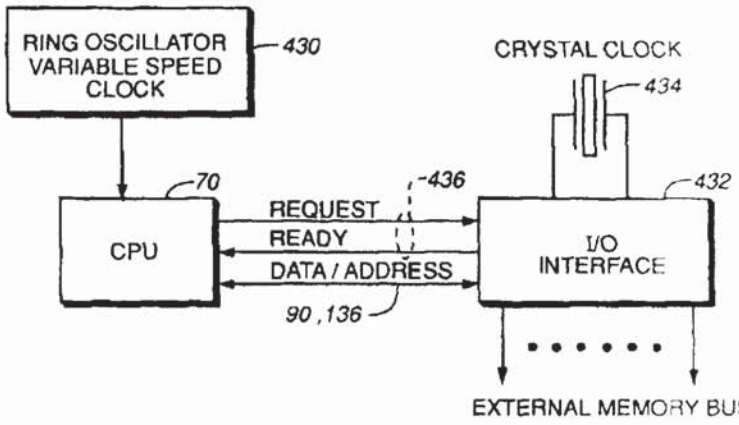
Plaintiffs Technology Property Limited's and Patriot Scientific Corporation's Claim Construction Brief filed Mar. 19, 2007 in 2:05–CV–494 (TJW).

(Continued)

Primary Examiner—Sam Rimell

(57) **ABSTRACT**

A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.



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EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

ONLY THOSE PARAGRAPHS OF THE SPECIFICATION AFFECTED BY AMENDMENT ARE PRINTED HEREIN.

Column 17, lines 12–37:

Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor **50** provides a dual-clock scheme as shown in FIG. **17**, with the CPU **70** operating **[**a synchronously**]** *asynchronously* to I/O interface **432** forming part of memory controller **118** (FIG. **2**) and the I/O interface **432** operating synchronously with the external world of memory and I/O devices. The CPU **70** executes at the fastest speed possible using the adaptive ring counter clock **430**. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor **50** for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface **432**, speed of which is controlled by a conventional crystal clock **434**. The interface **432** processes requests for memory accesses from the microprocessor **50** and acknowledges the presence of I/O data. The microprocessor **50** fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. By decoupling the variable speed of the CPU **70** from the fixed speed of the I/O interface **432**, optimum performance can be achieved by each. Recoupling between the CPU **70** and the interface **432** is accomplished with handshake signals on lines **436**, with data/addresses passing on bus **90**, **136**.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

Claims **3**–**5** and **8** are cancelled.

Claims **1**, **6** and **10** are determined to be patentable as amended.

Claims **2**, **7** and **9**, dependent on an amended claim, are determined to be patentable.

New claims **11**–**16** are added and determined to be patentable.

1. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, *wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.*

6. A microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an *off-chip* external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an *off-chip* external clock, independent of said oscillator, connected to said input/output interface wherein said *off-chip* external clock is operative at a frequency independent of a clock frequency of said oscillator *and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.*

10. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an **[**on chip**]** *on-chip* input/output interface between said central processing unit and an *off-chip* external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an *off-chip* external clock wherein said *off-chip* external clock is operative at a frequency independent of a clock frequency of said variable speed clock *and wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock.*

11. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein said central processing unit operates asynchronously to said input/output interface.

12. The microprocessor system of claim 11, in which said second clock is a fixed frequency clock.

13. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;

an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and further wherein said central processing unit operates asynchronously to said input/output interface.

14. The microprocessor system of claim 13 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

15. The microprocessor system of claim 13 wherein said oscillator comprises a ring oscillator.

16. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock, wherein said central processing unit operates asychronously to said input/output interface.

* * * * *

Exhibit “T”

United States Patent [19]

Magar

[11] **Patent Number: 4,503,500**

[45] **Date of Patent: Mar. 5, 1985**

[54] **MICROCOMPUTER WITH BUS INTERCHANGE MODULE**

[75] Inventor: **Surendar S. Magar**, Houston, Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **619,650**

[22] Filed: **Jun. 15, 1984**

Related U.S. Application Data

[63] Continuation of Ser. No. 347,860, Feb. 11, 1982.

[51] **Int. Cl.**³ **G06F 3/00**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** 364/200, 900

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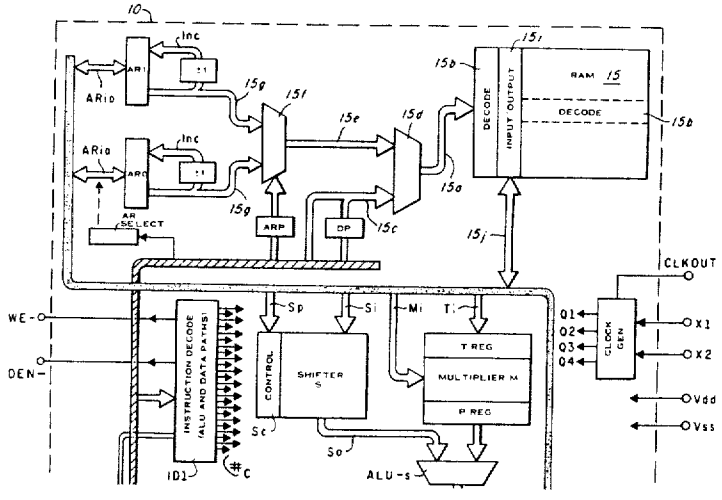
Primary Examiner—Gareth D. Shaw
Assistant Examiner—Ronni S. Malamud
Attorney, Agent, or Firm—John G. Graham

[57] **ABSTRACT**

A system for real-time digital signal processing employs a single-chip microcomputer device having separate on-chip program ROM and data RAM, with separate address and data paths for program and data. An external program address bus allows off-chip program fetch in an expansion mode, with the opcode returned by an external data bus. A bus interchange module allows transfer between the separate internal program and data busses in special circumstances. The internal busses are 16-bit, while the ALU and accumulator are 32-bit. A multiplier circuit produces a single state 16×16 multiply function separate from the ALU, with 32-bit output to the ALU. One input to the ALU passes through a 0-to-15 bit shifter with sign extension.

9 Claims, 15 Drawing Figures



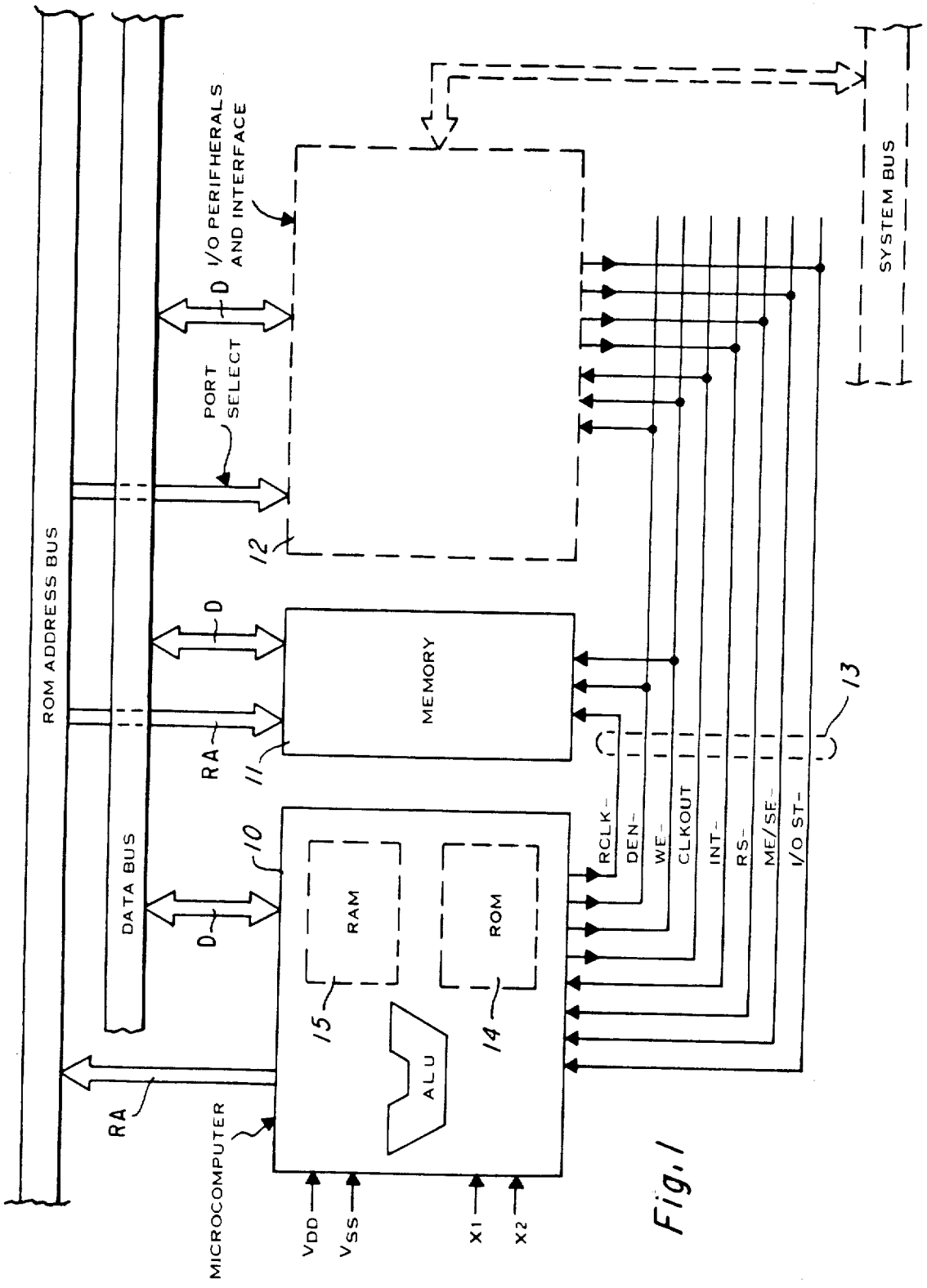

ROM ADDRESS BUS
DATA BUS
I/O PERIFHERALS AND INTERFACE
PORT SELECT
SYSTEM BUS
MEMORY
RA
D
RAM
ROM
ALU
MICROCOMPUTER
RCLK-
DEN-
WE-
CLKOUT
INT-
RS-
ME/SE-
I/O ST-
VDD
VSS
X1
X2
12
11
10
15
14
13

Fig. 1

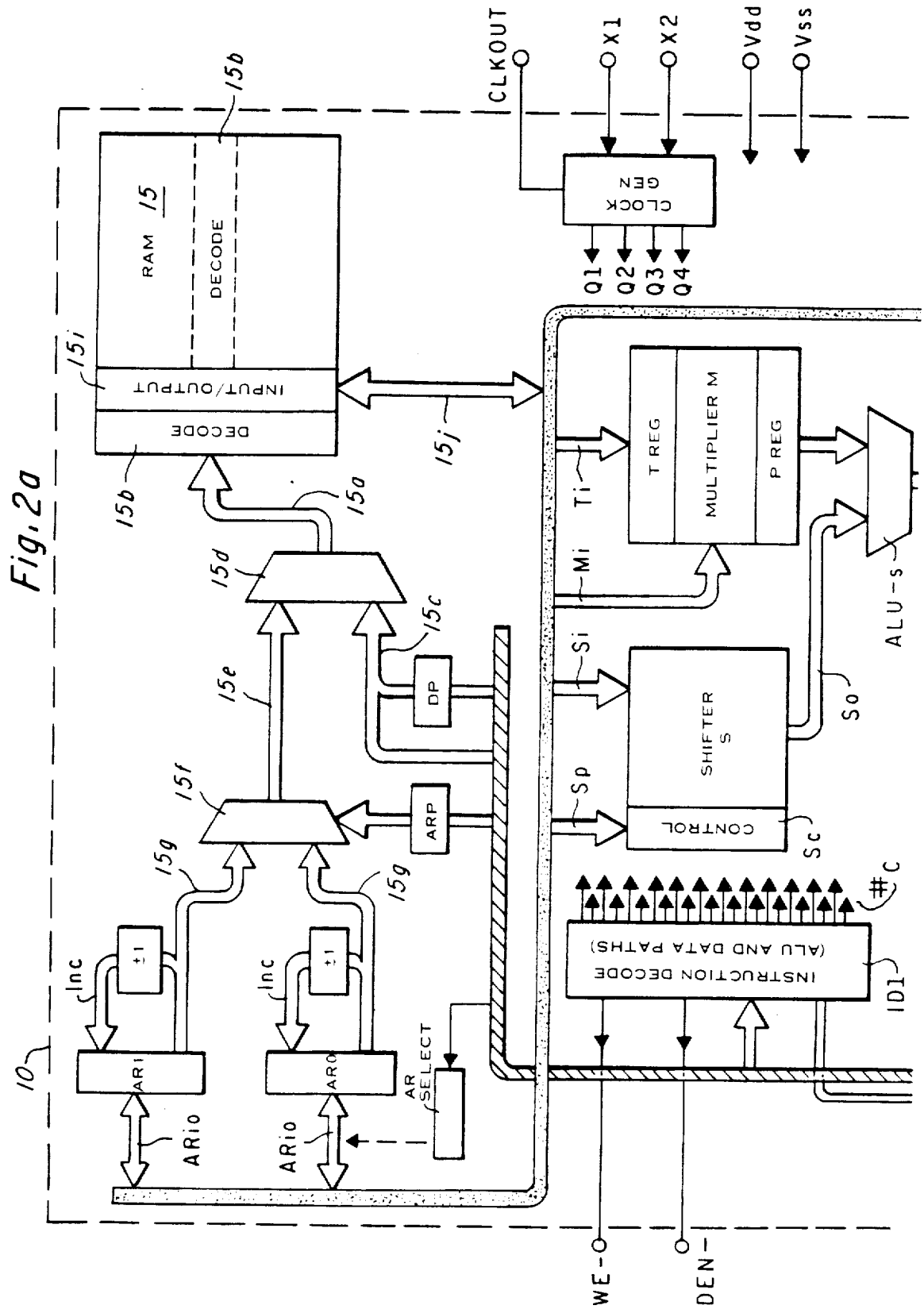


Fig. 2a
CLKOUT
X1
X2
Vdd
Vss
CLOCK GEN
Q1
Q2
Q3
Q4
15b
RAM 15
DECODE
15i
INPUT/OUTPUT
DECODE
15b
15a
15j
T REG
MULTIPLIER M
P REG
Ti
Mi
ALU-s
15d
15c
15e
DP
Si
SHIFTER S
So
15f
ARP
Sp
CONTROL
Sc
15g
15g
#c
INSTRUCTION DECODE (ALU AND DATA PATHS)
ID1
Inc
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AR1
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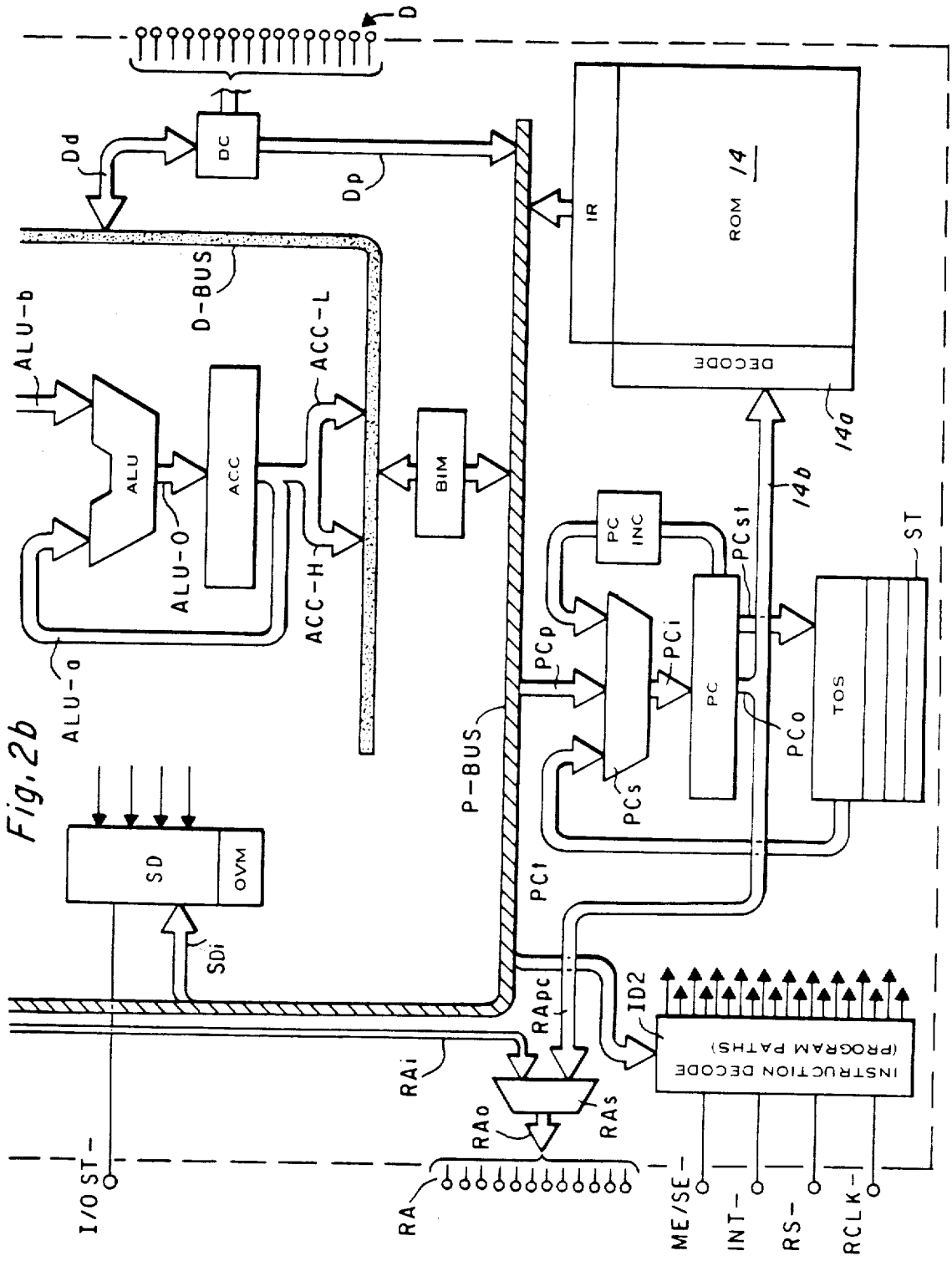

D
Dd
DC
Dp
D-BUS
ALU-b
ALU
ACC
ACC-L
ACC-H
ALU-o
ALU-O
BIM
IR
ROM 14
DECODE
14a
14b
PC INC
PCst
ST
PCp
PCi
PC
PCo
TOS
PCs
P-BUS
PC1
SD
OVM
SDi
RApc
ID2
INSTRUCTION DECODE
(PROGRAM PATHS)
RAi
RAo
RAs
I/O ST-
RA
ME/SE-
INT-
RS-
RCLK-

Fig. 2b

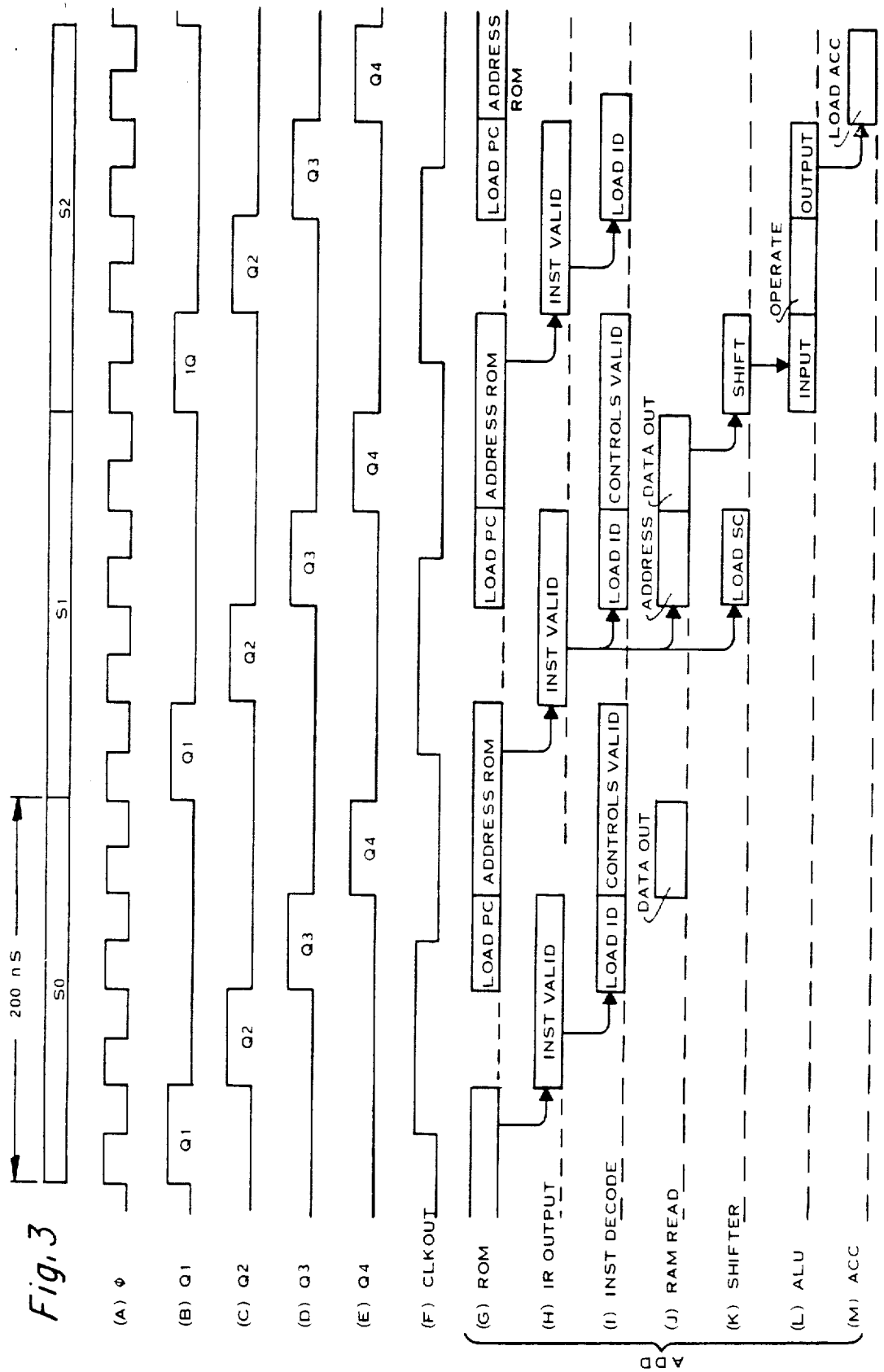

200 nS
S0
S1
S2
(A) Φ
(B) Q1
(C) Q2
(D) Q3
(E) Q4
(F) CLKOUT
(G) ROM
(H) IR OUTPUT
(I) INST DECODE
(J) RAM READ
(K) SHIFTER
(L) ALU
(M) ACC
LOAD PC
ADDRESS ROM
INST VALID
LOAD ID
CONTROLS VALID
DATA OUT
LOAD SC
SHIFT
OPERATE
INPUT
OUTPUT
LOAD ACC

Fig. 3

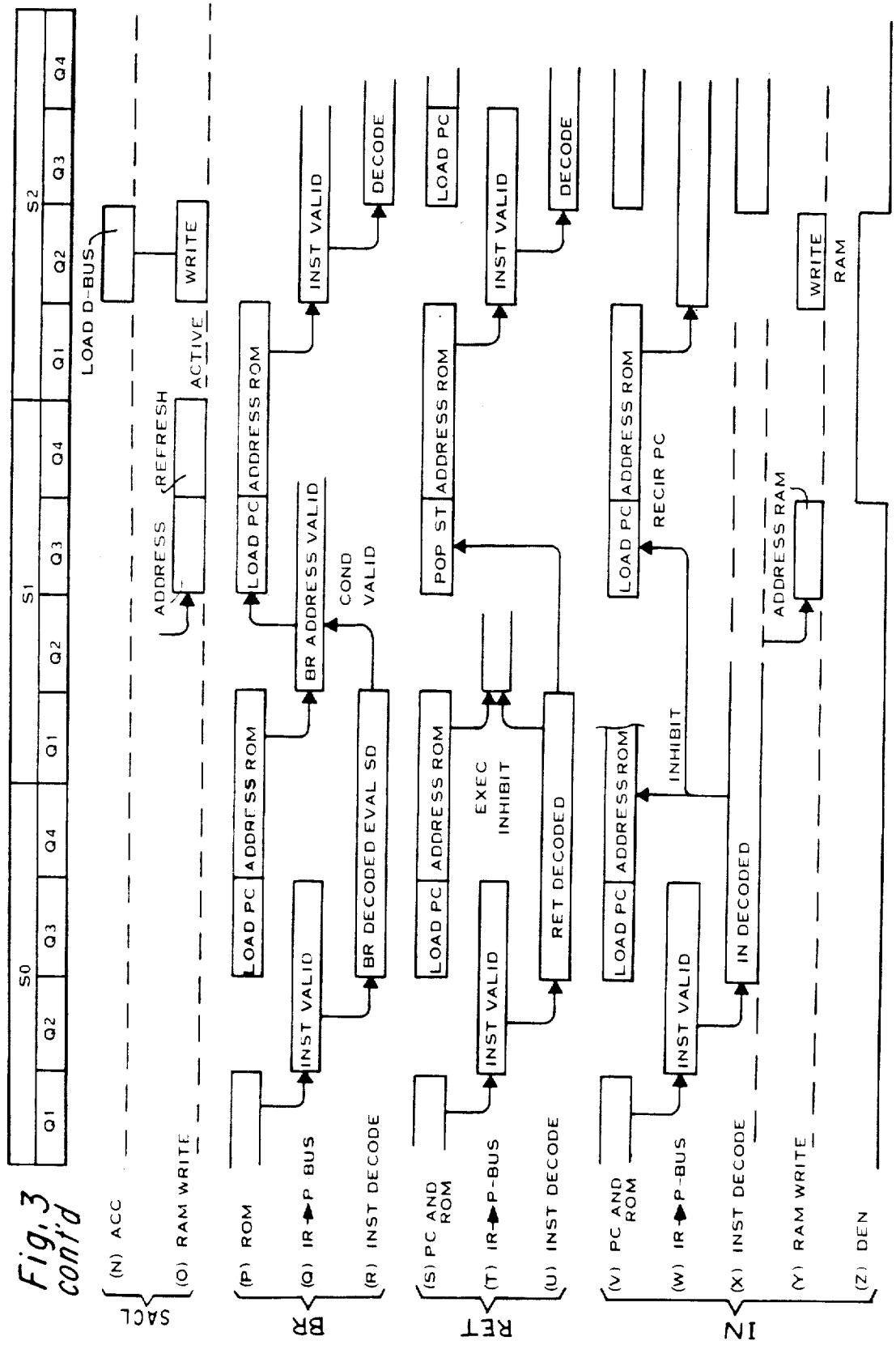

S0
S1
S2
Q1
Q2
Q3
Q4
(N) ACC
(O) RAM WRITE
ADDRESS
REFRESH
ACTIVE
LOAD D-BUS
WRITE
SACL
(P) ROM
(Q) IR→P BUS
(R) INST DECODE
LOAD PC
ADDRESS ROM
INST VALID
BR DECODED EVAL SD
BR ADDRESS VALID
COND VALID
DECODE
BR
(S) PC AND ROM
(T) IR→P-BUS
(U) INST DECODE
EXEC INHIBIT
RET DECODED
POP ST
LOAD PC
RET
(V) PC AND ROM
(W) IR→P-BUS
(X) INST DECODE
(Y) RAM WRITE
(Z) DEN
INHIBIT
RECIR PC
IN DECODED
ADDRESS RAM
WRITE RAM
IN

Fig. 3 cont'd

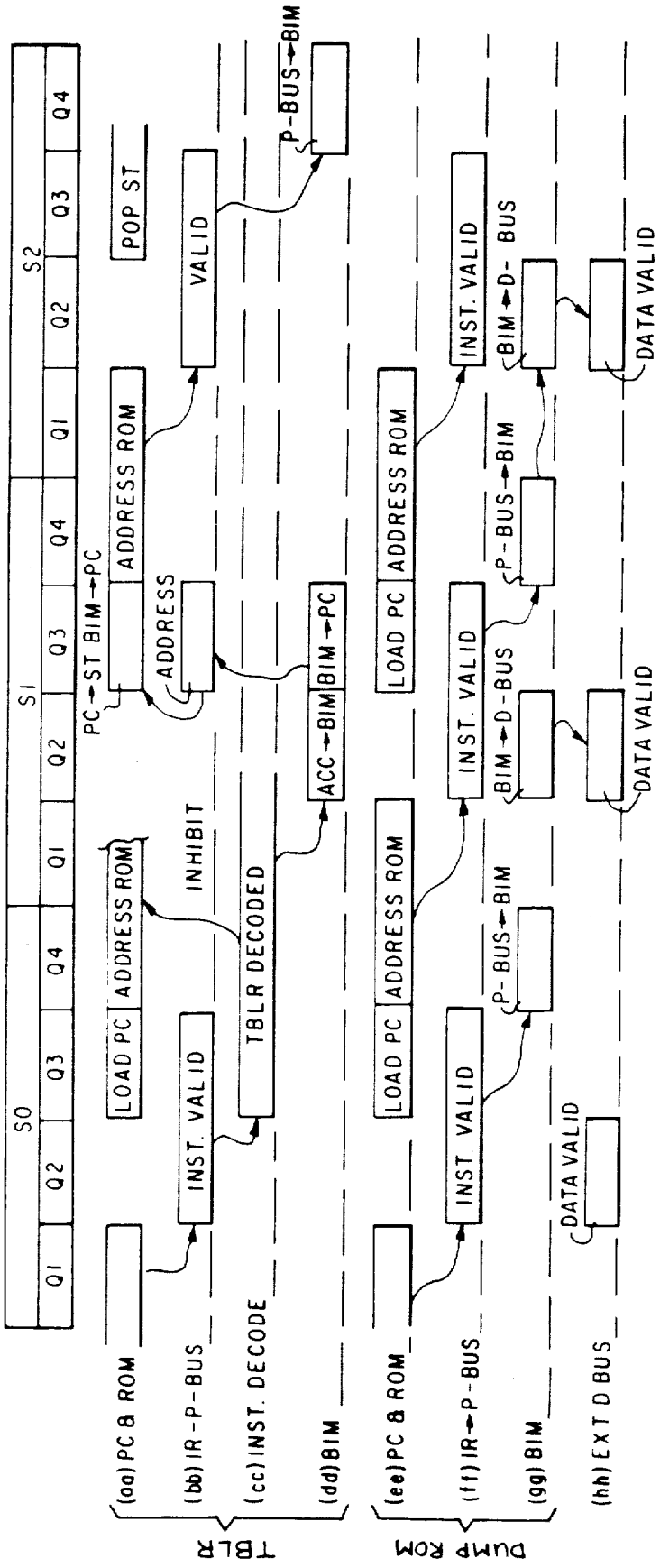

S0
S1
S2
Q1
Q2
Q3
Q4
(aa) PC & ROM
(bb) IR-P-BUS
(cc) INST. DECODE
(dd) BIM
TBLR
LOAD PC
ADDRESS ROM
INST. VALID
TBLR DECODED
INHIBIT
PC→ST BIM→PC
ADDRESS
VALID
POP ST
ACC→BIM BIM→PC
P-BUS→BIM
(ee) PC & ROM
(ff) IR→P-BUS
(gg) BIM
(hh) EXT D BUS
DUMP ROM
BIM→D-BUS
P-BUS→BIM
DATA VALID
BIM→D- BUS

Fig. 3 (cont'd)

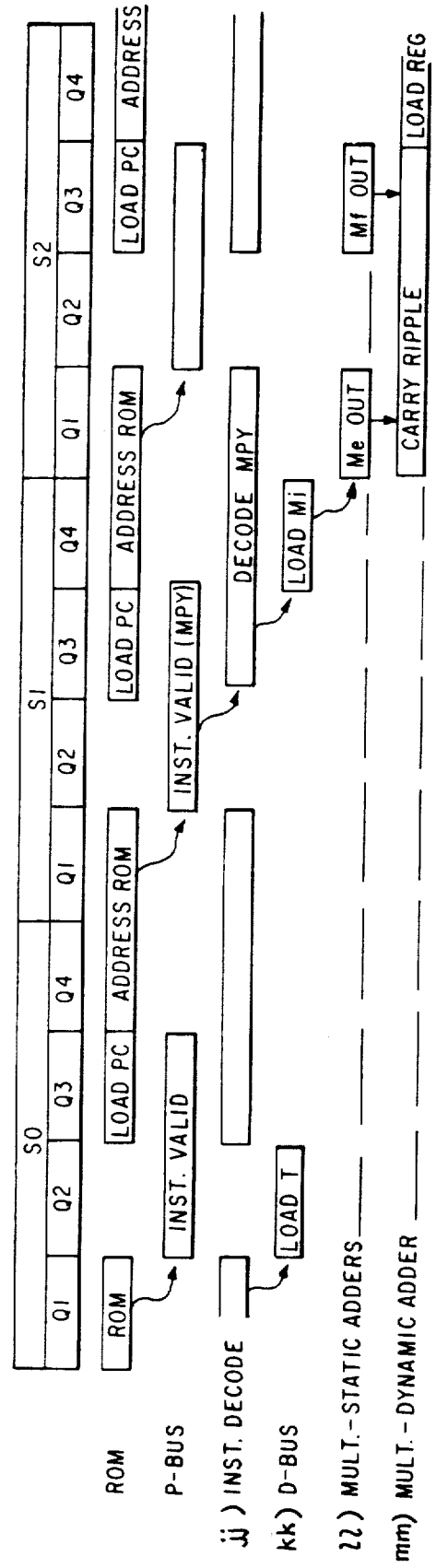


Fig. 3(cont'd) MULTIPLY INSTRUCTION

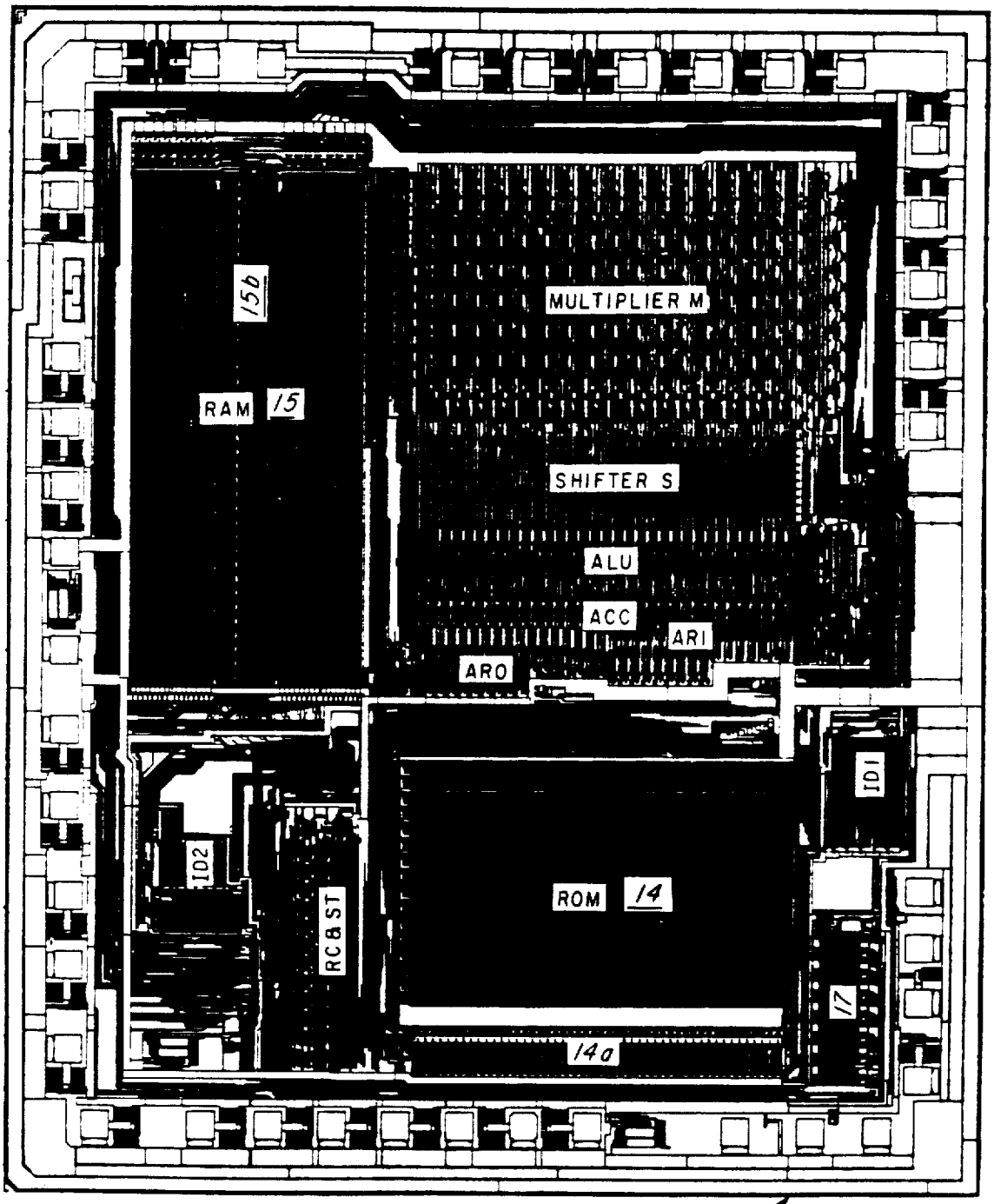

15b
MULTIPLIER M
RAM 15
SHIFTER S
ALU
ACC
ARI
ARO
ID1
ID2
RC & ST
ROM 14
17
14a

Fig. 4

10

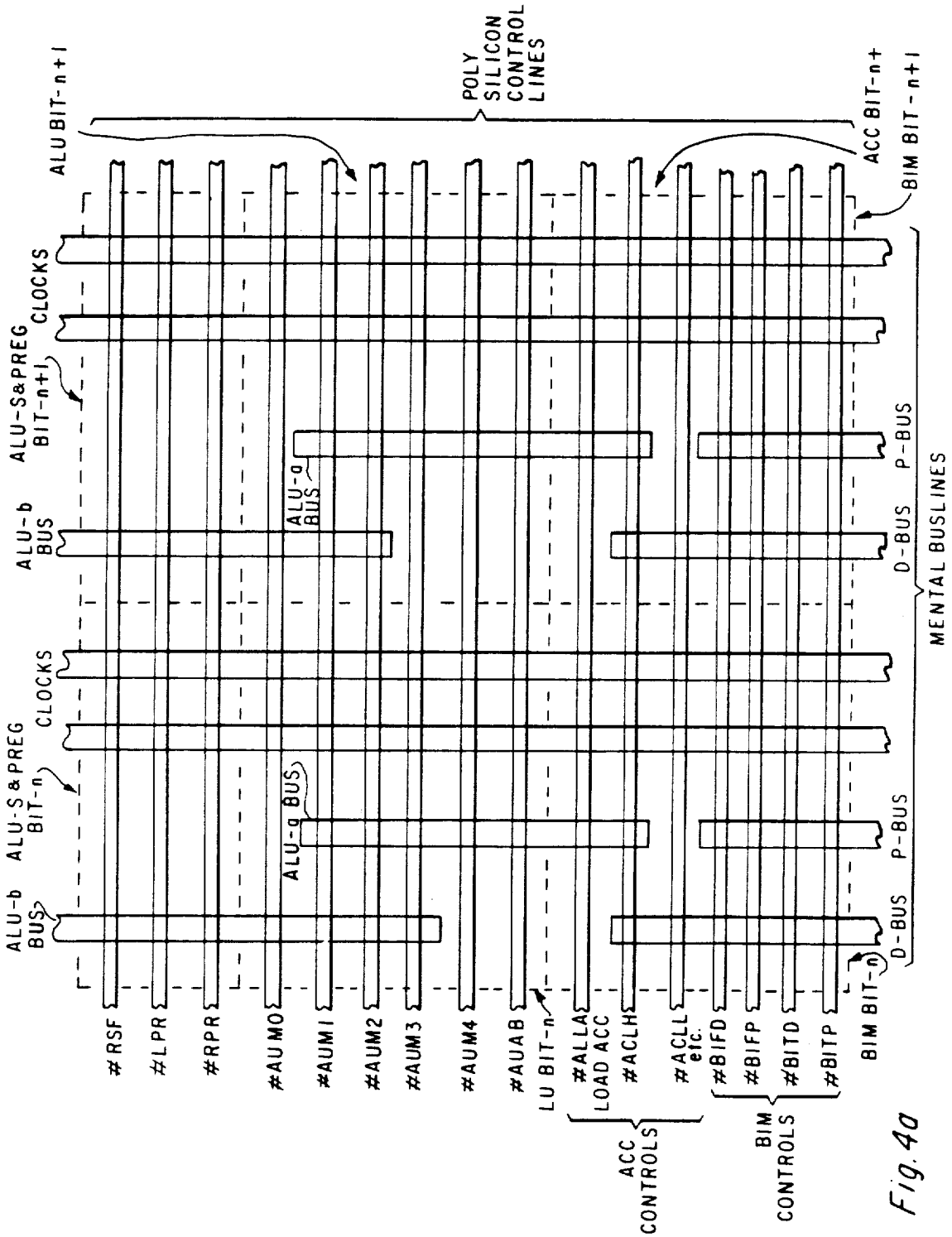

ALU BIT-n+1
POLY SILICON CONTROL LINES
ACC BIT-n+
BIM BIT-n+1
ALU-S&PREG CLOCKS
ALU-S&PREG BIT-n+1
ALU-b BUS
ALU-a BUS
D-BUS P-BUS
METAL BUSLINES
ALU-S&PREG CLOCKS
ALU-S&PREG BIT-n
ALU-b BUS
ALU-a BUS
D-BUS P-BUS
#RSF
#LPR
#RPR
#AUMO
#AUM1
#AUM2
#AUM3
#AUM4
#AUAB
LU BIT-n
#ALLA LOAD ACC
#ACLH
#ACLL etc.
ACC CONTROLS
#BIFD
#BIFP
#BITD
#BITP
BIM CONTROLS
BIM BIT-n

Fig. 4a

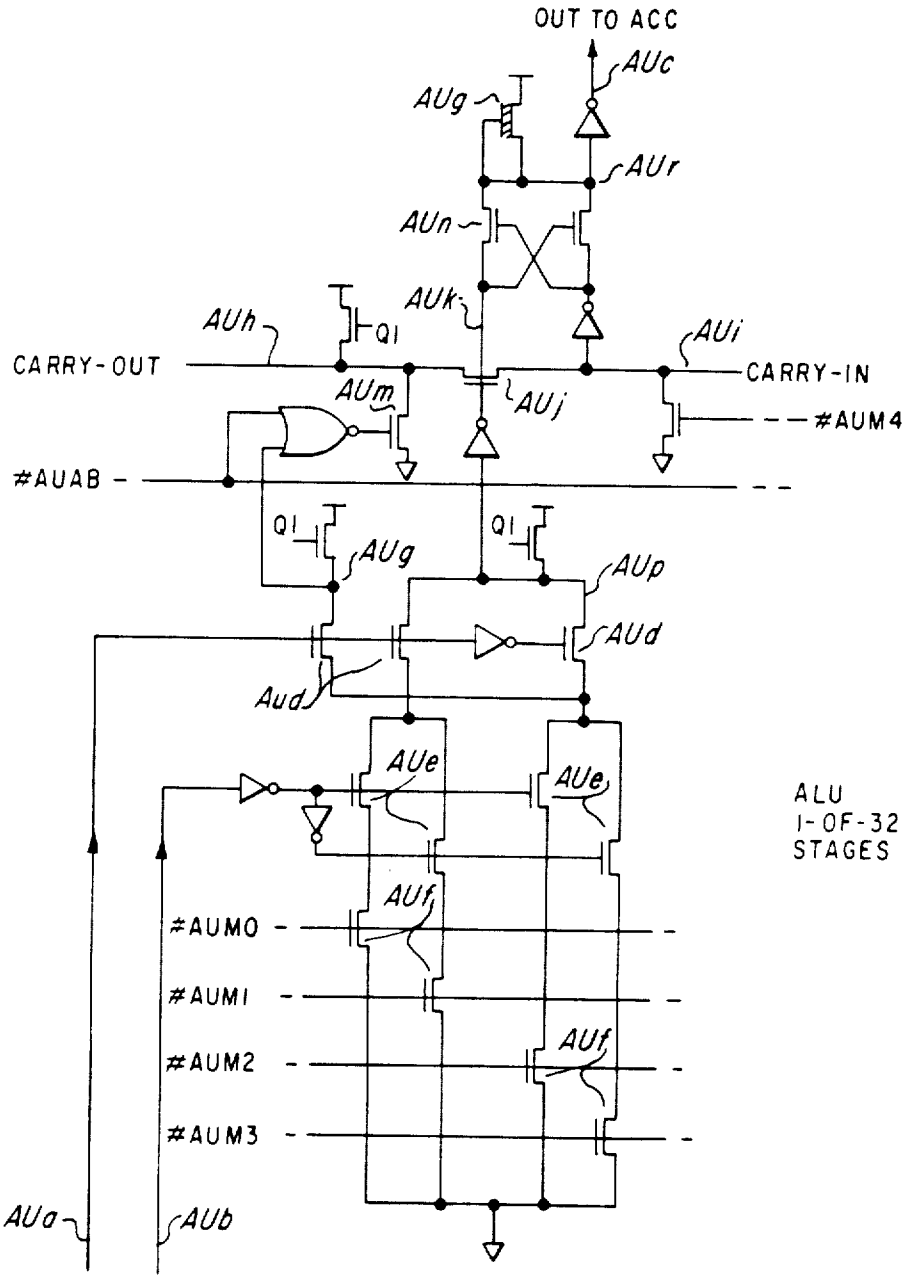

OUT TO ACC
AUc
AUg
AUr
AUn
AUk
AUh
Q1
AUi
CARRY-OUT
AUm
AUj
CARRY-IN
#AUM4
#AUAB
Q1
Q1
AUg
AUp
AUd
Aud
AUe
AUe
ALU
1-OF-32
STAGES
AUf
#AUM0
#AUM1
AUf
#AUM2
#AUM3
AUa
AUb

Fig. 5a

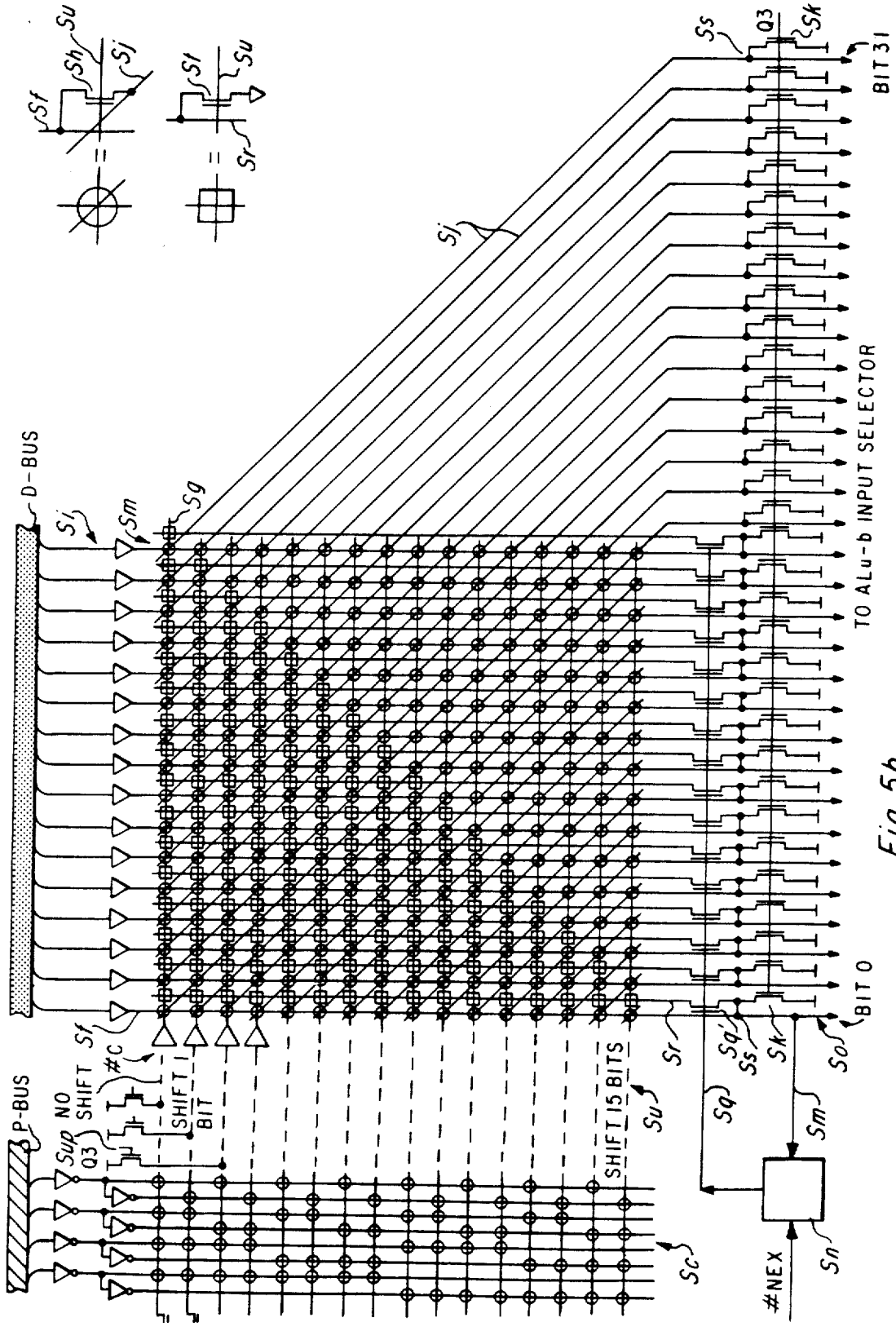
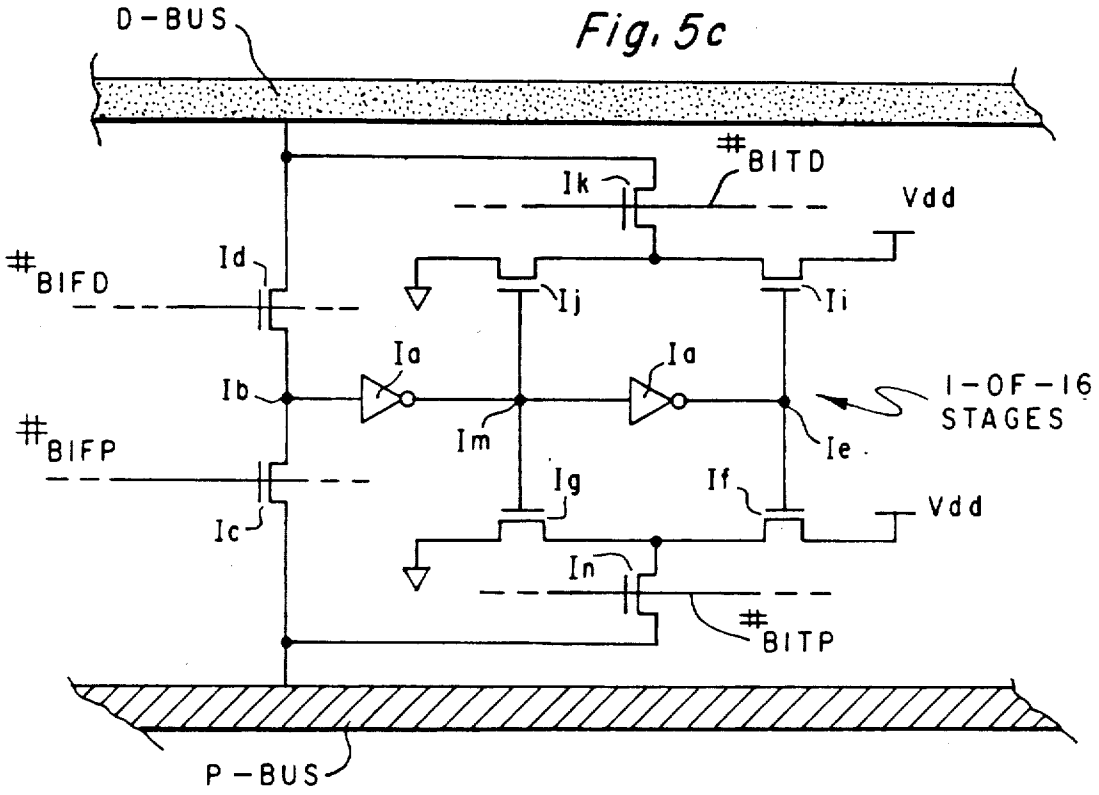

D-BUS
P-BUS
NO SHIFT
SHIFT 1 BIT
SHIFT 15 BITS
TO ALu-b INPUT SELECTOR
BIT 31
BIT 0
#NEX
Q3

Fig. 5b

Fig. 5c


D-BUS
#BITD
Ik
Vdd
#BIFD
Id
Ij
Ii
Ia
Ia
Ib
I-OF-16
STAGES
#BIFP
Im
Ie
Ig
If
Vdd
Ic
In
#BITP
P-BUS

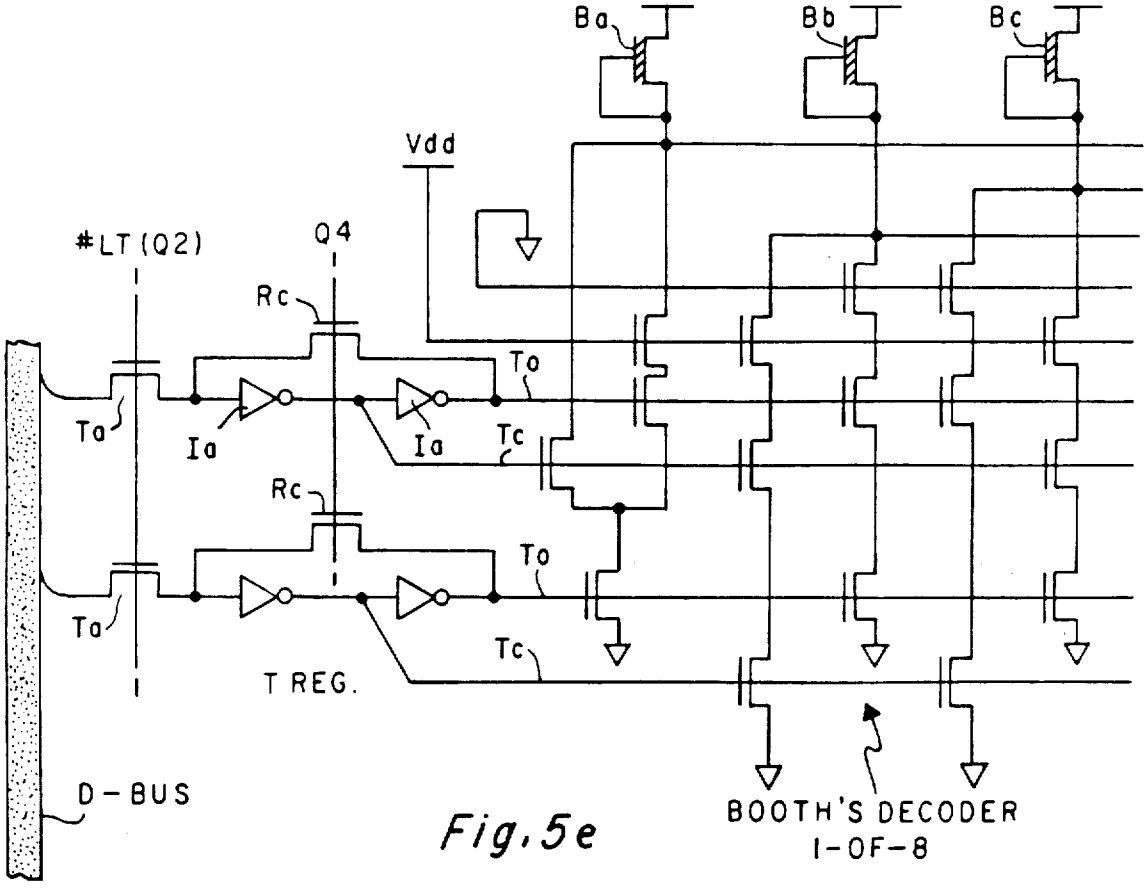

Ba
Bb
Bc
Vdd
#LT(Q2)
Q4
Rc
To
Ta
Ia
Ia
Tc
Rc
To
Ta
Tc
T REG.
D-BUS
BOOTH'S DECODER
1-OF-8

Fig. 5e

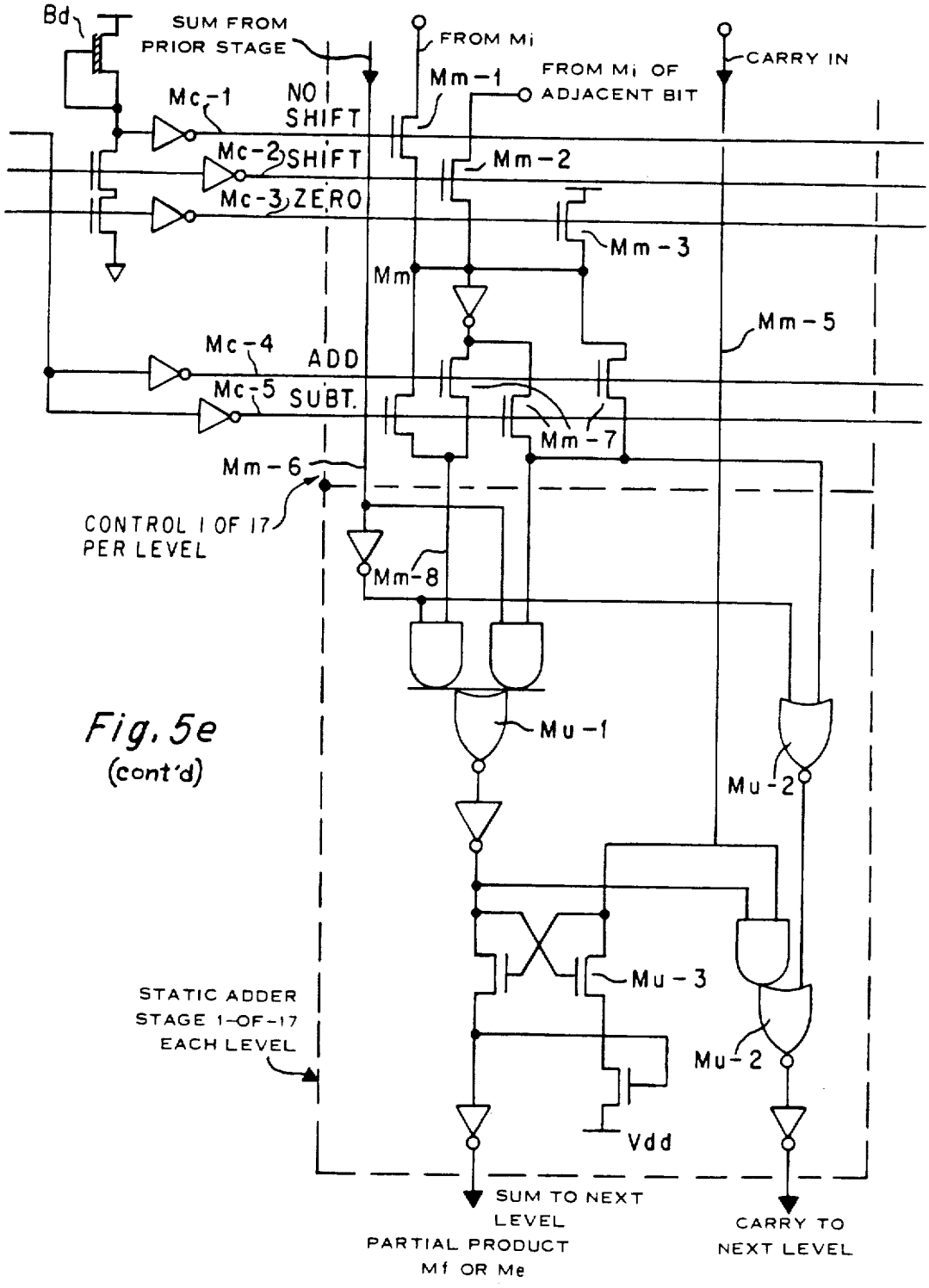

Bd
SUM FROM PRIOR STAGE
FROM Mi
FROM Mi OF ADJACENT BIT
CARRY IN
Mm-1
Mc-1
NO SHIFT
Mc-2 SHIFT
Mc-3 ZERO
Mm-2
Mm-3
Mm
Mm-5
Mc-4
ADD
Mc-5 SUBT.
Mm-7
Mm-6
CONTROL 1 OF 17 PER LEVEL
Mm-8
Mu-1
Mu-2
Mu-3
Mu-2
STATIC ADDER STAGE 1-OF-17 EACH LEVEL
Vdd
SUM TO NEXT LEVEL PARTIAL PRODUCT Mf OR Me
CARRY TO NEXT LEVEL

Fig. 5e (cont'd)

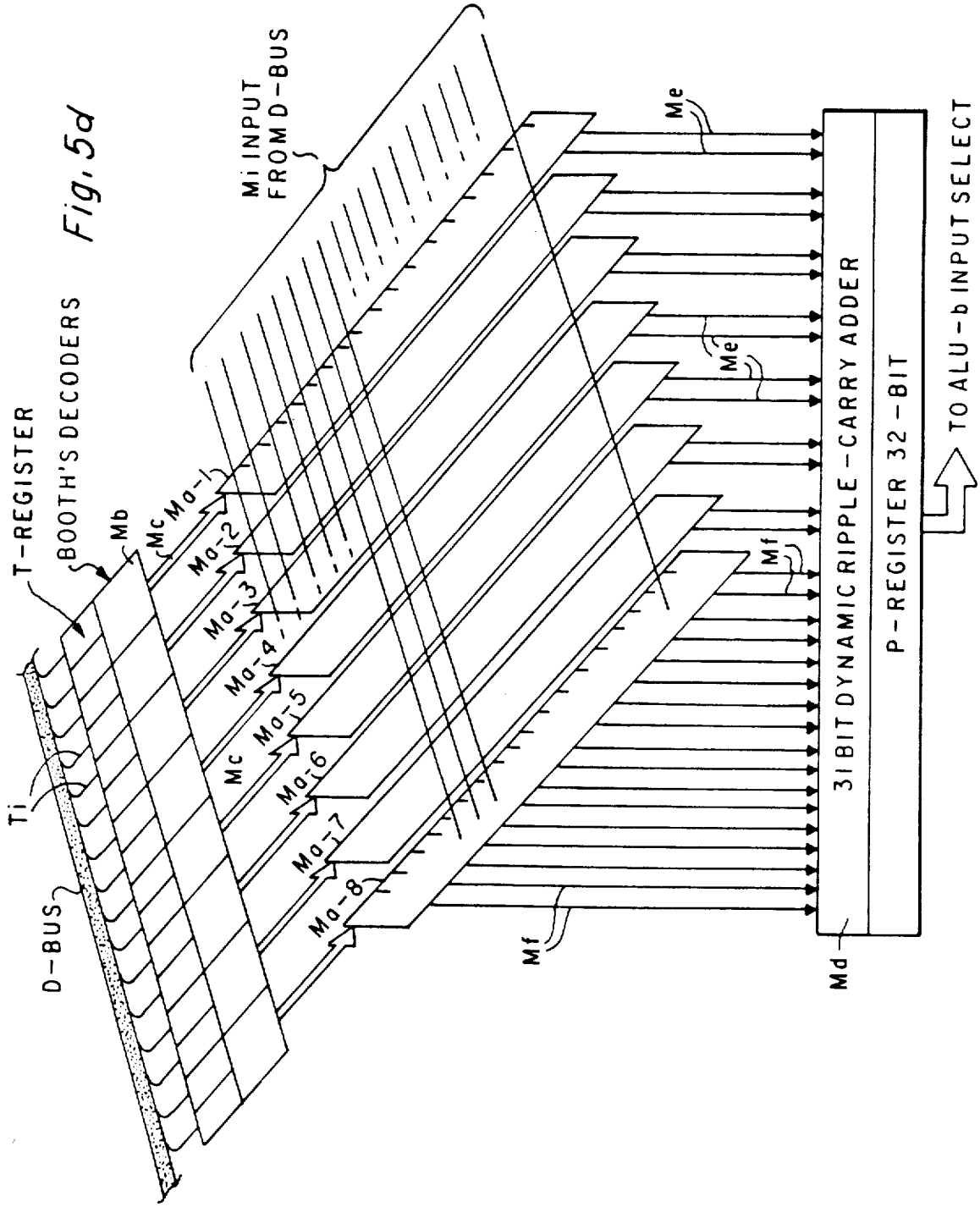

Mi INPUT FROM D-BUS
Me
Me
Mf
Mf
Md
T-REGISTER
BOOTH'S DECODERS
Mb
Mc
Mo-1
Mo-2
Mo-3
Mo-4
Mo-5
Mo-6
Mo-7
Mo-8
Mc
Ti
D-BUS
31 BIT DYNAMIC RIPPLE-CARRY ADDER
P-REGISTER 32-BIT
TO ALU-b INPUT SELECT

Fig. 5d

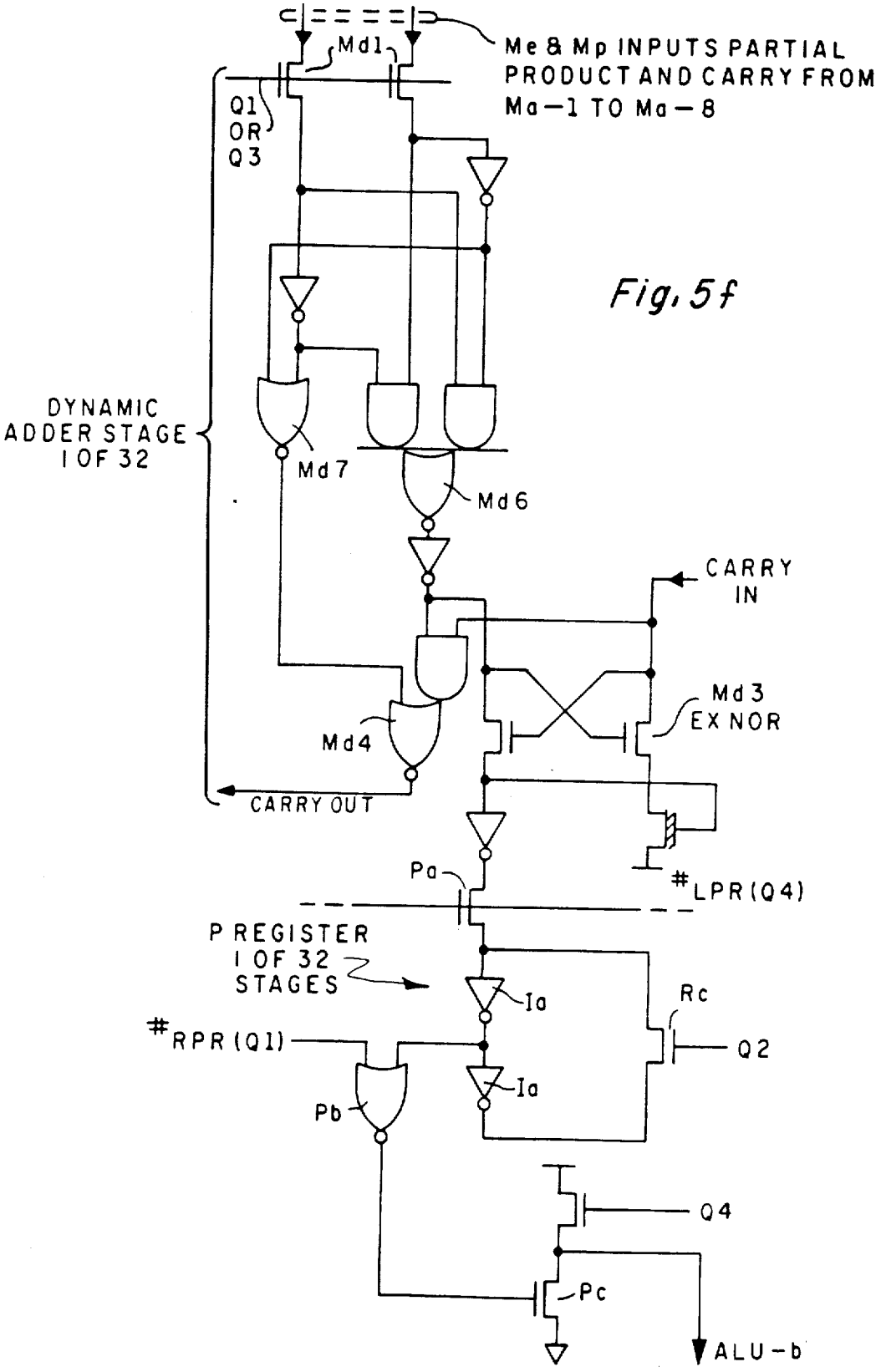

Me & Mp INPUTS PARTIAL PRODUCT AND CARRY FROM Ma−1 TO Ma−8
Md1
Q1 OR Q3
DYNAMIC ADDER STAGE 1 OF 32
Md7
Md6
CARRY IN
Md3 EX NOR
Md4
CARRY OUT
Pa
#LPR(Q4)
P REGISTER 1 OF 32 STAGES
Ia
Rc
#RPR(Q1)
Q2
Ia
Pb
Q4
Pc
ALU−b

Fig. 5f

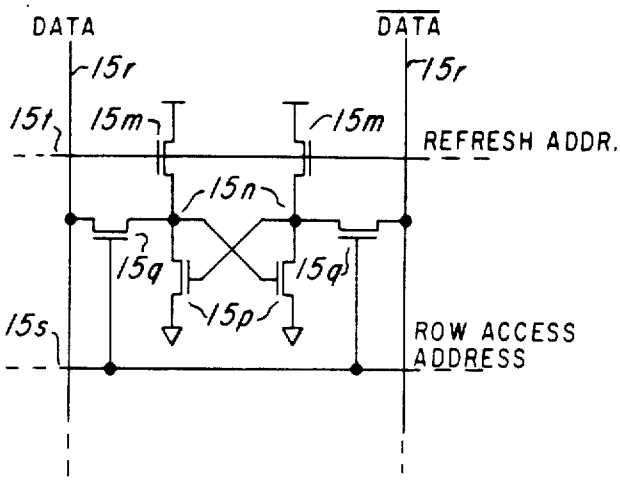

DATA
DATA
15r
15r
15t
15m
15m
REFRESH ADDR.
15n
15q
15q
15p
15s
ROW ACCESS ADDRESS

Fig. 5g

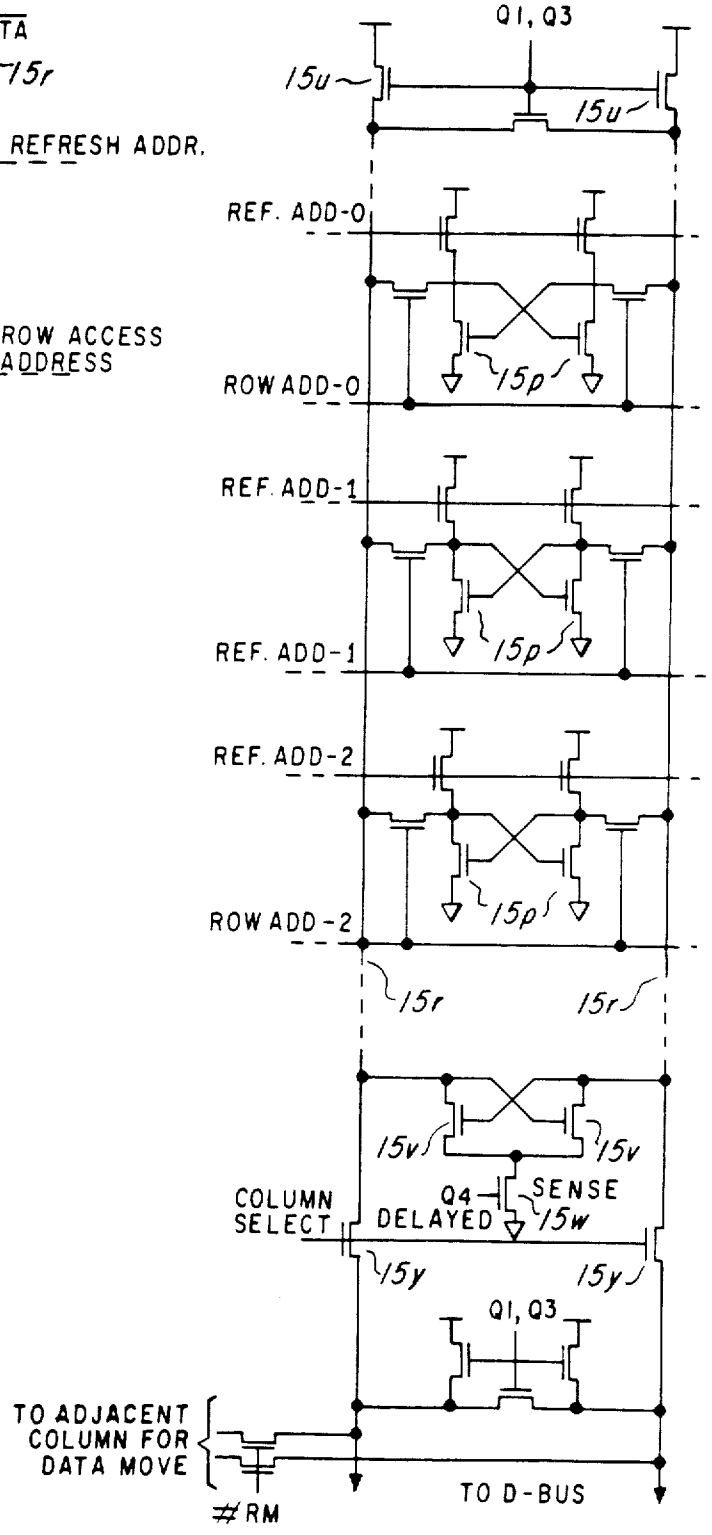

Q1, Q3
15u
15u
REF. ADD-0
15p
ROW ADD-0
REF. ADD-1
15p
REF. ADD-1
REF. ADD-2
15p
ROW ADD-2
15r
15r
15v
15v
COLUMN SELECT
Q4 DELAYED
SENSE
15w
15y
15y
Q1, Q3
TO ADJACENT COLUMN FOR DATA MOVE
TO D-BUS
#RM

Fig. 5h

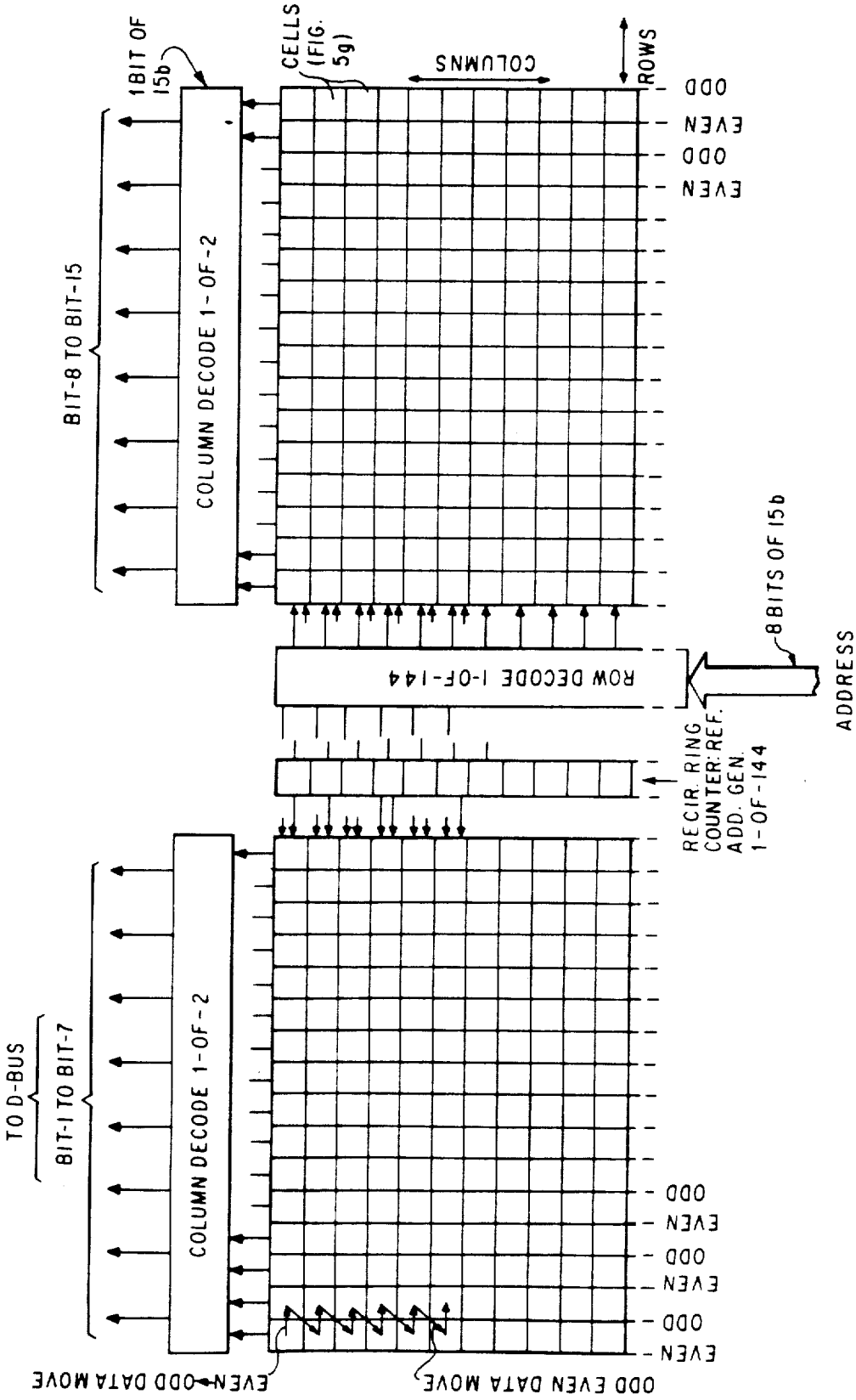

1 BIT OF 15b
CELLS (FIG. 5g)
COLUMNS
ROWS
ODD
EVEN
ODD
EVEN
BIT-8 TO BIT-15
COLUMN DECODE 1-OF-2
8 BITS OF 15b
ADDRESS
ROW DECODE 1-OF-144
RECIR. RING COUNTER: REF. ADD. GEN. 1-OF-144
TO D-BUS
BIT-1 TO BIT-7
COLUMN DECODE 1-OF-2
ODD
EVEN
ODD
EVEN
ODD
EVEN
EVEN-ODD DATA MOVE
ODD EVEN DATA MOVE

Fig. 5i

MICROCOMPUTER WITH BUS INTERCHANGE MODULE

This is a continuation of application Ser. No. 347,860, filed Feb. 11, 1982.

BACKGROUND OF THE INVENTION

This invention relates to integrated semiconductor devices and systems, and more particularly to a high-speed, miniaturized, electronic digital signal processing system in single-chip microcomputer form.

A microprocessor device is a central processing unit or CPU for a digital processor which is usually contained in a single semiconductor integrated circuit or "chip" fabricated by "MOS/LSI" technology, as shown in U.S. Pat. No. 3,757,306 issued to Gary W. Boone and assigned to Texas Instruments. The Boone patent shows a single-chip 8-bit CPU including a parallel ALU, registers for data and addresses, an instruction register and a control decoder, all interconnected using the Von Neuman architecture and employing a bidirectional parallel bus for data, address and instructions. U.S. Pat. No. 4,074,351, issued to Gary W. Boone and Michael J. Cochran, assigned to Texas Instruments, shows a single-chip "microcomputer" type device which contains a 4-bit parallel ALU and its control circuitry, with on-chip ROM for program storage and on-chip RAM for data storage, constructed in the Harvard architecture. The term microprocessor usually refers to a device employing external memory for program and data storage, while the term microcomputer refers to a device with on-chip ROM and RAM for program and data storage; the terms are also used interchangably, however, and are not intended as restrictive as to this invention.

Subsequent to 1971 when U.S. Pat. Nos. 3,757,306 and 4,074,351 were originally filed, many improvements have been made in microprocessors and microcomputers to increase the speed and capability of these devices and reduce the cost of manufacture, providing more circuitry and functions in less space, i.e., smaller chip size. Improved VLSI semiconductor processing and photolithographic techniques allow narrower line widths and higher resolution, providing added circuit density and higher speed, but circuit and system improvements also contribute to the goals of increased performance with smaller chip size. Some of these improvements in microcomputers are disclosed in the following U.S. Patents, all assigned to Texas Instruments: U.S. Pat. No. 3,991,305 issued to Edward R. Caudel and Joseph H. Raymond Jr.; U.S. Pat. No. 4,156,927 issued to David J. McElroy and Graham S. Tubbs; U.S. Pat. No. 3,934,233 issued to R. J. Fisher and G. D. Rogers; U.S. Pat. No. 3,921,142 issued to J. D. Bryant and G. A. Hartsell; U.S. Pat. No. 3,900,722 issued to M. J. Cochran and C. P. Grant; U.S. Pat. No. 3,932,846 issued to C. W. Brixely et al; U.S. Pat. No. 3,939,335 issued to G. L. Brantingham, L. H. Phillips and L. T. Novak; U.S. Pat. No. 4,125,901 issued to S. P. Hamilton, L. L. Miles, et al; U.S. Pat. No. 4,158,432 issued to M. G. VanBavel; U.S. Pat. No. 3,757,308 and U.S. Pat. No. 3,984,816. The devices described in these patents have been of the Harvard architecture and of the 4-bit type, particularly adapted for calculator or controller applications.

Additional examples of microprocessor and microcomputer devices in the evolutation of this technology are described in publications. In Electronics, Sept. 25, 1972, pp. 31–32, a 4-bit P-channel MOS microcomputer with on-chip ROM and RAM is shown which is similar to U.S. Pat. No. 3,991,305. Two of the most widely used 8-bit microprocessors like that of U.S. Pat. No. 3,757,306 are described in Electronics, Apr. 18, 1974 at pp. 88–95 (the Motorola 6800) and pp. 95–100 (the Intel 8080). A microcomputer version of the 6800 is described in Electronics, Feb. 2, 1978 at pp. 95–103. Likewise, a single-chip microcomputer version of the 8080 is shown in Electronics, Nov. 25, 1976 at pp. 99–105. Another single-chip microcomputer, the Mostek 3872, is shown in Electronics, May 11, 1978, at p. 105–110 and an improved version of the 6800 is disclosed in ELectronics, Sept. 17, 1979 at pp. 122–125. Sixteen-bit microprocessors based on minicomputer instruction sets evolved such as the part number TMS9900 described in a book entitled "9900 Family Systems Design", published in 1978 by Texas Instruments Incorporated, P.O. Box 1443, M/S 6404, Houston, Tex. 77001, Library of Congress Catalog No. 78-058005. The 8086, a 16-bit microprocessor evolving from the 8080, is described in Electronics, Feb. 16, 1978, pp. 99–104, while a 16-bit microprocessor identified as the 68000 (based on the 6800) is described in Electronic Design, Sept. 1, 1978 at pp. 100–107, and in IEEE Computer, Vol. 12. No. 2, pp. 43–52 (1979).

These prior 8-bit and 16-bit microprocessors and microcomputers have been general-purpose processors of the Von Neuman architecture with multiplexed address/data busses, and usually have been microcoded as described in U.S. patent application Ser. No. 209,915, filed Nov. 24, 1980 by Guttag, McDonough and Laws (now U.S. Pat. No. 4,402,043, or Ser. No. 253,624, filed Apr. 13, 1981, by Hayn, McDonough and Bellay, both assigned to Texas Instruments, and at pp. 28–34, IEEE Spectrum, March 1979, by McKevitt and Bayliss, or Proceedings 11th Annual Microprogramming Workshop, December, 1979 by Stintter and Tredenick. Microcoding, originally described by Wilkes in 1951, employs a control ROM to store microinstruction sequences entered by instruction words; the programmer works in a higher level machine code, so the number of assembly language code statements is supposedly reduced, and thus programming cost is reduced.

In contrast, a special-purpose high-speed microcomputer device according to the embodiment of the invention described herein departs from these contemporary microprocessor devices in several major respects in order to achieve substantial speed and performance advantages. This device is a non-microcoded processor of modified Harvard architecture.

It is the principal object of this invention to provide improved features of a microcomputer device and system, particularly one adapted for real-time digital signal processing. Another object is to provide a high-speed microcomputer of enhanced capabilities.

SUMMARY OF THE INVENTION

In accordance with one embodiment, features of the invention are included in a system for real-time digital signal processing employing a single-chip microcomputer device having separate on-chip program ROM and data RAM, with separate address and data paths for program and data. An external program address bus allows off-chip program fetch in an expansion mode, with the opcode returned by an external data bus. A bus interchange module allows transfer between the sepa-

rate internal program and data busses in special circumstances. The internal busses are 16-bit, while the ALU and accumulator are 32-bit. A multiplier circuit produces a single state 16×16 multiply function separate from the ALU, with 32-bit output to the ALU. One input to the ALU passes through a 0-to-15 bit shifter with sign extension.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as other features and advantages thereof, will be best understood by reference to the detailed description which follows, read in conjunction with the accompanying drawings, wherein;

FIG. **1** is an electrical diagram in block form of a microcomputer system employing features of the invention;

FIG. **2** is an electrical diagram in block form of an MOS/LSI microcomputer device (including a CPU or central processor unit) employed in the system of FIG. **1** and utilizing features of the invention;

FIGS. **3***a*–**3***mm* are timing diagrams showing voltage or event vs. time in the operation of the microcomputer of FIG. **2**;

FIGS. **4** and **4***a* are greatly enlarged plan views of a semiconductor chip containing the microcomputer of FIG. **2**, showing the physical layout of the various parts of the device;

FIGS. **5***a*–**5***i* are electrical schematic diagram of particular circuits in the microcomputer device of FIG. **2**.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENT

Microprocessor System

The microcomputer device to be described herein is primarily used for signal processing, but concepts thereof may be used in processor devices of various configurations, and these devices may be used in many different systems; in one embodiment the microcomputer is used in a system shown in generalized form in FIG. **1**. The system may be, for example, a voice communication system, a speech analysis system, a small "personal" or "home" computer, a single-board general purpose microcomputer, a word processing system, a computer terminal having local processing capability with display and typewriter keyboard, or any one of many applications of various types. The system includes a single-chip MOS/LSI central processing unit or microcomputer **10** which will be described in detail, along with a program or data memory **11** and input/output or I/O devices **12**. Usually the I/O devices **12** for the typical system include analog-to-digital and/or digital-to-analog converters, a modem, a keyboard, a CRT display, a disc drive, etc. Often the I/O **12** includes coupling to a general purpose processor; that is the microcomputer **10** is an attached processor in a larger system with interface via the I/O **12**. The microcomputer **10**, program data memory **11** and I/O **12** communicate with one another by two multibit, parallel address and data busses, D and RA, along with a control bus **13**. The microcomputer **10** has suitable supply voltage and crystal-input terminals; for example, the device employs a single +5 V Vcc supply and ground or Vss, and a crystal is connected to terminals X1 and X2 of the device **10** to control certain system timing. The microcomputer **10** is a very high speed device with a crystal input of 20 MHZ, providing an instruction execution rate of five million per second, in one embodiment.

The microcomputer device **10** is a general purpose microcomputer specifically aimed at serving a large class of serial signal processing problems such as digital filtering, signal handling for telecommunications modems (modulation, demodulation), data compression for linear predictive code (LPC) speech signals, fast Fourier transforms, and in general for virtually all computation intensive analog system functions, including detection, signal generation, mixing, phase tracking, angle measurement, feedback control, clock recovery, correlation, convolution, etc. It is suitable for applications which have computational requirements similar to those for control and signal processing, such as coordinate transformation, solution of linear differential equations with constant coefficients, averaging, etc. The device **10** is usually interfaced via I/O **12** to a general purpose processor such as a 99000, an 8600 or a 68000, to construct processing systems as will be explained.

It is understood that, even though described in the context of a microcomputer in the preferred embodiment, with an on-chip program ROM **14** and data RAM **15**, nevertheless, some concepts of the invention may be used in a single-chip microprocessor with all off-chip program memory and/or data memory instead of the on-chip memory illustrated. Indeed, modes of operation are provided which disable the on-chip memory. Also, a microcomputer is shown having two separate external program address and data busses instead of the multiplexed, bidirectional busses which are now common, but some features herein disclosed are applicable where busses are multiplexed. The advantage of separating the busses and separating program and data memory space is speed.

In general terms, the system of FIG. **1** functions in the following manner: the microcomputer **10** fetches an instruction word internally by accessing the ROM **14** or externally by sending out an address on the ROM address bus RA to the memory **11** (and RCLK-on control bus **13**). If external, the instruction word is received back via the data bus D from the addressed location in the memory **11**. This instruction is executed in the next machine cycle (of length of 200 ns defined by a 20 MHz clock or crystal X1, X2) while a new instruction is being fetched; execution of an instruction may include accessing the on-chip RAM **15** for an operand, or writing a result into data RAM **15**, and an arithmetic or logic operation in ALU.

In the example to be described in detail, a 12-bit instruction address applied internally to ROM **14** or externally to the RA bus directly addresses 2^{12} or 4K words of program instruction or constants in ROM **14** and memory **11**. When reading from memory **11**, a DEN– (data bus enable bar) command is asserted on control bus **13**. It is also possible to write into the memory **11**, and for this purpose a WE– (write enable bar) command is asserted by the device **10** on one of the control bus lines **13**; the memory **11** may contain read/write memory devices in some or all of the address space, so the WE– command permits a write function.

The I/O devices **12** are addressed as ports; this interface to external devices **12** is accomplished using the address and data busses RA and D and control bus **13**, but the I/O devices **12** do not occupy locations in the logical address space like the memory **11**. This is in contrast to conventional memory-mapped I/O.

Data input/output via I/O or peripherals **12** employs a 3-bit field from the bus RA to select one of eight 16-bit ports in peripheral circuitry **12**. The selected 16-bit port is then accessed for read or write via the bus D. This operation uses one of the two instructions IN or OUT, on the control bus **13**, WE− is active for write or OUT, or DEN− is active for read or IN. A ROM clock RCLK− is active on control bus **13** on every machine cycle except when either DEN− or WE− is active; that is, the memory **11** is activated by RCLK− for possible instruction word access from off-chip in each machine cycle, but if accessing peripheral **12** using DEN− or WE− then the RCLK− does not occur.

A reset signal RS− on the control bus **13** clears the program counter and address bus RA (resets to zero), sets the data bus D in a high impedance state, and the memory controls DEN−, WE− and RCLK− in an inactive (high) state. All address and temporary data registers within the microcomputer **10** are cleared by a reset routine in the ROM **14**, but the internal RAM is not cleared. In this manner, the peripheral circuitry **12** (such as a main processor) can assert control, or initiate a start-up or power-on sequence.

An interrupt signal INT− on the control bus **13** causes the microcomputer **10** to halt execution (saving the current ROM address) and go to an interrupt vector address, unless interrupts are masked by the program.

The ME/SE− line in the control bus **13** defines the memory expansion mode or systems emulator mode for the microcomputer **10**. When this pin is held high (at +Vcc), the microcomputer executes from on-chip ROM and off-chip memory **11**, but when low (Vss) the chip is in the systems emulator mode and execution is only from the memory **11** which is PROM, EPROM or RAM so the program can be easily changed.

The Microcomputer Chip

The internal architecture of the microcomputer **10** is shown in a detailed block diagram in FIG. **2**. This device is a single-chip semiconductor integrated circuit mounted in a standard dual-in-line package or a chip carrier. Sixteen pins or terminals of the package are needed for the 16-bit data bus D, twelve to sixteen are used for the address bus RA (depending upon memory size) and the remaining terminals are used for the power supply Vcc and Vss, the crystal X1, X2, and the control bus **13**.

In addition to the program and data memory **14** and **15**, the microcomputer **10** contains a central processing unit or CPU for the system of FIG. **1**, and this CPU includes a 32-bit arithmetic logic unit or ALU, a 32-bit accumulator Acc to hold operands and results, multiplier M separate from the ALU, a shifter S which is one input to the ALU, status or flag decode SD, and an instruction decoder ID1 which receives part of the current instruction word and generates the control bits for the CPU and data memory portions of the device **10**.

The program memory **14** has associated with it a program counter PC to hold the instruction address used to access the ROM **14** or sent out on bus RA to the memory **11**, an instruction register IR to receive the instruction word from ROM **14**, a stack ST to save program memory addresses, and an instruction decoder ID2 which receives part of the current instruction word and generates control bits for the program memory portion of the microcomputer.

Associated with the data memory **15** are two auxiliary address registers AR0 and AR1 for the data memory **15**, a page register ARP to select between the registers AR0 and AR1 as the data memory address, and a data page buffer DP to hold certain bits of the data memory address.

The CPU is oriented around two internal busses, a 12-bit program bus (P-Bus) and a 16-bit data bus (D-Bus). Program access and data access can thus occur simultaneously, and the address spaces are separate. A bus interchange module BIM permits loading the program counter PC from Acc, for example, or accessing ROM **14** for constants via P-Bus, BIM and D-Bus.

The two major requirements for a signal processing microcomputer are high speed arithmetic and flexibility. Performance is achieved by using separate, principally on-chip program and data memories **14** and **15**, a large single accumulator Acc and a parallel multiplier M. A special purpose operation, data move, is defined within the data memory **15** which further enhances the performance in convolution operations. Flexibility has been achieved by defining an instruction set as will be described with reference to Table A, incorporating memory expansion and a single lever of interrupt.

The device can be configured with, for example, less than 2K or 2^{11} words of on-chip program memory **14** and the architecture allows for memory expansion up to 4K or 2^{12} words by the addition of external program memory in the memory **11**. In addition, a separate mode allows the device **10** to be configured as a system emulation device; in this "system emulator" mode, the entire 4K memory space is external and the ROM **14** is not used.

The CPU

The arithmetic logic unit or ALU consists of thirty-two parallel stages, each separate stage performing an arithmetic or logic function on its two input bits and producing a one-bit output and carry/borrow. The ALU has two 32-bit data inputs ALU-a and ALU-b, and a 32-bit data output ALU-o to accumulator Acc. The ALU-a input is always from the accumulator Acc and the ALU-b input is always either from the shifter S or from a 32-bit product register P in the multiplier M. The particular function performed on data passing through the ALU is defined by the current instruction word in IR which is applied by the program bus P-Bus to an instruction decoder ID1. The source of the ALU-b input is defined by an input select circuit ALU-s which selects from these two alternatives, based upon the contents of the current instruction word, i.e., the outputs #C of the decoder ID1. The shifter S receives a 16-bit input Si from D-Bus and produces a 32-bit output So which is the input Si shifted from zero to fifteen places to the left. Left-shifted data is zero-filled, i.e., all right-hand bit positions are filled with zeros when data is shifted out to the left. A unique feature is that the high-order bit is sign extended during shift operations. The ALU operates in twos-complement. The shifter S includes a shift control Sc loaded with a four-bit value from P-Bus via lines Sp so an arithmetic instruction can directly define the number of bits shifted in the path from D-Bus to the ALU-b input.

In this description, the LSB is considered to be on the right and the MSB on the left, so left-shift is toward more significant bits. Bit-0 is the MSB and bit-15 is the LSB. Data is always in signed 2's complement in this architecture.

The multiplier M is a 16×16 multiplier using carry feed-forward, constructed in partly dynamic and partly

static logic, to implement Booth's algorithm. One input to the multiplier M is the T register which is a 16-bit register for temporary storage of the multiplicand received from D-Bus via lines Ti. The other 16-bit input is via lines Mi from the D-Bus; this multiplier input may be from the data memory **15** or may be a 13-bit multiply-immediate value derived directly from the instruction word (loaded right-justified and sign-extended).

The ALU always receives the contents of the accumulator Acc as its ALU-a input, and always stores its output in Acc, i.e., Acc is always the destination and the primary operand. The unit will add, subtract and perform the logic operations of And, Or and Exclusive Or. The logic operation results are between the lower half of Acc (bits **16–31**) and a 16-bit value from the data memory **15**. Due to passing the data memory value through the shifter S (with zero shift), the operand for the logical operation result of the MSBs (bits **0–15**) is zero. The final 32-bit result reaching the accumulator is thus in two parts: Bits **0–15** will be Acc bits **0–15** Anded (or Or'ed, etc) with zero; bits **16–31** of the result will be Acc bits **16–31** Anded (etc.) with the data memory value. The accumulator Acc output, in addition to the 32-bit ALU-a input, includes high and low 16-bit outputs Acc-H (bits **0–15**) and Acc-L (bits **16–31**); separate instructions "store accumulator high" SACH and SACL "store accumulator low" are provided for storing high and low-order Acc bits in the data memory **15**.

The status decoder SD monitors the Acc whenever an instruction which updates Acc is executed. Four bits of SD are OV, L, G and Z. Accumulator overflow (or underflow) is indicated by the OV bit, Acc contents less than zero is indicated by the L bit, Acc greater than zero indicated by the G bit, and Acc equal zero indicated by the Z bit. Upon interrupt the OV bit is saved in an overflow flag register, but the other bits are available only up to the time the next accumulator instruction is executed.

The accumulator overflow mode is a single-bit mode register OVM (included in SD), directly under program control, to allow for saturated results in signal processing computations. When the overflow mode OVM is reset, overflow results are loaded via ALU-o into the accumulator Acc from the ALU without modification. When the overflow mode is set, overflow results are set to the largest, or smallest, representable value of the ALU and loaded into the accumulator Acc. The largest or smallest value is determined by the sign of the overflow bit. This allows a saturated Acc result in signal processing applications, modeling the saturation process of analog signals.

A separate status bit in SD monitors the condition of the currently used auxiliary register AR0 or AR1 and detects the all-zero condition of the least significant nine bits of the current auxiliary register (i.e. loop counter portion). This bit is used for a branch instruction conditioned on non-zero for the auxiliary register (BARNZ), "branch on auxiliary register non-zero."

The input/output status bit (I/O ST−) is an external pin which is part of the control bus **13** and provides "branch on I/O zero" instruction (BIOZ) to interrogate the condition of peripheral circuits **12**. A zero level on the I/O ST− pin will cause a branch when sampled by the BIOZ instruction.

The bus interchange module BIM exchanges the low-order twelve bits of the 16-bit value on the D-Bus with the twelve bits on the P-Bus. This operation is not available to the programmer as an instruction, but instead is needed as an inherent operation in instructions such as table look up (TBLR A).

PROGRAM MEMORY ADDRESSING

The program memory **14** is a ROM which is partitioned to produce a 16-bit output to instruction register IR, and this ROM employs a decoder **14***a* which selects one 16-bit instruction word based on an 11-bit or 12-bit address on input lines **14***b*. In the example embodiment, the ROM **14** contains less than 2K words, so an 11-bit address can be used, but the on-chip program memory could be expanded to 4K with a 12-bit address. The circuit of the ROM **14** is especially adapted for fast access as will be explained. The address input **14***b* is received from the program counter PC which is a 12-bit register containing the address of the instruction following the one being executed. That is, at the time when the control bits #C are valid at the outputs of the instruction decoders ID1 and ID2 for one instruction, PC contains the address of the next instruction; an address in PC goes into decoder **14***a* and the next instruction is read from ROM **14** into IR, and the program counter PC is incremented via PCinc in preparation for another instruction fetch. That is, PC is self incrementing under control of a #C control bit from ID2. The output PCo from the program counter PC is also applied via lines RApc and selector RAs (and output buffers not shown) to the external RA bus via output lines RAo and twelve output pins of the microcomputer device. The RA bus (RA0 through RA11) contains the PC output via RApc when the selector RAs is in one mode, or contains the input RAi when executing I/O instructions IN and OUT. Whenever the address in PC is above the highest address in ROM **14**, off-chip program addressing to memory **11** is assumed; however, the device is designed to operate principally with the on-chip ROM, so for many uses of the device off-chip fetches for program instructions would never be needed. The program counter PC may be loaded via input PCi and selector PCs from the P-Bus for branch or call instructions, or loaded from the accumulator Acc via Acc-L, D-Bus, BIM, P-Bus, PCp and PCi in a "call accumulator" CALLA instruction.

The register stack ST is used for saving the contents of PC during subroutine and interrupt calls. In the illustrated embodiment, the stack ST contains four 12-bit registers constructed as a first-in, last-out push-down stack, although a larger or smaller number of registers could be used. The current contents of PC are saved by "pushing" onto the top-of-stack register TOS via lines PCst. Succesive CALL instructions will keep pushing the current contents of PC onto TOS as the prior contents are shifted down, so up to four nested subroutines can be accomodated A subroutine is terminated by execution of a return instruction RET which "pops" the stack, returning the contents of TOS to PC via lines PCt, selector PCs and input PCi, allowing the program to continue from the point it had reached prior to the last call or interrupt. When TOS is popped, the addresses in lower registers of ST move up one position. Each subroutine, initiated by a call instruction or an interrupt, must be terminated by a RET instruction.

In an example embodiment, the ROM **14** contains 1536 words, so the remainder of the 4K program address space, 2560 words, is off-chip in the memory **11**. When the memory expansion control pin ME/SE− is high, at logic 1, the device interprets any program address in PC in the 0-to-1535 range as being an on-chip

address for the ROM **14**, and any address in the 1536–4095 range as being an off-chip address so that the PC contents are sent out via RApc and RAo to the RA bus. An output strobe RCLK— generated by the decoder ID2 for every machine state enables the external memory **11** (except when IN or OUT instructions are being executed). When off-chip program memory **11** is accessed, the instruction word read from memory **11** is applied to the external bus D and thus to the internal P-Bus via input/output control DC and lines Dp; this is a 16-bit instruction and, like the output of ROM **14** via IR, it is loaded into decoders ID1 and ID2 for execution, or loaded into PC via PCp, or otherwise used just as an on-chip instruction fetch.

When the ME/SE— pin is at zero the device enters the system emulator mode wherein the entire 4K program address space is off-chip, so all PC addresses are applied to the RA bus via RApc and RAo. This mode is necessary when a user is developing systems or programs, prior to arriving at a final version of code for the ROM **14**. That is, the microcomputer **10** can operate with no code permanently programmed into the ROM so that new programs (stored in RAM or EPROM in the memory **11**) can be tested and debugged, then when the final code is extablished the chips **10** are produced in large volume with this code mask-programmed into the ROM **14**.

In either mode, the first two program addresses 0000 and 0001 are used for the reset function. When the reset pin RS— is brought low, an address of all zeros is forced into the program counter PC, as will be explained. Also, the third address is reserved for an interrupt vector; when the INT— pin is brought low, an address of 0002 is forced into PC to begin an interrupt routine.

DATA MEMORY ADDRESSING

The data memory **15** in the example embodiment contains 144 16-bit words, and so an 8-bit address is needed on address input **15***a* to the RAM address decoder **15***b*. However, the RAM **15** may be constructed with up to 512 words, requiring a 9-bit address, so the addressing arrangement will be described in terms of address bits which are unused in some embodiments. Each 128 word block of the RAM **15** is considered to be a page, so a 7-bit address field in an instruction word from program memory **14** on P-Bus via input **15***c* is used to directly address up to 128 words of data memory **15**. Two auxiliary registers AR0 and AR1 are employed in the example embodiment; however, up to eight of these 16-bit registers may be used, with the particular one currently being used as the source of the address for the RAM **15** being defined by the auxiliary register pointer ARP. With two registers AR0 and AR1, the pointer ARP is only one bit, but for an embodiment with eight auxiliary registers the pointer ARP is a 3-bit register. The 16-bit auxiliary registers AR0 and AR1 are under control of store, load or modify auxiliary register instructions SAR, LAR, and MAR as will be described. Nine-bit addresses from the low-order parts of the auxiliary registers may be applied to the address input **15***a* via selector **15***d*, , lines **15***e*, selector **15***f*, and lines **15***g*. When one of the auxiliary registers is to be the source of the RAM address, the selector **15***d* uses the value on lines **15***e* as the address input **15***a*, whereas if the P-Bus is to be the source of the RAM address the selector **15***d* uses a 7-bit address from input **15***c* and a 1-bit (expandable to 3-bit or 4-bit) page address from the data page register DP. The selector **15***f* is controlled by the pointer ARP which is loaded from P-Bus as defined by an instruction. The auxiliary registers are used for indirect addressing wherein an instruction need not contain a complete address for RAM **15** but instead merely specifies that an auxiliary register is to be used for this address; such instructions can also specify increment or decrement for the auxiliary register selected, in which case the nine LSBs of AR0 or AR1 are changed by +1 or −1 via paths Inc. The auxiliary registers may be thus used as loop counters. The auxiliary registers are accessed by the D-Bus vis lines ARio so these registers may be used as miscellaneous working registers, or may be initially loaded to begin a loop count.

The data memory **15** is accessed via the D-Bus and an input/output circuit **15***i*, via lines **15***j*. Construction of the data memory is such that a data move wholly within the RAM **15** is permitted, according to an important feature of the microcomputer **10**. Under instruction control, the data at one address can be moved to the next higher location in one machine cycle without using the ALU or D-Bus. Thus during an add, for example, the accessed data can be also moved to the next higher address. INPUT/OUTPUT FUNCTIONS

Input and output of data from the microcomputer chip **10** uses the data bus D and two of the lines of the control bus **13**, these being data enable bar (DE—) and write enable bar (WE—). Two instructions, IN and OUT, are employed for the data input and output functions. The external data bus D is coupled to the internal data bus D-Bus by the input/output control and data buffers DC. The output buffers in D1 are tri-state, so the output to data bus D is always placed in a high impedence state except when IN or OUT is being executed; to this end, one of the controls #C from the instruction decode ID1 sets the output buffers in high impdence state whenever IN or OUT is not decoded. When the instruction IN is present, the control DC activates sixteen input buffers, so the external data bus D is coupled to the internal D-Bus via DC and lines Dd for data input. When the OUT instruction is decoded, a control #C from ID1 activates output buffers in DC so the internal D-Bus is coupled via Dd and DC to the external bus D.

Execution of an IN instruction will also generate a data enable DEN— strobe on line **13***a* from ID1, and will couple the D-Bus to the RAM **15** via **15***i* and **15***j*, so the data from external will be entered into on-chip data memory. The intended uses of the microcomputer as a signal processor require hundreds or thousands of accesses to RAM **15** for every off-chip reference. That is, a value will be fetched from off-chip then convolution or like operations performed using this new value and other data in the RAM **15**, so thousands of instruction executions will transpire before another off-chip reference is needed. For this reason, the architecture favors internal data manipulation over off-chip data access.

Execution of an OUT instruction causes generation of an off-chip write enable WE— strobe on line **13***b* from ID1 and outputs data from RAM **15** via **15***i* and **15***j*, D-Bus, lines Dd and buffer DC to the external bus D. Referring to FIG. **1**, this data may be written into one of the ports (selected by the 3-bit RAi value) in the peripherals **12**.

Implicit in both the IN and OUT instructions is a 3-bit port address on lines RAi from ID1. This address is multiplexed onto the three LSBs (RA9–RA11) of the external address bus RA via selector RAs. Up to eight

peripherals may thus be addressed. The remaining high order bits of the RA bus outputs are held at logic zero during these instructions.

THE INSTRUCTION SET

The microcomputer **10** of FIGS. **1** and **2** executes the instruction set of Table A. The Table shows in the first column in mneumonic or assembly language name of each instruction used in writing source code, followed in the second column by the object code in binary which is the form the code appears in the ROM **14** and in the instruction register IR. This binary code is decoded in ID1 and ID2 to generate all of the controls #C to execute the desired operation by accessing various busses and registers and setting the functions of the ALU. The Table also gives the number of cycles or machine states employed by the microcomputer in executing the instruction; note that all instructions except branches, calls, table look-up and input/output are executed in one state time. The microcomputer is not microcoded; the standard ALU instructions are executed in one state. The Table also shows the number of instruction words needed to execute each instruction; it is important to note that only branches and call direct require two instruction words. The right-hand column is a brief description of the operation for each instruction.

Most of the instructions of Table A show the low-order eight bits (bits **8–15**) as "IAAAAAAA", which is the direct or indirect RAM **15** address for one operand. If the "I" bit, bit-**8**, is 0, the direct addressing mode is used, so the "A" field of the instruction word, bits **9–15**, is employed as a direct address connected from IR through P-Bus, lines **15***c* and selector **15***d* to address input **15***a*. In this direct addressing mode, the auxiliary registers AR0–AR1 are not used.

For the instructions containing "IAAAAAA", the indirect addressing mode is specified by a 1 in the I field, bit-**8**, of these instructions. The input address on lines **15***a* for the RAM **15** will in this case be obtained from one of the auxiliary registers AR0 or AR1, and bit **15** will select which one. If bit-**15** is 0, AR0 is used; if bit-**15** is 1, AR1 is used. Thus bit-**15** coupled from IR via P-Bus controls the selector **15***f* (and can be loaded into the ARP register). Since the number of auxiliary registers is expandable to eight, bits **13–15** of these indirect-address instructions are reserved for use with a 3-bit selector **15***f* and ARP register to define one-of-eight in the indirect addressing mode. Bit-**10** to bit-**12** are controls in indirect addressing: bit-**10** causes the addressed auxiliary register to be incremented if 1, or no change if 0; bit-**11** causes the addressed AR to be decremented if 1 or no change if 0; bit-**12** if 0 causes bit-**15** to be loaded into ARP after execution of the current instruction, or if 1 leaves the ARP unchanged.

The shift code SSSS used in many instructions of Table A is a four-bit field loaded into shift control Sc via Sp to define the number of spaces (zero to fifteen) that the data coming from the RAM **15** via D-bus is left shifted as it passes through the shifter S on the way to the ALU-b input.

Although not material to the structure described herein, assembly language formats using the instruction set of Table A employ "A" to designate direct addressing and "@" to designate indirect. Thus, "ADD S,A" means add contents of memory location defined by the A field of the instruction word. "ADD A@" means add using contents of the data memory location addressed by the auxiliary register AR0 or AR1 selected by the existing contents of ARP. ADD S@+ means add using current contents of ARP to define AR then increment this auxiliary register for loop counting. ADD S@ is the same as previous except decrement by 1. ADD S@,AR is same as previous except ARP is loaded with the value of bit-**15** to define a new auxiliary register for subsequent operations.

The descriptions given in the right-hand column of Table A assume direct addressing. For indirect addressing, the above explanation applies.

The ADD instruction thus adds the 16-bit contents of RAM **15** (at location OAAAAAAA for direct, or the contents at the locations in RAM **15** selected by the chosen AR if indirect), shifted SSSS spaces left, to the 32-bit contents of the Acc, and stores the result in the Acc. ADDH does the same except only the high-order half of Acc is the source of one operand and destination of the result, and no shift is performed.

The subtract instructions SUB and SUBH subtract the addressed RAM **15** data from the accumulator and store the result in Acc, but are otherwise the same as add. The load instruction LAC loads Acc with the 16-bit data addressed by IAAAAAAA which is left-shifted by SSSS bits. Only ADD, SUB and LAC specify a shift.

There are four instructions associated with the auxiliary registers: SAR, LAR, LARK and MAR. Store auxiliary register SAR causes the contents of one of the auxiliary registers defined by RRR to be stored in the memory location IAAAAAAA; the load AR instruction LAR is the reverse of SAR. With the LARK instruction a constant K from IR (bits **8–15**) is loaded into the AR defined by RRR; this 8-bit constant K is right-justified and MSBs set to zero in the 16-bit auxiliary register. The modify auxiliary instruction MAR causes one auxiliary register to be modified by bits-**10** to **12** as above, but no add or memory **15** access is implemented. The MAR code is operative only in the indirect mode, I=1; in direct mode this instruction results in no-op.

The input/output instructions are written in assembly language as "IN PA, A" or "OUT PA, A", where PA is the 3-bit port address PPP output on bits **9–11** of the RA bus (generated from the decoder ID1 and coupled via lines RAi). IN enables DEN− and disables RCLK−, while OUT enables WE− and disables RCLK−. The peripheral devices **12** decode RA9–RA11 to select one of eight 16-bit ports or locations for read or write via the bus D. These instructions use two machine states so that the data input pins of bus D are free on the second state to allow external fetch of the next instruction from memory **11** instead of ROM **14**.

The store accumulator instructions SACL and SACH, written as "SACL X,A" in assembly, cause the low or high order bits of Acc to be left-shifted XXX places and stored in the data memory **15** at the location defined direct or indirect by IAAAAAAA. The X field is not fully implemented in the example embodiment; for SACL only X=0 is allowed and for SACH only X=0, X=1 and X=4 are allowed. This shift is implemented in the accumulator circuitry itself rather than in the shifter S.

The arithmetic and logic instructions without shift code are ADDH, ADDS, SUBH, SUBS, SUBC, ZALH, ZALS, EXOR, AND, OR and LACK. These are all written as ADDH A, for example, in assembly language. ADDH causes the 16-bit data from the defined location in RAM **15** to be added to the high-order

half of Acc and stored in the high-order half of Acc; actually the data from RAM **15** is left shifted sixteen bits in shifter S as it goes from D-Bus to the ALU-b input. The ADDS instruction means that the sign extension is suppressed in the shifter S; the data from RAM **15** defined by A is treated as a 16-bit positive number instead of a signed 2's complement integer. SUBH and SUBS correspond to ADDH and ADDS except subtract is performed in the ALU.

The conditional subtract instruction SUBC is used in divide operations. The contents of the defined location in RAM **15** are subtracted from the contents of Acc and left-shifted fifteen bits, producing an ALU output ALU-o which, if equal to zero is left-shifted by one bit and a +1 is added, with the result stored in Acc. If the ALU output is not equal to zero then it is left-shifted by one-bit and stored in Acc (the +1 is not added). SUBC is a two-cycle instruction that assumes the accumulator is not used in the following instruction. If the following operation involves Acc then a NO OP instruction should be inserted after SUBC.

The "xero accumulator load high" instruction ZALH fetches the 16-bit word at the addressed location in the RAM and loads it into the high-order half of Acc (bits **0–15**); the Acc has been zeroed, so the low-order bits **16–31** reamin zero. The shifter S is in the data path from D-Bus via ALU to Acc, so a 16-bit shift is performed in ZALH to move the data to the high-order half. The ZALS instruction fetches a word from RAM and loads it into the low-order half of the zeroed Acc, with sign extension suppressed in the shifter S.

The logic operations EXOR, AND and OR are performed in 32-bit format, even though the operand fetched is sixteen bits. For EXOR, the high-order half of Acc is Exclusive Or'ed with zeros, concatenated with Exclusive Or of the fetched data with the low-order half of Acc, both halves of the result being stored in Acc. The same applies to OR and AND.

The load accumulator instruction LACK causes an 8-bit constant contained in the eight LSB's of the instruction word to be loaded into the eight LSB's of Acc, right justified; the upper twenty-four bits of Acc are zeroed. To accomplish this operation, the instruction word on P-Bus from IR (after ID1 and ID2 are loaded, of course), is coupled to the D-Bus by BIM, and thence to the ALU-b via shifter S (with no shift). The ALU performs "pass ALU-b" or add zeros to b, leaving the constant in Acc.

The data shift or data move instruction DSHT causes the contents of the defined location in the RAM **15** to be moved to the defined location plus one. This is accomplished internal to the RAM **15** without using the ALU or data bus D-Bus. The operation cannot cross a page boundry, however.

The "load T" instructions are used to set up multiply operations. LT causes the T register to be loaded from RAM **15** with the value defined by IAAAAAAA. The "load T with data move" instruction LTD employs an operation like DSHT in the RAM; the T register is loaded with the contents of the RAM **15** location defined by IAAAAAAA, then this same value is shifted to location IAAAAAAA+1, and also the contents of Acc is added in ALU to the contents of the P register with the result going to Acc. The LTA instruction is the same as LTD but without data move; the T register is loaded from RAM **15** and the P register is added to Acc, with result to Acc.

The multiply instruction MPY causes the 16-bit contents of T register to be multiplied in multiplier M (not using ALU) by the value from RAM **15** on the input Mi from D-Bus, with the 32-bit result going to the P register. The "multiply constant" instruction MPYK causes the 16-bit contents of T register to be multiplied by a 13-bit constant C from the opcode in IR; the 32-bit result stays in P register. For MPYK, the constant is connected from IR to Mi via P-Bus, BIM and D-Bus.

The "load data page" instructions LDPK and LDP cause the data page register DP to be loaded with up to eight bits from the opcode itself or from the defined location in RAM **15**. In the embodiment shown, the DP register is only one bit, but in other embodiments with a larger RAM **15** the DP register contains up to eight bits. The page address remains the same until a new load page instruction occurs.

The load status and store status instructions LST and SST are used in call subroutine or interrupts to save the contents of the status circuits SD, or restore status SD. These instructions are used instead of hard wired circuits for performing this function.

The disable and enable interrupt instructions DINT and EINT are used to mask or unmask the interrupt capability, i.e., these instructions reset or set a latch which determines whether or not the microcomputer **10** responds to the INT− pin.

An absolute value instruction ABS functions to assure that the accumulator contains only an absolute valve, i.e., if Acc is less than zero, the absolute value of Acc is loaded into Acc, but if Acc is greater than zero there is no change. Similarly, the zero accumulator instruction ZAC clears Acc.

The overflow mode instructions RAMV and SAMV cause the overflow mode latch OVM in the status decode SD to be set to 1 or reset to 0. When set, the ALU output is set to its maximum or minimum before loading into Acc upon overflow. This simulates the effect of saturating an amplifier in an analog circuit, and is useful in signal processing.

Three P register instructions PAC, HPAC and SPAC are used in manipulating data after a multiply MPY or MPYK. PAC loads the accumulator with the contents of the P register by passing the 32-bit data through the ALU without performing any operation to modify the data; actually the ALU-a input is zeroed and an ADD is executed. The APAC instruction adds the contents of the P register to the contents of Acc, with the result going to Acc. Similarly, the SPAC subtracts the contents of P register from Acc, result to Acc.

The subroutine instructions are CALL, CALLA and RET. CALL is a two-word instruction; the first word is the opcode and the second is the absolute address of the first instruction in the subroutine. When CALL is decoded in ID2, PC is incremented to fetch the next instruction word which is the address, then the incremented contents of PC are pushed to stack ST. The subroutine ends in return RET which causes the address on TOS to be popped and loaded into PC. To save status, SST must be used before CALL, and LST inserted after RET. The CALLA instruction is unique for a Harvard architecture machine; this uses the contents of Acc as the subroutine address rather than using the next location addressed by PC+1. The low-order bits of Acc are transferred via Acc-L and BIM to the P-Bus and thus via PCp to the program counter PC. The incremented PC is saved in CALLA by pushing to ST just as in a CALL.

The table look up instructions TBLR and TBLW also employ the Acc as an address source. These instructions require three states to execute. The RAM **15** location defined by IAAAAAAA is transferred via D-Bus and BIM to P-Bus, and thus via PCp to PC, from whence this address is applied via RApc to the external RA bus, or to ROM **14**.

The branch instructions all require two words, the first being the opcode and the second at PC+1 being the address. The low-order bits **8–15** of the opcodes are unused. Unconditional branch B loads the word at PC+1 into PC as the next address. BARNZ is conditional upon whether or not a loop counter, one of the auxiliary registers defined by ARP, is not-zero. BV causes a branch if the overflow bit OV in the status decode SD is a 1. BIOZ causes a branch if the IO bit from I/O ST− is a 1 in the status decoder SD. The six instructions BLZ, BLEZ, BGZ, BGEZ, BNZ and BZ are all dependent upon the defined condition in SD reflecting the condition in Acc.

SYSTEM TIMING

Referring to FIGS. *3a–3ii*, the timing of the system of FIG. **1** and the CPU chip of FIG. **2** is illustrated in a sequence of voltage vs. time waveforms or event vs. time diagrams. The chip **10** includes a clock generator **17** which has two external pins X1 and X2 to which a crystal (or external generator) is connected. The basic crystal frequency is up to 20 MHz and is represented by a clock **0** of FIG. *3a*. This clock **0** has a period of 50 ns, minimum, and is used to generate four quarter-cycle clocks Q1, Q2, Q3 and Q4 seen in FIGS. *3b–3e*, providing the basic internal timing for the microcomputer chip **10**. A set of four quarter cycle clocks Q1 to Q4 defines one machine state time of 200 ns, minimum; the states are referred to as S0, S1, S2, in FIG. **3**. The clock generator **17** produces an output CLKOUT, FIG. *3f*, on one of the control bus lines **13**. CLKOUT has the same period as Q1, but 50% duty cycle and beginning at the midpoint of Q1. This output is used for timing or synchronizing external elements of the system of FIG. **1**.

Internally, the microcomputer **10** executes one instruction per state time for most types of instructions, so five million instructions per second are executed. Of course, some instructions such as input/output, branch, call or table look-up require two or three state times. Assuming a sequence of single-state instructions such as add, load, store, etc., a new address is loaded into PC during each Q3 as seen in FIG. *3g*, then the ROM **14** is addressed during Q4 and Q1 so an instruction word output is produced from IR onto P-Bus starting in the next Q2 and continuing through Q3, as seen in FIG. *3h*. The ROM **14** access time is thus about 100 ns. If an external instruction fetch from memory **11** is used, the same access time applies. The instruction decoders ID1 and ID2 receive the instruction word from P-Bus during Q3 as seen in FIG. *3i*, and most of the decoder outputs #C are valid during Q1, although some fast controls are available in Q4. For direct addressing of the RAM, the address on bit-**9** to bit-**15** of P-Bus is immediately gated into the RAM decoder **15***b* when P-Bus becomes valid, but in either direct or indirect the RAM address is valid by the beginning of Q3 as seen in FIG. *3j*. For RAM read, the data output via **15***j* to D-Bus is valid on Q4, FIG. *3j*, and this data passes through the shifter S, FIG. *3k*, and is available as an ALU input during Q1, FIG. *3l*. The ALU controls #C are valid in Q2 and ALU output ALU-o is available during Q3. The accumulator Acc is loaded from ALU in Q4, FIG. *3m*.

It is thus seen that an ADD instruction, for example, for which fetch began at Q3 of the S0 state in FIGS. *3a–3m*, will be completed, i.e., the result loaded into Acc, in Q4 of state S2. There is substantial overlap of instruction execution. A new instruction fetch begins during Q3 of each state time, so execution of two more instructions have begun before one is finished.

Not shown in FIGS. *3a–3m* is the write-RAM function. The RAM **15** is always written into during Q2. Addressing the RAM is always during Q3, however. Thus, an instruction such as "store accumulator low" SACL is illustrated in FIGS. *3n* and *3o*. The RAM address is received from the instruction register via P-Bus on Q3 of S1 (assuming the SACL instruction was fetched beginning at Q3 of S0), and the write will not occur until Q2 of state S2. During the read slot, Q4 of S1, a refresh occurs for the addressed row of the RAM, then the same address stays until Q2 of state S2 for the write. The D-Bus is loaded from Acc during this same Q2, see FIG. *3n*.

If the accumulator must perform the saturate function in the overflow mode, i.e., OVM set to **1**, this will be performed after the load accumulator function of FIGS. *3m*. That is, for the ADD instruction of FIGS. *3a–3m*, the Acc is saturated during Q1 if the next state S3, so that when the accumulator is accessed by the following instruction it will be available to load the D-Bus on Q2.

When an instruction uses the data move function within the RAM **15**, the move operation occurs during Q1 as illustrated in FIG. *3o*. Also, if the increment loop counter function is performed for the auxiliary registers AR0 or AR1, the increment (or decrement) is executed in Q1. The T register, auxiliary registers AR0 or AR1, ARP latch, DP register and stack ST registers are each loaded during Q2 of any state time if these functions are included in the current instruction.

The bus interchange module BIM always executes a transfer from D-Bus to P-Bus beginning in Q2, if this function is defined by the instruction. The transfer from P-Bus to D-Bus by BIM is begun during Q4. The D-Bus is precharged on Q3 of every cycle, so no data can carry over on D-Bus through Q3 of any state, nor can data be loaded to or from D-Bus during Q3.

The program counter PC is incremented by the PCinc path during Q3 of each state time. That is, the load PC function of FIG. *3g* is the incremented value just generated.

Execution of a branch instruction is illustrated in FIGS. *3p–3r*. If the instruction loaded into the decoders ID1 and ID2 during Q3 of state S0 is a branch, the status decode SD bits from the previous instruction are valid during Q1 of S1 so the decision of branch or not is made at this point. Meanwhile, of course, another instruction fetch has begun so if the branch condition is met the instruction delivered to P-Bus during Q2 of S1 is used as the next address; if the condition is not met, however, this instruction is discarded. Assuming the condition is met, the branch address is loaded from IR via P-Bus to PC during Q3 of S1, and the new instruction delivered to IR and P-Bus in Q2 of S2 then decoded and executed beginning at Q3 of S2, FIG. *3r*.

A CALL instruction is executed in the same time sequence as a branch, seen in FIGS. *3p–3r*, except no SD evaluation is needed, and PC+1 is pushed to stack ST during Q3 of S1.

A return instruction RET is a two cycle instruction as illustrated in FIGS. 3*s*–3*u*. If the instruction loaded into the decoders ID1 and ID2 during Q3 of state S0 is RET, the instruction fetch which began with PC+1 and load PC in Q3 of S) is discarded and a pop stack function is performed in Q3 of S1 so the next instruction fetch is to the return address. The instruction fetched during Q4 of S1 is then decoded and executed beginning at Q3 of S2.

Input (or output) instructions are executed in two cycles as illustrated in FIGS. 3*v*–3*x*. Assume the opcode loaded into the decoder ID2 in Q3 of S0 is IN. The instruction fetched beginning at Q3 of S0 is not used; execution is inhibited by the decode of IN. The contents of PC at Q3 of S1 are saved until Q3 of S2 for the next instruction fetch; that is, PC is recirculated back to PC by the increment path, but no increment is performed. The controls #C produced from decode of IN are available for two states. The RAM address is loaded from P-Bus on Q3 of S1, seen in FIG. 3*y*, and the data input reaches D-Bus on Q4 of S1 and is written into RAM **15** during Q2 of S2. The DEN− control is active from Q4 of S1 through Q2 of S2 for the IN function. An OUT instruction is executed like IN except the RAM **15** is read during Q4 of S1 and the WE− control is active instead of DEN−.

A table look up instruction is executed as shown in FIGS. 3*aa*–3*cc*. The TBLR opcode is decoded beginning at Q3 of S0 and causes the Acc to be loaded via D-Bus to BIM in Q2 of S1, then PC is loaded via P-Bus from BIM in Q3 of S1 so the content of Acc is used as the next instruction fetch address. Meanwhile, execution of the instruction fetched beginning at Q3 of S0 is inhibited by preventing a ROM read control #RR from loading IR with the ROM **14** output, at Q2 of S1. The incremented contents of PC from Q3 of S0 are pushed to ST during Q3 of S1, then popped at Q3 of S2 as the next instruction address. The data fetched from ROM **14** (or memory **11**) using the address from Acc during Q4/S1 to Q1/S2 is loaded onto P-Bus during Q2 of S2 where it remains until Q4 of S2 at which time the BIM accepts the data from P-Bus and then transfers it to D-Bus on Q2 of S3, the next state. The destination address for RAM **15** loaded into decoder **15***b* from P-Bus by Q3 of S1 and remains for two states, so the RAM write occurring at Q2 of S3 will use the RAM address defined in the original TBLR opcode.

One of the problems inherent in manufacturing microcomputer devices is that of testing the parts to determine whether or not all of the elements are functional. In many microcomputers, the instruction words read from the internal ROM are not available on external busses and so the ROM cannot be checked in any way other than by executing all possible functions, which can be lengthy. The device of FIG. **2** allows the ROM **14** to be read out one word at a time using the interchange module as illustrated in FIGS. 3*ee*–3*hh*. A test mode, not part of the instruction set of Table A, is entered by holding the I/O ST− pin at above Vdd, for example **10**V, and holding RS− low, producing an input to the decoders ID1 and ID2 causing a ROM output function in which the ROM **14** is accessed every cycle and PC incremented as seen in FIG. 3*ee*. The P-Bus receives the ROM output, FIG. 3*ff*, but the opcodes are not loaded into the decoders ID1, ID2. Instead, the BIM accepts the opcodes from P-Bus on Q4 of each cycle and transfers to D-Bus on the next Q2, as seen in FIG. 3*hh*.

THE CHIP LAYOUT

In FIG. **4**, the microcomputer **10** of FIGS. **1** and **2** is illustrated in chip layout form. This is a top view of an MOS/LSI chip which is about 150 mils on a side. A major part of the area of the chip **10** is occupied by the memory including the ROM **14** and RAM **15** with their address decoders, and by the 16×16 multiplier M. The ROM **14** has associated with it an X address decoder **14**X and a separate Y address decoder **14***y* for instruction word output; twelve address bits are used to define one of up to 4096 16-bit words in the ROM **14**, although in this example only 1536 are on-chip.

The RAM **15** has an X address decoder **15***b*–*x* which selects 1-of-72 row lines, and a Y address decoder **15***b*–*y* and sense amplifiers **15***s* which select 1-of-2 column lines, so only eight bits are needed for the RAM select in this embodiment (eight bits could accomodate a 256 byte RAM).

The busses RA and D have twelve or sixteen bonding pads on the chip (total of twenty-eight) for connection to external, and the areas of the chip around these bonding pads seen in FIG. **4** are occupied by the buffers used for the ports. It will be noted that the RA bus is only used for output, so only output buffers are needed for this port, while the D-Bus requires tri-state output buffers as well as input buffers.

The multiplier M, shifter S, ALU, accumulator Acc and auxiliary registers AR0, AR1 on the chip **10** of FIG. **4** comprise a 32-bit wide "strip" which is an array of rows (parallel to control lines #C) and columns (parallel to metal bus lines such as D-Bus and P-Bus and ALU and register bits) containing all of the 16-bit and 32-bit registers, ALU bits, and the like circuitry associated with the D-Bus and related control lines #C. As set forth in U.S. Pat. No. 4,402,044 issued to McDonough and Guttag, assigned to Texas Instruments, an important feature is that the 32-bit ALU and its associated 32-bit Acc registers, the two 16-bit AR registers, the shifter S, and the bus interchange BIM as described above are laid out on the MOS/LSI chip **10** in a regular strip pattern as seen in FIG. **4**. Other circuitry connected to the D-Bus and the ALU-b input and having controls #C shared by sixteen or thirty-two bits may also be in the strip, such as AR and BIM. The Acc and the ALU each contain thirty-two bits or stages which are laid out in a regular pattern like memory cells, the bits arrayed and aligned horizontally and vertically as seen in FIG. **4**. D-Bus and P-Bus of FIG. **2** are each sixteen parallel metal strips on top of the cells of the ALU and registers, and all of the dozens of control lines #C are horizontal polysilicon lines typically used as the control gates for transistors in the ALU and its associated registers and like circuitry. This layout arrangement is advantageous because the multiplier ALU and registers, and perpendicular control lines #C and metal busses fit in an array with virtually none of the wasted space used merely for routing conductors in conventional contruction of microprocessors. Metal bus lines such as P-Bus and D-Bus and control lines #C are in large part routed over functional regions or cells of the chip in the strip rather than over unused silicon, and many 90 degree turns are produced inherently at functional cells rather than in conductor routing. In the prior devices, the controls, the registers, the ALU, etc. where islands of circuitry connected by busses or conductors. The enlarged view of FIG. **4***a* shows a small part of the strip, two-bits wide, illustrating the metal bus

lines and the polysilicon control lines #C for an N-channel silicon gate MOS device made generally by a single-level polysilicon process according to U.S. Pat. No. 4,055,444, assigned to Texas Instruments. Various contacts (not shown) would be made within each register bit or stage from metal to silicon or to polysilicon. It is significant to note that many of the connecting lines from registers to busses illustrated in FIG. **2** are not physically lines or elongated conductors at all but instead are merely metal-to-silicon or metal-to-poly contact areas along the metal bus lines of FIG. **4***a*. That is, routing of 16-bit or 32-bit sets of parallel conductors is minimized by the strip feature, and the size of the chip **10** is reduced. All busses are not needed in any one part of the strip, and thus the pitch or maximum width of cells of the strip is minimized since the the metal-to-metal spacing is a critical limiting factor in bit density.

The internal program of the microcomputer **10** may be modified at the gate level mask in making the chip. The macro code or program in the ROM **14** is defined by a single mask in the manufacturing process as set forth for example in U.S. Pat. Nos. 3,541,543, 4,208,726 or 4,230,504, assigned to Texas Instruments. By rewriting this user or macrocode, keeping the instruction set defined by **ID1** and ID2 the same, a wide variety of different functions and operations are available.

ARITHMETIC LOGIC UNIT

A detailed schematic diagram of one bit of the 32-bit ALU is shown in FIG. **5***a*. The ALU operates under control of six of the #C commands from the instruction decode **ID1**, these commands being labelled #AUM-**0**–#AUM**4** (valid on Q2) and #AUAB (valid on Q1). The ALU-a input, inverted, is on line AUa and the ALU-b input inverted, is on line AUb, both being valid on Q1, one from Acc and the other from the shifter S or P register. The ALU output is at line AUc, valid on Q4, representing one of the inverted 32-bit parallel output ALU-o to Acc. Table B shows the function produced by operation of the ALU for various combinations of the six #C commands. This ALU is generally the same as U.S. Pat. No. 4,422,143, issued to Karl M. Guttag, assigned to Texas Instruments. Propagate and generate nodes AUp and AUg are precharged on Q1 and conditionally discharged by transistors AUd controlled by the ALU-a input, transistor AUe controlled by the ALU-b input and its complement, and transistors AUf controlled by the #AUM0–#AUM3 commands, according to the functions of Table B. A carry-out node AUh and a carry-in node AUi for each bit are coupled by a propagate-carry transistor AUj controlled by a line AUk which is the propagate node AUp inverted. The carry-out node AUh is precharged on Q1 and conditionally discharged via transistor AUm which is controlled by a NOR gate having the generate node AUg as one input and the absolute value command #AUAB as the other, so if #AUAB is 1 the transistor AUm is off and carry-out bar is always 1, meaning no carry or absolute value. If #AUAB is 0, the generate signal on AUg controls. The inverted propagate signal on AUk is one input to an Exclusive Nor circuit AUn with static load AUq; the inverted carry-in bar of line AUi is the other input to the Exclusive NOR, resulting in an output AUr which inverted is the ALU output AUc. The carry-in bar node AUi is made unconditionally 0 when control #AUM4 is high for logic functions OR, AND and EXOR, so this input to circuit AUn is unconditionally 1, but for ADD, SUB, etc., the control #AUM4 is 0 and the carry-in from the node AUu of the next low-order bit of the ALU controls.

THE SHIFTER S

Referring to FIG. **5***b*, the shifter S includes a 16-bit input Si, a shift matrix Sm, a shift controller Sc, and a 32-bit output So going to the ALU-b input. The input Si is connected to receive the D-Bus at all times and to drive lines Sf in the matrix Sm through high level buffers. If no shift is to be performed, a line Sg is high, turning on all sixteen of the transistors Sh for this line, so the 16-bit data on lines Sf will appear on the sixteen right-most output lines So via diagonal lines Sj. All of the lines Sf are precharged on Q3 via thirty-two transistors Sk then conditionally discharged by the input Si. The sign bit is extended by detecting the MSB bit-**0** of the input Si by the line Sm. A gate Sn also receives a #NEX not extend command from **ID1** (one of the controls #C) to kill the sign extension for certain instructions of Table A. Based on the incoming sign bit Sm and #NEX, the gate Sn generates an extend command on line Sq to transistors Sq'. The transistors Sq' in series with lines Sr conditionally discharge the nodes Ss on lines Sf through transistors St. The control Sc is a 1-of-16 decoder or selector which receives the bits **4**–**7** of the instruction word from the P-Bus on 4-bit input Sp during Q3 and activates one of the sixteen lines Su; the lines Su are precharged in Q3 via transistors Sup and conditionally discharged during Q4 via transistors Sud and Sc'. The controls for the shifter S consist of the 4-bit value on Sp (the SSSS field of the ADD instruction, for example) defining the number of positions of left shift, and controls on lines #C for negating sign extension, etc. Since the data is usually in two's complement, the sign bit is extended to all bits to the left of the most significant data bit. The sign bit is 0 for positive and 1 for negative. If the shift is to be seven bits, for example, the seventh line Su stays high on Q4 and all others go low. This turns on all transistors Sh and St in the seventh row and all other transistors Sh and St are off. The 16-bit data coming in on lines Si thus moved via transistors Sh and lines Sj to a position on lines So seven bits to the left of the zero shift (right-most) position, and zero-filled to the right due to the prcharge Sk. To the left, the sign bit will stay 0 is the bit-**0** is low, but if bit-**0** is 1 then Sq is high, transistors Sq are on, allowing all bits to the left to discharge.

BUS INTERCHANGE MODULE

The bus interchange module BIM, shown in detail in FIG. **5***c*, consists of sixteen identical stages, only one of which is illustrated. Each stage has two clocked inverters Ia, with no feedback loop since data is not held in BIM longer than about half a state time. Input node Ib is connected to the respective bit of P-Bus via one of sixteen transistors Ic driven by a control bit #BIFP valid on Q4. The D-Bus is connected to the input node Ib via transistors Id driven by the control bit #BIFD (Bus Interchange From D) from decoder **ID1** valid on Q2. The output node Ie is connected to the P-Bus by a push-pull stage including transistors If and Ig, and a transistor Ih driven by a control bit #TP, valid during Q2 and Q3. Likewise, output node Ie is coupled to the D-Bus via a push-pull stage having driver transistors Ii and Ij, and a transistor Ik driven by a control bit #BITD valid on Q2 and Q4. The transistors Ig and Ij are driven by node Im at the output of the first inverter Ia, providing a push-pull output. Data is transferred

from D-Bus to nodes Ib, Im, Ie on Q2, and then from these nodes to P-Bus on Q4. Similarly, data is transferred from P-Bus to nodes Ib, Im, Ie on Q4, and then from these nodes to D-Bus on Q4 on the next Q2.

THE MULTIPLIER

Referring to FIG. 5*d*, a schematic representation of the multiplier M and its T and P registers is shown, and corresponding detailed circuit diagrams are shown in FIGS. 5*e*, 5*f*. The 16-bit output of the T register is applied to a set of eight Booth's decoders Mb which produce eight sets of outputs Mc, each set including five functions: shift or no shift, and add, subtract or zero. A set of eight banks of 17-it static carry-feed-forward adders Ma-1 to Ma-8 receive the Mc inputs when the T register is loaded, and so a significant part of the multiplication function is initiated before the MPY instruction is executed. The adders Ma-1 to Ma-8 are static in that no clock Q1–Q4 is needed to cause them to operate. Each stage of each level or bank includes a control section Mm responsive to the decoder outputs Me, and the control section feeds an adder. Level Ma-2 uses half adders and levels Mc-3 to Mc-8 use full adders. The first level Mc-1 does not need an adder because there is no partial product from the prior stage, so it has only the control section. When the MPY instruction is decoded, on Q4 the second operand is applied to the static adders from D-Bus by 16-bit input Mi. As each level of the eight levels of adders Ma-1 to Ma-8 calculates the sum, the partial product is fed forward via lines Mf to the next higher level, except for the two LSBs of each level which are fed to the dynamic adders Md via lines Me. When the static adder array settles, the 17-bit output Mg from the level Ma-8 plus the seven lower level 2-bit LSB outputs Me, is applied to a carry-ripple adder MD(31-stages) to perform the final carry evaluation, producing a 31-bit product in two's complement notation. The 31-bits are sign extended to obtain a 32-bit product in the product register P.

Booth's 2-bits algorithm reduces the number of adder stages to about half the number otherwise required. When performing multiply in the classic pencil and paper method, the right or LS digit of one operand is multiplied by the other operand to produce a partial product, then the next digit is multiplied to produce another partial product which is shifted one digit with respect to the first. Booth's algorithm gave a method of multiplying in binary which allowed two bits to be treated each time, instead of one. Thus, level Ma-1 multiplies the two LSBs of T reg times all bits of D-Bus, producing a partial product Me and Mf. The second level Ma-2 multiplies the next two bits of T reg to D-Bus, adds the partial product Mf from Ma-1, and generates a new partial product Mf and two more bits Me because this operation shifts two bits each level.

In FIG. 5*e*, one of the eight decoders Mb is shown, along with two bits of the T register. The T register stage consists of two inverters Ia with a recirculate transistor Rc clocked in Q4. The stage is loaded via transistor Ta by a #LT command from ID1 occurring on Q2 during an LT instruction. The outputs of two stages of the T register and complements are applied by lines To and Tc to one Booth decoder Mb. The decoder consists of four logic circuits, each having a static load Ba, Bb, Bc or Bd and a pattern of transistors Be with the lines To and Tc applied to the gates. Two of the terms have 1 or 0 fixed in the gates by lines Bf. Outputs Mc-1 and Mc-2 represent no-shift and shift commands and come from the logic stages Be and Bd. Outputs Mc-4 and Mc-5 are true and complement outputs from load Ba of the first of the logic circuits, and these represent add and subtract commands. The output Me-3 from Bb is the zero command.

The first level Ma-1 of the static adders is simpler than the higher levels in that only the D-Bus input Mi and the inputs Mc are involved, with no partial product. Two stages of this first level are seen in FIG. 5*g*, along with two of the seventeen stages of level Ma-2 and level Ma-3. The control sections Mm are all the same on all levels. Note that no elements are clocked.

The decoders Mb and control sections Mm with controls Mc define the Booth's two-bits at a time algorithm which reduces circuitry and increases speed by a factor of two. When two bits are interrogated successively, the only operations required are add, subtract, do nothing or shift by one bit. Considering the input from T as one operand, and from D-Bus as the other, the following table describes the function

Ti + 1	Ti	(Ti − 1)	Function	Partial Product
0	0	(0)	Do nothing	K + O
0	0	(1)	Add D	K + D
0	1	(0)	Add D	K + D
0	1	(1)	Shift D & Add	K + 2D
1	0	(0)	Shift D & Add	K − 2D
1	0	(1)	Subtract D	K − D
1	1	(0)	Subtract D	K − D
1	1	(1)	Do nothing	K + O

An example of multiplication using Booth's two bit algorithm is as follows:

D = 001101 (= 13 decimal)
T = 100111(0) (= −25 decimal)

	Ti+1	Ti	(Ti−1)	
000000000000 — — —	1	1	(0)	→ K − D
111111(10011) — — —	0	1	(1)	→ K + 2D
000(001101)0 — — —	1	0	(0)	→ K − 2D
1(110011)0				
111010111011				

(= −325 decimal)

In the control sections Mm the inputs Mi from the D-Bus are controlled by a transistor Mm-1 and control Mc-1, not shift. The Mi input for the adjacent bit is gated in by transistor Mm-2 and the Mc-2 shift command, providing the "2D" function as just described. The zero is provided by transistor Mm-3 and zero control Mc-3 which results in mode Mm-4 being connected to Vcc (zero in two's complement). The carry-in from

the prior stage is on line Mm-5, and the partial product from the prior stage is on line Mm-6. The add or subtract control is provided by transistors Mm-7 controlled by the Mc-4 and Mc-5 add and subtract commands. The full adder includes logic gate Mn-1 receiving the outputs of the control section, as well as gates Mn-2 and the exclusive Nor Mn-3, producing a sum on line Mn-4 and a carry on line Mn-5. Speed is increased by using carry feed forward instead of carry ripple on the same level. Level Ma-1 has no partial product or sum Mm-6 from the prior stage, nor carry-in Mn-5, so the adder is not needed, only the control, producing a sum (a difference) at mode Mn-8 and no carry. The second level Ma-2 is a half adder since no carry feed forward is received from Ma-1.

One of the adder stages of the 31-stage ripple-through carry adder is shown in FIG. 5*f*, along with one stage of the P register. The adder stage receives two inputs Me, gated on Q1 or Q3 by transistors Md1. The six LSBs of adder Md have their inputs gated in on Q1 because the static array levels Ma-1, Ma-2 and Ma-3 will have settled and outputs Me will be valid at this point, so the add and ripple through in Md can begin, although the outputs Mf are not yet valid. Thus, the more significant bits are gated on Q3 at transistors Md1. A carry input Md2 from the next lower-significant stage is applied to one input of an exclusive NOR circuit Md3, and to a carrry output gate Md4 which produces a carry output Md5 to the next higher stage. A propagate term is generated from the inputs Me and the carry-in by logic gate Md6, and a carry generate term by a logic gate Md7 with Md4. The same output Md8 is connected by line Md9 to the input of the P register stage, gated by #LPR (load P Reg) from ID1 on Q4 by transistor Pa. The P register stage consists of pair of inverters Ia and recirculate transistor Rc gated on Q2. The output is applied to the ALU-b input on Q1 by gate Pb with #NRPR (not read P Reg) from ID1 as one input, along with an inverter Pc. Transistor Pd precharges the ALU-b input on Q4.

The timing of the multiplier operation is illustrated in FIGS. 3*jj* to 3*mm*. On Q2 of So, the register is loaded and outputs Mc from the Booth's decoder become valid. The Mi inputs from D-Bus are valid at Q4 of S1, assuming the MPY instruction is valid in decoder ID1 at Q3 of S1. The lower bits of the dynamic adder Md are loaded with Me on Q1 of S2, via Md1, and the carry begins to ripple through the lower of the 31-bits, then this continues in Q3 of S2 through the output Mf of the upper levels, so P register is loaded on Q4 of S2 via Pa, where the data remains until loaded to ALU-b on Q1 of a succeeding cycle.

THE RAM

The cell used in the RAM **15** is a pseudo-static 6-transistor cell as seen in FIG. 5*g*. This cell differs from the traditional 6-transistor static cell in that refresh transistors **15***m* are used in place of polysilicon resisters or depletion transistors used as load impedences. The implanted resistors or depletion devices are larger and interpose process complexities. The storage nodes **15***n* are connected through cross-coupled driver transistors **15***p* to ground; one transistor **15***p* is on and the other off, storing a 1 or 0. Read or write is through access transistors **15***q* to data and data bar lines **15***r*, with gates of the transistors **15***q* driven by a row address line **15***s*. Refresh is accomplished when the refresh line **15***t* is pulsed high allowing the node **15***n* which is at 1 to be charged back up to a level near Vdd, while the 0 node **15***n* will conduct the pulse of current to ground through the on transistor **15***p*. The row address on **15***s* is delayed slightly from the refresh line **15***t* so that both won't begin at the same time. In the timing sequence of the FIGS. 3*a*–3*e*, particularly FIGS. 3*j* and 3*o*, the cell of FIG. 5*j* is read in Q4 of any cycle, or written into on Q2.

Referring to FIG. 5*k*, several of the cells of FIG. 5*g* are shown in a column. The data and data bar lines **15***r* are precharged to Vdd-Vt on Q1 and Q3 by transistors **15***u*. The refresh address on lines **15***t*-0, **15***t*-1 and **15***t*-2, etc., occur in sequence, one-at-a-time, generated by a ring counter; for example, if the RAM **15** is partitioned in 64 rows, then a 64 bit ring counter generates one refresh address bit each state time, refreshing the entire array once each 64 states. The refresh pulse occurs on a line **15***t* during Q3, while transistors **15***u* precharge and equallize the data and data bar lines. A row address on a line **15***s* might begin to come up to 1 during the later part of Q3 since read access is in Q4, so the sizes of the transistors are such that nodes **15***n* will not be both forced to Vdd-Vt when transistors **15***m* and **15***q* are all turned on. The on transistor in the pair **15***p* will hold the 0 node lower than the 1 node. After the refresh pulse on **15***t* goes low, for a cell addressed for both read and refresh in Q3, the delayed Q3 address line stays high momentarily to assure that the zero-going line **15***r* will discharge at least slightly through **15***q* and **15***p* for the 0 side. Then a bistable sense circuit including cross-coupled transistors **15***v* is activated by transistor **15***w* having Q4 on its gate (delayed slightly to make sure Q3 has gone to zero). This flips the data and data bar lines to full logic level, after which the column access transistors **15***y* are activated for the addressed column and data can be read out onto the D-bus. Internal shift is implemented by lines **15***x* connecting nodes **15***z* to adjacent column lines **15***r* via transistors **15***z* activated by a RAM move command #RM from decoder ID1, occuring on Q4. The data is held until Q2 of the next cycle (after Q1 precharge of all data and data bar lines **15***r*) before being applied to the adjacent column for this move operation. Meanwhile, the row address may be incremented by 1; i.e., the next higher line **15***t*-1, etc., goes high so on Q2 the data is written into the next higher location.

The sixteen bits of the RAM **15** are arranged as seen in FIG. 5*i*, with column lines (data and data bar lines) **15***r* running vertical and row lines **15***s* horizontal. The RAM is only 32-columns wide, so the column select **15***y* is merely one-of-two, even or odd. There are in this embodiment 144 row lines **15***s*. The LSB of the address **15***b* to the RAM is the column address, even or odd. To implement the data move operation, on even columns the LSB of the address buffer is complemented, but for odd columns the LSB of the address buffer is complemented and also the row decoder output on line **15***s* is incremented.

TABLE A

THE INSTRUCTION SET

Source Code	Object Code-Binary	No. of Cycles	No. of Words	DESCRIPTION
ADD	0000SSSSIAAAAAAA	1	1	Add word at RAM address A (shifted S places to left) to Acc; Result to Acc
SUB	0001SSSSIAAAAAAA	1	1	Subtract word at address A (shifted S places to left) from ACC; Result to Acc
LAC	0010SSSSIAAAAAAA	1	1	Load Acc with word at address A (shifted S places to left)
SAR	00110RRRIAAAAAAA	1	1	Store contents of Aux Reg number R at location defined by A
LAR	00111RRRIAAAAAAA	1	1	Load Aux Reg R with value at location A
IN	01000PPPIAAAAAAA	2	1	Input value on external data bus, store in A
OUT	01001PPPIAAAAAAA	2	1	Output value at address A to ext data bus
SACL	01010XXXIAAAAAAA	1	1	Store low order Acc bits in location A, shifted X places left
SACH	01011XXXIAAAAAAA	1	1	Store high order Acc bits in location A, shifted X places left
ADDH	01100000IAAAAAAA	1	1	Add value at address A to high order Acc bits; result to Acc; no shift
ADDS	01100001IAAAAAAA	1	1	Add Acc to value at address A sign extension suppressed
SUBH	01100010IAAAAAAA	1	1	Subtract value at address A from high order Acc bits; result to Acc; no shift
SUBS	01100AAIAAAAAAA	1	1	Subtract with sign extension suppressed
SUBC	01100100IAAAAAAA	2	1	Conditional subtract for divide; left shift ALu output and conditional +1
ZALH	01100101IAAAAAAA	1	1	Zero Accumulator and Load High under half of Acc with addressed data
ZALS	01100110IAAAAAAA	1	1	Zero Accumlator and Load with sign Extension Suppressed
TBLR	01100111IAAAAAAA	3	1	Table Read; read data from program memory using Acc as address; store in RAM
MAR	01101000IAAAAAAA	1	1	Modify Auxiliary Registers
DSHT	01101001IAAAAAAA	1	1	Data Shift; value defined by A shifted to A+1
LT	01101010IAAAAAAA	1	1	Load T Reg with value defined by A
LTD	01101011IAAAAAAA	1	1	Load T Reg with value A; shift A to A+1; Acc+Preg Acc
LTA	01101100IAAAAAAA	1	1	Load T Reg with value defined by A; Acc+Preg Acc
MPY	01101101IAAAAAAA	1	1	Multiply T times value defined by A, result to P Reg
LDPK	01101110DDDDDDDD	1	1	Load page reg for data memory with 8-bit constant D
LDP	01101111IAAAAAAA	1	1	Load DP reg with value whose address is at A
LARK	01110RRRDDDDDDDD	1	1	Load Auxiliary Register R with 8-bit constant D; MSB's Zero
EXOR	01111000IAAAAAAA	1	1	Exclusive OR Acc with value defined by A; result to LSBs of Acc; zero MSB's
AND	01111001IAAAAAAA	1	1	AND LSB's of Acc with value defined by A; result to LSB's of Acc; (zero)-(MSB's)
OR	01111010IAAAAAAA	1	1	OR LSB's of Acc with value defined by A; result to Acc; (zero)-(MSB's of Acc)
LST	01111011IAAAAAAA	1	1	Load Status with 16-bit value found at location A in RAM
SST	01111100IAAAAAAA	1	1	Store Status in location defined by 8-bit address A in RAM
TBLW	01111101IAAAAAAA	3	1	Table Write; write the value at Ram address to program memory address in Acc
LACK	01111110DDDDDDDD	1	1	Load Accumulator with 8-bit constant from instruction word
NOOP	0111111110000000	1	1	No-operation
DINT	0111111110000000	1	1	Disenable Interrupt-masks interrupt input INT
EINT	0111111110000010	1	1	Enable Interrupt-unmasks interrupt input INT
ABS	0111111110001000	1	1	Absolute Value operation; if Acc 0, Acc Acc; else Acc Acc
ZAC	0111111110001001	1	1	Clear Accumulator; zeros Acc
RAMV	0111111110001010	1	1	Reset Overflow Mode
SAMV	0111111110001011	1	1	Set Overflow Mode
CALLA	0111111100001100	2	1	Call subroutine indirect
RET	0111111110001101	2	1	Return from Subroutine
PAC	0111111110001110	1	1	Load accumulator with contents of P Reg
APAC	0111111110001111	1	1	Add accumulator to contents of P Reg; Result to Acc
SPAC	0111111110010000	1	1	Subtract contents of P reg from Accumulator; Result to Acc
MPYK	100CCCCCCCCCCCC	1	1	Multiply by constant C
BARNZ	11110100XXXXXXXX	2	2	Branch if Loop Counter Not Zero, to location defined PC+1
BV	11110101XXXXXXXX	2	2	Branch if Overflow Bit in ST is 1
BIOZ	11110110XXXXXXXX	2	2	Branch if IO Bit in ST (from IO pin) is 1
CALL	11111000XXXXXXXX	2	2	Call Subroutine
B	11111001XXXXXXXX	2	2	Unconditional Branch to location W at PC+1
BLZ	11111010XXXXXXX	2	2	Branch if Acc is less than zero
BLEZ	11111011XXXXXXXX	2	2	Branch if Acc is less than or equal to zero
BGZ	11111100XXXXXXXX	2	2	Branch if Acc is greater than zero
BGEZ	11111101XXXXXXXX	2	2	Branch if Acc is greater than or equal to zero
BNZ	11111110XXXXXXXX	2	2	Branch if Acc is not zero
BZ	11111111XXXXXXXX	2	2	Branch if Acc is equal to zero

TABLE B

ALU FUNCTIONS

	Control Code						Propagate	Generate	
	#AUM0	#AUM1	#AUM2	#AUM3	#AUM4	#AUMB	Node	Node	Output
Add	0	1	1	0	0	0	A+B	AB	$A+B+C_{in}$
Subtract	1	0	0	1	0	0	A+B	AB	$A+B+C_{in}$
Load Acc	0	1	0	1	1	0	B	X	B+1=B
Exclusive Or	1	0	0	1	1	0	A+B	X	A+B+1=A+B
Or	1	0	0	1	1	0	AB (=A+B)	X	A+B+1=A+B
And	0	1	1	1	1	0	A+AB	X	(A+AB)+1=A+B=A
Abs. Value	0	0	1	1	0	1	A	0	$A+C_{in}$

What is claimed is:

1. A microcomputer formed in a single integrated circuit comprising:

an arithmetic/logic unit having data input and data output;

a data memory having an address input and having data input/output means;

data bus means coupled to the data input and data output of the arithmetic/logic unit and coupled to the data input/output means of the data memory, the data bus means transferring multi-bit data;

a program memory having an address input and having an instruction output, the program memory storing instruction words;

program address means having an input and including incrementing means; said program address means having an output connected to said address input of the program memory means;

control means for generating controls in response to instruction words; the controls defining operation of the arithmetic/logic unit, transfer of multi-bit data to and from the data bus means, and operation of said program address means;

program bus means coupling said instruction output to an input of said control means, and to said input of said program address means, the program bus means transferring multi-bit information;

timing means for establishing repetitive operating cycles wherein during one of said operating cycles multi-bit data is transferred from the data memory to the data input of the arithmetic/logic unit via said data bus means, the program address means applies an address to the address input of the program memory, and the control means receives an instruction word from the instruction output via said program bus means;

bus interchange means within said integrated circuit and coupled to said data bus means and to said program bus means for

(a) transferring said multi-bit data from the data bus means to the program bus means and for transferring said multi-bit data from the program bus means to said input of said program address means, both during one of said operating cycles, and

(b) transferring said multibit information from said instruction output of said program memory to said program bus means and transferring said multibit information from said program bus means to said data bus means, both during one of said operating cycles,

(c) all said transferring being in response to controls received from said control means generated from a single one of said instruction words.

2. A device according to claim **1** wherein:

after transferring said multi-bit data and multi-bit information in response to said single one of said instruction words via said bus interchange means,

multi-bit information from the program bus means is valid on said data bus means during one part of said one of said operating cycles and

multi-bit data from the data bus means is valid on said program bus means during another part of a different one of said operating cycles.

3. A device according to claim **2** wherein the bus interchange means receives said multi-bit data from the data bus means only during said one part for transfer to the program bus means, and receives said multi-bit information from the program bus means during said another part for transfer to the data bus means.

4. A device according to claim **1** wherein the data output of the arithmetic/logic unit is coupled to an accumulator and an output of the accumulator is coupled to the data bus means.

5. A device according to claim **4** wherein an output of the accumulator is coupled to a data input of the arithmetic/logic unit.

6. A microcomputer formed in a single integrated circuit comprising:

an arithmetic/logic unit having data input and data output;

a data memory having an address input and having data input/output means;

data bus means coupled to the data input and data output of the arithmetic/logic unit and coupled to the data input/output means of the data memory, the data bus means transferring multi-bit data;

a program memory having an address input and having an instruction output, the program memory storing instruction words;

program address means having an input and including incrementing means; said program address having an output connected to said address input of the program memory means;

program bus means separate from the data bus means and coupled to said instruction output and to said input of said program address means, the program bus means transferring multi-bit information;

control means having an input coupled to receive instruction words from said program bus means, said control means generating sets of controls in response to the instruction words; the sets of controls defining operation of the arithmetic/logic unit, transfer of multi-bit data to and from the data bus means, transfer of multibit information to and from the program bus means, and operation of said program address means;

timing means for establishing repetitive operating cycles wherein during one of said operating cycle multi-bit data is transferred from the data memory to the data input of the arithmetic/logic unit via said data bus means, the program address means applies an address to the address input of the program memory, and the control means receives an instruction word from the instruction output via said program bus means;

bus interchange means within said integrated circuit and coupled to said data bus means and to said program bus means, the bus interchange means including:

(a) means for transferring said multi-bit data from the data bus means to the program bus means and for transferring said multi-bit information from the program bus means to said data bus means,

(b) said means for transferring and said control means operating in response to one of said instructions words to transfer multi-bit data from the data bus means via said bus interchannge means to said input of the program address means, in one of said operating cycles,

(c) said means for transferring and said control means operating in response to a given instruction word to transfer multi-bit information from said instruction output of said program memory via said bus interchange means to said data bus means, in one of said operating cycles.

7. A microcomputer according to claim **6** wherein said one instruction word is the same as said given instruction word.

8. A microcomputer according to claim 6 including address and data bus means external to said integrated circuit and coupled to said address bus means and to said data bus means, and program and data memory means external to said integrated circuit coupled to said address and data bus means.

9. A microcomputer according to claim 8 wherein said address and data bus means external to the integrated circuit include an address bus and a data bus.

* * * * *

Exhibit “U”

#12D

TURNER, B

NANO-001/05US
N0765-2008

7/30/97

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on July 3, 1997.

Date: 7-3-97 By: Patricia K. Parry
Patricia K. Parry

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	Examiner: D. Eng
Charles H. Moore et al.	
Serial No. 08/484,918	Art Unit: 2315
Filed: June 7, 1995	
For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK	AMENDMENT Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Amendment is being submitted in response to the Office Action dated **April** 3, 1997 in the above-identified patent application.

IN THE CLAIMS

Please amend claim 73 as follows:

73 (Twice Amended). A microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and [including] being constructed of a second plurality of electronic devices, thus varying the [operating characteristics] processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of [transistors] electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said

integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation.

REMARKS

The above changes to the language of claim 73 clarify that claim and eliminate an inadvertent lack of antecedent basis problem in the former wording of the claim.

Claims 19-21, 65-67 and 72-79 were rejected under 35 U.S.C. § 103 as unpatentable over Magar, U.S. Patent 4,503,500. Shortly before issuing the Office Action, the Examiner had called to indicate that certain claims were allowable over the prior art, but when the undersigned attorney returned the Examiner's call, it was indicated that new prior art had been found and that a new action would be forthcoming. It is assumed that the Magar reference relied on is that new prior art. A review of the Magar reference shows that it is apparently no more pertinent than prior art acknowledged in the application, in that the clock disclosed in the Magar reference is in fact driven by a fixed frequency crystal, which is external to the Magar integrated circuit.

The clock gen circuit shown at the lower right hand edge of Fig. 2a in the Magar patent is of the same general type as shown at 434 in Fig. 17 of the present application, but depicted differently in that it shows the clock gen circuit portion which is on the semiconductor substrate, while Fig. 17 shows the external crystal at 434, connected to I/O interface 432 in the present invention. The crystal clock 434 is thus used in the invention for synchronizing I/O timing with the outside world, while the ring counter variable speed clock 430 also shown in Figure 17 is used for generating on-chip clock signals. The clock 430 is an example of the oscillator recited in the claims, the clock rate of which varies in the same way as a function of one or more device parameters associated with the integrated circuit substrate.

The definitive statement that the clock gen circuit in Fig. 2a in the Magar patent is equivalent to the "conventional crystal clock" 434 in Fig. 17 of the present application is at col. 15, lines 26-41 of Magar:

> "The chip 10 includes a clock generator 17 which has two external pins X1 and X2 to which a crystal (or external generator) is connected. The basic crystal frequency is up to 20 MHz and is represented by a clock 0 of Fig. 3a. This clock 0 has a period of 50 ns, minimum, and is used to generate for quarter-cycle clocks Q1, Q2, Q3 and Q4, seen in FIGS. 3b-3e, providing the basic internal timing for the microcomputer chip 10. A set of four quarter cycle clocks Q1 to Q4 defines one machine state of time of 200 ns., minimum; the states are referred to as SO, S1, S2 in FIG 3. The clock generator produces an output CLKOUT, Fig. 3f, on one of the control bus lines 13. CLKOUT has the same period as

Q1, but 50% duty cycle and beginning at the midpoint of Q1. This output is used for timing or synchronizing external components of the system of FIG. 1."

This description in Magar should be contrasted with the following detailed description of an embodiment of the present invention, as shown in Fig. 17, at explained at page **32,** lines **3-29:**

"Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor 50 provides a dual-clock scheme as shown in Figure 17, with the CPU 70 operating asynchronously to I/O interface **432** forming part of memory controller 118 (Figure **2)** and the I/O interface **432** operating synchronously with the external world of memory and I/O devices. The CPU 70 executes at the fastest speed possible using the adaptive ring counter clock **430.** Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor 50 for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface **432,** speed of which is controlled by a conventional crystal clock **434.** The interface **432** processes requests for memory accesses from the microprocessor 50 and acknowledges the presence of I/O data. The microprocessor 50 fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. By decoupling the variable speed of the CPU 70 from the fixed speed of the I/O interface **432,** optimum performance can be achieved by each. Recoupling between the CPU 70 and the interface **432** is accomplished with handshake signals on lines **436,** with data/addresses passing on bus **90,** 136."

From these two quotations, it is clear that the element in Fig. 17 missing from Fig. 2a in Magar is the ring counter variable speed clock 430, and that Magar is merely representative of the "most microprocessors" acknowledged as prior art in the above description from the present application, which prior art microprocessors use a "conventional crystal clock." Because the variable speed clock is a primary point of departure from the prior art, independent claims 19, 65, **73** and 78 all recite a system including a variable speed clock or a method including using a variable speed clock. In light of the prior art, of which Magar is a good example, Applicants are entitled to claims of this scope. Dependent claims 20, 66, 74 and 79 further recite a second clock, exemplified by the crystal clock **434** in Fig. 17.

Contrary to the Examiner's assertion in the rejection that "one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock vary together due to manufacturing variation, operating voltage and temperature of the IC", one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock *do not* vary together due to manufacturing variation, operating voltage and temperature of the IC in the Magar microprocessor, as taught in the above quotation from the reference. This is simply because the Magar microprocessor clock is

frequency controlled by a crystal which is also external to the microprocessor. Crystals are by design fixed-frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The Magar microprocessor in no way contemplates a variable speed clock as claimed.

In making the rejection based on Magar, the examiner appears to be confusing the multiple uses and meanings of the technical term "clock." A clock is simply an electrical pulse relative to which events take place. Conventionally, a CPU is driven by a clock that is generated by an crystal. The crystal might be connected directly to two pins on the CPU, as in Magar, and be caused to oscillate by circuitry contained in the CPU with the aid of possibly other external components. Alternatively, the crystal may be contained in a package with the oscillation circuitry, the packaged component thus called an oscillator, and connected to one pin on the CPU as in Edwards et al., U.S. Patent 4,680,698.

While an oscillator may be a clock, a clock is not usually an oscillator. An oscillator must exist someplace in the circuit from which a periodic clock is derived. In both cases, the crystal (or the entire oscillator in the second case) is external to the CPU, and the output of the oscillator circuitry is a "clock." This clock is typically modified to produce additional required clock signals for the system. The many clock signals are sometimes created by circuitry called a "clock generator." For example, see Magar, Fig. 2a. The "clock gen" connects to a crystal at external pins X1 and X2 and generates clock signals for the system Q1, Q2, Q3, Q4 and CLKOUT. Other cited reference have similar examples, see Palmer, U.S. Patent 4,338,675, Fig. 1, item 24; Pohlman et al., U.S. Patent 4, 112,490 Fig. 1, item 22. All these systems operate at a frequency determined by the external crystal. The single, fixed, oscillation frequency of the crystal is determined by how the device is manufactured, i.e., how the crystal is cut and trimmed, and other factors. Crystals are used precisely for this purpose; they oscillate at a given frequency within a tolerance determined by their manufacture. Because of the cutting and trimming required, and that the crystal slice is typically suspended by two wires to allow it to freely oscillate, crystal oscillators have never, to Applicants' knowledge, been fabricated on a single silicon substrate with a CPU, for instance. Even if they were, as previously mentioned, crystals are by design fixed-frequency devices whose oscillation frequency is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The oscillation frequency of a crystal on the same substrate with the microprocessor would inherently not vary due to variations in manufacturing, operating voltage and temperature in the same way as the frequency capability of the microprocessor on the same underlying substrate, as claimed.

Note that the term clock can refer to many different signals since the definition is broad, and that it can also refer to the oscillator that is required to generate the clock. While a crystal-controlled oscillator typically operates at a single speed, the circuitry around the crystal may be

designed so that the output of the entire oscillator circuit can be varied. Many mechanisms can be used to control the output of a variable-frequency oscillator, including manual inputs, program-controlled inputs, temperature sensors, or other devices. Non-crystal controlled oscillators are also possible, and when they are designed as variable-frequency oscillators they are typically also controlled by manual inputs, program-controlled inputs, temperature sensors and other devices.

The present invention is unique in that it applies, and can only apply, in the circumstance where the oscillator or variable speed clock is fabricated on the same substrate as the driven device. The example given is a non-crystal controlled circuit, a ring oscillator. **A** ring oscillator will oscillate at a frequency determined by its fabrication and design and the operating environment. Thus in this example, the user designs the ring oscillator (clock) to oscillate at a frequency appropriate for the driven device when both the oscillator and the device are under specified fabrication and environmental parameters. Crucial to the present invention is that since both the oscillator or variable speed clock and driven device are on the same substrate, when the fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together. This differs from all cited references in that the oscillator or variable speed clock and the driven device are on the same substrate, and that the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so. Like the cited references, the driven device might additionally contain clock generation circuitry to produce variations on the clock output of the oscillator or variable speed clock for the other circuitry on the device.

The remaining Bennett et al., Brantingham, Pollack, Gruner et al.and Suzuki et al. references, cited but not applied in a rejection, have been reviewed and found not pertinent to the invention as claimed.

Based on the above remarks, the rejection under 35 USC § 103 is believed to be overcome. All of the claims in the application are believed to be patentable over the prior art. This application is believed to be in condition for allowance, and allowance is solicited.

Respectfully submitted,

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Exhibit “V”

39-.702 GP 2315

PATENT

NANO-001/05US
N0765-2008

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of)

Charles H. Moore et al.

Serial No. 08/484,918

Filed: June 7, 1995

For: HIGH PERFORMANCE, LOW COST MICROPROCESSOR

Examiner: D. Eng

Art Unit: 2315

AMENDMENT

Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Amendment is being submitted in response to the first Office Action in the above-identified patent application.

IN THE SPECIFICATION

At page 1, line 1, please change the title from "HIGH PERFORMANCE, LOW COST MICROPROCESSOR" to --HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK--.

Please rewrite the Abstract as follows:

--A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.--

IN THE CLAIMS

Please amend claims 19-20 and 65-66 as follows:

19(Amended). A microprocessor system, comprising a single integrated circuit a central processing unit and a ring [counter] oscillator variable speed system clock connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring [counter] oscillator variable speed system clock [being provided in a single integrated circuit] each including a plurality of electronic devices of like type, said central processing unit operating at a variable processing frequency dependent upon a variable speed of said ring oscillator variable speed system clock.

20(Amended). The microprocessor system of Claim 19 additionally comprising an input/output interface connected to exchange coupling control signals, address and data with said [input/output interface] central processing unit, and a second clock independent of said ring [counter] oscillator variable speed system clock connected to said input/output interface.

65(Amended). In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:

[which comprises fabricating] providing a ring [counter] oscillator system clock having a plurality of transistors within the integrated circuit, said plurality of transistors having operating characteristics disposed to vary similarly to operating characteristics of transistors included within the microprocessor; [and the microprocessor each having a plurality of transistors having operating characteristics which vary in the same way with variations in their fabrication,] and

using the ring [counter] oscillator system clock for clocking the microprocessor, said central processing unit operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock.

66(Amended). The method of Claim 65 additionally comprising the steps of:

providing an input/output interface for the microprocessor integrated circuit, [and]

clocking the input/output interface with a second clock independent of the ring [counter] oscillator system clock, and

buffering information within said input/output interface received from said microprocessor integrated circuit.

Please add the following new claims 71-79:

71. The microprocessor system of claim 20 further including system memory coupled to said input/output interface, said system memory being synchronized to said second clock and operating synchronously with respect to said ring oscillator variable speed system clock.

72. The method of claim 65 further including the steps of

transferring information to and from said microprocessor in synchrony with said ring oscillator system clock, and

buffering said information to facilitate transfer of said information to and from system memory synchronously with respect to said ring oscillator system clock.

73. A microprocessor system comprising:

a central processing unit disposed upon a substrate, said central processing unit operating at a processing frequency and including a first plurality of transistors;

an oscillator disposed upon said substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and including a second plurality of transistors designed such that operating characteristics of said first plurality and said second plurality of transistors vary in the same way as a function of parameter variation in one or more operational parameters associated with said substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation)

74. The microprocessor system of claim 73 wherein said one or more parameters are included within the set consisting of: operating temperature of said substrate, operating voltage of said substrate, and fabrication process of said substrate.

75. The microprocessor system of claim 73 further comprising:

an input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, address and data with said central processing unit;

an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

76. The microprocessor system of claim 75 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.

77. The microprocessor system of claim 73 wherein said oscillator comprises a ring oscillator.

78. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon a substrate, said central processing unit including a first plurality of transistors and being operative at a processing frequency;

clocking said central processing unit at a clock rate using an oscillator disposed upon said substrate, said oscillator being provided so as to include a second plurality of transistors with said central processing unit being clocked by said oscillator at a variable frequency dependent upon variation in one or more operational parameters associated with said substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more operational parameters associated with said substrate.

79. The method of claim 78 further comprising the steps of

connecting an input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, address and data between said input/output interface and said central processing unit;

clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

REMARKS

This amendment responds to the first office action. Claims 19-20 and 65-66 have been amended, and new claims 71-79 have been added.

The Examiner has requested that applicants update the status of the parent application. Applicants note that the parent application Serial No. 07/389,334 has issued as U.S. Pat. No. 5,440,749. Also pursuant to the Examiner's request, a new title and new abstract more aptly descriptive of the invention have been provided.

The Examiner has rejected claims 19-21 and 65-67 under 35 U.S.C. § 112 as being indefinite. With respect to the apparatus claims, the Examiner asserted that there exists no functional relationship and interconnection between the claimed components. Similarly, the Examiner asserted that a functional relationship does not exist between the steps of the method claims, and that it is unclear what the steps try to accomplish.

Applicants note that the present invention is directed to a microprocessor system including a central processing unit and a ring oscillator variable speed system clock connected thereto. In accordance with the claimed invention, the central processing unit and the ring oscillator variable speed system clock are provided in a single integrated circuit. This allows, for example, the central processing unit to track variations in the speed of the ring oscillator variable speed system clock, since the elements of each are disposed in the same integrated circuit. By this amendment the term "ring counter" has been replaced with "ring oscillator", in order to more particularly identify the ring oscillator (FIG. 18) incorporated within a preferred implementation of the microprocessor system of the invention.

Although applicants submit that the "functional relationship" between the claimed central processing unit and system clock connected thereto is inherently clear, the apparatus and method claims have been amended in an effort to accommodate the Examiner's concerns with respect to 35 **U.S.C.** §112. For example, claim 19 now recites a "functional relationship" in that it is made explicit that the ring oscillator variable speed system clock is disposed to clock the central processing unit. Moreover, the central processing unit and ring oscillator variable speed system clock are described as "each including a plurality of electronic devices of like type". This allows the central processing unit to operate at a

variable processing frequency which depends upon a variable speed of the ring oscillator variable speed system clock. See, for example, the specification at page 31, line *33* to page 32, line 1:

> By deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast. For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor 50 will operate slower than normal. Since the microprocessor 50 *ring oscillator clock 430 is made from the same transistors on the same die as the latches and gates,* it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.

Method claim 65 has been similarly amended, and now recites the step of:

> fabricating a ring oscillator system clock having a plurality of transistors, said plurality of transistors having operating characteristics disposed to vary similarly to operating characteristics of transistors included within the microprocessor ... .

The method claims thus now prescribe a technique for clocking a microprocessor using a ring oscillator system clock comprised of transistors having similar operating characteristics as those within the microprocessor. This advantageously allows the processing frequency of the microprocessor to track the clock rate of the ring oscillator system clock.

The Examiner has rejected claims 19 and *65* under *35* U.S.C. § 103 as being unpatentable over Sheets. The Examiner stated that Sheets teaches a microprocessor system having a microprocessor and a variable speed clock generator. Although admitting that Sheets does not disclose that his clock is implemented using a ring oscillator, the Examiner opined that a "counter is a basis component of [a] clock generator". It was further asserted that choosing the counter to be of the ring type is merely a matter of design choice.

Applicants again observe that the present invention is directed to a system and method for clocking a central processing unit disposed *within the same integrated circuit* as a ring oscillator variable speed system clock. This allows, for example, the central processing unit to track variations in the speed of the ring oscillator variable speed system clock, since the elements of each are disposed in the same integrated circuit. That is, the operational speed of the microprocessor and ring oscillator clock are designed to vary similarly as a function of variation in temperature, processing and other parameters affecting circuit performance.

The system of Sheets effects microprocessor clocking in a way which is entirely dissimilar from that of the present invention, and in fact teaches away from Applicants' clocking scheme. In particular, Sheets describes the use of discrete, commercially available microprocessor chips, e.g., the Motorola 68000 (col. 5, line 16), driven by a separate clock (VCO 12 of FIG. 1). As is well known, such microprocessor chips include terminals or pins, such as the CLK and INT terminals of microprocessor (FIG. 1), for receiving inputs from external devices like the VCO 12 and fixed oscillator 103. Because the VCO 12 is not integral with the microprocessor 101, Sheets has proposed a technique for adjusting the frequency of VCO 12 in accordance with a desired operating frequency of the microprocessor 101. Specifically, a digital word indicative of this desired operating frequency is written by microprocessor 101 to VCO 12 by way of data bus 104 as a means of adjusting clock frequency.

The present invention does not similarly rely upon provision of frequency control information to an external clock, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, since the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance. Sheets' system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.

Although the foregoing clearly indicates the existence of a patentable distinction between the system of Sheets and the present invention, claims 19 and 65 have nonetheless been amended to advance prosecution of the application. Specifically, claims 19 and 65 now explicitly recite that the ring oscillator and microprocessor are provided within the same integrated circuit. Moreover, these claims further state that the plurality of transistors included within the ring oscillator clock have operating characteristics which vary similarly to operating characteristics of transistors included within the microprocessor, thereby enabling the processing frequency of the microprocessor to track the speed of the ring oscillator clock:

> …The CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process.
> (page 32, lines 10-13)

Neither of these aspects of the present invention are suggested by Sheets. As discussed above, Sheets describes the use of commercially available microprocessor chips, and depicts the microprocessor 101 as being coupled to a separate clock (i.e, VCO 12) by way of a data bus 104 and address bus 105. Moreover, the VCO 12 clearly is not comprised of transistors having operating characteristics disposed to vary similarly to those of transistors within the microprocessor 101. Rather, the VCO 12 is seen to be comprised of an LC oscillator (col. 3, line 58 and FIG. 6), which clearly is not adapted to mimic variation in the speed of transistors within the microprocessor 101. Accordingly, applicant respectfully submits that amended claims 19 and 65 are patentable over Sheets, and requests that the rejection thereof under 35 U.S.C. § 103 be withdrawn.

Since Schaire does not supplement the lack of teaching within Sheets with respect to amended claims 19 and 65, it is also respectfully submitted that pending claims 20-21 and 66-67 are patentable over Sheets in view of Schaire. Further with regard to pending claims 20 and 66, it is observed that Schaire provides no indication that bus interface unit 10 is clocked by a signal from a clock different from that used to clock the host microprocessor. That is, the origin of high-speed clock signal 230 (FIG. 1) provided to bus interface unit 10 does not appear to be described. Hence, Schaire fails to teach the claimed provision of separate, independent clock signals to an input/output interface buffer and microprocessor. Accordingly, applicant respectfully requests that the outstanding rejection of claims 20-21 and 66-67 under 35 U.S.C. § 103 be withdrawn.

By this amendment new claims 71-79 have also been added to more particularly identify the invention which appears to be available for protection. In this regard new claims 71-72 point out that information is transferred to and from the microprocessor in synchrony with the ring oscillator system clock, and that this information is buffered to facilitate transfer thereof to and from system memory synchronously with respect to the ring oscillator system clock. New claims 73-79 explicitly recite that the central processing unit and ring oscillator include first and second pluralities of transistors, respectively, and that the

operating characteristics of these transistors vary in the same way as a function of variation in operational parameters (e.g., operating temperature) of the substrate. This advantageously allows a processing frequency of the central processing unit to track a clock rate of the ring oscillator as a function of substrate parameter variation.

Accordingly, in view of the above remarks, it is submitted that this application is now ready for allowance. Early notice to this effect is solicited.

If in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned at (415) 843-5000.

Respectfully submitted,

COOLEY GODWARD CASTRO
HUDDLESON & TATUM

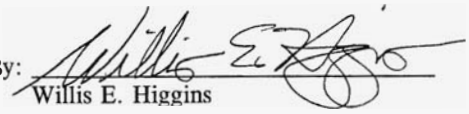
By: 
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Exhibit “W”

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Date: 1-8-97 By: Patricia K. Parus

IN THE UNITED STATES PATENT AMI) TRADEMARK OFFICE

In re application of

Charles H. Moore et al.

Serial No. 08/484,918

Filed: June 7, 1995

For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

Examiner: D. Eng

Art Unit: 2315

AMENDMENT

Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Amendment is being submitted in response to the Final Rejection dated July 8, 1996 in the above-identified patent application.

IN THE CLAIMS

Please amend claims 19, 65, 66, 71, 72, 73, 74 and 78 as follows;

19(Twice Amended). A microprocessor system, comprising a single integrated sircuit including a central processing unit and a ring oscillator variable speed system clock connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices [of like type] correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit [operating at a variable processing frequency dependent upon a variable speed of] and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said integrated circuit.

65(Twice Amended). In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of

providing a ring oscillator system clock [having a plurality] constructed of [transistors] electronic devices within the integrated circuit, said [plurality of transistors] electronic devices having operating characteristics [disposed to] which will, because said ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary [similarly to] together with operating characteristics of [transistors] electronic devices included within the microprocessor; and

using the ring oscillator system clock for clocking the microprocessor, said [central processing unit] microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock.

66(Twice Amended). The method of Claim 65 additionally comprising the steps of:

providing an input/output interface for the microprocessor integrated circuit, and

clocking the input/output interface with a second clock independent of the ring oscillator system clock[, and

buffering information within said input/output interface received from said microprocessor integrated circuit].

72(Amended). The method of claim 65 further including the [steps] step of

transferring information to and from said microprocessor in synchrony with said ring oscillator system clock[, and

buffering said information to facilitate transfer of said information to and from system memory synchronously with respect to said ring oscillator system clock].

73(Amended). A microprocessor system comprising:

a central processing unit disposed upon [a] an integrated circuit substrate, said central processing unit operating at a processing frequency and [including] constructed of a first plurality of [transistors] electronic devices;

an oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and including a second plurality of [transistors] electronic devices, thus varying the [designed such that] operating characteristics of said first plurality and said second plurality of transistors [vary] in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate thereby enabling said processing frequency to track said clock rate in response to said parameter variation

74(Amended). The microprocessor system of claim 73 wherein said one or more operational parameters [are included within the set consisting of:] include operating temperature of said substrate[,] or operating voltage of said substrate[, and fabrication process of said substrate].

78(Amended). In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon [a] an integrated circuit substrate, said central processing unit [including] being constructed of a first plurality of transistors and being operative at a processing frequency;

providing a variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors; and

clocking said central processing unit at a clock rate using [an oscillator, disposed upon said substrate, said oscillator being provided so as include a second plurality of transistors] variable speed clock with said central processing unit being clocked by said [oscillator] variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate.

Cancel claim 71.

REMARKS

Appreciation is expressed for the courteous and helpful telephone interview granted by the Examiner on January 7 and 8, 1997, with the undersigned attorney and Mr. George Shaw, representing the assignee of the application. The above changes to the claims are based on the discussion in the interview. Proposed changes to claims 19, 65 and 73 were sent by facsmile to the Examiner on January 7 to facilitate the further discussion on January 8. On January 8, the Examiner agreed that these changes merited further consideration of the application and appeared to overcome the prior art of record. The following remarks in part summarize the discussion in the interview and respond to specific points in the Final Rejection.

In the interview, the fact that operating characteristics of electronic devices in an integrated circuit will track one another depending on variations in the manufacturing process used to make the integrated circuit was discussed. This fact is described at page 31, line 1 through page 32, line 1 of this application, in the context of the microprocessor system of this invention. This fact is utilized in the present invention to provide a variable speed clock for the microprocessor, with the

clock speed varying in the same way as variations in the operating characteristics of the electronic devices making up the microprocessor. This allows the microprocessor to operate at its fastest safe operating speed, given its manufacturing process or changes in its operating temperature or voltage. In contrast, prior art microprocessor systems are given a rated speed based on possible worst case operating conditions and an external clock is used to drive them no faster than the rated speed. Under other than worst case operating conditions, the prior art microprocessors are actually capable of operating at a faster clock speed than their rated speed.

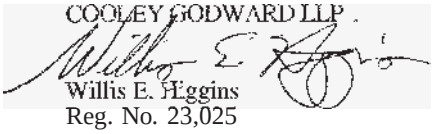
The above changes to the claims have been made to bring out the above distinction over the prior art more clearly. It is believed that they overcome the rejection of claims 19-21, 65-67 and 71-79 under 35 USC § 112, define statutory subject matter, i.e, a system implemented as a single integrated circuit having defined characteristics or a process, as well as distinguishing over the prior art of record.

In the rejection under 35 USC § 103, the Examiner contends that the Sheets reference "clearly indicates in lines 46-48 of column 2 that the system 100 shown in Figure 1 is fabricated *on* a ***single chip*** using MOS technology." Specific issue is taken with the inclusion of the italicized language in this characterization of the reference. Sheets does not say that the system 100 is on a single chip, only that it is implemented in MOS technology. At column 5, lines 15-17, a specific example of the Motorola 68000 microprocessor is given. That microprocessor is driven by an external clock that provides a clock signal to a designated pin of the microprocessor integrated circuit package. Applicants are aware of no prior art teaching or suggesting a variable speed oscillator in the same integrated circuit with a microprocessor and clocking the microprocessor with a clock speed that varies correspondingly with changes in operating characteristics of electronic devices making up the microprocessor, as a result of being in the same integrated circuit as the microprocessor, as claimed. Even if the Examiner is correct that the variable clock in Sheets is in the same integrated circuit as the microprocessor of system 100, that still does not give the claimed subject matter. In Sheets, a command input is required to change the clock speed. In the present invention, the clock speed varies correspondingly to variations in operating parameters of the electronic devices of the microprocessor because both the variable speed clock and the microprocessor are fabricated together in the same integrated circuit. No command input is necessary to change the clock frequency. The rejection under 35 USC § 103 is believed to be overcome.

All of the claims in the application are believed to be patentable over the prior art. This application is believed to be in condition for allowance, and allowance is solicited.

Respectfully submitted,

COOLEY GODWARD LLP



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