Nos. 2016-1306, -1307, -1309, -1310, -1311

In the United States Court of Appeals for the Federal Circuit

TECHNOLOGY PROPERTIES LIMITED LLC, PHOENIX DIGITAL SOLUTIONS LLC, PATRIOT SCIENTIFIC CORPORATION,

Plaintiffs-Appellants,

v.

HUAWEI TECHNOLOGIES CO., LTD., FUTUREWEI TECHNOLOGIES, INC., HUAWEI DEVICE CO., LTD., HUAWEI DEVICE USA INC., HUAWEI TECHNOLOGIES USA INC., ZTE CORPORATION, ZTE USA, INC., SAMSUNG ELECTRONIC CO., LTD, SAMSUNG ELECTRONICS AMERICA, INC., LG ELECTRONICS, INC., LG ELECTRONICS U.S.A., INC., NINTENDO CO., LTD., NINTENDO OF AMERICA INC.,

Defendants-Appellees.

Appeal from the United District Court
for the Northern District of California, Case Nos. 3:12-cv-03865-VC, 3:12-cv-03876-VC, 3:12-cv-03877-VC, 3:12-cv-03880-VC, and 3:12-cv-03881-VC.
The Honorable **Vince Chhabria**, Judge Presiding.

CORRECTED JOINT APPENDIX

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. HUAWEI TECHNOLOGIES CO., LTD., et al., Defendants.	Case No. 3:12-cv-03865-VC (PSG) **FINAL JUDGMENT**
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. ZTE CORPORATION, et al., Defendants.	Case No. 3:12-cv-03876-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. SAMSUNG ELECTRONICS CO., LTD., et al., Defendants.	Case No. 3:12-cv-03877-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. LG ELECTRONICS, INC., et al., Defendants.	Case No. 3:12-cv-03880-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. NINTENDO CO., LTD, et al. Defendants.	Case No. 3:12-cv-03881-VC (PSG)

Based upon this Court's construction of the term "an entire oscillator disposed upon said integrated circuit substrate" as "an [oscillator] located entirely on the same semiconductor substrate as the [central processing unit] that does not require a control signal and whose frequency is not fixed by any external crystal" in U.S. Patent No. 5,809,336 (the "'336 patent") pursuant to the Claim Construction Report and Recommendation, dated September 22, 2015, and this Court's Order Adopting Magistrate Judge's Report and Recommendation, dated November 9, 2015, Plaintiffs Technology Properties Limited LLC, Phoenix Digital Solutions LLC, and Patriot Scientific Corporation (collectively, "Plaintiffs") and Defendants Huawei Technologies Co., Ltd.,

Huawei Device Co., Ltd., Huawei Device USA, Inc., Futurewei Technologies, Inc., Huawei Technologies USA, Inc., ZTE Corporation, ZTE (USA) Inc., Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., LG Electronics, Inc., LG Electronics U.S.A., Inc., Nintendo Co., Ltd., and Nintendo of America, Inc. (collectively, "Defendants") (together, the "Parties") have stipulated that all Defendants are entitled to a judgment of non-infringement as a matter of law as to all of Plaintiffs' asserted claims of the '336 patent in the above-titled and numbered civil cases (collectively, "this Action").

Accordingly, the Court enters Judgment as follows:

Judgment is entered against Plaintiffs and for Defendants as to Plaintiffs' claims for patent infringement with respect to the '336 patent, subject to the parties' right to appeal.

Subject to the parties' right to appeal, the Court further enters judgment for Defendants and against Plaintiffs on Defendants' respective counterclaims seeking declaratory judgment of non-infringement and Defendants' respective affirmative defenses of non-infringement, and declares the '336 patent not infringed by Defendants. Plaintiffs shall take nothing from Defendants with respect to the asserted claims of the '336 patent.

All other claims, counterclaims, defenses, or other matters which have been asserted, including Defendants' counterclaims of patent invalidity, are dismissed without prejudice.

Each party shall bear its own costs and attorneys' fees.

IT IS SO ORDERED

Dated: November 13, 2015

VINCE CHHABRIA
United States District Judge

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

TECHNOLOGY PROPERTIES LIMITED LLC, et al.,

Plaintiffs,

v.

HUAWEI TECHNOLOGIES CO., LTD., et al.,

Defendants.

Case No. 12-cv-03865-VC

ORDER ADOPTING MAGISTRATE JUDGE'S REPORT AND RECOMMENDATION

Re: Dkt. Nos. 98, 105

TECHNOLOGY PROPERTIES LIMITED, LLC, et al.,

Plaintiffs,

v.

ZTE CORPORATION, et al.,

Defendants.

Case No. 12-cv-03876-VC

Re: Dkt. Nos. 109, 112

TECHNOLOGY PROPERTIES LIMITED LLC, et al.,

Plaintiffs,

v.

SAMSUNG ELECTRONIC CO., LTD, et al.,

Defendants.

Case No. 12-cv-03877-VC

Re: Dkt. Nos. 104, 107

United States District Court
Northern District of California

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. LG ELECTRONICS, INC., et al., Defendants.	Case No. 12-cv-03880-VC Re: Dkt. Nos. 117, 120

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. NINTENDO CO., LTD, et al., Defendants.	Case No. 12-cv-03881-VC Re: Dkt. Nos. 106, 109

United States District Court
Northern District of California

The Court agrees with the plaintiffs that de novo review of the Magistrate Judge's Report and Recommendation is warranted. Having reviewed the Report and Recommendation de novo, the Court adopts it without modification.

IT IS SO ORDERED.

Dated: November 9, 2015

VINCE CHHABRIA
United States District Judge

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. HUAWEI TECHNOLOGIES CO., LTD., et al., Defendants.	Case No. 3:12-cv-03865-VC **CLAIM CONSTRUCTION REPORT AND RECOMMENDATION**
TECHNOLOGY PROPERTIES LIMITED LLC, ET AL., PLAINTIFFS, V. ZTE CORPORATION, et al., DEFENDANTS.	Case No. 3:12-cv-03876-VC
TECHNOLOGY PROPERTIES LIMITED LLC, ET AL., PLAINTIFFS, V. SAMSUNG ELECTRONICS CO., LTD., et al., DEFENDANTS.	Case No. 3:12-cv-03877-VC

TECHNOLOGY PROPERTIES LIMITED LLC, ET AL., PLAINTIFFS, V. LG ELECTRONICS, INC., et al., DEFENDANTS.	Case No. 3:12-cv-03880-VC
TECHNOLOGY PROPERTIES LIMITED LLC, ET AL., PLAINTIFFS, V. NINTENDO CO., LTD., et al., DEFENDANTS.	Case No. 3:12-cv-03881-VC

The parties to this patent infringement suit dispute the construction of just one claim term in U.S. Patent No. 5,809,336: "an entire oscillator disposed upon said integrated circuit substrate."[1] At issue is the impact of various statements made by the patent applicant to the examiner during the patent's prosecution. Because these statements would be understood by one of ordinary skill in the art as disclaiming certain scope of the disputed "entire oscillator" term, the court RECOMMENDS construction of the term to reflect this disclaimer, as follows: "an [oscillator] located entirely on the same semiconductor substrate as the [central processing unit] that does not require a control signal and whose frequency is not fixed by any external crystal."

I.

Consistent with the Supreme Court's admonition in 1886 that a patent claim not be "a nose of wax, which may be turned and twisted in any direction,"[2] the Federal Circuit has long held that a claim term must be understood as limited if the applicant argued as much during prosecution in

[1] *See* Docket No. 89 at 6-7.

[2] *White v. Dunbar*, 119 U.S. 47, 51 (1886).

order to overcome prior art.[3] "'[T]he prosecution history can often inform the meaning of the claim language by demonstrating . . . whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be.'"[4]

Plaintiff Technology Property Limited and Patriot Scientific brought these patent infringement suits for infringement of three patents: U.S Patent Nos. 5,440,749, 5,530,890 and 5,809,336. Only the '336 patents remains at issue; the others were dismissed by stipulation.[5] The '336 patent, titled "High Performance Microprocessor Having Variable Speed System Clock," was derived along with the others from a single patent application that was subject to nothing less than a ten-way restriction requirement. The result is that the '336 specification includes much discussion that is irrelevant to that which the '336 patent specifically claims.[6]

The '336 patent claims an invention that allows the frequency of a central processing unit, the brains of any computing device, to fluctuate based on local conditions. Traditional microprocessors use off-chip, fixed frequency clocks to regulate the CPU's frequency.[7] One result is that the clock needs to be set lower than the CPU's maximum possible frequency to ensure proper operation under worst-case conditions. The '336 patent solves this problem by placing a ring oscillator on the same silicon substrate as the CPU to act as the CPU's clock. Because the ring oscillator is on the same silicon substrate and is made of the same components as the CPU, it is subject to the same environmental conditions and thus will allow the CPU to operate at higher rates

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[3] *See, e.g., Southwall Techs., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995); *see also Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319, 1325 (Fed. Cir. 2002) ("Explicit arguments made during prosecution to overcome prior art can lead to a narrow claim interpretation because '[t]he public has a right to rely on such definitive statements made during prosecution.'") (quoting *Digital Biometrics, Inc. v. Identix, Inc.*, 149 F.3d 1335, 1347 (Fed. Cir. 1998)).

[4] *Abbott Labs. v. Sandoz, Inc.*, 566 F.3d 1282, 1289 (Fed. Cir. 2009) (quoting *Phillips v. AWH Corp.*, 415 F.3d 1303, 1317 (Fed. Cir. 2005) (en banc)).

[5] *See* Docket No. 86; all docket references are to Case No. 3:12-cv-03865-VC.

[6] *See, e.g.*, Docket No. 28-3, Ex. C at 3:27-35, 16:43-17:37.

[7] *See* Docket No. 28-3, Ex. C at 16:48-50, 17:12-13.

during good conditions and lower rates during bad. As the specification explains, the microprocessor may "operate over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing" that "all affect transistor gate propagation delays."[8] Because other devices with which the microprocessor communicates, both on-chip and off-chip, cannot tolerate a variable speed clock, a second, conventional "crystal clock" is separately connected to the input/output interface.[9]

During the '336 patent's prosecution, the applicants made a variety of arguments to the examiner to overcome two key prior art references: U.S. Patent No. 4,503,500 ("Magar") and U.S. Patent No. 4,670,837 ("Sheets"). With respect to Magar, the examiner initially rejected the claims after noting that certain circuitry in Magar was fabricated on the same microprocessor substrate as the CPU, as required by the claims. The applicants then attempted to distinguish Magar by emphasizing that the clock disclosed in Magar was fixed by a crystal that was external to the microprocessor, unlike their on-chip variable speed clock:

> [O]ne of ordinary skill in the art should readily recognize that the speed of the CPU and clock *do not* vary together due to manufacturing variation, operating voltage, and temperature of the IC in the Magar processor . . . This is simply because the Magar microprocessor clock is frequency controlled by a crystal which is also external to the microprocessor. Crystals are by design fixed frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The Magar microprocessor in no way contemplates a variable speed clock as claimed.[10]

In the same amendment, the applicants also argued that the Magar clock could not practice the claimed invention because of its reliance on a crystal, which by its nature cannot vary its oscillation frequency:

> [C]rystal oscillators have never, to Applicants' knowledge, been fabricated on a single silicon substrate with a CPU, for instance. Even if they were, as previously mentioned, crystals are by design fixed-frequency devices whose oscillation

[8] Docket No. 28-3, Ex. C at 16:44-48.

[9] *See* Docket No. 28-3, Ex. C at 17:14-34, Fig. 17.

[10] Docket No. 90-7, Ex. D at 3-4.

> frequency is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The oscillation frequency of a crystal on the same substrate with the microprocessor would inherently not vary due to variations in manufacturing, operating voltage and temperature in the same way as the frequency capability of the microprocessor on the same underlying substrate, as claimed.[11]

The PTO nonetheless issued a second rejection based on Magar, and the applicants responded by emphasizing again that the claimed invention did not rely on an external crystal's fixed frequency to set the clock's frequency rate:

> The essential difference is that the frequency or rate of the . . . signals is determined by the processing and/or operating parameters of the integrated circuit containing the . . . circuit, while the frequency or rate of the . . . signals depicted in Magar . . . are determined by the fixed frequency of the external crystal.[12]

The applicants also disclaimed the use of an external crystal to cause clock signal oscillation:

> Magar's clock generator relies on an external crystal connected to terminals X1 and X2 to oscillate . . . . It is not an entire oscillator in itself. And with the crystal, the clock rate generated is also conventional in that it is a fixed, not a variable, frequency. The Magar clock is comparable in operation to the conventional crystal clock 434 depicted in Fig. 17 of the present application for controlling the I/O interface at a fixed rate frequency, and not at all like the clock on which the claims are based.[13]

The examiner similarly issued an initial rejection in view of Sheets. In response, the applicants distinguished their "present invention" from microprocessors that rely on frequency control information from an external source:

> The present invention does not similarly rely upon provision of frequency control information to an external clock, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, since the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance.

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[11] *Id.* at 4.

[12] *Id.* at 4.

[13] *Id.* at 3.

> Sheets' system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.[14]

Because the applicants referred to the "present invention" in this statement, their disclaimer applies to all claims.[15]

But that disclaimer, like the prior disclaimers, could not secure allowance. In response to a subsequent rejection, the applicants went even further and disclaimed the use of controlled inputs altogether, regardless whether the control is on-chip or not:

> Even if the examiner is correct that the variable clock in Sheets is in the same circuit as the microprocessor of system 100, that still does not give the claimed subject matter. In Sheets, a command input is required to change the clock speed. In the present invention, the clock speed varies correspondingly to variations in operating parameters . . . . No command input is necessary to change the clock frequency.[16]

Thus, according to applicants, controlling the on-chip oscillator's speed using a command signal "does not give the claimed subject matter."[17] Indeed, in a later amendment, the applicants left no doubt that, unlike "all cited references," the claimed oscillator is completely free of inputs and extra components:

> Crucial to the present invention is that . . . when fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together. This differs from all cited references in that . . . the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so.[18]

After overcoming these and other objections by the examiner, the '336 patent issued on September 15, 1998. The patent has been construed in three previous litigations, including

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[14] Docket No. 90-9, Ex. F at 8.

[15] *See, e.g.*, *Ballard Med. Prods. v. Allegiance Healthcare Corp.*, 268 F.3d 1352, 1360-62 (Fed. Cir. 2001).

[16] Docket No. 90-10, Ex. G at 4.

[17] *Id.*

[18] Docket No. 90-7, Ex. D at 5.

one before the undersigned that resulted in a nine-day trial. In the Eastern District of Texas, Judge Ward construed the "entire ring oscillator" claim term in claim 1 to preclude reliance on either a control signal or an external crystal/clock generator to generate a clock signal.[19] In reaching this conclusion, Judge Ward explained: "The Court agrees with the defendants that the applicant disclaimed the use of an input control signal and an external crystal/clock generator to generate a clock signal."[20]

Similarly, in a United States International Trade Commission investigation, Judge Gildea construed "entire oscillator" as precluding reliance on either a control signal or an external crystal/clock generator to generate a clock signal.[21] Judge Gildea found that Plaintiffs clearly and unambiguously disclaimed any oscillator that relies on a control signal or an external crystal or frequency generator.[22] The Commission affirmed Judge Gildea's construction.[23]

Likewise, this court construed "ring oscillator" as "an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment,"[24] and instructed the jury that the term "entire oscillator" excludes any external clock used to generate the CPU clock signal.[25]

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[19] *See* Docket No. 90-15, Ex. L at 12.

[20] *Id.*

[21] *See* Docket No. 90-16, Ex. M at 40-41; Docket No. 90-17, Ex. N at 16-25.

[22] *See* Docket No. 90-20, Ex. Q at 39-40 (finding that "the essential point made by the applicants in seeking to gain acceptance" of their claims, and their "unqualified statements in distinguishing" the prior art, constituted a "clear disavowal" of claim scope).

[23] *See* Docket No. 90-17, Ex. N at 16-25.

[24] *See Acer, Inc. v. Tech. Properties Ltd.*, No. 5:08-CV-00877 PSG, 2013 WL 4515545, at *5 (N.D. Cal. Aug. 21, 2013).

[25] *See* Docket No. 90-13, Ex. J at 26; Docket No. 90-14, Ex. K at 2; *see also* Docket No. 90-18, Ex. O at 11, and n.24.

The parties to this litigation agree that the disputed term must be limited as "an [oscillator] that is located entirely on the same semiconductor substrate as the [central processing unit]."[26] Where they disagree is whether the term should further be limited to read as "an [oscillator] that is located entirely on the same semiconductor substrate as the [central processing unit] and does not rely on a control signal or an external crystal/clock generator to cause clock signal oscillation or control clock signal frequency."[27]

II.

This court has jurisdiction under 28 U.S.C. §§ 1331 and 1338. The presiding judge referred all pretrial matters to the undersigned pursuant to Fed. R. Civ. P. 72(a).[28]

"To construe a claim term, the trial court must determine the meaning of any disputed words from the perspective of one of ordinary skill in the pertinent art at the time of filing."[29] This requires a careful review of the intrinsic record comprised of the claim terms, written description and prosecution history of the patent.[30]

While claim terms "are generally given their ordinary and customary meaning,"[31] the claims themselves and the context in which the terms appear "provide substantial guidance as to the meaning of particular claim terms."[32] Indeed, a patent's specification "is always highly relevant

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[26] Docket No. 89 at 7.

[27] *Id.*

[28] *See* Docket No. 17.

[29] *Chamberlain Group, Inc. v. Lear Corp.*, 516 F.3d 1331, 1335 (Fed. Cir. 2008).

[30] *See id.* ("To construe a claim term, the trial court must determine the meaning of any disputed words from the perspective of one of ordinary skill in the pertinent art at the time of filing. Intrinsic evidence, that is the claims, written description, and the prosecution history of the patent, is a more reliable guide to the meaning of a claim term than are extrinsic sources like technical dictionaries, treatises, and expert testimony.") (citing *Phillips*, 415 F.3d at 1312).

[31] *Phillips*, 415 F.3d at 1312 (quoting *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996)).

[32] *Phillips*, 415 F.3d at 1314

to the claim construction analysis."[33] Claims "must be read in view of the specification, of which they are part."[34]

Although the patent's prosecution history "lacks the clarity of the specification and thus is less useful for claim construction purposes," it "can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be."[35] The court also has the discretion to consider extrinsic evidence, including dictionaries, learned treatises and testimony from experts and inventors.[36] Such evidence, however, is "less significant than the intrinsic record in determining the legally operative meaning of claim language."[37] No extrinsic evidence is necessary to resolve the dispute here, however, because the intrinsic record is dispositive that the applicant disclaimed certain claim scope to convince the examiner to issue the patent.

III.

"[T]here is no principle of patent law that the scope of surrender of subject matter made during prosecution is limited to what is absolutely necessary to avoid a prior art reference that was the basis for an examiner's rejection."[38] Whether necessary or not to get the examiner to avoid Magar and Sheets, the applicant here surrendered subject matter that the definition of the "entire oscillator" term must account, albeit in language different than that proposed by either side.

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[33] *Phillips*, 415 F.3d at 1312-15.

[34] *Markman v. Westview Instruments, Inc*., 52 F.3d 967, 979 (Fed. Cir. 1995); *see also Ultimax Cement Mfg. Corp v. CTS Cement Mfg. Corp*., 587 F. 3d 1339, 1347 (Fed. Cir. 2009).

[35] *Phillips*, 415 F.3d at 1317 (internal quotations omitted).

[36] *See id*. ("Although we have emphasized the importance of intrinsic evidence in claim construction, we have also authorized district courts to rely on extrinsic evidence, which 'consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises.'") (quoting *Markman*, 52 F.3d at 980).

[37] *Phillips*, 415 F.3d at 1317 (citing *C.R. Bard, Inc. v. U.S. Surgical Corp*., 388 F.3d 858, 862 (Fed. Cir. 2004)) (internal quotations and additional citations omitted).

[38] *Norian Corp. v. Stryker Corp*., 432 F.3d 1356, 1361 (Fed. Cir. 2005).

To avoid Magar, the applicants surrendered any oscillator that like Magar's is fixed by an off-chip crystal. Over and over again, the applicants insisted that its claims did not read on Magar because of this distinction. Whether styled by the applicants as an "essential difference" or "not at all like the clock on which the claims are based,"[39] Magar is distinct from the invention because it fixes the frequency of the CPU with a crystal oscillator that is not on the same silicon substrate. Having sold the Patent Office on this distinction, and told the world the same in the prosecution history, the applicants understood that they could not later claim anything else. The Federal Circuit has taught this lesson over and over again.[40]

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[39] Docket No. 90-8, Ex. E at 3, 4.

[40] *See, e.g.*, *Southwall*, 54 F.3d at 1576 ("Claims may not be construed one way in order to obtain their allowance and in a different way against accused infringers."); *Rheox*, 276 F.3d at 1325 ("Explicit arguments made during prosecution to overcome prior art can lead to a narrow claim interpretation because '[t]he public has a right to rely on such definitive statements made during prosecution.'"); *Gillespie v. Dywidag Sys. Int'l, USA*, 501 F.3d 1285, 1291 (Fed. Cir. 2007) ("The patentee is held to what he declares during the prosecution of his patent."); *Computer Docking Station Corp. v. Dell, Inc.*, 519 F.3d 1366, 1379 (Fed. Cir. 2008) (holding that "the sum of the patentees' statements during prosecution would lead a competitor to believe that the patentee had disavowed coverage of laptops" and, thus, affirming. the trial court's construction of the portable computer limitation); *Seachange Int'l, Inc. v. C-COR, Inc.*, 413 F.3d 1361, 1372-75 (Fed. Cir. 2005) ("Where an applicant argues that a claim possesses a feature that the prior art does not possess in order to overcome a prior art rejection, the argument may serve to narrow the scope of otherwise broad claim language."); *see also Am. Piledriving Equip. v. Geoquip, Inc.*, 637 F. 3d 1324, 1336 (Fed. Cir. 2011) ("[A]n applicant's argument that a prior art reference is distinguishable on a particular ground can serve as a disclaimer of claim scope even if the applicant distinguishes the reference on other grounds as well."); *Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) ("The purpose of consulting the prosecution history in construing a claim is to 'exclude any interpretation that was disclaimed during prosecution.'"; "Accordingly, 'where the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender.'") (citations omitted); *Microsoft Corp. v. Multi-Tech. Sys., Inc.*, 357 F.3d 1340, 1349 (Fed. Cir. 2004) (a court "cannot construe the claims to cover subject matter broader than that which the patentee itself regarded as comprising its invention and represented to the PTO"); *Springs Window Fashions LP v. Novo Indus., L.P.*, 323 F.3d 989, 993-96 (Fed. Cir. 2003) (rejecting patentee's attempt to narrow the scope of disclaimer, even though the examiner did not rely on the disclaimer to issue the claims); *N. Am. Container Inc. v. Plastipak Packaging Inc.*, 415 F.3d 1335, 1345-46 (Fed. Cir. 2005) (holding that "the applicant, through argument [that the prior-art inner walls are 'slightly concave'] during the prosecution, disclaimed inner walls of the base portion having any concavity. . . . [a]lthough the inner walls disclosed in the [prior art] may be viewed as entirely concave").

The song remains much the same regarding Sheets. The applicants distinguished Sheets repeatedly on the ground that Sheets requires control signals, frequency control information or command inputs. In contrast, they characterize the invention upon relying upon or requiring any such signals, information or inputs.[41] Because applicants described this distinction as no less than "crucial," and applicable to the "present invention," their disclaimer applies to all claims.[42]

Plaintiffs principally argue that the distinctions drawn from Magar and Sheets are already expressly included in the patent claims themselves. It is true that the "on-chip/off-chip" distinction and the invention's variability depending on PVT are reflected in other limitations. But those other limitations do not get at the full range of distinctions drawn, especially the claimed invention's oscillator frequency not being fixed by any crystal off-chip and the oscillator not needing any control inputs. The Federal Circuit has been clear that claim construction must reflect all disclaimers, not merely a subset.[43]

The undersigned appreciates that the construction recommended differs from the constructions adopted in the Eastern District of Texas, the International Trade Commission and by the undersigned as presiding judge in *HTC*. It also must be noted that neither party urged this particular language. But putting aside any notion that this court is bound in this case by any prior construction, the recommended construction is consistent with the fundamental meaning of those earlier constructions. After multiple rounds of briefing by the parties and a lengthy hearing, the undersigned is convinced that the particular language urged recommended here best captures what actually happened at the patent office. In the universe of claim construction, that directive is ultimate prime.

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[41] *See* Docket No. 90-9, Ex. F at 8; *see also* Docket No. 90-10, Ex. G at 4.

[42] *See, e.g.*, *Ballard Med. Prods. v. Allegiance Healthcare Corp.*, 268 F.3d 1352, 1360-62 (Fed. Cir. 2001).

[43] *See Krippelz v. Ford Motor Co*., 667 F.3d 1261, 1267 (Fed. Cir. 2012); *Am. Piledriving Equip. v. Geoquip, Inc*., 637 F.3d 1324, 1336 (Fed. Cir. 2011); *Elkay v. Mgf. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 979 (Fed. Cir. 1999).

SO ORDERED.

Dated: September 22, 2015

PAUL S. GREWAL
United States Magistrate Judge

US005809336A

United States Patent [19]

Moore et al.

[11] **Patent Number: 5,809,336**

[45] **Date of Patent: Sep. 15, 1998**

[54] **HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK**

[75] Inventors: **Charles H. Moore**, Woodside; **Russell H. Fish, III**, Mt. View, both of Calif.

[73] Assignee: **Patriot Scientific Corporation**, San Diego, Calif.

[21] Appl. No.: **484,918**

[22] Filed: **Jun. 7, 1995**

Related U.S. Application Data

[62] Division of Ser. No. 389,334, Aug. 3, 1989, Pat. No. 5,440,749.

[51] **Int. Cl.**[6] **G06F 1/04**

[52] **U.S. Cl.** **395/845**

[58] **Field of Search** 395/500, 551, 395/555, 845

[56] **References Cited**

U.S. PATENT DOCUMENTS

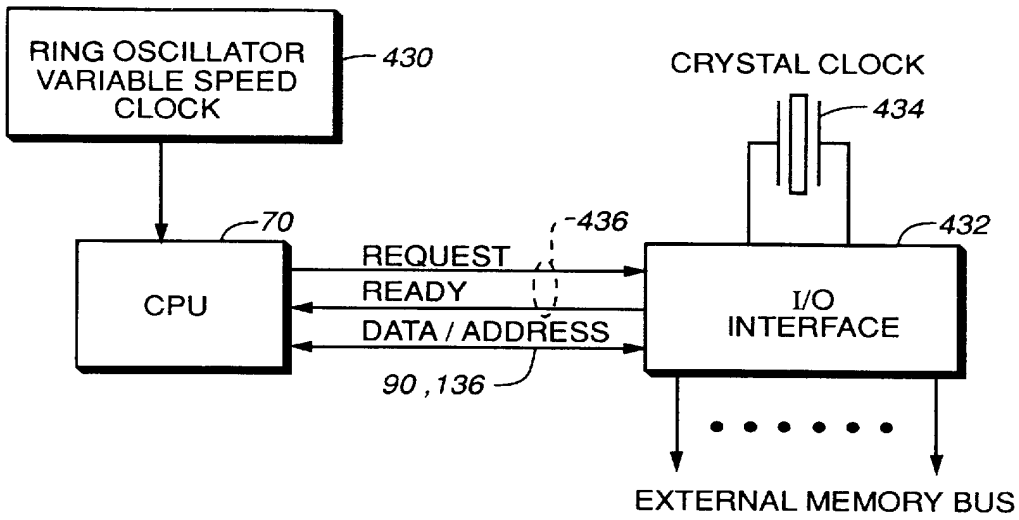
3,967,104	6/1976	Brantingham	364/709.09
3,980,993	9/1976	Bredart et al.	395/550
4,003,028	1/1977	Bennett et al.	395/742
4,042,972	8/1977	Gruner et al.	395/389
4,050,096	9/1977	Bennett	395/494
4,112,490	9/1978	Pohlman et al.	395/287
4,315,308	2/1982	Jackson	395/853
4,338,675	7/1982	Palmer	364/748
4,398,265	8/1983	Puhl et al.	395/882
4,453,229	6/1984	Schaire	395/250
4,503,500	3/1985	Magan	395/800
4,539,655	9/1985	Trussell et al.	395/280
4,553,201	11/1985	Pollack	395/183.22
4,627,082	12/1986	Pelgrom et al.	377/63
4,670,837	6/1987	Sheets	395/550
4,680,698	7/1987	Edwards et al.	395/800
4,761,763	8/1988	Hicks	395/286
5,414,862	5/1995	Suzuki et al.	395/750

Primary Examiner—David Y. Eng
Attorney, Agent, or Firm—Cooley Godward LLP

[57] **ABSTRACT**

A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.

10 Claims, 19 Drawing Sheets



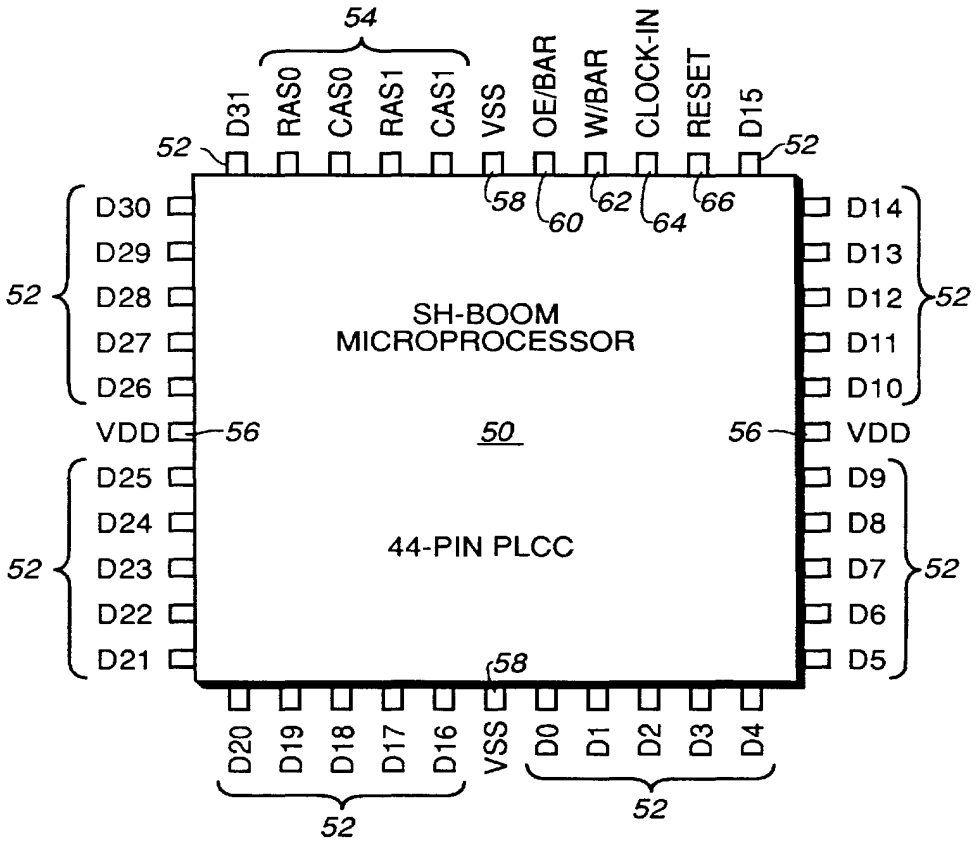

54
D31
RAS0
CAS0
RAS1
CAS1
VSS
OE/BAR
W/BAR
CLOCK-IN
RESET
D15
52
58
60
62
64
66
D30
D29
D28
D27
D26
VDD
D25
D24
D23
D22
D21
D14
D13
D12
D11
D10
VDD
D9
D8
D7
D6
D5
SH-BOOM
MICROPROCESSOR
50
44-PIN PLCC
56
D20
D19
D18
D17
D16
VSS
D0
D1
D2
D3
D4

FIG._1

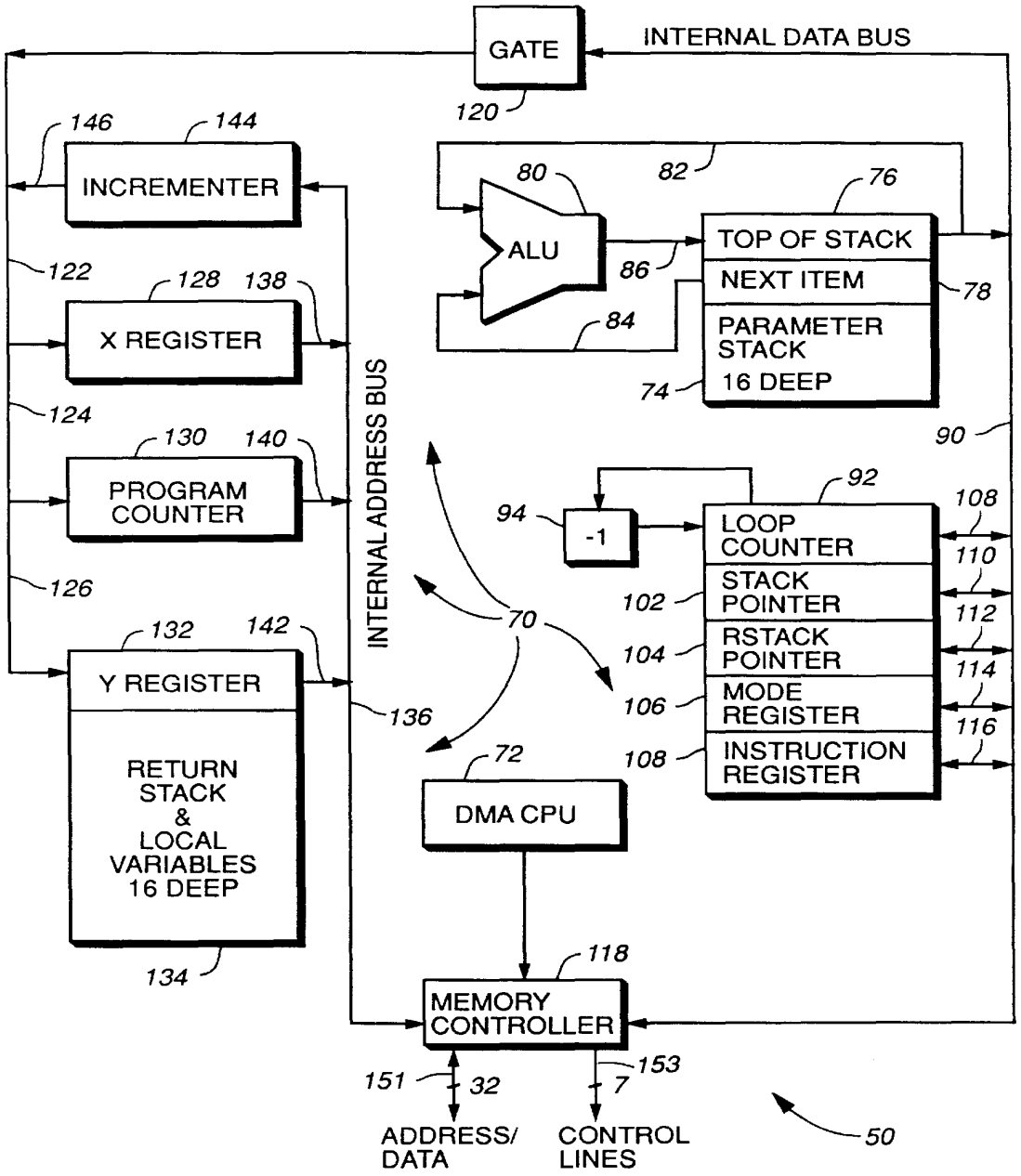

GATE
INTERNAL DATA BUS
120
146
144
INCREMENTER
80
82
76
ALU
TOP OF STACK
NEXT ITEM
PARAMETER STACK
16 DEEP
86
84
78
74
122
128
138
X REGISTER
124
130
140
PROGRAM COUNTER
126
INTERNAL ADDRESS BUS
90
92
94
-1
LOOP COUNTER
STACK POINTER
RSTACK POINTER
MODE REGISTER
INSTRUCTION REGISTER
108
110
112
114
116
102
104
106
108
70
132
142
Y REGISTER
136
RETURN STACK & LOCAL VARIABLES 16 DEEP
134
72
DMA CPU
118
MEMORY CONTROLLER
151
32
153
7
ADDRESS/ DATA
CONTROL LINES
50

FIG._2

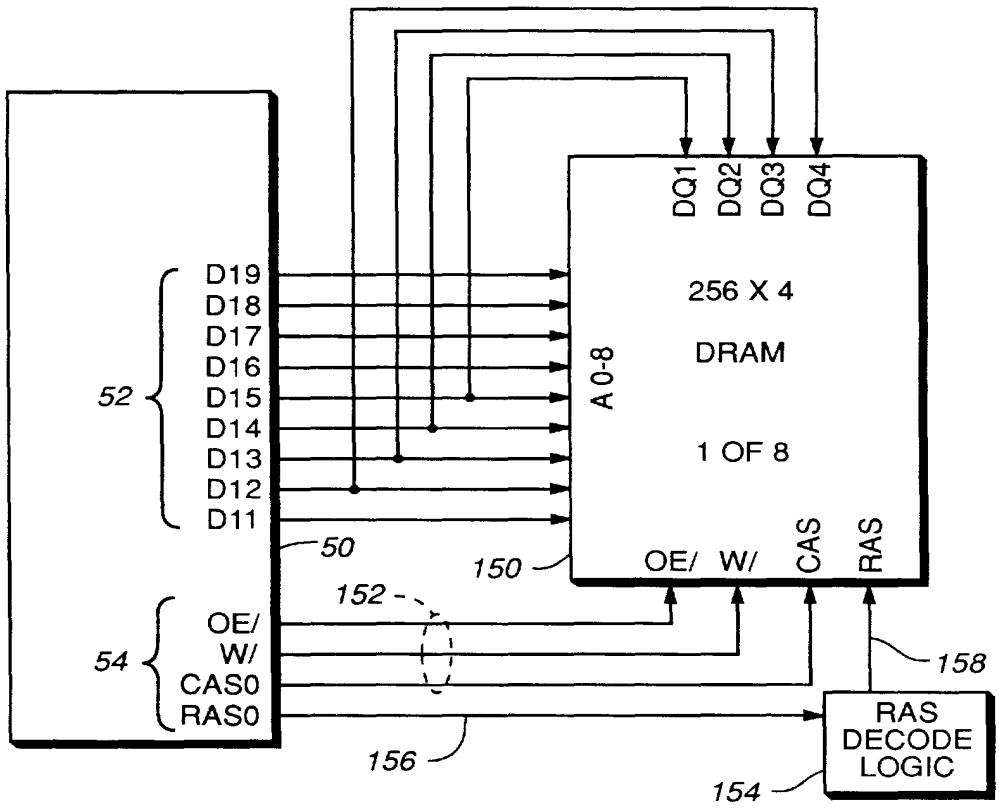

DQ1
DQ2
DQ3
DQ4
256 X 4
DRAM
1 OF 8
A 0-8
OE/
W/
CAS
RAS
D19
D18
D17
D16
D15
D14
D13
D12
D11
52
50
150
152
OE/
W/
CAS0
RAS0
54
156
158
RAS
DECODE
LOGIC
154

FIG._3

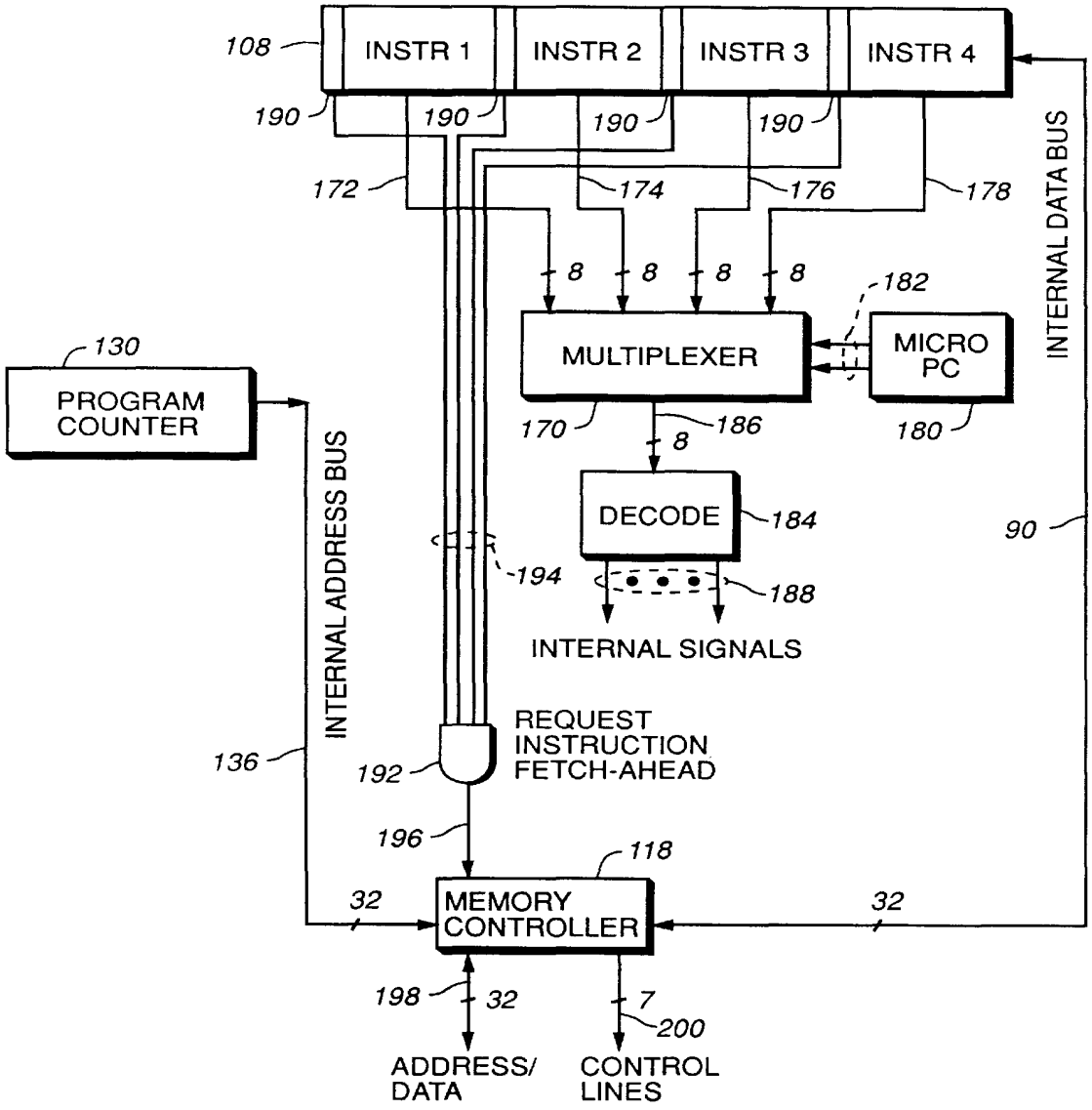

108
INSTR 1
INSTR 2
INSTR 3
INSTR 4
190
172
174
176
178
8
182
MULTIPLEXER
MICRO PC
130
PROGRAM COUNTER
170
186
180
DECODE
184
194
188
INTERNAL SIGNALS
INTERNAL ADDRESS BUS
INTERNAL DATA BUS
90
136
192
REQUEST INSTRUCTION FETCH-AHEAD
196
118
32
MEMORY CONTROLLER
198
7
200
ADDRESS/ DATA
CONTROL LINES

FIG._4

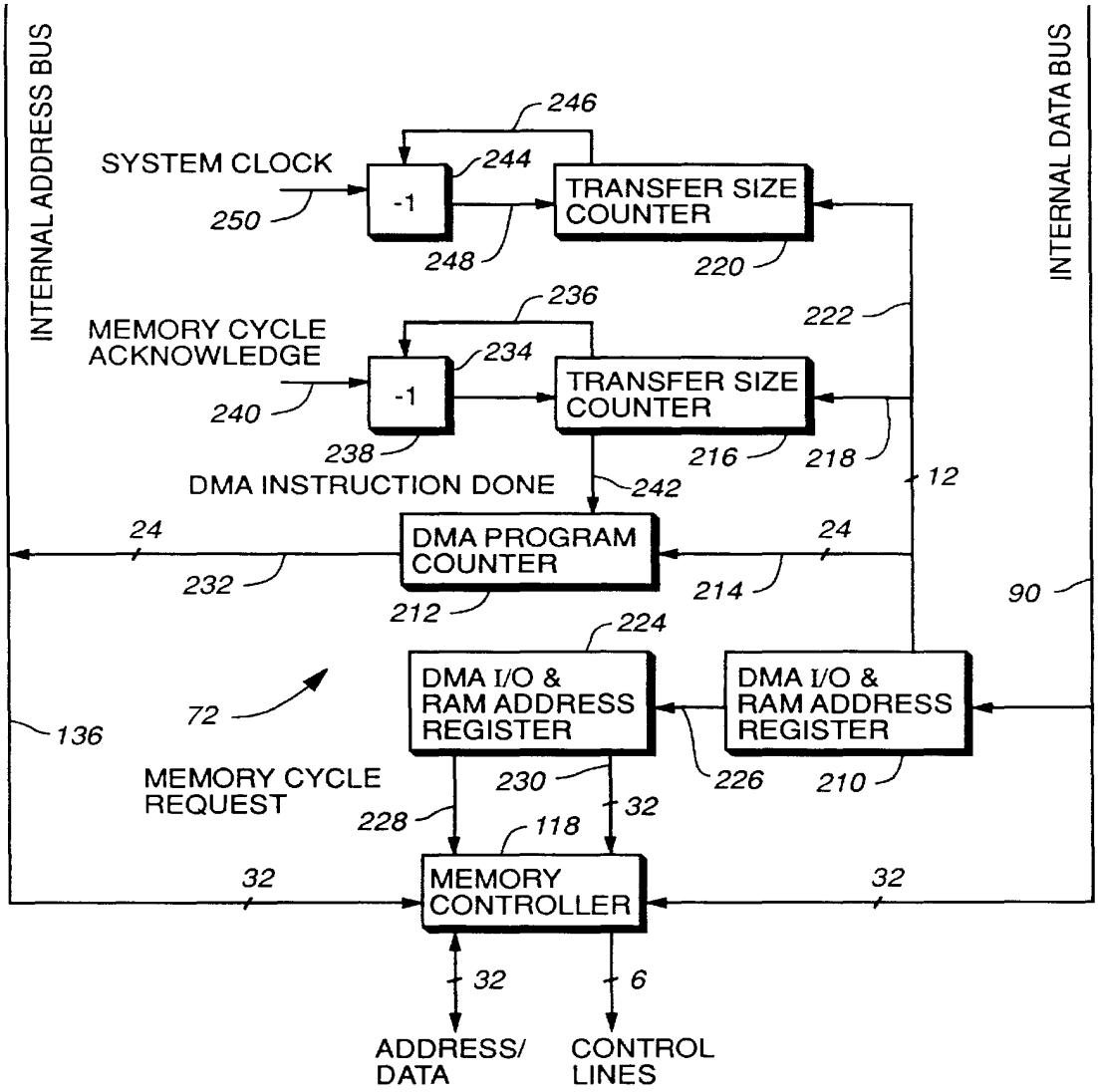

INTERNAL ADDRESS BUS
INTERNAL DATA BUS
SYSTEM CLOCK
250
246
244
-1
248
TRANSFER SIZE COUNTER
220
MEMORY CYCLE ACKNOWLEDGE
240
236
234
-1
238
TRANSFER SIZE COUNTER
216
218
222
12
DMA INSTRUCTION DONE
242
24
232
DMA PROGRAM COUNTER
212
24
214
90
224
72
136
DMA I/O & RAM ADDRESS REGISTER
DMA I/O & RAM ADDRESS REGISTER
226
210
MEMORY CYCLE REQUEST
230
228
32
118
32
MEMORY CONTROLLER
32
32
6
ADDRESS/ DATA
CONTROL LINES

FIG._5

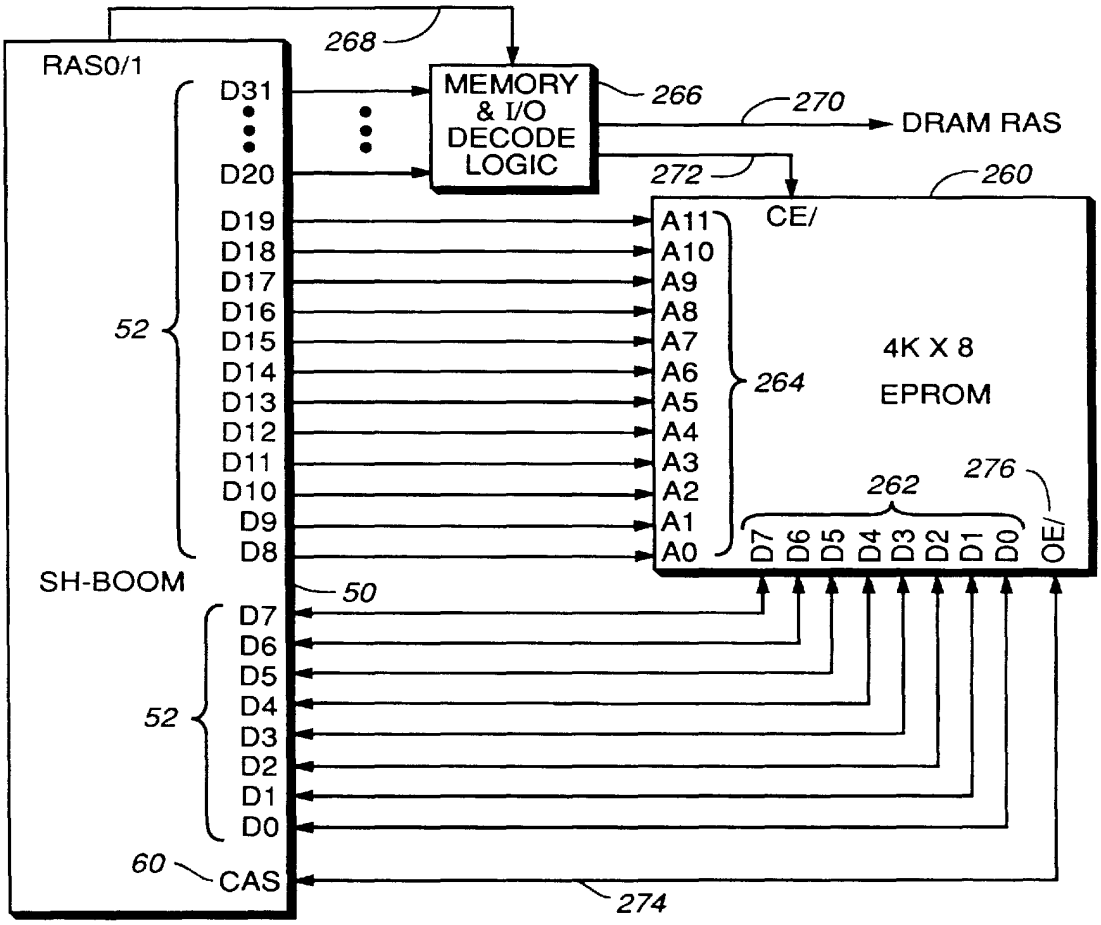

268
RAS0/1
D31
D20
MEMORY & I/O DECODE LOGIC
266
270
DRAM RAS
272
260
CE/
D19
D18
D17
D16
D15
D14
D13
D12
D11
D10
D9
D8
52
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
264
4K X 8
EPROM
262
276
D7
D6
D5
D4
D3
D2
D1
D0
OE/
SH-BOOM
50
52
60
CAS
274

FIG._6

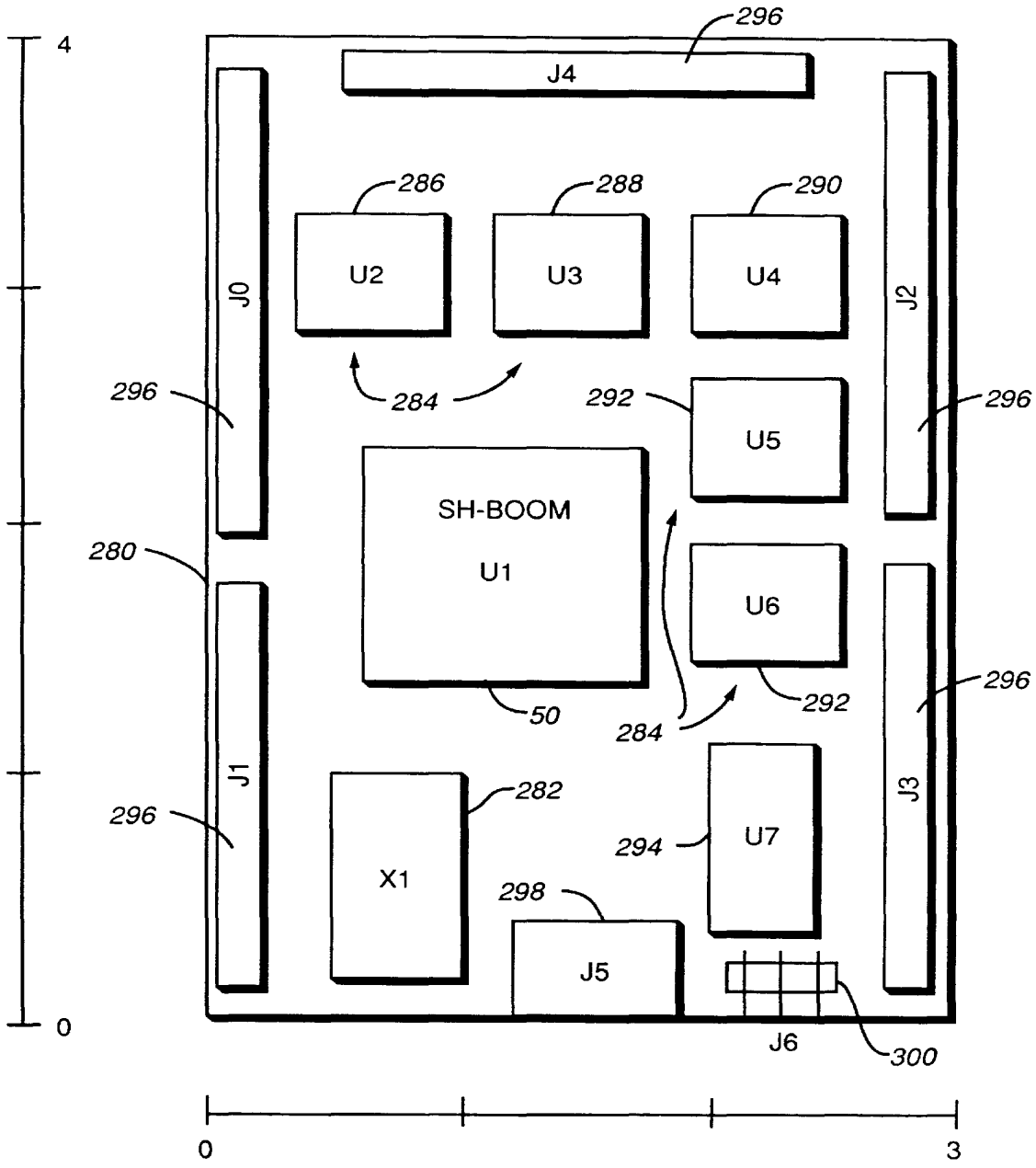

296
J4
286
288
290
U2
U3
U4
J0
J2
284
296
292
296
U5
SH-BOOM
U1
280
U6
296
50
284
292
J1
J3
296
282
294
U7
X1
298
J5
J6
300
4
0
0
3

FIG._7

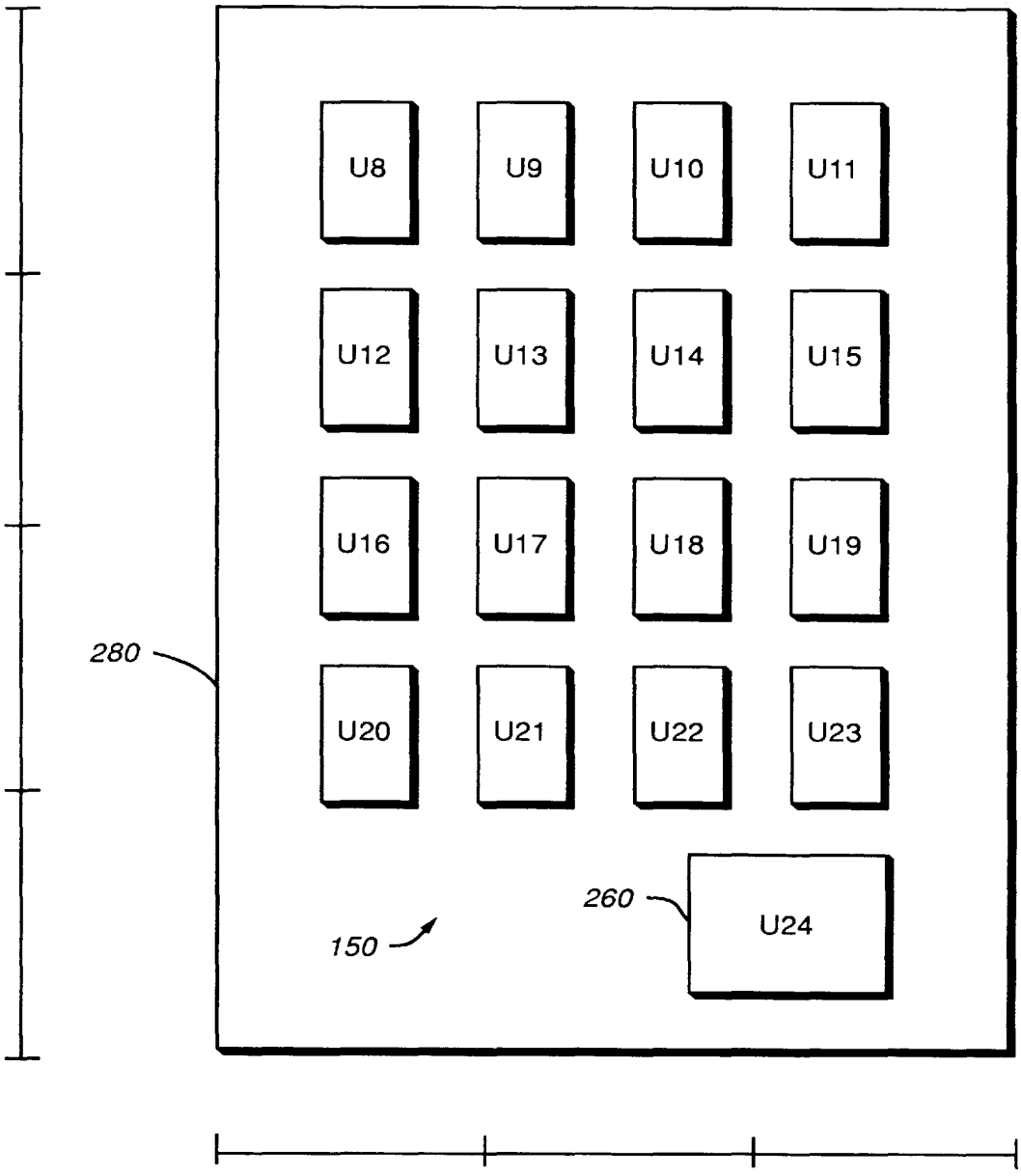

U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
280
260
150

FIG._8

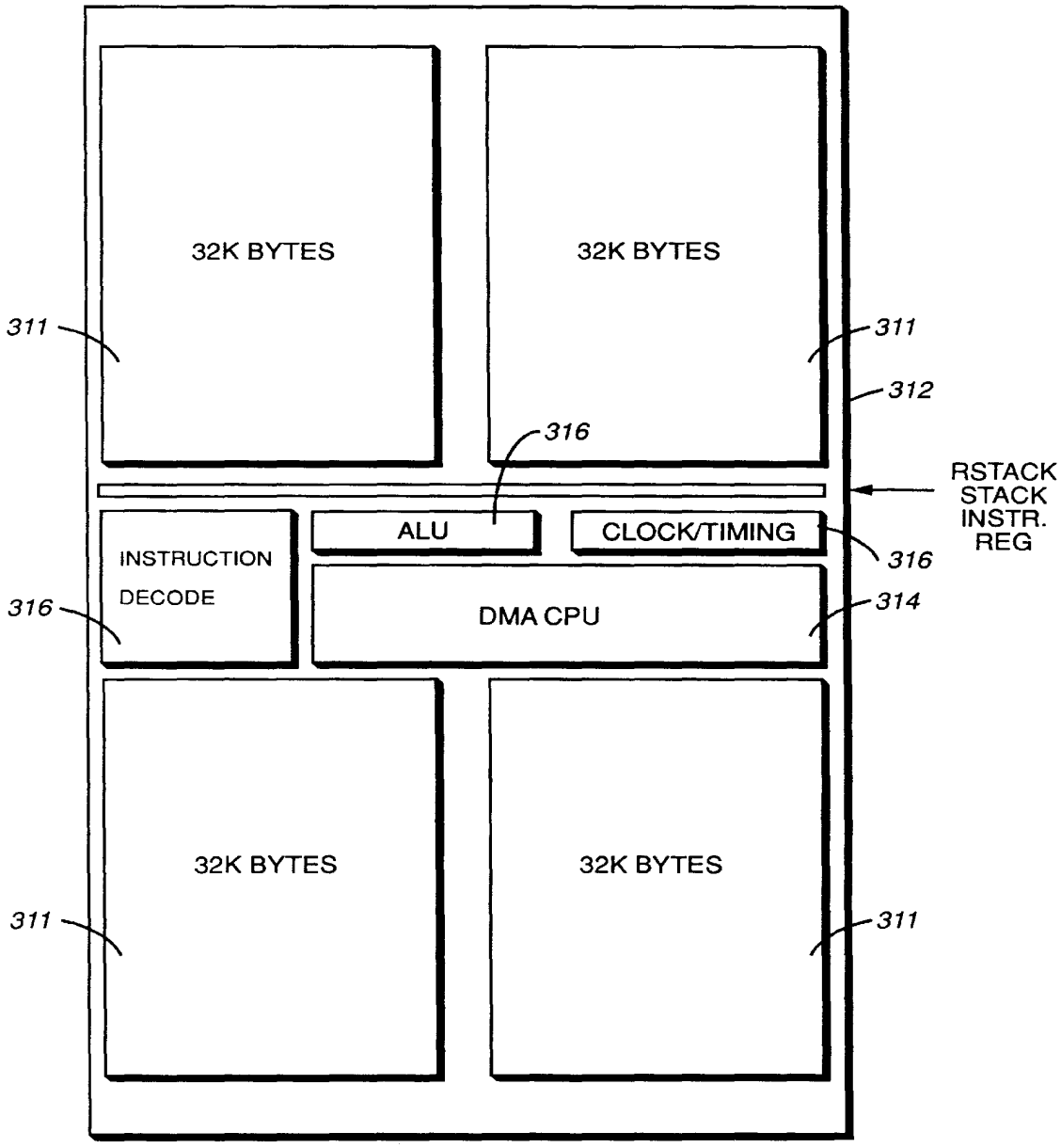

32K BYTES
32K BYTES
311
311
312
316
RSTACK
STACK
INSTR.
REG
ALU
CLOCK/TIMING
316
INSTRUCTION
DECODE
316
DMA CPU
314
32K BYTES
32K BYTES
311
311

FIG._9

FIG._10

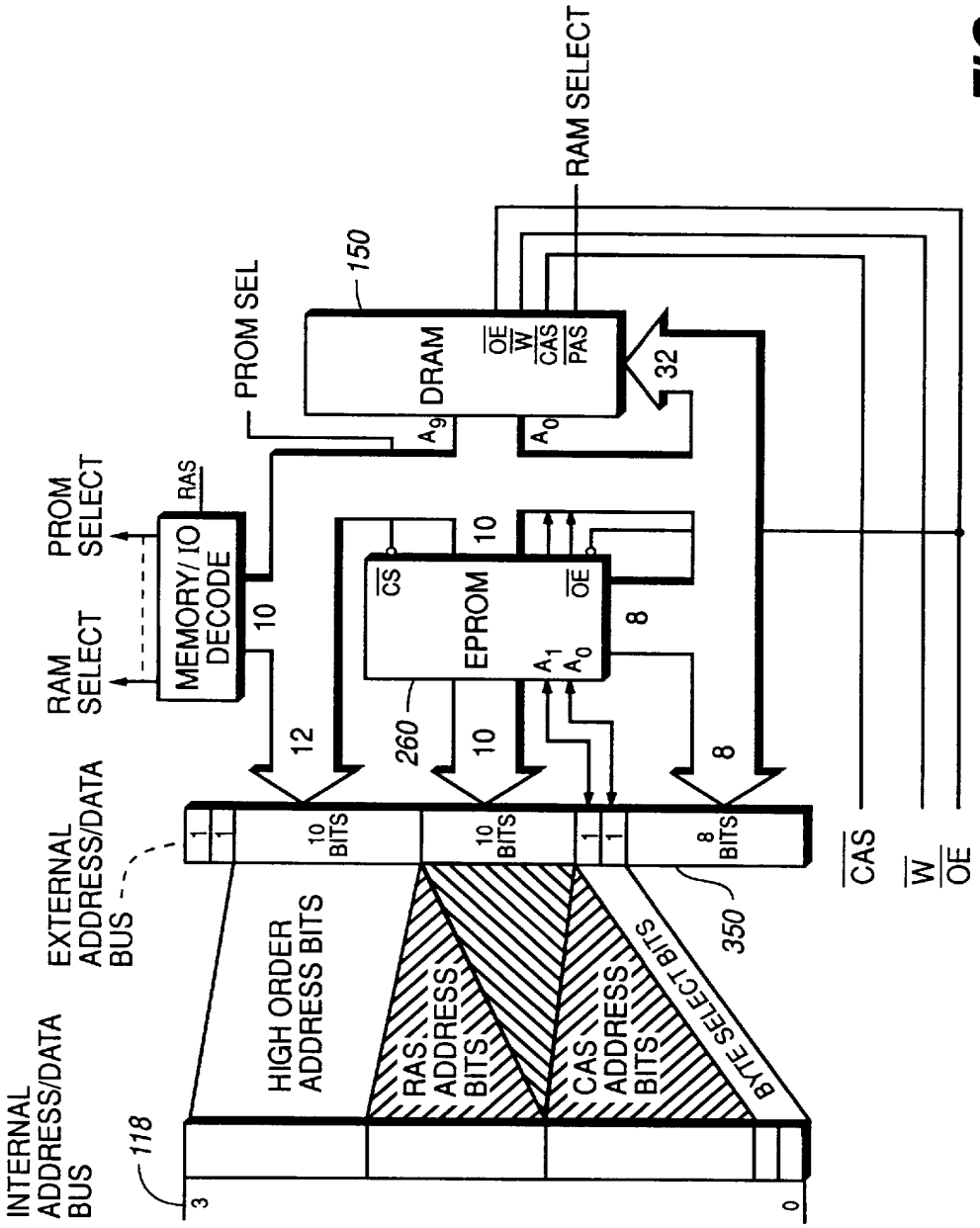
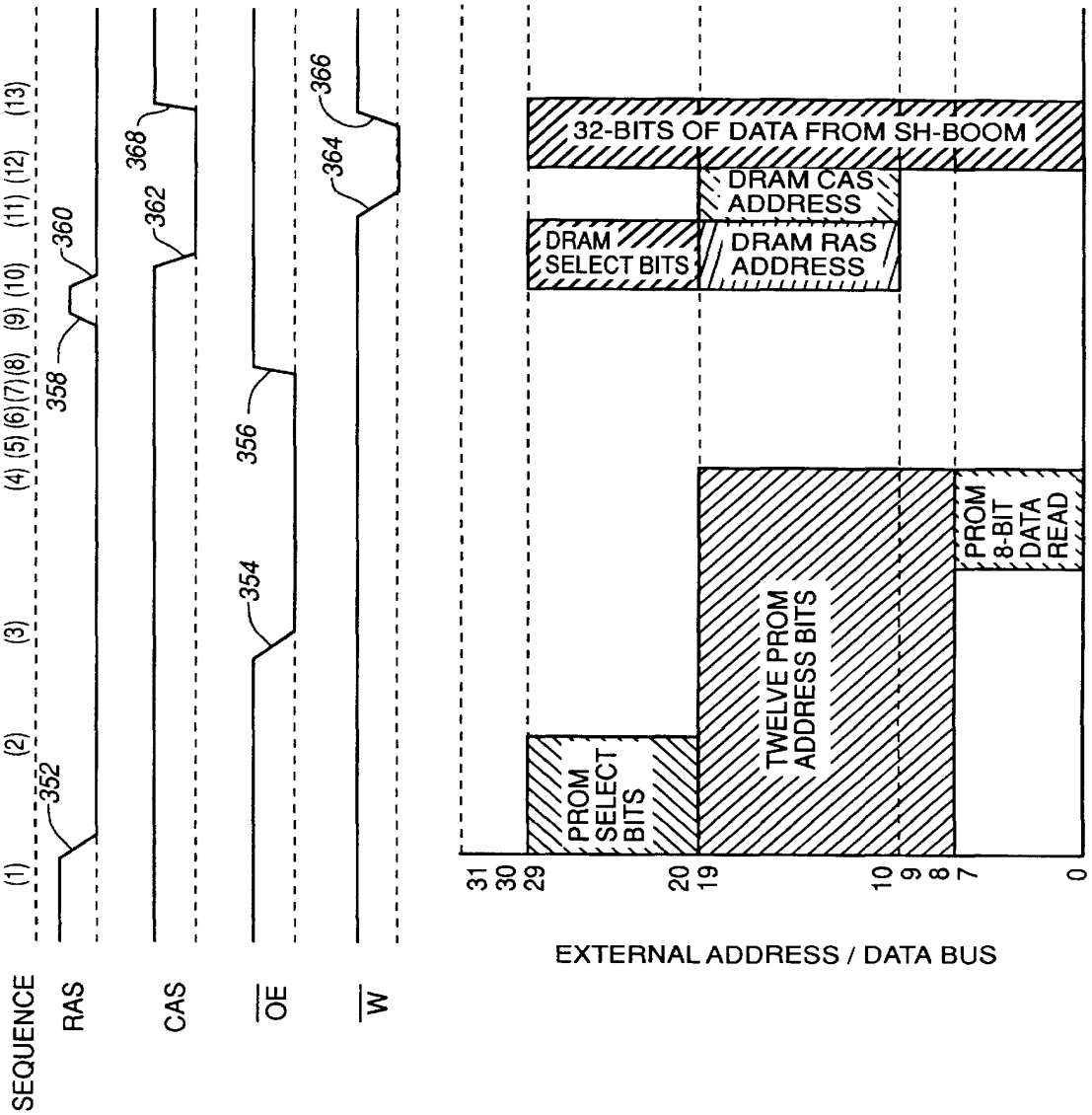

RAM SELECT
PROM SEL
150
DRAM
OE
W
CAS
PAS
32
A9
A0
PROM SELECT
RAS
MEMORY/IO DECODE
10
RAM SELECT
CS
EPROM
OE
A1
A0
10
8
260
12
10
8
EXTERNAL ADDRESS/DATA BUS
1
1
10 BITS
10 BITS
1
1
8 BITS
CAS
W
OE
350
HIGH ORDER ADDRESS BITS
RAS ADDRESS BITS
CAS ADDRESS BITS
BYTE SELECT BITS
INTERNAL ADDRESS/DATA BUS
118
3
0

FIG._11


SEQUENCE
RAS
CAS
OE
W
(1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11) (12) (13)
352
354
356
358
360
362
364
366
368
32-BITS OF DATA FROM SH-BOOM
DRAM CAS ADDRESS
DRAM SELECT BITS
DRAM RAS ADDRESS
PROM SELECT BITS
TWELVE PROM ADDRESS BITS
PROM 8-BIT DATA READ
31 30 29 20 19 10 9 8 7 0
EXTERNAL ADDRESS / DATA BUS

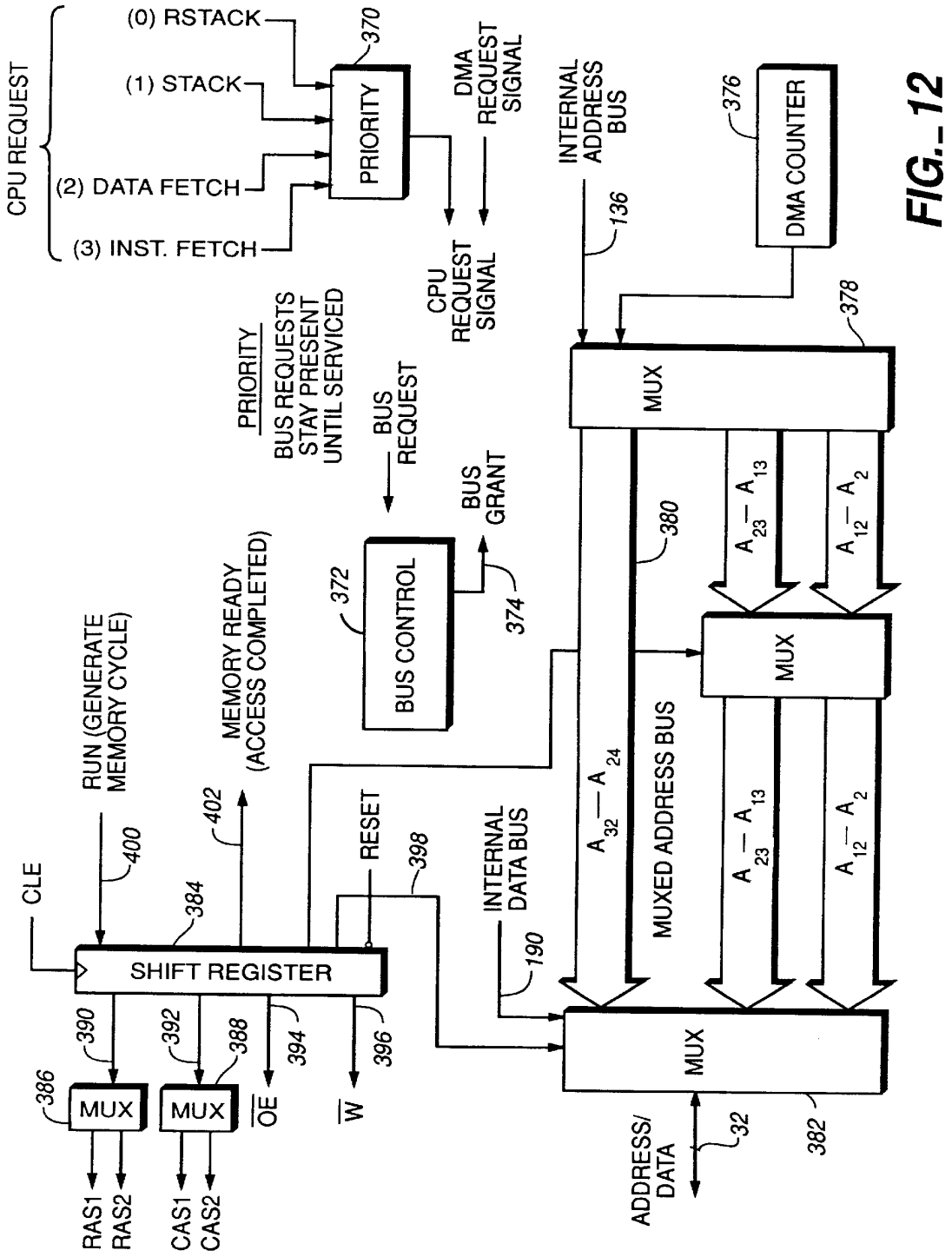

CPU REQUEST
(0) RSTACK
(1) STACK
(2) DATA FETCH
(3) INST. FETCH
370
PRIORITY
DMA REQUEST SIGNAL
CPU REQUEST SIGNAL
INTERNAL ADDRESS BUS
136
376
DMA COUNTER
378
MUX
PRIORITY
BUS REQUESTS STAY PRESENT UNTIL SERVICED
BUS REQUEST
BUS GRANT
372
BUS CONTROL
374
380
A_{23} — A_{13}
A_{12} — A_2
MUX
MEMORY READY (ACCESS COMPLETED)
RUN (GENERATE MEMORY CYCLE)
400
402
RESET
398
CLE
384
INTERNAL DATA BUS
190
A_{32} — A_{24}
MUXED ADDRESS BUS
A_{23} — A_{13}
A_{12} — A_2
SHIFT REGISTER
390
392
388
394
396
386
MUX
MUX
OE
W
MUX
RAS1
RAS2
CAS1
CAS2
ADDRESS/ DATA
32
382

FIG._12

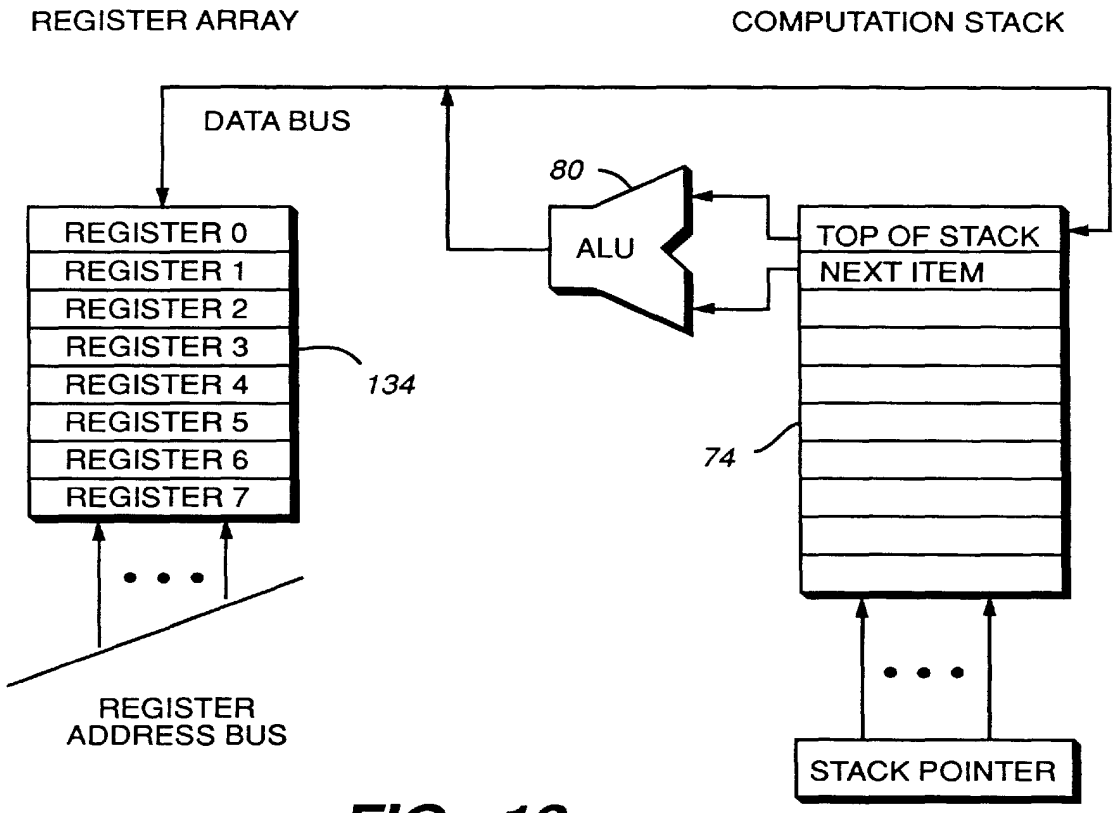

REGISTER ARRAY
COMPUTATION STACK
DATA BUS
80
ALU
REGISTER 0
REGISTER 1
REGISTER 2
REGISTER 3
REGISTER 4
REGISTER 5
REGISTER 6
REGISTER 7
134
TOP OF STACK
NEXT ITEM
74
REGISTER
ADDRESS BUS
STACK POINTER

FIG._13

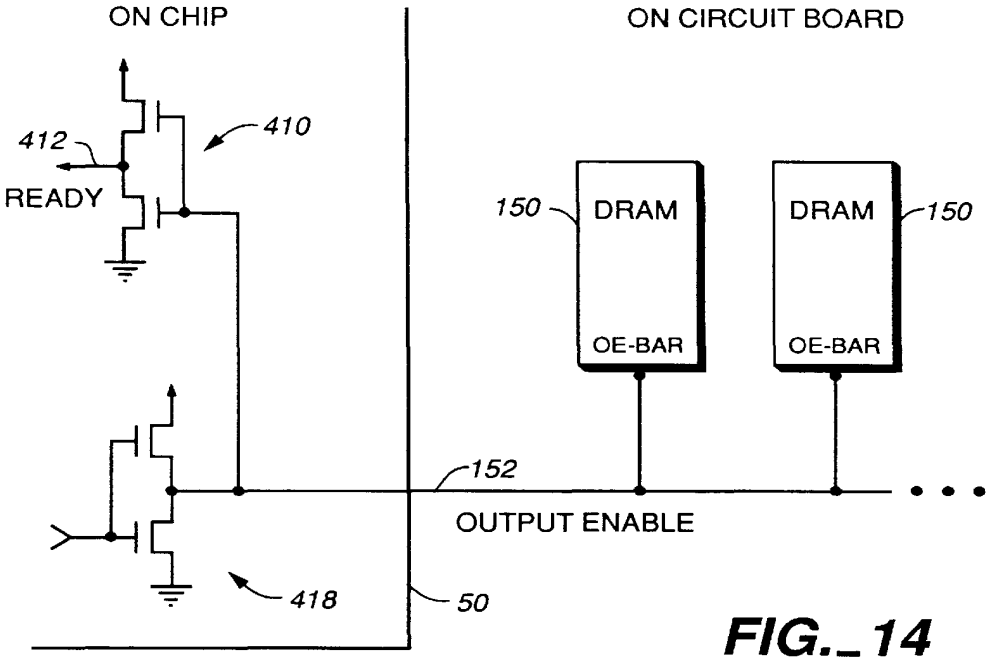

ON CHIP
ON CIRCUIT BOARD
412
410
READY
150
DRAM
OE-BAR
DRAM
OE-BAR
150
152
OUTPUT ENABLE
418
50

FIG._14

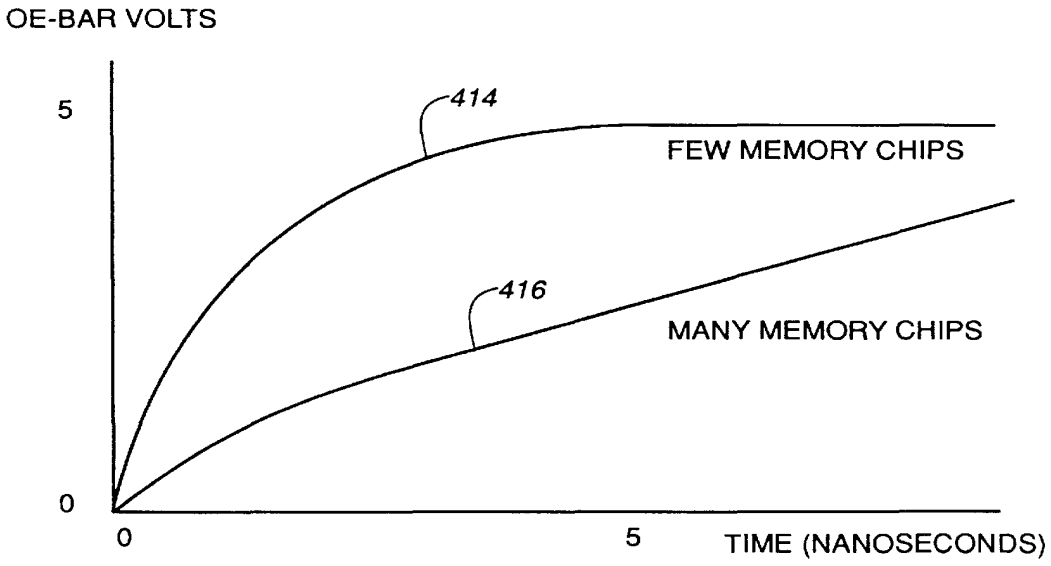

OE-BAR VOLTS
5
0
414
FEW MEMORY CHIPS
416
MANY MEMORY CHIPS
0
5
TIME (NANOSECONDS)

FIG._15

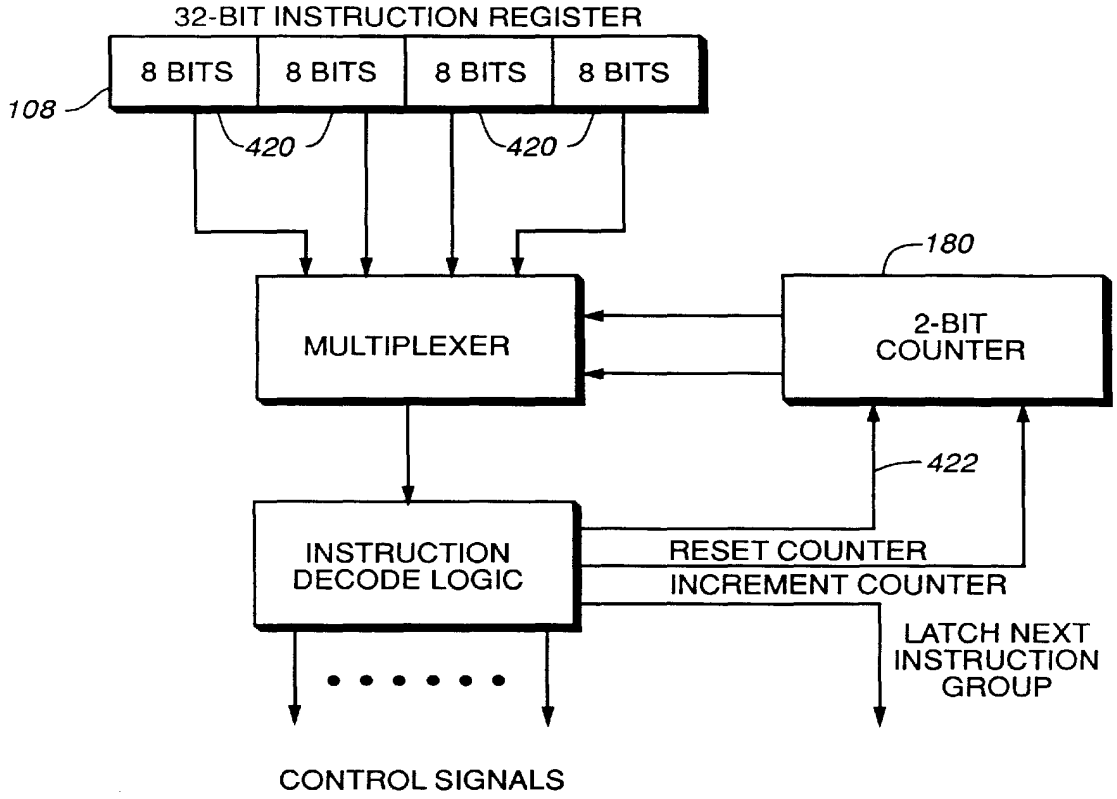

32-BIT INSTRUCTION REGISTER
8 BITS
8 BITS
8 BITS
8 BITS
108
420
420
180
MULTIPLEXER
2-BIT COUNTER
422
INSTRUCTION DECODE LOGIC
RESET COUNTER
INCREMENT COUNTER
LATCH NEXT INSTRUCTION GROUP
CONTROL SIGNALS

FIG._16

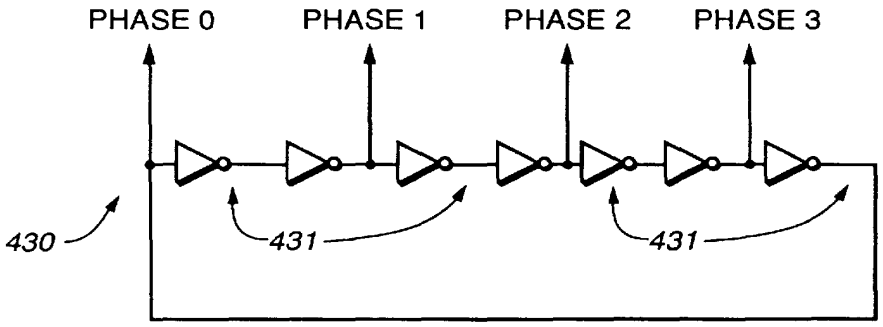

PHASE 0
PHASE 1
PHASE 2
PHASE 3
430
431
431

FIG._18

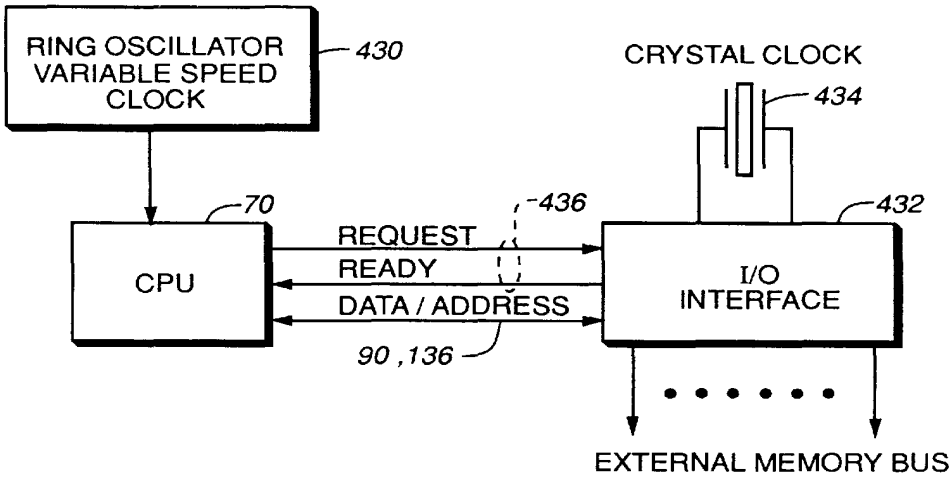

RING OSCILLATOR
VARIABLE SPEED
CLOCK
430
CRYSTAL CLOCK
434
70
436
432
CPU
REQUEST
READY
DATA / ADDRESS
I/O
INTERFACE
90 ,136
EXTERNAL MEMORY BUS

FIG._17

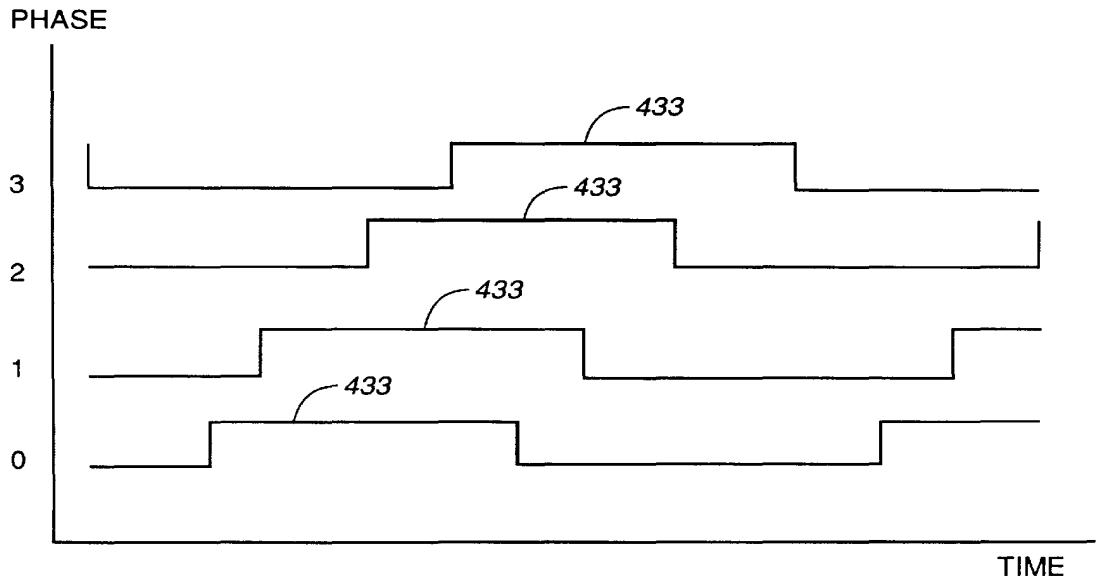

PHASE
433
433
433
433
3
2
1
0
TIME

FIG._19

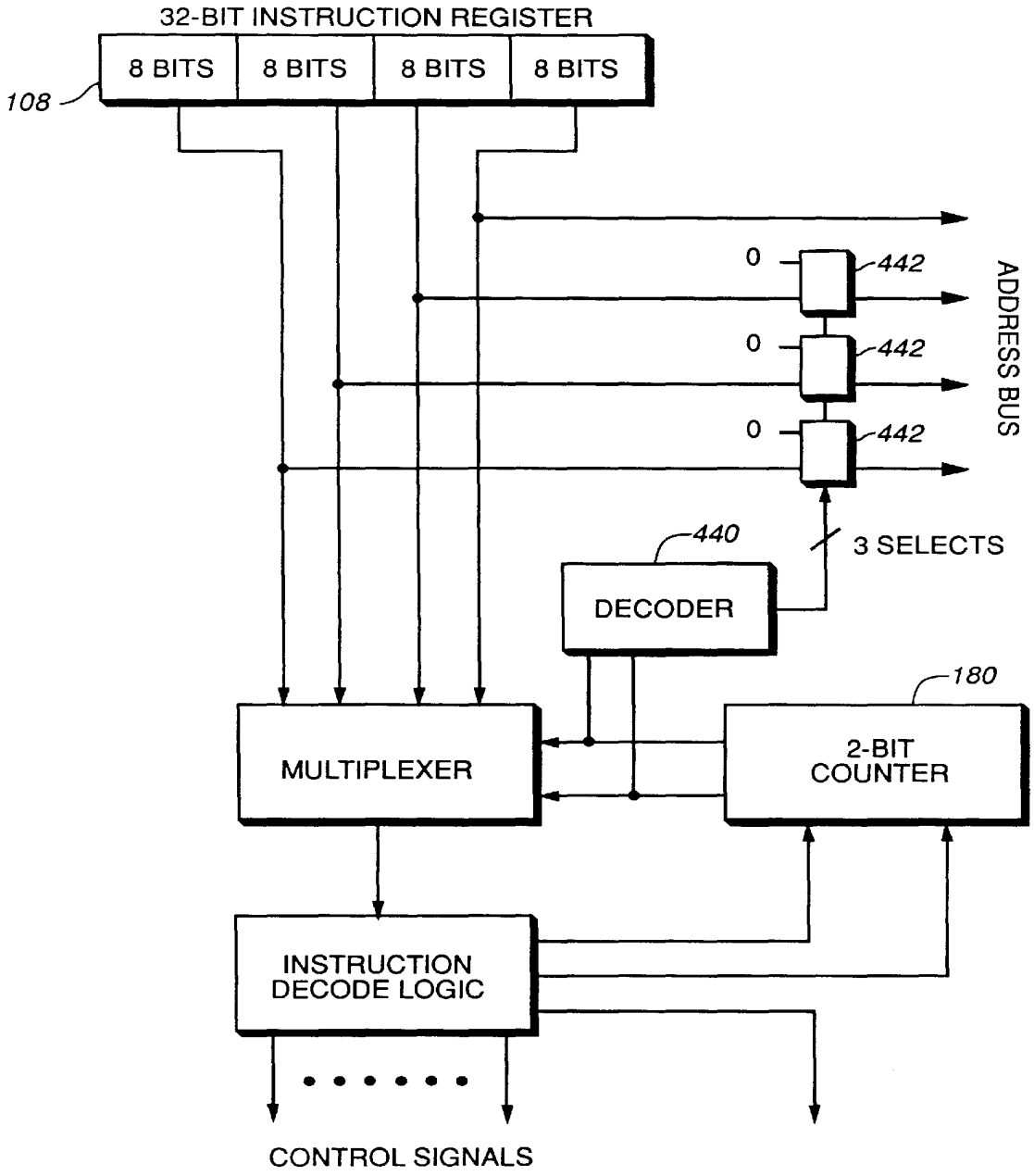

32-BIT INSTRUCTION REGISTER
8 BITS
8 BITS
8 BITS
8 BITS
108
0
442
0
442
0
442
ADDRESS BUS
440
3 SELECTS
DECODER
180
MULTIPLEXER
2-BIT COUNTER
INSTRUCTION DECODE LOGIC
CONTROL SIGNALS

FIG._20

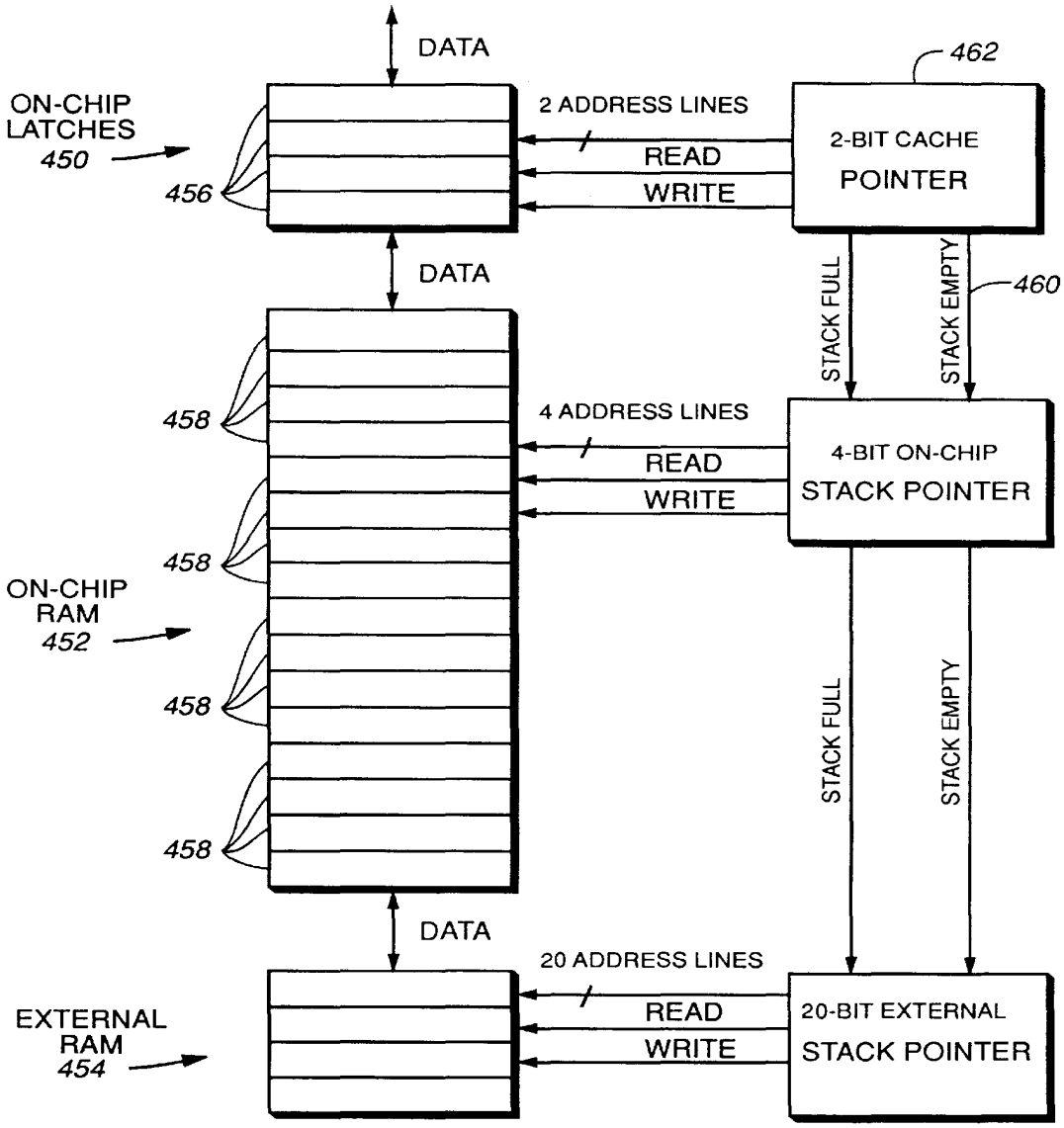

DATA
462
ON-CHIP LATCHES 450
2 ADDRESS LINES
READ
WRITE
2-BIT CACHE POINTER
456
DATA
STACK FULL
STACK EMPTY
460
458
4 ADDRESS LINES
READ
WRITE
4-BIT ON-CHIP STACK POINTER
458
ON-CHIP RAM 452
458
STACK FULL
STACK EMPTY
458
DATA
20 ADDRESS LINES
READ
WRITE
20-BIT EXTERNAL STACK POINTER
EXTERNAL RAM 454

FIG._21

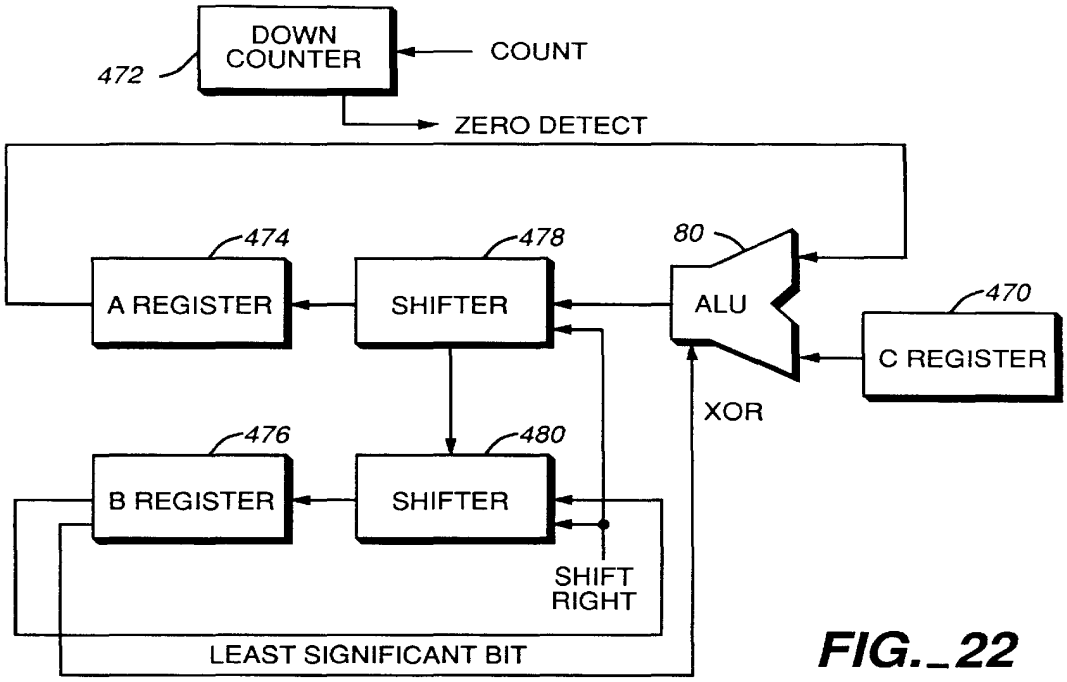

DOWN COUNTER
472
COUNT
ZERO DETECT
474
A REGISTER
478
SHIFTER
80
ALU
470
C REGISTER
XOR
476
B REGISTER
480
SHIFTER
SHIFT RIGHT
LEAST SIGNIFICANT BIT

FIG._22

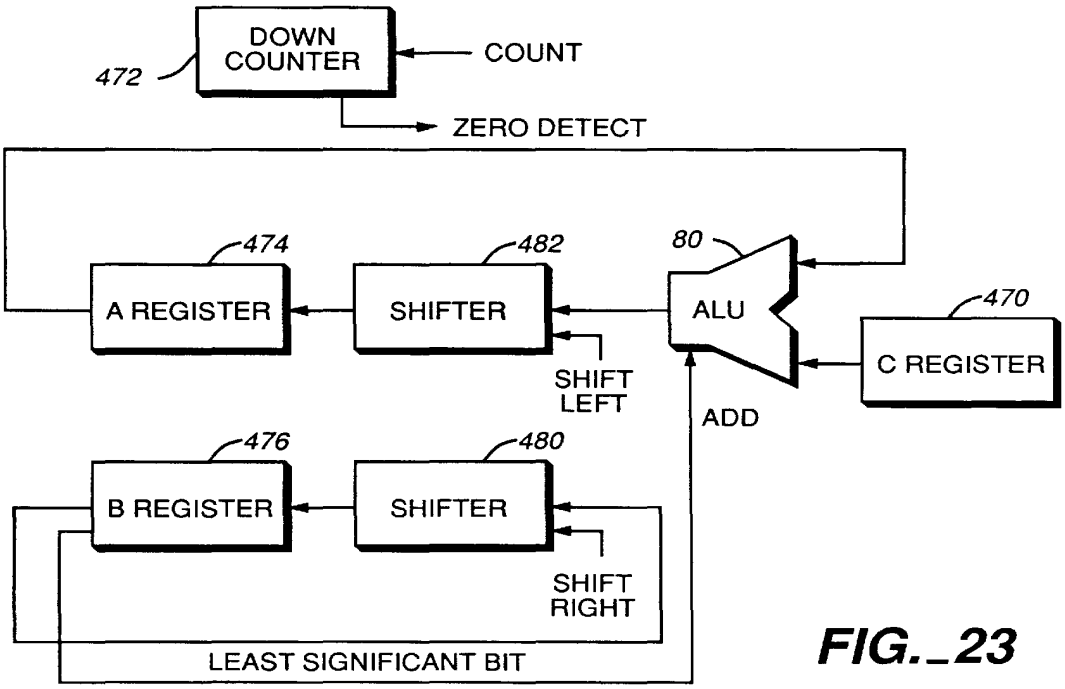

DOWN COUNTER
472
COUNT
ZERO DETECT
474
A REGISTER
482
SHIFTER
80
ALU
470
C REGISTER
SHIFT LEFT
ADD
476
B REGISTER
480
SHIFTER
SHIFT RIGHT
LEAST SIGNIFICANT BIT

FIG._23

HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a division of U.S. application Ser. No. 07/389,334, filed Aug. 3, 1989, now U.S. Pat. No. 5,440,749.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to a simplified, reduced instruction set computer (RISC) microprocessor. More particularly, it relates to such a microprocessor which is capable of performance levels of, for example, 20 million instructions per second (MIPS) at a price of, for example, 20 dollars.

2. Description of the Prior Art

Since the invention of the microprocessor, improvements in its design have taken two different approaches. In the first approach, a brute force gain in performance has been achieved through the provision of greater numbers of faster transistors in the microprocessor integrated circuit and an instruction set of increased complexity. This approach is exemplified by the Motorola 68000 and Intel 80X86 microprocessor families. The trend in this approach is to larger die sizes and packages, with hundreds of pinouts.

More recently, it has been perceived that performance gains can be achieved through comparative simplicity, both in the microprocessor integrated circuit itself and in its instruction set. This second approach provides RISC microprocessors, and is exemplified by the Sun SPARC and the Intel 8960 microprocessors. However, even with this approach as conventionally practiced, the packages for the microprocessor are large, in order to accommodate the large number of pinouts that continue to be employed. A need therefore remains for further simplification of high performance microprocessors.

With conventional high performance microprocessors, fast static memories are required for direct connection to the microprocessors in order to allow memory accesses that are fast enough to keep up with the microprocessors. Slower dynamic random access memories (DRAMs) are used with such microprocessors only in a hierarchical memory arrangement, with the static memories acting as a buffer between the microprocessors and the DRAMs. The necessity to use static memories increases cost of the resulting systems.

Conventional microprocessors provide direct memory accesses (DMA) for system peripheral units through DMA controllers, which may be located on the microprocessor integrated circuit, or provided separately. Such DMA controllers can provide routine handling of DMA requests and responses, but some processing by the main central processing unit (CPU) of the microprocessor is required.

SUMMARY OF THE INVENTION

Accordingly, it is an object of this invention to provide a microprocessor with a reduced pin count and cost compared to conventional microprocessors.

It is another object of the invention to provide a high performance microprocessor that can be directly connected to DRAMs without sacrificing microprocessor speed.

It is a further object of the invention to provide a high performance microprocessor in which DMA does not require use of the main CPU during DMA requests and responses and which provides very rapid DMA response with predictable response times.

The attainment of these and related objects may be achieved through use of the novel high performance, low cost microprocessor herein disclosed. In accordance with one aspect of the invention, a microprocessor system in accordance with this invention has a central processing unit, a dynamic random access memory and a bus connecting the central processing unit to the dynamic random access memory. There is a multiplexing means on the bus between the central processing unit and the dynamic random access memory. The multiplexing means is connected and configured to provide row addresses, column addresses and data on the bus.

In accordance with another aspect of the invention, the microprocessor system has a means connected to the bus for fetching instructions for the central processing unit on the bus. The means for fetching instructions is configured to fetch multiple sequential instructions in a single memory cycle. In a variation of this aspect of the invention, a programmable read only memory containing instructions for the central processing unit is connected to the bus. The means for fetching instructions includes means for assembling a plurality of instructions from the programmable read only memory and storing the plurality of instructions in the dynamic random access memory.

In another aspect of the invention, the microprocessor system includes a central processing unit, a direct memory access processing unit and a memory connected by a bus. The direct memory access processing unit includes means for fetching instructions for the central processing unit and for fetching instructions for the direct memory access processing unit on the bus.

In a further aspect of the invention, the microprocessor system, including the memory, is contained in an integrated circuit. The memory is a dynamic random access memory, and the means for fetching multiple instructions includes a column latch for receiving the multiple instructions.

In still another aspect of the invention, the microprocessor system additionally includes an instruction register for the multiple instructions connected to the means for fetching instructions. A means is connected to the instruction register for supplying the multiple instructions in succession from the instruction register. A counter is connected to control the means for supplying the multiple instructions to supply the multiple instructions in succession. A means for decoding the multiple instructions is connected to receive the multiple instructions in succession from the means for supplying the multiple instructions. The counter is connected to said means for decoding to receive incrementing and reset control signals from the means for decoding. The means for decoding is configured to supply the reset control signal to the counter and to supply a control signal to the means for fetching instructions in response to a SKIP instruction in the multiple instructions. In a modification of this aspect of the invention, the microprocessor system additionally has a loop counter connected to receive a decrement control signal from the means for decoding. The means for decoding is configured to supply the reset control signal to the counter and the decrement control signal to the loop counter in response to a MICROLOOP instruction in the multiple instructions. In a further modification to this aspect of the invention, the means for decoding is configured to control

the counter in response to an instruction utilizing a variable width operand. A means is connected to the counter to select the variable width operand in response to the counter.

In a still further aspect of the invention, the microprocessor system includes an arithmetic logic unit. A first push down stack is connected to the arithmetic logic unit. The first push down stack includes means for storing a top item connected to a first input of the arithmetic logic unit and means for storing a next item connected to a second input of the arithmetic logic unit. The arithmetic logic unit has an output connected to the means for storing a top item. The means for storing a top item is connected to provide an input to a register file. The register file desirably is a second push down stack, and the means for storing a top item and the register file are bidirectionally connected.

In another aspect of the invention, a data processing system has a microprocessor including a sensing circuit and a driver circuit, a memory, and an output enable line connected between the memory, the sensing circuit and the driver circuit. The sensing circuit is configured to provide a ready signal when the output enable line reaches a predetermined electrical level, such as a voltage. The microprocessor is configured so that the driver circuit provides an enabling signal on the output enable line responsive to the ready signal.

In a further aspect of the invention, the microprocessor system has a ring counter variable speed system clock connected to the central processing unit. The central processing unit and the ring counter variable speed system clock are provided in a single integrated circuit. An input/output interface is connected to exchange coupling control signals, addresses and data with the input/output interface. A second clock independent of the ring counter variable speed system clock is connected to the input/output interface.

In yet another aspect of the invention, a push down stack is connected to the arithmetic logic unit. The push down stack includes means for storing a top item connected to a first input of the arithmetic logic unit and means for storing a next item connected to a second input of the arithmetic logic unit. The arithmetic logic unit has an output connected to the means for storing a top item. The push down stack has a first plurality of stack elements configured as latches and a second plurality of stack elements configured as a random access memory. The first and second plurality of stack elements and the central processing unit are provided in a single integrated circuit. A third plurality of stack elements is configured as a random access memory external to the single integrated circuit. In this aspect of the invention, desirably a first pointer is connected to the first plurality of stack elements, a second pointer connected to the second plurality of stack elements, and a third pointer is connected to the third plurality of stack elements. The central processing unit is connected to pop items from the first plurality of stack elements. The first stack pointer is connected to the second stack pointer to pop a first plurality of items from the second plurality of stack elements when the first plurality of stack elements are empty from successive pop operations by the central processing unit. The second stack pointer is connected to the third stack pointer to pop a second plurality of items from the third plurality of stack elements when the second plurality of stack elements are empty from successive pop operations by the central processing unit.

In another aspect of the invention, a first register is connected to supply a first input to the arithmetic logic unit. A first shifter is connected between an output of the arithmetic logic unit and the first register. A second register is connected to receive a starting polynomial value. An output of the second register is connected to a second shifter. A least significant bit of the second register is connected to The arithmetic logic unit. A third register is connected to supply feedback terms of a polynomial to the arithmetic logic unit. A down counter, for counting down a number corresponding to digits of a polynomial to be generated, is connected to the arithmetic logic unit. The arithmetic logic unit is responsive to a polynomial instruction to carry out an exclusive OR of the contents of the first register with the contents of the third register if the least significant bit of the second register is a "ONE" and to pass the contents of the first register unaltered if the least significant bit of the second register is a "ZERO", until the down counter completes a count. The polynomial to be generated results in said first register.

In still another aspect of the invention, a result register is connected to supply a first input to the arithmetic logic unit. A first, left shifting shifter is connected between an output of the arithmetic logic unit and the result register. A multiplier register is connected to receive a multiplier in bit reversed form. An output of the multiplier register is connected to a second, right shifting shifter. A least significant bit of the multiplier register is connected to the arithmetic logic unit. A third register is connected to supply a multiplicand to said arithmetic logic unit. A down counter, for counting down a number corresponding to one less than the number of digits of the multiplier, is connected to the arithmetic logic unit. The arithmetic logic unit is responsive to a multiply instruction to add the contents of the result register with the contents of the third register, when the least significant bit of the multiplier register is a "ONE" and to pass the contents of the result register unaltered, until the down counter completes a count. The product results in the result register.

The attainment of the foregoing and related objects, advantages and features of the invention should be more readily apparent to those skilled in the art, after review of the following more detailed description of the invention, taken together with the drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an external, plan view of an integrated circuit package incorporating a microprocessor in accordance with the invention.

FIG. **2** is a block diagram of a microprocessor in accordance with the invention.

FIG. **3** is a block diagram of a portion of a data processing system incorporating the microprocessor of FIGS. **1** and **2**.

FIG. **4** is a more detailed block diagram of a portion of the microprocessor shown in FIG. **2**.

FIG. **5** is a more detailed block diagram of another portion of the microprocessor shown in FIG. **2**.

FIG. **6** is a block diagram of another portion of the data processing system shown in part in FIG. **3** and incorporating the microprocessor of FIGS. **1–2** and **4–5**.

FIGS. **7** and **8** are layout diagrams for the data processing system shown in part in FIGS. **3** and **6**.

FIG. **9** is a layout diagram of a second embodiment of a microprocessor in accordance with the invention in a data processing system on a single integrated circuit.

FIG. **10** is a more detailed block diagram of a portion of the data processing system of FIGS. **7** and **8**.

FIG. **11** is a timing diagram useful for understanding operation of the system portion shown in FIG. **12**.

FIG. **12** is another more detailed block diagram of a further portion of the data processing system of FIGS. **7** and **8**.

FIG. **13** is a more detailed block diagram of a portion of the microprocessor shown in FIG. **2**.

FIG. **14** is a more detailed block and schematic diagram of a portion of the system shown in FIGS. **3** and **7–8**.

FIG. **15** is a graph useful for understanding operation of the system portion shown in FIG. **14**.

FIG. **16** is a more detailed block diagram showing part of the system portion shown in FIG. **4**.

FIG. **17** is a more detailed block diagram of a portion of the microprocessor shown in FIG. **2**.

FIG. **18** is a more detailed block diagram of part of the microprocessor portion shown in FIG. **17**.

FIG. **19** is a set of waveform diagrams useful for understanding operation of the part of the microprocessor portion shown in FIG. **18**.

FIG. **20** is a more detailed block diagram showing another part of the system portion shown in FIG. **4**.

FIG. **21** is a more detailed block diagram showing another part of the system portion shown in FIG. **4**.

FIGS. **22** and **23** are more detailed block diagrams showing another part of the system portion shown in FIG. **4**.

DETAILED DESCRIPTION OF THE INVENTION

Overveiw

The microprocessor of this invention is desirably implemented as a 32-bit microprocessor optimized for:

HIGH EXECUTION SPEED, and

LOW SYSTEM COST.

In this embodiment, the microprocessor can be thought of as 20 MIPS for 20 dollars. Important distinguishing features of the microprocessor are:

Uses low-cost commodity DYNAMIC RAMS to run 20 MIPS

4 instruction fetch per memory cycle

On-chip fast page-mode memory management

Runs fast without external cache

Requires few interfacing chips

Crams 32-bit CPU in 44 pin SOJ package

The instruction set is organized so that most operations can be specified with 8-bit instructions. Two positive products of this philosophy are:

Programs are smaller,

Programs can execute much faster.

The bottleneck in most computer systems is the memory bus. The bus is used to fetch instructions and fetch and store data. The ability to fetch four instructions in a single memory bus cycle significantly increases the bus availability to handle data.

Turning now to the drawings, more particularly to FIG. **1**, there is shown a packaged 32-bit microprocessor **50** in a 44-pin plastic leadless chip carrier, shown approximately 100 times its actual size of about 0.8 inch on a side. The fact that the microprocessor **50** is provided as a 44-pin package represents a substantial departure from typical microprocessor packages, which usually have about 200 input/output (I/O) pins. The microprocessor **50** is rated at 20 million instructions per second (MIPS). Address and data lines **52**, also labelled **D0–D31**, are shared for addresses and data without speed penalty as a result of the manner in which the microprocessor **50** operates, as will be explained below.

DYNAMIC RAM

In addition to the low cost 44-pin package, another unusual aspect of the high performance microprocessor **50** is that it operates directly with dynamic random access memories (DRAMs), as shown by row address strobe (RAS) and column address strobe (CAS) I/O pins **54**. The other I/O pins for the microprocessor **50** include V_{DD} pins **56**, V_{SS} pins **58**, output enable pin **60**, write pin **62**, clock pin **64** and reset pin **66**.

All high speed computers require high speed and expensive memory to keep up. The highest speed static RAM memories cost as much as ten times as much as slower dynamic RAMs. This microprocessor has been optimized to use low-cost dynamic RAM in high-speed page-mode. Page-mode dynamic RAMs offer static RAM performance without the cost penalty. For example, low-cost 85 nsec. dynamic RAMs access at 25 nsec when operated in fast page-mode. Integrated fast page-mode control on the microprocessor chip simplifies system interfacing and results in a faster system.

Details of the microprocessor **50** are shown in FIG. **2**. The microprocessor **50** includes a main central processing unit (CPU) **70** and a separate direct memory access (DMA) CPU **72** in a single integrated circuit making up the microprocessor **50**. The main CPU **70** has a first **16** deep push down stack **74**, which has a top item register **76** and a next item register **78**, respectively connected to provide inputs to an arithmetic logic unit (ALU) **80** by lines **82** and **84**. An output of the ALU **80** is connected to the top item register **76** by line **86**. The output of the top item register at **82** is also connected by line **88** to an internal data bus **90**.

A loop counter **92** is connected to a decrementer **94** by lines **96** and **98**. The loop counter **92** is bidirectionally connected to the internal data bus **90** by line **100**. Stack pointer **102**, return stack pointer **104**, mode register **106** and instruction register **108** are also connected to the internal data bus **90** by lines **110**, **112**, **114** and **116**, respectively. The internal data bus **90** is connected to memory controller **118** and to gate **120**. The gate **120** provides inputs on lines **122**, **124**, and **126** to X register **128**, program counter **130** and Y register **132** of return push down stack **134**. The X register **128**, program counter **130** and Y register **132** provide outputs to internal address bus **136** on lines **138**, **140** and **142**. The internal address bus provides inputs to the memory controller **118** and to an incrementer **144**. The incrementer **144** provides inputs to the X register, program counter and Y register via lines **146**, **122**, **124** and **126**. The DMA CPU **72** provides inputs to the memory controller **118** on line **148**. The memory controller **118** is connected to a RAM (not shown) by address/data bus **150** and control lines **152**.

FIG. **2** shows that the microprocessor **50** has a simple architecture. Prior art RISC microprocessors are substantially more complex in design. For example, the SPARC RISC microprocessor has three times the gates of the microprocessor **50**, and the Intel 8960 RISC microprocessor has 20 times the gates of the microprocessor **50**. The speed of this microprocessor is in substantial part due to this simplicity. The architecture incorporates push down stacks and register write to achieve this simplicity.

The microprocessor **50** incorporates an I/O that has been tuned to make heavy use of resources provided on the integrated circuit chip. On chip latches allow use of the same I/O circuits to handle three different things: column addressing, row addressing and data, with a slight to non-existent speed penalty. This triple bus multiplexing results in fewer buffers to expand, fewer interconnection lines, fewer I/O pins and fewer internal buffers.

The provision of on-chip DRAM control gives a performance equal to that obtained with the use of static RAMs. As a result, memory is provided at ¼ the system cost of static RAM used in most RISC systems.

The microprocessor **50** fetches 4 instructions per memory cycle; the instructions are in an 8-bit format, and this is a 32-bit microprocessor. System speed is therefore 4 times the memory bus bandwidth. This ability enables the microprocessor to break the Von Neumann bottleneck of the speed of getting the next instruction. This mode of operation is possible because of the use of a push down stack and register array. The push down stack allows the use of implied addresses, rather than the prior art technique of explicit addresses for two sources and a destination.

Most instructions execute in 20 nanoseconds in the microprocessor **50**. The microprocessor can therefore execute instructions at 50 peak MIPS without pipeline delays. This is a function of the small number of gates in the microprocessor **50** and the high degree of parallelism in the architecture of the microprocessor.

FIG. **3** shows how column and row addresses are multiplexed on lines D**8**–D**14** of the microprocessor **50** for addressing DRAM **150** from I/O pins **52**. The DRAM **150** is one of eight, but only one DRAM **150** has been shown for clarity. As shown, the lines D**11**–D**18** are respectively connected to row address inputs A**0**–A**8** of the DRAM **150**. Additionally, lines D**12**–D**15** are connected to the data inputs DQ**1**–DQ**4** of the DRAM **150**. The output enable, write and column address strobe pins **54** are respectively connected to the output enable, write and column address strobe inputs of the DRAM **150** by lines **152**. The row address strobe pin **54** is connected through row address strobe decode logic **154** to the row address strobe input of the DRAM **150** by lines **156** and **158**.

D**0**–D**7** pins **52** (FIG. **1**) are idle when the microprocessor **50** is outputting multiplexed row and column addresses on D**11**–D**18** pins **52**. The D**0**–D**7** pins **52** can therefore simultaneously be used for I/O when right justified I/O is desired. Simultaneous addressing and I/O can therefore be carried out.

FIG. **4** shows how the microprocessor **50** is able to achieve performance equal to the use of static RAMS with DRAMs through multiple instruction fetch in a single clock cycle and instruction fetch-ahead. Instruction register **108** receives four 8-bit byte instruction words 1–4 on 32-bit internal data bus **90**. The four instruction byte 1–4 locations of the instruction register **108** are connected to multiplexer **170** by busses **172**, **174**, **176** and **178**, respectively. A microprogram counter **180** is connected to the multiplexer **170** by lines **182**. The multiplexer **170** is connected to decoder **184** by bus **186**. The decoder **184** provides internal signals to the rest of the microprocessor **50** on lines **188**.

Most significant bits **190** of each instruction byte 1–4 location are connected to a 4-input decoder **192** by lines **194**. The output of decoder **192** is connected to memory controller **118** by line **196**. Program counter **130** is connected to memory controller **118** by internal address bus **136**, and the instruction register **108** is connected to the memory controller **118** by the internal data bus **90**. Address/data bus **198** and control bus **200** are connected to the DRAMS **150** (FIG. **3**).

In operation, when the most significant bits **190** of remaining instructions 1–4 are "1" in a clock cycle of the microprocessor **50**, there are no memory reference instructions in the queue. The output of decoder **192** on line **196** requests an instruction fetch ahead by memory controller **118** without interference with other accesses. While the current instructions in instruction register **108** are executing, the memory controller **118** obtains the address of the next set of four instructions from program counter **130** and obtains that set of instructions. By the time the current set of instructions has completed execution, the next set of instructions is ready for loading into the instruction register.

Details of the DMA CPU **72** are provided in FIG. **5**. Internal data bus **90** is connected to memory controller **118** and to DMA instruction register **210**. The DMA instruction register **210** is connected to DMA program counter **212** by bus **214**, to transfer size counter **216** by bus **218** and to timed transfer interval counter **220** by bus **222**. The DMA instruction register **210** is also connected to DMA I/O and RAM address register **224** by line **226**. The DMA I/O and RAM address register **224** is connected to the memory controller **118** by memory cycle request line **228** and bus **230**. The DMA program counter **212** is connected to the internal address bus **136** by bus **232**. The transfer size counter **216** is connected to a DMA instruction done decrementer **234** by lines **236** and **238**. The decrementer **234** receives a control input on memory cycle acknowledge line **240**. When transfer size counter **216** has completed its count, it provides a control signal to DMA program counter **212** on line **242**. Timed transfer interval counter **220** is connected to decrementer **244** by lines **246** and **248**. The decrementer **244** receives a control input from a microprocessor system clock on line **250**.

The DMA CPU **72** controls itself and has the ability to fetch and execute instructions. It operates as a co-processor to the main CPU **70** (FIG. **2**) for time specific processing.

FIG. **6** shows how the microprocessor **50** is connected to an electrically programmable read only memory (EPROM) **260** by reconfiguring the data lines **52** so that some of the data lines **52** are input lines and some of them are output lines. Data lines **52** D**0**–D**7** provide data to and from corresponding data terminals **262** of the EPROM **260**. Data lines **52** D**9**–D**18** provide addresses to address terminals **264** of the EPROM **260**. Data lines **52** D**19**–D**31** provide inputs from the microprocessor **50** to memory and I/O decode logic **266**. RAS 0/1 control line **268** provides a control signal for determining whether the memory and I/O decode logic provides a DRAM RAS output on line **270** or a column enable output for the EPROM **260** on line **272**. Column address strobe terminal **60** of the microprocessor **50** provides an output enable signal on line **274** to the corresponding terminal **276** of the EPROM **260**.

FIGS. **7** and **8** show the front and back of a one card data processing system **280** incorporating the microprocessor **50**, MSM514258-10 type DRAMs **150** totalling 2 megabytes, a Motorola 50 MegaHertz crystal oscillator clock **282**, I/O circuits **284** and a 27256 type EPROM **260**. The I/O circuits **284** include a 74HC04 type high speed hex inverter circuit **286**, an IDT39C828 type 10-bit inverting buffer circuit **288**, an IDT39C822 type 10-bit inverting register circuit **290**, and two IDT39C823 type 9-bit non-inverting register circuits **292**. The card **280** is completed with a MAX12V type DC-DC converter circuit **294**, 34-pin dual AMP type headers **296**, a coaxial female power connector **298**, and a 3-pin AMP right angle header **300**. The card **280** is a low cost, imbeddable product that can be incorporated in larger systems or used as an internal development tool.

The microprocessor **50** is a very high performance (50 MHz) RISC influenced 32-bit CPU designed to work closely with dynamic RAM. Clock for clock, the microprocessor **50** approaches the theoretical performance limits possible with a single CPU configuration. Eventually, the microprocessor **50** and any other processor is limited by the bus bandwidth and the number of bus paths. The critical conduit is between the CPU and memory.

One solution to the bus bandwidth/bus path problem is to integrate a CPU directly onto the memory chips, giving every memory a direct bus the CPU. FIG. **9** shows another microprocessor **310** that is provided integrally with 1 mega-

bit of DRAM **311** in a single integrated circuit **312**. Until the present invention, this solution has not been practical, because most high performance CPUs require from 500,000 to 1,000,000 transistors and enormous die sizes just by themselves. The microprocessor **310** is equivalent to the microprocessor **50** in FIGS. **1–8**. The microprocessors **50** and **310** are the most transistor efficient high performance CPUs in existence, requiring fewer than 50,000 transistors for dual processors **70** and **72** (FIG. **2**) or **314** and **316** (less memory). The very high speed of the microprocessors **50** and **310** is to a certain extent a function of the small number of active devices. In essence, the less silicon gets in the way, the faster the electrons can get where they are going.

The microprocessor **310** is therefore the only CPU suitable for integration on the memory chip die **312**. Some simple modifications to the basic microprocessor **50** to take advantage of the proximity to the DRAM array **311** can also increase the microprocessor **50** clock speed by **50** percent, and probably more.

The microprocessor **310** core on board the DRAM die **312** provides most of the speed and functionality required for a large group of applications from automotive to peripheral control. However, the integrated CPU **310**/DRAM **311** concept has the potential to redefine significantly the way multiprocessor solutions can solve a spectrum of very compute intensive problems. The CPU **310**/DRAM **311** combination eliminates the Von Neumann bottleneck by distributing it across numerous CPU/DRAM chips **312**. The microprocessor **310** is a particularly good core for multiprocessing, since it was designed with the SDI targeting array in mind, and provisions were made for efficient interprocessor communications.

Traditional multiprocessor implementations have been very expensive in addition to being unable to exploit fully the available CPU horsepower. Multiprocessor systems have typically been built up from numerous board level or box level computers. The result is usually an immense amount of hardware with corresponding wiring, power consumption and communications problems. By the time the systems are interconnected, as much as 50 percent of the bus speed has been utilized just getting through the interfaces.

In addition, multiprocessor system software has been scarce. A multiprocessor system can easily be crippled by an inadequate load-sharing algorithm in the system software, which allows one CPU to do a great deal of work and the others to be idle. Great strides have been made recently in systems software, and even UNIX V.4 may be enhanced to support multiprocessing. Several commercial products from such manufacturers as DUAL Systems and UNISOFT do a credible job on 68030 type microprocessor systems now.

The microprocessor **310** architecture eliminates most of the interface friction, since up to 64 CPU **310**/RAM **311** processors should be able to intercommunicate without buffers or latches. Each chip **312** has about 40 MIPS raw speed, because placing the DRAM **311** next to the CPU **310** allows the microprocessor **310** instruction cycle to be cut in half, compared to the microprocessor **50**. A 64 chip array of these chips **312** is more powerful than any other existing computer. Such an array fits on a 3×5 card, cost less than a FAX machine, and draw about the same power as a small television.

Dramatic changes in price/performance always reshape existing applications and almost always create new ones. The introduction of microprocessors in the mid 1970s created video games, personal computers, automotive computers, electronically controlled appliances, and low cost computer peripherals.

The integrated circuit **312** will find applications in all of the above areas, plus create some new ones. A common generic parallel processing algorithm handles convolution/Fast Fourier Transform (FFT)/pattern recognition. Interesting product possibilities using the integrated circuit **312** include high speed reading machines, real-time speech recognition, spoken language translation, real-time robot vision, a product to identify people by their faces, and an automotive or aviation collision avoidance system.

A real time processor for enhancing high density television (HDTV) images, or compressing the HDTV information into a smaller bandwidth, would be very. feasible. The load sharing in HDTV could be very straightforward. Splitting up the task according to color and frame would require 6, 9 or 12 processors. Practical implementation might require 4 meg RAMs integrated with the microprocessor **310**.

The microprocessor **310** has the following specifications:

CONTROL LINES
4—POWER/GROUND
1—CLOCK
32—DATA I/O
4—SYSTEM CONTROL
EXTERNAL MEMORY FETCH
EXTERNAL MEMORY FETCH AUTOINCREMENT X
EXTERNAL MEMORY FETCH AUTOINCREMENT Y
EXTERNAL MEMORY WRITE
EXTERNAL MEMORY WRITE AUTOINCREMENT X
EXTERNAL MEMORY WRITE AUTOINCREMENT Y
EXTERNAL PROM FETCH
LOAD ALL X REGISTERS
LOAD ALL Y REGISTERS
LOAD ALL PC REGISTERS
EXCHANGE X AND Y
INSTRUCTION FETCH
ADD TO PC
ADD TO X
WRITE MAPPING REGISTER
READ MAPPING REGISTER
REGISTER CONFIGURATION
MICROPROCESSOR **310** CPU **316** CORE
COLUMN LATCH**1** (1024 BITS) 32×32 MUX
STACK POINTER (16 BITS)
COLUMN LATCH**2** (1024 BITS) 32×32 MUX
RSTACK POINTER (16 BITS)
PROGRAM COUNTER 32 BITS
X0 REGISTER 32 BITS (ACTIVATED ONLY FOR ON-CHIP ACCESSES)
Y0 REGISTER 32 BITS (ACTIVATED ONLY FOR ON-CHIP ACCESSES)
LOOP COUNTER 32 BITS
DMA CPU **314** CORE
DMA PROGRAM COUNTER 24 BITS
INSTRUCTION REGISTER 32 BITS
I/O & RAM ADDRESS REGISTER 32 BITS
TRANSFER SIZE COUNTER 12 BITS
INTERVAL COUNTER 12 BITS

To offer memory expansion for the basic chip **312**, an intelligent DRAM can be produced. This chip will be optimized for high speed operation with the integrated circuit **312** by having three on-chip address registers: Program Counter, X Register and Y register. As a result, to access the intelligent DRAM, no address is required, and a total access cycle could be as short as 10 nsec. Each

expansion DRAM would maintain its own copy of the three registers and would be identified by a code specifying its memory address. Incrementing and adding to the three registers will actually take place on the memory chips. A maximum of 64 intelligent DRAM peripherals would allow a large system to be created without sacrificing speed by introducing multiplexers or buffers.

There are certain differences between the microprocessor **310** and the microprocessor **50** that arise from providing the microprocessor **310** on the same die **312** with the DRAM **311**. Integrating the DRAM **311** allows architectural changes in the microprocessor **310** logic to take advantage of existing on-chip DRAM **311** circuitry. Row and column design is inherent in memory architecture. The DRAMs **311** access random bits in a memory array by first selecting a row of 1024 bits, storing them into a column latch, and then selecting one of the bits as the data to be read or written.

The time required to access the data is split between the row access and the column access. Selecting data already stored in a column latch is faster than selecting a random bit by at least a factor of six. The microprocessor **310** takes advantage of this high speed by creating a number of column latches and using them as caches and shift registers. Selecting a new row of information may be thought of as performing a 1024-bit read or write with the resulting immense bus bandwidth.

1. The microprocessor **50** treats its 32-bit instruction register **108** (see FIGS. **2** and **4**) as a cache for four 8-bit instructions. Since the DRAM **311** maintains a 1024-bit latch for the column bits, the microprocessor **310** treats the column latch as a cache for 128 8-bit instructions. Therefore, the next instruction will almost always be already present in the cache. Long loops within the cache are also possible and more useful than the 4 instruction loops in the microprocessor **50**.

2. The microprocessor **50** uses two 16×32-bit deep register arrays **74** and **134** (FIG. **2**) for the parameter stack and the return stack. The microprocessor **310** creates two other 1024-bit column latches to provide the equivalent of two 32×32-bit arrays, which can be accessed twice as fast as a register array.

3. The microprocessor **50** has a DMA capability which can be used for I/O to a video shift register. The microprocessor **310** uses yet another 1024-bit column latch as a long video shift register to drive a CRT display directly. For color displays, three on-chip shift registers could also be used. These shift registers can transfer pixels at a maximum of 100 MHz.

4. The microprocessor **50** accesses memory via an external 32-bit bus. Most of the memory **311** for the microprocessor **310** is on the same die **312**. External access to more memory is made using an 8-bit bus. The result is a smaller die, smaller package and lower power consumption than the microprocessor **50**.

5. The microprocessor **50** consumes about a third of its operating power charging and discharging the I/O pins and associated capacitances. The DRAMs **150** (FIG. **8**) connected to the microprocessor **50** dissipate most of their power in the I/O drivers. A microprocessor **310** system will consume about one-tenth the power of a microprocessor **50** system, since having the DRAM **311** next to the processor **310** eliminates most of the external capacitances to be charged and discharged.

6. Multiprocessing means splitting a computing task between numerous processors in order to speed up the solution. The popularity of multiprocessing is limited by the expense of current individual processors as well as the limited interprocessor communications ability. The microprocessor **310** is an excellent multiprocessor candidate, since the chip **312** is a monolithic computer complete with memory, rendering it low-cost and physically compact.

The shift registers implemented with the microprocessor **310** to perform video output can also be configured as interprocessor communication links. The INMOS transputer attempted a similar strategy, but at much lower speed and without the performance benefits inherent in the microprocessor **310** column latch architecture. Serial I/O is a prerequisite for many multiprocessor topologies because of the many neighbor processors which communicate. A cube has 6 neighbors. Each neighbor communicates using these lines:

DATA IN
CLOCK IN
READY FOR DATA
DATA OUT
DATA READY?
CLOCK OUT

A special start up sequence is used to initialize the on-chip DRAM **311** in each of the processors.

The microprocessor **310** column latch architecture allows neighbor processors to deliver information directly to internal registers or even instruction caches of other chips **312**. This technique is not used with existing processors, because it only improves performance in a tightly coupled DRAM system.

7. The microprocessor **50** architecture offers two types of looping structures: LOOP-IF-DONE and MICRO-LOOP. The former takes an 8-bit to 24-bit operand to describe the entry point to the loop address. The latter performs a loop entirely within the 4 instruction queue and the loop entry point is implied as the first instruction in the queue. Loops entirely within the queue run without external instruction fetches and execute up to three times as fast as the long loop construct. The microprocessor **310** retains both constructs with a few differences. The microprocessor **310** microloop functions in the same fashion as the microprocessor **50** operation, except the queue is 1024-bits or 128 8-bit instructions long. The microprocessor **310** microloop can therefore contain jumps, branches, calls and immediate operations not possible in the 4 8-bit instruction microprocessor **50** queue.

Microloops in the microprocessor **50** can only perform simple block move and compare functions. The larger microprocessor **310** queue allows entire digital signal processing or floating point algorithms to loop at high speed in the queue.

The microprocessor **50** offers four instructions to redirect execution:

CALL
BRANCH
BRANCH-IF-ZERO
LOOP-IF-NOT-DONE

These instructions take a variable length address operand 8, 16 or 24 bits long. The microprocessor **50** next address logic treats the three operands similarly by adding or subtracting them to the current program counter. For the microprocessor **310**, the 16 and 24-bit operands function in the same manner as the 16 and 24-bit operands in the microprocessor **50**. The 8-bit class operands are reserved to operate entirely within the instruction queue. Next address decisions can therefore be made quickly, because only 10 bits of addresses are affected, rather than 32. There is no carry or borrow generated past the 10 bits.

8. The microprocessor **310** CPU **316** resides on an already crowded DRAM die **312**. To keep chip size as small as

possible, the DMA processor **72** of the microprocessor **50** has been replaced with a more traditional DMA controller **314**. DMA is used with the microprocessor **310** to perform the following functions:

Video output to a CRT

Multiprocessor serial communications

8-bit parallel I/O

The DMA controller **314** can maintain both serial and parallel transfers simultaneously. The following DMA sources and destinations are supported by the microprocessor **310**:

DESCRIPTION	I/O	LINES
1. Video shift register	OUTPUT	1 to 3
2. Multiprocessor serial	BOTH	6 lines/channel
3. 8-bit parallel	BOTH	8 data, 4 control

The three sources use separate 1024-bit buffers and separate I/O pins. Therefore, all three may be active simultaneously without interference.

The microprocessor **310** can be implemented with either a single multiprocessor serial buffer or separate receive and sending buffers for each channel, allowing simultaneous bidirectional communications with six neighbors simultaneously.

FIGS. **10** and **11** provide details of the PROM DMA used in the microprocessor **50**. The microprocessor **50** executes faster than all but the fastest PROMs. PROMS are used in a microprocessor **50** system to store program segments and perhaps entire programs. The microprocessor **50** provides a feature on power-up to allow programs to be loaded from low-cost, slow speed PROMs into high speed DRAM for execution. The logic which performs this function is part of the DMA memory controller **118**. The operation is similar to DMA, but not identical, since four 8-bit bytes must be assembled on the microprocessor **50** chip, then written to the DRAM **150**.

The microprocessor **50** directly interfaces to DRAM **150** over a triple multiplexed data and address bus **350**, which carries RAS addresses, CAS addresses and data. The EPROM **260**, on the other hand, is read with non-multiplexed busses. The microprocessor **50** therefore has a special mode which unmultiplexes the data and address lines to read 8 bits of EPROM data. Four 8-bit bytes are read in this fashion. The multiplexed bus **350** is turned back on, and the data is written to the DRAM **150**.

When the microprocessor **50** detects a RESET condition, the processor stops the main CPU **70** and forces a mode **0** (PROM LOAD) instruction into the DMA CPU **72** instruction register. The DMA instruction directs the memory controller to read the EPROM **260** data at 8 times the normal access time for memory. Assuming a 50 MHz microprocessor **50**, this means an access time of 320 nsec. The instruction also indicates:

The selection address of the EPROM **260** to be loaded,

The number of 32-bit words to transfer,

The DRAM **150** address to transfer into.

The sequence of activities to transfer one 32-bit word from EPROM **260** to DRAM **150** are:

1. RAS goes low at **352**, latching the EPROM **260** select information from the high order address bits. The EPROM **260** is selected.
2. Twelve address bits (consisting of what is normally DRAM CAS addresses plus two byte select bits are placed on the bus **350** going to the EPROM **260** address pins. These signals will remain on the lines until the data from the EPROM **260** has been read into the microprocessor **50**. For the first byte, the byte select bits will be binary 00.
3. CAS goes low at **354**, enabling the EPROM **260** data onto the lower 8 bits of the external address/data bus **350**. NOTE: It is important to recognize that, during this part of the cycle, the lower 8 bits of the external data/address bus are functioning as inputs, but the rest of the bus is still acting as outputs.
4. The microprocessor **50** latches these eight least significant bits internally and shifts them 8 bits left to shift them to the next significant byte position.
5. Steps 2, 3 and 4 are repeated with byte address 01.
6. Steps 2, 3 and 4 are repeated with byte address 10.
7. Steps 2, 3 and 4 are repeated with byte address 11.
8. CAS goes high at **356**, taking the EPROM **260** off the data bus.
9. RAS goes high at **358**, indicating the end of the EPROM **260** access.
10. RAS goes low at **360**, latching the DRAM select information from the high order address bits. At the same time, the RAS address bits are latched into the DRAM **150**. The DRAM **150** is selected.
11. CAS goes low at **362**, latching the DRAM **150** CAS addresses.
12. The microprocessor **50** places the previously latched EPROM **260** 32-bit data onto the external address/data bus **350**. W goes low at **364**, writing the 32 bits into the DRAM **150**.
13. W goes high at **366**. CAS goes high at **368**. The process continues with the next word.

FIG. **12** shows details of the microprocessor **50** memory controller **118**. In operation, bus requests stay present until they are serviced. CPU **70** requests are prioritized at **370** in the order of: 1, Parameter Stack; 2, Return Stack; 3, Data Fetch; 4, Instruction Fetch. The resulting CPU request signal and a DMA request signal are supplied as bus requests to bus control **372**, which provides a bus grant signal at **374**. Internal address bus **136** and a DMA counter **376** provide inputs to a multiplexer **378**. Either a row address or a column address are provided as an output to multiplexed address bus **380** as an output from the multiplexer **378**. The multiplexed address bus **380** and the internal data bus **90** provide address and data inputs, respectively, to multiplexer **382**. Shift register **384** supplies row address strobe (RAS) **1** and **2** control signals to multiplexer **386** and column address strobe (CAS) **1** and **2** control signals to multiplexer **388** on lines **390** and **392**. The shift register **384** also supplies output enable (OE) and write (W) signals on lines **394** and **396** and a control signal on line **398** to multiplexer **382**. The shift register **384** receives a RUN signal on line **400** to generate a memory cycle and supplies a MEMORY READY signal on line **402** when an access is complete.

STACK/REGISTER ARCHITECTURE

Most microprocessors use on-chip registers for temporary storage of variables. The on-chip registers access data faster than off-chip RAM. A few microprocessors use an on-chip push down stack for temporary storage.

A stack has the advantage of faster operation compared to on-chip registers by avoiding the necessity to select source and destination registers. (A math or logic operation always uses the top two stack items as source and the top of stack as destination.) The stack's disadvantage is that it makes some operations clumsy. Some compiler activities in particular require on-chip registers for efficiency.

As shown in FIG. **13**, the microprocessor **50** provides both on-chip registers **134** and a stack **74** and reaps the benefits of both.

BENEFITS:

1. Stack math and logic is twice as fast as those available on an equivalent register only machine. Most programmers and optimizing compilers can take advantage of this feature.
2. Sixteen registers are available for on-chip storage of local variables which can transfer to the stack for computation. The accessing of variables is three to four times as fast as available on a strictly stack machine.

The combined stack **74**/register **134** architecture has not been used previously due to inadequate understanding by computer designers of optimizing compilers and the mix of transfer versus math/logic instructions.

ADAPTIVE MEMORY CONTROLLER

A microprocessor must be designed to work with small or large memory configurations. As more memory loads are added to the data, address, and control lines, the switching speed of the signals slows down. The microprocessor **50** multiplexes the address/data bus three ways, so timing between the phases is critical. A traditional approach to the problem allocates a wide margin of time between bus phases so that systems will work with small or large numbers of memory chips connected. A speed compromise of as much as 50% is required.

As shown in FIG. **14**, the microprocessor **50** uses a feedback technique to allow the processor to adjust memory bus timing to be fast with small loads and slower with large ones. The OUTPUT ENABLE (OE) line **152** from the microprocessor **50** is connected to all memories **150** on the circuit board. The loading on the output enable line **152** to the microprocessor **50** is directly related to the number of memories **150** connected. By monitoring how rapidly OE **152** goes high after a read, the microprocessor **50** is able to determine when the data hold time has been satisfied and place the next address on the bus.

The level of the OE line **152** is monitored by CMOS input buffer **410** which generates an internal READY signal on line **412** to the microprocessor's memory controller. Curves **414** and **416** of the FIG. **15** graph show the difference in rise time likely to be encountered from a lightly to heavily loaded memory system. When the OE line **152** has reached a predetermined level to generate the READY signal, driver **418** generates an OUTPUT ENABLE signal on OE line **152**.

SKIP WITHIN THE INSTRUCTION CACHE

The microprocessor **50** fetches four 8-bit instructions each memory cycle and stores them in a 32-bit instruction register **108**, as shown in FIG. **16**. A class of "test and skip" instructions can very rapidly execute a very fast jump operation within the four instruction cache.

SKIP CONDITIONS:

Always

ACC non-zero

ACC negative

Carry flag equal logic one

Never

ACC equal zero

ACC positive

Carry flag equal logic zero

The SKIP instruction can be located in any of the four byte positions **420** in the 32-bit instruction register **108**. If the test is successful, SKIP will jump over the remaining one, two, or three 8-bit instructions in the instruction register **108** and cause the next four-instruction group to be loaded into the register **108**. As shown, the SKIP operation is implemented by resetting the 2-bit microinstruction counter **180** to zero on line **422** and simultaneously latching the next instruction group into the register **108**. Any instructions following the SKIP in the instruction register are overwritten by the new instructions and not executed.

The advantage of SKIP is that optimizing compilers and smart programmers can often use it in place of the longer conditional JUMP instruction. SKIP also makes possible microloops which exit when the loop counts down or when the SKIP jumps to the next instruction group. The result in very fast code.

Other machines (such as the PDP-8 and Data General NOVA) provide the ability to skip a single instruction. The microprocessor **50** provides the ability to skip up to three instructions.

MICROLOOP IN THE INSTRUCTION CACHE

The microprocessor **50** provides the MICROLOOP instruction to execute repetitively from one to three instructions residing in the instruction register **108**. The microloop instruction works in conjunction with the LOOP COUNTER **92** (FIG. **2**) connected to the internal data bus **90**. To execute a microloop, the program stores a count in LOOP COUNTER **92**. MICROLOOP may be placed in the first, second, third, or last byte **420** of the instruction register **108**. If placed in the first position, execution will just create a delay equal to the number stored in LOOP COUNTER **92** times the machine cycle. If placed in the second, third, or last byte **420**, when the microloop instruction is executed, it will test the LOOP COUNT for zero. If zero, execution will continue with the next instruction. If not zero, the LOOP COUNTER **92** is decremented and the 2-bit microinstruction counter is cleared, causing the preceding instructions in the instruction register to be executed again.

Microloop is useful for block move and search operations. By executing a block move completely out of the instruction register **108**, the speed of the move is doubled, since all memory cycles are used by the move rather than being shared with instruction fetching. Such a hardware implementation of microloops is much faster than conventional software implementation of a comparable function.

OPTIMAL CPU CLOCK SCHEME

The designer of a high speed microprocessor must produce a product which operate over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing. Temperature, voltage, and process all affect transistor propagation delays. Traditional CPU designs are done so that with the worse case of the three parameters, the circuit will function at the rated clock speed. The result are designs that must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse case conditions.

The microprocessor **50** uses the technique shown in FIGS. **17–19** to generate the system clock and its required phases. Clock circuit **430** is the familiar "ring oscillator" used to test process performance. The clock is fabricated on the same silicon chip as the rest of the microprocessor **50**.

The ring oscillator frequency is determined by the parameters of temperature, voltage, and process. At room temperature, the frequency will be in the neighborhood of 100 MHZ. At 70 degrees Centigrade, the speed will be 50 MHZ. The ring oscillator **430** is useful as a system clock, with its stages **431** producing phase 0-phase 3 outputs **433** shown in FIG. **19**, because its performance tracks the parameters which similarly affect all other transistors on the same silicon die. By deriving system timing from the ring

oscillator **430**, CPU **70** will always execute at the maximum frequency possible, but never too fast. For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor **50** will operate slower than normal. Since the microprocessor **50** ring oscillator clock **430** is made from the same transistors on the same die as the latches and gates, it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.

ASYNCHRONOUS/SYNCHRONOUS CPU

Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor **50** provides a dual-clock scheme as shown in FIG. **17**, with the CPU **70** operating a synchronously to I/O interface **432** forming part of memory controller **118** (FIG. **2**) and the I/O interface **432** operating synchronously with the external world of memory and I/O devices. The CPU **70** executes at the fastest speed possible using the adaptive ring counter clock **430**. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor **50** for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface **432**, speed of which is controlled by a conventional crystal clock **434**. The interface **432** processes requests for memory accesses from the microprocessor **50** and acknowledges the presence of I/O data. The microprocessor **50** fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. By decoupling the variable speed of the CPU **70** from the fixed speed of the I/O interface **432**, optimum performance can be achieved by each. Recoupling between the CPU **70** and the interface **432** is accomplished with handshake signals on lines **436**, with data/addresses passing on bus **90**, **136**.

ASYNCHRONOUS/SYNCHRONOUS CPU IMBEDDED ON A DRAM CHIP

System performance is enhanced even more when the DRAM **311** and CPU **314** (FIG. **9**) are located on the same die. The proximity of the transistors means that DRAM **311** and CPU **314** parameters will closely follow each other. At room temperature, not only would the CPU **314** execute at 100 MHZ, but the DRAM **311** would access fast enough to keep up. The synchronization performed by the I/O interface **432** would be for DMA and reading and writing I/O ports. In some systems (such as calculators) no I/O synchronization at all would be required, and the I/O clock would be tied to the ring counter clock.

VARIABLE WIDTH OPERANDS

Many microprocessors provide variable width operands. The microprocessor **50** handles operands of 8, 16, or 24 bits using the same op-code. FIG. **20** shows the 32-bit instruction register **108** and the 2-bit microinstruction register **180** which selects the 8-bit instruction. Two classes of microprocessor **50** instructions can be greater than 8-bits, JUMP class and IMMEDIATE. A JUMP or IMMEDIATE op-code is 8-bits, but the operand can be 8, 16, or 24 bits long. This magic is possible because operands must be right justified in the instruction register. This means that the least significant bit of the operand is always located in the least significant bit of the instruction register. The microinstruction counter **180** selects which 8-bit instruction to execute. If a JUMP or IMMEDIATE instruction is decoded, the state of the 2-bit microinstruction counter selects the required 8, 16, or 24 bit operand onto the address or data bus. The unselected 8-bit bytes are loaded with zeros by operation of decoder **440** and gates **442**. The advantage of this technique is the saving of a number of op-codes required to specify the different operand sizes in other microprocessors.

TRIPLE STACK CACHE

Computer performance is directly related to the system memory bandwidth. The faster the memories, the faster the computer. Fast memories are expensive, so techniques have been developed to move a small amount of high-speed memory around to the memory addresses where it is needed. A large amount of slow memory is constantly updated by the fast memory, giving the appearance of a large fast memory array. A common implementation of the technique is known as a high-speed memory cache. The cache may be thought of as fast acting shock absorber smoothing out the bumps in memory access. When more memory is required than the shock can absorb, it bottoms out and slow speed memory is accessed. Most memory operations can be handled by the shock absorber itself.

The microprocessor **50** architecture has the ALU **80** (FIG. **2**) directly coupled to the top two stack locations **76** and **78**. The access time of the stack **74** therefore directly affects the execution speed of the processor. The microprocessor **50** stack architecture is particularly suitable to a triple cache technique, shown in FIG. **21** which offers the appearance of a large stack memory operating at the speed of on-chip latches **450**. Latches **450** are the fastest form of memory device built on the chip, delivering data in as little as 3 nsec. However latches **450** require large numbers of transistors to construct. On-chip RAM **452** requires fewer transistors than latches, but is slower by a factor of five (15 nsec access). Off-chip RAM **150** is the slowest storage of all. The microprocessor **50** organizes the stack memory hierarchy as three interconnected stacks **450**, **452** and **454**. The latch stack **450** is the fastest and most frequently used. The on-chip RAM stack **452** is next. The off-chip RAM stack **454** is slowest. The stack modulation determines the effective access time of the stack. If a group of stack operations never push or pull more than four consecutive items on the stack, operations will be entirely performed in the 3 nsec latch stack. When the four latches **456** are filled, the data in the bottom of the latch stack **450** is written to the top of the on-chip RAM stack **452**. When the sixteen locations **458** in the on-chip RAM stack **452** are filled, the data in the bottom of the on-chip RAM stack **452** is written to the top of the off-chip RAM stack **454**. When popping data off a full stack **450**, four pops will be performed before stack empty line **460** from the latch stack pointer **462** transfers data from the on-chip RAM stack **452**. By waiting for the latch stack **450** to empty before performing the slower on-chip RAM access, the high effective speed of the latches **456** are made available to the processor. The same approach is employed with the on-chip RAM stack **452** and the off-chip RAM stack **454**.

POLYNOMIAL GENERATION INSTRUCTION

Polynomials are useful for error correction, encryption, data compression, and fractal generation. A polynomial is generated by a sequence of shift and exclusive OR operations. Special chips are provided for this purpose in the prior art.

The microprocessor **50** is able to generate polynomials at high speed without external hardware by slightly modifying how the ALU **80** works. As shown in FIG. **21**, a polynomial is generated by loading the "order" (also known as the feedback terms) into C Register **470**. The value thirty one (resulting in 32 iterations) is loaded into DOWN COUNTER **472**. A register **474** is loaded with zero. B register **476** is loaded with the starting polynomial value. When the POLY

instruction executes, C register **470** is exclusively ORed with A register **474** if the least significant bit of B register **476** is a one. Otherwise, the contents of the A register **474** passes through the ALU **80** unaltered. The combination of A and B is then shifted right (divided by 2) with shifters **478** and **480**. The operation automatically repeats the specified number of iterations, and the resulting polynomial is left in A register **474**.

FAST MULTIPLY

Most microprocessors offer a 16×16 or 32×32 bit multiply instruction. Multiply when performed sequentially takes one shift/add per bit, or 32 cycles for 32 bit data. The microprocessor **50** provides a high speed multiply which allows multiplication by small numbers using only a small number of cycles. FIG. **23** shows the logic used to implement the high speed algorithm. To perform a multiply, the size of the multiplier less one is placed in the DOWN COUNTER **472**. For a four bit multiplier, the number three would be stored in the DOWN COUNTER **472**. Zero is loaded into the A register **474**. The multiplier is written bit reversed into the B Register **476**. For example, a bit reversed five (binary 0101) would be written into B as 1010. The multiplicand is written into the C register **470**. Executing the FAST MULT instruction will leave the result in the A Register **474**, when the count has been completed. The fast multiply instruction is important because many applications scale one number by a much smaller number. The difference in speed between multiplying a 32×32 bit and a 32×4 bit is a factor of 8. If the least significant bit of the multiplier is a "ONE", the contents of the A register **474** and the C register **470** are added. If the least significant bit of the multiplier is a "ZERO", the contents of the A register are passed through the ALU **80** unaltered. The output of the ALU **80** is shifted left by shifter **482** in each iteration. The contents of the B register **476** are shifted right by the shifter **480** in each iteration.

INSTRUCTION EXECUTION PHILOSOPHY

The microprocessor **50** uses high speed D latches in most of the speed critical areas. Slower on-chip RAM is used as secondary storage.

The microprocessor **50** philosophy of instruction execution is to create a hierarchy of speed as follows:

Logic and D latch transfers	1 cycle	20 nsec
Math	2 cycles	40 nsec
Fetch/store on-chip RAM	2 cycles	40 nsec
Fetch/store in current RAS page	4 cycles	80 nsec
Fetch/store with RAS cycle	11 cycles	220 nsec

With a 50 MHZ clock, many operations can be performed in 20 nsec. and almost everything else in 40 nsec.

To maximize speed, certain techniques in processor design have been used. They include:

Eliminating arithmetic operations on addresses,

Fetching up to four instructions per memory cycle,

Pipelineless instruction decoding

Generating results before they are needed,

Use of three level stack caching.

PIPELINE PHILOSOPHY

Computer instructions are usually broken down into sequential pieces, for example: fetch, decode, register read, execute, and store. Each piece will require a single machine cycle. In most Reduced Instruction Set Computer (RISC) chips, instruction require from three to six cycles.

RISC instructions are very parallel. For example, each of 70 different instructions in the SPARC (SUN Computer's RISC chip) has five cycles. Using a technique called "pipelining", the different phases of consecutive instructions can be overlapped.

To understand pipelining, think of building five residential homes. Each home will require in sequence, a foundation, framing, plumbing and wiring, roofing, and interior finish. Assume that each activity takes one week. To build one house will take five weeks.

But what if you want to build an entire subdivision? You have only one of each work crew, but when the foundation men finish on the first house, you immediately start them on the second one, and so on. At the end of five weeks, the first home is complete, but you also have five foundations. If you have kept the framing, plumbing, roofing, and interior guys all busy, from five weeks on, a new house will be completed each week.

This is the way a RISC chip like SPARC appears to execute an instruction in a single machine cycle. In reality, a RISC chip is executing one fifth of five instructions each machine cycle. And if five instructions stay in sequence, an instruction will be completed each machine cycle.

The problems with a pipeline are keeping the pipe full with instructions. Each time an out of sequence instruction such as a BRANCH or CALL occurs, the pipe must be refilled with the next sequence. The resulting dead time to refill the pipeline can become substantial when many IF/THEN/ELSE statements or subroutines are encountered.

THE PIPELINE APPROACH

The microprocessor **50** has no pipeline as such. The approach of this microprocessor to speed is to overlap instruction fetching with execution of the previously fetched instruction(s). Beyond that, over half the instructions (the most common ones) execute entirely in a single machine cycle of 20 nsec. This is possible because:

1. Instruction decoding resolves in 2.5 nsec.
2. Incremented/decremented and some math values are calculated before they are needed, requiring only a latching signal to execute.
3. Slower memory is hidden from high speed operations by high-speed D latches which access in 4 nsec.

The disadvantage for this microprocessor is a more complex chip design process. The advantage for the chip user is faster ultimate throughput since pipeline stalls cannot exist. Pipeline synchronization with availability flag bits and other such pipeline handling is not required by this microprocessor.

For example, in some RISC machines an instruction which tests a status flag may have to wait for up to four cycles for the flag set by the previous instruction to be available to be tested. Hardware and software debugging is also somewhat easier because the user doesn't have to visualize five instructions simultaneously in the pipe.

OVERLAPPING INSTRUCTION FETCH/EXECUTE

The slowest procedure the microprocessor **50** performs is to access memory. Memory is accessed when data is read or written. Memory is also read when instructions are fetched. The microprocessor **50** is able to hide fetch of the next instruction behind the execution of the previously fetched instruction(s). The microprocessor **50** fetches instructions in 4-byte instruction groups. An instruction group may contain from one to four instructions. The amount of time required to execute the instruction group ranges from 4 cycles for simple instructions to 64 cycles for a multiply.

When a new instruction group is fetched, the microprocessor instruction decoder looks at the most significant bit of all four of the bytes. The most significant bit of an instruction determines if a memory access is required. For example, CALL, FETCH, and STORE all require a memory access to

execute. If all four bytes have nonzero most significant bits, the microprocessor initiates the memory fetch of the next sequential 4-byte instruction group. When the last instruction in the group finishes executing, the next 4-byte instruction group is ready and waiting on the data bus needing only to be latched into the instruction register. If the 4-byte instruction group required four or more cycles to execute and the next sequential access was a column address strobe (CAS) cycle, the instruction fetch was completely overlapped with execution.

INTERNAL ARCHITECTURE

The microprocessor **50** architecture consists of the following:

PARAMETER STACK	<---> ALU* <--->	Y REGISTER RETURN STACK
<---32 BITS---> 16 DEEP		<---32 BITS---> 16 DEEP
Used for math and logic.		Used for subroutine and interrupt return addresses as well as local variables.
Push down stack. Can overflow into off-chip RAM.		Push down stack. Can overflow into off-chip RAM. Can also be accessed relative to top of stack.
LOOP COUNTER	(32-bits, can decrement by 1) Used by class of test and loop instructions.	
X REGISTER	(32-bits, can increment or decrement by 4). Used to point to RAM locations.	
PROGRAM COUNTER	(32-bits, increments by 4). Points to 4-byte instruction groups in RAM.	
INSTRUCTION REG	(32-Bits). Holds 4-byte instruction groups while they are being decoded and executed.	

MODE - A register with mode and status bits.

MODE-BITS:

- Slow down memory accesses by 8 if "1". Run full speed if "0". (Provided for access to slow EPROM.)
- Divide the system clock by 1023 if "1" to reduce power consumption. Run full speed if "0". (On-chip counters slow down if this bit is set.)
- Enable external interrupt 1.
- Enable external interrupt 2.
- Enable external interrupt 3.
- Enable external interrupt 4.
- Enable external interrupt 5.
- Enable external interrupt 6.
- Enable external interrupt 7.

ON-CHIP MEMORY LOCATIONS:

MODE-BITS	
DMA-POINTER	
DMA-COUNTER	
STACK-POINTER	- Pointer into Parameter Stack.
STACK-DEPTH	- Depth of on-chip Parameter Stack
RSTACK-POINTER	- Pointer into Return Stack
RSTACK-DEPTH	- Depth of on-chip Return Stack

*Math and logic operations use the TOP item and NEXT to top Parameter Stack items as the operands. The result is pushed onto the Parameter Stack. *Return addresses from subroutines are placed on the Return Stack. The Y REGISTER is used as a pointer to RAM locations. Since the Y REGISTER is the top item of the Return Stack, nesting of indices is straightforward.

ADDRESSING MODE HIGH POINTS

The data bus is 32-bits wide. All memory fetches and stores are 32-bits. Memory bus addresses are 30 bits. The least significant 2 bits are used to select one-of-four bytes in some addressing modes. The Program Counter, X Register, and Y Register are implemented as D latches with their outputs going to the memory address bus and the bus incrementer/decrementer. Incrementing one of these registers can happen quickly, because the incremented value has already rippled through the inc/dec logic and need only be clocked into the latch. Branches and Calls are made to 32-bit word boundaries.

INSTRUCTION SET

32-BIT INSTRUCTION FORMAT

The thirty two bit instructions are CALL, BRANCH, BRANCH-IF-ZERO, and LOOP-IF-NOT-DONE. These instructions require the calculation of an effective address. In many computers, the effective address is calculated by adding or subtracting an operand with the current Program Counter. This math operation requires from four to seven machine cycles to perform and can definitely bog down machine execution. The microprocessor's strategy is to perform the required math operation at assembly or linking time and do a much simpler "Increment to next page" or "Decrement to previous page" operation at run time. As a result, the microprocessor branches execute in a single cycle.

24-BIT OPERAND FORM:

Byte 1	Byte 2	Byte 3	Byte 4
WWWWWW XX -	YYYYYYYY -	YYYYYYYY -	YYYYYYYY

With a 24-bit operand, the current page is considered to be defined by the most significant 6 bits of the Program Counter.

16-BIT OPERAND FORM: QQQQQQQQ-WWWWWW XX-YYYYYYYY-YYYYYYYY With a 16-bit operand, the current page is considered to be defined by the most significant 14 bits of the Program Counter.

8-BIT OPERAND FORM: QQQQQQQQ-QQQQQQQQ-WWWWWW XX-YYYYYYYY With an 8-bit operand, the current page is considered to be defined by the most significant 22 bits of the Program Counter.

QQQQQQQQ—Any 8-bit instruction.

WWWWWW—Instruction op-code.

XX—Select how the address bits will be used:

00—Make all high-order bits zero. (Page zero addressing)

01—Increment the high-order bits. (Use next page)

10—Decrement the high-order bits. (Use previous page)

11—Leave the high-order bits unchanged. (Use current page)

YYYYYYYY—The address operand field. This field is always shifted left two bits (to generate a word rather than byte address) and loaded into the Program Counter. The microprocessor instruction decoder figures out the width of the operand field by the location of the instruction op-code in the four bytes.

The compiler or assembler will normally use the shortest operand required to reach the desired address so that the leading bytes can be used to hold other instructions. The effective address is calculated by combining:

The current Program Counter,

The 8, 16, or 24 bit address operand in the instruction, Using one of the four allowed addressing modes.

EXAMPLES OF EFFECTIVE ADDRESS CALCULATION

Example 1

Byte 1	Byte 2	Byte 3	Byte 4
QQQQQQQQ	QQQQQQQQ	00000011	10011000

The "QQQQQQQQs" in Byte 1 and 2 indicate space in the 4-byte memory fetch which could be hold two other

instructions to be executed prior to the CALL instruction. Byte 3 indicates a CALL instruction (six zeros) in the current page (indicated by the 11 bits). Byte 4 indicates that the hexadecimal number **98** will be forced into the Program Counter bits **2** through **10**. (Remember, a CALL or BRANCH always goes to a word boundary so the two least significant bits are always set to zero). The effect of this instruction would be to CALL a subroutine at WORD location HEX 98 in the current page. The most significant 22 bits of the Program Counter define the current page and will be unchanged.

Example 2

Byte 1	Byte 2	Byte 3	Byte 4
000001 01	00000001	00000000	00000000

If we assume that the Program Counter was HEX 0000 0156 which is binary:

00000000 00000000 00000001 01010110=OLD PROGRAM COUNTER.

Byte 1 indicates a BRANCH instruction op code (000001) and "01" indicates select the next page. Byte 2,3, and 4 are the address operand. These 24-bits will be shifted to the left two places to define a WORD address. HEX 0156 shifted left two places is HEX 0558. Since this is a 24-bit operand instruction, the most significant 6 bits of the Program Counter define the current page. These six bits will be incremented to select the next page. Executing this instruction will cause the Program Counter to be loaded with HEX 0400 0558 which is binary:

00000100 00000000 00000101 01011000=NEW PROGRAM COUNTER.

INSTRUCTIONS

CALL-LONG

0000 00XX-YYYYYYYY-YYYYYYYY-YYYYYYYY

Load the Program Counter with the effective WORD address specified. Push the current PC contents onto the RETURN STACK.

OTHER EFFECTS: CARRY or modes, no effect. May cause Return Stack to force an external memory cycle if on-chip Return Stack is full.

BRANCH

0000 01XX-YYYYYYYY-YYYYYYYY-YYYYYYYY

Load the Program Counter with the effective WORD address specified.

OTHER EFFECTS: NONE

BRANCH-IF-ZERO

0000 10XX-YYYYYYYY-YYYYYYYY-YYYYYYYY

Test the TOP value on the Parameter Stack. If the value is equal to zero, load the Program Counter with the effective WORD address specified. If the TOP value is not equal to zero, increment the Program Counter and fetch and execute the next instruction.

OTHER EFFECTS: NONE

LOOP-IF-NOT-DONE

0000 11YY-(XXXX XXXX)-(XXXX XXXX)-(XXXX XXXX)

If the LOOP COUNTER is not zero, load the Program Counter with the effective WORD address specified. If the LOOP COUNTER is zero, decrement the LOOP COUNTER, increment the Program Counter and fetch and execute the next instruction.

OTHER EFFECTS: NONE

8-BIT INSTRUCTIONS PHILOSOPHY

Most of the work in the microprocessor **50** is done by the 8-bit instructions. Eight bit instructions are possible with the microprocessor because of the extensive use of implied stack addressing. Many 32-bit architectures use 8-bits to specify the operation to perform but use an additional 24-bits to specify two sources and a destination.

For math and logic operations, the microprocessor **50** exploits the inherent advantage of a stack by designating the source operand(s) as the top stack item and the next stack item. The math or logic operation is performed, the operands are popped from the stack, and the result is pushed back on the stack. The result is a very efficient utilization of instruction bits as well as registers. A comparable situation exists between Hewlett Packard calculators (which use a stack) and Texas Instrument calculators which don't. The identical operation on an HP will require one half to one third the keystrokes of the TI.

The availability of 8-bit instructions also allows another architectural innovation, the fetching of four instructions in a single 32-bit memory cycle. The advantages of fetching multiple instructions are:

Increased execution speed even with slow memories,

Similar performance to the Harvard (separate data and instruction busses) without the expense,

Opportunities to optimize groups of instructions,

The capability to perform loops within this mini-cache.

The microloops inside the four instruction group are effective for searches and block moves.

SKIP INSTRUCTIONS

The microprocessor **50** fetches instructions in 32-bit chunks called 4-byte instruction groups. These four bytes may contain four 8-bit instructions or some mix of 8-bit and 16 or 24-bit instructions. SKIP instructions in the microprocessor skip any remaining instructions in a 4-byte instruction group and cause a memory fetch to get the next 4-byte instruction group. Conditional SKIPs when combined with 3-byte BRANCHES will create conditional BRANCHES. SKIPs may also be used in situations when no use can be made of the remaining bytes in a 4-instruction group. A SKIP executes in a single cycle, whereas a group of three NOPs would take three cycles.

SKIP-ALWAYS—Skip any remaining instructions in this 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group.

SKIP-IF-ZERO—If the TOP item of the Parameter Stack is zero, skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is not zero, execute the next sequential instruction.

SKIP-IF-POSITIVE—If the TOP item of the Parameter Stack has a the most significant bit (the sign bit) equal to "0", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is not "0", execute the next sequential instruction.

SKIP-IF-NO-CARRY—If the CARRY flag from a SHIFT or arithmetic operation is not equal to "1", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the CARRY is equal to "1", execute the next sequential instruction.

SKIP-NEVER (NOP) execute the next sequential instruction. (Delay one machine cycle).

SKIP-IF-NOT-ZERO—If the TOP item on the Parameter Stack is not equal to "0", skip any remaining instructions

in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item is equal "0", execute the next sequential instruction.

SKIP-IF-NEGATIVE—If the TOP item on the Parameter Stack has its most significant bit (sign bit) set to "1", skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the TOP item has its most significant bit set to "0", execute the next sequential instruction.

SKIP-IF-CARRY—If the CARRY flag is set to "1" as a result of SHIFT or arithmetic operation, skip any remaining instructions in the 4-byte instruction group. Increment the most significant 30-bits of the Program Counter and proceed to fetch the next 4-byte instruction group. If the CARRY flag is "0", execute the next sequential instruction.

MICROLOOPS

Microloops are a unique feature of the microprocessor architecture which allows controlled looping within a 4-byte instruction group. A microloop instruction tests the LOOP COUNTER for "0" and may perform an additional test. If the LOOP COUNTER is not "0" and the test is met, instruction execution continues with the first instruction in the 4-byte instruction group, and the LOOP COUNTER is decremented. A microloop instruction will usually be the last byte in a 4-byte instruction group, but it can be any byte. If the LOOP COUNTER is "0" or the test is not met, instruction execution continues with the next instruction. If the microloop is the last byte in the 4-byte instruction group, the most significant 30-bits of the Program Counter are incremented and the next 4-byte instruction group is fetched from memory. On a termination of the loop on LOOP COUNTER equal to "0", the LOOP COUNTER will remain at "0". Microloops allow short iterative work such as moves and searches to be performed without slowing down to fetch instructions from memory.

EXAMPLE

Byte 1	Byte 2
FETCH-VIA-X-AUTO-INCREMENT	STORE-VIA-Y-AUTOINCREMENT
Byte 3	Byte 4
ULOOP-UNTIL-DONE	QQQQQQQQ

This example will perform a block move. To initiate the transfer, X will be loaded with the starting address of the source. Y will be loaded with the starting address of the destination. The LOOP COUNTER will be loaded with the number of 32-bit words to move. The microloop will FETCH and STORE and count down the LOOP COUNTER until it reaches zero. QQQQQQQQ indicates any instruction can follow.

MICROLOOP INSTRUCTIONS

ULOOP-UNTIL-DONE—If the LOOP COUNTER is not "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0", continue execution with the next instruction.

ULOOP-IF-ZERO—If the LOOP COUNTER is not "0" and the TOP item on the Parameter Stack is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

ULOOP-IF-POSITIVE—If the LOOP COUNTER is not "0" and the most significant bit (sign bit) is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

ULOOP-IF-NOT-CARRY-CLEAR—If the LOOP COUNTER is not "0" and the floating point exponents found in TOP and NEXT are not aligned, continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the exponents are aligned, continue execution with the next instruction. This instruction is specifically designed for combination with special SHIFT instructions to align two floating point numbers.

ULOOP-NEVER—(DECREMENT-LOOP-COUNTER) Decrement the LOOP COUNTER. Continue execution with the next instruction.

ULOOP-IF-NOT-ZERO—If the LOOP COUNTER is not "0" and the TOP item of the Parameter Stack is "0", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the TOP item is "1", continue execution with the next instruction.

ULOOP-IF-NEGATIVE—If the LOOP COUNTER is not "0" and the most significant bit (sign bit) of the TOP item of the Parameter Stack is "1", continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the most significant bit of the Parameter Stack is "0", continue execution with the next instruction.

ULOOP-IF-CARRY-SET—If the LOOP COUNTER is not "0" and the exponents of the floating point numbers found in TOP and NEXT are not aligned, continue execution with the first instruction in the 4-byte instruction group. Decrement the LOOP COUNTER. If the LOOP COUNTER is "0" or the exponents are aligned, continue execution with the next instruction.

RETURN FROM SUBROUTINE OR INTERRUPT

Subroutine calls and interrupt acknowledgements cause a redirection of normal program execution. In both cases, the current Program Counter is pushed onto the Return Stack, so the microprocessor can return to its place in the program after executing the subroutine or interrupt service routine.

NOTE: When a CALL to subroutine or interrupt is acknowledged the Program Counter has already been incremented and is pointing to the 4-byte instruction group following the 4-byte group currently being executed. The instruction decoding logic allows the microprocessor to perform a test and execute a return conditional on the outcome of the test in a single cycle. A RETURN pops an address from the Return Stack and stores it to the Program Counter.

RETURN INSTRUCTIONS

RETURN-ALWAYS—Pop the top item from the Return Stack and transfer it to the Program Counter.

RETURN-IF-ZERO—If the TOP item on the Parameter Stack is "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-POSITIVE—If the most significant bit (sign bit) of the TOP item on the Parameter Stack is a "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-CARRY-CLEAR—If the exponents of the floating point numbers found in TOP and NEXT are not aligned, pop the top item from the Return Stack and

transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-NEVER (NOP)—Execute the next instruction.

RETURN-IF-NOT-ZERO—If the TOP item on the Parameter Stack is not "0", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-NEGATIVE—If the most significant bit (sign bit) of the TOP item on the Parameter Stack is a "1", pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

RETURN-IF-CARRY-SET—If the exponents of the floating point numbers found in TOP and NEXT are aligned, pop the top item from the Return Stack and transfer it to the Program Counter. Otherwise execute the next instruction.

HANDLING MEMORY FROM DYNAMIC RAM

The microprocessor **50**, like any RISC type architecture, is optimized to handle as many operations as possible on-chip for maximum speed. External memory operations take from 80 nsec. to 220 nsec. compared with on-chip memory speeds of from 4 nsec. to 30 nsec. There are times when external memory must be accessed.

External memory is accessed using three registers:

X-REGISTER—A 30-bit memory pointer which can be used for memory access and simultaneously incremented or decremented.

Y-REGISTER—A 30-bit memory pointer which can be used for memory access and simultaneously incremented or decremented.

PROGRAM-COUNTER—A 30-bit memory pointer normally used to point to 4-byte instruction groups. External memory may be accessed at addresses relative to the PC. The operands are sometimes called "Immediate" or "Literal" in other computers. When used as memory pointer, the PC is also incremented after each operation.

MEMORY LOAD & STORE INSTRUCTIONS

FETCH-VIA-X—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. X is unchanged.

FETCH-VIA-Y—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. Y is unchanged.

FETCH-VIA-X-AUTOINCREMENT—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of X to point to the next 32-bit word address.

FETCH-VIA-Y-AUTOINCREMENT—Fetch the 32-bit memory content pointed to by Y and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of Y to point to the next 32-bit word address.

FETCH-VIA-X-AUTODECREMENT—Fetch the 32-bit memory content pointed to by X and push it onto the Parameter Stack. After fetching, decrement the most significant 30 bits of X to point to the previous 32-bit word address.

FETCH-VIA-Y-AUTODECREMENT—Fetch the 32-bit memory content pointed to by Y and push it onto the Parameter Stack. After fetching, decrement the most significant 30 bits of Y to point to the previous 32-bit word address.

STORE-VIA-X—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. X is unchanged.

STORE-VIA-Y—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. Y is unchanged.

STORE-VIA-X-AUTOINCREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. After storing, increment the most significant 30 bits of X to point to the next 32-bit word address.

STORE-VIA-Y-AUTOINCREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. After storing, increment the most significant 30 bits of Y to point to the next 32-bit word address.

STORE-VIA-X-AUTODECREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by X. After storing, decrement the most significant 30 bits of X to point to the previous 32-bit word address.

STORE-VIA-Y-AUTODECREMENT—Pop the top item of the Parameter Stack and store it in the memory location pointed to by Y. After storing, decrement the most significant 30 bits of Y to point to the previous 32-bit word address.

FETCH-VIA-PC—Fetch the 32-bit memory content pointed to by the Program Counter and push it onto the Parameter Stack. After fetching, increment the most significant 30 bits of the Program Counter to point to the next 32-bit word address.

*NOTE When this instruction executes, the PC is pointing to the memory location following the instruction. The effect is of loading a 32-bit immediate operand. This is an 8-bit instruction and therefore will be combined with other 8-bit instructions in a 4-byte instruction fetch. It is possible to have from one to four FETCH-VIA-PC instructions in a 4-byte instruction fetch. The PC increments after each execution of FETCH-VIA-PC, so it is possible to push four immediate operands on the stack. The four operands would be the found in the four memory locations following the instruction.

BYTE-FETCH-VIA-X—Fetch the 32-bit memory content pointed to by the most significant 30 bits of X. Using the two least significant bits of X, select one of four bytes from the 32-bit memory fetch, right justify the byte in a 32-bit field and push the selected byte preceded by leading zeros onto the Parameter Stack.

BYTE-STORE-VIA-X—Fetch the 32-bit memory content pointed to by the most significant 30 bits of X. Pop the TOP item from the Parameter Stack. Using the two least significant bits of X place the least significant byte into the 32-bit memory data and write the 32-bit entity back to the location pointed to by the most significant 30 bits of X.

OTHER EFFECTS OF MEMORY ACCESS INSTRUCTIONS:

Any FETCH instruction will push a value on the Parameter Stack **74**. If the on-chip stack is full, the stack will overflow into off-chip memory stack resulting in an additional memory cycle. Any STORE instruction will pop a value from the Parameter Stack **74**. If the on-chip stack is empty, a memory cycle will be generated to fetch a value from off-chip memory stack.

HANDLING ON-CHIP VARIABLES

High-level languages often allow the creation of LOCAL VARIABLES. These variables are used by a particular procedure and discarded. In cases of nested procedures, layers of these variables must be maintained. On-chip storage is up to five times faster than off-chip RAM, so a means of keeping local variables on-chip can make operations run faster. The microprocessor **50** provides the capability for both on-chip storage of local variables and nesting of multiple levels of variables through the Return Stack.

The Return Stack **134** is implemented as 16 on-chip RAM locations. The most common use for the Return Stack **134** is storage of return addresses from subroutines and interrupt calls. The microprocessor allows these 16 locations to also be used as addressable registers. The 16 locations may be read and written by two instructions which indicate a Return Stack relative address from 0–15. When high-level procedures are nested, the current procedure variables push the previous procedure variables further down the Return Stack **134**. Eventually, the Return Stack will automatically overflow into off-chip RAM.

ON-CHIP VARIABLE INSTRUCTIONS

READ-LOCAL-VARIABLE XXXX—Read the XXXXth location relative to the top of the Return Stack. (XXXX is a binary number from 0000–1111). Push the item read onto the Parameter Stack.

OTHER EFFECTS: If the Parameter Stack is full, the push operation will cause a memory cycle to be generated as one item of the stack is automatically stored to external RAM. The logic which selects the location performs a modulo **16** subtraction. If four local variables have been pushed onto the Return Stack, and an instruction attempts to READ the fifth item, unknown data will be returned.

WRITE-LOCAL-VARIABLE XXXX—Pop the TOP item of the Parameter Stack and write it into the XXXXth location relative to the top of the Return Stack. (XXXX is a binary number from 0000–1111.)

OTHER EFFECTS: If the Parameter Stack is empty, the pop operation will cause a memory cycle to be generated to fetch the Parameter Stack item from external RAM. The logic which selects the location performs a modulo **16** subtraction. If four local variables have been pushed onto the Return Stack, and an instruction attempts to WRITE to the fifth item, it is possible to clobber return addresses or wreak other havoc.

REGISTER AND FLIP-FLOP TRANSFER AND PUSH INSTRUCTIONS

DROP—Pop the TOP item from the Parameter Stack and discard it.

SWAP—Exchange the data in the TOP Parameter Stack location with the data in the NEXT Parameter Stack location.

DUP—Duplicate the TOP item on the Parameter Stack and push it onto the Parameter Stack.

PUSH-LOOP-COUNTER—Push the value in LOOP COUNTER onto the Parameter Stack.

POP-RSTACK-PUSH-TO-STACK—Pop the top item from the Return Stack and push it onto the Parameter Stack.

PUSH-X-REG—Push the value in the X Register onto the Parameter Stack.

PUSH-STACK-POINTER—Push the value of the Parameter Stack pointer onto the Parameter Stack.

PUSH-RSTACK-POINTER—Push the value of the Return Stack pointer onto the Return Stack.

PUSH-MODE-BITS—Push the value of the MODE REGISTER onto the Parameter Stack.

PUSH-INPUT—Read the 10 dedicated input bits and push the value (right justified and padded with leading zeros) onto the Parameter Stack.

SET-LOOP-COUNTER—Pop the TOP value from the Parameter Stack and store it into LOOP COUNTER.

POP-STACK-PUSH-TO-RSTACK—Pop the TOP item from the Parameter Stack and push it onto the Return Stack.

SET-X-REG—Pop the TOP item from the Parameter Stack and store it into the X Register.

SET-STACK-POINTER—Pop the TOP item from the Parameter Stack and store it into the Stack Pointer.

SET-RSTACK-POINTER—Pop the TOP item from the Parameter

Stack and store it into the Return Stack Pointer.

SET-MODE-BITS—Pop the TOP value from the Parameter Stack and store it into the MODE BITS.

SET-OUTPUT—Pop the TOP item from the Parameter Stack and output it to the 10 dedicated output bits.

OTHER EFFECTS: Instructions which push or pop the Parameter Stack or Return Stack may cause a memory cycle as the stacks overflow back and forth between on-chip and off-chip memory.

LOADING A SHORT LITERAL

A special case of register transfer instruction is used to push an 8-bit literal onto the Parameter Stack. This instruction requires that the 8-bits to be pushed reside in the last byte of a 4-byte instruction group. The instruction op-code loading the literal may reside in ANY of the other three bytes in the instruction group.

EXAMPLE

BYTE 1	BYTE 2	BYTE 3
LOAD-SHORT-LITERAL	QQQQQQQQ	QQQQQQQQ
BYTE 4		
00001111		

In this example, QQQQQQQQ indicates any other 8-bit instruction. When Byte 1 is executed, binary 00001111(HEX 0f) from Byte 4 will be pushed (right justified and padded by leading zeros) onto the Parameter Stack. Then the instructions in Byte 2 and Byte 3 will execute. The microprocessor instruction decoder knows not to execute Byte 4. It is possible to push three identical 8-bit values as follows:

BYTE 1	BYTE 2
LOAD-SHORT-LITERAL	LOAD-SHORT-LITERAL
BYTE 3	BYTE 4
LOAD-SHORT-LITERAL	00001111
SHORT-LITERAL-INSTRUCTION	

LOAD-SHORT-LITERAL—Push the 8-bit value found in Byte 4 of the current 4-byte instruction group onto the Parameter Stack.

LOGIC INSTRUCTIONS

Logical and math operations used the stack for the source of one or two operands and as the destination for results. The stack organization is a particularly convenient arrangement for evaluating expressions. TOP indicates the top value on the Parameter Stack **74**. NEXT indicates the next to top value on the Parameter Stack **74**.

AND—Pop TOP and NEXT from the Parameter Stack, perform the logical AND operation on these two operands, and push the result onto the Parameter Stack.

OR—Pop TOP and NEXT from the Parameter Stack, perform the logical OR operation on these two operands, and push the result onto the Parameter Stack.

XOR—Pop TOP and NEXT from the Parameter Stack, perform the logical exclusive OR on these two operands, and push the result onto the Parameter Stack.

BIT-CLEAR—Pop TOP and NEXT from the Parameter Stack, toggle all bits in NEXT, perform the logical AND operation on TOP, and push the result onto the Parameter Stack. (Another way of understanding this instruction is thinking of it as clearing all bits in TOP that are set in NEXT.)

MATH INSTRUCTIONS

Math instruction pop the TOP item and NEXT to top item of the Parameter Stack **74** to use as the operands. The results are pushed back on the Parameter Stack. The CARRY flag is used to latch the "33rd bit" of the ALU result.

ADD—Pop the TOP item and NEXT to top item from the Parameter Stack, add the values together and push the result back on the Parameter Stack. The CARRY flag may be changed.

ADD-WITH-CARRY—Pop the TOP item and the NEXT to top item from the Parameter Stack, add the values together. If the CARRY flag is "1" increment the result. Push the ultimate result back on the Parameter Stack. The CARRY flag may be changed.

ADD-X—Pop the TOP item from the Parameter Stack and read the third item from the top of the Parameter Stack. Add the values together and push the result back on the Parameter Stack. The CARRY flag may be changed.

SUB—Pop the TOP item and NEXT to top item from the Parameter Stack, Subtract NEXT from TOP and push the result back on the Parameter Stack. The CARRY flag may be changed.

SUB-WITH-CARRY—Pop the TOP item and NEXT to top item from the Parameter Stack. Subtract NEXT from TOP. If the CARRY flag is "1" increment the result. Push the ultimate result back on the Parameter Stack. The CARRY flag may be changed.

SUB-X—

SIGNED-MULT-STEP—

UNSIGNED-MULT-STEP—

SIGNED-FAST-MULT—

FAST-MULT-STEP—

UNSIGNED-DIV-STEP—

GENERATE-POLYNOMIAL—

ROUND—

COMPARE—Pop the TOP item and NEXT to top item from the Parameter Stack. Subtract NEXT from TOP. If the result has the most significant bit equal to "0" (the result is positive), push the result onto the Parameter Stack. If the result has the most significant bit equal to "1" (the result is negative), push the old value of TOP onto the Parameter Stack. The CARRY flag may be affected.

SHIFT/ROTATE

SHIFT-LEFT—Shift the TOP Parameter Stack item left one bit. The CARRY flag is shifted into the least significant bit of TOP.

SHIFT-RIGHT—Shift the TOP Parameter Stack item right one bit. The least significant bit of TOP is shifted into the CARRY flag. Zero is shifted into the most significant bit of TOP.

DOUBLE-SHIFT-LEFT—Treating the TOP item of the Parameter Stack as the most significant word of a 64-bit number and the NEXT stack item as the least significant word, shift the combined 64-bit entity left one bit. The CARRY flag is shifted into the least significant bit of NEXT.

DOUBLE-SHIFT-RIGHT—Treating the TOP item of the Parameter Stack as the most significant word of a 64-bit number and the NEXT stack item as the least significant word, shift the combined 64-bit entity right one bit. The least significant bit of NEXT is shifted into the CARRY flag. Zero is shifted into the most significant bit of TOP.

OTHER INSTRUCTIONS

FLUSH-STACK—Empty all on-chip Parameter Stack locations into off-chip RAM. (This instruction is useful for multitasking applications). This instruction accesses a counter which holds the depth of the on-chip stack and can require from none to 16 external memory cycles.

FLUSH-RSTACK—Empty all on-chip Return Stack locations into off-chip RAM. (This instruction is useful for multitasking applications). This instruction accesses a counter which holds the depth of the on-chip Return Stack and can require from none to 16 external memory cycles.

It should further be apparent to those skilled in the art that various changes in form and details of the invention as shown and described may be made. It is intended that such changes be included within the spirit and scope of the claims appended hereto.

What is claimed is:

1. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.

2. The microprocessor system of claim **1** in which said second clock is a fixed frequency clock.

3. In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:

providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;

using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;

providing an on chip input/output interface for the microprocessor integrated circuit; and

clocking the input/output interface with a second clock independent of the ring oscillator system clock.

4. The method of claim **3** in which the second clock is a fixed frequency clock.

5. The method of claim **3** further including the step of:

transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.

6. A microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and

the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;

an on-chip input/output interface, connected between said said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

7. The microprocessor system of claim **6** wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

8. The microprocessor system of claim **6** wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.

9. The microprocessor system of claim **6** wherein said oscillator comprises a ring oscillator.

10. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

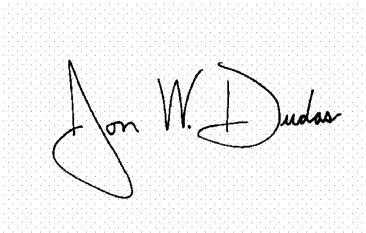
PATENT NO. : 5,809,336
APPLICATION NO. : 08/484918
DATED : September 15, 1998
INVENTOR(S) : Moore et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 34,
Line 25, delete "oscillator" and insert --variable speed clock--.

Signed and Sealed this

Twenty-second Day of May, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office

US005809336C1

(12) **EX PARTE REEXAMINATION CERTIFICATE** (7235th)

United States Patent
Moore et al.

(10) **Number: US 5,809,336 C1**
(45) **Certificate Issued: Dec. 15, 2009**

(54) **HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK**

(75) Inventors: **Charles H. Moore**, Woodside, CA (US); **Russell H. Fish, III**, Mt. View, CA (US)

(73) Assignee: **Patriot Scientific Corporation**, San Diego, CA (US)

Reexamination Request:
No. 90/008,306, Oct. 19, 2006
No. 90/008,237, Nov. 17, 2006
No. 90/008,474, Jan. 30, 2007

Reexamination Certificate for:
Patent No.: **5,809,336**
Issued: **Sep. 15, 1998**
Appl. No.: **08/484,918**
Filed: **Jun. 7, 1995**

Certificate of Correction issued May 22, 2007.

Related U.S. Application Data

(62) Division of application No. 07/389,334, filed on Aug. 3, 1989, now Pat. No. 5,440,749.

(51) **Int. Cl.**

G06F 7/76	(2006.01)
G06F 7/48	(2006.01)
G06F 12/08	(2006.01)
G06F 7/78	(2006.01)
G06F 9/30	(2006.01)
G06F 9/32	(2006.01)
G06F 15/76	(2006.01)
G06F 15/78	(2006.01)
G06F 7/52	(2006.01)
G06F 9/38	(2006.01)
G06F 7/58	(2006.01)

(52) **U.S. Cl.** **710/25**; 711/E12.02; 712/E9.016; 712/E9.028; 712/E9.046; 712/E9.055; 712/E9.057; 712/E9.058; 712/E9.062; 712/E9.078; 712/E9.08; 712/E9.081

(58) **Field of Classification Search** ..... None
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,603,934	A	9/1971	Heath, Jr. et al.
3,696,414	A	10/1972	Allen et al.
3,849,765	A	11/1974	Hamano
3,878,513	A	4/1975	Werner
3,919,695	A	11/1975	Gooding
3,924,245	A	12/1975	Eaton et al.

(Continued)

FOREIGN PATENT DOCUMENTS

EP	0 200 797	A1	11/1986
EP	0 208 287		1/1987
EP	113 516	B1	6/1988

(Continued)

OTHER PUBLICATIONS

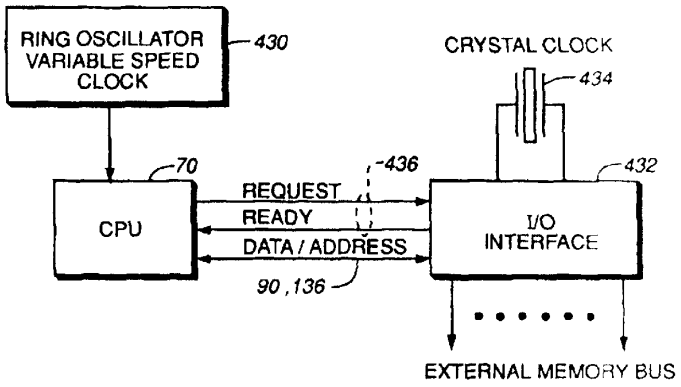
Memorandum Opinion and Order filed Jun. 15, 2007 in 2:05–CV–494 (TJW).
Plaintiffs Technology Property Limited's and Patriot Scientific Corporation's Claim Construction Brief filed Mar. 19, 2007 in 2:05–CV–494 (TJW).

(Continued)

Primary Examiner—Sam Rimell

(57) **ABSTRACT**

A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.



U.S. PATENT DOCUMENTS

3,967,104	A	6/1976	Brantingham et al.
3,968,501	A	7/1976	Gilbert
3,976,977	A	8/1976	Porter et al.
3,980,993	A	9/1976	Bredart et al.
4,003,028	A	1/1977	Bennett et al.
4,003,033	A	1/1977	O'Keefe et al.
4,037,090	A	7/1977	Raymond, Jr.
4,042,972	A	8/1977	Gruner et al.
4,050,058	A	9/1977	Garlic
4,050,096	A	9/1977	Bennett et al.
4,067,058	A	1/1978	Brandstaetter et al.
4,067,059	A	1/1978	Derchak
4,075,691	A	2/1978	Davis et al.
4,079,455	A	3/1978	Ozga
4,107,773	A	8/1978	Gilbreath et al.
4,110,822	A	8/1978	Porter et al.
4,112,490	A	9/1978	Pohlman et al.
4,125,871	A	11/1978	Martin
4,128,873	A	12/1978	Lamiaux
4,144,562	A	3/1979	Cooper
4,217,637	A	8/1980	Faulkner et al.
4,223,380	A	9/1980	Antonaccio et al.
4,223,880	A	9/1980	Brems
4,224,676	A	9/1980	Appelt
4,236,152	A	11/1980	Masuzawa et al.
4,242,735	A	12/1980	Sexton
4,253,785	A	3/1981	Bronstein
4,255,785	A	3/1981	Chamberlin
4,292,668	A	9/1981	Miller et al.
4,295,193	A	10/1981	Pomerene
4,305,045	A	12/1981	Metz et al.
4,315,305	A	2/1982	Siemon
4,315,308	A	2/1982	Jackson
4,317,227	A	2/1982	Skerlos
4,320,467	A	3/1982	Glass
4,321,706	A	3/1982	Craft
4,328,557	A	5/1982	Gastinel
4,334,268	A	6/1982	Boney et al.
4,335,447	A	6/1982	Jerrim
4,338,675	A	7/1982	Palmer et al.
4,348,720	A	9/1982	Blahut et al.
4,348,743	A	9/1982	Dozier
4,354,228	A	10/1982	Moore et al.
4,358,728	A	11/1982	Hashimoto
4,361,869	A	11/1982	Johnson et al.
4,364,112	A	12/1982	Onodera et al.
4,376,977	A	3/1983	Bruinshorst
4,382,279	A	5/1983	Ugon
4,390,946	A	6/1983	Lane
4,396,979	A	8/1983	Mor et al.
4,398,263	A	8/1983	Ito
4,398,265	A	8/1983	Puhl et al.
4,402,042	A	8/1983	Guttag
4,403,303	A	9/1983	Howes et al.
4,412,283	A	10/1983	Mor et al.
4,425,628	A	1/1984	Bedard et al.
4,449,201	A	5/1984	Clark
4,450,519	A	5/1984	Guttag et al.
4,462,073	A	7/1984	Grondalski
4,463,421	A	7/1984	Laws
4,467,810	A	8/1984	Vollmann
4,471,426	A	9/1984	McDonough
4,472,789	A	9/1984	Sibley
4,488,217	A	12/1984	Binder et al.
4,494,021	A	1/1985	Bell et al.
4,509,115	A	4/1985	Manton et al.
4,538,239	A	8/1985	Magar
4,539,655	A	9/1985	Trussell et al.
4,541,045	A	9/1985	Kromer, III
4,541,111	A	9/1985	Takashima et al.
4,553,201	A	11/1985	Pollack et al.
4,556,063	A	12/1985	Thompson et al.
4,562,537	A	12/1985	Barnett et al.
4,566,063	A	1/1986	Zolnowsky
4,577,282	A	3/1986	Caudel et al.
4,607,332	A	8/1986	Goldberg
4,616,338	A	10/1986	Helen et al.
4,626,798	A	12/1986	Fried
4,626,985	A	12/1986	Briggs
4,626,988	A	12/1986	George
4,627,082	A	12/1986	Pelgrom et al.
4,630,195	A	12/1986	Hester et al.
4,630,934	A	12/1986	Arber
4,641,246	A	2/1987	Halbert et al.
4,649,471	A	3/1987	Briggs et al.
4,660,155	A	4/1987	Thaden et al.
4,660,180	A	4/1987	Tanimura et al.
4,665,495	A	5/1987	Thaden
4,670,837	A	6/1987	Sheets
4,679,166	A	7/1987	Berger et al.
4,680,698	A	7/1987	Edwards et al.
4,689,581	A	8/1987	Talbot
4,691,124	A	9/1987	Ledzius et al.
4,698,750	A	10/1987	Wilkie et al.
4,701,884	A	10/1987	Aoki et al.
4,704,678	A	11/1987	May
4,708,490	A	11/1987	Arber
4,709,329	A	11/1987	Hecker
4,710,648	A	12/1987	Hanamura et al.
4,713,749	A	12/1987	Magar et al.
4,714,994	A	12/1987	Oklobdzija
4,720,812	A	1/1988	Kao et al.
4,724,517	A	2/1988	May
4,739,475	A	4/1988	Mensch, Jr.
4,750,111	A	6/1988	Crosby, Jr. et al.
4,758,948	A	7/1988	May et al.
4,760,521	A	7/1988	Rehwald et al.
4,761,763	A	8/1988	Hicks
4,763,297	A	8/1988	Uhlenhoff
4,766,567	A	8/1988	Kato
4,772,888	A	9/1988	Kimura
4,777,591	A	10/1988	Chang et al.
4,780,814	A	10/1988	Hayek
4,783,734	A	11/1988	May et al.
4,787,032	A	11/1988	Culley
4,794,526	A	12/1988	May et al.
4,797,850	A	1/1989	Amitai
4,803,621	A	2/1989	Kelly
4,805,091	A	2/1989	Thiel et al.
4,809,169	A	2/1989	Sfarti et al.
4,809,269	A	2/1989	Gulick
4,811,208	A	3/1989	Myers et al.
4,816,989	A	3/1989	Finn et al.
4,816,996	A	3/1989	Hill et al.
4,819,151	A	4/1989	May
4,833,599	A	5/1989	Colwell et al.
4,835,738	A	5/1989	Niehaus et al.
4,837,563	A	6/1989	Mansfield et al.
4,837,682	A	6/1989	Culler
4,853,841	A	8/1989	Richter
4,860,198	A	8/1989	Takenaka
4,868,735	A	9/1989	Moller et al.
4,870,562	A	9/1989	Kimoto et al.
4,872,003	A	10/1989	Yoshida
4,882,710	A	11/1989	Hashimoto et al.
4,890,225	A	12/1989	Ellis, Jr. et al.
4,899,275	A	2/1990	Sachs et al.
4,907,225	A	3/1990	Gulick et al.
4,910,703	A	3/1990	Ikeda et al.
4,912,632	A	3/1990	Gach et al.
4,914,578	A	4/1990	MacGregor et al.

4,926,323	A	5/1990	Baror et al.
4,931,748	A	6/1990	McDermott et al.
4,931,986	A	6/1990	Daniel et al.
4,933,835	A	6/1990	Sachs
4,942,553	A	7/1990	Dalrymple et al.
4,956,811	A	9/1990	Kajigaya et al.
4,959,782	A	9/1990	Tulpule et al.
4,967,326	A	10/1990	May
4,967,352	A	10/1990	Keida et al.
4,967,398	A	10/1990	Jamoua et al.
4,974,157	A	11/1990	Winfield et al.
4,979,102	A	12/1990	Tokuume
4,980,821	A	12/1990	Koopman et al.
4,988,892	A	1/1991	Needle
4,989,113	A	1/1991	Asal
4,989,133	A	1/1991	May et al.
4,989,135	A	1/1991	Miki
4,990,847	A	2/1991	Ishimaru et al.
5,008,816	A	4/1991	Fogg, Jr. et al.
5,013,985	A	5/1991	Itoh et al.
5,021,991	A	6/1991	MacGregor et al.
5,022,395	A	6/1991	Russie
5,023,689	A	6/1991	Sugawara
5,031,092	A	7/1991	Edwards et al.
5,036,300	A	7/1991	Nicolai
5,036,460	A	7/1991	Takahira et al.
5,047,921	A	9/1991	Kinter et al.
5,053,952	A	10/1991	Koopman, Jr. et al.
5,068,781	A	11/1991	Gillett, Jr. et al.
5,070,451	A	12/1991	Moore et al.
5,081,574	A	1/1992	Larsen et al.
5,091,846	A	2/1992	Sachs et al.
5,097,437	A	3/1992	Larson et al.
5,103,499	A	4/1992	Miner et al.
5,109,495	A	4/1992	Fite et al.
5,121,502	A	6/1992	Rau et al.
5,127,091	A	6/1992	Boufarah et al.
5,127,092	A	6/1992	Gupta et al.
5,134,701	A	7/1992	Mueller et al.
5,146,592	A	9/1992	Pfeiffer et al.
5,148,385	A	9/1992	Frazier
5,157,772	A	10/1992	Watanabe
5,179,689	A	1/1993	Leach et al.
5,179,734	A	1/1993	Candy et al.
5,226,147	A	7/1993	Fujishima et al.
5,237,699	A	8/1993	Little et al.
5,239,631	A	8/1993	Boury et al.
5,241,636	A	8/1993	Kohn
5,261,057	A	11/1993	Coyle et al.
5,261,082	A	11/1993	Ito et al.
5,261,109	A	11/1993	Cadambi et al.
5,325,513	A	6/1994	Tanaka et al.
5,339,448	A	8/1994	Tanaka et al.
5,353,417	A	10/1994	Fuoco et al.
5,353,427	A	10/1994	Fujishima et al.
5,379,438	A	1/1995	Bell et al.
5,410,654	A	4/1995	Foster et al.
5,410,682	A	4/1995	Sites et al.
5,414,862	A	5/1995	Suzuki et al.
5,421,000	A	5/1995	Fortino et al.
5,440,749	A	8/1995	Moore et al.
5,459,846	A	10/1995	Hyatt
5,511,209	A	4/1996	Mensch, Jr.
5,530,890	A	6/1996	Moore et al.
5,537,565	A	7/1996	Hyatt
5,604,915	A	2/1997	Moore et al.
5,659,703	A	8/1997	Moore et al.
5,784,584	A	7/1998	Moore et al.
6,598,148	B1	7/2003	Moore et al.

FOREIGN PATENT DOCUMENTS

EP	0288649	11/1988
JP	58-25710 A	2/1983
JP	61-127228 A	6/1984
JP	61-138356 A	6/1986
JP	62-145413	6/1987
JP	05-189383	7/1998

OTHER PUBLICATIONS

Defendants' Brief Regarding Construction of Disputed Claim Terms of the 336 and 148 Patents filed Apr. 2, 2007 in 2:05–CV–494 (TJW).

Defendants' Brief Regarding Construction of Disputed Claim Terms of the 584 Patent filed Apr. 2, 2007 in 2:05–CV–494 (TJW).

Plaintiffs' Claim Construction Reply Brief filed Apr. 9, 2007 in 2:05–CV–494 (TJW).

Defendants' Unopposed Motion for Leave to File a Sur–Reply Brief Regarding Claim Construction filed Apr. 19, 2007 in 2:05–CV–494 (TJW).

Defendants' Sur–Reply Brief Regarding Construction of Disputed Claim Terms of the 336 Patent filed Apr. 29, 2007 in 2:05–CV–494 (TJW).

Declaration of Roger L. Cook in Support of Plaintiffs Technology Property Limited's and Patriot Scientific Corporations's Claim Construction Brief filed Mar. 19, 2007 in 2:05–CV–00494 (TJW).

Supplemental Declaration of Roger L. Cook in Support of Plaintiffs Technology Property Limited's and Patriot Scientific Corporations's Claim Construction Brief filed Apr. 9, 2007 in 2:05–CV–00494 (TJW).

Declaration of David J. Lender filed Apr. 2, 2007 in 2:05–CV–00494 (TJW).

Supplemental Declaration of Alvin M. Despain in Support of Plaintiffs' Reply Claim Construction Brief filed Apr. 9, 2007 in 2:05–CV–0049 (TJW).

Declaration of Alvin M. Despain in Support of Plaintiffs' Claim Construction Brief filed Mar. 19, 2007 in 2:05–CV–00494 (TJW).

Nakamura et al., "Microprocessors—Special Purpose," 1987 IEEE International Solid–State Circuits Conference, Feb. 26, 1987.

Transputer Reference Manual, INMOS Limited 1988.

Horwitz et al., "A 20–MIPS Peak, 32–bit Microprocessor with On–Chip Cache," *IEEE Journal of Solid State Circuits*, SC–22(5):790–799 (Oct. 1987).

Submicron Systems Architecture Project, Caltech Computer Science Technical Report, Nov. 1, 1991.

Stevens, C. W., "The Transputer," *IEEE*, pp. 292–300 (1985).

Bosshart et al., "A 533K–Transistor LISP Processor Chip", *IEEE Journal of Solid State Circuits*, SC–22(5): 808–819 (Oct. 1987).

Jguppi et al., "A 20 Mips Sustained 32b CMOS with 64b Data Bus," *IEEE Int'l Solid State Circuits Conf.*, pp. 84–86 (1989).

May, D., "The Influence of VLSI Technology on Computer Architecture," pp. 247–256.

"Motorola MC68HC11A8 HCMOS Single–Chip Microcomputer," table of contents and introduction (1985).

"Motorola MC146805H2, advance information," pp. 1–12.

"MC68332 32–Bit Microcontroller System Integration User's Manual Preliminary Edition, Revision 0.8," (1989).

The Ring Oscillator VCO Schematic.

"INMOS T800 Transputer Data Sheet," (Apr. 1987).
"INMOS T414 Transputer Preliminary Data Sheet," (Feb. 1987).
"INMOS T212 Transputer Preliminary Data Sheet," (Aug. 1987).
"INMOS M212 Disk Processor Product Overview," (Oct. 1987).
Budinich et al., eds. *International Conference on the Impact of Digital Microelectronics & Microprocessors on Particle Physics*, pp. 204–213 (1988).
INMOS Presentation given at Jun. 15, 1988 Workshop on Computer Architecture.
Moore, P., "INMOS Technical Note 15: IMS B005 Design of a Disk Controller board with drives," Dec. 3, 1986.
Matthys R. J., *Crystal Oscillator Circuits*, pp. 25–64 (1983).
Elliot et al., eds. *Scientific Applications of Multiprocessors* Prentice Hall (1988).
Transputer Reference Manual, Cover page, Introduction and pp. 73and 96, INMOS Limited (1988).
"INMOS IMS T414 Transputer," (Jun. 1987).
"INMOS IMS T414 Engineering Data," pp. 107–163.
"INMOS Engineering Data, IMS T414M Transputer, Extended Temperature," (Aug. 1987).
"SM550 High Speed CMOS 4–bit Microcomputer SM–550 Series," (1982) document in Japanese.
"MC88100 RISC Microprocessor User's Manual," Motorola (1989).
Mead et al., eds., *Introduction of VLSI Systems*, Addison Wesley Publishers, (1980).
Moelands, A. P. M., "Serial I/O with the MA B8400 series microcomputers," *Electronic Components and Applications*, 3(1):38–46 (1980).
Stanley, R. C., "Microprocessors in brief," *IBM J. Res. Develop.*, 29(2):110–118 (Mar. 1985).
"MC68332 User's Manual," Motorola (1995).
"TMS370 Microcontroller Family User's Guide," Texas Instruments (1996).
"INMOS Preliminary Data IMS T800 transputer," (Apr. 1987).
"INMOS Engineering Data IMS T212 transputer Preliminary," (Aug. 1987).
"INMOS Product Overview IMS M212 disc processor," (Oct. 1987).
"MN18882 LSI User's Manual," (document in Japanese).
"MN1880 (MN18882) Instruction Manual," (document in Japanese).
"MN188166 User's Manual," (document in Japanese).
Paker, Y., *Multi–Processor Systems*, pp. 1–23 (1983).
"HP Sacajawea External Reference Specification Preliminary Version 1.1," (Jan. 14, 1987).
"Data sheet MOS Integrated Circuit uPD75008," NEC (1989).
Product Brochure by Motorola for MC146805H2.
Shyam, M., "Hardware External Reference Specification for Enhanced Champion/Paladin," Revision of Nov. 11, 1986.
Fish deposition transcript, vols. 1 and 2, held Jun. 25, 2007 and Jun. 26, 2007 in case No. 2–05CV–494 (TJW).
Exhibit 4 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); memo of Sep. 12, 1992 Fish to Higgins re: ShBoom Patents.
Exhibit 5 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Sep. 11, 1992 Higgins to Falk re: patent application for High Performance Low Cost Microprocessor.
Exhibit 6 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Sep. 30, 1992 Higgins to Falk re: patent application for High Performance Low Cost Microprocessor.
Exhibit 8 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Mostek 1981 3870/F8 Microcomputer Data Book (1981).
Exhibit 9 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); "IC Master 1980", pp. 2016–2040, published by Fairchild (1980).
Exhibit 10 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of May 12, 1992, Fish to Higgens.
Exhibit 12 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Agreement executed Jan. 3, 1989 between PTA Inc. and Chuck Moore, dba Computer Cowboys.
Exhibit 13 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Oki japan MSH–Boom 96000 Schematic (Jul. 13, 1989).
Exhibit 14 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Assignment of U.S. Appl. No. 07/389,334 from Fish to Fish Family Trust.
Exhibit 15 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Stock Purchase and Technology Transfer Agreement between Fish Family Trust, Helmut Falk, and Nanotronics Corporation (Aug. 16, 1991).
Exhibit 16 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); fax of Jul. 16, 2004Mmarshall to Suanders and Heptig w/ attached Jul. 15, 2004 memo from Beatie re: Fish and Moore.
Exhibit 17 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Fax of Jul. 29, 2004, Heptig to Marshall with attached executed agreement.
Exhibit 18 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Plaintiffs' Second Amended Complaint filed Sep. 22, 2006 in 3:06–CV–00815.
Exhibit 19 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Settlement Agreement between Patriot Scientific Corporation, Fish, and the trustee of Fish Family Trust.
Exhibit 21 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Comparisons of RISC Chips (Dec. 11, 1988).
Exhibit 22 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); VL86C010 An Affordable 32–bit RISC Microprocessor System, VLSI Technology, Inc.
Exhibit 23 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); VY86Cxxx ARM 32–Bit CMOS product literature, EDN (Nov. 21, 1991).
Exhibit 24 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Apr. 26, 1989 Ireland to Fish w/ copy of Apr. 17, 1989 article in Electronic News titled "35ns 256K Device, VLSI Debuts SRAM Designed With Hitachi,".
Exhibit 28 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Introduction to RISC Technology, LSI Logic Corporation (Apr. 1988).
Exhibit 29 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); "SH–Boom Patent Documentation," (Jun. 21, 1989).
Exhibit 30 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); "Sh–Boom Licensing Strategy," (Jan. 19, 1990).

Exhibit 31 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); "Transputer Includes Multiprocessing protocol," Jan. 2, 1991.
Exhibit 32 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); article titled "INMOS details next Transputer," (Apr. 18, 1991).
Exhibit 33 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Articles from Electronic World News.
Exhibit 35 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); INMOS Preliminary Data IMS T414 transputer.
Exhibit 36 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Comparison of Intel 80960 and Sh–Boom Microprocessors (1989).
Exhibit 37 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Memo of Jul. 13, 1989, Fish to Chu w/ attached comparison of MIPS 2000 to Sh–Boom.
Exhibit 38 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); fax of Jun. 10, 1992 Fish to Higgins w/ attached document titled State of the Prior Art ShBoom Microprocessor.
Exhibit 39 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Apr. 12, 1989 Time and Responsibility Schedule.
Exhibit 40 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); handwritten note.
Exhibit 41 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); memo of Jun. 1989 to PT Acquisitions, Inc. re: fees due for searches conducted.
Exhibit 42 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); memo of Jun. 28, 1992 Fish to Higgins re: Dialog Patents re: ShBoom.
Exhibit 43 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Aug. 6, 1998 Haerr to Turner transmitting documents.
Exhibit 44 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); Declaration of Moore re: U.S. Appl. No. 08/484,918.
Exhibit 45 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); fax of Nov. 3, 1989, Leckrone to Fish with attached draft license agreement between PT Acquisitions and Oki Electric Industries.
Exhibit 46 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Nov. 29, 1989 Fish to Slater re: Japanese "borrowing" Sh–Boom 50 MHz RISC Chip.
Exhibit 47 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Dec. 29, 1989 Leckrone to Fish re: ShBoom project.
Exhibit 48 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Jul. 16, 1990 Fish to Leckron re: attorney client relationship and conflict of interest.
Exhibit 49 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Jul. 24, 1990 Leckrone to Fish re: letter of Jul. 16, 1990 (EX 48).
Exhibit 50 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Aug. 27, 1990 Moore to Fish re: ShBoom confidentiality.
Exhibit51 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); PT Acquisitions / Alliance Semiconductor Corp. Manufacturing Agreement (Jul. 20 1990).
Exhibit 52 to Fish deposition of Jun. 25–26, 2007 in case No. 2–05CV–494 (TJW); letter of Feb. 6, 1990 to PT Acquisitions from Dun & Bradstreet Receivable Recovery Systems re: final notice for payment of account.
National Semiconductor HPC16400/HPC36400/HPC46400 High–Performance microControllers with HDLC Controller product literature.
NEC Data Sheet Mos Integrated Circuit uPD7225 Programmable LCD Controller/Driver. Part Nos. uPD7225G00, uPD7225G01, uPD7225GB–3B7.
NEC Electronics Inc. High–End, 8–Bit, Single–Chip CMOS Microcomputers product literature.
NEC Electronics Inc. uPD78C10/C11/C14 8–Bit, Single–Chip CMOS Microcomputers with A/D Converter product literature.
NEC Electronics Inc. Microcomputer Products Single–Chip Products Data Book vol. 1 of 2 cover page.
NEC Electronics Inc. Microcomputer Products Microprocessors, Peripherals, & DSP Products Data Book vol. 2 of 2 cover page.
NEC Electronics Inc. MOS Integrated Circuit uPD70208H, 70216H Data Sheet, V40HL, V50HL, 16/8; 16–Bit Microprocessor.
NEC Electronics Inc. MOS Integrated Circuit uPD7225 Programmable LCD Controller/Driver.
Signetics Microprocessor Data manual cover page.
Signetics Microprocessor Products Data manual, 8×330 Floppy Disk Formatter/Controller product specification.
Signetics Microprocessor Products Data manual, SC96AH Series Single–Chip 16–Bit Microcontrollers preliminary specification.
Realtime DSP; The TMS320C30 Course, Revision 3 (educational document re programming Digital Signal Processor microprocessor).
Texas Instruments TMS320C30 Digital Signal Processor product literature.
Texas Instruments TMS320C30 Digital Signal Processor product literature.
Texas Instruments TMS34010 Graphics System Processor product literature.
Texas Instruments TMS320 DSP Designer's Notebok, Using a TMS320C30 Serial Port as an Asynchronous RS–232 Port Application Brief: SPRA240.
UK application 8233733 as filed Nov. 26, 1982.
Office Action of Jan. 31, 2000 in U.S. Appl. No. 09/124,623.
TPL Infringement Contention for the TLCS–900/L Series.
TPL Infringement Contention for Toshiba Microcontroller.
TPL Infringement Contention for Toshiba TC35273.
Duell, C. H., "Everything that can be invented has been invented," 2 pages downloaded from http://www.tplgroup.net/patents/index.php.
Alliacense Product Report, NEC Microcontroller, UPD789473, B Bit Microcontroller, pp. 1–38.
Mostek Corp., Advertisement, EDN, Nov. 20, 1976.
Guttag, K.M., "The TMS34010: An Embedded Microprocessor," *IEEE Micro*, 8(3):39–52 (May 1988).
"8–Bit Single–Chip Microprocessor Data Book," Hitachi America Ltd., Table of Contents and pp. 251–279) Jul. 1985).
Request for Reexamination of U.S. Patent 6,598,148 as filed Sep. 21, 2006.
Office action of Nov. 22, 2006 in application No. 90/008, 227.
Toshiba TLCS–42, 47, 470 User's Manual Published in Apr. 1986.
Fukui et al., "High Speed CMOS 4–bit Microcomputer SM550 Series," published 1982, 1983.

Intel 80386 Programmer's Reference Manual, published by Intel (1986).
Fairchild Microcomputers, F8/3870, F6800, Bit Slice, IC Master 1980, pp. 1, 2016–2040 (1980).
Mostek Corp., "Mostek 1981 3870/F8 Microcomputer Data Book", Feb. 1981, pp. III–76 through III–77, III–100 through III–129, and VI–1 through VI–31.
IBM Systems Reference Library, IBM System/360 Model 67 Functional Characteristics, File No. S360–01, Form A27–2719–0, published by IBM (1967).
Anderson, D.W., The IBM System/360 Model 91: Machine Philosophy and Instruction Handling, IBM Journal, (1967).
GE–625/ 635 Programming Reference Manual, revised Jan. 1966.
Clipper™ 32–Bit Microprocessor, Introductions to the Cliper Architecture, published by Fairchild in 1986.
Simpson et al., "The IBM RT PC Romp processor and memory management unit architecture," *IBM systems Journal*, 26(4):346–360.
M68300 Family MC68332 User's Manual, published by Motorola, Inc. in 1995.
Ditzel et al., "The Hardware Architecture of the Crisp Microprocessor," AT & T Information Systems, ACM, pp. 309–319 and table of contents (1987).
i860 64–Bit Microprocessor, published by Intel Corporation Feb. 1989.
Rau et al., "The Cydra 5 Departmental Supercomputer, Design Philosophies, Decisions, and Trade–offs," *IEEE* pp. 12–36 (1989).
Datasheet for Intel 4004 Single Chip 4–Bit 9–Channel Microprocessor, pp. 8–15 to 8–23.
Intel MCS–4 Micro Computer Set (Nov. 1971).
Intel 8008 8–Bit Parallel Central Processor Unit published by Intel (Nov. 1972).
iAPX 386 High Performance 32–Bit Microprocessor Product Review, published by Intel (Apr. 1984).
Intel 80386 Programmer's Reference Manual, published in Intel (1986).
Motorola MC68020 32–Bit Microprocessor User's Manual (1984).
Thornton, J. E., "Design of a Computer, The Control Data 6600," published by Advanced Design Laboratory (1970).
6400/6500/6600 Computer Reference Manual, published by Control Data® (1965, 1966, 1967).
Grishman, R., "Assembly Language Programming for the Control Data 6600 and Cyber Series Algorithmics".
Hennessy et al., "MIPS: A Microprocessor Architecture," *IEEE*, pp. 17–22 (1982).
Hennessy et al., "Hardware/software tradeoff for increased performance," *Proceedings of the Symposium on Architectural Support for Programming Languages and Operating Systems*, pp. 2–11, ACM, Apr. 1982.
Hennessy et al., "MIPS: A VLSI Processor Architecture, Technical Report 223," Computer Systems Laboratory, Department of Electrical Engineering and Computer Science, Standford University Nov. 1981.
Gross et al., "Measurement and evaluation of MIPS architecture and processor," *ACM Trans. Computer Systems*, pp. 229–257 Aug. 1988.
Bit Sparc Integer Unit B5000 Datasheet attached to a presentation by Anant Agrawal in 1989.
Sequin et al., "Design and Implementation of RISC1," pp. 276–298 from *VLSI Architecture*, B. Randell and P.C. Treleaven, editors, Prentice Hall, 1983.
Ungar et al., "Architecture of SOAR: Smalltalk on a RISC," *Proceedings of the 11th Annual International Symposium on Computer Architecture ISCA '84*. ACM Press, New York, NY, pp. 188–197 (1984).
Cray–I Computer System Hardware Reference Manual, Publication No. 2240004, Rev C, Nov. 4, 1997.
Acorn Computers, Ltd., Acorn RISC Machine CPU Software Manual, Issue 1.00 Oct. 1985.
Patterson et al., "Architecture of a VLSI Instruction Cache for A RISC," *ACM*, pp. 108–116 (1983).
Patterson, D. A., "Reduced Instruction Set Computers" *Communication of the ACM*, 28(1):8–21, Jan. 1985.
Patterson, D. A., "RISC watch", pp. 11–19 (Mar. 1984).
Sherburne, R. W., "Processor Design Tradeoffs in VLSI," U.C. Berkeley, May 1984. PhD Dissertation.
Excerpt from A Seymour Cray Perspective http://research.Microsoft.com/users/gbell/craytalk/std001.htm (Slide 1).
Excerpt from A Seymour Cray Perspective htpp.//research.microsoft.com/users/gbell/craytalk/std029.htm (Slide 29).
RISC Roots: CDC 6600 (1965).
http://www.bitsavers.org/pdf/tdc/6x00/.
Simpson, R.O., "The IBM RT Personal computer," *BYTE*, 11(11):43–78 (Oct. 1986).
Ryan, D.P., "Intel's 80960: An Architecture Optimized for Embedded Control," *IEEE, Micro,* published in Jun. 1988.
Waters, F., "IBM RT Personal Computer Technology," IBM Corp. 1986.
Alliacense Product Report, USP 5784584, TLCS–900/H1 Series TMP92C820, Toshiba Microcontroller TMP92C820 / TLCS–900/H1 Series 16–bit Microcontroller, pp. 1–9, filed Aug. 14, 2006 in 2:05–CV–00494–TJW.
Alliacense Product Report, NEC Microcomputer, USP 5784584, V850E2 32 Bit Microcontroller, pp. 1–8 (2006).
"8 bit Dual 1–chip Microcomputer MN1890 Series User's Manual," translation of original Japanese language document, by Matsushita Electric Industrial Co., Ltd. Semiconductor Sales Division.
Sibigtroth, J. M., "Motorola's MC68HC11: Definition and Design of a VLSI Microprocessor," *IEEE Micro* 4(1):54–65 (1984).
"Specification Sheet, MN18882 (Book)," translation of the Japanese language original, Code No. MIG0175, Matsushita Electronics Industry Corporation, Microcomputer Products Division, Oct. 2, 1990.
"DS5000 Soft Microcontroller User's Guide Preliminary V 1.0," Dallas Semiconductor.
MN188166 User's Manual, Japanese language document with English translation.
Alliacense Product Report—Preliminary Review, USP 5,440,749; GPS Car Navigation Main Processor.
Alliacense Product Report—Preliminary Review, USP 5,440,749; GSP Navigation System GPS Chipset.
Alliacense Product Report—Preliminary Review, USP 5,440,749; GPS Navigation System Main Microprocessor.
Alliacense Product Report—Preliminary Review, USP 5,440,749; Kyocera Digital Camera Finecam S3R Image Processor.
Alliacense Product Report—Preliminary Review, USP 5,440,749; PDA/Mobile Navigation, GPS Processor.
Motorola MC68020 32–bit Microprocessor User's Manual, 2nd Edition, Rev. 1, Prentice–Hall, 1985.
Barron et al., "The Transputer," *Electronics*, pp. 109–115 (1983).

Burroughs Corporation, "Burroughs B7700 Systems Reference Manual," 1973.
Fiasconaro, J., "Microarchitecture of the HP9000 Series 500 CPU," *Microarchitecture of VLSI Computers, NATO ASI Series No. 96*, Antognetti, eds., pp. 55–81.
MacGregor et al., "The Motorola MC68020," *IEEE Micro*, 4(4):103–118 (1984).
Best et al., "An Advanced–Architecture CMOS/SOS Microprocessor", IEEE Micro, vol. 2, No. 3, vol. 2, No. 3 (Jul. 1982), pp. 10–26.
Technology Properties Limited (TPL), Moore Microprocessor Patent (MMP) Portfolio, downloaded from <<www.tpl-group.net/patents/index.php>> downloaded on Aug. 3, 2006, 3 pages total.
Acorn's RISC Leapfrog, Acorn User special issue, Jun. 1987; 59: 149–153.
Agrawal, et al., "Design Considerations for a Bipolar Implementation of SPARC," Compcon Spring apos;88. Thirty–Third IEEE Computer Society International Conference, Digest of Papers, Feb. 29–Mar. 3, 1988, pp. 6–9.
Agrawal, "An 80 MHz Bipolar ECL Implementation of SPARC," Sun Microsystems, Inc., Jun. 25, 1989, 40 pages total.
ARM Datasheet, Part No. 1 85250 0360 0, Issue No. 1 (Mar. 17, 1987).
Atmel SPARC Instruction Set, "Assembly Language Syntax," Rev. 4168C–AERO–08/01, 2002.
Bagula, "A 5V Self–Adaptive Microcomputer with 16Kb of #2 Program Storage and Security," IEEE International Solid–State Circuit Conference, 1983, pp. 34–35.
Bayko, Great Microprocessors of the Past and Present (V 11.7.0), downloaded from: <<http://web.archive.org/web/20010107210400/http://bwrc.eecs.berkeley.edu/CIC/Archive/cup_history.html>>, Feb. 2007, 60 pages total.
Books Review: Operating Systems A Systematic View, William S. Davis, Addison–Wesley Publishing Company, Inc., 1987; 26(4):453–454.
Bourke, "Character Synchronization During Overrun Conditions," Delphion, IBM Technical Disclosure Bulletin, Dec. 1977.
Burroughs Corporation, "Burroughs B5500 Information Processing System Reference Manual," 1973.
CAL Run Fortran Guide, University of California, Computer Center, Berkeley, 292 pages total, (Sep. 1974).
CDC 6000 Computer Systems—Cobol Instant 6000, Version 3; Control Data Publication No. 60327600A (Apr. 1971).
CDC 6000 Computer Systems, 7600 Computer Systems: Fortran Extended Instant 6000 Version 3, 7600 Version 1; Control Publication No. 60305900A (May 1971).
CDC 6000 Computer Systems/7600 Computer Systems: Fortran Extended Reference Manual, 6000 Version 3, 7600 Version 1; Control Data Publication No. 60329100, Revision D (1972).
CDC 6000 Series Computer System, 6642 Distributive Data Path Operation and Programming Reference Manual; Control Data Publication No. 60376300C (Mar. 1979).
CDC 6000 Series Computer Systems—Chippewa Operating System Documentation, vol. I, Preliminary Edition (updated May 1966).
CDC 6000 Series Computer Systems—Chippewa Operating System Documentation, vol. II, Preliminary Edition, Peripheral Packages and Overlays (Oct. 1965).
CDC 6000 Series Computer Systems—Chippewa Operating System Documentation, vol. III, Preliminary Edition, DSD—The Systems Display, (Nov. 1965).
CDC 6000 Series Computer Systems Ascent General Information Manual; Control Data Publication No. 60135400 (Feb. 66).
CDC 6000 Series Computer Systems Chippewa Operating System Reference Manual; Control Data Publication No. 60134400 (Dec. 1965).
CDC 6000 Series Computer Systems Hardware Reference Manual; Control Data Publication No. 60100000 (Aug. 1978).
CDC 6000 Series Computer Systems/ 7600 Computer System: 6000 Compass Version 2, 7600 Versions 1 & 2 Reference Manual; Control Data Publication No. 60279900, Revision D, (1970, 1971, 1972).
CDC 6000 Series Computer Systems: Chippewa Operating System Fortran Reference Manual; Control Data Publication No. 60132700A (May 1966).
CDC 6000 Series Computer Systems: Peripheral Equipment Reference Manual; Control Data Publication No. 60156100, Revision J (Mar. 1970).
CDC 6000 Series Computer Systems: Site Preparation and Installation Manual; Control Data Publication No. 60142400, Revision B (Sep. 1965).
CDC 6000 Series Computer Systems: Fortran Extended General Information, Control Data Publication No. 60176400 (Oct. 1966).
CDC 6000 Series Fortran Extended 4.0, Internal Maintenance Specifications , (1971).
CDC 6000 Series Introduction and Peripheral Processors Training Manual, Second Edition, Control Data Publication No. 60250400 (Nov. 1968).
CDC 6400 Central Processor, Control Data Publication No. 60257200 (Feb. 1967).
CDC 6400/6500/6600 Ascent–to–Compass Translator; Control Data Publication No. 60191000 (Mar. 1967).
CDC 6400/6500/6600 Computer System Input/Output Specification; Control Data Publication No. 60045100 (Sep. 1967).
CDC 6400/6500/6600 Computer System Instant SMM; Control Data Publication No. 60299500 (Nov. 1969).
CDC 6400/6500/6600/ Computer Systems Compass Reference Manual; Data 60190900, Revision B (Mar. 1969).
CDC 6400/6500/6600 Computer Systems Reference Manual; Control Data Publication No. 60100000, Revision K (Aug. 1970).
CDC 6400/6500/6600 Extended Core Storage Systems Reference Manual; Control Data Publication No. 60225100, (Feb. 1968).
CDC 6400/6500/6600 Jovial General Information Manual; Control Data Publication No. 60252100A (Mar. 1969).
CDC 6400/6500/6600 Computer Systems: Ascent/Asper Reference Manual; Control Data Publication No. 60172700 (Jul. 1966).
CDC 6400/6600 Fortan Conversion Guide; Data Publication No. 60175500 (Aug. 1966).
CDC 6400/6600 Systems Bulletin (Oct. 10, 1968), 84 pages.
CDC 6400/6600, Export/Import 8231 Reference Manual; Data Publication No. 60189100 (Apr. 1967).
CDC 6600 Central Processor vol. 1; Control & Memory; Data Control Publication Nol. 021067 (Mar. 1967).
CDC 6600 Central Processor, vol. 2, Functional Units; Control Data Publication No. 60239700 (Mar. 1967).

CDC 6600 Chassis Tabs; Control Data Publication No. 63016700A (Apr. 1965).

CDC 6600 Chassis Tabs; Control Data Publication No. 63019800 (Mar. 1965).

CDC 6600 Chippewa Operating System; Control Data Publication No. 60124500, Revision C (Apr. 1965).

CDC 6600 Computer System 6601 A–J, 6613A/B/C, 6604A/B/C, 6614–A/B/C/ Central Processor (including Functional Units) vol. 1, Diagrams & Circuit Description; Control Data Publication No. 60119300BT (Jan. 1968).

CDC 6600 Computer System 6601 A–J, 6613A/B/C, 6604A/B/C/, 6614–A/B/C Peripheral and Control Processor/Central Memory/Clock/Extended Core Storage Coupler (Std Opt 10102 and/or Spec Opt 60080)/Power Wiring, vol. 2, Diagrams & Circuit Descriptions; Control Data Publication No. 60119300BT (Jan. 1968).

CDC 6600 Computer System Operating System/Reference Manual, SIPROS66, 1st ed.; Control Data Publication No. 60101800A (1965).

CDC 6600 Computer System Programming System/Reference Manual, vol. 1. Ascent; Control Data Publication No. 601016008 (1965).

CDC 6600 Computer System Programming System/Reference Manual, vol. 2, Asper; Control Data Publication No. 60107008 (1965).

CDC 6600 Computer System Programming vol. 3, Fortran 66; Control Data Publication No. 60101500B (1965).

CDC 6600 Computer Training Manual vol. 2, Preliminary Edition, Section 7.2 Shift Functional Units, 164 pages.

CDC 6600 Data Channel Equipment 6602–B/6612–A, 6603–B, 6622–A, 6681–B, 6682–A6683–A, S.O. 60022, 60028, 60029, Diagrams & Circuit Description' Control Data Publication No. 60125000, Revision G (Jun. 1966).

CDC 6600 Training Manual; Control Data Publication No. 60147400, Revision A (Jun. 1965).

CDC 6603—A/B/C Disk File Controller Reference Manual; Control Data Publication No. 60334000 (1970).

CDC 6638 Disk File Subsystem Training Supplement; Control Data Publication 602500800A (Oct. 1968).

CDC 6638 Disk File System Standard Option 10037–A, 6639–A/B File Controller—Diagrams and Circuit Description/Maintenance/Maintenance Aids/Parts List/Wire Lists/Chassis Tabs; Control Data No. 60227300, Revision H (Mar. 1974).

CDC 6639—A/B Disk File Controller Reference Manual; Control Data Publication No. 60334100E (Aug. 1973).

CDC 6639 Disk Controller Training Manual Test Edition (Sep. 1967), 28 pages.

CDC APL Version 2 Reference Manual, CDC Operating Systems :NOS; Control Data Publication No. 60454000F (Nov. 1980).

CDC Basic Version 3 Reference Manual: NOS 1 & NOS/BE 1; Control Data Publication No. 19983900G (Oct. 1980).

CDC Chippewa Operating System, Document Class ERS, System No. E012, Version 1.1; External Reference Specifications—Chippewa Operating System, (Jun. 1966).

CDC Chippewa Operating System, Document Class SIR, System No. E012, Version 1.0, (Mar. 3, 1966).

CDC Chippewa Operating System, Document Class SIR, System No. E012, Version 1.1, (Mar. 3, 1966).

CDC Cobol Version 4 Instant Manual, Cyber 170 Series, Cyber 70 Models 72, 73, 74, 6000 Series; Control Data Publication No. 60497000A (Feb. 1976).

CDC Cobol Version 5 Instant Manual, Operating Systems: NOS 1/BE 1; Control Data Publication No. 60497300B (Feb. 198).

CDC Codes/Control Data 6400/6500/6600 Computer Systems; Control Data Publication No. 60141900, Revision C (1966, 1967).

CDC Codes/Control Data 6400/6500/6600/6700 Computer Systems; Control Data Publication No. 60141900, Revision D (1966, 1967).

CDC Codes/Control Data 6600; Control Data Publication No. 60141900, Revision A (May 1965).

CDC Compass Version3 Instant, Operating Systems: NOS 1, NOS 2, NOS/BE 1, Scope 2; Control Data Publication No. 60492800D (Jun. 1982).

CDC Course No. FH4010–1C, NOS Analysis, Student Handbook, Revision C (Apr. 1980).

CDC Course No. FH4010–4C NOS Analysis, Study Dump (Apr. 1980).

CDC Cyber 170 Models 720, 730, 740, 750 and 760 Model 176 (Level B/C) Computer Systems, Codes; Control Data Publication No. 60456920C, (Jun. 1981).

CDC Cyber 70 Computer Systems Models 72, 73, 74, 6000 Computer Systems: Fortran Reference Manual Models 72, 73, 74 Version 2.3, 6000 Version 2.3; Control Data Publication No. 19980400, Revision F (Jul. 1972).

CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems—ALGOL Reference Manual, Cyber 70 Series Version 4, 6000 Series Version 4, 7600 Series Version 4; Control Data Publication No. 60384700A (Aug. 1973).

CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems: Cobol Instant Models 72, 73, 74 Version 4, Model 76 Version 1, 6000 Version 4; Control Data Publication No. 60328400A (Dec. 1971).

CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems: Fortran Extended Instant Models 72, 73, 74 Version 4, Model 76 Version 2, 7600 Version 2, 6000 Version 4; Control Data Publication No. 60357900A (Nov. 1971).

CDC Cyber 70 Computer Systems Models 72, 73, 74, 76 7600 Computer System, 6000 Computer Systems: Fortran Extended Reference Manual Models 72, 73, 74 Version 4, Model 76 Version 2, 6000 Version 4; Control Data Publication No. 60306600A (Oct. 1971).

CDC Cyber 70 Series 6000 Series Computer Systems: APL *Cyber Reference Manual; Control Data Publication No. 19980400B (Jul. 1973).

CDC Cyber 70 Series Computer Systems 72, 73, 74, 6000 Series Computer Systems—Kornos 2.1 Workshop Reference Manual; Control Data Publication No. 97404700D (1976).

CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, Krono 2.1 Operator Guide; Control Data Guide; Control Data Publication 60407700A (Jun. 1973).

CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, Kronos 2.1 Installation Handbook; Control Data Publication No. 60407500A (Jun. 1973).

CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, Kronos 2.1 Time–Sharing User's Reference Manual; Control Data Publication No. 60407600B (May 1974).

CDC Cyber 70/ Model 76 Computer System, 7600 Computer System: Fortran Run, Version 2 Reference Manual; Control Data 60360700C (May 1974).
CDC Cyber Interactive Debug Version 1 Guide for Users of Fortran Extended Version 4, CDC Operating Systems: NOS 1, NOS/ BE1, Control Data Publication No. 60482700A (Feb. 1979).
CDC Cyber Interactive Debug Version 1 Guide for Users of Fortran Version 5, Operating Systems: NOS 1, NOS/ BE 1; Control Data Publication No. 6048100C (Sep. 1984).
CDC Cyber Interactive Debug Version 1 Reference Manual, NOS 1, NOS 2, NOS/ BE 1; Data Control Publication No. 60481400D (Jun. 1984).
CDC Cyber Loader Version 1 Instant, CDC Operating System NOS1, NOS/ BE 1; Control Data Publication No. 60449800C (Aug. 1979).
CDC Disk Storage Subsystem—Operation and Programming Manual; Control Data Publication No. 60383900, Version T (1972–1980).
CDC Fortran Extended 2.0, Document Class ERS, System No. C012, (Dec. 1966).
CDC Fortran Extended 2.0, Document Class IMS, Internal Maintenance Specifications—64/65/6600 V Fortran Extended Version 2 (Mar. 1969).
CDC Fortran Extended Version 4 Instant Manual, Operating Systems: NOS 1, NOS/BE, 1 Scope 2; Control Data Publication No. 60497900B (Jun. 1981).
CDC Fortran Extended, Sales Technical Memorandum (May 1967).
CDC Fortran Version 5 Instant, CDC Operating System: NOS 1, NOS/ BE 1, Scope 2; Control Data Publication No. 60483900A (Jan. 1981).
CDC GED Fortran Extended 1.0, Product No. C012, Dept. No. 254, Project No. 4P63FTN (Aug. 1967).
CDC Instant 6400/3500/6500 Simula; Control Data Publication No. 60235100, Revision A (Feb. 1969).
CDC Instant 6400/6500/6600 Compass; Control Data Publication No. 60191900, Revision A (1968).
CDC Instant Fortran 2.3 (6000 Series); Data Publication No. 60189500D (May 1969).
CDC Internal Maintenance Specification; Fortran V5.; Control Data Publication No. 77987506A.
CDC Internal Maintenance Specification; Fortran V5.; Control Data Publication No. 77987506A.
CDC Kronos 2.1 Reference Manual vol. 1 of 2; Control Data Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems; Control Data Publication No. 60407000D (Jun. 1975).
CDC Kronos 2.1 Time–Sharing User's Reference Manual, Cyber 70 Series Models 72, 73, 74, 6000 Series Computer Systems; Control Data Publication No. 60407600D (Jun. 1975).
CDC Model dd 60A Computer Control Console/Customer Engineering Manual; Control Data Publication No. 82100010 (Mar. 1965).
CDC Model dd60b Computer Control Console/Customer Engineering Manual/ Control Data Publication No. 82103500 (Feb. 1967).
CDC Network Products: Network Access Method Version 1, Network Definition Language Reference Manual; Control Data Publication No. 60480000J (May 1981).
CDC Network Products: Network Terminal User's Instant—Operating System NOS 1; Control Data Publication No. 60456270C, (Oct. 1980).
CDC NOS 2 Operations Handbook; Control Data Publication No. 60459310, (Aug. 1994).
CDC NOS Version 1 Applications Programmer's Instant, CDC Computer Systems; Cyber 170 Series, Cyber 70 Models, 71, 72, 73, 74, 6000 Series; Control Data Publication No. 60436000H (Jan. 1980).
CDC NOS Version 1 Internal Maintenance Specification vol. 1 of 3; Control Data Publication No. 60454300B (Aug. 1979).
CDC NOS Version 1 Internal Maintenance Specification vol. 2 of 3; Control Data Publication No. 60454300B (Aug. 1979).
CDC NOS Version 1 Internal Maintenance Specification vol. 3 of 3; Control Data Publication No. 60454300B (Aug. 1979).
CDC NOS Version 1 Operator's Guide, CDC Computer Systems: Cyber 170 Series, Cyber 70 Model 71, 72, 73, 74, 6000 Series (Dec. 1980).
CDC NOS Version 1 Reference Manual vol. 1 of 2, CDC Computer Systems: Cyber 170 Series, Cyber 70 Models 71,72, 73, 74, 6000 Series; Control Data Publication No. 60435400J (1979).
CDC NOS Version 1 Reference Manual vol. 2 of 2, CDC Computer Systems: Cyber 170 Series, Cyber 70 Models 71, 72, 73, 74, 6000 Series; Control Data Publication No. 60445300E (1977).
CDC NOS Version 1 System Maintenance Reference Manual; Control Data Publication No. 60455380H (Apr. 1981).
CDC NOS Version 2 Analysis Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60459300D (Oct. 84).
CDC NOS Version 2 Analysis Handbook; Control Data Publication No. 60459300U (Jul. 1994).
CDC NOS Version 2 Installation Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60459320E_(Mar. 1985).
CDC NOS Version 2 Operation/Analysis Handbook, Cyber 170, Cyber 70 Models 71, 72, 73, 74 6000, Control Data Publication No. 60459310C (Oct. 1983).
CDC NOS Version 2 System Maintenance Reference Manual, Cyber 170, Cyber 70 Models 71, 72, 73 74, 6000; Control Data Publication No. 60459300C (Oct. 1983).
CDC NOS/BE Version 1 Diagnostic Handbook, Cyber 180; Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publicaton No. 60494400–V (1986).
CDC NOS/BE Version 1 Installation Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60494300AB (Dec. 1988).
CDC NOS/BE Version 1 Reference Manual, Cyber 170 Series, Cyber 70 Models 71, 72, 73, 74, 6000 Series; Control Data Publication No. 60493800M 1981.
CDC Outline of Reports on Feasibility Study of 64/6600 Fortran Ver 3.0 and Conversational Fortran, Fortran Study Project, Product No. X010, Dept. No. 254, Project No. 4P63, (Jun. 1966).
CDC Pascal Version 1 Reference Manual, Operating Systems: NOS 2; Control Data Publication No. 60497700 (Sep. 1983).
CDC Pascal Version 1 Reference Manual, Operating Systems: NOS 2; Control Data Publication No. 60497700A (Dec. 1982).

CDC PL/1 Version 1 Instant, CDC Operating Systems: NOS 1, NOS/ BE1, Control Data Publication No. 60483700A (Nov. 1979).
CDC Simscript 11.5 Instant, Control Data Publication No. 84000450B (Sep. 1978).
CDC Sort/Merge Version 4 and 1 Instant, Operating Systems: NOS 1, NOS/BE 1, Scope 2; Control Data Publication No. 60497600C (Jan. 1981).
CDC Sort/Merge Vision 5 Reference Manual, Operating Systems: NOS 2, NOS/ BE 1; Control Data Publication No. 60484800C (Feb. 1984).
CDC SYMPL Version 1 Instant, NOS 1, NOS/BE 1, Scope 2; Control Data Publication No. 60482600A (May 1978).
CDC SYMPL Version 1 Users Guide, Operating Systems: NOS 1, NOS/BE 1, Scope 2; Control Data Publication No. 60499800B (Apr. 1978).
CDC Update Instant, Cyber 170 Series, Cyber 70 Series, 6000 Series, 7600 Computer Systems; Control Data Publication No. 60450000A (Nov. 75).
CDC Update Reference Manual Operating Systems: Scope 3.4, Kronos 2.1; Control Data Publication No. 60342500, Revision H (1971–1976).
CDC Xedit Version 3 Reference Manual, Operating System: NOS 1; Control Data Publication No. 60455730B (Aug. 1979).
Chippewa Laboratories Fortran Compiler Run, Preliminary Edition, CDC 6000 Series Computer Systems, (Apr. 1966).
Cho et al., WAM 3.6: A 40K Cache Memory and Memory Management Unit, ISSCC '86, Feb. 19, 1986.
Cordell, II et al., "Advanced Interactive Executive Program Development Enviornment," IBM Systems Journal, 1987; 26(4):381–382.
Crawford, "The i486 Executing Instructions in One Clock Cycle," IEEE Micro, pp. 28–36 (Feb. 1990).
Disk Routines and Overlays, Chippewa Operating System, CDC Development Division—Applications, (Nov. 1965).
Dowsing et al., "Computer Architecture: A First Course, Chapter 6: Architecture and the Designer," Van Nostrand Reinhold (UK) Co. Ltd., pp. 126–139.
Evans et al., "An Experimental 512–bit Nonvolatile Memory with Ferroelectric Storage Cell," IEEE Journal of Solid–State Circuits, 23(5):1171–1175.
Field Maintenance Print Set, KA780–01–01 Rev. A.
Fisher et al., "Very Long Instruction Word Architectures and the ELI–512," ACM pp. 140–150 (1983).
Furber, VSLI RISC Architecture and Organization, Chapter 3: Commercial VLSI RISC, pp. 124–129, Marcel Dekker, Inc., 1989.
GB Patent Application 8233733, INMOS, Ltd. Microcomputer, filed Nov. 26, 1962.
GE 600 Series, publication.
Gershon, Preface, IBM Systems Journal 26(4):324–325.
Green et al., "A Perspective on Advanced Peer–to–Peer Networking," IBM Systems Journal, 1987; 26(4):414–428.
Grimes et al., "64–bit Processor, The Intel i860 64–Bit Processor: A General–Purpose CPU with 3D Graphics Capabilities", published by Intel, p. 85 (Jul. 1989).
Hansen, "A RISC Microprocessor with Integral MMU and Cache Interface," ICCD '86, pp. 145–148, 1986.
Hennessy et al., "Hardware/software Tradeoff for Increased Performance," Technical Report No. 22.8, Computer Systems Laboratory, Feb. 1983, 24 pages.
Hennessy et al., "The MIPS Machine", COMPCON, IEEE, Spring 1982, pp. 2–7.
Hennessy, "Performance Issues in VLSI Processor Design," IEEE on VLSI in Computers, pp. 153–156 (1983).
Hinton, 80960—Next Generation, Compcon Spring 89, IEEE, 13–18 (1989).
Hollingsworth et al., "The Fairchild Clipper: Instruction Set Architecture and Processor Implementation," Report No. UCB/CSD 87/329, Computer Science Division (EECS), University of California Berkeley, California, (Feb. 11, 1987).
HP 9000 Instrument Controllers, Technical Specifications Guide, Oct. 1989.pdf.
HP 9000 Series Computer Systems, HP–UX Reference 09000–090004, Preliminary Nov. 1982.
Hughes, "Off–Chip Module Clock Controller", Delphion, IBM Technical Disclosure Bulletin, Sep. 1989.
Hunter, "Introduction to the Clipper Architecture," IEEE Micro, pp. 6–26 (Aug. 1987).
IBM RT PC, BYTE 1986 Extra Edition, Inside The IBM PCs, pp. 60–78.
INMOS Limited, IMS T424 Transputer Reference Manual, 1984.
Intel 388Tm DX Microprocessor 32–Bit CHMOS Microprocessor With Integrated Memory Management (1995).
Intel 80960CA User's Manual published by Intel (1989).
Intel Architecture Optimization Manual, Order No. 242816–003, published by Intel (1997).
Intel Architecture Software Developer's Manual, vol. 1; Basic Architecture, published by Intel (1997).
Intel 8080A/8080A–1/8080A–2, 8–Bit N–Channel Microprocessor, Order No. 231453–001, Its Respective Manufacturer (Nov. 1986).
Johnson et al., "A Variable Delay Line PLL for CPU–Coprocessor Synchronization," IEEE Journal of Solid–State Circuits, 23(5): 1218–1223, Oct. 1988.
Katevenis et al., "Reduced Instruction Set Computer Architecture for VLSI," Doctoral Dissertation, Oct. 1983.
Katevenis et al., "The RISC II Micro–Architecture," Journal of VLSI and Computer Systems, 1(2):138–152 (1984).
Kipp, "Micron Technology Inc. Reports Financial Results," Business Wire, New York, Sep. 26, 1988.
Kohn et al., "Introducing Intel i860 64–Bit Microprocessor," Intel Corporation, IEEE Micro (Aug. 1989).
Koopman, "RTX 4000," Proceedings of 1989 Rochester Forth Conference, pp. 84–86.
Koopman, "The WISC Concept: A proposal for a writable instruction set computer," BYTE, pp. 187–193. (Apr. 1987).
Koopman, Jr. et al. "MVP Microcoded CPU/16 Architecture," Proceedings of 1986 Rochester Forth Conference, pp. 277–280.
Koopman, Jr. et al., "WISC Technologies, Inc., Writable Instruction Set, Stack Oriented Computers: The WISC Concept," 1987 Rochester Forth Conference, Journal of Forth Application and Research, 5(1):49–71.
Koopman, Jr., Slack Computers: the new wave, 1989.
Loucks et al., "Advanced interactive Executive (AIX) Operating System Overview," IBM Systems Journal, 1987; 26(4):326–345.
Matick, "Self–Clocked Cache," Delphion, IBM Technical Disclosure Bulletin, Apr. 1985.
Miller, Frequency Modulated Ring Oscillator for a Mode Regulated Substrate Bias Generator, Delphion, IBM Technical Disclosure Bulletin, Sep. 1989.
Mills et al, "Box Structured Information Systems," IBM Systems Journal, 1987; 26(4):395–413.

MMP Portfolio, News Release: Roland Becomes 50th Licensee, Setting a Major Milestone in Moore Microprocessor Patent Licensing Program, 3 pages (May 1, 2009).

Moussouris et al., "A CMOS RISC Processor Integrated System Functions," Proceedings of 31st IEEE Computer Society International Conference, Cathedral Hill Hotel, San Francisco, CA Mar. 3–6, 1986, pp .126–131, 1986.

Olson, Semiconductor Die with Wiring Skirt (Packaging Structure), Delphion, IBM Technical Disclosure Bulletin, Jul. 1978.

O'Neil, "Pipeline Memory System for Drams", Delphion, IBM Technical Disclosure Bulletin, May 1989.

Patterson et al., "RISC I: A Reduced Instruction Set VLSI Computer," Proceedings of the 8th annual symposium on Computer Architecture on Computer Architecture, Miinneapolis, Minnesota, pp. 443–457 (May 1981).

Pountain, "The Archimedea A310," BYTE, 1987.

Przybyiski et al., "Organization and VLSI Implementation of MIPS," Technical Report CSL–TR–84–259, Apr. 1984.

Przybyiski, "The Design Verification and Testing of MIPS", 1984 Conference on Advanced Research in VLSI, pp. 100–109.

Roche et al., "Method of Assuring a Two–Cycle Start, Zero Cycle Stop, Non–Chopping on Chip Clock Control Throughout a VLSI Clock System," Delphion, IBM Technical Disclosure Bulletin, Sep. 1989.

Rowen et al., "A Pipelined 32b NMOS Microprocessors and Microcontrollers," IEEE International Solids–State Circuits Conference, pp. 180–181, 1984.

Rubinfeld et al., "The CVAX CPU, A CMOS VAX Microprocessor Chip", International Conference on Computer Design, Oct. 1987.

Sanamrad et al., "A Hardware System Analysis Processor," IEEE, Aug. 1987, pp. 73–80.

Shih, "Microprogramming Heritage of RISC Design," Proceedings of the 23rd annual workshop and symposium on Microprogramming and microarchitecture, pp. 275–280 (1990).

Sultan et al., "Implementing System–36 Advanced Peer–to–Peer Networking," IBM Systems Journal, 1987; 26(4):429–452.

Thornton, J. E., "Considerations in Computer Design Leading Up To the Control Data 6600," Control Data Chippewa Laboratory (1970).

VAX 11/780 Architecture Handbook vol. 1, 1977–1978, 2–7 and G–8.

VAX 8800 System Technical Description vol. 2, EK–KA881–TD–PRE, Section 6, Instruction Box (IBOX), Preliminary Edition (Jul. 1986).

VAX Maintenance Handbook; VAX–11/780, EK–VAXV2–HB–002, 1983 Edition.

VL86C010 RISC Family Data Manual, Application Specific Logic Product Division, 1987.

Waters et al., "AIX Usability Enhancements and Human Factors," IBM Systems Journal, 1987; 26(4):383–394.

Williams, "Chip Set Tackles Laptop Design Issues, Offers Flat–Panel VGA Control," Computer Design, Oct. 15, 1988; 27(19):21–22.

IEEE Std 796–1983, Microcomputer System Bus, pp. 9–46 (Dec. 1983).

Mead & Conway, Introduction to VLSI Systems, pp. 1–429 (1980).

EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

ONLY THOSE PARAGRAPHS OF THE SPECIFICATION AFFECTED BY AMENDMENT ARE PRINTED HEREIN.

Column 17, lines 12–37:

Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor **50** provides a dual-clock scheme as shown in FIG. **17**, with the CPU **70** operating **[**a synchronously**]** *asynchronously* to I/O interface **432** forming part of memory controller **118** (FIG. **2**) and the I/O interface **432** operating synchronously with the external world of memory and I/O devices. The CPU **70** executes at the fastest speed possible using the adaptive ring counter clock **430**. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor **50** for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface **432**, speed of which is controlled by a conventional crystal clock **434**. The interface **432** processes requests for memory accesses from the microprocessor **50** and acknowledges the presence of I/O data. The microprocessor **50** fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. By decoupling the variable speed of the CPU **70** from the fixed speed of the I/O interface **432**, optimum performance can be achieved by each. Recoupling between the CPU **70** and the interface **432** is accomplished with handshake signals on lines **436**, with data/addresses passing on bus **90**, **136**.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

Claims **3**–**5** and **8** are cancelled.

Claims **1**, **6** and **10** are determined to be patentable as amended.

Claims **2**, **7** and **9**, dependent on an amended claim, are determined to be patentable.

New claims **11**–**16** are added and determined to be patentable.

1. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface*, wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.*

6. A microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an *off-chip* external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an *off-chip* external clock, independent of said oscillator, connected to said input/output interface wherein said *off-chip* external clock is operative at a frequency independent of a clock frequency of said oscillator *and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator*.

10. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an **[**on chip**]** *on-chip* input/output interface between said central processing unit and an *off-chip* external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an *off-chip* external clock wherein said *off-chip* external clock is operative at a frequency independent of a clock frequency of said variable speed clock *and wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock.*

11. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein said central processing unit operates asynchronously to said input/output interface.

12. The microprocessor system of claim 11, in which said second clock is a fixed frequency clock.

13. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;

an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and further wherein said central processing unit operates asynchronously to said input/output interface.

14. The microprocessor system of claim 13 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

15. The microprocessor system of claim 13 wherein said oscillator comprises a ring oscillator.

16. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock, wherein said central processing unit operates asychronously to said input/output interface.

* * * * *

US005809336C2

(12) **EX PARTE REEXAMINATION CERTIFICATE** (7887th)

United States Patent
Moore et al.

(10) **Number: US 5,809,336 C2**
(45) **Certificate Issued: Nov. 23, 2010**

(54) **HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK**

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Reexamination Request:
No. 90/009,457, Aug. 24, 2009

Reexamination Certificate for:

Patent No.:	**5,809,336**
Issued:	**Sep. 15, 1998**
Appl. No.:	**08/484,918**
Filed:	**Jun. 7, 1995**

Reexamination Certificate C1 5,809,336 issued Dec. 15, 2009

Certificate of Correction issued May 22, 2007.

Related U.S. Application Data

(62) Division of application No. 07/389,334, filed on Aug. 3, 1989, now Pat. No. 5,440,749.

(51) **Int. Cl.**

G06F 7/76	(2006.01)
G06F 7/48	(2006.01)
G06F 12/08	(2006.01)
G06F 7/78	(2006.01)
G06F 9/30	(2006.01)
G06F 9/32	(2006.01)
G06F 15/76	(2006.01)
G06F 15/78	(2006.01)
G06F 7/52	(2006.01)
G06F 9/38	(2006.01)
G06F 7/58	(2006.01)

(52) **U.S. Cl.** **710/25**; 711/E12.02; 712/E9.016; 712/E9.028; 712/E9.046; 712/E9.055; 712/E9.057; 712/E9.058; 712/E9.062; 712/E9.078; 712/E9.08; 712/E9.081

(58) **Field of Classification Search** ..... None
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,348,743	A	9/1982	Dozier
4,691,124	A	9/1987	Ledzius et al.
4,766,567	A	8/1988	Kato
4,853,841	A	8/1989	Richter
4,931,748	A	6/1990	McDermott et al.
5,809,336	A	9/1998	Moore et al.

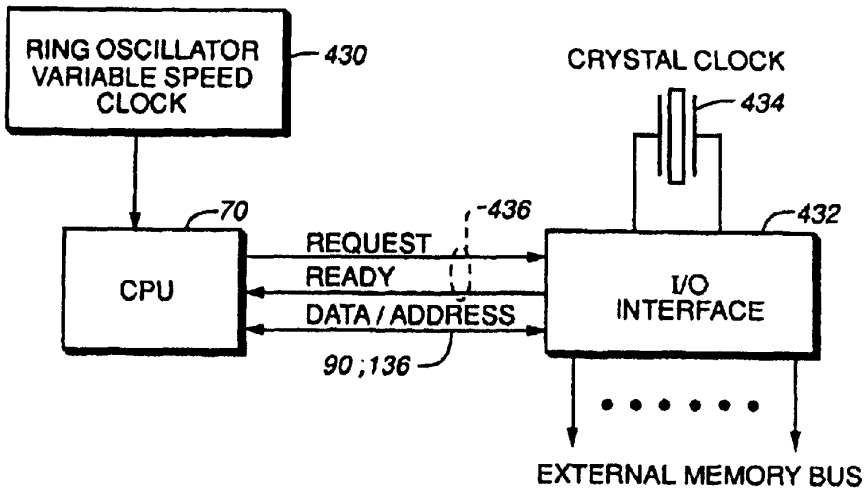
OTHER PUBLICATIONS

U.S. Patent No. 5,809,336, as certified by Ex Parte Reexamination Certificate (7235th) U.S. 5,809,336 C1, issued Dec. 15, 2009, 51 pages.
In re Recreative Technologies Corp., 83 F.3d 1394, 38 USPQ 2.d 1776 (Fed. Cir. 1996), 6 pages.

Primary Examiner—B. James Peikari

(57) **ABSTRACT**

A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and the ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.



EX PARTE
REEXAMINATION CERTIFICATE
ISSUED UNDER 35 U.S.C. 307

NO AMENDMENTS HAVE BEEN MADE TO THE PATENT

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claims **1**, **2**, **6**, **7** and **9-16** is confirmed.

Claims **3-5** and **8** were previously cancelled.

* * * * *

ADRMOP,AO279,APPEAL,CLOSED,PROTO,ProSe,REFDIS,REFSET-NC,RELATE

U.S. District Court
California Northern District (San Francisco)
CIVIL DOCKET FOR CASE #: 3:12-cv-03865-VC

Technology Properties Limited LLC et al v. Huawei Technologies Co., Ltd. et al
Assigned to: Hon. Vince Chhabria
Referred to: Magistrate Judge Paul Singh Grewal
Magistrate Judge Nathanael M. Cousins (Settlement)
Relate Case Cases: 3:12-cv-03876-VC
3:12-cv-03881-VC
3:12-cv-03880-VC
3:12-cv-03870-VC
5:08-cv-00882-PSG
3:12-cv-03877-VC
3:12-cv-03879-VC
Case in other court: Federal Circuit, 16-01306
Cause: 35:145 Patent Infringement

Date Filed: 07/24/2012
Date Terminated: 11/13/2015
Jury Demand: Plaintiff
Nature of Suit: 830 Patent
Jurisdiction: Federal Question

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Vinh Huy Pham
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Date Filed	#	Docket Text

07/24/2012	1	COMPLAINT FOR PATENT INFRINGEMENT: DEMAND FOR JURY TRIAL; against Huawei North America, Huawei Technologies Co., Ltd. (Filing fee $ 350.00, receipt number 54611012265.). Filed byTechnology Properties Limited LLC, Phoenix Digital Solutions LLC, Patriot Scientific Corporation. (aaa, COURT STAFF) (Filed on 7/24/2012) (Additional attachment(s) added on 8/9/2012: # 1 Civil Cover Sheet) (aaa, COURT STAFF). (Entered: 07/27/2012)
07/24/2012	2	ADR SCHEDULING ORDER: Case Management Statement due by 10/17/2012. Case Management Conference set for 10/24/2012 10:00 AM. Signed by Magistrate Judge Nathanael M. Cousins on 7/24/12. (Attachments: # 1 NC Standing Order, # 2 Standing Order)(aaa, COURT STAFF) (Filed on 7/24/2012) (Entered: 07/27/2012)
07/24/2012	3	Summons Issued as to Huawei Technologies Co., Ltd. (aaa, COURT STAFF) (Filed on 7/24/2012) (Entered: 07/27/2012)
07/24/2012	4	Summons Issued as to Huawei North America. (aaa, COURT STAFF) (Filed on 7/24/2012) (Entered: 07/27/2012)
07/24/2012	5	REPORT on the filing or determination of an action regarding:**PATENT INFRINGEMENT** (cc: form mailed to register). (aaa, COURT STAFF) (Filed on 7/24/2012) (Entered: 07/27/2012)
08/06/2012	6	CLERKS NOTICE to Plaintiff(s) Attorney(s) via e-mail or U.S. mail re: Failure to E-File/E-Mail re 1 Complaint & in a separate pdf attachment the Civil Cover Sheet and/or Failure to Register as an E-Filer (aaa, COURT STAFF) (Filed on 8/6/2012) (Entered: 08/06/2012)
09/20/2012	7	MOTION to Stay *District Court Litigation Pending Resolution of Proceeding Pending Before the U.S. International Trade Commission* filed by Huawei Technologies Co., Ltd.. Motion Hearing set for 10/31/2012 01:00 PM in Courtroom A, 15th Floor, San Francisco before Magistrate Judge Nathanael M. Cousins. Responses due by 10/4/2012. Replies due by 10/11/2012. (Attachments: # 1 Proposed Order)(Hector, Morgan) (Filed on 9/20/2012) (Entered: 09/20/2012)
09/20/2012	8	Declaration of Morgan L. Hector in Support of 7 MOTION to Stay *District Court Litigation Pending Resolution of Proceeding Pending Before the U.S. International Trade Commission* filed byHuawei Technologies Co., Ltd.. (Attachments: # 1 Exhibit 1, # 2 Exhibit 2, # 3 Exhibit 3)(Related document(s) 7) (Hector, Morgan) (Filed on 9/20/2012) (Entered: 09/20/2012)
09/21/2012	9	CLERKS NOTICE REGARDING Consent/Declination to Proceed Before United States Magistrate Judge. Parties shall file their form no later than 9/28/2012. (lmh, COURT STAFF) (Filed on 9/21/2012) (Entered: 09/21/2012)
09/25/2012	10	CONSENT/DECLINATION to Proceed Before a US Magistrate Judge by Huawei Technologies Co., Ltd... (Hector, Morgan) (Filed on 9/25/2012) (Entered: 09/25/2012)
09/26/2012	11	CLERK'S NOTICE of Impending Reassignment to U.S. District Judge. (lmh, COURT STAFF) (Filed on 9/26/2012) (Entered: 09/26/2012)

09/27/2012	12	ORDER, Case reassigned to Hon. Phyllis J. Hamilton. Magistrate Judge Nathanael M. Cousins no longer assigned to the case.. Signed by Executive Committee on 9/27/12. (ha, COURT STAFF) (Filed on 9/27/2012) (Entered: 09/27/2012)
10/02/2012	13	STIPULATION WITH PROPOSED ORDER *Staying Action Pursuant to 28 U.S.C. 1659* filed by Huawei Technologies Co., Ltd.. (Hector, Morgan) (Filed on 10/2/2012) (Entered: 10/02/2012)
10/04/2012	14	STIPULATION AND ORDER STAYING ACTION by Hon. Phyllis J. Hamilton granting 13 Stipulation.(nah, COURT STAFF) (Filed on 10/4/2012) (Entered: 10/04/2012)
10/10/2012	15	ACKNOWLEDGEMENT OF SERVICE Executed as to 1 Complaint, *Summons, et al.* Acknowledgement filed by Patriot Scientific Corporation, Phoenix Digital Solutions LLC, Technology Properties Limited LLC. (Breit, Michelle) (Filed on 10/10/2012) (Entered: 10/10/2012)
10/15/2014	16	**ORDER RELATING CASES Signed by Judge Paul S. Grewal on October 15, 2014. (psglc1S, COURT STAFF) (Filed on 10/15/2014) (Entered: 10/15/2014)**
10/17/2014	17	**ORDER REASSIGNING AND RELATING CASES, AND ORDER REFERRING CASE to Magistrate Judge Paul Grewal for Report and Recommendation/PRETRIAL MANAGEMENT. Signed by Judge Vince Chhabria on 10/17/2014. (knm, COURT STAFF) (Filed on 10/17/2014) (Entered: 10/23/2014)**
10/23/2014		Case reassigned to Judge Hon. Vince Chhabria. Judge Hon. Phyllis J. Hamilton no longer assigned to the case. (sv, COURT STAFF) (Filed on 10/23/2014) (Entered: 10/23/2014)
10/23/2014	18	NOTICE of Appearance by William Frederick Abrams *NOTICE OF APPEARANCE OF WILLIAM F. ABRAMS ON BEHALF OF DEFENDANT HUAWEI TECHNOLOGIES, CO., LTD.* (Abrams, William) (Filed on 10/23/2014) (Entered: 10/23/2014)
10/23/2014	19	MOTION for leave to appear in Pro Hac Vice *APPLICATION FOR ADMISSION OF ATTORNEY PRO HAC VICE (TIMOTHY BICKHAM)* (Filing fee $ 305, receipt number 0971-9019529.) filed by Huawei Technologies Co., Ltd.. (Attachments: # 1 Declaration Certificate of Good Standing)(Bickham, Timothy) (Filed on 10/23/2014) (Entered: 10/23/2014)
10/24/2014		CASE REFERRED to Magistrate Judge Paul Singh Grewal for Discovery (ahm, COURT STAFF) (Filed on 10/24/2014) (Entered: 10/24/2014)
10/24/2014	20	CLERK'S NOTICE SETTING CASE MANAGEMENT CONFERENCE FOLLOWING REASSIGNMENT: Case Management Conference set for 11/18/2014 at 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul S. Grewal. Case Management Statement due by 11/11/2014. ***This is a text only docket entry, there is no document associated with this notice.*** (ofr, COURT STAFF) (Filed on 10/24/2014) (Entered: 10/24/2014)

10/24/2014	21	**Order by Hon. Vince Chhabria granting 19 Motion for Pro Hac Vice- Bickham.(knm, COURT STAFF) (Filed on 10/24/2014) (Entered: 10/24/2014)**
11/11/2014	22	NOTICE of Appearance by Vinh Huy Pham *on Behalf of Phoenix Digital Solutions and Technology Properties Limited LLC* (Pham, Vinh) (Filed on 11/11/2014) (Entered: 11/11/2014)
11/11/2014	23	Certificate of Interested Entities by Patriot Scientific Corporation, Phoenix Digital Solutions LLC, Technology Properties Limited LLC (Pham, Vinh) (Filed on 11/11/2014) (Entered: 11/11/2014)
11/11/2014	24	NOTICE of Change In Counsel by Morgan Linscott Hector *Regarding Withdrawal of Attorney Huan-Yi Lin For Huawei Technologies Co., Ltd. and Request For Removal From ECF Service List* (Hector, Morgan) (Filed on 11/11/2014) (Entered: 11/11/2014)
11/11/2014	25	JOINT CASE MANAGEMENT STATEMENT filed by Patriot Scientific Corporation, Phoenix Digital Solutions LLC, Technology Properties Limited LLC. (Otteson, James) (Filed on 11/11/2014) (Entered: 11/11/2014)
11/12/2014	26	NOTICE of Appearance by David L. Lansky *on behalf of PHOENIX DIGITAL SOLUTIONS LLC and TECHNOLOGY PROPERTIES LIMITED* (Lansky, David) (Filed on 11/12/2014) (Entered: 11/12/2014)
11/12/2014	27	NOTICE of Appearance by Philip William Marsh (Marsh, Philip) (Filed on 11/12/2014) (Entered: 11/12/2014)
11/12/2014	28	FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT against Huawei Technologies Co., Ltd., Futurewei Technologies, Inc., Huawei Device Co., Ltd., Huawei Device USA Inc., Huawei Technologies USA Inc.. Filed byTechnology Properties Limited LLC, Phoenix Digital Solutions LLC, Patriot Scientific Corporation. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C)(Otteson, James) (Filed on 11/12/2014) Modified on 11/13/2014 (farS, COURT STAFF). (Entered: 11/12/2014)
11/12/2014	29	Proposed Summons. (Otteson, James) (Filed on 11/12/2014) (Entered: 11/12/2014)
11/12/2014	30	Proposed Summons. (Otteson, James) (Filed on 11/12/2014) (Entered: 11/12/2014)
11/12/2014	31	Proposed Summons. (Otteson, James) (Filed on 11/12/2014) (Entered: 11/12/2014)
11/12/2014	32	Proposed Summons. (Otteson, James) (Filed on 11/12/2014) (Entered: 11/12/2014)
11/12/2014	33	NOTICE of Appearance by Thomas T. Carmack (Carmack, Thomas) (Filed on 11/12/2014) (Entered: 11/12/2014)
11/13/2014	34	Summons Issued as to Futurewei Technologies, Inc., Huawei Device Co., Ltd., Huawei Device USA Inc., Huawei Technologies USA Inc.. (Attachments: # 1 summons, # 2 summons, # 3 summons)(farS, COURT STAFF) (Filed on 11/13/2014) (Entered: 11/13/2014)

11/17/2014	35	CLERK'S NOTICE RESETTING TIME ON NOVEMBER 18, 2014 CASE MANAGEMENT CONFERENCE: 11/18/2014 10:00 AM Case Management Conference is reset to 1:00 PM (SPECIAL SET) in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul S. Grewal. ***This is a text only docket entry, there is no document associated with this notice.*** (ofr, COURT STAFF) (Filed on 11/17/2014) (Entered: 11/17/2014)
11/17/2014	36	ACKNOWLEDGEMENT OF SERVICE Executed as to 28 Amended Complaint, Acknowledgement filed by Phoenix Digital Solutions LLC, Technology Properties Limited LLC. (Pham, Vinh) (Filed on 11/17/2014) (Entered: 11/17/2014)
11/18/2014	37	**Minute Entry for proceedings held before Magistrate Judge Paul Singh Grewal: Case Management Conference held on 11/18/2014. The court denies Defendant LG's Motion to Stay. The court will proceed to issue a Case Management Scheduling Order. (Date Filed: 11/18/2014) FTR Time (FTR: (1:01 to 1:28) Plaintiff Attorney(s) present: Jim Otteson. Also present: Charles Hoge, telephonically. Defendant Attorney(s): Mark Fowler, Mike Bettinger, William Abrams, Bill Frankel, Joshua Masur, Shelley Mack, Matthew Brigham & David Eiseman. This is a text only Minute Entry (ofr, COURT STAFF) (Entered: 11/18/2014)**
11/20/2014	38	**CASE MANAGEMENT ORDER Signed by Judge Paul S. Grewal on November 20, 2014. (psglc1S, COURT STAFF) (Filed on 11/20/2014) (Entered: 11/20/2014)**
11/20/2014		Set/Reset Hearing: Tutorial Hearing set for 11/4/2015 at 10:00 AM in Courtroom 5, 4th Floor, San Jose. Claims Construction and Summary Judgment Hearing set for 11/12/2015 at 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. (ofr, COURT STAFF) (Filed on 11/20/2014) (Entered: 11/21/2014)
12/18/2014	39	Certificate of Interested Entities by Futurewei Technologies, Inc., Huawei Device Co., Ltd., Huawei Device USA Inc., Huawei Technologies Co., Ltd., Huawei Technologies USA Inc. (Bickham, Timothy) (Filed on 12/18/2014) (Entered: 12/18/2014)
12/18/2014	40	*HUAWEI TECHNOLOGIES CO., LTD., HUAWEI DEVICE CO., LTD., HUAWEI DEVICE USA INC., FUTUREWEI TECHNOLOGIES, INC., and HUAWEI TECHNOLOGIES USA INC. ("HUAWEI DEFENDANTS')* ANSWER to 28 Amended Complaint *and*, COUNTERCLAIM against Patriot Scientific Corporation, Phoenix Digital Solutions LLC, Technology Properties Limited LLC byFuturewei Technologies, Inc., Huawei Technologies Co., Ltd., Huawei Technologies USA Inc., Huawei Device USA Inc., Huawei Device Co., Ltd.. (Bickham, Timothy) (Filed on 12/18/2014) Modified on 12/19/2014 (aaaS, COURT STAFF). (Entered: 12/18/2014)
01/12/2015	41	ANSWER TO COUNTERCLAIM 40 Answer to Amended Complaint,,, Counterclaim,, byPatriot Scientific Corporation, Phoenix Digital Solutions LLC, Technology Properties Limited LLC. (Otteson, James) (Filed on 1/12/2015) (Entered: 01/12/2015)

01/14/2015	42	Transcript of Proceedings of the official sound recording held on 11/18/14, before Magistrate Judge Paul S. Grewal. FTR/Transcriber Echo Reporting, Inc., Telephone number (858) 453-7590.;echoreporting@yahoo.com. Tape Number: FTR 1:01 - 1:28. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerks Office public terminal or may be purchased through the Court Reporter/Transcriber until the deadline for the Release of Transcript Restriction.After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. (Re (42 in 3:12-cv-03880-VC) Transcript Order) Redaction Request due 2/4/2015. Redacted Transcript Deadline set for 2/17/2015. Release of Transcript Restriction set for 4/14/2015. (tgb, COURT STAFF) (Filed on 1/14/2015) (Entered: 01/14/2015)
02/11/2015	43	**ORDER GRANTING-AS-MODIFIED UNOPPOSED MOTION TO MODIFY CASE SCHEDULE by Judge Paul S. Grewal granting-as-modified 45 , 46 in Case No. 3:12-cv-03880-VC. (psglc1S, COURT STAFF) (Filed on 2/11/2015) (Entered: 02/11/2015)**
02/11/2015		Set/Reset Hearing: 11/4/2015 Tutorial reset to 2/19/2016 at 10:00 AM in Courtroom 5, 4th Floor, San Jose. 11/12/2015 Claims Construction and Summary Judgment Hearing reset to 2/26/2016 at 10:00 AM. (ofr, COURT STAFF) (Filed on 2/11/2015) (Entered: 02/12/2015)
04/01/2015	44	**ERRONEOUSLY E-FILED, DISREGARD** NOTICE of Change In Counsel by Thomas T. Carmack (Carmack, Thomas) (Filed on 4/1/2015) Modified on 4/1/2015 (farS, COURT STAFF). (Entered: 04/01/2015)
04/01/2015	45	NOTICE of Change In Counsel by James Carl Otteson (Otteson, James) (Filed on 4/1/2015) (Entered: 04/01/2015)
04/10/2015	46	Joint MOTION for Judgment on the Pleadings filed by Futurewei Technologies, Inc., Huawei Device Co., Ltd., Huawei Device USA Inc., Huawei Technologies Co., Ltd., Huawei Technologies USA Inc.. Motion Hearing set for 5/19/2015 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 4/24/2015. Replies due by 5/1/2015. (Attachments: # 1 Proposed Order)(Bickham, Timothy) (Filed on 4/10/2015) (Entered: 04/10/2015)
04/15/2015	47	NOTICE of Appearance by Christopher D. Banys *on Behalf of Phoenix Digital Solutions LLC* (Banys, Christopher) (Filed on 4/15/2015) (Entered: 04/15/2015)
04/15/2015	48	NOTICE of Appearance by Jennifer Lu Gilbert *on Behalf of Phoenix Digital Solutions LLC* (Gilbert, Jennifer) (Filed on 4/15/2015) (Entered: 04/15/2015)
04/15/2015	49	MOTION for leave to appear in Pro Hac Vice *for Brent Nelson Bumgardner on Behalf of Phoenix Digital Solutions LLC* (Filing fee $ 305, receipt number 0971-9445028.) filed by Phoenix Digital Solutions LLC. (Attachments: # 1 Certificate of Good Standing)(Bumgardner, Brent) (Filed on 4/15/2015) (Entered: 04/15/2015)
04/15/2015	50	

		MOTION for leave to appear in Pro Hac Vice *for Berry J. Bumgardner on Behalf of Phoenix Digital Solutions LLC* (Filing fee $ 305, receipt number 0971-9445043.) filed by Phoenix Digital Solutions LLC. (Attachments: # 1 Certificate of Good Standing)(Bumgardner, Barry) (Filed on 4/15/2015) (Entered: 04/15/2015)
04/15/2015	51	MOTION for leave to appear in Pro Hac Vice *for Edward R. Nelson III on Behalf of Phoenix Digital Solutions LLC* (Filing fee $ 305, receipt number 0971-9445098.) filed by Phoenix Digital Solutions LLC. (Attachments: # 1 Certificate of Good Standing)(Nelson, Edward) (Filed on 4/15/2015) (Entered: 04/15/2015)
04/15/2015	52	NOTICE of Change In Counsel by James Carl Otteson *Notice of Change in Counsel For Plaintiff Phoenix Digital Solutions, LLC* (Otteson, James) (Filed on 4/15/2015) (Entered: 04/15/2015)
04/15/2015	53	MOTION for leave to appear in Pro Hac Vice *for Thomas Christopher Cecil on Behalf of Phoenix Digital Solutions LLC* (Filing fee $ 305, receipt number 0971-9445331.) filed by Phoenix Digital Solutions LLC. (Attachments: # 1 Certificate of Good Standing)(Cecil, Thomas) (Filed on 4/15/2015) (Entered: 04/15/2015)
04/16/2015	54	**ORDER GRANTING MOTION FOR PRO HAC VICE by Magistrate Judge Paul Singh Grewal granting 49 . (psglc1S, COURT STAFF) (Filed on 4/16/2015) (Entered: 04/16/2015)**
04/16/2015	55	**ORDER GRANTING MOTION FOR PRO HAC VICE by Magistrate Judge Paul Singh Grewal granting 50 . (psglc1S, COURT STAFF) (Filed on 4/16/2015) (Entered: 04/16/2015)**
04/16/2015	56	**ORDER GRANTING MOTION FOR PRO HAC VICE by Magistrate Judge Paul Singh Grewal granting 51 . (psglc1S, COURT STAFF) (Filed on 4/16/2015) (Entered: 04/16/2015)**
04/16/2015	57	**ORDER GRANTING MOTION FOR PRO HAC VICE by Magistrate Judge Paul Singh Grewal granting 53 . (psglc1S, COURT STAFF) (Filed on 4/16/2015) (Entered: 04/16/2015)**
04/16/2015	58	NOTICE of Appearance by Michael William Stebbins (Stebbins, Michael) (Filed on 4/16/2015) (Entered: 04/16/2015)
04/16/2015	59	NOTICE of Change In Counsel by James Carl Otteson *Notice of Change in Counsel For Plaintiff Technology Properties Limited, LLC* (Otteson, James) (Filed on 4/16/2015) (Entered: 04/16/2015)
04/17/2015	60	NOTICE of Appearance by William L. Bretschneider (Bretschneider, William) (Filed on 4/17/2015) (Entered: 04/17/2015)
04/22/2015	61	**ORDER GRANTING DEFENDANTS' UNOPPOSED MOTION FOR TRANSMISSION OF THE ITC RECORD TO THE DISTRICT COURT by Judge Paul S. Grewal; granting (48) Motion in case 3:12-cv-03880-VC. (psglc1S, COURT STAFF) (Filed on 4/22/2015) (Entered: 04/22/2015)**
04/24/2015	62	

		RESPONSE (re 46 Joint MOTION for Judgment on the Pleadings) *Plaintiffs' Opposition to Defendants' Motion for Judgment on the Pleadings* filed byPhoenix Digital Solutions LLC. (Attachments: # 1 Declaration Declaration of Thomas C. Cecil, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Proposed Order)(Bumgardner, Barry) (Filed on 4/24/2015) (Entered: 04/24/2015)
05/01/2015	63	REPLY (re 46 Joint MOTION for Judgment on the Pleadings) *DEFENDANTS' REPLY BRIEF IN SUPPORT OF MOTION FOR JUDGMENT ON THE PLEADINGS* filed byFuturewei Technologies, Inc., Huawei Device Co., Ltd., Huawei Device USA Inc., Huawei Technologies Co., Ltd., Huawei Technologies USA Inc.. (Bickham, Timothy) (Filed on 5/1/2015) (Entered: 05/01/2015)
05/04/2015	64	NOTICE of Appearance by Richard Cheng-hong Lin *On Behalf of Phoenix Digital Solutions LLC* (Lin, Richard) (Filed on 5/4/2015) (Entered: 05/04/2015)
05/04/2015	65	NOTICE of Appearance by Christopher J Judge *On Behalf of Phoenix Digital Solutions LLC* (Judge, Christopher) (Filed on 5/4/2015) (Entered: 05/04/2015)
05/18/2015	66	NOTICE of Appearance by Michael E Flynn-O'Brien *NOTICE OF APPEARANCE OF MICHAEL E. FLYNN-OBRIEN ON BEHALF OF DEFENDANTS HUAWEI TECHNOLOGIES CO., LTD., HUAWEI DEVICE CO., LTD., HUAWEI DEVICE USA INC., FUTUREWEI TECHNOLOGIES, INC., AND HUAWEI TECHNOLOGIES USA INC.* (Flynn-O'Brien, Michael) (Filed on 5/18/2015) (Entered: 05/18/2015)
05/19/2015	67	MOTION for leave to appear in Pro Hac Vice *on Behalf of Phoenix Digital Solutions* (Filing fee $ 305, receipt number 0971-9531066.) filed by Phoenix Digital Solutions LLC. (Attachments: # 1 Certificate of Good Standing) (Greskowiak McNulty, Stacy) (Filed on 5/19/2015) (Entered: 05/19/2015)
05/19/2015	68	**Minute Entry for proceedings held before Magistrate Judge Paul Singh Grewal: Motion Hearing held on 5/19/2015 re Defendants' Motion for Judgment on the Pleadings (ECF Nos. 60 in CV12-03863, 46 in CV12-03865, 51 in CV12-03876, 31 in CV12-03877 and 54 in CV12-03880).** **The court takes matters under submission; written order to be issued.** **Court Reporter Name: Summer Fisher. Time in Court: 10:26 to 10:46. Plaintiff Attorney(s) present: Christopher Banys, Barry Bumgardner, Charles Hoge, Thomas Cecil and William Bretschneider. Defendant Attorney(s) present: Hersh Mehta, Wasif Qureshi, Michael Flynn-O'Brien and Aaron Wainscoat. This is a text only Minute Entry. (ofr, COURT STAFF) (Date Filed: 5/19/2015) (Entered: 05/19/2015)**
05/19/2015	69	**ORDER GRANTING APPLICATION FOR ADMISSION OF ATTORNEY STACIE GRESKOWIAK MCNULTY PRO HAC VICE, granting 67 . Signed by Judge Paul S. Grewal on 5/19/2015. (ofr, COURT STAFF) (Filed on 5/19/2015) (Entered: 05/19/2015)**
06/09/2015	70	Letter from Plaintiffs Regarding Discovery . (Attachments: # 1 Exhibit A) (Banys, Christopher) (Filed on 6/9/2015) (Entered: 06/09/2015)

06/12/2015	71	Letter from Defendants In Response To Plaintiffs' Letter of June 9, 2015 re Discovery . (Bickham, Timothy) (Filed on 6/12/2015) (Entered: 06/12/2015)
06/17/2015	72	**ORDER DENYING REQUEST FOR USE OF LETTER BRIEFS FOR DISCOVERY. Signed by Judge Paul S. Grewal on June 17, 2015. (psglc1S, COURT STAFF) (Filed on 6/17/2015) (Entered: 06/17/2015)**
06/19/2015	73	MOTION for leave to appear in Pro Hac Vice (Filing fee $ 305, receipt number 0971-9613129.) filed by Phoenix Digital Solutions LLC. (Attachments: # 1 Certificate/Proof of Service Certificate of Good Standing) (Albritton, Eric) (Filed on 6/19/2015) (Entered: 06/19/2015)
06/19/2015	74	**ORDER GRANTING MOTION FOR PRO HAC VICE by Magistrate Judge Paul Singh Grewal granting 73 . (psglc1S, COURT STAFF) (Filed on 6/19/2015) (Entered: 06/19/2015)**
06/23/2015	75	CLAIM CONSTRUCTION STATEMENT *Patent Local Rule 4-3 Joint Claim Construction and Prehearing Statement* filed by Phoenix Digital Solutions LLC. (Attachments: # 1 Exhibit A, # 2 Exhibit B, # 3 Exhibit C, # 4 Exhibit D) (Bumgardner, Barry) (Filed on 6/23/2015) (Entered: 06/23/2015)
06/23/2015	76	MOTION to Quash *Plaintiffs' Motion to Limit Defendants' Subpoenas to Third Party Charles Moore or Alternatively for a Protective Order* filed by Phoenix Digital Solutions LLC. Motion Hearing set for 8/11/2015 10:00 AM in Courtroom 5, 4th Floor, San Jose before Magistrate Judge Paul Singh Grewal. Responses due by 7/7/2015. Replies due by 7/14/2015. (Attachments: # 1 Declaration of Barry J. Bumgardner in Support of Plaintiffs' Motion to Limit Defendants' Subpoenas to Third Party Charles Moore or Alternatively for a Protective Order, # 2 Exhibit 1, # 3 Exhibit 2, # 4 Proposed Order) (Bumgardner, Barry) (Filed on 6/23/2015) (Entered: 06/23/2015)
06/24/2015	77	MOTION for leave to appear in Pro Hac Vice *for John Murphy on Behalf of Plaintiff Phoenix Digital Solutions LLC* (Filing fee $ 305, receipt number 0971-9626097.) filed by Phoenix Digital Solutions LLC. (Attachments: # 1 Certificate of Good Standing)(Murphy, John) (Filed on 6/24/2015) (Entered: 06/24/2015)
06/25/2015	78	**ORDER GRANTING APPLICATION FOR ADMISSION OF ATTORNEY JOHN PAUL MURPHY PRO HAC VICE by Judge Paul S. Grewal, granting 77 . (ofr, COURT STAFF) (Filed on 6/25/2015) (Entered: 06/25/2015)**
06/25/2015	79	**STIPULATED PROTECTIVE ORDER by Judge Paul S. Grewal. Signed on 6/25/2015. (ofr, COURT STAFF) (Filed on 6/25/2015) (Entered: 06/25/2015)**
07/07/2015	80	RESPONSE (re 76 MOTION to Quash *Plaintiffs' Motion to Limit Defendants' Subpoenas to Third Party Charles Moore or Alternatively for a Protective Order*) filed byHuawei North America, Huawei Technologies Co., Ltd.. (Attachments: # 1 Declaration of Wasif Qureshi, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Proposed Order)(Bickham, Timothy) (Filed on 7/7/2015) (Entered: 07/07/2015)

07/08/2015	81	STIPULATION WITH PROPOSED ORDER *Stipulated Supplemental Protective Order Between Non-Party Qualcomm Incorporated, Plaintiffs and Defendants* filed by Phoenix Digital Solutions LLC. (Bumgardner, Barry) (Filed on 7/8/2015) (Entered: 07/08/2015)
07/08/2015	82	**ORDER GRANTING STIPULATED PROTECTIVE ORDER BETWEEN NON-PARTY QUALCOMM INCORPORATED, PLAINTIFFS AND DEFENDANTS by Magistrate Judge Paul Singh Grewal granting 81 . (psglc1S, COURT STAFF) (Filed on 7/8/2015) (Entered: 07/08/2015)**
07/09/2015	83	Letter from Plaintiffs Regarding Plaintiffs Proposed Revisions to Current Case Schedule. (Bumgardner, Barry) (Filed on 7/9/2015) Modified on 7/9/2015 (farS, COURT STAFF). (Entered: 07/09/2015)
07/09/2015	84	Letter from Defendants Regarding Proposed Revisions To Current Case Schedule . (Bickham, Timothy) (Filed on 7/9/2015) (Entered: 07/09/2015)
07/14/2015	85	**SECOND AMENDED CASE MANAGEMENT ORDER. Signed by Judge Paul S. Grewal on July 14, 2015. (psglc1S, COURT STAFF) (Filed on 7/14/2015) (Entered: 07/14/2015)**
07/14/2015		Resetting Hearings: 2/19/2016 Tutorial Hearing is advanced to 9/18/2015 at 10:00 AM in Courtroom 5, 4th Floor, San Jose. 2/26/2016 Markman hearing is advanced to 9/18/2015 at 10:00 AM in Courtroom 5, 4th Floor, San Jose. 2/26/2016 Summary Judgment Hearing is reset to 3/22/2016 at 10:00 AM in Courtroom 5, 4th Floor, San Jose. (ofr, COURT STAFF) (Filed on 7/14/2015) (Entered: 07/15/2015)
07/27/2015	86	STIPULATION *of Dismissal of U.S. Patent Nos. 5,440,749 and 5,530,890* filed by Phoenix Digital Solutions LLC. (Bumgardner, Barry) (Filed on 7/27/2015) (Entered: 07/27/2015)
07/28/2015	87	**ORDER DENYING AS MOOT 46 Motion for Judgment on the Pleadings entered by Magistrate Judge Paul Singh Grewal. See Docket No. 86. (This is a text-only entry generated by the court. There is no document associated with this entry.) (Entered: 07/28/2015)**
07/29/2015	88	Notice of Withdrawal of Motion *Unopposed Motion to Withdraw Without Prejudice Plaintiffs' Motion to Quash or Limit Defendants' Subpoenas to Third PArty Charles Moore or, Alternatively, for a Protective Order* (Bumgardner, Barry) (Filed on 7/29/2015) (Entered: 07/29/2015)
08/04/2015	89	CLAIM CONSTRUCTION STATEMENT *Brief* filed by Phoenix Digital Solutions LLC. (Attachments: # 1 Declaration of Barry J. Bumgardner, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F - Part 1, # 8 Exhibit F - Part 2, # 9 Exhibit G, # 10 Exhibit H, # 11 Exhibit I, # 12 Exhibit J, # 13 Exhibit K, # 14 Exhibit L, # 15 Exhibit M, # 16 Exhibit N, # 17 Exhibit O, # 18 Exhibit P, # 19 Exhibit Q, # 20 Exhibit R) (Bumgardner, Barry) (Filed on 8/4/2015) (Entered: 08/04/2015)
08/04/2015	90	CLAIM CONSTRUCTION STATEMENT *DEFENDANTS' OPENING CLAIM CONSTRUCTION BRIEF* filed by Futurewei Technologies, Inc.,

		Huawei Device Co., Ltd., Huawei Device USA Inc., Huawei Technologies Co., Ltd., Huawei Technologies USA Inc.. (Attachments: # 1 Declaration Wainscoat Declaration ISO Defendants Opening Claim Construction Brief, # 2 Exhibit Exhibit A - Part 1, # 3 Exhibit Exhibit A - Part 2, # 4 Exhibit Exhibit A - Part 3, # 5 Exhibit Exhibit B, # 6 Exhibit Exhibit C, # 7 Exhibit Exhibit D, # 8 Exhibit Exhibit E, # 9 Exhibit Exhibit F, # 10 Exhibit Exhibit G, # 11 Exhibit Exhibit H, # 12 Exhibit Exhibit I, # 13 Exhibit Exhibit J, # 14 Exhibit Exhibit K, # 15 Exhibit Exhibit L, # 16 Exhibit Exhibit M, # 17 Exhibit Exhibit N, # 18 Exhibit Exhibit O, # 19 Exhibit Exhibit P, # 20 Exhibit Exhibit Q - Part 1, # 21 Exhibit Exhibit Q - Part 2, # 22 Exhibit Exhibit Q - Part 3, # 23 Exhibit Exhibit Q- Part 4)(Bickham, Timothy) (Filed on 8/4/2015) (Entered: 08/04/2015)
08/10/2015	91	NOTICE of Change of Address by Michael E Flynn-O'Brien *NOTICE OF CHANGE OF FIRM ADDRESS* (Flynn-O'Brien, Michael) (Filed on 8/10/2015) (Entered: 08/10/2015)
08/18/2015	92	CLAIM CONSTRUCTION STATEMENT *Plaintiffs' Responsive Claim Construction Brief* filed by Phoenix Digital Solutions LLC. (Attachments: # 1 Declaration (Supplemental) Declaration of Barry J. Bumgardner in Support of Plaintiffs' Responsive Claim Construction Brief, # 2 Exhibit S, # 3 Exhibit T, # 4 Exhibit U, # 5 Exhibit V, # 6 Exhibit W)(Bumgardner, Barry) (Filed on 8/18/2015) (Entered: 08/18/2015)
08/18/2015	93	CLAIM CONSTRUCTION STATEMENT *Defendants' Responsive Claim Construction Brief* filed by Futurewei Technologies, Inc., Huawei Device Co., Ltd., Huawei Device USA Inc., Huawei Technologies Co., Ltd., Huawei Technologies USA Inc.. (Attachments: # 1 Supplement Declaration of Aaron Wainscoat In Support of Defendants' Responsive Claim Construction Brief, # 2 Exhibit R, # 3 Exhibit S, # 4 Exhibit T, # 5 Exhibit U)(Bickham, Timothy) (Filed on 8/18/2015) (Entered: 08/18/2015)
09/01/2015	94	NOTICE by Futurewei Technologies, Inc., Huawei Device Co., Ltd., Huawei Device USA Inc., Huawei Technologies Co., Ltd., Huawei Technologies USA Inc. *Defendants' Notice Regarding Technology Tutorial* (Bickham, Timothy) (Filed on 9/1/2015) (Entered: 09/01/2015)
09/09/2015	95	CLERK'S NOTICE RE ALLOTMENT OF TIME FOR SEPTEMBER 18, 2015 TUTORIAL AND MARKMAN HEARING: Parties are hereby notified that the court will allow each side 45 minutes to present the tutorial followed by 45 minutes for each side to argue claim construction issues in connection with the markman hearing. ***This is a text only docket entry, there is no document associated with this notice.*** (ofr, COURT STAFF) (Filed on 9/9/2015) (Entered: 09/09/2015)
09/14/2015	96	**STIPULATION AND ORDER REGARDING ENTRY OF EQUIPMENT INTO THE COURT PURSUANT TO GENERAL ORDER NO. 58 FOR THE TECHNOLOGY TUTORIAL AND CLAIM CONSTRUCTION HEARING by Judge Paul S. Grewal, granting (101) Stipulation in case 3:12-cv-03877-VC (ofr, COURT STAFF) (Filed on 9/14/2015) (Entered: 09/14/2015)**
09/18/2015	97	

		Minute Entry for proceedings held before Magistrate Judge Paul Singh Grewal as to 3:12-cv-03865-VC *Technology Properties Limited LLC et al v. Huawei Technologies Co., Ltd. et al.*, 3:12-cv-03876-VC *Technology Properties Limited, LLC et al v. ZTE Corporation et al*, 3:12-cv-03877-VC *Technology Properties Limited LLC et al v. Samsung Electronic Co., LTD et al.*, 3:12-cv-03880-VC *Technology Properties Limited LLC et al v. LG Electronics, Inc. et al.* and 3:12-cv-03881-VC *Technology Properties Limited LLC et al v. Nintendo Co., Ltd et al.* Tutorial Hearing and Markman Hearing held on 9/18/2015. Court to issue order. Court Reporter: Raynee Mercado. Time in Court: 9:58 to 11:41 and 11:51 to 12:43. Plaintiff Attorney(s) present: Christopher Banys, Barry Bumgardner, Thomas Cecil and Charles Hoge. Defendant Attorney(s) present: Mark Fowler, James Heintz, Hersh Mehta, Stephen Smith, Timothy Bickham and Wasif Qureshi. Also present: Vivek Subramanian. This is a text only Minute Entry (ofr, COURT STAFF) (Date Filed: 9/18/2015) (Entered: 09/18/2015)
09/22/2015	98	**CLAIM CONSTRUCTION REPORT AND RECOMMENDATION. Objections due by 10/6/2015. Signed by Judge Paul S. Grewal on September 22, 2015, re (89) in case 3:12-cv-03865-VC, (102) in case 3:12-cv-03876-VC, (95) in case 3:12-cv-03877-VC, (109) in case 3:12-cv-03880-VC, (97) in case 3:12-cv-03881-VC. (psglc1S, COURT STAFF) (Filed on 9/22/2015) (Entered: 09/22/2015)**
09/28/2015	99	*****EFILED IN ERROR, PLEASE DISREGARD***ORDER GRANTING JOINT MOTION TO STAY ALL PROCEEDINGS AND DEADLINES PENDING RESOLUTION OF OBJECTIONS TO CLAIM CONSTRUCTION REPORT AND RECOMMENDATION by Magistrate Judge Paul Singh Grewal, granting (110) in case 3:12-cv-03876-VC, (105) in case 3:12-cv-03877-VC, (118) in case 3:12-cv-03880-VC, (107) in case 3:12-cv-03881-VC. (psglc1S, COURT STAFF) (Filed on 9/28/2015) Modified on 9/28/2015 (ofr, COURT STAFF). (Entered: 09/28/2015)**
09/30/2015	100	Letter Brief *Letter Brief from Plaintiffs PDS, TPL and PSC to Judge Grewal requesting entry of an Order to stay all deadlines and proceedings, except for the deadlines for Plaintiffs to seek relief and file their objections to the recently issued Claim Construction Report and Recommendation* filed byPhoenix Digital Solutions LLC. (Bumgardner, Barry) (Filed on 9/30/2015) (Entered: 09/30/2015)
10/01/2015	101	TRANSCRIPT ORDER by Futurewei Technologies, Inc., Huawei Device Co., Ltd., Huawei Device USA Inc., Huawei Technologies Co., Ltd., Huawei Technologies USA Inc. for Court Reporter Raynee Mercado. (Flynn-O'Brien, Michael) (Filed on 10/1/2015) (Entered: 10/01/2015)
10/01/2015	102	TRANSCRIPT ORDER by Phoenix Digital Solutions LLC for Court Reporter Raynee Mercado. (Bumgardner, Barry) (Filed on 10/1/2015) (Entered: 10/01/2015)
10/01/2015	103	Letter from Letter Brief from Defendants Futurewei Technologies, Inc., Huawei Device Co., Ltd., Huawei Device USA Inc., Huawei Technologies Co., Ltd., Huawei Technologies USA Inc. *In Response to Letter Brief from*

		Plaintiffs 100 . (Bickham, Timothy) (Filed on 10/1/2015) (Entered: 10/01/2015)
10/02/2015	104	**ORDER GRANTING STAY. Signed by Judge Paul S. Grewal on October 2, 2015, re 100 . (psglc1S, COURT STAFF) (Filed on 10/2/2015) (Entered: 10/02/2015)**
10/06/2015	105	MOTION De Novo Determination of Dispositive Matter Referred to Magistrate Judge re 98 REPORT AND RECOMMENDATIONS re (1 in 3:12-cv-03881-VC) Complaint, filed by Patriot Scientific Corporation, Technology Properties Limited LLC, Phoenix Digital Solutions, LLC, (1 in 3:12-cv-03880-VC) Complaint, filed by Phoenix Digital Solutio *Plaintiffs' Motion for De Novo Determination of Dispositive Matter Referred to Magistrate Judge, or, In the Alternative, Motion for Relief from Nondispositive Pretrial Order of Magistrate Judge* filed by Phoenix Digital Solutions LLC. Motion Hearing set for 11/19/2015 10:00 AM in Courtroom 4, 17th Floor, San Francisco before Hon. Vince Chhabria. Responses due by 10/20/2015. Replies due by 10/27/2015. (Attachments: # 1 Declaration of Barry J. Bumgardner in Support of Plaintiffs' Motion for De Novo Determination, # 2 Exhibit A, # 3 Exhibit B, # 4 Exhibit C, # 5 Exhibit D, # 6 Exhibit E, # 7 Exhibit F, # 8 Exhibit G, # 9 Exhibit H, # 10 Exhibit I, # 11 Exhibit J, # 12 Exhibit K, # 13 Exhibit L, # 14 Exhibit M, # 15 Exhibit N, # 16 Exhibit O)(Bumgardner, Barry) (Filed on 10/6/2015) (Entered: 10/06/2015)
10/20/2015	106	RESPONSE (re 105 MOTION De Novo Determination of Dispositive Matter Referred to Magistrate Judge re 98 REPORT AND RECOMMENDATIONS re (1 in 3:12-cv-03881-VC) Complaint, filed by Patriot Scientific Corporation, Technology Properties Limited LLC, Phoenix Di) *OR, IN THE ALTERNATIVE, MOTION FOR RELIEF FROM NONDISPOSITIVE PRETRIAL ORDER OF MAGISTRATE JUDGE* filed byFuturewei Technologies, Inc., Huawei Device Co., Ltd., Huawei Device USA Inc., Huawei Technologies Co., Ltd., Huawei Technologies USA Inc.. (Attachments: # 1 Proposed Order, # 2 Declaration of A. Wainscoat, # 3 Exhibit A-Part 1, # 4 Exhibit A-Part 2, # 5 Exhibit A-Part 3, # 6 Exhibit B, # 7 Exhibit C, # 8 Exhibit D, # 9 Exhibit E, # 10 Exhibit F, # 11 Exhibit G, # 12 Exhibit H, # 13 Exhibit I, # 14 Exhibit J, # 15 Exhibit K, # 16 Exhibit L, # 17 Exhibit M-Part 1, # 18 Exhibit M-Part 2, # 19 Exhibit M-Part 3, # 20 Exhibit M-Part 4, # 21 Exhibit M-Part 5, # 22 Exhibit N, # 23 Exhibit O, # 24 Exhibit P, # 25 Exhibit Q-Part 1, # 26 Exhibit Q-Part 2, # 27 Exhibit Q-Part 3) (Bickham, Timothy) (Filed on 10/20/2015) (Entered: 10/20/2015)
10/21/2015	107	Transcript of Proceedings held on September 18, 2015, before Paul S. Grewal, Magistrate Judge. Court Reporter Raynee H. Mercado, CSR, telephone number 510-502-6175, cacsr8258@gmail.com, raynee_mercado@cand.uscourts.gov. Per General Order No. 59 and Judicial Conference policy, this transcript may be viewed only at the Clerk's Office public terminal or may be purchased through the Court Reporter until the deadline for the Release of Transcript Restriction. After that date it may be obtained through PACER. Any Notice of Intent to Request Redaction, if required, is due no later than 5 business days from date of this filing. (Re (101 in 3:12-cv-03865-VC) Transcript Order, (108 in 3:12-cv-03877-VC) Transcript Order, (102 in 3:12-cv-03865-VC) Transcript

		Order) Release of Transcript Restriction set for 1/19/2016. (rhm) (Filed on 10/21/2015) (Entered: 10/21/2015)
11/09/2015	108	**ORDER ADOPTING MAGISTRATE JUDGE'S REPORT AND RECOMMENDATIONS for (109 in 3:12-cv-03881-VC) Motion for Miscellaneous Relief,,,, filed by Phoenix Digital Solutions, LLC, (106 in 3:12-cv-03881-VC, 117 in 3:12-cv-03880-VC, 104 in 3:12-cv-03877-VC, 98 in 3:12-cv-03865-VC, 109 in 3:12-cv-03876-VC) Report and Recommendations, (107 in 3:12-cv-03877-VC) Motion for Miscellaneous Relief,,,, filed by Phoenix Digital Solutions LLC, (112 in 3:12-cv-03876-VC) Motion for Miscellaneous Relief,,,, filed by Phoenix Digital Solutions LLC, (120 in 3:12-cv-03880-VC) Motion for Miscellaneous Relief,,,, filed by Phoenix Digital Solutions LLC, (105 in 3:12-cv-03865-VC) Motion for Miscellaneous Relief,,,, filed by Phoenix Digital Solutions LLC. Signed by Judge Vince Chhabria on 11/9/2015. (tlS, COURT STAFF) (Filed on 11/9/2015) (Entered: 11/09/2015)**
11/12/2015	109	STIPULATION WITH PROPOSED ORDER *For Entry of Final Judgment Based on the Court's Claim Construction* filed by Futurewei Technologies, Inc., Huawei Device Co., Ltd., Huawei Device USA Inc., Huawei Technologies Co., Ltd., Huawei Technologies USA Inc.. (Attachments: # 1 Attachment - Final Judgment)(Bickham, Timothy) (Filed on 11/12/2015) (Entered: 11/12/2015)
11/13/2015	110	**Order by Hon. Vince Chhabria in case 3:12-cv-03876-VC; granting (125) Stipulation for Final Judgment in case 3:12-cv-03880-VC.Associated Cases: 3:12-cv-03880-VC, 3:12-cv-03865-VC, 3:12-cv-03876-VC, 3:12-cv-03877-VC, 3:12-cv-03881-VC(knm, COURT STAFF) (Filed on 11/13/2015) (Entered: 11/13/2015)**
11/13/2015		Report on the determination of action mailed to Commissioner (farS, COURT STAFF) (Filed on 11/13/2015) (Entered: 11/27/2015)
12/02/2015	111	NOTICE of Change In Counsel by Stacy Greskowiak McNulty *Notice of Change in Counsel for Plaintiff Phoenix Digital Solutions LLC* (Greskowiak McNulty, Stacy) (Filed on 12/2/2015) (Entered: 12/02/2015)
12/07/2015	112	NOTICE OF APPEAL to the Federal Circuit as to 110 Order on Stipulation, 108 Order Adopting Report and Recommendations,,, by Phoenix Digital Solutions LLC. Filing fee $ 505, receipt number 0971-10044827. Appeal Record due by 1/6/2016. (Bumgardner, Barry) (Filed on 12/7/2015) (Entered: 12/07/2015)
12/10/2015	113	Transmission of Notice of Appeal and Docket Sheet to the Federal Circuit Court of Appeals. Appeal Record due by 1/11/2016. (farS, COURT STAFF) (Filed on 12/10/2015) (Entered: 12/10/2015)
12/15/2015	114	USCA Case Number 16-1306 Federal Circuit for 112 Notice of Appeal to the Federal Circuit, filed by Phoenix Digital Solutions LLC. (farS, COURT STAFF) (Filed on 12/15/2015) (Entered: 12/15/2015)

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Exhibit A

Claim Terms and Constructions Agreed Upon by the Parties

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
		'749 PATENT		
1.	a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item	a portion of the first push down stack that receives items pushed from the means for storing next item and stores items on a "last in, first out" basis	a portion of the first push down stack that receives items pushed from the means for storing next item and stores items on a "last in, first out" basis	
2.	arithmetic logic unit	a digital circuit that performs arithmetic and logical operations	a digital circuit that performs arithmetic and logical operations	
3.	central processing unit	electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions	electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions	
4.	central processing unit integrated circuit	miniature circuit, on a single semiconductor substrate, that controls the interpretation and execution of programmed instructions	miniature circuit, on a single semiconductor substrate, that controls the interpretation and execution of programmed instructions	
5.	configured and connected to . . . supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle	configured and connected to . . . provide the multiple sequential instructions in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during a single memory cycle	configured and connected to . . . provide the multiple sequential instructions in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during a single memory cycle	

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
6.	first input of said ALU	a first input of the [ALU] for receiving data	a first input of the [ALU] for receiving data	
7.	means for storing a next item	Construed pursuant to 35 U.S.C. § 112(6) Structure: a register or its equivalents Function: storing a next item	Construed pursuant to 35 U.S.C. § 112(6) Structure: a register or its equivalents Function: storing a next item	
8.	means for storing a top item	Construed pursuant to 35 U.S.C. § 112(6) Structure: a register or its equivalents Function: storing a top item	Construed pursuant to 35 U.S.C. § 112(6) Structure: a register or its equivalents Function: storing a top item	
9.	memory external of said central processing unit integrated circuit	a memory on a separate substrate from the [central processing unit integrated circuit]	a memory on a separate substrate from the [central processing unit integrated circuit]	
10.	multiple sequential instructions	two or more instructions in a program sequence	two or more instructions in a program sequence	
11.	multiplexing means	a multiplexer	a multiplexer	
12.	second input of said ALU	a second input, distinct from the first input, of the ALU for receiving data	a second input, distinct from the first input, of the ALU for receiving data	
13.	single memory cycle	the time required to read information from the memory	the time required to read information from the memory	

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
		'890 PATENT		
14.	bus	a group of conductors	a group of conductors	
15.	central processing unit	electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions.	electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions.	
16.	loop counter	counter circuit in the main [CPU] that stores a variable value representing a remaining number of times a particular instruction or group of instructions is to be executed by the main [CPU]	counter circuit in the main [CPU] that stores a variable value representing a remaining number of times a particular instruction or group of instructions is to be executed by the main [CPU]	
17.	mode register	register that stores mode bits.	register that stores mode bits.	
18.	multiplexing means	a multiplexer	A multiplexer	
19.	return stack pointer	storage element in the main [central processing unit], separate and distinct from the stack pointer, that stores a value representing a location in the return push down stack	storage element in the main [central processing unit], separate and distinct from the stack pointer, that stores a value representing a location in the return push down stack	
20.	ring oscillator	an [oscillator] having multiple, odd number of inversions arranged in a loop, wherein the [oscillator] is variable based on the temperature, voltage and process parameters in the environment	an [oscillator] having multiple, odd number of inversions arranged in a loop, wherein the [oscillator] is variable based on the temperature, voltage and process parameters in the environment	

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
		'336 PATENT		
21.	central processing unit	electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions	electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions	
22.	clocking said central processing unit	providing a timing signal to said [central processing unit]	providing a timing signal to said [central processing unit]	
23.	external clock is operative at a frequency independent of a clock frequency of said oscillator	external clock wherein a change in the frequency of either the external clock or [oscillator] does not affect the frequency of the other	external clock wherein a change in the frequency of either the external clock or [oscillator] does not affect the frequency of the other	
24.	external memory bus	a [bus] coupled between the I/O interface and an external storage device	a [bus] coupled between the I/O interface and an external storage device	
25.	integrated circuit	miniature circuit on a single semiconductor substrate	miniature circuit on a single semiconductor substrate	`
26.	microprocessor	electronic circuit that interprets and executes programmed instructions	electronic circuit that interprets and executes programmed instructions	
27.	off-chip external clock	clock not on the integrated circuit substrate	clock not on the integrated circuit substrate	

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
28.	on-chip input/output interface	circuit having logic for input/output communications, where that circuit is located on the same semiconductor substrate as the [CPU]	circuit having logic for input/output communications, where that circuit is located on the same semiconductor substrate as the [CPU]	
29.	oscillator	circuit capable of maintaining an alternating output	circuit capable of maintaining an alternating output	
30.	oscillator . . . clocking	[oscillator] that generates the signal(s) used for timing the operation of the [CPU]	[oscillator] that generates the signal(s) used for timing the operation of the [CPU]	
31.	processing frequency	speed at which the [CPU] operates.	speed at which the [CPU] operates	
32.	ring oscillator	an [oscillator] having multiple, odd number of inversions arranged in a loop, wherein the [oscillator] is variable based on the temperature, voltage and process parameters in the environment	an [oscillator] having multiple, odd number of inversions arranged in a loop, wherein the [oscillator] is variable based on the temperature, voltage and process parameters in the environment	
33.	varying . . . in the same way	increasing and deceasing proportionally	increasing and deceasing proportionally	
34.	wherein said central processing unit operates asynchronously to said input/output interface	The timing control of the [central processing unit] that operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them.	The timing control of the [central processing unit] that operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them.	

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
13.	separate direct memory access central processing unit	A central processing unit that accesses memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit.	central processing unit that accesses memory, that fetches and executes instructions for itself directly and separately from the main central processing unit, and that fetches instructions for the main central processing unit	
14.	X register	A first register used in memory operations.	memory pointer which can be used for memory access and simultaneously incremented or decremented	
15.	Y register	A second register used in memory operations.	memory pointer which can be used for memory access and simultaneously incremented or decremented	

Nos.	Terms	Plaintiffs' Constructions	Defendants' Constructions	Notes
		'336 PATENT		
16.	an entire oscillator disposed upon said integrated circuit substrate	An [oscillator] that is located entirely on the same semiconductor substrate as the [central processing unit].	an [oscillator] that is located entirely on the same semiconductor substrate as the [central processing unit] and does not rely on a control signal or an external crystal/clock generator to cause clock signal oscillation or control clock signal frequency	

Accordingly, the Court construes the term "separate direct memory access central processing unit" to mean:

> **a central processing unit that accesses memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit.**

C. '336 Patent

1. Claim 1

Claim 1 of the '336 Patent provides:

> A microprocessor system, comprising
> a single integrated circuit including a central processing unit and an **entire ring oscillator variable speed system clock** in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,
> said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,
> a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;
> an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and
> a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.

The parties tender the phrase "ring oscillator" for construction.

Upon review, the Court finds that one of ordinary skill in the art would understand the phrase "ring oscillator" to mean: "interconnected electronic components comprising multiple odd numbers of inverters arranged in a loop."[30] When a voltage is applied, the ring oscillator generates signals that are used by the processing unit to regulate the timing of its operations. In contrast with a circuit

[30] The parties agree that a "ring oscillator" is "an oscillator having a multiple, odd number of inversions arranged in a loop," which is the construction arrived at by Judge Ward in the Texas action, though they disagree about whether additional limitations should be added to Judge Ward's construction of the term. (See Plaintiffs' Brief at 3; Defendants' Opening Claim Construction Brief for the "Top Ten" Terms at 16-17, Docket Item No. 310 in No. C 08-00877 JW.)

that receives its timing signal from an external clock, a person of ordinary skill in the art reading the patent would understand that Claim 1 claims a "single integrated circuit," fabricated so as to include a "ring oscillator."

At issue is whether the phrase "ring oscillator" should be given a specialized meaning based on statements made by the inventors during reexamination of Claims 4 and 8 of the '148 Patent.[31]

Claim 4 of the '148 Patent claims in pertinent part:

> A microprocessor integrated circuit comprising . . . a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said integrated circuit substrate.

Claim 8 of the '148 Patent has a similarly worded limitation.

During reexamination, the examiner reviewed the allowance of Claims 4 and 8 over U.S. Patent No. 4,689,581 ("Talbot"). The Talbot Patent, which is entitled "Integrated Circuit Phase Locked Loop Timing Apparatus," claims:

> an integrated circuit device . . . and a timing apparatus . . . formed on a common single chip, said timing apparatus comprising a phase locked loop [comprising, *inter alia*] a voltage controlled oscillator arranged to be controlled by [a] voltage signal to produce [an] output timing signal at its output.

(Talbot, Col. 10:48-11:9.)

Preliminarily, the examiner rejected Claims 4 and 8 of the '148 Patent as unpatentable over Talbot. During the course of reexamination proceedings, the examiner conducted an interview with the patent owner and discussed whether Claims 4 and 8 were allowable over Talbot.[32] Afterward,

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[31] Because the '148 Patent shares the same specification with the '336 Patent and is directly related to the other three Patents-in-Suit, the Court finds that any representation regarding similar terms made by the inventors during the prosecution of the '148 Patent is relevant to its consideration and construction of the terms in the '336 Patent. See Microsoft Corp. v. Multi-Tech Sys., Inc., 357 F.3d 1340, 1350 (Fed. Cir. 2004) ("Any statement of the patentee in the prosecution of a related application as to the scope of the invention would be relevant to claim construction.").

[32] (See Otteson Decl., Ex. X, Ex Parte Reexamination Interview Summary, Docket Item No. 310-2.)

the examiner prepared and sent to the patent owner an "Interview Summary."[33] Specifically, with respect to the discussion of Talbot, the examiner wrote:

> Continuing, the patent owner further argued that the reference of Talbot does not teach of a "ring oscillator." The patent owner discussed features of a ring oscillator, such as being **non-controllable**, and being **variable based on the environment**. **The patent owner argued that these features distinguish over what Talbot teaches**. The examiner will reconsider the current rejection based on a forthcoming response, which will include arguments similar to what was discussed.[34]

In its post-interview submission, the patent owner reiterated the contention that the claim should be allowed because Talbot disclosed a "voltage-controlled oscillator" and not the "ring oscillator" disclosed in the claim:

> Further, Talbot does not teach, disclose, or suggest the ring oscillator recited in claim 4. The Examiner cited col. 3, ll. 26-36, and oscillator circuit 12 shown in FIG. 1 of Talbot as teaching the recited ring oscillator. Talbot discusses a voltage-controlled oscillator (VCO) 12, but does not teach or disclose a ring oscillator.[35]

During the course of these claim construction proceedings, the inventors have continued to maintain that Talbot was overcome during reexamination because it does not disclose a "ring oscillator."[36]

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[33] An examiner's interview summary may serve as a basis for finding a prosecution disclaimer that narrows the claim scope. See, e.g., Rheox, Inc. v. Entact, Inc., 276 F.3d 1319, 1322 (Fed. Cir. 2002); Biovail Corp. Int'l v. Andrx Pharms., Inc., 239 F.3d 1297, 1302-04 (Fed. Cir. 2001).

[34] (See Chen Decl., Ex. 4, Ex Parte Reexamination Interview Summary, Docket Item No. 316-4 (emphasis added).)

[35] (Otteson Decl., Ex. Y, Remarks/Arguments at 11, hereafter, "Remarks," Docket Item No. 310-3.)

[36] For instance, Defendants argued during the Markman hearing that the inventors' written submission distinguished the Talbot reference because Talbot lacked a ring oscillator and never mentioned a requirement of "non-controllability." Further, Defendants also refer to the inventors' written response on February 21, 2008, which states:

> Further, **Talbot does not teach, disclose, or suggest the ring oscillator** recited in claim 4. ... Talbot discusses a voltage-controlled oscillator (VCO) 12, but **does not teach or disclose a ring oscillator**. Talbot provides two different implementations of the VCO 12 in FIGS. 3-4, **neither one of which is a ring oscillator**. Talbot refers to the oscillator of FIG. 3 as a "frequency controlled oscillator" (col. 7, ll. 21-22) and the oscillator of FIG. 4 simply as a "voltage controlled oscillator" (col. 8, ll. 59-65). As the sole inventor of the cited reference,

The Court has examined the Talbot patent. Although the component is, indeed, referred to as a "voltage-controlled oscillator," declarations and other extrinsic materials that have been tendered during the claim construction proceedings call into question the validity of the inventors' contention to the PTO and to this Court that the "ring oscillator" is different from the "voltage-controlled oscillator" disclosed in Talbot. On the one hand, the Court has received extrinsic evidence that the voltage-controlled oscillator disclosed in Talbot *is* a ring oscillator. On the other hand, arguments have been submitted claiming that the voltage-controlled oscillator of Talbot *is not* a ring oscillator.[37]

Under clear Federal Circuit law, a submission made by an inventor during reexamination is regarded as a disavowal only if the court finds that the allegedly disavowing statement is "so clear as to show reasonable clarity and deliberateness, and so unmistakable as to show unambiguous evidence of disclaimer." Omega Eng'g, Inc. v. Raytek Corp., 334 F.3d 1314, 1325 (Fed. Cir. 2003) (citations omitted).

Here, before arriving at a decision on the definition of the phrase "ring oscillator" in the context of the Talbot reference, the Court finds that it would benefit from further briefing. In the supplement briefs, the declarants shall fully articulate the technical basis for their opinions with respect to whether the voltage-controlled oscillator disclosed in Talbot is or is not a ring oscillator. The Court will return to the construction of the phrase "ring oscillator" following the completion of the supplement briefing.

> Talbot presumably possesses at least ordinary skill in the art, yet Talbot did not characterize either of the disclosed oscillators as ring oscillators. Applicants respectfully assert that the reason they were not characterized by Talbot as ring oscillators is because **they are not ring oscillators**. For at least the foregoing reasons, **Talbot does not teach, disclose, or suggest a ring oscillator** as recited in the claims. (Remarks at 11 (emphases added).)

[37] This issue is important to claim construction, because it is relevant to understanding in what manner the ring oscillator is "non-controllable," as distinguished from the voltage-controlled oscillator disclosed in Talbot. Resolving this conflict might affect how the Court approaches issues with respect to the validity of the patent claim at issue.

patent refer to how instructions and data are organized in memory; the '749 patent claims how multiple sequential instructions are supplied to the CPU in a single memory cycle. Plaintiffs ignore the significant distinctions between the claims of the two patents, as they must, because it is the *claims* of a patent that define the scope of the invention.

Unlike the '584 patent, the '749 patent claims "multiple sequential instructions". The claimed multiple sequential instructions are not the same as the '584 patent's "instruction groups" for at least the simple reason there is no limitation in the '749 claims requiring an operand as is the case in, for example, claim 29 of the '584 patent. Moreover, there is no limitation in the claims of the '749 patent that even implicitly require such hypothetically present operands be right justified because, in contrast to claim 29 of the '584 patent, there is no that requirement any operand be located at a "predetermined position." Thus, Judge Ward's construction of "instruction groups," with its limitation on operands in the context of a claim directed to "certain instructions," is inapplicable here.

For the foregoing reasons, TPL's proposed construction should be adopted.

B. <u>The Proper Construction of "Separate Direct Memory Access Central Processing Unit" ('890 Patent)</u>.

The parties dispute the proper construction of the term "separate direct memory access central processing unit," as follows:

Disputed Term	Plaintiffs' Proposed Construction	TPL's Proposed Construction
separate direct memory access central processing unit	a separate CPU that fetches and executes instructions for performing direct memory access without using the main CPU	electrical circuit for reading and writing to memory that is separate from a main CPU

A straightforward reading of claim 1 of the '890 patent provides for: (i) a main central processing unit (or main CPU); and (ii) a direct memory access central processing unit (or DMA CPU) that is separate from the main CPU:

> A microprocessor, which comprises a main central processing unit and a separate direct memory access central processing unit in a single integrated circuit comprising said

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORPORATION, ALLIACENSE LTD., Defendants.	Case No. 5:08-cv-00877 PSG **(Re: Docket Nos. 356, 357, 358, 374)**
HTC CORPORATION, HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORPORATION, ALLIACENSE LTD., Defendants.	Case No. 5:08-cv-00882 PSG **(Re: Docket Nos. 385, 387, 388, 403)**

CLAIM CONSTRUCTION ORDER

On November 30, 2012, following reassignment of this case to the undersigned with the consent of the parties and in light of the retirement of Chief Judge Ware, and the completion of an

extended *Markman* hearing, the court issued an order from the bench construing five of the parties' disputed terms. The court provided a written summary of its constructions a few days later.[1] The court now explains its reasoning below.

I. BACKGROUND

In this suit, Plaintiffs Acer, Inc., Acer America Corp., Gateway, Inc., HTC Corp., and HTC America, Inc.[2] seek a declaratory judgment that they do not infringe patents owned by Defendants Technology Properties, Patriot Scientific, and Alliacense (collectively "TPL"). All of the patents at issue relate to various aspects of microprocessors.

On November 30, 2012, the court held a claim construction hearing to consider five disputed terms. Prior to the case being reassigned to the undersigned, Judge Ware considered the same five terms.[3] He construed three of them and asked for more briefing on two of them, although he also provided a tentative construction for the two.[4]

The Eastern District of Texas also has considered related terms in another case that TPL filed in 2006 against unrelated third parties. In that case, Judge Ward held a claim construction hearing and issued a decision construing terms based upon patents with the same specification as the patents at issue in this suit.[5] Several terms he construed overlap with terms at issue here. Although the case resolved before proceeding to trial, TPL appealed a portion of the claim construction ruling to the Federal Circuit with respect to one of the three patents in suit; the Federal Circuit affirmed the district court's judgment against TPL.[6]

[1] *See* Docket No. 381.

[2] Barco N.V. was originally a party and was a party to the motions at issue, but is no longer involved in the case.

[3] *See* Docket No. 336.

[4] *See id.*

[5] *See Tech. Properties Ltd. v. Matsushita Elec. Indus. Co., Ltd.*, 514 F. Supp. 2d 916, 927 (E.D. Tex. 2007) *aff'd sub nom.*, 276 F. App'x 1019 (Fed. Cir. 2008). At issue were United States Patent Nos. 5,809,336, 6,598,148, and 5,784,584.

[6] *See Tech. Properties Ltd., Inc. v. Arm, Ltd.*, 276 F. App'x 1019 (Fed. Cir. 2008).

The terms at issue are found in United States Patent No. 5,440,749 (the "'749 Patent") titled "High Performance, Low Cost Microprocessor Architecture,"[7] United States Patent No. 5,809,336 (the "'336 Patent") titled "High Performance Microprocessor Having Variable Speed System Clock,"[8] and United States Patent No. 5,530,890 (the "'890 Patent"), titled "High Performance, Low Cost Microprocessor."[9] All three patents derive from the same original patent application that was subject to a ten-way restriction requirement and eventually resulted in six different patents known as the Moore Microprocessor Portfolio patents, all of which share a common specification.

The '749 Patent claims an invention that accelerates the operation of microprocessors by fetching multiple instructions from memory per memory cycle. Because a CPU can execute instructions faster than it can fetch them from memory, fetching multiple instructions per memory cycle can improve overall performance.

The '336 Patent claims an invention that allows the frequency of a CPU to fluctuate based upon conditions. Traditional microprocessors use fixed frequency clocks to regulate the frequency with which the CPU operates. Fixed clocks generally have to be set lower than the CPU's maximum possible frequency to ensure proper operation under the worst-case conditions. The '336 Patent claims an invention that solves this problem by placing a ring oscillator on the same microchip as the CPU to act as the clock. Because the ring oscillator is on the same microchip and made out of the same components as the CPU, it is subject to the same environmental conditions and thus it will operate at a variable speed based upon conditions allowing the CPU to operate at higher rates during good conditions and lower rates during bad.

The '890 Patent relates to microprocessor architecture and claims a direct memory access mechanism. Most microprocessors have a direct memory access controller that handles the slow operation of reading and writing to memory so that the CPU can execute other instructions while waiting. The patent discloses a direct memory access CPU, which can execute some instructions in addition to reading and writing to memory for the CPU.

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[7] *See* Docket No. 358-2.

[8] *See* Docket No. 358-6.

[9] *See* Docket No. 368-2.

II. LEGAL STANDARDS

Claim construction is exclusively within the province of the court.[10] "To construe a claim term, the trial court must determine the meaning of any disputed words from the perspective of one of ordinary skill in the pertinent art at the time of filing."[11] This requires a careful review of the intrinsic record, comprised of the claim terms, written description, and prosecution history of the patent.[12] While claim terms "are generally given their ordinary and customary meaning," the claims themselves and the context in which the terms appear "provide substantial guidance as to the meaning of particular claim terms."[13] Indeed, a patent's specification "is always highly relevant to the claim construction analysis."[14] Claims "must be read in view of the specification, of which they are part."[15]

Although the patent's prosecution history "lacks the clarity of the specification and thus is less useful for claim construction purposes," it "can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be."[16] The court also has the discretion to consider extrinsic evidence, including dictionaries, scientific treatises, and testimony from experts and inventors. Such evidence, however, is "less significant than the intrinsic record in determining the legally operative meaning of claim language."[17]

Judge Ware has already considered all of the terms currently before the court. Although the court granted leave for parties to file motions for reconsideration, it will take as its starting point that

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[10] *See Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 387 (1996).

[11] *Chamberlain Group, Inc. v. Lear Corp.*, 516 F.3d 1331, 1335 (Fed. Cir. 2008).

[12] *See id.*; *Phillips v. AWH Corp*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (internal citations omitted).

[13] *Phillips*, 415 F.3d at 1312, 1314.

[14] *Id.* at 1312-15.

[15] *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996); *see also Ultimax Cement Mfg. Corp v. CTS Cement Mfg. Corp.*, 587 F. 3d 1339, 1347 (Fed. Cir. 2009).

[16] *Phillips*, 415 F.3d at 1317 (internal quotations omitted).

[17] *Id.* (internal quotations omitted).

the earlier constructions are correct. Consistent with Local Rule 7-9, absent newly discovered material facts, change in law, or manifest failure to consider material facts or arguments, the court will not alter any earlier constructions.[18]

III. CLAIM CONSTRUCTION

A. "instruction register"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
Register that receives and holds one or more instructions for supplying to circuits that interpret the instructions, in which any operands that are present must be right-justified in the register	Register that receives and holds one or more instructions for supplying to circuits that interpret the instructions

The parties dispute the construction of "instruction register" as used in claim 1 of the '749 Patent. The term "instruction register" was added to a wherein clause in claim 1 of the '749 patent during reexamination. The patent claims a microprocessor system

> wherein the microprocessor system comprises an instruction register configured to store the multiple sequential instructions and from which instructions are accessed and decoded.[19]

Judge Ware tentatively construed "instruction register" in the '749 patent as having its plain and ordinary meaning.[20] Quoting a dictionary, he determined that instruction register meant a "register in a central processing unit that holds the address of the next instruction to be executed."[21] After construing the term, the court noted that the prosecution history might convince the court to limit its construction and requested more briefing.[22]

The parties agree that the term has a slightly different meaning than the one the court previously adopted because the court's previous definition came from a software dictionary and the patents are hardware-related. The parties agree that the meaning of "instruction register" in the

[18] *See Therasense, Inc. v. Becton, Dickinson & Co.*, 560 F. Supp. 2d 835, 844 (N.D. Cal. 2008) (following courts in the Northern District of California that "have required a litigant to meet the Civil Local Rule 7-9 standard when requesting reconsideration of a claim construction").

[19] *See* Docket No. 358-2, Reexam. Cert., col.1 ll.55-60.

[20] *See* Docket No. 336 at 11.

[21] *Id.* at 10 (quoting MICROSOFT COMPUTER DICTIONARY 276 (5th ed. 2002)).

[22] *See id.* at 11 n.23.

context of hardware is a "register that receives and holds one or more instructions for supplying to circuits that interpret the instructions." The court takes this construction as its starting point.

TPL urges the court to keep this construction while Plaintiffs argue for a more limited construction requiring that the operands in the register be right-justified. Even though Judge Ware's prior order indicated he was interested in an explanation of the prosecution history, the parties' arguments remain focused on the specification.

Plaintiffs argue that the specification requires the right-justified limitation for the register that it seeks. The Federal Circuit has instructed that "the specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess" or "reveal an intentional disclaimer."[23] However, only a clear disclaimer can justify narrowing the construction.[24] Where a patent consistently references a certain limitation or a preferred embodiment as the present invention, that also can serve to limit the scope of the invention where no other intrinsic evidence suggests otherwise.[25]

Here, Plaintiffs rely on a section of the patent specification that explains that the patented invention is able to use variable width operands because "operands must be right justified in the instruction register."[26] The specification describes this limitation as necessary to make the "magic" of the patent possible.[27] Plaintiffs argue that this is the equivalent of defining the "present invention," but the intrinsic evidence does not clearly support this limitation.

First, the right justified limitation is not a clear and consistent limitation given the overall context of the patent and the specification. The '749 patent is derived from an application that was subject to a ten-way restriction requirement that eventually resulted in six different patents. The original application, which eventually issued as the '749 patent disclosed all of the inventions in

[23] *Phillips*, 415 F.3d at 1316.

[24] *See Voda v. Cordis Corp.*, 536 F.3d 1311, 1320 (Fed. Cir. 2008).

[25] *See Absolute Software, Inc.*, 659 F.3d at 1136.

[26] *See* Docket No. 358-2 at col.18 ll.43-45.

[27] *Id.*

what is now their extensive shared specification.[28] Plaintiffs rely on one small section of the common specification, with the heading "Variable Width Operands," covering about twenty lines of the thirty-three column specification.[29] Although this small section contains strong limiting language, because the specification is common to ten different inventions, it does not necessarily apply to the '749 Patent. In fact, Judge Ware previously held that one of those inventions, disclosed in the '584 patent, deals specifically with variable width operands.[30] But variable width operands are not essential to what is claimed in the '749 Patent. Claim 1 of the '749 Patent, the claim at issue here, does not contain the term operand or require variable width operands. Although parties focus on the '749 patent, the same reasoning applies to the '890 Patent.

Second, the specification actually discloses an embodiment where the operands are not right justified. In one embodiment, the instruction register receives four 8-bit instructions.[31] The specification disclosed two instructions, the "Read-Local-Variable XXXX" and "Write-Local-Variable XXXX," which are fixed width instructions that have a 4-bit opcode and a 4-bit operand.[32] These instructions can go into any of the four 8-bit slots in the instruction register and thus would contain operands that are not right justified.[33] At oral argument, Plaintiffs disputed TPL's characterization of these embodiments, arguing that the "4-bit operands" are not actually operands, but the location in temporary storage where the operand actually exists.[34] Even if the location in temporary storage is not a traditional operand, it acts similarly to one and adds further intrinsic evidence supporting a finding that the right justified limitation does not apply to the '749 and '890 patents.

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[28] *See generally*, Docket No. 358-2 at col.1-35.

[29] *See* Docket No. 358-2 at col.18 ll.35-56.

[30] *See* Docket No. 336 at 11.

[31] *See* Docket No. 358-2 at col.7 ll.50-58.

[32] *See* Docket No. 358-2 at col.31-32 ll.45-15.

[33] *See generally*, *id.* at col.7 ll.50-58.

[34] *See* Docket No. 382 at 106-07.

Plaintiffs do briefly cite to the prosecution history where, in a handwritten summary of an in-person interview in response to a Patent Office Action rejecting several of the claims of a related patent, the examiner stated "Claim 1: Operand width is variable + right adjusted."[35] Because various claims were withdrawn, however it is unclear to exactly what claim the examiner referred. This is not clear and unmistakable disavowal by the applicant.[36]

The parties agreed upon meaning alone should control. Accordingly, the court construes "instruction register" as the "register that receives and holds one or more instructions for supplying to circuits that interpret the instructions."

B. "ring oscillator"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is (1) non-controllable; and (2) variable based on the temperature, voltage and process parameters in the environment	an oscillator having a multiple, odd number of inversions arranged in a loop

The parties ask the court to construe the term "ring oscillator" as it is used in claim 1 of the '336 Patent. Judge Ware held that one of ordinary skill in the art would understand the term to mean "interconnected electronic components comprising multiple odd numbers of inverters arranged in a loop."[37] However, he ordered more briefing as to whether the court should give the terms a specialized meaning based upon the statements of the inventors during reexamination to distinguish their invention from the Talbot Patent.[38]

Once again, the parties agree on the basic meaning of the term, but dispute additional limitations. They agree that the meaning of the term is at least "an oscillator having a multiple, odd

[35] Docket No. 363-19 at 2.

[36] *See Univ. of Pittsburgh of Commonwealth Sys. of Higher Educ. v. Hedrick*, 573 F.3d 1290, 1297 (Fed. Cir. 2009) (finding a "patentee may limit the meaning of a claim term by making a clear and unmistakable disavowal of scope during prosecution," but an examiner's summary of disavowal may only create a "weak inference" of the disavowal); *3M Innovative Properties Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1373 (Fed. Cir. 2003) (finding that prosecution history "cannot be used to limit the scope of a claim unless the *applicant* took a position before the PTO." (emphasis in the original)).

[37] Docket No. 336 at 13.

[38] *Id.* at 14-16.

number of inversions arranged in a loop." TPL urges the court to adopt meaning alone while the Plaintiffs argue that the term must be further limited to be: (1) non-controllable and (2) variable based on temperature, voltage, and process parameters in the environment. Plaintiffs argue that the prosecution history and specification support their position. As explained below, the prosecution history is too ambiguous to support Plaintiffs' construction in full, but the specification and especially the claim language do support Plaintiffs' second limitation.

1. Prosecution history

A "clear and unmistakable" disavowal by the patentee during prosecution or reexamination can narrow the scope of a claim.[39] However, because the "ongoing negotiations between the inventor and the examiner" can "often produce ambiguities," the doctrine only applies to "unambiguous disavowals."[40]

In the patent examiner's summary of his meeting with the patent owner, he wrote that

> the patent owner further argued that the reference of Talbot does not teach of a 'ring oscillator.' The patent owners discussed features of a ring oscillator, such as being non-controllable and being variable based upon the environment. The patent owner argued that these features distinguish over what Talbot teaches.[41]

The examiner finished his summary noting that he would "reconsider the current rejection based upon a forthcoming response, which will include arguments similar to what was discussed."[42] The subsequent written response argued that the Talbot reference did not teach a ring oscillator generally, and did *not* specifically argue that the ring oscillator was "non-controllable."[43] The examiner accepted this argument and withdrew the rejection.[44]

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[39] *Grober v. Mako Products, Inc.*, 686 F.3d 1335, 1341 (Fed. Cir. 2012), reh'g denied (Sept. 14, 2012).

[40] *Id.*

[41] Docket No. 357-5 at 5. The interview summary relates to the '148 patent, but it shares the same specification with the '336 patent.

[42] *Id.*

[43] *See id.*

[44] *Id.* at 27.

Plaintiffs argue that the examiner's summary is a clear disavowal that should limit the scope of the claim. The court disagrees. The Federal Circuit has suggested that where, as here, the "disavowal" is only an examiner's summary of a patentee's statement, it only creates a "weak inference" of a disavowal.[45] The subsequent prosecution history does not support Plaintiffs' claim construction because the patent owner appears to have made a different argument in his written reply, simply stating that the Talbot reference did not include a ring oscillator *generally* and not distinguishing the ring oscillator of the '336 Patent based on the examiner's stated exemplary features of ring oscillators.[46]

During prosecution, the patent owner also stated that the "the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so."[47] This statement is not a disavowal because it only affirms that external inputs are "not required." The statement does not clearly impose a prohibition on all types of control.

2. Specification

Plaintiffs also argue that the specification supports their proposed construction. The specification describes the "ring oscillator" as having its frequency "determined by the parameters of temperature, voltage, and process."[48] Although this portion of the specification appears to disclose the preferred embodiment rather than constitute an express limitation on the claimed invention,[49] Claim 1 of the '336 Patent *claims* that the processing frequency of the CPU and the ring

[45] *See Univ. of Pittsburgh*, 573 F.3d at 1297.

[46] *See generally, Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1124 (Fed. Cir. 2004) (describing a series of exchanges between the patent owner and the examiner as the parties "talking past one another" and finding no clear evidence of a disavowal from the confused exchange).

[47] Docket No. 363-4 at 6.

[48] *See* Docket No. 358-6 at col.16 ll.59-60.

[49] *See Brookhill-Wilk 1, LLC. v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1301-02 (Fed. Cir. 2003) ("statements from the description of the preferred embodiment are simply that-descriptions of a preferred embodiment. . . Absent a clear disclaimer of particular subject matter, the fact that the inventor anticipated that the invention may be used in a particular manner does not limit the scope to that narrow context.")

oscillator vary together due to manufacturing variations, operating voltage, and temperature.[50] The claim itself provides that the "ring oscillator" is "constructed of the same process technology with corresponding manufacturing variations" on the same single integrated circuit so that its performance will fluctuate with the CPU because they are subject to the same "manufacturing variations" and "operating voltage and temperature."[51] During oral argument, TPL admitted that a ring oscillator on the same microprocessor as the CPU will vary based upon voltage, temperature, and process variations.[52] Therefore, based upon the claim language and the specification, the court finds that the disclosed "ring oscillator" varies with voltage, temperature, and process variations.

Even though the claimed "ring oscillator" is "determined by the parameters of temperature, voltage, and process," it does not necessarily follow, as Plaintiffs' argue, that the "ring oscillator" must be non-controllable.[53] The claims do not mention "controllable" or "non-controllable" in relation to the "ring oscillator" and neither does the specification. The term "non-controllable" is only used by the patent examiner in the prosecution history discussed above. Additionally, in the preferred embodiment, the "ring oscillator" is "determined" by temperature, voltage, and process,[54] which suggests at least one embodiment in which the ring oscillator is controlled.

Because of the clear limitation in the claims that temperature, voltage, and process determine the "ring oscillator's" frequency, the court includes those limitations in the construction of the term, but does not find similar support for importing the "non-controllable" limitation. The court therefore construes "ring oscillator" as "an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment."

[50] *See* Docket No. 358-6, Reexam. Cert. col.2 ll.3-5.

[51] *Id.* at col.1-2 ll.59-05.

[52] *See* Docket No. 382 at 49:3-7.

[53] *See, e.g., Brookhill-Wilk*, 334 F.3d at 1301-02.

[54] *See* Docket No. 358-6 at col.16 ll.59-60.

C. "separate DMA CPU"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
a central processing unit that accesses memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit	Electrical circuit for reading and writing to memory that is separate from a main CPU

Judge Ware previously construed the term "separate direct memory access central processing unit" ("separate DMA CPU") from Claim 11 of the '890 Patent. Claim 11 claims

> A microprocessor, which comprises a main central processing unit and a separate direct memory access [DMA] central processing unit [CPU] in a single integrated circuit comprising said microprocessor . . .

The court construed "separate DMA CPU," consistent with its plain and ordinary meaning as "a central processing unit that accesses memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit."[55] Plaintiffs urge the court to keep this construction while TPL argues that previously unaddressed parts of the prosecution history support a different construction broad enough to include standard DMA controllers, which do not execute instructions.

TPL's primary argument is that the history of the Moore patents supports a broader construction. TPL argues that the DMA CPU that fetches and executes its own instructions was one of the ten categories of inventions derived from the original application, but not the invention that eventually became the patent at issue, the '890 Patent. As explained above, the original patent application for what became the '749 Patent was subject to a ten-way restriction. A restriction indicates that "two or more independent and distinct inventions are claimed in one application."[56] One of these 10 categories of inventions was focused on a "microprocessor system having a DMA for fetching instruction[s] for a CPU and itself."[57] The patentee eventually abandoned this application. The '890 Patent came from a different category of invention "drawn to a microprocessor architecture."[58] TPL argues that because the '890 Patent came from a different

[55] Docket No. 336 at 13.

[56] 35 U.S.C. § 121.

[57] Docket No. 368-7 at 3.

[58] *Id.* *See also* Docket No. 356 at 3-4.

invention category, it should not be read to include the definition of the "DMA CPU" that was the subject of another invention.

The court disagrees. The fact that one abandoned patent focused on a particular subject matter does not necessarily mean that same subject matter cannot be within the scope of another related patent based upon the same specification. First, restriction requirements have little, if any, evidentiary weight.[59] Second, there is nothing in the claims to suggest that "DMA CPU" should have anything other than its plain and ordinary meaning. Third, the specification supports the plain and ordinary meaning. The specification discloses a "DMA CPU" in figures 2 and 9. When describing figure 2, the specification states that the "DMA CPU 72 controls itself and has the ability to fetch and execute instructions. It operates as a co-processor to the main CPU 70."[60] The "DMA CPU 314" in figure 9 is part of another microprocessor that the specification describes as equivalent to the microprocessor in figure 2.[61] A separate passage in a later section of the specification describes another embodiment where the "DMA processor 72 of the microprocessor 50 has been replaced with a more traditional DMA controller 314."[62] The specification goes on to describe the characteristics of a DMA controller. These sections are clear that a DMA controller is distinct from a DMA CPU and the patent refers to each by name where appropriate. Thus where the patent claims a DMA CPU, it means a DMA CPU and not a DMA controller.

TPL also argues that statements made during reexamination by the requester and the examiner support its position. The court disagrees. First, the examiner and the reexamination requester made the cited statements, not the patent owner.[63] Second, regardless of who made the

[59] *See Honeywell Int'l, Inc. v. ITT Indus., Inc.*, 452 F.3d 1312, 1319 (Fed. Cir. 2006); *Rambus Inc. v. Hynix Semiconductor Inc.*, 569 F. Supp. 2d 946, 962 (N.D. Cal. 2008) ("In laying out the details of the original restriction requirement, the court recognizes its limited evidentiary significance.").

[60] *See* Docket No. 368-2 at col.8 ll.22-24.

[61] *See id.* at col.9 ll.5-6.

[62] *Id.* at col.12 ll.62-65.

[63] *See 3M Innovative Properties Co.*, 350 F.3d at 1373 (finding that prosecution history "cannot be used to limit the scope of a claim unless the *applicant* took a position before the PTO."(emphasis in the original)).

statements, they do not clearly show that the term "DMA CPU" was understood to include a DMA controller.[64]

During oral argument, TPL argued that the term "independently" in the original construction is unsupported.[65] The court agrees with this point. Even if the DMA CPU fetches and executes its own instructions, it cannot do so independently. The reason for putting the CPU and DMA CPU on the same chip is so they can work together.[66] Otherwise, the evidence in support of changing the court's prior construction is unpersuasive.

The court construes "separate DMA CPU" as "a central processing unit that accesses memory and that fetches and executes instructions directly and separately of the main central processing unit."

D. "supply the multiple sequential instructions"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
provide the multiple sequential instructions in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during a single memory cycle without using a prefetch buffer or a one-instruction-wide instruction buffer that supplies on instruction at a time	provide the multiple sequential instructions in parallel to said central processing unit integrated circuit during a single memory cycle

The parties ask the court to construe the phrase "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle," from claim 1 of the '749 patent. Judge Ware previously determined that this phrase was composed of commonly used words that the patentee intended to have their plain and ordinary meaning. Plaintiffs argue for a narrower construction based upon disavowals during reexamination while TPL argues for a broad construction. The parties specifically dispute what limitations the patent places on how the "multiple sequential instructions" are provided to the CPU.

[64] *See id.* at 1346-47 ("An applicant's silence in response to an examiner's characterization of a claim does not reflect the applicant's clear and unmistakable acquiescence to that characterization if the claim is eventually allowed on grounds unrelated to the examiner's unrebutted characterization.").

[65] *See* Docket No. 382 at 121-22.

[66] *See* Docket No. 368-2, Reexam. Cert., col.1 ll.22-24; Docket No. 368-2 at col.8 ll.22-24 (the DMA CPU "operates as a co-processor to the main CPU").

During reexamination, TPL unambiguously disavowed that instructions could be provided to the CPU one-by-one. The PTO issued a reexamination rejecting claims in the '749 Patent, including claim 1, based upon the "Edwards" patent[67] and an article by Doug MacGregor.[68] To distinguish the Edwards patent, TPL argued that in the Edwards patent, "instructions are supplied to a one-instruction-wide instruction buffer, one at a time," while for the '749 Patent "[f]etching multiple instructions into a prefetch buffer and then supplying them one at a time is not sufficient to meet the claim limitation—the supplying of 'multiple sequential instructions to a CPU during a single memory cycle.'"[69] Similarly, in distinguishing the invention in MacGregor, TPL wrote that "non-parallel supplying of instructions to the CPU is not supplying them to the CPU during a single memory cycle as required by the claim."[70] By this language, TPL clearly and unambiguously disavowed supplying instructions to the CPU one-by-one.

Plaintiffs also urge the court to find TPL disavowed specific structures or components in the above statements, but these statements as to structures are not clearly disavowals because they are made in the context of describing the prior art. There may be ways of incorporating such structures consistent with not supplying the instructions one-by-one.

Accordingly, the court construes the phrase "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle" as "provide the multiple sequential instructions in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during a single memory cycle."

E. "clocking said CPU"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
timing the operation of the CPU such that it will always execute at the maximum frequency possible, but never too fast	timing the operation of the CPU

[67] U.S. Patent No. 4,680,698.

[68] Doug MacGregor *et al.*, "The Motorola MC68020," IEEE Micro 101 (August 1984).

[69] Docket No. 358-3 at 27.

[70] *Id.* at 46.

The parties ask the court to construe "clocking said CPU," which appears in claims 1, 6, and 10 of the '336 Patent. Generally speaking, "clocking the CPU" refers to using the system clock to control the speed of the CPU. Judge Ware previously considered "clocking said CPU" and based upon the plain and ordinary meaning of the term, construed it as "providing a timing signal to said central processing unit." The court considered other language in the written description that suggested a more limited construction, but ultimately determined that the patentee had not "demonstrated a clear intention to limit the claim scope."[71] Similarly, Judge Ward construed a longer term[72] from claim 1 containing the term "clocking said CPU" as "an oscillator that generates the signal(s) used for timing the operation of the CPU."[73] In construing the term, Judge Ward similarly did not adopt the type of limiting language that Plaintiffs advocate.

As discussed above and explained in the patent, the disclosed invention uses a variable speed clock—a ring oscillator—that varies with temperature, voltage, and process. The specification states that "[b]y deriving system time from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast."[74] Plaintiffs argue that this is a clear limitation that should be read into the claims. In general, absent a clear intention to limit the scope of a claim, a description of an embodiment should not limit claim language that otherwise has a broader effect.[75] This rule applies even if the patent only describes a single embodiment.[76] Judge Ware previously considered and rejected Plaintiffs attempt to limit the claim based upon the specification and this court agrees. There is no support in the claim language itself for the requirement that the clock always forces the CPU to operate at its maximum frequency. The court finds that operating at

[71] Docket No. 336 at 17-18 (quoting *Innova/Pure Water*, 381 F.3d at 1117).

[72] Judge Ward construed "an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit."

[73] *Tech. Properties Ltd. v. Matsushita Elec. Indus. Co., Ltd.*, 514 F. Supp. 2d 916, 927 (E.D. Tex. 2007) aff'd sub nom., 276 F. App'x 1019 (Fed. Cir. 2008).

[74] *See* Docket No. 358-6 at col.16-17 ll.63-2.

[75] *See Innova/Pure Water*, 381 F.3d at 1117.

[76] *See id.*

the maximum frequency is merely the preferred embodiment and not the only manner in which the invention can operate.

Plaintiffs also try to introduce evidence from the prosecution history to support their argument. Although Plaintiffs quote a section from the prosecution history where the applicants used the magic words "the present invention," what the applicants disclosed is that the present invention includes a variable speed clock on the same microprocessor as the CPU and thus its speed will vary based upon environmental conditions.[77] This is exactly what is claimed in claim 1. The excerpt goes on to explain that one advantage of the variable speed clock is that it "allows the microprocessor to operate at its fastest safe operating speed,"[78] but again, this is just one embodiment and not necessarily a *requirement* of the invention. Plaintiffs' other citations to the prosecution history are similarly unconvincing.

Because the parties have not convinced the court that the prior construction was in error, the Court declines to change its construction. Accordingly, the court construes "clocking said CPU" as "providing a timing signal to said central processing unit."

IV. CONCLUSION

For the reasons set forth above, the court construes the claims as follows:

CLAIM TERM	CONSTRUCTION
"instruction register"	Register that receives and holds one or more instructions for supplying to circuits that interpret the instructions
"ring oscillator"	an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment
"separate DMA CPU"	a central processing unit that accesses memory and that fetches and executes instructions directly and separately of the main central processing unit
"supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle"	provide the multiple sequential instructions in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during

[77] *See* Docket No. 358-9 at 4-5.

[78] *Id.* at 5.

	a single memory cycle
"clocking said CPU"	Providing a timing signal to said central processing unit

Dated: August 21, 2013

PAUL S. GREWAL
United States Magistrate Judge

PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of **CERTAIN WIRELESS CONSUMER ELECTRONICS DEVICES AND COMPONENTS THEREOF**	**Inv. 337-TA-853**

ORDER NO. 31: [CORRECTED[1]] CONSTRUING THE TERMS OF THE ASSERTED CLAIMS OF THE PATENT AT ISSUE

(April 18, 2013)

[1] The parties' agreed construction for the term "external clock is operative at a frequency independent of a clock frequency of said variable speed clock" has been corrected.

PUBLIC VERSION

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PUBLIC VERSION

The following abbreviations may be used in this Markman Order:

JXM	Joint Exhibit
CXM	Complainants' Markman exhibit
CDXM	Complainants' demonstrative Markman exhibit
CMBr.	Complainants' initial Markman brief
CRMBr.	Complainants' reply Markman brief
RXM	Respondents' Markman exhibit
RDXM	Respondents' demonstrative Markman exhibit
RMBr.	Respondents' initial Markman brief
RRMBr.	Respondents' reply Markman brief
SMBr.	Commission Investigative Staff's initial Markman brief
SRMBr.	Commission Investigative Staff's reply Markman brief
Tr.	Markman hearing transcript
Stip.	Technology Stipulation
JL	Parties' Final Joint Submission Concerning Construction of Claim Terms From U.S. Patent No. 5,809,336, dated 3/12/13

I. INTRODUCTION.

The Commission instituted this Investigation pursuant to subsection (b) of Section 337 of the Tariff Act of 1930, as amended, to determine:

> whether there is a violation of subsection (a)(1)(B) of section 337 in the importation into the United States, the sale for importation, or the sale within the United States after importation of certain wireless consumer electronic devices and components thereof that infringe one or more of claims 1, 6, 7, 9-11, and 13-16 of the '336 patent and whether an industry in the United States exists as required by subsection (a)(2) of section 337.

77 Fed. Reg. 51572 (August 24, 2012).

The Notice of Investigation names Technology Properties Limited LLC and Phoenix Digital Solutions LLC of Cupertino, California and Patriot Scientific Corporation of Carlsbad, California as complainants and Acer, Inc. of Taipei, Taiwan; Acer America Corporation of San Jose, California; Amazon.com, Inc. of Seattle, Washington; Barnes and Noble, Inc. of New York, New York; Garmin Ltd of Schaffhausen, Switzerland; Garmin International, Inc. of Olathe, Kansas; Garmin USA, Inc. of Olathe, Kansas; HTC Corporation of Taoyuan, Taiwan; HTC America of Bellevue, Washington; Huawei Technologies Co, Ltd. of Shenzhen, China; Huawei North America of Plano, Texas; Kyocera Corporation of Kyoto, Japan; Kyocera Communications, Inc. of San Diego, California; LG Electronics, Inc. of Seoul, Korea; LG Electronics U.S.A., Inc. of Englewood Cliffs, New Jersey; Nintendo Co. Ltd. of Kyoto, Japan; Nintendo of America, Inc. of Redmond, Washington; Novatel Wireless, Inc. of San Diego, California; Samsung Electronics Co., Ltd., of Seoul, Korea; Samsung Electronics America, Inc. of Ridgefield Park, New Jersey; Sierra Wireless, Inc. of British Columbia, Canada; Sierra Wireless America, Inc. of Carlsbad, California; ZTE Corporation of Shenzhen, China; and ZTE (USA) Inc. of Richardson, Texas as respondents. (*Id.*) The Commission Investigative Staff ("Staff") of the Office of Unfair Import Investigations is also a party in this investigation. (*Id.*)

On March 5, 2013, the Administrative Law Judge held a Markman hearing in order to permit the parties to present their positions with respect to the interpretation of certain disputed claim language in the asserted patents. Complainants, Respondents, and Staff attended the Markman hearing.

After reviewing the parties' Markman briefs, presentations, and evidence, the Administrative Law Judge finds as follows.

The claim terms construed in this Order are done so for the purposes of this Section 337 Investigation. Only claim terms in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Vanderlande Indus. Nederland BV v. Int'l Trade Comm.*, 366 F.3d 1311, 1323 (Fed. Cir. 2004); *Vivid Tech., Inc. v. American Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999). Hereafter, discovery and briefing in this Investigation shall be governed by this construction of the claim terms. All other claim terms shall be deemed undisputed and shall be interpreted by the Administrative Law Judge in accordance with their ordinary meaning as viewed by a person of ordinary skill in the art.

II. RELEVANT LAW.

Any finding of infringement requires a two-step analysis. First, the asserted patent claims must be construed as a matter of law to determine their proper scope. Second, a factual determination must be made whether the properly construed claims read on the accused devices. *See Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 976 (Fed. Cir. 1995) (*en banc*), *aff'd*, 517 U.S. 370 (1996).

Claim construction begins with the language of the claims themselves. Claims should be given their ordinary and customary meaning as understood by a person of ordinary skill in the art, viewing the claim terms in the context of the entire patent. *Phillips v. AWH Corp.*, 415 F.3d 1303,

1312-13 (Fed. Cir. 2005). In some cases, the ordinary meaning of claim language is readily apparent and claim construction will involve little more than "the application of the widely accepted meaning of commonly understood words." *Id.* at 1314. In other cases, claim terms have a specialized meaning and it is necessary to determine what a person of ordinary skill in the art would have understood disputed claim language to mean by analyzing "the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, as well as the meaning of technical terms, and the state of the art." *Id.* (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1116 (Fed. Cir. 2004)).

The claims themselves provide substantial guidance as to the meaning of disputed claim language. *Id.* at 1314. "[T]he context in which a term is used in the asserted claim can be highly instructive." *Id.* Likewise, other claims of the patent at issue, regardless of whether they have been asserted against respondents, may show the scope and meaning of disputed claim language. *Id.*

With respect to claim preambles, a preamble may limit a claimed invention if it (i) recites essential structure or steps, or (ii) is "necessary to give life, meaning, and vitality" to the claim. *Eaton Corp. v. Rockwell Int'l Corp.*, 323 F.3d 1332, 1339 (Fed. Cir. 2003) (citations omitted). The Federal Circuit has explained that a "claim preamble has the import that the claim as a whole suggests for it. In other words, when the claim drafter chooses to use both the preamble and the body to define the subject matter of the claimed invention, the invention so defined, and not some other, is the one the patent protects." *Id.* (quoting *Bell Communications Research, Inc. v. Vitalink Communications Corp.*, 55 F.3d 615, 620 (Fed. Cir. 1995)). When used in a patent preamble, the term "comprising" is well understood to mean "including but not limited to," and thus, the claim is

open-ended. *CIAS, Inc. v. Alliance Gaming Corp.*, 504 F.3d 1356, 1360 (Fed. Cir. 2007). The patent term "comprising" permits the inclusion of other unrecited steps, elements, or materials in addition to those elements or components specified in the claims. *Id.*

In cases where the meaning of a disputed claim term in the context of the patent's claims remains uncertain, the specification is the "single best guide to the meaning of a disputed term." *Phillips*, 415 F.3d at 1321. Moreover, "[t]he construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction." *Id.* at 1316. As a general rule, however, the particular examples or embodiments discussed in the specification are not to be read into the claims as limitations. *Id.* at 1323.

The prosecution history may also explain the meaning of claim language, although "it often lacks the clarity of the specification and thus is less useful for claim construction purposes." *Id.* at 1317. The prosecution history consists of the complete record of the patent examination proceedings before the U.S. Patent and Trademark Office, including cited prior art. *Id.* It may reveal "how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be." *Id.*

If the intrinsic evidence is insufficient to establish the clear meaning of a claim, a court may resort[2] to an examination of the extrinsic evidence. *Zodiac Pool Care, Inc. v. Hoffinger Industries, Inc.*, 206 F.3d 1408, 1414 (Fed. Cir. 2000). Extrinsic evidence may shed light on the relevant art, and consists of all evidence external to the patent and the prosecution history, "including expert and inventor testimony, dictionaries, and learned treatises." *Phillips*, 415 F.3d at 1317. In evaluating expert testimony, a court should disregard any expert testimony that is conclusory or

[2] "In those cases where the public record unambiguously describes the scope of the patented invention, reliance on any extrinsic evidence is improper." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996).

"clearly at odds with the claim construction mandated by the claims themselves, the written description, and the prosecution history, in other words, with the written record of the patent." *Id.* at 1318. Furthermore, expert testimony is only of assistance if, with respect to the disputed claim language, it identifies what the accepted meaning in the field would be to one skilled in the art. *Symantec Corp. v. Computer Associates International, Inc.*, 522 F.3d 1279, 1290-91 (Fed. Cir. 2008). Testimony that recites how each expert would construe the term should be accorded little or no weight. *Id.* Extrinsic evidence is inherently "less reliable" than intrinsic evidence, and "is unlikely to result in a reliable interpretation of patent claim scope unless considered in the context of the intrinsic evidence." *Phillips*, 415 F.3d at 1318-19.

III. U.S. PATENT NO. 6,150,689

A. Overview

This Investigation concerns U.S. Patent No. 5,809,336, titled "High Performance Microprocessor Having Variable Speed System Clock" ("the '336 patent"), which resulted from U.S. Patent Application No. 484,918 filed on June 7, 1995. (JXM-0001.) The '336 patent is a division of Serial No. 389,334, filed on August 3, 1989 and issued as U.S. Patent No. 5,440,749. (*Id.*) The '336 patent issued on September 15, 1998 and names Charles H. Moore and Russell H. Fish, III as the inventors. (*Id.*) The patent was assigned to Patriot Scientific Corporation. (*Id.*; Complaint at ¶36; *id.*, Ex. 8.)

The '336 patent discloses a microprocessor system having (1) an on-chip variable speed clock and (2) a second independent clock connected to an input/output (I/O) interface. (Stip. at 2.) Microprocessors must operate over (1) temperature ranges, (2) voltage variations and (3) variations in semiconductor processing, each of which affects operating speed ("PVT parameters" for "process," "voltage" and "temperature"). (*Id.* (citing JXM-0001 at 16:44-53).) The '336 patent

discloses a microprocessor having a clock circuit and a CPU fabricated on the same substrate. (*Id.* (citing JXM-0001 at 16:56-58).) The '336 patent presents the following embodiment in Figure 17:

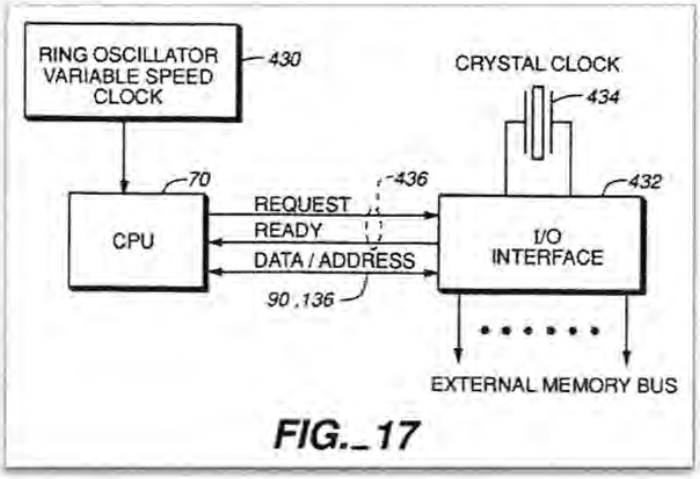


FIG._17

In the embodiment shown in Figure 17, CPU 70 operates asynchronously with I/O interface 432. (*Id.* (citing JXM-0001 at 17:14-19).) I/O interface 432 is controlled independently by crystal clock 434. (*Id.* (citing JXM-0001 at 17:17-19, 17:25-27).) The on-chip ring oscillator variable speed clock 430 clocks the CPU 70. (*Id.* (citing JXM-0001 at 16:59-60, 17:19-22, 17:32-34).)

Asserted claims 1, 6, 7, 9-11, and 13-16 of the '336 patent are shown below.

> 1. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit, and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein a clock signal of said

second clock originates from a source other than said ring oscillator variable speed system clock.

6. A microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.

7. The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

9. The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.

10. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock and wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock.

11. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein said central processing unit operates asynchronously to said input/output interface.

13. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;

an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and further wherein said central processing unit operates asynchronously to said input/output interface.

14. The microprocessor system of claim 13 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

15. The microprocessor system of claim 13 wherein said oscillator comprises a ring oscillator.

16. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying

> in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;
>
> connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and
>
> clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock, wherein said central processing unit operates asychronously to said input/output interface.

(JXM-0001 at 33:17-19, 33:23-24, Ex Parte reexamination Certificate at 1:59-3:26, 3:29-4:46.)

B. Level of Ordinary Skill in the Art

Claims should be given their ordinary and customary meaning as understood by a person of ordinary skill in the art. *Phillips*, 415 F.3d at 1312-13. Complainants' expert opines that a person of ordinary skill in the art with respect to the '336 patent would have a minimum of a bachelor's degree in electrical engineering and two to three years of experience in semiconductor design. (*See* Initial Report of Dr. Vojin G. Oklobdzija (Infringement and Domestic Industry) at 7.) Respondents' expert opines that the relevant level of ordinary skill in the art is a master's degree in electrical engineering, computer engineering, or a related field, and at least 5 years of experience in integrated circuit design, or a commensurate amount of relevant experience. (*See* Opening Expert Report of Eby G. Friedman, Ph. D Regarding U.S. Patent No. 5,809,336 at 23.) Upon consideration of these opinions and the technology at issue, the Administrative Law Judge finds that a person of ordinary skill in the art would have at least a bachelor's degree in electrical engineering, computer engineering, or a related field and at least 5 years of experience in integrated circuit design or a related field or a graduate degree in electrical engineering, computer

engineering, or a related field and at least 3 years of experience in integrated circuit design or a related field.

C. Agreed Constructions

1. Claims 1, 6, 10, 11, 13, 16—*"central processing unit"*

The parties agree that the term "central processing unit" in claims 1, 6, 10, 11, 13, and 16 of the '336 patent should be construed to mean "electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions." (JL at 1.)

2. Claims 1, 11—*"second clock independent of said ring oscillator variable speed system clock"*

The parties agree that the term "second clock independent of said ring oscillator variable speed system clock" in claims 1 and 11 of the '336 patent should be construed to mean "a second clock wherein a change in the frequency of either the second clock or ring oscillator system clock does not affect the frequency of the other." (JL at 2.)

3. Claims 1, 6, 10, 11, 13, 16—*"on-chip input/output interface"*

The parties agree that the term "on-chip input/output interface" in claims 1, 6, 10, 11, 13, and 16 of the '336 patent should be construed to mean "a circuit having logic for input/output communications, where that circuit is located on the same semiconductor substrate as the CPU." (JL at 2.)

4. Claims 6, 13—*"external clock is operative at a frequency independent of a clock frequency of said oscillator"*

The parties agree that the term "external clock is operative at a frequency independent of a clock frequency of said oscillator" in claims 6 and 13 of the '336 patent should be construed to mean "an external clock wherein a change in the frequency of either the external clock or oscillator does not affect the frequency of the other." (JL at 2.)

5. Claims 10, 16—*"external clock is operative at a frequency independent of a clock frequency of said variable speed clock"*

The parties agree that the term "external clock is operative at a frequency independent of a clock frequency of said variable speed clock" in claims 10 and 16 of the '336 patent should be construed to mean "an external clock wherein a change in the frequency of either the external clock or the variable speed clock does not affect the frequency of the other." (JL at 2.)

D. Construction of Disputed Claim Terms

1. Claims 1, 9, 11, 15—*"ring oscillator"*

The parties' proposed constructions for this term are as follows:

Respondents	Complainants	Staff
an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is: (1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters in the environment	interconnected electronic components comprising multiple odd numbers of inversions arranged in a loop, where three or more inversions are required to maintain an oscillating output	an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage, and process parameters in the environment

(CMBr. at 7; RMBr. at 56; SMBr. at 22-23.) There is no unique definition set forth in either the claims or in the specification of the patent. Rather, the specification says this: "The microprocessor **50** uses the technique shown in FIGS. **17-19** to generate the system clock and its required phases. Clock circuit **430** is the *familiar* 'ring oscillator' used to test process performance." (JXM-0001 at 16:54-55 (emphasis added).) Figure 18 of the patent illustrates the "[c]lock circuit **430,**" as shown here:

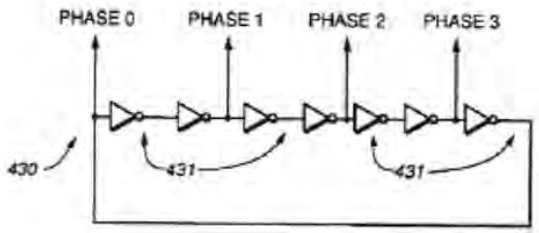


FIG._18

Complainants' arguments in support of their proposed construction

Complainants say a person of ordinary skill in the art would understand the term "ring oscillator" to mean "interconnected electronic components comprising multiple odd numbers of inverters arranged in a loop." (CMBr. at 7.) In so saying, Complainants refer to the claim construction that was previously made by a judge in a parallel federal district court case involving some of the parties in this investigation: "an oscillator having multiple odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment." (*Id.* at 6-7 (citing CXM-0003[3] at 2).)

Complainants say the oscillation of the claimed device depends on there being at least three inverters for output. (*Id.* at 8 (citing Oklobdzija Decl. at ¶¶ 9-10).) Complainants note that the claimed device oscillates because its signals, as they move around the loop or ring of inverters, alternates between 1and 0. (*Id.*) A sample signal taken at any point in the loop of inverters will be opposite one taken there in a succeeding cycle. This would not be the case if there were an even number of inverters in the loop—in that instance, the signal would be the same for every cycle. (*Id.* (citing Oklobdzija Decl. at ¶ 7).) Furthermore, a ring oscillator will not work with just a single

[3] Renumbered as JXM-0009 (Claim Construction Order of Paul S. Grewal, dated Dec. 4, 2012, in Case No. 5:08-cv-00877 PSG: Acer, Inc. et al. v. Technology Properties, Ltd., et al.)

inverter. (*Id.* (citing Oklobdzija Dec. at ¶¶ 7, 15).) Complainants say that the ring oscillator of the '336 patent, by inclusion of its circuitry within the wider network of integrated circuitry for the microprocessor, can be used for generating a clock signal for the central processing unit. (*Id.* at 9 (citing JXM-0001 at claims 1 and 11).)

There is nothing within the context of the asserted claims that suggests that the claimed ring oscillator has to be non-controllable or necessitates adding the words "variable based on the temperature, voltage, and process parameters in the environment," argue the Complainants. (*Id.*) Nor does anything expressed in the claims preclude an additional element for managing the oscillator clock, according to Complainants. (*Id.*) As for the other limitation proposed by Respondents—that the oscillation of the ring oscillator clock is variable based on temperature, voltage, and processing characteristics—Complainants argue that this verbiage adds nothing to the meaning of the term ring oscillator and diverges from the gist of the claim itself, thereby creating ambiguity. (*Id.*)

Complainants further argue that the specification supports their contention that, to a person of ordinary skill in the art, the term ring oscillator, as it pertains to the asserted claims of the '336 patent, should be understood according to its common and ordinary meaning. (*Id.*) The specification states that the "[c]lock circuit **430** is the familiar 'ring oscillator'" used to test process performance. (*Id.* (citing JXM-0001 at 16:54-58).) Also, the specification says the ring oscillator clock is "fabricated on the same silicon chip as the rest of the microprocessor," as illustrated in Figure 17 of the patent, while Figure 19 discloses a sampling of a clock signal over time at various points, or phases, which are depicted in Figure 18. (*Id.* at 9-10.)

Respondents' arguments in support of their proposed construction

Respondents say that in order to overcome a rejection of the asserted claims, the patent owner (Charles Moore)[4] argued that the voltage-controlled oscillator ("VCO") of a prior patent, U.S. Patent No. 4,689,581 ("Talbot"), did not teach the "ring oscillator" claimed in the '336 patent. (RMBr. at 57.) Respondents quote the following comment of the examiner in support of their position:

> Continuing, the patent owner further argued that the reference of Talbot does not teach of a "ring oscillator." The patent owner discussed features of a ring oscillator, such as being non-controllable, and being variable based on the environment. The patent owner argued that these features distinguish over what Talbot teaches.

(*Id.* (citing JXM-0005[5] (Interview Summary, Feb. 12, 2008, Control No. 90/008,227)).) In light of this written comment by the examiner, which Respondents describe as disavowing arguments, Respondents maintain that the term "ring oscillator" must include the limitations "non-controllable" and "variable based on temperature, voltage, and process parameters in the environment." (*Id.*) According to Respondents, Federal Circuit law is clear that "[a]rguments made during the prosecution of a patent application are given the same weight as claim amendments." (*Id.* at 57-58 (citing *Elkay Mfg. v. Ebco Mfg. Co.*, 192 F.3d 973, 979 (Fed. Cir. 1999)).) They say it is black letter law that a court "cannot construe the claims to cover subject matter broader than that which the patentee itself regarded as comprising its invention and represented to the PTO." (*Id.* at 58 (citing *Microsoft Corp. v. Multi-Tech Sys., Inc.*, 357 F.3d 1340, 1349 (Fed. Cir. 2004)).) Respondents note that "[t]he purpose of consulting the prosecution

[4] JXM-0014 at TPL-853_02954311. Although Respondents say it was TPL (Technology Properties Limited) that did this, the exhibits identify Charles Moore as the owner and party involved. Charles Moore and Russell Fish are identified in the patent as the inventors, and Patriot Scientific Corporation is identified as assignee. (JXM-00014 at TPL853_00000003.)

[5] Renumbered JXM-0014.

history in construing a claim is to 'exclude any interpretation that was disclaimed during prosecution.'" (*Id.* (citing *Chimie v. PPG Indus. Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005)).) They say that "where the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender." (*Id.* (quote *Chimie*, 402 F.3d at 1384).) Additionally, they cite and quote *Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1312, 1325 (Fed. Cir. 2002): "Explicit arguments made during prosecution to overcome prior art can lead to narrow claim interpretation because 'the public has a right to rely on such definitive statements made during prosecution.'" (*Id.*)

Respondents argue that an examiner's interview summary is a proper basis for finding a disavowal of claim scope because it expressly reflects what the patent owner argued. (*Id.*) According to Respondents, the examiner had no motive to misstate the position that was being advocated by the patent applicants in pursuit of the patent. (*Id.* at 58-59.) Moreover, say the Respondents, the applicants did not dispute the accuracy of any aspect of the examiner's summary of what had been discussed. (*Id.* at 59.) Thus, the disavowal recorded by the examiner remains effective even though it occurred during the reexamination of the '148 patent, because that patent shares the same specification as, and is directly related to, the '336 patent, both patents claiming a ring oscillator. (*Id.*)

Respondents further argue that the applicants' disavowals in connection with the professed ring oscillator being non-controllable and variable based on the temperature, voltage, and process parameters in the environment was essentially a shorthand summary of numerous arguments made by the applicants during the original prosecution of the patent, in order to overcome multiple prior art references, and underscores the fact that the ring oscillator is indeed non-controllable inasmuch

as its variation in frequency is a result of environmental factors. (*Id.*) During the prosecution of the '336 patent, the applicants repeatedly drew a distinction between deliberate control of an oscillator's frequency by means of an input signal, such as a crystal or some other component of the system, and its frequency variations stemming from the environmental factors of temperature, voltage, and process, according to Respondents. (*Id.* at 60.) Respondents say the patent owner consistently characterized the claimed variable speed clock, ring oscillator variable system clock, and oscillator as environmentally dependent and expressly distinguished prior art clocks that were controlled, whether through clock control signals, frequency control information, or command inputs, and therefore it comes as no surprise that during reexamination the owner again emphasized the features of a ring oscillator as being non-controllable and variable based on the environment. (*Id.* at 61-62.)

Staff's arguments in support of its proposed construction

Staff says that the '336 patent shares essentially the same specification and drawings as U.S. Patent No. 6,598,148 ("the '148 patent), and during reexamination of the '148 patent the applicants argued that a prior art patent, U.S. Patent No. 4,689,581 ("Talbot") does not teach a ring oscillator, even though Talbot teaches a voltage-controlled oscillator that has a multiple odd number of inversions arranged in a loop. (SMBr. at 23-24.) According to Staff, Talbot discloses three inversions arranged in a loop, yet the '336 patent applicants made clear that Talbot does not teach a ring oscillator and therefore he disclaimed the subject matter disclosed in Talbot. (*Id.* at 24.) The only question, argues Staff, is the scope of the disclaimer. (*Id.*)

Staff criticizes Respondent's use of the term "non-controllable" because the patentee did not argue that "controllability" was the reason that Talbot's oscillators were not the claimed ring oscillators. (*Id.*) Furthermore, argues Staff, Talbot can be distinguished fully based on the fact

that the frequency of the variable speed ring oscillator clock of the '336 patent is determined, not by an external crystal or off-chip components but by "the parameters of temperature, voltage, and process" as described in the specification and articulated throughout the intrinsic record. (*Id.* at 24-25.)

For these reasons, Staff submits that the term ring oscillator should be interpreted to mean "an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment." (*Id.* at 25.)

Administrative Law Judge's construction

The Administrative Law Judge finds that the term "ring oscillator" as it appears in the asserted claims was not invested with any unique or special meaning by the inventor of the '336 patent. The specification, as has been pointed out by others, says that the "[c]lock circuit **430** is the *familiar* 'ring oscillator' used to test process performance." (JXM-0001 at 16:56-57 (emphasis added).) Thus a person of ordinary skill in the art of the '336 patent would, by the lights of all parties to this investigation, know and understand what a ring oscillator is. There is no legal basis for Respondent's inclusion of the word "non-controllable," as pointed out by both Complainants and Staff. The Federal Circuit has pointed out that "[a]lthough…the prosecution history is always relevant to claim construction, it is also true that the prosecution history may not be used to infer the intentional narrowing of a claim absent the applicants' clear disavowal of claim coverage, such as an amendment to overcome a rejection." *Amgen Inc. v. Hoechst Marion Roussel, Inc.*314 F.3d 1313, 1327 (Fed. Cir. 2003). The court further said: "No such clear disavowal occurred here." (*Id.*) More specifically, the court in *Gemstar-TV Guide Intern., Inc. v. International Trade Comm'n,*_383 F.3d 1352, 1375 (Fed. Cir.2004) said: "Gemstar's statements in the prosecution

history do not indicate a disavowal or disclaimer of claim scope (citation omitted), but merely provide an example to illustrate differences between the invention and the prior art. In essence, Gemstar stated only that the [prior-art] reference was incapable of performing a certain type of search, not that the scope of the claimed invention was limited to that particular type of search. Contrary to the ITC's holding, the prosecution history did not limit the '121 patent to that particular sequence of logical searching." The same thinking holds true with respect to the prosecution history of the '336 patent and the alleged disavowals referenced by the Respondents.

On the other hand, Complainant's substitution of "interconnected electronic components" is unnecessary and uninformative for purposes of understanding what a person of ordinary skill in the art would apprehend a ring oscillator to be. Integrated circuits in general consist of interconnected electronic components. So the phrase "integrated electronic components" does not aid in describing what a person of ordinary skill in the relevant art would understand a ring oscillator to be. The purpose of claim construction is to clarify or settle, to the extent necessary to resolve the competing contentions of the parties, asserted claim terms, and not simply to reformulate the inventor's words in alternative ways. Further, the latter portion of Complainant's construction is encompassed in the earlier portion: "multiple" by definition means more than one, and "odd numbers" by definition excludes the quantity two, which is the only number other than one that is less than three. Therefore, the last clause in Complainants' proposed construction is tautological.

As for Staff's construction, its distinctive verbiage is the clause "wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment." However, this, in its own way, is superfluous too, because later in the claim it is stated: "and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations

and due to at least operating voltage and temperature of said single integrated circuit". Therefore, this notion is expressed in subsequent language of the claim and does not need to be prefaced in order to understand the term "ring oscillator."

For the foregoing reasons, the Administrative Law Judge concludes that the term "ring oscillator" means "an oscillator having a multiple, odd number of inversions arranged in a loop."

2. Claims 1, 11—*"an entire ring oscillator variable speed system clock in said single integrated circuit"*

The parties' proposed constructions for this term are as follows:

Respondents	Complainants	Staff
a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an external crystal/ clock generator to generate a clock signal	a ring oscillator, variable speed system clock, wherein the ring oscillator is located entirely on the same semiconductor substrate as the central processing unit	a ring oscillator variable speed system clock that includes all components that determine clock frequency located on the same semiconductor substrate as the CPU

(CMBr. at 13; RMBr. at 12; SMBr. at 7.)

Complainants' arguments for their proposed construction

Complainants say the claims simply discuss a ring oscillator with circuitry that is entirely integrated in the same semiconductor as the central processing unit, or CPU. (CMBr. at 13.) They say there is nothing in the claim language that suggests that the ring oscillator cannot use a "control signal" or reference an "external crystal." (*Id.*) Complainants contend that their proposed construction is consistent with the specification of the '336 patent, which says: "Clock circuit is the familiar 'ring oscillator"…fabricated on the same silicon chip as the rest of the microprocessor." (*Id.* at 13-14 (citing JXM-0001 at 16:56-58).) Further, they argue that their construction is supported by the prosecution history, noting that the patent applicants added the word "entire" during the initial prosecution of the '336 patent in an attempt to distinguish it from a

prior patent, U.S. Patent No. 4,503,500 ("Magar"). They said Magar does not have an oscillator integrated on the same silicon die as the CPU and therefore the patent applicants observed that the "entire oscillator" of the '336 invention needs to be physically integrated on the same silicon die as the CPU. (*Id.* at 14.)

Complainants say Respondents' construction, which precludes use of any external auxiliary crystal/clock in conjunction with the "entire ring oscillator variable speed system clock," mischaracterizes Magar and the gist of the applicants' statements in that regard because Magar's oscillator was not on the same integrated circuit as the CPU. According to the '336 invention, the claimed oscillator is an entire ring oscillator that is integrated on the same silicon die as the CPU, but there is no clear disavowal in the file history of the '336 patent that prohibits the use of an off-chip crystal for a reference signal, especially when the "entire ring oscillator" is fully integrated on the chip. (*Id.*) Similarly, according to Complainants, Respondents' attempt to add a limitation that excludes a control signal has no basis in the file history's discussion of "entire" or anywhere else in the internal record of the '336 patent. (*Id.*) Therefore, argue Complainants, there is no clear disavowal of the use of a "control signal." (*Id.*)

Respondents' arguments for their proposed construction

Respondents say the essence of the parties' dispute regarding this claim term, and those other claim terms with similar language, focuses on what the applicants needed to disclaim in order to succeed in getting their patent application issued. (RMBr. at 13.) Respondents contend that their constructions embody the clear disavowals of claim scope by the applicants during the prosecution of the '336 patent and are consistent with the teachings and criticisms of the prior art expressed in the specification. (*Id.*) These "unambiguous disclaimers and teachings" establish that the claimed "entire oscillator" and "entire clock" do not rely on any off-chip crystals, off-chip

clock generators, or control signals. (*Id.*) Respondents say that, in contrast, Complainants' constructions ignore these clear disclaimers and teachings and fail to define what it means for a clock oscillator to be located "entirely" on the same substrate as the CPU. (*Id.*) Because the applicants clearly and unambiguously disclaimed an on-chip clock or oscillator that relies on external off-chip crystals and off-chip clock generators, Respondents argue that their construction, which embodies these disclaimers, should be adopted. (*Id.*)

Respondents say a key feature of the asserted claims is the requirement that the entire variable speed clock or oscillator be located on the same integrated circuit substrate as the CPU that is to be clocked, without having to rely on any external, fixed-frequency source, such as a crystal. (*Id.* at 14.) Consequently, the speed of the variable speed clock and the processing frequency capability of the CPU at any point in time are determined by the process, voltage, and temperature of the integrated circuit. (*Id.* (citing JXM-0001 at 16:59-60, 65-67, 17:5-10, 19-22).) The purported result of this arrangement, say Respondents, is that the performance of the CPU is optimized so that it "will always execute at the maximum frequency possible, but never too fast." (*Id.* (citing JXM-0001 at 16:67-17:2).)

Respondents say the language of the asserted claims and the teachings of the specification describe a purported improvement over the prior art method of clocking a CPU with a fixed clock whose frequency is controlled by an external fixed-speed crystal or clock generator. The specification of the '336 patent makes note that a fixed-speed clock is always set at a frequency well below the maximum potential frequency at which the CPU could operate under the optimal process, voltage, and temperature conditions because, by definition, a fixed-speed clock cannot vary in speed in response to such conditions. (*Id.* (citing JXM-0001 at 16:44-53).) This less-than-optimal design is necessary in order to adapt to instances when the CPU is operating

under the worst of conditions with respect to process, voltage, and temperature. (*Id.*) Setting the frequency of the system at a lower-than-optimal level is inefficient, according to the teaching of the '336 patent, which the claimed invention seeks to overcome by fabricating the CPU and its clock entirely on the same substrate, so that PVT conditions will affect both the CPU and the clock alike, free of control from any external fixed-speed clocking mechanisms. (*Id.* (citing JXM-0001 at 16:44-17:10, 19-22).) Thus, the frequencies of the CPU and clock will automatically vary in response to changes in consequential PVT factors. (*Id.* at 14-15.) In light of the criticisms that were made in the '336 patent in this regard, a proper construction should account for such disclaimers because the Federal Circuit has recognized that a correct claim construction excludes from the scope of the claims those features that the specification criticizes and allegedly overcomes. (*Id.* at 15 (citing *Chicago Board Options Exch. Inc. v. Int'l Secs. Exch., LLC,* 677 F.3d 1361, 1372 (Fed. Cir. 2012)).)

Respondents point to the fact that during the prosecution of the '336 patent the applicants repeatedly distinguished their purported invention from the prior art on the basis that that their on-chip clock and oscillator do not rely on external crystals or frequency generators, as the prior art does, and therefore a proper construction should acknowledge and express this disclaimer. (*Id.*) Specifically, during the prosecution of the '336 patent the examiner issued a non-final rejection in light of Figure 2a of Magar. In his rejection, the examiner said the "CLOCK GEN" (clock generator) circuitry disclosed in that figure is fabricated on the same microprocessor substrate as the CPU, as is required in the claims of the '336 patent. (*Id.* (citing JXM-0002 at TPL-85300002433-36).) In response, the applicants attempted to distinguish Magar on the basis that an external off-chip crystal drives the clock that is disclosed in Magar. (*Id.* at 16 (citing JXM-0002 at TPL85300002426).) The applicants also emphasized that there is a difference

between their claimed variable speed clock and the combination of a clock generator and external clock disclosed in Magar, say Respondents. (*Id.* at 16-17 (citing JXM-0002 at TPL85300002427-28).) Thus, says Respondents, in their first amendment during the course of prosecution the applicants expressly and unambiguously disclaimed clocks and oscillators that rely on an external crystal for frequency control. (*Id.* at 17.)

According to Respondents, because the patent examiner was still not convinced by this attempt to distinguish Magar, the applicants further amended their claims to explicitly require that the entire oscillator/clock be included on the same integrated circuit substrate as the CPU. (*Id.* (citing JXM-0002 at TPL85300002399-400).) Also, the applicants further attempted to distinguish Magar from their claimed invention by arguing that Magar's clock generator could not operate properly without the use of an external component, such as a crystal, and in so doing, directed the examiner to Magar's disclosure that "chip 10 includes a clock generator 17 which has two external pins, X1 and X2, to which a crystal, or external generator, is connected. (*Id.* (citing JXM-0002 at TPL85300002402).) Because Magar does not disclose what components are included in its clock generator or how it uses the signal from the crystal, the only basis for the applicants' disclaimers is Magar's reliance on the external crystal or clock generator, regardless of how the signal supplied by the external crystal or clock generator is used, say Respondents. (*Id.* at 17-18.) Further confirming the scope of their clear disclaimer, the applicants rejected any dependence on an external crystal by telling the examiner that "[w]hile most of Magar's clock (generator) circuitry is on the IC, the entire oscillator, which because it requires an external crystal, is not." (*Id.* at 18.) Once again, according to Respondents, the applicants expressly disclaimed clocks and oscillators that rely on external crystal, but this time they went even further by

disclaiming reliance on an external crystal generally, and not just for purposes of controlling frequency. (*Id.*)

The applicants reinforced this disclaimer by explaining and characterizing "the essential difference" between Magar's fixed-frequency clock and the variable-speed clock shown in Figure 18 of the '336 patent this way:

> The signals PHASE 0, PHASE 1, PHASE 2, and PHASE 3 in Applicants Fig 18 are synonymous with Q1, Q2, Q3 and Q4 depicted in Magar Fig. 2a. The essential difference is that the frequency or rate of the PHASE 0, PHASE 1, PHASE 2 and PHASE 3 signals is determined by the processing and/or operating parameters of the integrated circuit containing the Fig. 18 circuit, while the frequency or rate of the Q1, Q2, Q3 and Q4 signals depicted in Magar Fig. 2A are determined by the fixed frequency of the external crystal connected to the circuit portion outputting the Q1, Q2, Q3, and Q4 signals shown in Magar Fig. 2a.

(*Id.* (citing JXM-0002 at TPL85300002402).) Respondents say the applicants for the'336 patent concluded their arguments to the examiner by distinguishing their invention from an external crystal used for frequency control or oscillation by saying "[t]he Magar teaching…is specifically distinguished from the instant case in that it is both fixed frequency (being crystal based) and requires an external crystal frequency generator." (*Id.* at 18-19.)

The actions of the applicants in support of the '336 patent are clear in their declarations that the invention requires an "entire" on-chip clock or oscillator, which cannot rely on an external crystal or frequency generator, say Respondents. (*Id.* at 19.) Magar's clock generator was differentiated from the '336 patent by the applicants because it is not an "entire" clock but, instead, relies on an external crystal or a frequency generator. According to Respondents, the claimed "entire" clock and "entire" oscillator cannot be construed to encompass a reliance on an external crystal or frequency generator. (*Id.* at 19-20 (citing *Southwall Tech., Inc., v. Cardinal JG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995); *Rheox, Inc.*, 276 F.3d at 1325; *Gillespie v. Dywidag, Systs. Int'l.*

USA, 501 F.3d 1285, 1291; *Computer Docking Station Corp. v. Dell, Inc.*, 519 F.3d 1366, 1379 (Fed. Cir. 2008); *Am. Piledriving Equip. v. Geoquip, Inc.*, 634 F.3d 1324, 1336 (Fed. Cir. 2011); *Seachange Int'l, Inc. v. C-COR, Inc.*, 413 F.3d 1361, 1372-75 (Fed. Cir. 2005)).) Moreover, argue Respondents, regardless of whether either or both of these arguments was successful, or even necessary, in convincing the examiner to allow the sought-after claims, the public is entitled to rely on them. (*Id.* at 20 (citing *Elkay Mfg.*, 192 F.3d at 979).)

Respondents say that, in addition to disclaiming reliance on an external crystal or clock generator, the applicants repeatedly, clearly, and unambiguously disclaimed reliance on control signals for controlling the clock. (*Id.* at 20-21.) The first of these disclaimers concerned the examiner's rejection of the claims in light of U.S. Patent No. 4,670,837 to Sheets ("Sheets"). (*Id.* at 21.) The named inventors distinguished their invention from microprocessors that rely on frequency control information from an external clock source. (*Id.* (citing JXM-0002 at TPL85300002473).) Because the applicants referred to the "present invention" in making this disclaimer, it applies to all of the claims of the '336 patent, according to Respondents. (*Id.* (citing *Ballard Med. Prods. v. Allegiance Healthcare Corp.*, 268 F.3d 1352, 1360-62 (Fed. Cir. 2001)).)

In response to a subsequent rejection, the applicants went further and disclaimed the use of controlled oscillators altogether, regardless of whether the control is on the chip or not:

> Even if the examiner is correct that the variable clock in Sheets is in the same circuit as the microprocessor of system 100, that still does not give the claimed subject matter. In Sheets, a command input is required to change the clock speed.

(*Id.* (citing JXM-0002 at TPL85300002449).) According to the applicants' actions in this regard, simply having a CPU clock on the chip is not enough to meet the claimed invention because controlling the on-chip ring oscillator's speed by use of a command signal "does not give the claimed subject matter." (*Id.* (citing JXM-0002 at TPL85300002449).) In that same amendment,

the applicants left no doubt that, unlike "all cited references," the on-chip clock or on-chip oscillator of the invention is completely free of inputs and extra components:

> Crucial to the present invention is that …when fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together. This differs from all cited references in that…the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so.

(*Id.* at 21-22 (citing JXM-0002 at TPL85300002450).) This statement confirms the applicants' disclaimer of any reliance on control signals, argue Respondents. (*Id.* at 22.) Therefore, their constructions correctly include, and Complainants' constructions incorrectly ignore, a requirement that the clock or oscillator "not rely on…a control signal to generate a clock signal." (*Id.*)

Respondents call attention to the fact that the '336 patent was the subject of prior litigation in the United States District Court for the Eastern District of Texas, in which case the presiding judge construed the term "entire ring oscillator variable speed system clock in said single integrated circuit" as recited in claim 1 this way: "a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not directly rely on a command input control signal or an external crystal/clock generator to generate a clock signal." (*Id.* at 23 (citing RXM-2 at 11-12 (Markman Order in *Tech Props. Ltd. v. Matsushita Elec. Indus. Co., Ltd.*, 54 F.Supp. 2d 916, 926 (E.D. Tex. June 15, 2007))).) Respondents quote the district court judge's statement that he "agrees with the defendants that the applicant disclaimed the use of an input control signal and an external crystal/clock generator to generate a clock signal." (*Id.*) Respondents argue that their proposed construction largely mirrors the district court judge's construction. (*Id.*)

According to Respondents, Complainant Technical Properties Limited ("TPL") has itself embraced the Texas district court judge's construction, thereby recognizing that a clear disclaimer narrows the claim scope and that the applicants disclaimed the use of an external crystal/clock or external control signals for controlling the oscillator or clock. (*Id.* at 24.) In a pending federal district court case between TPL and HTC, Acer, and Gateway in the Northern District of California (Case Nos. 5:08-cv-00877, 5:08-cv-0082, 5:08-cv-05398) TPL asked the court to adopt the Texas court judge's prior construction for the three disputed claim limitations that include the word "entire." (*Id.* (citing RXM-0003 (Joint Claim Construction Statement at Ex. B. Rows 19, 23, and 28)).) According to Respondents, it is unfairly prejudicial to them and the public for TPL to argue for construction of terms a certain way in one case and another, contrary, way in a co-pending case. (*Id.*)

Respondents say the Texas district judge's construction differs from theirs in two ways. First, it adds the word "directly" as a qualifier to the term "rely on," and second, it adds "command input" as a qualifier of "control signal." According to Respondents, the Texas court's claim construction order does not explain why its construction includes these qualifiers or what they mean; nor would a person of ordinary skill in the art understand what "directly rely on" means in the context of the claims. (*Id.* at 24-25 (citing RXM-0004 (Declaration of Dr. Vivek Subramanian in Support Respondents' Initial Markman Brief) at ¶¶ 9-10).) They argue that nothing in the prosecution history or in the patent itself limits either of the applicants' disclaimers in the manner described in the Texas court's construction, noting that the applicants explained that "Magar…is specifically distinguished from the instant case in that it is both fixed frequency (being crystal based) and requires an external crystal or external frequency generator." (*Id.* (citing JXM-0002 at TPL85300002403).) There is no suggestion of a "direct" reliance on an external crystal by reason

of this statement, argue Respondents. (*Id.*) Similarly, they say, nothing in the following statement by the applicants limits the scope of the disclaimer to "direct" reliance on an external crystal: "one of ordinary skill in the art should readily recognize that the speed of the CPU and clock do not vary together due to manufacturing variation, operating voltage, and temperature of the IC in the Magar processor….This is simply because the Magar microprocessor clock is frequency controlled by a crystal which is also external to the microprocessor." (*Id.* (citing JXM-0002 at TPL85300002427).) Nor, argue Respondents, does this statement limit the frequency control to direct control, and in this regard, Magar is silent as to the specific components that constitute the "clock generator" and how these components interact with the crystal inputs, much less specify that the components are controlled "directly" by control signals. (*Id.*) Similarly, when the applicants told the examiner that the "present invention…differs from all cited references in that…the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so," they disclaimed all manual or programmed control signals, not just "command input" control signals. (*Id.* at 25-26 (citing JXM-0002 at TPL85300002429).) Therefore, argue Respondents, while the Texas court correctly recognized the external crystal/clock generator and control signal disclaimers, the "directly" and "command input" qualifiers in that constructions should not be adopted for purposes of this investigation. (*Id.* at 26.)

Staff's arguments for its proposed construction

Staff notes that during prosecution of the application that resulted in the '336 patent, the applicants amended the claims so as to distinguish Magar, which discloses an on-chip clock generator that relies on an off-chip component, an external crystal, to determine clock frequency and which the applicants alleged was distinct from their invention. (SMBr. at 8 (citing JXM-0002

at TPL85300002401-02).) Similarly, in the course of distinguishing the patent to Sheets, the applicants asserted:

> The present invention does not...rely upon provision of frequency control information to an external clock, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, since the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g. temperature) affecting circuit performance.

(*Id.* (citing JXM-0002 at TPL85300002473).)

According to Staff, Complainants' proposed construction is improper to the extent it fails to reflect these disclaimers. Staff says that, while Respondents' proposed construction appears to accurately capture the applicants' clear disclaimer, Respondents still have not offered a construction of the term "entire." Staff says that incorporating a proper construction of the term "entire" excludes what was disclaimed by the applicants because the prior art that they distinguished does not disclose an entire oscillator in the same integrated circuit as a microprocessor. (*Id.* at 9.) Staff says that both Magar and Sheets disclose oscillators relying on off-chip components to determine frequency, and therefore, Staff's construction better captures the meaning of the disputed phrases as they would be understood by a person of ordinary skill in the art. (*Id.*)

Complaints' response to Respondents and Staff

Complainants maintain that the word "entire" refers to the on-chip circuitry that is used to generate the clock signal, having recognized that traditional microprocessor systems were designed such that their central processing units would operate under worse case conditions, given wide temperature and voltage swings and semiconductor processing variations. (CRMBr. at 9

(citing JXM-0001 at 16:48-53).) Specifically, they argue, traditional CPUs relied on off-chip, fixed-speed crystals or clock generators to generate the clock signal; however, the CPU's speed capability was tied to processing variances and voltage and temperature swings. (*Id.* at 9-10.) For example, the external clock could not assume that the CPU could operate at a particular speed, because the CPUs capabilities were variable. (*Id.* at 10.) Therefore, the CPU had to be clocked at far less than its maximum operating capability to account for times when it would operate under worse case conditions. But in order to enhance CPU performance, the inventors of the '336 patent designed their microprocessor system so that the circuitry that generates the CPU clock "system clock" (ring oscillator, oscillator, variable speed clock) is fabricated on the same silicon chip as the rest of the microprocessor. (*Id.* (citing JXM-0001 at 16:57-58).) The preferred embodiment identifies the ring oscillator of the invention as the "system clock," argue Complainants. (*Id.* (citing JXM-0001 at 16:54-56).) And the terms "oscillator" and "variable speed clock" each refers to the on-chip oscillators that generate the CPU clock. (*Id.*) Because the on-chip oscillator is fabricated of transistors on the same substrate as the rest of the microprocessor, the transistors of the oscillator and the CPU will be similarly affected by manufacturing process variances, and voltage and temperature swings. (*Id.* (citing JXM-0001 at 16:63-17:10).)

Complainants say that each claim of the '336 patent includes a limitation requiring that the oscillator be deposed on the same integrated circuit as the CPU. (*Id.* at 10-11.) In each case, the claims make clear that it is the transistors or electronic components of the circuitry that generate the clock signal for the CPU that must be on the same substrate as the CPU, argue Complainants. (*Id.* at 11.) They say that during the prosecution of the '336 patent, the then-pending claims were rejected as obvious over Magar in view of U.S. Patent 4,627,082 ("Pelgrom"), and in response, the applicants, in order "to sharpen the distinction over the prior art," rewrote the independent claims

to add the word "entire," thus "to specify that the entire ring oscillator variable speed clock, variable speed clock, or oscillator be provided in the integrated circuit." (*Id.* (citing CXM-0016 (2/8/98 Amendment) at 3).) In distinguishing the invention from the prior art, the applicants wrote this:

> Because the prior art does not provide an entire ring oscillator variable speed system clock, variable speed clock or oscillator in the integrated circuit, in that the prior art circuits require an external crystal, the prior art fails to teach or suggest the invention as now claimed.

(*Id.* (citing CXM-0016 at 3).) Therefore, reason Complainants, the phrase "entire ring oscillator variable speed system clock" in claims 1 and 11 is properly construed to mean the ring oscillator, which is inherently variable in speed, on the integrated circuit which generates the system clock. (*Id.*) This construction, they argue, is supported by the '336 patent specification, which teaches that the "[c]lock circuit is the familiar 'ring oscillator'…fabricated on the same silicon chip as the rest of the microprocessor." (*Id.* (citing JXM-0001 at 16:56-58).)

Complainants argue that, contrary to Respondents' argument, there is nothing in the patent specification that comes close to a disclaimer of all uses of off-chip crystals or clock generators; moreover, the patent does not, as Respondents contend, criticize any and all uses of the external crystals and control signals. (*Id.*) Instead, according to Complainants, the patent teaches that, by clocking the CPU using an oscillator that is disposed on the same chip as the CPU, thus enabling both components to vary with PVT parameters, the speed of the CPU need not be fixed to the worse case conditions affecting the CPU. (*Id.* at 12.)

As for the prosecution history with respect to Magar, Complainants argue that Respondents repeatedly mischaracterize the prosecution history in order to argue that all use of an external crystal and frequency generators was disclaimed by the applicants for the '336 patent. (*Id.* at

12-13.) In particular, the Respondents assert that Magar teaches an oscillator as disclosed by an external crystal and an on-chip oscillator disclosed by the "clock gen" block. However, argue Complainants, in the file history, the applicants pointed out that Magar disclosed only one oscillator circuit, which was embodied by the external crystal. (*Id.* at 12-13.) Complainants say Respondents misuse this assertion, taken out of context, to mischaracterize the comments made by the applicants and in so doing assert that the applicants distinguished their invention from the prior art on the basis that their on-chip oscillator does not rely on an external crystal or frequency generator, without pointing out the applicants really distinguished their invention from the prior art system because Magar, unlike the invention, only had an external crystal oscillator for generating the clock signal for the system clock. (*Id.* at 13.)

Complainants say that Magar discloses an on-chip clock generator circuit "CLOCK GEN" into which is provided two signals from an off-chip crystal oscillator. (*Id.*) In a non-final rejection based on Magar, the examiner asserted that the "CLOCK GEN" circuitry was fabricated on the same microprocessor substrate as the CPU. (*Id.* (citing CXM-0015 (4/3/97 Office Action) at 2).) In response, the applicants specifically pointed out that their invention had an on-chip oscillator, unlike Magar, and was further distinguishable from Magar because an external fixed frequency crystal drives the clock disclosed in Magar: "The definitive statement that the clock gen circuit in Fig. 2a in the Magar patent is equivalent to the 'conventional crystal clock' 434 in Fig. 17 of the present application is at col. 15, lines 26-41 of Magar." (*Id.* (citing CXM-0013 (7/7/97 Amendment) at 2).)

To further clarify, argue Complainants, the applicants then quoted from their description of an embodiment of their invention which describes their variable speed clock and pointed out that "the variable speed clock is a primary point of departure from the prior art." (*Id.* (citing

CXM-0013 at 3).) The applicants, say Complainants, explained that not only is the crystal oscillator in Magar not made on the same integrated substrate as the CPU—and therefore the Magar clock is not capable of varying with the CPU based on variations in manufacturing process, operating voltage, and temperature—but even if the crystal were formed on the same substrate, which is not possible, it would not vary in the same way as the frequency capability of the microprocessor because the oscillation frequency of the crystal oscillator is designed not to vary in response to such things as temperature, voltage, or manufacturing conditions. (*Id.*) The applicants, note Complainants, made the following statement:

> The present invention is unique in that it applies, and can only apply, in the circumstance where the oscillator or variable speed clock is fabricated on the same substrate as the driven device. The example given is a non-crystal controlled circuit, a ring oscillator. A ring oscillator will oscillate at a frequency determined by its fabrication and design and the operating environment.

(*Id.* (citing CXM-0013 at 5).) Complainants argue that the applicants went on to explain that their invention differs from the cited prior art not only because the oscillator and the CPU are on the same substrate but also because "the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so." (*Id.* (citing CXM-0013 at 5).)

According to Complainants, the applicants' remarks in response to the second office action citing Magar do not include a clear and unambiguous disclaimer. (*Id.* at 15.) Complainants argue that the patent applicants maintained that Magar disclosed only an external crystal-based oscillator, noting in their Remarks that Magar did not disclose an "entire ring oscillator variable speed system clock, variable speed clock or oscillator in the integrated circuit" and instead (and not in addition to) "the prior art circuits require an external crystal," as noted in this extract from the prosecution history:

> Because the prior art does not provide an entire ring oscillator variable speed system clock, variable speed clock or oscillator in the integrated circuit, in that the prior art circuits require an external crystal, the prior art fails to teach or suggest the invention now claimed.

(*Id.* (citing CXM-0016 (2/8/98 Amendment) at 3).) Notably, according to Complainants, the applicants went on to emphasize that the external crystal in Magar is required for a particular purpose, oscillation of the clock:

> Magar's clock generator relies on an external crystal connected to terminals X1 and X2 to oscillate, as is conventional in microprocessor designs. It is not an entire oscillator in itself.

(*Id.* (citing CXM-0016 at 3).) The applicants also explained that in Magar the "entire oscillator" is not on the integrated circuit because "it requires an external crystal." (*Id.* (citing CXM-0016 at 4).) Then, say Complainants, the applicants pointed out that "as a self-contained on-chip circuit, Magar's clock gen is distinguished from an oscillator in at least that it lacks the crystal or external generator it requires." (*Id.*) Despite its name, Magar's "Clock Gen" is only circuitry to modify the clock speed provided by the external crystal oscillator and therefore Magar does not have an "entire" oscillator on the same circuit as the CPU because its oscillator was formed off the chip, argue Complainants. (*Id.* at 15-16.) In summarizing their points, the applicants wrote this:

> The Magar teaching is well known in the art as a conventional crystal controlled oscillator. It is specifically distinguished from the instant case in that it is both fixed-frequency (being crystal based) and requires an external crystal or external frequency generator.

(*Id.* at 16 (citing CXM-0016 at 5).) Complainants argue that the applicants were clearly pointing out that their invention does not require an external crystal oscillator or external frequency generator to generate the clock signal, and nowhere do they indicate that such components are prohibited from any embodiment that practices the invention. (*Id.*) It is clear from the file history,

they argue, that the applicants distinguished Magar on the basis that it did not have an "entire" on-chip oscillator as claimed. Because Magar did not have any on-chip oscillator, there was no issue as to whether such an on-chip oscillator could be regulated in any fashion by external circuitry. (*Id.*) Therefore, Respondents' assertion that the applicants "clearly and unambiguously" disclaimed any reliance on an external crystal/clock generator is incorrect and should be rejected, argue Complainants.

As for Respondents' argument that the applicants clearly and unambiguously disclaimed all reliance on control signals to control the clock based on their distinction from Sheets, Complainants say this too should be rejected as an inaccurate characterization of the prosecution history regarding Sheets. (*Id.* at 16-17.) Complainants say the applicants distinguished Sheets because it did not include an on-chip oscillator because it provides frequency control information to an external clock and requires a command signal to control the external clock. (*Id.* at 17 (citing CXM-0012 (4/15/96 Amendment) at 8).) Complainants quote the following passage therefrom:

> The present invention does not simply rely upon provision of frequency control information to an external clock, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described in Sheets....Sheet's system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.

(*Id.*)

According to Complainants, the applicants made the same "requirement" distinction in response to a subsequent rejection over Sheets, wherein they said this:

> Even if the examiner is correct that the variable clock in Sheets is in the same integrated circuit as the microprocessor of system 100, that still does not give the claimed subject matter. In Sheets a command input is required to change the clock

> speed [but in] the present invention…[n]o command input is necessary to change the clock frequency.

(*Id.*)

Administrative Law Judge's findings and construction

The Administrative Law Judge finds the proposed construction of Complainants to be inadequate. They propose this definition: "a ring oscillator, variable speed system clock, wherein the ring oscillator is located entirely on the same semiconductor substrate as the central processing unit". The insertion of the two commas is not explained, as there are no commas in the patentees' syntax: "an entire ring oscillator variable speed system clock in said single integrated circuit". It appears that the Complainants are treating the phrase "variable speed system clock" which lies between the two commas as merely an appositive of the term "ring oscillator," as though the latter term is explanatory of the earlier one. This is also suggested in Complainants' arguments that the preferred embodiment identifies the ring oscillator of the invention as the "system clock," and the terms "oscillator" and "variable speed clock" each refers to the on-chip oscillators that generate the CPU clock. However, the applicants made it clear that their invention is both an oscillator and a clock:

> Applicant's prior comments apparently did not make clear the distinction between an oscillator and a clock as it applies to the Magar reference. As a self-contained on-chip circuit, Magar's clock gen is distinguished from an oscillator in at least that it lacks the crystal or external generator that it requires. Thus Magar's circuit is not an entirely on-chip oscillator as contemplated in the present case, it is only a clock.

(JXM-0016 at 4.) The applicants then said this:

> As mentioned in Applicant's previous remarks, the term clock is sometimes used interchangeably with oscillator, even inappropriately, leading to confusion. And, adding to the confusion, in the instant case, 430 is both an oscillator and a clock in the conventional senses. It is an oscillator in that it oscillates without external components (unlike the Magar reference). An example of such an

> oscillator circuit which does not utilize external components is given in Fig. 18 of the present application. It is also a clock in Magar reference sense in that it produces the various timing signals needed of the CPU….

(*Id.*) Since, in the applicants' own words, "430," which is the "ring oscillator variable speed clock" is both an oscillator and a clock in the conventional senses, there is no reason for treating the term "variable speed system clock" as an appositive of the term "ring oscillator." Rather, the evidence points to the notion that a "ring oscillator variable speed system clock" is a grammatical unit: "both an oscillator and a clock in the conventional senses." Therefore, insofar as Complainants' insertion of the two commas is unexplained and could lead to an ambiguous and perhaps misleading construction, it is deemed improper.

The remainder of Complainants' proposed construction is found lacking because it fails to account for the actions of the applicants during the course of prosecution of the patent. They pointedly said this:

> Because the prior art does not provide an entire ring oscillator variable speed system clock, variable speed clock or oscillator in the integrated circuit, in that the prior art circuits require an external crystal, the prior art fails to teach or suggest the invention as now claimed.

(*Id.* at 3.) It is manifest therefore that the term "entire" as it was argued by the applicants to the examiner, for the very purpose of overcoming his rejection based on Magar and Pelgrom, requires that the ring oscillator variable speed system clock, as taught by the invention of the '336 patent, be on the same semiconductor substrate as the central processing unit. Magar's clock generator "is not an entire oscillator in itself" because it "relies on an external crystal connected to terminals X1 and X2 to oscillate." (*Id.*) "It is specifically distinguished from the instant case in that it is *both* fixed-frequency (being crystal based) and requires an external crystal or external frequency generator." (*Id.* at 5 (emphasis added).)

Exhibit “F” – Part 2

Complainants' proposed construction does not convey the essential point made by the applicants in seeking to gain acceptance of the examiner for their purported invention by asserting that the ring oscillator variable speed clock "does not utilize external components" (JXM-0016 at 4.) On the other hand, Respondents' proposed construction does. It expresses the fact that the ring oscillator variable speed system clock is a self-contained oscillator and clock which does not utilize external components (as is disclosed in Fig. 18 of the '336 patent). Furthermore, it captures the distinction argued by the applicants in distinguishing Sheets, when they said this:

> The present invention does not similarly rely upon provision of frequency control information to an external clock, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, since the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance. Sheets' system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.

(JXM-0017 at 8.)

Although the Complainants argue that the applicants' statements during prosecution of the patent do not amount to a clear disavowal, the Administrative Law Judge finds otherwise. In *Safran v. Johnson & Johnson,* ___ F.3d___ 2013 WL 1338910 (Fed. Cir. 2012) at *7, the court said:

> To be sure, a prosecution disclaimer requires "clear and unambiguous disavowal of claim scope," *Storage Tech. Corp. v. Cisco Sys., Inc.*, 329 F.3d 823, 833 (Fed.Cir.2003), but applicants rarely submit affirmative disclaimers along the lines of "I hereby disclaim the following ..." during prosecution and need not do so to meet the applicable standard. In this case, Saffran's unqualified assertion that "the device used is a sheet" extends beyond illuminating "how the inventor understood the invention," *Phillips v. AWH Corp.*, 415 F.3d 1303, 1317 (Fed.Cir.2005) (en banc), to provide an affirmative definition for the disputed term. Given such definitive statements during prosecution, the interested public was entitled to

conclude that the "device" recited in the claims of the '760 patent is a continuous sheet.

The same holds true here, where the applicants' unqualified statements in distinguishing Magar, Pelgrom, and Sheets support the conclusion that the entire ring oscillator is both entirely on the same semiconductor substrate as the central processing unit but also does not rely on a control signal or an external crystal/clock generator to generate a clock signal.

Although Staff's construction also addresses the point, it does so too broadly with the words "all components that determine clock frequency." How literally the word "determine" is to be applied in the context of the claim is a subject that invites further debate.

Therefore, the Administrative Law Judge concludes that the term "an entire ring oscillator variable speed system clock in said single integrated circuit" as it appears in claims 1 and 11 means "a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the central processing unit and does not rely on a control signal or an external crystal/clock generator to generate a clock signal".

3. Claims 6, 13—*"an entire oscillator disposed upon said integrated circuit substrate"*

The parties' proposed constructions for this term are as follows:

Respondents	Complainants	Staff
an oscillator that is located entirely on the same semiconductor substrate as the central processing unit and does not rely on a control signal or an external crystal/ clock generator to generate a clock signal	an oscillator that is located entirely on the same semiconductor substrate as the central processing unit	an oscillator that includes all components that determine oscillator frequency located on the same semiconductor substrate as the CPU

(CMBr. at 15; RMBr. at 12; SMBr. at 7.) Complainants say the parties generally agree on the construction of this phrase with the exception that the Respondents seek to add the same improper limitations as those discussed in connection with the previous claim term, and for the same reasons

provided by Complainants in that regard, Respondents' proposed construction should be rejected and Complainants' should be accepted. (CMBr. at 15.)

Respondents' argument with respect to this claim term is the same as its argument with respect to the previous claim term, as mentioned above, and therefore need not and will not be repeated here. (RMBr. at 12-25.) The same holds true for Staff. (SMBr. at 6-9.)

Administrative Law Judge's findings and construction

The Administrative Law Judge finds that the same evidence and reasoning applies to this term as to the prior term and therefore concludes that the term "an entire oscillator disposed upon said single integrated circuit substrate" means "an oscillator that is located entirely on the same substrate as the central processing unit and does not rely on a control signal or an external crystal/clock generator to generate a clock signal".

4. Claims 10, 16—*"an entire variable speed clock disposed upon said integrated circuit substrate"*

The parties' proposed constructions for this term are as follows:

Respondents	Complainants	Staff
a variable speed clock that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an external crystal/ clock generator to generate a clock signal	a variable speed clock that is located entirely on the same semiconductor substrate as the central processing unit	a variable speed clock that includes all components that determine clock frequency located on the same semiconductor substrate as the CPU

(CMBr. at 15; RMBr. at 13; SMBr. at 7.) Complainants say the parties generally agree on the construction of this phrase with the exception that the Respondents seek to add the same improper limitations as those discussed in connection with the previous claim terms, and for the same reasons provided by Complainants in that regard, Respondents' proposed construction should be rejected and Complainants' should be accepted. (CMBr. at 16.) Respondents' argument with

respect to this claim term is the same as its argument with respect to the previous claim terms, as mentioned above, and therefore need not and will not be repeated here. (RMBr. at 12-25.) The same holds true for Staff. (SMBr. at 6-9.)

Administrative Law Judge's findings and construction

The Administrative Law Judge finds that the same evidence and reasoning applies to this term as to the two previous claim terms and therefore concludes that the term "an entire variable speed clock disposed upon said single integrated circuit substrate" means "a variable speed clock that is located entirely on the same semiconductor substrate as the central processing unit and does not rely on a control signal or an external crystal/clock generator to generate a clock signal".

5. Claims 1, 6, 10, 11, 13, 16—*"clocking said central processing unit"*

The parties' proposed constructions for this term are as follows:

Respondents	Complainants	Staff
timing the operation of the CPU such that it will always execute at the maximum speed possible, but never too fast	providing a timing signal to said central processing unit	

(CMBr. at 16; RMBr. at 62; SMBr. at 26.)

Complainants' arguments in support of their proposed construction

Complainants say the plain and ordinary meaning of "clocking said central processing unit" is to provide a timing signal to the central processing unit, a statement that is supported by the general discussion of the purpose of the ring oscillator variable speed clock in the '336 patent. (CMBr. at 16 (citing JXM-0001 at 16:43-17:37).) Complainants say their proposed construction is supported by the district court judges' constructions in the Texas and California cases previously mentioned. (*Id.*) Complainants say the Respondents seek to import a limitation from the preferred

embodiment of the invention, which they say is improper, even when there is but one embodiment disclosed. (*Id.* at 16-17 (citing JXM-0001 at 16:59-17:2; *Innova/Pure Water,* 381 F.3d at 1117).) Complainants argue that because the patentee never made any clear intention to limit the claim scope of the '336 patent in the manner suggested by Respondents, their proposed additional limitation should be rejected. (*Id.* at 18.)

Respondents' arguments for their proposed construction

Respondents says their proposed construction of this limitation is drawn directly from clear statements in the specification and prosecution history describing the purported invention as including a central processing unit that "will always execute at the maximum speed possible, but never too fast." (RMBr. at 62.) In this regard, argue Respondents, the specification asserts that the alleged invention surpasses the prior art because "[by] deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast." (*Id.* at 62-63 (citing JXM-0001 at 16:59-17:2).) Respondents argue that these statements must be reflected in the construction of the claims because when the embodiment "is described in the specification as the invention itself, the claims are not necessarily entitled to a scope broader than that embodiment." (*Id.* at 63 (citing *Edwards Lifesciences LLC v. Cook, Inc.,* 582 F.3d 1322, 1330 (Fed. Cir. 2009)).) The say, more specifically, "[w]here the specification makes clear that the invention does not include a particular feature, that feature is deemed to be outside the reach of the claims of the patent, even though the language of the claims, read without reference to the specification, might be considered broad enough to encompass the feature in question." (*Id.*) They also contend that when the specification, as here, "describes a feature of the invention…and criticizes other products… that lack that same feature, this operates as a clear disavowal of these other products…." (*Id.*)

According to Respondents, all of these principles apply here because the specification of the '336 patent emphatically declares that the CPU of the alleged invention "always" executes at the maximum speed and criticizes products that lack this feature. (*Id.*) The applicants also relied on this feature to distinguish the Sheets reference during the prosecution of the '336 patent when they argued that "CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430." (*Id.* (citing JXM-0002 (4/15/96 Amendment) at 8-9).)

Staff's arguments for its proposed construction

Staff says its proposed construction is consistent with the plain language of the claims, the intrinsic record of the '336 patent, and the prior Markman orders of the district court judges previously mentioned. (SMBr. at 26.) Staff says the specification of the '336 patent describes an embodiment of a microprocessor system using clocking techniques that overcome prior art limitations requiring that clock speeds be restricted based on worst-case conditions. (*Id.* (citing JXM-0001 at 15:44-53).) Although the disclosed clocking technique purportedly allows a microprocessor to be clocked at optimal speed, the specification does not express a clear intent to so limit the claims. (*Id.* at 27.) It is possible for a designer to vary clock speed by changing the number of inverters used in the ring inverter, as indicated in Figure 18 of the '336 patent, and this disclosure is consistent with the constructions proposed by Staff and Complainants, says Staff. (*Id.*) Moreover, the plain language of the claim does not require or even suggest that the CPU must be clocked at the maximum speed possible. Instead, the speed of the disclosed clock depends on the propagation delay of the ring oscillator: too few inverters and the clock will oscillate too fast; too many inverters and the clock will oscillate sub-optimally. (*Id.*)

Staff argues that Respondents' construction attempts to import limitations from a disclosed embodiment into the claims, which is improper. (*Id.* (citing *Intel Corp. v. U.S. Int'l Trade*

Comm'n, 946 F.2d 821, 836 (Fed. Cir. 1991) ("Where a specification does not require a limitation, that limitations should not be read from the specification into the claims.")).) Staff maintains that even though the specification recites that "CPU 70 will always execute at the maximum frequency possible, but never too fast," the intrinsic evidence does not show an express intent to import this limitation into the claims. (*Id.* at 28 (citing *Thorner v. Sony Computer Entertainment America, LLC*, 669 F.3d 1362, 1368 (Fed. Cir. 2012)).)

Administrative Law Judge's findings and construction

The Administrative Law Judge concludes that Respondents' proposed construction impermissibly reads into the claims a limitation expressed in the specification: "such that it will always execute at the maximum speed possible, but never too fast." In the first place, the statement in itself, divorced from the surrounding discussion, is susceptible to misinterpretation. What does it mean to say never too fast? Strictly speaking, if something is designed to operate at the maximum speed possible, it cannot by so doing be operating too fast. What is meant by "too fast"? Too fast for what? In the end, there is only one word in this term that is in question, "clocking," although the parties are in agreement as to the basic meaning of the word. Respondents say it is "timing the operation of the CPU" and Complaints and Staff say it is "providing a timing signal to the central processing unit." In this respect the parties are in accord. However, Respondents seek to impose a further limitation, one which adds ambiguity, and this is not helpful. Furthermore, it violates the principle that the words of a claim are generally to be given their plain and ordinary meaning.

For these reasons, the Administrative Law Judge concludes that the term "clocking said central processing unit" means "providing a timing signal to said central processing unit."

6. Claims 6, 13—*"thereby enabling said processing frequency to track said clock rate in response to said parameter variation"*

The parties' proposed constructions for this term are as follows:

Respondents' Proposed Construction	Staff's Proposed Construction	TPL's Proposed Construction
said parameter variation directly causing said processing frequency to track said clock rate		[thereby enabling] the processing frequency of the central processing unit to follow said clock rate in response to said parameter variation

(CMBr. at 18; RMBr. at 43; SMBr. at 16.)

Complainants' arguments in support of their proposed construction

Complainants begin by criticizing Respondents' and Staffs' proposed construction on the ground that they seek to rewrite the claim language that is clear on its face: fabricating the oscillator and CPU on the same chip enables or allows the "processing frequency of the central processing unit" to follow or track "said clock rate in response to said parameter variation." (CMBr. at 18.) According to Complainants, Respondents seek to read "enabling" entirely out of the claim. (*Id.*) Complainants say the word "enable" connotes "allow," or "make possible," or "create the capability." (*Id.* at 18-19.) They say the Respondents want to replace "enable" with "directly causing," an expression for which there is no basis. (*Id.* at 19.)

According to Complainants, the '336 specification supports their construction that the invention "enables" or "makes possible" the capability for the frequency of the CPU to follow the clock rate in response to changes in parameters like temperature, voltage and semiconductor processing variations. (*Id.* (citing JXM-0001 at 16:47-67).) Complainants argue that, contrary to Respondents' suggestion, nothing in the specification demands a limitation that parameter variations must "directly cause" the processing frequency of the CPU to track the clock rate. (*Id.*) The specification explains that all of the transistors on the same silicon die, both the transistors of

the ring oscillator and those of the CPU, will be affected "similarly" because they are fabricated on the same piece of silicon. (*Id.*) The invention enables a clocking system that takes advantage of the laws of physics, which dictate that all of the transistors on the same chip will be affected "similarly" as certain parameters vary. (*Id.*)

Complainants argue that the prosecution history demonstrates that their proposed construction is correct, because there is nothing in the history that contradicts the clear meaning of the claim as recited in Complainants' construction. The language "thereby enabling said processing frequency to track said clock rate in response to said parameter variation" was added in an amendment of April 15, 1996. (*Id.* at 19-20 (citing CXM-0012 (claim 73)).) In explaining the amendment, the applicants' attorney made the following observation: "This advantageously allows a processing frequency of the central processing unit to track a clock rate of the oscillator as a function of substrate parameter variation." (*Id.* at 20 (citing CXM-0012 at 9-10).) Complainants argue that this explanation is entirely consistent with the Complainants' proposed construction and does not support Respondents' additional limitation. (*Id.*)

Respondents' arguments in support of their proposed construction

Respondents argue that the specification teaches that the PVT parameters (process, voltage, and temperature) determine the ring oscillator frequency, which in turn drives the CPU frequency. In this regard, the specification states "the ring oscillator frequency is determined by the parameters of temperature, voltage, and process…[and] its performance tracks the parameters which similarly affect all other transistors on the same silicon die." (RMBr. at 44 (citing JXM-0001 at 16:59-67).) The CPU, in turn, derives its system timing from the ring oscillator. (*Id.* (citing JXM-001 at 16:67-17:2 ("By deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast.")).) In other words,

argue Respondents, any change to the PVT parameters will directly cause a change in the CPU processing frequency. (*Id.*)

According to Respondents, the prosecution history is in accord with their proposed construction, revealing that the patent applicants distinguished Magar precisely on this point, as shown by this excerpt:

> The Examiner states that "Since Pelgrom's [Magar's] [sic] microprocessor is made of electronic components, it would have been obvious, from the teaching of Pelgrom, to a person of ordinary skill in the art to have the components of Magar' [sic] microprocessor and clock (oscillator) make [sic] of the same process for ensuring processing frequency of the cpu [sic] to track the clock rate in response to parameter variations." Applicant agrees that the processing frequency capability of the CPU would track the clock rate capability of the clock generator, as this is controlled by the laws of physics on which the Pelgrom reference is based. However, there would be no "tracking" of the clock rate produced by the Magar clock generator, because the entire circuit is not provided on the integrated circuit.

(*Id.* at 44-45 (citing JXM-0002 (February 10, 1999 Amendment) at 3).) The applicants acknowledged that the processing frequency capability of the Magar CPU would track the clock rate capability of the Magar clock generator in response to PVT parameter variations, as controlled by the laws of physics, argue Respondents. (*Id.* at 45.) However, the applicants argued that because the Magar clock generator is not entirely on the same circuit as the CPU, the Magar CPU would not track the actual clock rate—the applicants argued that while the parameter variation would cause changes to the clock rate capability, the result would not be changes to the clock rate. (*Id.*)

In contrast, argue Respondents, the '336 patent claims that both the ring oscillator and the CPU are on the same integrated circuit, and therefore any parameter variation directly causes the CPU processing frequency to track the clock rate. (*Id.*) One of the named inventors confirmed that a key to the alleged invention was combining the entire clock and CPU to allow the PVT

parameter variations to cause the CPU to track the clock rate. (*Id.* (citing RXM-0001C (Fish Dep.) at 140).)

Respondents argue that Federal Circuit precedent supports their construction in respect of equating the phrase "in response to" with "directly causing." (*Id.* at 46.) They say the Federal Circuit affirmed a lower court's construction of "in response to" as requiring direct causation. (*Id.* (citing *Am. CalCar, Inc. v. Am. Honda Motor Co.*, 651 F.3d 1318, 1339-41 (Fed. Cir. (2011)).) In that case, the plaintiff argued that the lower court had misconstrued the term "identifying one of the plurality of providers in response to the vehicle condition," while defendant argued that the "district court properly construed the claims to require a cause-and-effect relationship… require[ing] that the processor identify a provider directly in response to a vehicle condition." (*Id.*) Respondents quote this passage from the Federal Circuit's decision:

> We agree with the district court's claim construction…[that] '[i]n response to' connotes that the second event occur in reaction to the first event. The language of the claim itself suggests that when a vehicle condition is detected, the processing element identifies a provider automatically as opposed to requiring further user interaction. Further, the specification fails to disclose any embodiment that requires any type of user interaction prior to identification of a service provider.

(*Id.* (quoting *Am. CalCar*, 651 F.3d at 1339-40).) According to Respondents, the prosecution history and specification confirm that the same direct cause and effect relationship exists between a parameter variation and the CPU system timing, in accordance with Respondents' and Staff's proposed construction. (*Id.*)

Respondents argue that there is no reason to alter the term "track" to "follow" as Complainants do in their proposed construction. (*Id.*) Nowhere do the claims, specification, or prosecution history refer to the CPU processing frequency "following" a clock rate, say Respondents. (*Id.*) In contrast, the claims as well as the specification and prosecution history use

the term "track" numerous times. (*Id.* at 46-47.) Therefore, there is no need to construe the word "track" as "follow." (*Id.* (citing *Interactive Gift Express, Inc. v. CompuServe Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001) ("If the claim language is clear on its face, then our consideration of the rest of the intrinsic evidence is restricted to determining if a deviation from the clear language of the claims is specified.")).)

Staff's arguments in support of its proposed construction

According to Staff, the '336 patent disparages conventional CPU clocking techniques for failing to achieve maximum theoretical performance. (SMBr. at 16 (citing JXM-0001 at 16:44-53).) As a result, conventional microprocessor systems "must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in wors[t] case conditions." (*Id.* (quoting JXM-0001 at 16:50-53).) Staff argues that, in order to overcome this purported deficiency in prior art designs, the '336 patent proposes using a variable speed ring oscillator clock that is located entirely on the same integrated circuit as the microprocessor. (*Id.* (citing JXM-0001 at 16:54-58).) The frequency of the variable speed ring oscillator clock is determined, not by an external crystal or off-chip components but by "the parameters of temperature, voltage, and process." (*Id.* (citing JXM-0001 at 16:59-60).) Therefore, parameter variations affect the microprocessor performance and the clock speed in the same manner, and the disclosed clock inherently compensates for such parameter variations, such that "CPU 70 will always execute at the maximum frequency possible, but never too fast." (*Id.* (citing JXM-0001 at 17:1-2).)

Staff says the purpose of the variable speed clock is to overcome deficiencies in the prior art that require designers to limit performance such that the system will correctly function under worst case conditions, and therefore a person of ordinary skill in the art at the time of invention

would understand the invention as requiring direct causality between parameter variation and clock speed. (*Id.* at 17.)

Staff argues that the plain language of the claim requires direct causality between parameter variation and processing speed. (*Id.*) The claim recites varying "the processing frequency…as a function of parameter variation." (*Id.*) As concluded by the judge in the Texas case "a person of ordinary skill in the art reading the patent would understand that the phrase 'as a function of' is describing a variable that depends on and varies with another." (*Id.* (citing SXM-0002, App., Tab 2, *Markman* Order II, at 0046).) Staff argues that such a dependence gives rise to a direct causal relationship, and therefore the constructions proposed by Respondents and the Staff are consistent with both the claim and the specification. (*Id.*)

Therefore, the Staff submits that the phrase "thereby enabling said processing frequency to track said clock rate in response to said parameter variation" should be interpreted to mean "said parameter variation directly causing said processing frequency to track said clock rate." (*Id.*)

Complainants' response to Respondents' and Staff's arguments

Complainants argue that the constructions proposed by Respondents and Staff suffer from at least two major problems. (CRMBr. at 32.) First, these parties ignore the first two words of the phrase, "thereby enabling." (*Id.*) Second, they ignore the preceding limitation of each claim; in other words, the other parties do not consider the apparatus in each claim that "thereby enables" the rest of the disputed phrase. (*Id.*) In so doing, they ignore the '336 patent's teachings about the relationship between the on-chip oscillator and the processing capability of the CPU. (*Id.* (citing JXM-0001 at 16:63-67, 17:2-10).)

Complainants argue that, as explained in both the claims and the specification, the on-chip oscillator is used to "clock" (i.e., provide a timing signal to) the CPU. (*Id.*) Moreover, because the

oscillator and the CPU are fabricated on the same silicon die, the frequency capability of the oscillator and the processing frequency capability of the CPU naturally will vary similarly because of the PVT parameter variations. (*Id.* at 32-33.) Therefore, the PVT variations do not "directly cause" the processing frequency of the CPU to track the clock rate, as suggested by Respondents. Rather, argue Complainants, the claimed structure allows PVT variations to influence both the on-chip oscillator and the processing capability of the CPU in a similar manner, "thereby enabling" the clock to provide an appropriate timing signal to the CPU. (*Id.*) The processing frequency of the CPU must "track" the clock rate of the on-chip oscillator, because the on-chip oscillator generates the clock signals for timing the operation of the CPU.

Complainants argue that their proposed construction is also confirmed by the prosecution history, in which the applicants repeatedly explained that disposing the CPU and the oscillator within the same integrated circuit "allows" the CPU to track variations in the speed of the oscillator. (*Id.*) Complainants say a proper claim construction begins with the words of the claims themselves, which are to be given their ordinary and customary meaning. (*Id.* (citations omitted).) Respondents and Staff, according to Complainants, ignore the words "thereby enabling" in their constructions of the disputed phrase, and this deficiency on their part undermines their proposed constructions. (*Id.*)

Complainants argue that Respondents attempt to frame the dispute in terms of whether the words "in response to" require a particular direct causation, but the real question is whether the words "thereby enabling" require anything more than their plain and ordinary meaning: "allowing," "making possible," or "providing the means" for the processing frequency of the CPU to track the clock rate in response to parameter variations. (*Id.* at 33-34.) The words of the disputed phrase are clear as they stand, and no one disputes the "said processing frequency" is the

frequency at which the CPU operates, argue Complainants. The limitation expressly provides that the processing frequency is "enable[d]" to track the clock rate, and by definition the verb "enable" means "making possible," not "directly causing" something to happen, as Respondents argue. (*Id.*)

Furthermore, nothing in the plain language of this phrase states or implies that the "parameter variation" "directly causes" the CPU processing frequency to track the clock rate, argue Complainants. (*Id.*) Rather, the word "thereby" clearly refers back to the claims' earlier descriptions of the structure of the invention—an oscillator clock or oscillator that is fabricated in the same integrated circuit as the CPU. (*Id.*) This, according to Complainants, is the structure that "thereby enables" the CPU frequency to track the clock rate in response to the PVT variations. (*Id.*)

Specifically, argue Complainants, the limitations of claims 6 and 13 preceding the "thereby enabling" language explain that the CPU and the entire oscillator are disposed upon the same integrated circuit and that the oscillator clocks the CPU. (*Id.* (citing JXM-0001 at *Ex Parte* Reexamination Certificate C1, claim 6, col. 2, ll. 14-23, claim 13, col. 3, ll. 34-38).) The claims also explain that this structure provides common operating characteristics for the transistors of the oscillator and the CPU, "thus varying the processing frequency of [the CPU] and the clock rate of [the oscillator] in the same way as a function of parameter variation." The structure that "thereby enables" is the previously recited structure, which is the CPU and oscillator disposed upon the same integrated circuit. (*Id.* at 34-35.) So it is this structure that "enables" the "processing frequency of [the CPU] to track said clock rate [of the oscillator] in response to said parameter variation." (*Id.* at 35.) In contrast, the claim language does not require that the

parameter variation must "directly cause" frequency to track the clock rate, as suggested by Respondents and Staff, say Complainants. (*Id.*)

Complainants argue that Staff's separate assertion that a direct causal relationship between the CPU's processing frequency and PVT parameter variations is separately required by the "thus varying" limitation because it includes the phrase "as a function parameter variation" is incorrect because nothing in that language requires "direct causality" between parameter variation and CPU processing frequency. (*Id.*) Nor is Staff's construction supported over Complainants' by the claim construction of the judge in the Texas district court case, who observed that the phrase "as a function of" "describes a variable that depends on and varies with another." (*Id.* at n. 5 (citing JXM-008 (Ware Order) at 18).) The CPU will be enabled to track the clock rate of the oscillator because they are manufactured on the same integrated circuit with the same devices, say Complainants. (*Id.* at 35.) Complainants say they do no dispute that the processing frequency of the CPU will ultimately vary with parameter variations, but not "directly." (*Id.*) Rather, parameter variations influence the oscillator frequency, which causes a change in the processing frequency of the CPU. (*Id.*) In other words, argue Complainants, as the disputed phrase specifically states, the CPU's processing frequency is "enabled," or "allowed," to track the clock rate in response to parameter variation. But the parameter variation does not directly cause tracking, say Complainants. (*Id.*)

In sum, say Complainants, their construction is consistent with the ordinary meaning of the claim language in its entirety; whereas, Respondents' and Staff's constructions read out the language "thereby enabling" and improperly import the narrowing words "directly causing" in a way that is inconsistent with the rest of the claim language. (*Id.* at 36.)

Complainants claim that the specification of the '336 patent also supports their construction, because it states this, for example:

> The ring oscillator frequency is determined by the parameters of temperature, voltage, and process.... The ring oscillator **430** is useful as a system clock...because its performance tracks the parameters which similarly affect all other transistors on the same silicon die.

(*Id.* (citing JXM-0001 at 16:59-67).) According to Complainants, Respondents recognize that there is only an indirect relationship between the parameter variations and the CPU processing frequency because they argue this in their brief: "The specification teaches that the PVT parameters (*i.e.*, temperature, voltage, and process) determine the ring oscillator frequency, which in turn drives the CPU frequency." (*Id.* (citing RMBr. at 44).)

According to Complainants, the following passage in the specification also agrees with their description of the invention:

> [I]f the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor **50** will operate slower than normal. Since the microprocessor **50** ring oscillator clock **430** is made from the same transistors on the same die as the latches and gates, it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chips logic to operate properly.

(*Id.* (citing JXM-0001 at 17:2-10).) Clearly, argue Complainants, the invention takes advantage of the fact that the oscillator and the CPU are fabricated on the same silicon die, but it is also clear that the CPU derives its timing from the oscillator. (*Id.*) Therefore, even though PVT parameters influence the transistors of both the CPU and the oscillator, the CPU derives its timing directly from the clock rate, not from parameter variations. (*Id.*)

Complainants say Respondents and Staff do not dispute that the term "to track" means "to follow;" nor do they offer any alternative construction. Instead, Respondents maintain that the term "track" is clear on its face, without offering their understanding of that clear meaning. (*Id.*)

Therefore, say Complainants, if Respondents agree that the term "track" has the meaning of "to follow" no claim construction is required. (*Id.*)

Administrative Law Judge's findings and construction

The Administrative Law Judge finds that the intrinsic evidence does not support Respondents' and Staff's insertions of the limitation "directly causing" in their proposed constructions. Enablement and causation do not mean the same thing; the latter term means effectuating; the former does not. The addition of "directly" adds an even further departure from concept of enablement. Whether the processing frequency actually tracks the clock rate in a given instance depends on how responsive the former is to the latter: there may be a threshold involved. Therefore, tracking may be enabled but not necessarily caused, or effectuated, by changes in the relevant parameters. For this reason, Respondents' and Staff's proposed constructions deviate from the language of the claims. Furthermore, the word "directly" interjects a limitation that is not justified by the intrinsic record. Although the invention recognizes that processing, voltage, and temperature are factors that affect the behavior of the electronic elements that make up the central processing unit and the ring oscillator, the invention does not specify precisely the manner by which that occurs. Therefore injection of the term "directly causes" mischaracterizes the invention.

The Administrative Law Judge finds that the Complainants' proposed construction more accurately reflects the intrinsic evidence and, with slight modification, should be adopted as follows: "thereby allowing the processing frequency of the central processing unit to follow said clock rate in response to said parameter variation."

7. Claims 1, 11—*"varying together;"* Claims 10, 16—*"varying in the same way;"* and Claims 6, 13—*"varying... in the same way"*

The parties' proposed constructions are as follows:

Term	Proposed Constructions		
	Complainants	Respondents	Staff
"varying together" (claims 1, 11) "varying in the same way" (claims 10, 16) "varying...in the same way" (claims 6, 13)	**No construction necessary. But if construed:** changing in a corresponding manner	increasing and decreasing proportionally	increasing and decreasing proportionally

(CMBr. at 20; RMBr. at 36; SMBr. at 14.)

Complainants' arguments in support of their proposals

Complaints report that the parties agree that the term "varying," as it appears in the claims shown above, should be construed the same way in each instance. Complainants argue that Respondents propose an unnecessary and improper additional limitation with the word "proportionally." (CMBr. at 20.) According to Complainants, each of the claims is simply reciting how the invention of the '336 patent applies the law of physics, with the transistors of the CPU and those of the clock varying in a similar manner because they are formed on the same semiconductor substrate. (*Id.* at 21.)

Complainants argue that the specification of the '336 patent explains that the clock frequency and the processing capability of the CPU will vary "similarly" because the transistors of both are fabricated in the same silicon die. (*Id.*) The specification, say Complainants, succinctly explains how the CPU and the clock transistors vary together:

> The designer of a high speed microprocessor must produce a product which operate[s] over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing. Temperature, voltage, and process all affect transistor propagation delays.
>
> ***
>
> Clock circuit 430 is the familiar "ring oscillator" used to test process performance. The clock is fabricated on the same silicon chip as the rest of the microprocessor 50.
>
> ***
>
> The ring oscillator 430 is useful as a system clock. . .because its performance tracks the parameters which similarly affect all other transistors on the same silicon die.

(*Id.* (citing JXM-0001 at 16:44-67).) Nothing in the specification indicates that "varying together" or "varying in the same way" must be "proportional," argue Complainants. Rather, the fact that the clock and the CPU are fabricated on the same silicon die means they will vary in a "similar" manner with any changes in temperature, voltage, and semiconductor processing. (*Id.*)

Complainants also argue that the prosecution file history explains that clock frequency and CPU processing capability vary similarly with parameter variations. (*Id.* at 22.) The reason for this is simple, according to Complainants: The transistors of the ring oscillator clock are manufactured on the same silicon die as the transistors of the CPU. (*Id.* (citing CXM-0012 at 7-8).) There is nothing in the file history that indicates that the "varying" mentioned must be "proportional." (*Id.*)

According to Complainants, all of the intrinsic evidence in the claims, the specification, and the prosecution history is consistent with respect to the term "varying," and no construction is needed; however, if a construction is deemed necessary, it should be this: "changing in a corresponding manner." (*Id.*)

Respondents' arguments in support of their proposed construction

Respondents argue that Complainants should be estopped from advancing their proposed construction because it is inconsistent with Complainant TPL's two previous positions with

respect to the "varying" limitations. (RMBr. at 36-37.) Respondents say the specification of the '336 patent, the patent's prosecution history, Complainants' prior admissions, and testimony of the named inventor all support Respondents' and Staff's proposed constructions. (*Id.* at 37.) Respondents also say the Complainants' proposed interpretation is admittedly non-technical, wholly unhelpful to one of ordinary skill in the art, and inconsistent with the positions that TPL previously took in respect to similar claim language that has been rejected by at least one of the named inventors. (*Id.*)

Respondents note that the "varying" limitations have been the subject of two prior Markman rulings in separate federal district court proceedings, one in the Eastern District of Texas, and the other in the Northern District of California. (*Id.*) In each of those cases, the "varying" limitation was construed to mean "increasing and decreasing proportionally." (*Id.*) In the Texas case the district court rejected TPL's proposed construction and instead construed the "varying" limitation to mean "increasing and decreasing proportionally," which Respondents note is identical to their and Staff's proposed constructions. (*Id.* (citing RXM-0002 (*Markman* Order, June 15, 2007) at 15-16).) And in the California case, TPL abandoned the construction it had proposed in the Texas district court case and proposed the construction that had been adopted by the Texas court, *i.e.*, "increasing and decreasing proportionally." (*Id.* (citing RXM-0003 (Joint Claim Construction Statement, October 29, 2010), Ex. A at 5).) The defendants in the California case, Acer and HTC[6], agreed with TPL's proposed construction. The interpretation of the "varying" limitations in the California district court case is identical to the one in the Texas district court case, note Respondents. (*Id.*)

[6] Two of the Respondents named in this investigation.

Respondents point out that in this investigation TPL rejects the construction that the two district courts, and TPL itself, previously adopted. (*Id.* at 38.) Instead, TPL now argues that the "varying" limitations no longer require a construction or, alternatively, that another and different construction should be applied. (*Id.*) In so doing, TPL advances two distinct constructions for the "varying" limitations, one in the pending California litigation, and another in this investigation, both of which affect Acer and HTC. (*Id.*) According to Respondents, the doctrine of judicial estoppel precludes TPL from advancing its present construction, for three reasons. First, because it is inconsistent with the two earlier positions TPL adopted in the Texas and California cases; second, because TPL successfully convinced the California court to adopt the construction they are now disputing in this investigation; and third, because TPL will derive an unfair advantage and impose prejudice upon HTC and Acer Respondents by forcing them to simultaneously defend against two competing claim construction proposals. (*Id.* (citing *Transclean Corp. v. Jiffy Lube Int'l. Inc.*, 474 F.3d 1298, 1307 (Fed. Cir. 2007); *New Hampshire v. Maine*, 532 U.S. 742, 750-752 (2001)).)

According to Respondents, the specification, prosecution history, TPL's prior positions, and testimony from the named inventors all support Respondents' proposed construction, and Staff's too. (*Id.*) The '336 patent describes and claims a microprocessor system with a ring oscillator and a CPU on the same substrate. (*Id.*) The patent explains that the primary purpose of the invention is to allow the CPU to operate at the highest safe operating speed at all times: "CPU 70 will always execute at the maximum frequency possible, but never too fast." (*Id.* (citing JXM-0001 at 16:67-17:2).) Therefore, the ring oscillator is used to clock the CPU because the speed of the ring oscillator "tracks the parameters (temperature, voltage, and process) which similarly affect all other transistors on the same silicon die," including the transistors of the CPU.

(*Id.* at 38-39 (citing JXM-0001 at 16:59-67).) Because the ring oscillator and the CPU contain transistors that have been made in common, they are affected in the same way by changes in temperature, voltage, and process parameters. (*Id.* at 39 (citing JXM-0001 at 17:21-22).) When the ring oscillator speeds up, the CPU speeds up in the same way. When the ring oscillator slows down, the CPU slows down in the same way. (*Id.* (citing JXM-0001 at 17:2-10).) Thus, the CPU's processing frequency capability automatically varies with the ring oscillator's speed. (*Id.*)

During prosecution of the '336 patent, the applicants repeatedly stressed that their invention is different from the prior art because its ring oscillator's speed automatically varies with, or tracks, the CPU's processing frequency capability with changes to parameters such as temperature and voltage, note Respondents. (*Id.*) In an office action, the patent examiner rejected all of the pending claims over Magar, which discloses a microprocessor with a clock generator fabricated on the same silicon chip as the microcomputer. (*Id.* (citing RXM-8 at Fig. 2A).) The examiner concluded that "[s]ince the microcomputer of Magar is fabricated on a single chip, one of ordinary skill in the art should readily recognize that the speed of the cpu [sic] and the clock vary together due to manufacturing variation, operating voltage, and temperature of the IC." (JXM-0002 (July 7, 1997 Amendment) at 3).)

In response, the applicants made it clear that the "varying" limitations require the ring oscillator's speed to automatically vary together with the CPU's processing frequency capability: "Crucial to the present invention is that since both the oscillator or variable speed clock and the driven device [i.e., CPU] are on the same substrate, when fabrication and environmental parameters vary, the oscillator or clock frequency and the frequency capability of the driven device will automatically vary together." (*Id.* at 39-40 (citing JXM-0002 (July 7, 1997 Amendment) at 5).) In an attempt to overcome a later office action rejecting the '336 patent application claims

based on Magar, the applicants equated this "crucial" feature with "tracking" the clock rate, explaining that "there would be no 'tracking' of the clock rate produced by the Magar clock generator…." (*Id.* at 40 (citing JXM-0002 (February 10, 1998 Amendment) at 3).) Respondents note that in the district court case in California TPL agreed that "track" should be accorded the same definition as "varying"—"increasing and decreasing proportionately." (*Id.* at n. 26 (citing RXM-0003 (October 29, 2010 Joint Claim Construction Statement) at Ex. A).) Furthermore, one of the named inventors, Russell Fish, explained that the word "track" means proportional. (*Id.* (citing RXM-0001C (Fish Dep.) at 166).)

Also, argue Respondents, the applicants explained that, under the laws of physics, a CPU's processing frequency capability necessarily tracks the rate of the variable speed clock when both are located on the same substrate. (*Id.* at 40-41 (citing JXM-0002 (April 24, 1998 Supplemental Amendment) at 1-3).) In the Texas case, TPL confirmed that the laws of physics control the relationship between the CPU clock speed and the CPU processing frequency. (*Id.* at 41 (citing RXM-11 (*TPL v. Fujitsu, et al.,* Case No. 2:05-CV-00494, Dkt. 96, TPL's Mot. To Correct Preliminary Infringement Contentions, Ex. A-1) at 6 ("According to the laws of physics…the processing frequency of said central processing unit and the speed of said ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature.")).)

Therefore, reason Respondents, based on the claims, the specification, the prosecution history, the named inventor's testimony and TPL's prior actions, the "varying" limitations should be construed to mean "increasing and decreasing proportionally." (*Id.* at 41.)

As for TPL's proposed construction in this investigation, Respondents point to the fact that the second named inventor of the '336 patent, Charles Moore, himself rejected such a construction

as meaningless. (*Id.* at 41-42 (citing RXM-9 (Moore Dep., Vol. 1) at 138).) He also testified then that the term "corresponding" was unhelpful with respect to the relationship between the clock speed and the CPU frequency because the term has no technical meaning, saying, "Corresponding is—is perhaps a legal term, but it's not a technical term." (*Id.* at 42 (citing RXM-9 at 137-138).)

Respondents point out that in the Texas case, TPL itself argued that its opponents' proposed interpretation of the "varying" limitations was improper because the word "commensurately" had no technical meaning, and a person of ordinary skill would not know how to quantify this requirement, nor think to do so. (*Id.* (citing RXM-12 (TPL's Claim Construction Reply Brief, April 9, 2007, E.D. Tex., at 9)).) Now, contrary to TPL's past arguments and the testimony of Mr. Moore, who is a paid consultant to Complainants, TPL seeks to "encumber" the "varying" limitations with another non-technical and unusable interpretation, argue Respondents, and this effort should be rejected. (*Id.*)

Staff's arguments in support of its proposed construction

Staff notes that in the Texas court litigation the judge construed the term "varying" to mean "increasing and decreasing proportionally." (SMBr. at 13.) Staff points out that TPL later agreed with this construction in another case pending in the Northern District of California. (*Id.* at 13-14.) However, notes Staff, TPL now proposes a similar but slightly different construction. (*Id.* at 14.) Staff reasons that unless TPL provides compelling reasons to do otherwise, Staff believes that the construction adopted by the Texas district court should also be applied here: "increasing and decreasing proportionally." (*Id.*)

Complainants' reply to Respondents' and Staff's arguments

Complainants say they oppose Respondents' and Staff's proposed constructions because of their use of the term "proportionally," which could be misunderstood to introduce a mathematical

relationship between the variations in the processing frequency or processing frequency capability of the CPU and the speed of the oscillator clock due to the PVT parameters. (CRMBr. at 25.) Complainants argue that the Respondents' proposed construction is ambiguous because the term "proportionally" is often used to describe a particular fixed mathematical relationship between two variables, such that a change in the one is accompanied by a change in the other and the changes are always related by use of a constant. (*Id.*) Thus, for example, the circumference of a circle is proportional to its diameter. (*Id.*) If the size of the circle's diameter increases, the circle's circumference increases by a mathematical certainty. However, such a relationship is not recited in the '336 patent's claims, argue Complainants; nor is it taught in the patent's specification. (*Id.*)

According to Complainants, Respondents Acer and HTC sought a claim construction which introduces such a mathematical functional relationship in the Northern District of California case by focusing on the larger phrase "varying…in the same way as a function of parameter variation." However, the presiding judge rejected any construction that imposed a mathematical relationship and found that no further construction was needed. (*Id.* at 26 (citing JXM-0007 (Ware Order) at 18).) However, argue Complainants, Respondents are now covertly seeking to obtain that same rejected mathematical restriction through the importation of the term "proportionally" in the construction of the terms "varying together" and "varying in the same way." Complainants argue that such mathematical proportionality is not part of the '336 patent invention and should not be permitted by means of claim construction. (*Id.*) At the very least, argue Complainants, if the word "proportionally" is included in the construction of the "varying" terms, there should be an explicit clarification saying that a mathematical relationship is not required. (*Id.*) Complainants acknowledge that the district court judge in the Texas case adopted the term "proportionally" and that later, in the Northern District of California case, Complainants agreed to a construction

incorporating the term "proportionally" to construe "varying together" and "varying in the same way"; however, Complainants say they did not expect or intend by their agreement that that construction would be used to limit the claims of the '336 patent to require a predetermined relationship between variations in the oscillator clock and the CPU processing frequency, and because that possibility exists here, oppose such a construction unless it is specified that a mathematical relationship is not required. (*Id.* at n. 4.)

Complainants argue that if the inventors of the '336 patent had intended to limit their invention to a microprocessor system in which the processing frequency capability of the CPU and the speed of the clock varied "proportionally" in a mathematical relationship, they could, and would, have used that term in the claims and specification, but they did not. (*Id.* at 27.) They could and would have used other terms that indicate a constant relationship with certain mathematical precision in the rate of change between the two variables, but they did not. (*Id.*)

Complainants argue that the words chosen by the inventors, "varying together", "varying…in the same way," and "varying in the same way," do not invoke a mathematical relationship. (*Id.*) The inventors chose terms that are sufficient to convey that the '336 invention takes advantage of the laws of physics in that the transistors of the CPU and those of the clock change in a similar manner because they are formed on the same semiconductor substrate, argue Complainants. (*Id.*) Because nothing in the claims supports a construction that would introduce a requirement of mathematical proportionality as part of "varying together" or "varying in the same way," Respondents' and Staff's constructions should not be adopted, argue Complainants. (*Id.*)

Complainants argue that none of Respondents' citations to the specification teach that the CPU processing frequency and the clock will vary proportionally or in a specific mathematical relationship to one another. (*Id.* at 27-28.) Respondents point to teachings in the specification that

only loosely define the relationship, such as the disclosure that the ring oscillator's speed "tracks the parameters which similarly affect all other transistors on the same silicon die." (*Id.* at 28 (citing JXM-0001 at 16:59-67).) The phrase "similarly affect" is far from synonymous with the certainty that is associated with a mathematical "proportionality," argue Complainants. (*Id.*)

As for the testimony of the inventors that Respondents have cited, Complainants argue that it is entitled to no weight for purposes of claim construction. (*Id.* (citing *Howmedica Osteonics Corp. v. Wright Medical Tech, Inc.*, 540 F.3d 1337, 1347 (Fed. Cir. 2008)).)

With respect to the prosecution history discussed by Respondents, Complainants say there is nothing in the statement that "the clock frequency and the frequency capability of the driven device will automatically vary together" that requires mathematical proportionality. (*Id.*) Nor is there anything in the statement that the CPU's processing frequency capability "tracks" the speed of the clock, because the transistors of both are on the same substrate, which requires mathematical proportionality simply because they vary in response to variations in temperature, voltage, and processing. (*Id.*)

Complainants argue that judicial estoppel is not applicable because compelling reasons exist for their changed position from the one they took in the claim construction discussion in the Northern District of California case, understanding that Respondents in this investigation are seeking to import a mathematical proportionality in respect to construction of the term "varying," whereas in the prior case Respondents were seeking to do that through the construction there of the term "as a function of parameter variation." Complainants say they opposed the efforts of the defendants to introduce a mathematical requirement in the California case, and the judge agreed with them and declined to adopt a claim construction that would have that effect. (*Id.*) But in this investigation, argue Complainants, Respondents appear to be adopting a more covert means to

improperly narrow the "varying" limitations. (*Id.*) Rather than seeking construction of the phrase "as a function of parameter variation" that would require a mathematical relationship and face inevitable rejection in the face of the district court judge's ruling on that point in the California case, Respondents now appear to be seeking to achieve that objective through their proposed construction of the term "varying." Complainants argue that for judicial estoppel to apply, the party's later position must be "clearly inconsistent" with its earlier position, and the party must be deriving an unfair advantage or imposing an unfair detriment on the opposing party by taking inconsistent positions. (*Id.* at 30-31.) Complainants argue that they have consistently maintained that the '336 patent claims are not limited in a way that imposes a mathematical-type functional relationship on the "varying" limitations. (*Id.*) In fact, say Complainants, the judge in the Northern District of California case agreed with them on this point and they prevailed; thus, the evidence does not establish that Complainants are being inconsistent for purposes of judicial estoppel. (*Id.* at 31.) Complainants argue that if Respondents get their way on this point, it is they who will obtain an unfair advantage and Complainants who will suffer unfair detriment. (*Id.*)

In sum, Complainants maintain that the "varying" terms require no construction and that attempts to more precisely define the terms through claim construction will result in substituting foreign terms that themselves need separate constructions, but if a construction is deemed necessary, that construction should be this: "changing in a corresponding manner." (*Id.*)

Administrative Law Judge's findings and construction

The Administrative Law Judge finds that the intrinsic evidence does not disclose that the inventors meant anything more by the term "varying" than what is denoted by its plain and ordinary meaning in each instance in which the term appears in the asserted claims of the '336 patent. Therefore, no claim construction is necessary. The Administrative Law Judge concludes

that judicial estoppel does not apply, for the reasons given by Complainants. Further, the Administrative Law Judge finds the word "proportionally" as it is employed in the constructions proffered by Respondents and Staff adds a limitation that is not supported by the language of the claims, the specification, or the prosecution history. The word "proportionally" denotes a mathematical relationship that is not denoted or connoted by the term "varying." The latter word indicates change generally, but not necessarily by the same degree or ratio. Something may vary in the same manner, such as faster or slower, but not necessarily to the same degree, ratio, or proportion. Nothing that Respondents or Staff have pointed to in the intrinsic record evidences that the invention is limited to proportional variations.

Accordingly, the Administrative Law Judge finds that the term "varying" requires no construction and would have been understood by a person of ordinary skill in the art at the time of the invention according to its plain and ordinary meaning.

8. Claims 11, 13, 16—*"wherein said central processing unit operates asynchronously to said input/output interface"*

The parties' proposed constructions are as follows:

Term	Proposed Constructions		
	Complainants	Respondents	Staff
"wherein said central processing unit operates asynchronously to said input/output interface" (claims 11, 13, 16)	the timing control of the central processing unit operates independently of (not derived from) the timing control of the input/output interface such that there is no readily predictable phase relationship between them	the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them	the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them

(CMBr. at 23; RMBr. at 30; SMBr. at 12.)

Complainants' arguments in support of their proposed construction

Complainants argue that the prosecution history makes clear that "not derived from" is incorporated into the definitions of "asynchronously" and "independently" and therefore this phrase is definitional and is not an additional limitation. (CMBr. at 23.) Complainants argue that because the words "not derived from" are merely explanatory and do not add a limitation that is different from "independently," their proposed construction, not Respondents' or Staff's, should be adopted. (*Id.* at 24.)

Respondents' arguments in support of their proposed construction

Respondents note that the "asynchronous" limitation was the subject of a Markman hearing in the ongoing Northern District of California case, in which the judge construed the term to mean "the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them." (RMBr. at 30 (citing RXM-0005 (June 12, 2012 *Markman* Order) at 21).) Respondents' say that its proposed construction, and Staff's too, is identical to the construction of the judge in the California case and should be adopted here. (*Id.*)

Respondents argue that although Complainants' proposed construction appears similar it deviates in one major and problematic way and that is by replacing the phrase "operates independently of and is not derived from" with "operates independently of (is not derived from)." (*Id.*) This departure, argue Respondents, appears to be motivated by one of two reasons: to define "operates independently of" as "not derived from" in the hopes of effectively reading out "operates independently of" from the interpretation and thereby collapsing the two requirements into one, or else making "not derived from" appear superfluous in the hope of having it dropped from TPL's construction. (*Id.* at 30-31.) Regardless of the reason, argue Respondents, the prosecution history

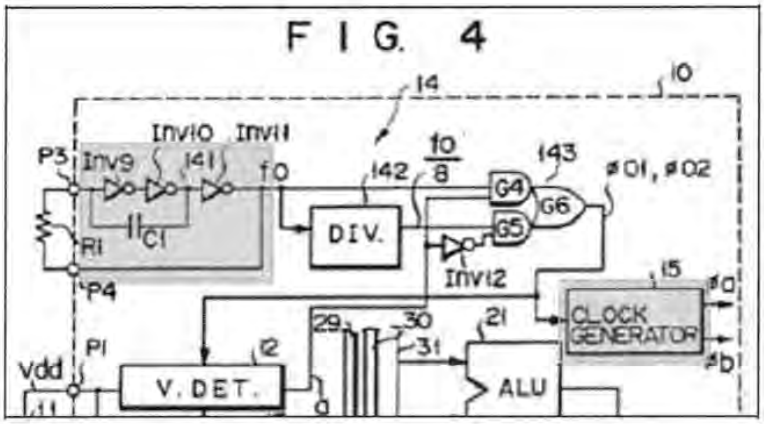
confirms that the "asynchronously" limitation separately requires both of these phrases. (*Id.* at 31.)

According to the '336 patent, "[m]ost microprocessors derive all system timing from a single clock." (*Id.* (citing JXM-0001 at 17:12-13).) However, this is disadvantageous because "different parts of the system can slow all operations." (*Id.* (citing JXM-0001 at 17:13-14).) To overcome this problem, the '336 patent teaches the use of a dual-clock scheme in which a variable speed ring oscillator clocks a CPU and a separate fixed-speed crystal is connected to an I/O interface. (*Id.*) As shown in Figure 17 of the '336 patent, the ring oscillator variable speed system clock **430**, which provides timing control for the CPU, and the crystal clock **434**, which provides timing control for the I/O interface, are not connected; wherefore, neither clock is derived from the other. (*Id.*) In other words, argue Respondents, Figure 17 shows that the CPU and I/O interface clocks operate asynchronously. (*Id.*) In fact, the specification of the '336 patent makes clear that "by decoupling the variable speed of the CPU 70 from the fixed speed of the I/O interface **432**, optimum performance can be achieved by each." (*Id.* at 31-32 (citing JXM-0001 at 17:32-34).) Respondents argue that their construction is consistent with this decoupling because it requires that the timing controls for the CPU and the I/O interface both operate independently of the other and not be derived from one another. (*Id.* at 32.)

In contrast, Complainants' construction ignores that the clocks need to be decoupled and instead requires only that the CPU's timing control not be derived from the I/O interface's timing control, thus ignoring the teaching of the patent. (*Id.*)

Respondents say the reexamination history of the '336 patent confirms that the proper interpretation of the "asynchronous" limitation separately includes the phrases "operates independently of" and "not derived from." (*Id.*) When the reexamination began, claims 11, 13,

and 16 required independent clocks but did not include the "asynchronous" limitations. (*Id.* at 32-33 (citing JXM-5 (September 8, 2008 Amendment) at 2-8).) During the course of the reexamination, the examiner rejected these claims based on the Kato reference. (*Id.* (citing RXM-0006 (U.S. Patent No. 4,766,567 ("Kato") at FIG. 4)).) Figure 4 of Kato is reproduced in part here:



Respondents say the examiner concluded that Kato shows two independent clocks because clocks 141 and 15, highlighted in the figure reproduced above, are "physically independent," and clocks 141 and 15 "can never possibly be at the same frequency." (*Id.* (citing JXM-5 (March 17 2009 Office Action) at 29).) Because the named inventors were not able to convince the examiner that Kato does not show two independent clocks, the inventors distinguished Kato by amending the claims to add the "asynchronous" limitation and pointing to a passage in Kato that states that the two clock signals are "in synchronism with" each other. (*Id.* (citing JXM-5 at 18-19).) Specifically, the inventors argued that the clock signals in Kato were synchronous because they were derived from one another, as quoted here:

> **The clock signals øa and øb are produced in synchronism with the signal from clock (14), and so the clock signals themselves are in synchronism with each other** .... Since the input-output (27) is a component of the data processing circuit,

> it would be understood by one of ordinary skill in the art that the input-output (27) operates in synchronism with the other components of the data synchronism with each other) being supplied to the components of the data *processing circuit*.... Kato does not disclose asynchronous operation among the components of his data processing circuit.

(*Id.* at 33-34 (emphasis added by Respondents).) Further, the named inventors cited the following passage from a textbook establishing that clocks in an asynchronous system are not independent and are also not derived from one another:

> An asynchronous system is one containing two or more independent clock signals. So long as each clock drives independent logic circuitry, such a system is effectively a collection of independent synchronous systems. ***The logical combination of signals derived from independent clocks***, however, poses difficulty because of the unpredictability of their phase relationship.

(*Id.* at 34 (citing Ex. A ("Computational Structures") at 93 (emphasis added by Respondents)).) Respondents note that the district court in the California case, in construing the "asynchronous" limitation based on this passage, explained that "[a] person of ordinary skill would understand that the inventors acted as their own lexicographers to define the term 'asynchronously' such that clocks must be both independent *and* not derived from one another." (*Id.* (citing *Acer, Inc. v. TPL* 2010 U.S. Dist. LEXIS 81322 at *46 (N.D. Cal. June 12, 2012).) In so doing, the inventors made it clear that asynchronously requires two separate characteristics, independence and non-derivation from the other signal. (*Id.*)

Respondents argue that Complainants ignore these two separate requirements and attempt to collapse them into the same word, and in the process, contradict their own representations to the patent examiner that a signal can be independent while still being synchronous with another signal:

> As will be explained, the term "independent" (recited in Claim 6) and the term "synchronously" (recited in Claim 8) are not inconsistent, or otherwise in conflict, with each other....The original clock can be both independent of the oscillator, as required by Claim 6, and comprise a fixed-frequency clock which operates

synchronously relative to the oscillator, as required by Claim 8.

(*Id.* at 34-35 (citing JXM-5 (September 2, 2009 Remarks) at 21-22).) Therefore, independence alone is not enough to define "asynchronous," according to Respondents; something more is required. (*Id.* at 35.) To be truly "asynchronous," based on the inventors' position during reexamination, the signal must be more than just independent; the signal must also not be derived from the other signal at issue. (*Id.*) Complainants' proposed construction fails to capture this representation to the patent examiner, and for these reasons, Respondents' and Staff's constructions capture this concept and are therefore correct. (*Id.*)

Staff's arguments in support of its construction

Staff says it is unclear whether the private parties have an actual substantive dispute and absent a compelling explanation from Complainants for their proposed construction, Staff agrees with Respondents and proposes that this term be construed consistently with the construction of the district court judge in the California case. (SMBr. at 12.) Staff submits that the phrase "wherein said central processing unit operates asynchronously to said input/output interface" should be interpreted to mean "the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them." (*Id.* at 13.)

Administrative Law Judge's findings and construction

The Administrative Law Judge finds that the difference between the opposing constructions is syntactical: Complainants enclose the phrase "not derived from" within parenthesis, signifying that the phrase is appositional to the clause "operates independently of." The Administrative Law Judge disagrees that this is a proper construction and agrees with the district court's construction in the California case, which is the exact construction being proposed

by Respondents and Staff here. While the difference in the proposed constructions appears subtle, it is significant. For the reasons set out by Respondents in their brief, the Administrative Law Judge concludes that "asynchronous" as employed by the inventors in the asserted claims of the '336 patent connotes that the timing control of the central processing unit operates not just independently of but is also not derived from the timing control of the input/output interface. Respondents' and Staff's constructions make this point clear; whereas, Complainants' construction does not. As the inventors argued to the patent examiner, "An asynchronous system is one containing two or more independent clock signals. So long as each clock drives independent logic circuitry, such a system is effectively a collection of independent synchronous systems." (*See* RMBr. at 34 (citing Ex. A ("Computational Structures") at 93).)

Therefore, the Administrative Law Judge concludes that the term "wherein said central processing unit operates asynchronously to said input/output interface" means this: "the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them."

IV. EXPERTS

Each party may file one supplemental expert report of no more than 20 pages by April 26, 2013 that addresses those final claim constructions, if any, discussed above in this Markman Order that substantively differ from the constructions proposed by any party. No other issues may be discussed. Each party may submit a rebuttal expert report of no more than 15 pages responding to only those issues raised in the opposing party's supplemental expert report, if any, by May 3, 2013. No additional discovery will be permitted. The Administrative Law Judge will not consider any

requests to change the dates of the hearing based on the issuance of this Markman Order or any supplemental or rebuttal expert reports relating thereto.

V. SETTLEMENT.

The Administrative Law Judge recommends, but does not order, that the parties engage in renewed settlement talks in order to resolve all or portions of this Investigation.

VI. STREAMLINING THE INVESTIGATION.

To the extent that this Markman Order will enable the parties to streamline the remaining portions of this Investigation, such as through the elimination of asserted claims or asserted prior art, the Administrative Law Judge expects the parties to notify the Administrative Law Judge in writing as soon as practicable. The parties should use their best efforts to remove extraneous, unduly repetitive, or unsupported claims or defenses in the period before the hearing.

Within seven days of the date of this document, each party shall submit to the Office of the Administrative Law Judges a statement as to whether or not[7] it seeks to have any portion of this document deleted from the public version. Any party seeking to have any portion of this document deleted from the public version thereof must submit to this office a copy of this document with red brackets clearly indicating any portion asserted to contain confidential business information.

The parties' submissions may be made by facsimile and/or hard copy by the aforementioned date. In addition, an electronic courtesy copy is required pursuant to Ground Rule

[7] This means that parties that do not seek to have any portion redacted are still required to submit a statement to this effect.

PUBLIC VERSION

1.3.2. The parties' submissions concerning the public version of this document need not be filed with the Commission Secretary.

SO ORDERED.

E. James Gildea
Administrative Law Judge

CERTAIN WIRELESS CONSUMER ELECTRONICS DEVICES AND COMPONENTS THEREOF **Inv. No. 337-TA-853**

PUBLIC CERTIFICATE OF SERVICE

I, Lisa R. Barton, hereby certify that the attached **ORDER** has been served by hand upon, the Commission Investigative Attorney, Whitney Winston, Esq., and the following parties as indicated on MAY 7 2013

Lisa R. Barton, Acting Secretary
U.S. International Trade Commission
500 E Street, SW, Room 112
Washington, DC 20436

On Behalf of Complainants Technology Properties Limited LLC and Phoenix Digital Solutions LLC:

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( ) Via Hand Delivery
( ) Via Overnight Delivery
(✓) Via First Class Mail
( ) Other:_____

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( ) Via Overnight Delivery
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On Behalf of Respondents Acer Inc., Acer America Corporation, Amazon.com Inc. and Novatel Wireless, Inc.:

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CERTAIN WIRELESS CONSUMER ELECTRONICS DEVICES AND COMPONENTS THEREOF **Inv. No. 337-TA-853**

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION and HTC AMERICA, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED,

Defendants.

Case No. 5:08-CV-00882 PSG

(Related to Case No. 5:08-CV-00877 PSG)

PLAINTIFFS' NOTICE OF MOTION AND MOTION FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT AND NO WILLFUL INFRINGEMENT OF U.S. PATENT NO. 5,809,336

Complaint Filed: February 8, 2008
Trial Date: September 23, 2013

Date: August 13, 2013
Time: 10:00 a.m.
Place: Courtroom 5, 4th Floor
Judge: Hon. Paul S. Grewal

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NOTICE OF MOTION AND MOTION

PLEASE TAKE NOTICE that Plaintiffs HTC Corporation and HTC America, Inc. (collectively "Plaintiffs" or "HTC") move, pursuant to Federal Rule of Civil Procedure 56, for (1) summary judgment of non-infringement for all of the HTC products accused under U.S. Patent No. 5,809,336 (the "'336 patent") by Defendants Technology Properties Limited, Alliacense Limited, and Patriot Scientific Corporation (collectively "TPL" or "Defendants"); and (2) summary judgment of no willful infringement of the '336 patent. This Motion is filed pursuant to the briefing schedule established by the Court's order of July 3, 2013, as amended on July 12, 2013. (Doc. Nos. 452, 456.) This Motion is based on the Memorandum of Points and Authorities set forth below, the supporting declaration of Kyle D. Chen ("Chen Decl.") and exhibits thereto, and such other matters as may be presented at the hearing on HTC's motion and allowed by the Court.

MEMORANDUM OF POINTS AND AUTHORITIES

I. INTRODUCTION

TPL's infringement case against HTC fails because TPL cannot establish at least two claim limitations recited in every independent claim. The accused HTC products do not practice these limitations, and TPL has no evidence that they do. Summary judgment of non-infringement is therefore warranted.

First, every independent claim of the '336 patent recites an "*entire* ring oscillator variable speed system clock" (claims 1, 11), an "*entire* oscillator" (claims 6, 13), or "an *entire* variable speed system clock" (claims 10, 16) disposed on the same integrated circuit substrate as the CPU. (These terms are collectively referred to as the "entire" terms in this brief.) Two other judges have held that the patentee during prosecution expressly disclaimed any microprocessor system in which the clock or oscillator that clocks the central processing unit ("CPU") relies upon a reference signal from an external crystal.

Most recently, in a parallel International Trade Commission ("ITC") Investigation No. 337-TA-853 (the "ITC investigation"), Administrative Law Judge E. James Gildea issued an exhaustive 75-page claim construction order in which he agreed with and adopted HTC's constructions for the same "entire" limitations at issue in this motion. Judge Gildea's order

involved the identical asserted claims of the '336 patent and, although it is not controlling on this Court, is highly persuasive in that it thoroughly evaluates these terms from the '336 patent. Before that, Judge Ward of the Eastern District of Texas (now retired) construed "*entire* ring oscillator variable speed system clock" (claims 1, 11) from the '336 patent and similarly found that the patentee disclaimed an arrangement in which the on-chip ring oscillator directly relies upon a reference signal from an external crystal. Both judges correctly found that the patentee made clear and unambiguous disclaimers in order to obtain the '336 patent. And even TPL, in several briefs it has filed with this Court, has acknowledged these same disclaimers. Under those disclaimers, HTC's accused products cannot infringe and summary judgment of non-infringement is warranted.

Second, each independent claim of the '336 patent requires that the speed of the CPU clock "vary" with the process, voltage, and temperature ("PVT") parameters. TPL offers no evidence whatsoever that HTC's accused products meet this limitation. TPL's expert relies entirely on speculation and "generally accepted principles" relating to semiconductor circuits, but provided no specific factual analysis and no application of those "generally accepted principles" to any HTC product. TPL did not perform any testing of the accused products. And when TPL's expert, who has worked on this and the related matters since 2007, was asked at his deposition if he even looked into whether it would be possible to perform those tests, he remarkably responded: "I haven't. I haven't had time to do it."

But HTC did perform those tests. They showed that the accused products do not exhibit the variation required by the claims. The accused CPU clocks are so stable, in fact, that they fall within what one of ordinary skill in the art would regard as "fixed" speed clocks. Summary judgment of non-infringement is therefore warranted with respect to this claim element as well.

TPL cannot show infringement—let alone willful infringement—of the '336 patent. The undisputed record establishes that HTC's accused products not only fail to satisfy these claim limitations, but also fall squarely within the realm of the prior art microprocessor systems that the patentee disclaimed during prosecution. Because TPL's claims cannot be (and have not been) construed to recapture subject matter it disclaimed, HTC cannot infringe and summary judgment should be granted with respect to all claims of the '336 patent.

II. BACKGROUND

A. Relevant Procedural History

HTC filed this declaratory judgment action on February 8, 2008. TPL, after a protracted and failed attempt to transfer this action to the Eastern District of Texas, counterclaimed for infringement of U.S. Patent Nos. 5,440,749 (the "'749 patent"), 5,530,890 (the "'890 patent") 5,809,336 (the "'336 patent"), and 6,598,148 (the "'148 patent") (collectively, the "patents-in-suit"). (*See* Doc No. 60.) This case was delayed during its pendency due, in large part, to TPL's attempt to transfer the actions, reexaminations of the patents-in-suit, and start-and-stop claim construction proceedings caused by two judicial reassignments.

More specifically, this case was originally assigned to Judge Fogel but reassigned to Chief Judge Ware on September 1, 2011. (Doc. No. 320.) At the time of the first reassignment, the parties had completed briefing on claim construction and were awaiting a claim construction hearing. Judge Ware directed the parties to redo claim construction briefing and, on June 12, 2012, issued a "First Claim Construction Order" construing a handful of disputed terms, declining to consider certain other terms, and requesting further briefing on the term "ring oscillator" in the '336 patent. (Doc. No. 364.) With respect to the three "entire" terms from the '336 patent, however, Judge Ware construed only one of those terms ("an entire variable speed system clock") and did not address the other two. On August 15, 2012, in light of Judge Ware's retirement, this case was reassigned to Judge Grewal. (Doc. No. 370.)

HTC filed its supplemental brief on October 21, 2012 addressing Judge Ware's questions regarding the term "ring oscillator" (a portion of one of the three "entire" terms of the '336 patent), and specifically noted that Judge Ware did not construe the three "entire" terms and that it may therefore seek construction following resolution of the "ring oscillator" issue. (*See* Doc. No. 394, at 1 n.1.) On December 4, 2012, Judge Grewal issued a further claim construction order responding to the additional briefing ordered by Judge Ware, and ruled on various motions for reconsideration filed on various aspects of Judge Ware's claim construction rulings. (Doc. No. 410.)

On December 7, 2012, counsel for HTC contacted counsel for TPL and indicated that following Judge Grewal's construction of "ring oscillator," it intended to file a motion to construe the three "entire" limitations from the '336 patent that had not been addressed. (*See* Declaration of Kyle D. Chen in Support of Motion for Summary Judgment ("Chen Decl."), Ex. 2 (December 2012 e-mail chain).) After further communications between counsel, HTC notified TPL that it believed the issues relating to the "entire" terms could more efficiently and effectively be taken up by the Court in connection with a summary judgment motion of non-infringement. (*Id.*) TPL responded: "Sounds good. Thanks." (*Id.*)

B. Proceedings in the Parallel ITC Investigation

As this case was proceeding in early 2013, the exact same claim construction issues regarding the "entire" limitations were being litigated in the ITC investigation before Judge Gildea. On April 18, 2013, after extensive briefing from TPL, HTC, and the other respondents and the ITC Staff, and following a full day hearing, Judge Gildea issued a 75-page claim construction order construing various terms from the '336 patent—including all three of the "entire" terms from the '336 patent. (Chen Decl. Ex. 3 (04/18/2013 Public ITC Order).) In his order, Judge Gildea adopted HTC's proposed constructions for all three of the "entire" terms. (*Id.* at 37-42.) Judge Gildea specifically rejected TPL's construction on the ground that it "does not convey the essential point made by the applicants in seeking to gain acceptance of the examiner for their purported invention by asserting that the ring oscillator variable speed clock 'does not utilize external components.'" (*Id.* at 39 (citation omitted).)

On June 4, 2013, TPL served its Final Infringement Contentions and the opening report of its expert on infringement issues, Dr. Vojin G. Oklobdzija. At that time, TPL also withdrew its claims of infringement as to the '148 and '749 patents, and as such, is only asserting the '336 and '890 patents against HTC. Dr. Oklobdzija was deposed on July 13 and 15, 2013.

C. Overview of '336 Patent

Because this Court has received multiple rounds of briefing on the '336 patent, (*see* Doc Nos. 245, 349, 394), HTC will provide only a brief summary of the patent here:

To control the pace of operation of a microprocessor, its CPU must be driven by a "clock" that generates a timing signal. The '336 patent explains that traditional microprocessors relied on an *external*, *fixed speed* crystal to generate the internal timing signal for the CPU. The alleged invention removes reliance on such external, fixed speed crystal and instead relies on an *internal*, *variable speed* clock or oscillator located entirely inside the integrated circuit substrate.

In particular, the '336 patent is directed towards a variable speed clock located entirely inside the same integrated circuit substrate as the CPU. ('336, 16:60-17:2.)[1] The '336 specification explains that a high speed microprocessor must "operate over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing," which "all affect transistor propagation delays." (*Id.* at 16:44-48.) These parameters—"process," "voltage," and "temperature"—are referred to as "PVT" parameters.

As the specification and the prosecution history explain, prior art microprocessor systems relied on an external, fixed speed crystal to generate the internal clock signal for the CPU. ('336, 16:48-50, 17:12-13; *see* Part IV.A.1, *infra*.) Because the speed of the CPU clock signal is fixed and does not vary based on PVT parameters, it must be designed to clock the CPU at a speed that is slow enough to ensure error-free operation during worst-case conditions for all possible PVT parameters. (*Id.*) As a result, prior art microprocessor systems "must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse [sic] case conditions." ('336, 16:50-53.)

To overcome this purported problem, the '336 patent teaches a microprocessor system in which the CPU is clocked by an internal clock or oscillator that adjusts its speed to match the CPU's maximum capabilities automatically at any given time under the then existing PVT parameters. ('336, 3:26-34 (Summary of the Invention).) The other devices with which the CPU must communicate, however, cannot operate at a variable speed, so the claimed microprocessor system requires a second or external clock that is independent of the CPU's variable speed clock or

[1] A copy of the '336 patent is attached as Exhibit 1 to the Chen Declaration.

oscillator. (*Id.*) The '336 patent explains that this second or external clock connected to the input/output (I/O) interface is a fixed speed crystal clock, which is the same type of clock relied upon by prior art systems to also clock the CPU. ('336, 17:32-34.)

Unlike the I/O interface's fixed speed crystal clock that varies so little in response to the PVT parameters,[2] the frequency (*i.e.*, speed) of the claimed variable speed clock or oscillator for the CPU varies significantly and is ***determined*** by the PVT parameters. ('336, 16:59-60 ("The ring oscillator frequency is determined by the parameters of temperature, voltage, and process . . . ."), 17:32-34 ("By decoupling the variable speed of the CPU **70** from **the fixed speed of the I/O interface 432**, optimum performance can be achieved by each.") (emphasis added), and Fig. 17 (crystal clock **434**).) For example, the '336 specification discloses that the speed of the variable speed clock will be 100 megahertz at room temperature, but will slow to 50 megahertz if the temperature rises to 70°C/158° F, and may vary by as much as a factor of four (*i.e.*, by as much as 400%) depending on all PVT parameters. ('336, 16:59-63, 17:21-22.)

III. LEGAL STANDARD FOR SUMMARY JUDGMENT

To evaluate claims of patent infringement, the Court first construes the claims as a matter of law and then compares the claims as construed to the accused device(s). *See Bayer AG v. Elan Pharm. Research Corp.*, 212 F.3d 1241, 1247 (Fed. Cir. 2000). The absence of even a single claim limitation precludes a finding of infringement. *Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1330 (Fed. Cir. 2001). To prove infringement, TPL bears the burden of proving that the accused products meet each element of each asserted claim. *Id.* A party seeking summary judgment does not need to present affirmative evidence of non-infringement. *See Celotex Corp. v. Catrett*, 477 U.S. 317, 326 (1986). To obtain summary judgment of non-infringement, "nothing more is required than the filing of a summary judgment motion stating that the patentee had no evidence of infringement and pointing to the specific ways in which accused systems did not meet the claim limitations." *Exigent Tech., Inc. v. Atrana Solutions, Inc.*, 442 F.3d 1301, 1309 (Fed.

[2] For example, named inventor Russell Fish, III testified that although crystal frequencies will vary slightly with temperature, "it is a fixed clock for all intents and purposes" because the "crystal is as fixed as you can make it." (Chen Decl. Ex. 4 (Fish ITC Depo.) at 145:21-24.)

Cir. 2006). This case presents a particularly compelling case for summary judgment because there is no material disagreement between TPL and HTC (or their respective experts) about how the accused HTC products operate. The facts required to establish entitlement to summary judgment were readily admitted or acknowledged by TPL's own expert. The Federal Circuit has repeatedly emphasized that such a case is particularly suited to summary judgment. *See, e.g.*, *MyMail, Ltd. v. Am. Online, Inc.*, 476 F.3d 1372, 1378 (Fed. Cir. 2007).

IV. HTC DOES NOT INFRINGE THE '336 PATENT

The purported "problem" that the '336 patent was attempting to solve is reflected in at least two express limitations in every asserted claim: (1) the "entire" clock limitations and (2) the requirement that the speed of the clock or oscillator clocking the CPU be "varying" with the PVT parameters. Both of these limitations go to the core of the purported problem addressed by the '336 patent. TPL cannot show that the accused HTC products satisfy either of these claim limitations, literally or under the doctrine of equivalents.

The reason HTC does not infringe is straightforward: HTC's accused products did not adopt the "solution" described in the '336 patent. Those products, if anything, embrace the purported "problem" the '336 patent sought to solve. HTC's accused products, like the prior art, use a fixed speed clock that relies on an external crystal. And like the prior art, those products generate a stable and fixed clock signal frequency that exhibits only minimal variation based on a wide range of PVT parameters—the direct opposite of the system described in the '336 patent.

In summary, the HTC accused products, much like the prior art, rely on a fixed-frequency, crystal-based clocking system that intentionally excludes the purported benefit of varying frequency based on PVT parameters.

A. The Accused HTC Products Do Not Satisfy the "Entire" Limitations

Every independent claim of the '336 patent recites an "entire" ring oscillator, oscillator, or variable speed clock disposed on the same substrate as the CPU. These "entire" terms fall into the following three groups:

- "an entire ring oscillator variable speed system clock in said single integrated circuit" (claims 1, 11);

- "an entire oscillator disposed upon said integrated circuit substrate" (claims 6, 13); and
- "an entire variable speed system clock disposed upon said integrated circuit substrate" (claims 10, 16).

To convince the examiner to allow their claims over invalidating prior art, as explained below, the applicants repeatedly and unambiguously told the PTO that their allegedly inventive microprocessor system did not rely on any external crystal or frequency generator of a fixed speed, and that their internal clock or oscillator speed is variable. Those clear statements and disclaimers must be reflected in the construction of the three "entire" terms. And because the only infringement theory proffered for those limitations relies on an interpretation that was expressly disclaimed, the Court should grant summary judgment of non-infringement.

1. The "Entire" Limitations Should Be Construed To Exclude Reliance on a Control Signal or an External Crystal/Clock Generator To Generate a Clock Signal

The first step in any infringement analysis is to construe the disputed language of the asserted claim. *Freedman Seating Co. v. Am. Seating Co.*, 420 F.3d 1350, 1356-57 (Fed. Cir. 2005). Judge Ware construed only one of the "entire" terms prior to his retirement. As the Federal Circuit has observed, "district courts may engage in a rolling claim construction, in which the court revisits and alters its interpretation of the claim terms as its understanding of the technology evolves." *Pressure Prods. Med. Supplies, Inc. v. Greatbatch Ltd.*, 599 F.3d 1308, 1316 (Fed. Cir. 2010). This Court should now address all three "entire" limitations together and, as explained below, should adopt the construction adopted by Judge Gildea for all three terms.[3] Because the construction of the "entire" limitations is fundamental to the question of infringement, the Court should resolve this issue now. *See O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008) ("When the parties present a fundamental dispute regarding the scope of a claim term, it is the court's duty to resolve it.").

[3] Although HTC believes that this Court should apply Judge Gildea's consistent constructions across all three "entire" terms, as explained in Part IV.A.2, below, summary judgment of non-infringement of claims 10 and 16 would also be warranted under Judge Ware's construction of the single "entire" term that he construed from those claims.

HTC has proposed a set of consistent and parallel constructions of the three "entire" terms as set forth below:

Claim Term from the '336 Patent	HTC's Proposed Construction (Also Adopted by Judge Gildea)
an entire ring oscillator variable speed system clock in said single integrated circuit (claims 1, 11)	a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an external crystal/ clock generator to generate a clock signal
"an entire oscillator disposed upon said integrated circuit substrate" (claims 6, 13)	an oscillator that is located entirely on the same semiconductor substrate as the central processing unit and does not rely on a control signal or an external crystal/ clock generator to generate a clock signal
"an entire variable speed system clock disposed upon said integrated circuit substrate" (claims 10, 16)	a variable speed clock that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an external crystal/ clock generator to generate a clock signal

The key component of HTC's proposal is that each of the "entire ring oscillator," "entire oscillator," and "entire variable speed system clock" does not "rely on a control signal or an external crystal/ clock generator to generate a clock signal." This requirement captures the clear disclaimers made by the applicants during the prosecution of the '336 patent and is consistent with the specification's teachings and its criticisms of the prior art. This issue goes to the heart of this case as every accused '336 product includes an off-chip, fixed speed crystal that controls the frequency of the alleged on-chip clock or oscillator. Because the applicants clearly and unambiguously disclaimed on-chip oscillators and clocks that rely on external off-chip crystals and off-chip clock generators, HTC's proposed constructions should be adopted.

a. The Specification Describes the Importance of a Variable Speed Clock that Does Not Rely on an External Crystal or External Frequency Generator

One of the key features recited in the claims is the requirement that the "entire" variable speed clock or oscillator be located on the same integrated circuit substrate as the CPU that it clocks. The specification makes clear that, as a consequence of locating both the variable speed clock or oscillator and the CPU on the same substrate, the speed of such clock or oscillator will

vary based on the PVT (process, voltage, and temperature) parameters to which the integrated circuit is then subjected. ('336, 16:59-60, 65-67, 17:5-10, 19-22.) Performance of the CPU is thereby allegedly optimized such that the "CPU **70** will always execute at the maximum frequency possible, but never too fast." ('336, 16:67-17:2.)

In doing so, the specification describes an alleged improvement over the prior art solution of clocking a CPU with a fixed clock whose frequency is controlled by an external fixed speed crystal or clock generator. As the specification explains, this fixed speed clock is always set at a frequency well below the maximum theoretical frequency at which the CPU can operate under optimal PVT parameters because, by definition, a fixed speed clock cannot vary its speed with the PVT parameters. ('336, 16:44-53.) This setting is necessary to account for times when the CPU is operating under the worst-case PVT parameters. (*Id*.) But according to the '336 patent, setting the frequency at this lower level is inefficient. (*Id.*)

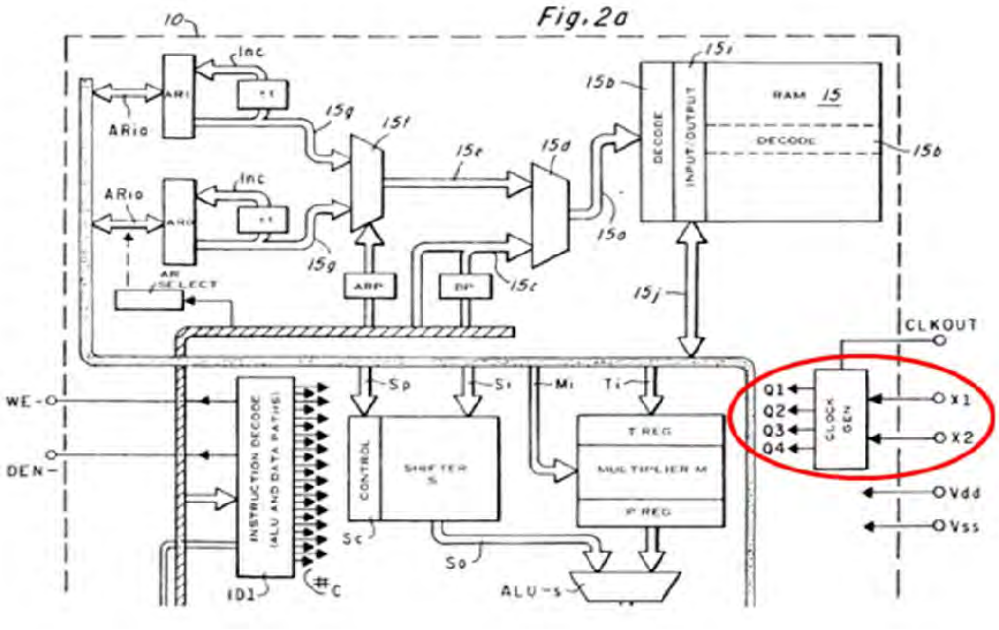
The claimed invention thus seeks to overcome this alleged inefficiency by fabricating the CPU and its clock entirely on the same substrate so that the PVT parameters affect both the CPU and the clock in the same way, without the CPU clock being controlled by an external fixed speed clock source. (*Id*. at 16:44-17:10, 19-22.) As a result, the CPU and clock's respective frequencies automatically vary in response to changes in the PVT parameters. (*Id*.)

b. The Applicants Repeatedly Disclaimed Reliance on External Crystals and External Frequency Generators

During the original prosecution of the '336 patent, the applicants repeatedly distinguished their purported invention from the prior art on the basis that their on-chip clock and on-chip oscillator do not rely on an external crystal or an external frequency generator. In doing so, the applicants clearly and unambiguously disclaimed any clock or oscillator, even though fabricated on the same substrate as the CPU, that relies on an external crystal or frequency generator.

Specifically, during the original prosecution, the PTO issued a non-final rejection based on U.S. Patent No. 4,503,500 to Magar ("Magar"), Fig. 2a of which is reproduced below. (Chen Decl. Ex. 5 ('336 prosecution history, Apr. 3, 1997 rejection) (TPL85300002433-34).) In his rejection, the examiner asserted that the "CLOCK GEN" (clock generator) circuitry in Fig. 2a of

Magar was fabricated on the same microprocessor substrate 10 as the CPU, as required by the claims. (*Id.* at 2 (TPL85300002434).) *See* Magar, Fig. 2a reproduced below (red circle added).



In response, the applicants attempted to distinguish Magar on the basis that an external off-chip crystal (connected to the X1 and X2 inputs in the figure above) drove the clock in Magar:

> A review of the Magar reference shows that it is apparently no more pertinent than prior art acknowledged in the application, in that ***the clock disclosed in the Magar reference is in fact driven by a fixed frequency crystal, which is external to the Magar integrated circuit***.

(Chen Decl. Ex. 6 ('336 prosecution history, July 7, 1997 Amendment) at 2 (emphasis added) (TPL85300002426).) The applicants further emphasized the difference between the claimed variable speed clock and Magar's clock generator's reliance on the frequency of an external crystal:

> Contrary to the Examiner's assertion in the rejection that 'one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock vary together due to manufacturing variation, operating voltage and temperature of the IC [integrated circuit],' one of ordinary skill in the art should readily recognize that the speed of the CPU and clock ***do not*** vary together due to manufacturing variation, operating voltage, and temperature of the IC in the Magar processor . . . ***This is simply because the Magar microprocessor clock is <u>frequency controlled</u> by a crystal which is also external to the microprocessor. Crystals are by design fixed frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating***

> ***voltage and temperature. The Magar microprocessor in no way contemplates a variable speed clock as claimed.***

(*Id*. at 3-4 (second emphasis added) (TPL85300002427-28).) Through these exchanges, the applicants unambiguously disclaimed clocks and oscillators that rely on an external crystal for frequency control.

The PTO subsequently issued a second rejection based on Magar. In response, the applicants amended their claims to explicitly require that ***the entire*** oscillator/clock be on the same integrated circuit substrate as the CPU.[4] (Chen Decl. Ex. 7 ('336 prosecution history, Feb. 10, 1998 Amendment) at 1-2 (TPL85300002399-400).) Along with this amendment, the applicants again tried to distinguish Magar from the claimed invention, arguing that Magar's clock generator could not operate properly without the use of an external component such as a crystal. In doing so, the applicants directed the examiner to Magar's disclosure at 15:26-27, which states that "chip 10 includes a clock generator 17 which has two external pins X1 and X2 to which a crystal (or external generator) is connected." (*Id*. at 4 (TPL85300002402).) The applicants then, consistent with their earlier statements, further distinguished an external crystal by stating:

> [W]hile most of Magar's clock (generator) circuitry is on the IC, ***the entire oscillator, which because it requires an external crystal, is not***.

(*Id*. at 4 (emphasis added) (TPL85300002402).) The applicants reinforced their disclaimers by identifying "the essential difference" between Magar's fixed-frequency clock and the variable speed clock of the '336 patent—that Magar's clock relies on an external crystal while the frequency of the '336 clock (in Figure 18) is determined by PVT parameters:

> The signals PHASE 0, PHASE 1, PHASE 2 and PHASE 3 in Applicants' Fig. 18 are synonymous with Q1, Q2, Q3 and Q4 depicted in Magar Fig. 2a. The ***essential difference*** is that the ***frequency or rate of the PHASE 0, PHASE 1, PHASE 2 and PHASE 3 signals is determined by the processing and/or***

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[4] Then pending claim 19 was amended to recite "an entire ring oscillator variable speed system clock in said single integrated circuit," claim 73 was amended to recite "an entire oscillator disposed upon said integrated circuit substrate," and claim 78 was amended to recite "an entire variable speed clock disposed upon said integrated circuit substrate." (Chen Decl. Ex. 7 ('336 prosecution history, Feb. 10, 1998 Amendment) at 1-2.)

> ***operating parameters of the integrated circuit*** containing the Fig. 18 circuit, ***while the frequency or rate of the Q1, Q2, Q3 and Q4 signals depicted in Magar Fig. 2a are determined by the fixed frequency of the external crystal*** connected to the circuit portion outputting the Q1, Q2, Q3 and Q4 signals shown in Magar Fig. 2a.

(*Id.* (emphasis added).) The applicants concluded their argument about Magar by specifically distinguishing their claimed system from an external crystal used for frequency control or oscillation:

> The Magar teaching . . . is specifically distinguished from the instant case in that it is both fixed frequency (being crystal based) and ***requires an external crystal or external frequency generator***.

(*Id.* at 5 (emphasis added) (TPL85300002403).)

The applicants' statements to the PTO made clear that the alleged invention requires an "entire" on-chip clock or "entire" oscillator that does not rely on an external crystal or external frequency generator. Magar's clock generator was repeatedly distinguished as not disclosing the claimed "entire" clock because Magar's clock generator relies on an external crystal or external frequency generator. The claimed "entire" clocks and "entire" oscillators cannot therefore be construed to encompass reliance on an external crystal or external frequency generator. *See Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319, 1325 (Fed. Cir. 2002) ("Explicit arguments made during prosecution to overcome prior art can lead to a narrow claim interpretation because '[t]he public has a right to rely on such definitive statements made during prosecution.'"); *Am. Piledriving Equip. v. Geoquip, Inc.*, 637 F.3d 1324, 1336 (Fed. Cir. 2011) ("[A]n applicant's argument that a prior art reference is distinguishable on a particular ground can serve as a disclaimer of claim scope even if the applicant distinguishes the reference on other grounds as well.").[5]

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[5] The patentee's disclaimers are also consistent with testimony from the named inventors describing their alleged invention. Although inventor testimony is not part of the intrinsic record, it may be used to "provide background information, including explanation of the problems that existed at the time the invention was made and the inventor's solution to these problems." *Voice Techs. Group, Inc. v. VMC Sys., Inc.*, 164 F.3d 605, 615-16 (Fed. Cir. 1999). In this case, inventor Charles Moore testified that the variable speed clock of the alleged invention would not be connected, directly or indirectly, to a crystal oscillator. (Chen Decl. Ex. 8 (Moore E.D. Tex. Depo.) at 23:15-17 (TPL8531710898).) The other named inventor, Russell Fish, III, agreed. (Chen Decl. Ex. 4 (Fish ITC Depo.) at 201:2-9.) Mr. Fish also testified that the presence of inputs into the variable speed clock or oscillator would indicate a system that did not include the '336 clock. (*Id.* at 83:14-84:12.)

c. The Applicants Also Repeatedly Disclaimed Reliance on Control Signals To Control the Clock

In addition to disclaiming reliance on an external crystal or clock generator, the applicants also disclaimed reliance on control signals to control the clock or oscillator. The first of these disclaimers occurred in response to the examiner's rejection of the claims in light of U.S. Patent No. 4,670,837 to Sheets ("Sheets"). In attempting to overcome Sheets, the applicants distinguished microprocessors that rely on frequency control information from an external source:

> ***The present invention does not similarly rely upon provision of frequency control information to an external clock***, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit ***obviates the need for provision of the type of frequency control information described by Sheets . . . Sheets' system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention***.

(Chen Decl. Ex. 9 ('336 prosecution history, Apr. 15, 1996 Amendment) at 8 (emphasis added) (TPL85300002473).) In response to a subsequent rejection based on Sheets, the applicants went even further and disclaimed the use of controlled oscillators altogether, regardless of whether the control is on-chip or not:

> Even if the examiner is correct that the variable clock in Sheets is in the same integrated circuit as the microprocessor of system **100*, that still does not give the claimed subject matter.*** In Sheets, a command input is required to change the clock speed.

(Chen Decl. Ex. 10 ('336 prosecution history, January 8, 1997 Amendment) at 4 (emphasis added) (TPL85300002449).)

Simply having a CPU clock on the chip was not enough, according to the applicants, to meet the claimed invention because controlling the on-chip ring oscillator's speed using a command signal "does not give the claimed subject matter." (*Id.*) Indeed, in response to a subsequent rejection based on Magar, the applicants left no doubt that, unlike "all cited references," the on-chip clock or on-chip oscillator of their purported invention is completely free of inputs and extra components:

> Crucial to the present invention is that . . . when the fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together. ***This differs from all cited references in that . . . the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so.***

(Chen Decl. Ex. 6 ('336 prosecution history, July 7, 1997 Amendment) at 5 (emphasis added) (TPL85300002429).) This prosecution statement confirms the applicants' clear disclaimer of any reliance on input control signals. Accordingly, HTC's proposed constructions include the requirement that the clock or oscillator "does not rely on . . . a control signal to generate a clock signal," and should be adopted.

d. HTC's and Judge Gildea's Construction Is Consistent with the Previous Construction by Judge Ward and TPL's Positions in this Litigation

Judge Gildea is not the only judge who has found that the applicants disclaimed an on-chip clock that relies on a control signal or an external crystal or clock generator to generate a clock signal.[6] The '336 patent was also the subject of prior litigation in the Eastern District of Texas before Judge Ward. *See Tech. Props. Ltd. v. Matsushita Elec. Indus. Co., Ltd.*, 514 F. Supp. 2d 916 (E.D. Tex. 2007). Judge Ward construed an "entire ring oscillator variable speed system clock in said single integrated circuit" of claim 1 as "a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not directly rely on a command input control signal or an external crystal/clock generator to generate a clock signal." *Id.* at 926. Judge Ward explained: "The Court agrees with the defendants that the applicant disclaimed the use of an input control signal and an external crystal/clock generator to generate a clock signal." *Id.* (emphasis added).[7]

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[6] The ITC Staff Attorney Whitney Winston, a graduate from the Massachusetts Institute of Technology, in this parallel ITC investigation also agrees that HTC's proposed constructions "accurately capture the patentee's clear disclaimer." (Chen Decl. Ex. 11 (02/08/2013 OUII Opening Markman Brief) at 9.)

[7] Judge Ward's construction largely mirrors the construction adopted by Judge Gildea and proposed by HTC. The only differences are that Judge Gildea did not include certain language from Judge Ward's construction ("*directly* rely upon," "*command input* control signal"). Accordingly, while Judge Ward's prior claim construction correctly recognized the applicant's disclaimers regarding reliance on an external crystal/clock generator or control signal, the

TPL itself acknowledged this disclaimer by repeatedly urging this Court to adopt Judge Ward's construction—in at least three claim construction briefs filed with this Court. (*See* Doc. No. 228 at 18 (12/09/2010 TPL Claim Construction Brief); Doc. No. 258 at 18 (02/11/2011 TPL Claim Construction Brief); Doc. No. 339 at 19 (12/23/2011 TPL Claim Construction Brief).) During the ITC case, however, TPL retreated from its long-standing position and sought a different construction. (Chen Decl. Ex. 3 (04/18/2013 Public ITC Order) at 20.)

2. The HTC Accused Products Do Not Meet the "Entire" Limitations as a Matter of Law

After the relevant claim language has been construed, the second step in an infringement analysis is to compare the accused product with the claim as construed by the Court. *See Freedman Seating Co.*, 420 F.3d at 1357. TPL can present no evidence to raise a genuine issue of material fact as to whether the accused HTC products rely on an external crystal or clock to generate a clock signal for the CPU. As shown below, there can be no infringement because the accused HTC products operate in precisely the same manner as the prior art distinguished during prosecution—they rely on an external crystal or clock to generate a clock signal.

According to TPL's expert, the on-chip clock that TPL contends meets the "entire" limitations on all of the accused HTC products is based on a structure known as a "phase-locked loop" ("PLL"). TPL contends that the PLLs in the accused HTC products include either a voltage-controlled oscillator ("VCO") or a current-controlled oscillator ("ICO"). (*See* Chen Decl. Ex. 12 (Oklobdzija 07/13/2013 Depo.) at 56:13-57:23.) These VCOs or ICOs, according to TPL's expert, "directly clock the CPU." (*Id.* at 57:5-9.)

The problem with TPL's infringement theory, however, is that the oscillators in the accused products indisputably rely on an external crystal or clock generator to clock the CPU. Similar to a "cruise control" in an automobile that maintains a constant speed, the PLLs and their VCOs and ICOs in the accused HTC products maintain a stable CPU frequency. (Declaration of

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"directly" and "command input" qualifiers in that construction should not be adopted here because there is no support for that specific language from the intrinsic record.

Thomas A. Gafford ("Gafford Decl.") Ex. 1 (Gafford 07/02/2013 Non-Infringement Rep.), ¶ 149.) The PLLs accomplish this stability by relying on an input signal from an external signal, known as a "reference" signal, that provides a fixed and stable frequency. (Chen Decl. Ex. 12 (Oklobdzija 07/13/2013 Depo.) at 57:10-15, 57:24-58:18; Chen Decl. Ex. 14 (Oklobdzija 06/04/2013 Infringement Rep.), ¶ 91 ("That other reference frequency is usually produced externally to the chip and that oscillator is encapsulated in a noise free, temperature and voltage controlled environment assuring the frequency stability of the reference signal.").)

All of the PLLs in the HTC accused products receive this external "reference" signal, according to TPL's expert, from either an external crystal or an external clock generator. (*See* Chen Decl. Ex. 12 (Oklobdzija 07/13/2013 Depo.) at 58:14-18.) In the words of TPL's expert, "they all must have a reference. That's essential part of PLL." (*Id.*; *see also id.* at 59:3-7 ("[I]t's the nature of PLL that must receive a reference. Now, that reference can be either an external clock generator or external crystal. In both cases the reference is external.").)

This "reference" signal directly controls the frequency of the on-chip oscillator. In particular, the PLL circuitry on the chip takes the external reference signal and "multiplies" it by a constant value to obtain a higher frequency. (Chen Decl. Ex. 14 (Oklobdzija 06/04/2013 Infringement Rep.), ¶ 91.) For example, in the accused Qualcomm MSM7x30 chip, a PLL clocks the CPU at a fixed speed of 768 MHz. The PLL circuitry on the chip obtains this frequency by taking the reference frequency from the external crystal—19.2 MHz—and multiplying it by 40. A PLL maintains this fixed frequency by constantly comparing the frequency of the oscillator to the crystal frequency, and correcting the oscillator frequency such that it remains a constant multiple of the reference frequency supplied by the crystal. (Gafford Decl. Ex. 1 (Gafford 07/02/2013 Non-Infringement Rep.), ¶ 40*; see also* Chen Decl. Ex. 14 (Oklobdzija 06/04/2013 Infringement Rep.), ¶ 122 ("The reference clock provides the timing reference used by the PLL. The PLL uses this reference to calibrate its own ring oscillator VCO, which generates the clock signal.").) The frequency of the on-chip clock in the accused HTC products, therefore, directly depends on the frequency of the external crystal.

HTC's expert, Mr. Gafford, was also able to empirically confirm that the accused HTC products rely on an external crystal/clock generator. (Gafford Decl. Ex. 1 (Gafford 07/02/2013 Non-Infringement Rep..), ¶¶ 110-15, 203-09.) He ran a series of tests on certain HTC accused products in which he was able to increase or decrease the reference frequency and measure its effect on the frequency produced by the PLL. (*Id.*) His testing showed a linear relationship between the reference frequency and the frequency of the on-chip PLL—if you increase the frequency of the reference signal, for example, the frequency of the on-chip PLL increases. (*Id.* ¶¶ 204-09.) And if you decrease the frequency of the reference signal, the frequency of the on-chip PLL decreases in direct response. (*Id.*) TPL's expert testified that he was "not surprised" with Mr. Gafford's results. (*See* Chen Decl. Ex. 12 (Oklobdzija 07/13/2013 Depo.) at 126:12-127:7.) Nor should he have been surprised because "in general it's true if we have a PLL as we have described that depends on the reference[, a]nd so if the reference is affected, then the output frequency will be affected as well." (*Id.* at 84:17-22). And these results were not surprising given that the accused phones were *designed* to maintain a fixed and stable frequency based on the crystal reference.

Non-infringement would also be warranted even if the Court applied Judge Ware's construction of "an entire variable speed system clock" as to claims 10 and 16, which he construed as "a variable speed clock that is located ***entirely*** on the same semiconductor substrate as the central processing unit." (Doc. No. 364, at 19 (emphasis added).) As explained previously, the PLL and the external crystal are inextricably intertwined components of the clocking mechanism for the CPU. Because it is undisputed that the crystal is not on the same semiconductor substrate as the accused oscillator, TPL cannot show that the clock is located entirely on the same substrate as required under Judge Ware's construction. As the applicants emphasized in discussing the "entire" terms in the '336 patent during the original prosecution, "while most of Magar's clock (generator) circuitry is on the IC, the entire oscillator, which because it requires an external crystal, is not." (Chen Decl. Ex. 7 ('336 prosecution history, Feb. 10, 1998 Amendment) at 4 (emphasis added) (TPL85300002402).)

A finding of non-infringement, as noted previously, is entirely consistent with the prosecution history in which the applicant argued that Magar was "distinguished from the instant case in that it is both fixed frequency (being crystal based) and ***requires an external crystal or external frequency generator***." (*Id.* at 5 (TPL85300002403).) "Claims may not be construed one way in order to obtain their allowance and in a different way against accused infringers." *Southwall Techs., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995). For all of these reasons, therefore, TPL cannot establish infringement of the '336 patent, literally or under the doctrine of equivalents, as a matter of law.

B. The Accused HTC Products Also Do Not Satisfy the "Varying" Limitations as a Matter of Law

The accused HTC products do not infringe for another reason that is separate from the "entire" limitations discussed above. Each independent claim of the '336 patent requires that the variable speed clock or oscillator be "varying" based on the PVT parameters as follows:

Claim Term from the '336 Patent (in Underlining with Surrounding Language)
"a processing frequency capability of said central processing unit and ***a speed of said*** ring oscillator variable speed system ***clock varying*** together ***due to said manufacturing variations and due to at least operating voltage and temperature*** of said single integrated circuit" (claims 1, 11)
"***varying*** the processing frequency of said first plurality of electronic devices and ***the clock rate*** of said second plurality of electronic devices in the same way ***as a function of parameter variation in one or more fabrication or operational parameters*** associated with said integrated circuit substrate" (claims 6, 13)
"said processing frequency and ***said clock rate varying*** in the same way ***relative to said variation in said one or more fabrication or operational parameters*** associated with said integrated circuit substrate" (claims 10, 16)

As shown in the chart above, the requirement may be stated in slightly different language in the independent claims, but the underlying requirement is the same—the speed or clock rate of the claimed variable speed clock or oscillator must be "varying" with the PVT parameters.

Summary judgment is appropriate because TPL has offered no evidence whatsoever to show that the claimed "clock" or "oscillator" is "varying" with the PVT parameters as recited in

the claims. The sum total of TPL's analysis in its expert report for these "varying" limitations, aside from parroting the claim language, is the assertion that one of ordinary skill in the art would understand the variation to exist for the accused products "based on generally accepted principles relating to semiconductor ICs." (*See, e.g.*, Chen Decl. Ex. 15 (Appendix K to Oklobdzija 06/04/2013 Infringement Rep.), Ex. HTC-A-1 at page 5 of 30.) TPL's expert did not perform further analysis or apply these "generally acceptable principles" to any accused product. Nor did TPL's expert perform any testing to determine whether this variation actually exists in the accused HTC products. (*See* Chen Decl. Ex. 12 (Oklobdzija 07/13/2013 Depo.) at 70:13-16.) And when asked at his deposition whether he had investigated whether it would be possible to do such a test, he responded: "**I haven't had time to do it**." (*Id.* at 71:10-14.) This was a remarkable statement coming from an expert witness who has been working on this case for more than six years. (Chen Decl. Ex. 13 (Oklobdzija 07/15/2013 Depo.) at 402:10-13.)

In any event, HTC's expert did perform a series of tests on accused HTC products to assess whether the variation required by the claim occurs. (Gafford Decl. Ex. 1 (Gafford 07/02/2013 Non-Infringement Rep.), ¶¶ 145-169.) For example, Mr. Gafford tested the frequency of the PLL that clocks the CPU of a Qualcomm MSM7x30 chip through temperature variations from -5ºC to 55ºC (23ºF to 131ºF). (*Id.* ¶ 153.) His testing found that the frequency variance was only +/- 0.00043%, the kind of tightly-controlled frequency that is, for intents and purposes, a fixed speed clock signal like a crystal. (*Id.*) Mr. Gafford also tested and showed similar stability of +/- 0.0003% and +/- 0.00033% in the frequencies of the two PLLs that clock the CPUs in two separate Qualcomm MSM8655 chips (*id.*, ¶ 158), presumably having process variations between them. In fact, TPL's expert, when asked what kind of variance he would expect to see from crystals chosen by phone manufacturers today, he estimated that the variation would be between 4 and 12 parts per million over a similar temperature range (0.0004% to 0.0012%). (*See* Chen Decl. Ex. 12 (Oklobdzija 07/13/2013 Depo.) at 89:21-90:1; 92:20-93:10.) The PLLs' frequency variations in Mr. Gafford's test results certainly fall within this range. These results should hardly be surprising given that the accused HTC products, as noted above, have PLLs specifically designed to operate within tight tolerances and produce fixed, stable frequencies.

The frequency variation of the claimed "variable speed" clock or oscillator envisioned in the '336 specification, in sharp contrast, can be "a factor of two" or "a factor of four" (200% to 400%). (*See* '336, 16:43-46 ("The result are [sic] designs that must be clocked a factor of two slower than their maximum theoretical performance . . . ."), 16:60-63 ("At room temperature, the frequency will be in the neighborhood of 100 MHZ. At 70 degrees Centigrade, the speed will be 50 MHZ."), 17:21-22 ("Speed may vary by a factor of four depending upon temperature, voltage, and process.").) The variation observed by Mr. Gafford (+/-0.0003% to +/-0.00043%) falls well within what the specification and prosecution history expressly consider to be the kind of "minimal" variances in a reference crystal. The file history confirms that the type of miniscule variations exhibited by the accused HTC products do not meet the "varying" claim limitations. As the applicants explained in distinguishing the Magar reference: "Crystals are by design fixed frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature**.** The Magar microprocessor in no way contemplates a variable speed clock as claimed." (Chen Decl. Ex. 6 ('336 prosecution history, July 7, 2997 Amendment) at 3-4 (TPL85300002427-28).) TPL has offered no proof whatsoever that the accused PLL and its VCO or ICO varies beyond the "minimally" expected variance of a crystal clock.

V. TPL CANNOT SHOW WILLFUL INFRINGEMENT OF THE '336 PATENT

Because TPL cannot establish infringement of the '336 patent, its claim for willful infringement necessarily fails. But even if a genuine issue of material fact existed on the issue of infringement of the '336 patent (which it does not), the Court should dispose of TPL's baseless willful infringement claim on summary judgment because, at every relevant time period, HTC had clear, legitimate, and objectively reasonable defenses to TPL's claims.

The Federal Circuit has held that a showing of willful infringement requires that the plaintiff establish by clear and convincing evidence (1) that the accused infringer "acted despite an objectively high likelihood that its actions constituted infringement of a valid patent," and (2) that this objectively defined risk "was either known or so obvious that it should have been known to the accused infringer." *In re Seagate Tech., LLC*, 497 F.3d 1360, 1371 (Fed. Cir. 2007) (*en banc*).

TPL cannot establish either prong because it has proffered no evidence whatsoever of willful infringement. HTC propounded an interrogatory specifically asking TPL to identify its evidence and the complete factual basis for its allegation of willful infringement against HTC. (*See* Chen Decl. Ex. 17 (TPL's Response to HTC Interrogatory No. 9) at 22.) TPL's response included a parade of groundless objections but provided no substantive response. (*Id.*) TPL never supplemented its response to this interrogatory, and fact discovery closed long ago.

Moreover, the evidence affirmatively establishes that TPL could not establish willful infringement even if it had responded to HTC's interrogatory. Under the objective prong of the willful infringement analysis, "a patentee must show by clear and convincing evidence that the infringer acted despite an objectively high likelihood that its actions constituted infringement of a valid patent." *In re Seagate Tech., LLC*, 497 F.3d at 1371. "The state of mind of the accused infringer is not relevant to this objective inquiry." *Id.* This objective determination entails an assessment of the reasonableness of the accused infringer's defenses, such as its arguments about non-infringement. *See Bard Peripheral Vascular, Inc. v. W.L. Gore & Assocs., Inc*., 682 F.3d 1003, 1006 (Fed. Cir. 2012).

The Federal Circuit recently made clear that this objective prong presents a legal question suitable for summary judgment. "When a defense or noninfringement theory asserted by an infringer is purely legal (*e.g.*, claim construction), the objective recklessness of such a theory is a purely legal question to be determined by the judge." *Id*. at 1007. Even in those instances when the objective prong turns on factual issues, "the judge remains the final arbiter of whether the defense was reasonable, even when the underlying fact question is sent to a jury." *Id*.

TPL's willful infringement claim fails as a matter of law under the objective prong because HTC had reasonable non-infringement and invalidity defenses. As explained above, HTC had clear non-infringement arguments based on a claim construction that has been adopted by two different judges. Both Judge Gildea's and Judge Ward's constructions require that the "entire" clock not rely upon an external crystal or clock generator. *See* Part IV.A above. HTC's view of the file history, coupled with the undisputed operation of its products, provided a more than reasonable basis for its defense of non-infringement.

Although the ITC Investigation is still ongoing, the assigned ITC Staff Attorney Whitney Winston, a graduate from the Massachusetts Institute of Technology, has concluded that that HTC does not infringe the '336 patent. (*See* Chen Decl. Ex. 16 (OUII Post Hearing Brief) at 1.) HTC's non-infringement position was clearly sufficiently compelling and reasonable that a neutral ITC Staff attorney, who represents neither side, agreed with that position. (*Id.*) Despite differences in the accused products, TPL and HTC are advancing substantially the same theories of infringement and non-infringement in both the ITC and the district court cases. The Staff's opinion validates the objective reasonableness of HTC's position on non-infringement of the '336 and negates Defendants' ability to establish by clear and convincing evidence that HTC's actions were "objectively reckless."

Because HTC'S non-infringement defenses were objectively reasonable—in fact, more than sufficient to warrant summary judgment—TPL's entire willful infringement claim fails. *See Bard Peripheral Vascular, Inc*., 682 F.3d at 1006 (satisfying objective prong is a "threshold determination" for a finding of willfulness).

VI. CONCLUSION

For the foregoing reasons, HTC respectfully requests that the Court grant summary judgment of non-infringement and no willful infringement with respect to the '336 patent.

Dated: July 16, 2013

Respectfully submitted,

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, et al., Defendants.	Case No.: 5:08-cv-00882-PSG **ORDER RE: HTC'S MOTIONS FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT AND NO WILLFULNESS** **(Re: Docket Nos. 457, 458)**

Before the court in this patent case are two motions for summary judgment brought by Plaintiffs HTC Corporation and HTC America, (collectively "HTC"). HTC first moves for "full" summary judgment of non-infringement and no willful infringement of U.S. Patent No. 5,809,336 ("the '336 patent"). HTC separately moves for partial summary judgment of non-infringement of the '336 patent and U.S. Patent No. 5,530,890 ("the '890 patent") and no willful infringement of the '890 patent. On August 13, 2013, the parties appeared for a hearing. Having considered the papers and arguments of counsel:

The court DENIES HTC's motion for summary judgment of "full" non-infringement of the '336 patent.

The court DENIES HTC's motion for partial summary judgment of non-infringement of the '336 patent.

The court DENIES HTC's motion for summary judgment of no willful infringement of the '336 patent.

The court GRANTS HTC's motion for partial summary judgment of non-infringement of the '890 patent.

The court GRANTS-IN-PART HTC's motion for partial summary judgment of no willful infringement of the '890 patent.

The court sets forth its reasoning below.

I. BACKGROUND

HTC Corporation is a Taiwan corporation with its principal place of business in Taoyuan, Taiwan, R.O.C. HTC's subsidiary, HTC America, is a Texas corporation with its principal place of business in Bellevue, Washington. Defendants Technology Properties Limited and Alliacense, Limited ("Alliacense") are California corporations with their principal place of business in Cupertino, California; Patriot Scientific Corporation ("Patriot") is a Delaware corporation with its principal place of business in Carlsbad, California. These defendants – Technology Properties Limited, Alliacense, and Patriot (collectively "TPL") – claim ownership of a family of related microprocessor patents. TPL refers to those patents as the Moore Microprocessor Portfolio patents ("MMP patents"), in recognition of co-inventor Charles Moore's contributions. HTC filed this suit on February 8, 2008, seeking a judicial declaration that four of the MMP patents – U.S. Patent Nos. 5,809,336 ("the '336 patent"), 5,784,584 ("the '584 patent"), 5,440,749 ("the '749 patent"), and 6,598,148 ("the '148 patent") – are invalid and/or not infringed.[1] TPL counterclaimed for

[1] *See* Docket No. 1.

infringement of the '336, '749, '148, and '890 patents on November 21, 2008.[2] On April 25, 2008, TPL filed two complaints in the Eastern District of Texas against HTC alleging infringement of the four patents at issue in the pending declaratory judgment action.[3] On June 4, 2008, TPL filed additional patent infringement actions against HTC in the Eastern District of Texas asserting U.S. Patent No. 5,530,890 ("the '890 patent").[4] On July 10, 2008, HTC amended its complaint before this court, adding claims for declaratory relief with respect to the '890 patent.[5] On February 23, 2009 the parallel Texas litigation was dismissed without prejudice following Judge Fogel's decision to deny TPL's Motion to Dismiss, or in the Alternative, to Transfer Venue in the California action.[6] On March 25, 2010, the court accepted the parties' stipulation to dismiss the '584 patent from this litigation.[7] On August 24, 2012, Technology Properties Limited, Patriot, and Phoenix Digital Solutions initiated an International Trade Commission ("ITC") investigation regarding HTC's alleged infringement of the '336 patent.[8] On July 17, 2013, the court accepted the parties' stipulation to dismiss the '148 and '749 patents from this litigation.[9]

The bottom line is that only the '336 and '890 patents remain at issue for the purposes of this litigation.

A. The '336 Patent

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[2] *See* Docket No. 60 at 6-8.

[3] *See* Docket No. 16 at 3.

[4] *See* Docket No. 35 at 5.

[5] *See* Docket No. 34.

[6] See Docket Nos. 49 (denying motion to dismiss, to transfer venue, and to stay) and 88 (granting motion for leave to file motion for reconsideration and denying motion for reconsideration).

[7] *See* Docket No. 152.

[8] *See* Docket No. 561-1. Claims 1, 6, 7, 9-11, and 13-16 were asserted in the investigation. On September 6, 2013, Administrative Law Judge James Gildea issued an Initial Determination from in the ITC proceeding holding that HTC did not violate Section 337 of the Tariff Act of 1930. *See id.*

[9] *See* Docket No. 462.

The '336 patent issued on September 15, 1998 and describes a microprocessor with an internal variable speed clock, or oscillator, that drives the processor's central processing unit ("CPU"). Traditional microprocessors use external, fixed speed crystals to clock the CPU. A CPU's maximum possible processing capacity depends on process, voltage, and temperature ("PVT parameters"). An external clock must therefore set the timing of the CPU to suboptimal PVT conditions, resulting in waste of the CPU's processing speed under optimal conditions. The internal, variable clock described in the '336 patent claims real-time adjustment of the timing of the CPU by placing the clock on the chip itself. Thus, the CPU can perform optimally under any set of parameters. The microprocessor nevertheless requires a second external clock because devices other than the CPU do not operate at variable speed.

TPL claims that HTC's accused products infringe the '336 patent by their internal, variable speed oscillator on their microprocessors. At issue are claims 1, 6, 10, 11, 13, and 16.[10]

Claim 1 provides:

> A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.

Claim 6 provides:

> A microprocessor system comprising:

[10] Docket No. 494 at 7.

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices; an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.

Claim 10 provides:

In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of: providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency; providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors; clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate; connecting an [on chip] on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock and wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock.

Claim 11 provides:

A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator

variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperatureof said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein said central processing unit operates asynchronously to said input/output interface.

Claim 13 provides:

A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices; an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and further wherein said central processing unit operates asynchronously to said input/output interface.

Claim 16 provides:

In a microprocessor system including a central processing unit, a method for locking said central processing unit comprising the steps of providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency; providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors; clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate; connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus,

and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock, wherein said central processing unit operates asynchronously to said input/output interface.

B. The '890 Patent

The '890 patent first issued on June 25, 1996 and originally included ten claims, nine of which depended from the sole independent claim, claim 1.[11] On January 19, 2009, the '890 patent was subjected to ex parte reexamination.[12] An amended version of the patent emerged on March 1, 2011.[13] The reexamination proceeding resulted in the cancellation of claims 1-4, confirmation of the patentability of claims 5-10, and addition of claims 11-20. At issue in this suit are claims 11, 12, 13, 17, and 19.[14]

Claim 11, the amended independent claim on which all of the other claims depend, describes:

> A microprocessor, which comprises a main central processing unit and a separate direct memory access central processing unit in a single integrated circuit comprising said microprocessor, said main central processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus, said internal data bus being bidirectionally connected to a loop counter, said loop counter being connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register, said stack pointer pointing into said first push down stack, said internal data bus being connected to a memory controller, to a Y register of a return push down stack, an X register and a program counter, said Y register, X register and program counter providing outputs to an internal address bus, said internal address bus providing inputs to said memory controller and to an incrementer, said incrementer being connected to said internal data bus, said direct memory access central processing

[11] *See* Docket No. 458 at 2.

[12] *See id.*

[13] *See id.*

[14] *See id.*

> unit providing inputs to said memory controller, said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory.

During reexamination, the patentee added the phrase "said stack pointer pointing into said first push down stack," which did not appear in claim 1.

II. SUMMARY JUDGMENT STANDARDS

Summary judgment is appropriate only if there is "no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law."[15] The moving party bears the initial burden of production by identifying those portions of the pleadings, discovery, and affidavits which demonstrate the absence of a triable issue of material fact.[16] The standard for summary judgment differs depending on whether the moving party bears the burden of persuasion at trial.[17] If the moving party bears the burden of persuasion at trial, that party must present "credible evidence" showing that he is entitled to a directed verdict.[18] The burden of production then shifts to the non-moving party to produce evidence raising a genuine issue of material fact.[19] On the other hand, if the moving party does not bear the burden of persuasion at trial, he can prevail on a motion for summary judgment in two ways: by proffering "affirmative evidence negating an element of the non-moving party's claim," or by showing the non-moving party has insufficient evidence to establish an "essential element of the non-moving party's claim."[20] If met by the moving party, the burden of production then shifts to the non-moving party, who must then provide

[15] Fed. R. Civ. P. 56(a).

[16] *See* Fed. R. Civ. P. 56(c)(1); *Celotex Corp. v. Catrett*, 477 U.S. 317, 323 (1986).

[17] *See Celotex Corp.*, 477 U.S. at 331.

[18] *Id.*

[19] *See id.*

[20] *Id.*

specific facts showing a genuine issue of material fact for trial.[21] In both instances, the ultimate burden of persuasion remains on the moving party.[22] In reviewing the record, the court must construe the evidence and the inferences to be drawn from the underlying evidence in the light most favorable to the non-moving party.[23]

III. DISCUSSION

A. HTC's Motion for Summary Judgment of Non-Infringement and No Willful Infringement of the '336 Patent

1. Non-Infringement of the '336 Patent

The court first considers HTC's motion for summary judgment of "full" non-infringement of the '336 patent. HTC argues that summary judgment is warranted because when the independent claims of the '336 patent are properly construed, HTC's products do not perform the claimed invention. HTC specifically points to three terms that each appear in two claims: (1) "entire ring oscillator variable speed system clock" (claims 1 and 11), (2) "entire oscillator" (claims 6 and 13), and (3) "an entire variable speed system clock" (claims 10 and 16).

HTC argues as follows. The prosecution history of the '336 patent demonstrates the applicants' repeated and express disclaimer that the claimed timing element – the oscillator or variable speed clock – had any connection to or dependence on a reference signal from an external crystal or other fixed timing piece. To further distinguish the '336 patent, the applicants added the "entire" term to explicitly claim only a timing element that wholly and exclusively appeared with the CPU on the chip. HTC's processors, in contrast, rely on an external crystal timing piece (called

[21] *See id.* at 330; *T.W. Elec. Service, Inc. v. Pac. Elec. Contractors Ass'n*, 809 F.2d 630, 630 (9th Cir. 1987).

[22] *See id.*

[23] *See Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 248 (1986); *Matsushita Elec. Indus. Co. v. Zenith Radio Corp.*, 475 U.S. 574, 587 (1986).

a phase-locked loop or "PLL"). Unlike the invention, therefore, the timing elements of HTC's processors do not sit entirely on the chip and do not vary with PVT parameters.

TPL responds that HTC improperly seeks reconsideration of this court's previous claim construction. The court properly construed the "entire variable speed system clock" term and this construction should extend to the other three "entire" terms. HTC's additional limitations are not supported by the specification, which does not speak to whether the oscillator or variable speed system clock also could work with an external crystal. As for any disclaimer, the applicants never disclaimed all reliance or reference to an off-chip crystal. Instead, the disclaimer to avoid the Magar reference was to an off-chip oscillator that generated the on-chip clock. As to the Sheets reference, the applicants distinguished their clock reference by pointing out that it was not an on-chip oscillator but rather an off-chip clock, and that off-chip clock required a command input to change its frequency. The oscillator taught by the '336 patent, in contrast, is self-generating on the chip itself and does not require an outside command to change frequency. As to the variation argument, even by HTC's own admission, the on-chip HTC oscillators vary and the PLLs in fact serve to limit that variation. That the net result may be a minimal change in the frequency of the clock is not enough to take HTC's accused products beyond the claim language.

HTC replies that the on-chip oscillator does not "generate" the CPU clock unless it communicates with the PLL, making the PLL necessary to "generate" the clock – and thereby outside of the claim language (as construed in light of the disclaimers). HTC further replies that frequency control in fact is generation of the clock because the oscillator does not begin to run independently. The PLL controls the oscillator and sets the frequency, which generates the clock. As to the variation issue, HTC argues that a person of ordinary skill in the art would understand the de minimis variation experienced by its products as rendering the timing element essentially fixed.

The court agrees with HTC that the disputed limitations are properly understood to exclude any external clock used to generate a signal.[24] Nevertheless, there remains a factual dispute whether HTC's products contain an on-chip ring oscillator that is self-generating and does not rely on an input control to determine its frequency. While HTC's expert says that the PLLs generate the clock, TPL's expert counters that the ring oscillators generate the clock and the PLLs merely buffer or fix the frequency.[25] This is a classic factual question that requires a trial to answer.

2. Willful Infringement of the '336 Patent

To "establish willful infringement, a patentee must show by clear and convincing evidence that the infringer acted despite an objectively high likelihood that its actions constituted infringement of a valid patent."[26] A patentee therefore must establish two elements. First, the patentee must show the accused infringer acted with "objective recklessness." Objective recklessness remains a question of law "predicated on underlying mixed questions of law and fact."[27] The objective recklessness prong "entails an objective assessment of potential defenses based on the risk presented" by the patent which "may include questions of infringement but also can be expected in almost every case to entail questions of validity that are not necessarily

[24] The patentee's arguments traversing the prior art narrowed the claims. *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722, 740 (2002) ("A patentee's decision to narrow his claims through amendment may be presumed to be a general disclaimer of the territory between the original claim and the amended claim."); *cf. Saeilo Inc. v. Colt's Mfg. Co.*, 26 F. App'x 966, 973 (Fed. Cir. 2002) ("Where an amendment narrows the scope of a claim for a reason related to the statutory requirements for patentability, prosecution history estoppel acts as a complete bar to the application of the doctrine of equivalents to the amended claim element.").

[25] *Compare* Docket No. 457 at 16 ("the oscillators in the accused products indisputably rely on an external crystal or clock generator to clock" the CPU), *with* Docket No. 470 at 14 ("Each HTC product includes a CPU/system clock – a ***ring oscillator*** within a PLL – that ***generates*** a clock signal ***on its own***, as long as it has a power supply.") (emphasis in original).

[26] *In re Seagate Tech., LLC*, 497 F.3d 1360, 1371 (Fed. Cir. 2007) (*en banc*).

[27] *See Bard Peripheral Vascular, Inc. v. W.L. Gore & Assocs., Inc.*, 682 F.3d 1003, 1006-07 (Fed. Cir. 2012) (holding that the objective determination of recklessness, even though predicated on underlying mixed questions of law and fact, is decided by the judge as a question of law subject to de novo review).

dependent on the factual circumstances of the particular party accused of infringement."[28] Second, if the requisite threshold objective recklessness is established, then the patentee must show that the "objectively-defined risk" of infringement determined by the record developed in the infringement proceeding "was either known or so obvious that it should have been known to the accused infringer."[29]

HTC argues that TPL has not presented sufficient evidence to make a prima facie case of willful infringement, in view of its "clear, legitimate, and objectively reasonable defenses" to HTC's claims of infringement.[30] In particular, its proposed constructions have been adopted by other tribunals and the ITC in particular. HTC's non-infringement position at the ITC was "sufficiently compelling and reasonable" that both the ITC staff attorney and Judge Gildea himself agreed with HTC's position.[31]

TPL takes issue with HTC's reference in this case to the ITC litigation. Different theories of infringement and different products are implicated by the two cases. Different claim constructions have issued in the cases. The staff attorney's position and Judge Gildea's conclusions are therefore irrelevant. Separately, TPL's successful licensing of the MMP patent portfolio suggests that HTC could not reasonably or realistically expect its invalidity or

[28] *Id.* at 1006.

[29] *Seagate*, 497 F.3d at 1371.

[30] Looking to Fed. R. Civ. P. 37(c)(1) HTC further points out that TPL failed to substantively respond to its interrogatory about willful infringement. *See* Fed. R. Civ. P. 37(c)(1) ("If a party fails to provide information or identify a witness as required by Rule 26(a) or (e), the party is not allowed to use that information or witness to supply evidence on a motion, at a hearing, or at a trial, unless the failure was substantially justified or is harmless."). But TPL's response raising a host of objections appears substantially justified, even if it is not ultimately persuasive, and in any event HTC does not appear to have taken any steps whatsoever in the intervening four years to compel a more complete response.

[31] Judge Gildea's Initial Determination ("ID") did not issue until September 6, 2013, after the papers for this motion were filed.

non-infringement defenses to succeed in this litigation. Finally, direct pre-suit communication between HTC and TPL establishes that HTC had notice of its allegedly infringing activities.

District courts appear split as to whether current evidence that a party's actions were objectively reasonable is relevant to a willfulness analysis under *Seagate*. In *i4i Ltd. P'ship v. Microsoft Corp.*, Judge Davis held that the correct willfulness analysis "focuses on whether, given the facts and circumstances prior to [the accused infringer's] infringing actions, a reasonable person would have appreciated a high likelihood that acting would infringe a valid patent."[32] The "number of creative defenses that Microsoft is able to muster in an infringement action after years of litigation and substantial discovery is irrelevant to the objective prong of the *Seagate* analysis."[33] Judge Davis then explained that the court should more properly focus on whether defenses would have been objectively reasonable and apparent before Microsoft infringed and was sued.[34] In *Uniloc USA, Inc. v. Microsoft Corp.*, Judge Smith was "not convinced that such a 'before and after' line is so easily drawn, or for that matter appropriate, to measure the objective likelihood (or lack thereof) that a party acted to infringe a valid patent."[35] Judge Smith emphasized that "the inquiry is case-specific" and should focus on an objective view of the record.[36]

The court agrees with HTC that favorable court rulings can support the objective reasonableness of its non-infringement positions. The court cannot help but take note of the analogous issue of the "book of wisdom" when addressing patent damages. The Supreme Court has affirmed that after-arising "[e]xperience . . . is a book of wisdom that courts may not

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[32] 670 F. Supp. 2d 568, 582 (E.D. Tex. 2009).

[33] *Id.*

[34] *See id.*

[35] 640 F. Supp. 2d 150, 177 n. 33 (D.R.I. 2009).

[36] *Id.*

neglect."[37] Nonetheless, "as the party moving for summary judgment" HTC "must do more than persuade [the court] that its defenses were reasonable."[38] Instead, HTC "must establish that 'there is no genuine dispute as to any material fact' and that [the accused infringer] 'is entitled to judgment as a matter of law'—in other words, that *no reasonable fact-finder* could find willful infringement."[39]

Viewing the evidence in the light most favorable to TPL, the court concludes that a reasonable fact finder could plausibly find facts sufficient to support a conclusion of willful infringement. TPL's burden to show willful infringement by clear and convincing evidence is a steep one. But where factfinding is necessary, trial courts generally reserve willfulness until after a full presentation of the evidence on the record to the jury.[40] The record supports a finding that HTC knew about the patents and TPL's claims of infringement before it began the activities that allegedly infringe and as explained above, here there remains an important issue regarding the role of the external crystal in HTC's products in generating a signal.[41] Under these circumstances summary judgment on the issue of willfulness is not warranted.

B. Partial Summary Judgment of Non-Infringement of the '336 Patent and the '890 Patent and No Willful Infringement of the '890 Patent

HTC next moves for partial summary judgment of non-infringement of the '336 patent and the '890 patent based on the doctrine of absolute intervening rights. By this same motion, HTC also seeks summary judgment of no willful infringement under the '890 patent.

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[37] *Sinclair Ref. Co. v. Jenkins Petroleum Process Co.*, 289 U.S. 689, 690 (1933).

[38] *Kimberly-Clark Worldwide, Inc. v. First Quality Baby Products, LLC*, Case No. 1:09-cv-1685, 2013 WL 1465403, at *2 (M.D. Pa. Apr. 11, 2013)

[39] *Id.* (citing Fed. R. Civ. P. 56(a)).

[40] *See, e.g. Bard*, 682 F.3d at 1008; *Fujitsu Ltd. v. Belkin Int'l, Inc.*, Case No. 10-cv-03972-LHK, 2012 WL 4497966, at *39 (N.D. Cal. Sept. 28, 2012).

[41] *See* Docket No. 470-1, Ex. A (Nov. 7, 2006 correspondence from Alliacense to HTC); Docket No. 470-1, Ex. B (Nov. 20, 2006 correspondence from Alliacense to HTC).

Under 35 U.S.C § 307(b), a patent owner may not recover for infringement of claims that are invalidated or amended through the reexamination process.[42] The "reexamination statute restricts a patentee's ability to enforce the patent's original claims to those claims that survive reexamination in 'identical' form."[43] "'Identical' does not mean verbatim, but means at most without substantive change."[44] The court must therefore determine whether the scope of the claims are the same, not just whether the same words are used.[45] Section 307 shields "those who deem an adversely held patent to be invalid; if the patentee later cures the infirmity by reissue or reexamination, the making of substantive changes in the claims is treated as an irrebuttable presumption that the original claims were materially flawed."[46] The "statute relieves those who may have infringed the original claims from liability during the period before the claims are validated."[47]

Whether "amendments made to overcome rejections based on prior art are substantive depends on the nature and scope of the amendments, with due consideration to the facts in any given case that justice will be done."[48] "An amendment that clarifies the text of the claim or makes it more definite without affecting its scope is generally viewed as identical."[49] To make its determination under the so-called doctrine of intervening rights, the court must consider "the scope of the original and reexamined claims in light of the specification, with attention to the references

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[42] *See Fresenius USA, Inc. v. Baxter Intern., Inc.*, 721 F.3d 1330, 1339 (Fed. Cir. 2013).

[43] *Id.* (listing cases).

[44] *Id.*

[45] *See id.*

[46] *Bloom Eng'g Co. v. N. Am. Mfg. Co.*, 129 F.3d 1247, 1249 (Fed. Cir. 1997).

[47] *Id.*

[48] *Id.*

[49] *Id.*

that occasioned the reexamination, as well as the prosecution history and any other relevant information."[50]

1. Non-Infringement of the '336 Patent

As noted earlier the '336 patent issued September 15, 1998, and included ten originally-issued claims.[51] A series of ex parte reexamination requests were filed against the '336 patent between October 2006 and January 2007.[52] When the reexamination proceedings completed, claims 1, 6, and 10 emerged with modified language, and new independent claims 11, 13, and 16 were added. TPL amended claim 1 to further describe the "second clock independent of said ring oscillator" to say that "wherein a clock signal of said clock originates from a source other than said ring oscillator variable speed system clock." Claim 6 was amended to describe the "off-chip external clock" to likewise derive its "clock signal" "from a source other than said oscillator." Claim 10 includes a similar amendment that adds that the "off-chip external clock" has a "clock signal" that "originates form a source other than said variable speed clock." Claims 6 and 10 also added "off-chip" references to the descriptions of the second clocks. Claims 11, 13, and 16 were based on independent claims 1, 6, and 10, but during reexamination TPL added an additional clause to the end of each claim: "wherein said central processing unit operates asynchronously to said input/output interface."

In HTC's view, it should not be held liable for infringement of the '336 patent claims 1, 6, 10, 11, 13, and 16 because those claims were either substantially narrowed or newly-added through reexamination. Any recovery for the '336 patent should be limited to the date of the issuance of the reexamination certificate on December 15, 2009, because the amendments were sufficiently substantive to preclude recovery from before the amendments.

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[50] *Id.*

[51] *See* Docket No. 458 at 5.

[52] *Id.*

TPL responds that these amendments serve as nothing more than clarification of the claim language and that the scope of the claims have not changed. Several excerpts from the prosecution history of the reexamination demonstrate that the patentee believed the amended claim language only clarified how the second clock was "independent"[53] and that the "external" components were in fact "off-chip"[54].

HTC replies that the original claims differ from the amended claims in scope because the original claims spoke only to the difference in frequency control – and that is what "independence" really references in these claim terms. Because a clock with signal origins from the ring oscillator but with an independent frequency could exist under the original claims but not under the amended claims, the claim is narrower and therefore substantively different. For claims 11, 13, and 16, the "independent" clock signals could have a "readily predictable phase relationship." Because of that possibility, the claims are narrower and thereby substantively different. Further, the court should not credit self-serving testimony from the prosecution history.[55]

On balance, the court finds that the amended claim language added during reexamination did not substantively amend the asserted '336 claims' scope. "Independent" in the disputed claims must be understood to be just that: without dependence of any kind. While HTC offers a more nuanced interpretation that focuses exclusively on frequency control, it cites no intrinsic – or for that matter extrinsic evidence – to support its position. Coupled with the references in the prosecution history indicating that the amendments really were for clarification purposes only, TPL's argument is more persuasive.

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[53] *See* Docket No. 471-5, Ex. E at 2; Docket No. 471-6, Ex. F at 11, 27; Docket No. 471-7, Ex. G at 8-12, 14.

[54] *See* Docket No. 471-7, Ex. G at 12, 16.

[55] *See Moleculon Research Crop. v. CBS, Inc.*, 793 F.2d 1261, 1270 (Fed. Cir. 1986) (holding that documents submitted by the patentee during prosecution may be considered for claim interpretation purposes, but "might very well contain merely self-serving statements which likely would be accorded no more weight than testimony of an interested witness or argument of counsel. Issues of evidentiary weight are resolved on the circumstances of each case.").

2. Motion for Partial Summary Judgment of Non-Infringement and No Willful Infringement of the '890 Patent

a. Non-Infringement of the '890 Patent

The court next considers HTC's motion for summary judgment of non-infringement of the '890 patent claims 11, 12, 13, 17, and 19. As noted above, claims 12, 13, 17, and 19 all depend on independent claim 11.

HTC again argues the doctrine of absolute intervening rights entitles it to summary judgment of non-infringement. During reexamination, TPL added claim language further defining a stack pointer as "pointing into said first push down stack," after the examiner identified no function for the stack pointer in the original claim language. The examiner noted that the amendment to claim 1 prevented the claim from being anticipated by the prior art under 35 U.S.C. § 102. This change to the '890 patent during reexamination was substantive and that the absolute intervening rights doctrine bars liability arising before the reexamination terminated.

TPL initially responds that HTC's assertion of the absolute intervening rights doctrine is untimely because it did not include the affirmative defense in its answer to TPL's complaint.[56] As to the merits, TPL says that the amendment only clarified the claim scope but did not substantively amend the claim, precluding the absolute intervening rights doctrine. Further, in *Norwood v. Vance* the Ninth Circuit noted that parties may raise affirmative defenses for the first time at summary judgment only if the opposing party is not prejudiced.[57] Allowing HTC to assert the defense – four years into this litigation – would subject it to unfair prejudice.

The court is not persuaded that TPL has established the prejudice necessary to bar HTC's assertion of the absolute intervening rights doctrine at this stage in the litigation. TPL does not, for

[56] The initial declaratory judgment complaint in this case was filed February 8, 2008. *See supra* note 1. The '890 patent did not reissue following reexamination until March 1, 2011. *See supra* note 13.

[57] 591 F.3d 1062, 1075 (9th Cir. 2010).

example, articulate the discovery it might have otherwise taken had HTC promptly moved to amend its answer in 2011.

Turning to the merits, HTC asserts estoppel and argues claim 11 emerged from reexamination substantively different from former claim 1. During reexamination, the examiner found claim 1 invalid. In an August 12, 2010, advisory action the examiner noted that claim 1 failed to provide a function for the "stack pointer" and the claim language only identified the stack pointer as "bidirectionally connected to an internal bus," – an error claim 11 corrected. The examiner also observed that the additional language in claim 11 avoided the May reference, U.S. Patent No. 4,758,948 ("the '948 patent"), that teaches using a push down stack but not expressly a stack pointer performing the function that the amended language defines. Therefore, that the absolute intervening rights doctrine bars infringement liability prior to the issuance of the reexamination certificate.

TPL sees it differently. The change to claim 11 only makes the claim more definite. The examiner's primary concern with claim 1 centered on the discussion in the May patent of an instruction pointer. The instruction pointer identifies the instructions of a process and under the broadest interpretation the stack pointer likewise could be construed to read onto the prior art. No person of ordinary skill in the art would understand a stack pointer could not perform equivalently to an instruction pointer. As described in claim 1, the stack pointer would be understood by a person of ordinary skill in the art to point to only to the first push down stack referenced in claim 1 – and so the additional language only explicitly states what a person of ordinary skill in the art already would understand claim 1 to teach.

HTC replies that TPL's arguments rely on extrinsic evidence and that the intrinsic evidence reveals that absent the added limitation, the stack pointer was impermissibly vague and the amendment substantively narrowed the claim.

The court agrees with HTC. As the examiner's office actions indicated, in the original claim language the stack pointer did nothing except connect to the internal data bus, but TPL's argument that a person of ordinary skill in the art necessarily would color in the ambiguity with an understanding that the stack pointer points only to the first push down stack is not persuasive. As HTC points out, claim 1 (and claim 11) employs the term "comprising," which reveals that the claim is "inclusive or open-ended and does not exclude additional, unrecited elements or method steps."[58] Given that the specification in fact references a second push down stack, the second stack must be presumed to be distinct from the return stack identified in the claim language, other push down stacks potentially could be used and still fall within claim 1. Thus, where the stack pointer points matters. If multiple push down stacks were included in a processor, it is unclear under the language of claim 1 whether the stack pointer points to one of the stacks, all of the stacks, or some multiple in between.

At bottom, the court finds the added language limits the stack pointer to the first push down stack and substantively changes the scope of the claim. Because the added claim language narrows the scope of the claims, any claims of infringement before the date of the issuance of the reexamination certificate must be precluded.

b. Willful Infringement of the '890 Patent

The court finally addresses the issue of willful infringement related to the '890 patent.

HTC asserts that under the objective recklessness prong, the reexamination and amendment of the '890 patent supports HTC's position that it was not objectively reckless. HTC points out that TPL has offered no evidence that it even knew of the '890 patent before the suit. HTC also argues that the failure by TPL to pursue a preliminary injunction suggests that willful infringement is not at issue.

[58] *CollegeNet, Inc. v. ApplyYourself, Inc.*, 418 F.3d 1225, 1235 (Fed. Cir. 2005).

TPL responds that it provided notice to HTC of the patents and of its infringing behavior in 2006. The reexamination process actually cuts against HTC because most of the substance of the patents in fact survived intact with a "second stamp of validity from the PTO."[59] The PTO accepts 92% of reexamination applications, so the PTO's grant of patent reexamination is not enough to undercut willful infringement.[60] A "substantial question of patentability raised by a reexamination request is not dispositive" in a willfulness inquiry.[61]

Although the record at least suggests that HTC was made aware of the patents-in-suit as early as November 2006,[62] as discussed above the reexamined '890 patent bars claims of infringement before the date of the issuance of the certificate because the additional language added to independent claim 11 narrowed the scope of the claim.[63] It follows that because HTC cannot be held liable for infringement before March 1, 2011, willful infringement for this period is precluded.

The court next turns to whether HTC can be found to have willfully infringed the '890 patent following reexamination. Generally, a "patentee who does not attempt to stop an accused infringer's activities [by moving for a preliminary injunction] should not be allowed to accrue

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[59] Docket No. 469 at 17.

[60] *See id.* n.11.

[61] *Plumley v. Mockett*, 836 F. Supp. 2d 1053, 1075 (C.D. Cal. 2010); *see also See Lucent Techs., Inc. v. Gateway, Inc.*, Case No. 07–cv–2000–H, 2007 WL 6955272, at *7 (S.D. Cal. Oct. 30, 2007) ("The Court does not assume that a reexamination order will always prevent a plaintiff from meeting their burden on summary judgment regarding willful infringement, but it does consider this as one factor among the totality of the circumstances.").

[62] *See* Docket No. 469-12, Ex. C (correspondence from Alliacense notifying HTC that HTC was infringing the patents contained in the MMP Portfolio, including the '890 patent).

[63] Moreover, at least one district court has noted, albeit in dicta, that "a patentee's willful infringement claim fails as a matter of law where the PTO requires amendments to the patent before issuing a reexamination certificate." *Plumley*, 836 F. Supp. 2d at 1075 (explaining court's opinion in *TGIP, Inc. v. AT & T Corp.*, 527 F. Supp. 2d 561 (E.D. Tex. 2007)).

enhanced damages based solely on the infringer's post-filing conduct."[64] But as TPL happily highlights, HTC conceded in prior litigation "that *Seagate* did not create a *per se* bar to claims for post-filing willful infringement where an injunction was not sought."[65] "Because *Seagate* did not create a *per se* bar, the determination of whether a patentee may pursue a claim for willful infringement based on post-filing conduct without seeking a preliminary injunction 'will depend on the facts of each case.'"[66] Patentees who neither practice the invention nor directly compete with the accused infringer are "excused from *Seagate's* rule that a patentee must seek an injunction to sustain a claim for post-filing willful infringement."[67] There may be circumstances "where an infringer's post-filing conduct was found to be willful" where "some material change that could create an objectively high likelihood of infringing a valid patent, such as a patent surviving a reexamination proceeding without narrowed claims."[68]

Viewing the evidence in the light most favorable to TPL and drawing all reasonable inferences in its favor, especially TPL's successful licensing program related to the patents-in-suit, the court concludes that a reasonable fact finder could plausibly find facts supporting a conclusion of willful infringement following the reexamination of the '890 patent.

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[64] *Seagate*, 497 F.3d at 1372; *see also Anascape, Ltd. v. Microsoft Corp.*, Case No. 9:06-cv-158, 2008 WL 7182476 (E.D. Tex. Apr. 25, 2008) (patentee who did not move for preliminary injunction was not entitled to benefit from its lack of diligence by obtaining enhanced damages for willfulness during the post-filing period).

[65] *DataQuill Ltd. v. High Tech Computer Corp.*, 887 F. Supp. 2d 999, 1015 (S.D. Cal. 2011).

[66] *Id.* (citing *Seagate* 497 F.3d at 1374).

[67] *Id.*

[68] *LML Holdings, Inc. v. Pac. Coast Distrib. Inc.*, Case No. 11-cv-06173-YGR, 2012 WL 1965878 (N.D. Cal. May 30, 2012) (citing *St. Clair Intellectual Prop. Consultants, Inc. v. Palm, Inc.*, Case No. 04–1436–JJF–LPS, 2009 WL 1649751, at *1 (D. Del. Jun.10, 2009)); *see also Webmap Technologies, LLC v. Google, Inc.*, Case No. 2:09–cv–343–DF–CE, 2010 WL 3768097, at *2-3 (E.D. Tex. Sep. 10, 2010).

IT IS SO ORDERED.

Dated: September 17, 2013

PAUL S. GREWAL
United States Magistrate Judge

United States District Court
For the Northern District of California

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION and HTC AMERICA, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED,

Defendants.

Case No. 5:08-cv-00882 PSG

[Related to Case No. 5:08-CV-00877 PSG]

EMERGENCY MOTION FOR ADDENDUM TO JURY INSTRUCTIONS

Complaint Filed: February 8, 2008
Trial Date: September 23, 2013

Date: September 20, 2013
Time: 9:30 a.m.
Place: Courtroom 5, 4th Floor
Judge: Hon. Paul S. Grewal

NOTICE OF MOTION AND MOTION

PLEASE TAKE NOTICE that Plaintiffs HTC Corporation and HTC America, Inc. (collectively "Plaintiffs") move, on an emergency basis, pursuant to Civil Local Rules 6-3 and 7-11, this Court to add an addendum to the Joint Proposed Jury Instructions to reflect the Court's recent findings in its Order on Summary Judgment of Non-Infringement of the '336 Patent.

This Motion is based on the Memorandum of Points and Authorities set forth below, the accompanying Declaration of Kyle Chen, and such other matters as may be presented at the hearing on Plaintiffs' motion and allowed by the Court.

Plaintiffs notified Defendants' counsel on September 18, 2013, that Plaintiffs intended to file this motion and asked for a prompt response on whether Defendants opposed. Defendants and Plaintiffs were not able to reach a resolution.

MEMORANDUM OF POINTS AND AUTHORITIES

In light of the Court's Order (Dkt. No. 585) granting-in-part HTC's Motion for Summary Judgment of Non-Infringement of the '336 Patent and finding that the patentee disclaimed certain claim scope (*id*. at 11), Plaintiffs HTC Corporation and HTC America, Inc. ask the Court to add the following addendum to the Joint Proposed Jury Instructions (Dkt. No. 513). This addendum would add the following paragraph immediately before current paragraph no. 1 at line 15 of page 44 of those instructions:

> The terms "entire ring oscillator variable speed system clock" (in claims 1 and 11), "entire oscillator" (in claims 6 and 13), and "entire variable speed clock" (in claims 10 and 16) are not satisfied by an accused system that uses any external clock to generate a signal.
>
> An accused product can only infringe the '336 patent if that product contains an on-chip oscillator or clock that is (a) self-generating and (b) does not rely on an input control to determine its frequency.

///

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///

///

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Dated: September 18, 2013

Respectfully submitted,

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UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN JOSE DIVISION

HTC CORPORATION and HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00882 PSG **DEFENDANTS' OPPOSITION TO EMERGENCY MOTION FOR ADDENDUM TO JURY INSTRUCTIONS** Judge: Hon. Paul S. Grewal Date: September 20, 2013 Time: 9:30 a.m. Place: Courtroom 5, 4th Floor

Introduction

Although HTC titles its motion as a request for an addendum to the jury instructions, it is actually a motion for reconsideration of both the Court's summary judgment and claim construction orders. The motion seeks entry of yet ***another*** claim construction for "entire" that substantively differs from any construction HTC has previously requested in this case or the co-pending ITC action. Although this Court denied HTC's Motion for Summary Judgment of Non-Infringement of the '336 Patent in its entirety, HTC now re-writes the order as "granting-in-part" HTC's motion, and relies on it as the sole basis for the present request.

HTC's new "addendum" should be rejected because it imposes two new negative limitations on the "entire" elements that are not supported by the intrinsic evidence. Moreover, HTC's proposed addendum is hopelessly ambiguous and improperly conflates the two distinct concepts of: (1) generating a clock signal; and (2) regulating or adjusting the frequency of an already generated clock signal. While Defendants believe the Court has retained its original construction of "entire," the parties and the jury may also benefit from a clarification of the effect of the Court's September 17, 2013 Order – just not in the confusing manner proposed by HTC.

I. HTC'S MOTION FOR ADDENDUM TO JURY INSTRUCTIONS SHOULD BE DENIED BECAUSE IT SEEKS TO IMPOSE AMBIGUOUS AND UNSUPPORTED LIMITATIONS ON THE "ENTIRE" ELEMENTS.

In its September 17, 2013 Order (Dkt. No. 585), the Court denied HTC's Motion for Summary Judgment of Non-Infringement of the '336 Patent – the Court did ***not*** "grant-in-part" HTC's motion. In addition, the Court did not modify its claim construction for the "entire" elements.[1] Thus, for example, the construction of "entire oscillator" (claims 6 and 13) appears to remain as follows: "an oscillator that is entirely on the same semiconductor substrate as the central processing unit." If this remains the Court's construction, the parties should simply proceed to trial with that definition of "entire" – without HTC's confusing modifications.

[1] Although the Court noted in footnote 24 that "[t]he patentee's arguments traversing the prior art narrowed the claims," the Court did not provide specific guidance on the current scope and definition of the "entire" elements.

HTC now proposes to add two new negative limitations to the "entire" elements – one of which itself has two parts – as set forth below:

> **[1]** The terms "entire ring oscillator variable speed system clock" (in claims 1 and 11), "entire oscillator" (in claims 6 and 13), and "entire variable speed system clock" (in claims 10 and 16) are not satisfied by an accused system that uses any external clock to generate a signal.
>
> **[2]** An accused product can only infringe the '336 patent if that product contains an on-chip ring oscillator that is: **(a)** self-generating; and **(b)** does not rely on an input control to determine its frequency.

New limitation **[1]** is ambiguous. Presumably, HTC proposes this limitation in response to the Court's statement that it "agrees with HTC that the disputed limitations are properly understood to exclude any external clock used to generate a signal." Sept. 17, 2013 Order [Dkt. # 585] at 11. However, taken out of context, this statement is ambiguous because "uses any external clock to generate a signal" does not define what signal is being discussed and how the external clock may or may not be used to satisfy the claim. It also mischaracterizes the patent: Figure 17 shows the use of a conventional external crystal to clock the I/O interface. *See also* '336 17:12-34.

New limitation **[2]** is also ambiguous. The phrase "self-generating" is undefined. If "self-generating" means that the clock "does not rely on an input control to determine its frequency," then it is redundant. "Input control" are also undefined. It does not specify either the type of input or the type of control that is not permitted. Thus, HTC's proposed modifications to the Court's claim construction – whether by "addendum" to jury instructions or otherwise – should be rejected.

II. HTC'S NEW CLAIM LIMITATIONS SHOULD BE REJECTED BECAUSE THEY IMPROPERLY CONFLATE THE DISTINCT CONCEPTS OF "GENERATING A CLOCK SIGNAL" AND "REGULATING THE FREQUENCY OF A CLOCK SIGNAL," AND MISCONSTRUE THE MAGAR AND SHEETS REFERENCES.

New limitations **[1]** and **[2]** taken together are ambiguous and confusing. The source of the ambiguity is HTC's unjustified overextension of the arguments the patent applicants made during prosecution about the Sheets and Magar references. In addition, HTC repeatedly conflates the use of an external crystal oscillator and/or a control signal "to ***generate*** a clock signal" versus the use of an external crystal oscillator and/or a control signal "to determine or regulate the ***frequency*** of an already generated clock signal."

A. Contrary to HTC's Repeated and Unsupported Arguments, "Generating a Clock Signal" and "Regulating or Adjusting the Frequency of a Clock Signal" Are Not the Same; HTC's Effort to Conflate These Concepts is Designed to Confuse the Jury.

As an initial matter, "generating a clock signal" is ***not the same*** as "adjusting the frequency clock signal." Frequency is a ***characteristic*** of an already generated clock signal, as explained in Defendants' opposition to HTC's motion for summary judgment. In both its motion for summary judgment and its current emergency motion, HTC incorrectly argues that there should be no infringement if its products use a control signal or an external crystal/clock generator **to set or adjust the *frequency*** of the clock signal. This is quite different than arguing (as HTC did on summary judgment) that an external crystal and/or control signal may not be used to "***generate*** a clock signal." Equating "setting or adjusting the ***frequency*** of a clock signal" with "generating a clock signal" is fundamentally incorrect.

The difference between a **clock signal** and its **frequency** is apparent from the specification and claims of the '336 patent. For example:

> The ring oscillator 430 is useful as a **system clock** . . . because **its performance** tracks the parameters which similarly affect all other transistors on the same silicon die.

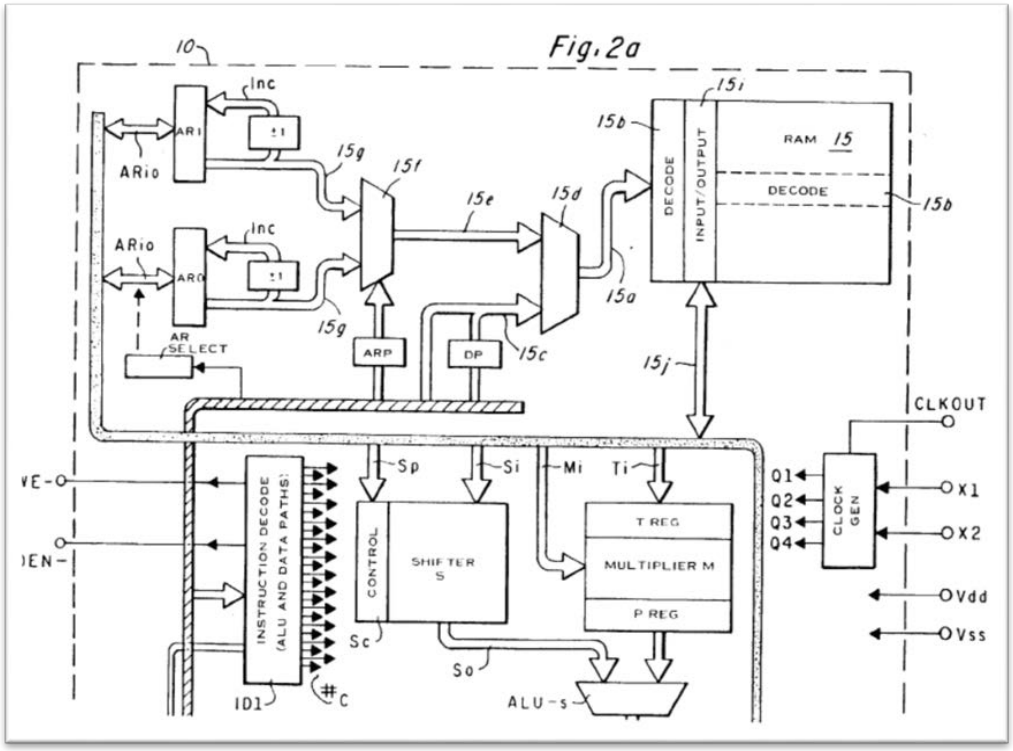
'336 at 16:63-67. In other words, the "performance" of the clock – *i.e.*, its speed or frequency – is ***not*** the same as the clock itself: its performance (frequency) changes, because it "tracks the parameters which similarly affect all other transistors on the same silicon die."

Similarly, claim 6 discusses "**an entire oscillator**" that "clock[s] said central processing unit ***at a clock rate.***" Plainly, the clock itself (the entire oscillator) is not the same as its "clock rate" (frequency), which is a ***characteristic*** of the already generated clock signal. Further, the "clock rate" in claim 6 has the ability to "vary" based on changes in "one or more fabrication or operational parameters." Obviously, the identity and source of the clock signal itself – the "entire oscillator" – does not change. By contrast, the "clock rate" (frequency) – which is a ***characteristic*** of the clock signal generated by the entire oscillator – can vary based on conditions.

Thus, equating "clock signal" and "frequency of the clock signal" is just plain wrong. And HTC improperly uses this flawed logic to argue for a confusing and ambiguous construction of "entire." The Court should reject HTC's invitation to adopt a legally incorrect construction.

B. The File History's Treatment of Magar and Sheets Do Not Support the Overreaching Limitations Sought by HTC.

HTC needs to stop misrepresenting to the Court about what Magar and Sheets disclosed, and how the patent applicants distinguished them. The applicants' never distinguished Magar by "unambiguously disclaim[ing] clocks and oscillators that ***rely on*** an external crystal for ***frequency control***," as HTC falsely argued in on summary judgment (HTC 457 Mot. at 12). First, the '336 patent ***shows the use of an external crystal*** (to clock the I/O interface). '336, Fig. 17; 17:12-34. HTC also blatantly mischaracterizes Magar, which included a CPU clock that was exactly like the prior art disclosed in the '336 patent (and the external crystal used to clock the I/O interface in Figure 17 of the '336 patent). The external crystal oscillator in Magar (connected at X1 and X2) generated the actual clock signal for the CPU; it was not a reference signal, and there was nothing in the "CLOCK GEN" circuitry box in Figure 2 of Magar to generate an oscillating clock signal:



Tyan Decl. [Dkt. # 471-1], Exh. A (Magar). Thus, distinguishing Magar had nothing to do with a disclaimer about the use of any external crystal for "frequency control." HTC should stop arguing, once and for all, that the Magar external crystal is the same thing as a reference crystal that is used

by a PLL. The two are completely different, and HTC's unsupportable mischaracterizations of Magar should be rejected. Neither Magar nor the applicants' statements in the file history had anything to do with the use of a crystal oscillator as a ***reference signal*** for a PLL. Rather, the off-chip crystal oscillator in Magar provided the actual clock signal for the CPU in the Magar microprocessor. **That is what applicants disclaimed:** ***the use of an external crystal to generate the actual clock signal for the CPU.***

HTC has also repeatedly misconstrued the file history's distinction of Sheets. As Defendants explained in their opposition to HTC's summary judgment motion, the applicants merely observed that ***Sheets lacked any on-chip oscillator***. Rather, Sheets provided "control information" – in the form of a "**digital word**" – to an **external clock**:

> The present invention does not similarly rely upon provision of frequency control information to an **external clock**, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. . . Sheets' system for providing clock control signals to an **external clock** is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.

Tyan Decl. [Doc. 471-1], Exh. F (4/1996 Amend.) at 8; Tyan Decl. [Doc. 471-1], Exh. B (Sheets) at 2:54-68 ("Microprocessor 101 . . . writes a **digital word** . . . via data bus 104 to VCO 102").

In a subsequent amendment, the applicants noted that the **external** Sheets clock "***required***" a "**digital word**" or "**command input**." By contrast, in the '336 invention, "both the variable speed clock and the microprocessor ***are fabricated together in the same integrated circuit***." Tyan Decl. [Dkt. # 471-1], Exh. G (1/1997 Amendment) at 4. Thus, the applicants distinguished Sheets on two bases: (1) unlike the '336 invention, Sheets lacked an on-chip clock/oscillator; and (2) the ***off-chip*** clock in Sheets ***required*** a "digital word"/"command input." These distinctions do not come close to constituting a disclaimer of any "control signal" for any purpose. Indeed, the analog voltage and/or current supplied to a ring oscillator are nothing like the "digital command word" in Sheets. For example, while any ring oscillator needs power to oscillate (*i.e.*, analog voltage/current), it does not have the ability to accept and process a "digital command word" – nor could it be "***required***" to do so.

Accordingly, Defendants respectfully ask the Court to deny HTC's Emergency Motion for Addendum to Jury Instructions. Rather, Defendants respectfully ask the Court to reaffirm its

original construction of "entire." If the Court deems it necessary, it might consider a clarification of the effect of its September 17, 2013 Order regarding the "entire" limitations.

Dated: September 18, 2013

Respectfully Submitted,
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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, et al., Defendants.	Case No.: 5:08-cv-00882-PSG **ORDER RE: EMERGENCY MOTION FOR ADDENDUM TO JURY INSTRUCTIONS** **(Re: Docket Nos. 513, 590)**

Before the court is Plaintiff HTC Corporation and HTC America, Inc.'s (collectively "HTC") Emergency Motion for Addendum to Jury Instructions. The parties appeared for a hearing earlier today. After considering the parties' arguments the court rules as follows:

The court's final jury instructions will instruct the jury that the terms "entire ring oscillator variable speed system clock" (in claims 1 and 11), "entire oscillator" (in claims 6 and 13), and "entire variable speed clock" (in claims 10 and 16) are properly understood to exclude any external clock used to generate a signal.[1]

[1] *See* Docket No. 513 at 11.

IT IS SO ORDERED.

Dated: September 20, 2013

PAUL S. GREWAL
United States Magistrate Judge

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, et al., Defendants.	Case No. 5:08-cv-00882-PSG **ORDER DENYING PLAINTIFFS' RENEWED MOTION FOR ENTRY OF JUDGMENT AS A MATTER OF LAW** **(Re: Docket No. 671)**

In this patent infringement suit, a jury found that the Plaintiffs in this action, HTC Corporation and HTC America, Inc. infringed a lone patent owned by Defendants Technology Properties Limited, Patriot Scientific Corporation, and Alliacense Limited (collectively, "TPL"). HTC now renews its motion for judgment as a matter of law pursuant to Fed. R. Civ. P. 50(b), arguing that no reasonable jury could have found that HTC infringes any asserted claim of U.S. Patent No. 5,809,336 ("the '336 patent). TPL opposes. The parties appeared for a hearing. After considering their oral arguments and those in the papers, the court DENIES HTC's motion.

I. BACKGROUND

Technology Properties Limited and Alliacense, Limited are California corporations with their principal place of business in Cupertino, California; Patriot Scientific Corporation is a Delaware corporation with its principal place of business in Carlsbad, California. These defendants – Technology Properties Limited, Alliacense, and Patriot (collectively "TPL") – claim ownership of a family of related microprocessor patents. TPL refers to those patents as the Moore Microprocessor Portfolio patents ("MMP patents"), in recognition of co-inventor Charles Moore's contributions.

A. The Long, Winding Road To Trial

HTC filed this suit on February 8, 2008, seeking a judicial declaration that four of the MMP patents – U.S. Patent Nos. 5,809,336 ("the '336 patent"), 5,784,584 ("the '584 patent"), 5,440,749 ("the '749 patent"), and 6,598,148 ("the '148 patent") – are invalid and/or not infringed.[1] TPL counterclaimed for infringement of the '336, '749, '148, and '890 patents on November 21, 2008.[2] On April 25, 2008, TPL filed two complaints in the Eastern District of Texas against HTC alleging infringement of the four patents at issue in the pending declaratory judgment action.[3] On June 4, 2008, TPL filed additional patent infringement actions against HTC in the Eastern District of Texas asserting U.S. Patent No. 5,530,890 ("the '890 patent").[4] On July 10, 2008, HTC amended its complaint before this court, adding claims for declaratory relief with respect to the '890 patent.[5] On February 23, 2009 the parallel Texas litigation was dismissed without prejudice following Judge Fogel's decision to deny TPL's Motion to Dismiss, or in the Alternative, to

[1] *See* Docket No. 1.

[2] *See* Docket No. 60 at 6-8.

[3] *See* Docket No. 16 at 3.

[4] *See* Docket No. 35 at 5.

[5] *See* Docket No. 34.

Transfer Venue in the California action.[6] On March 25, 2010, the court accepted the parties' stipulation to dismiss the '584 patent from this litigation.[7] On August 24, 2012, Technology Properties Limited, Patriot, and Phoenix Digital Solutions initiated an International Trade Commission investigation regarding HTC's alleged infringement of the '336 patent.[8] On July 17, 2013, the court accepted the parties' stipulation to dismiss the '148 and '749 patents from this litigation.[9] On September 19, 2013, the court accepted the parties stipulation to dismiss all claims relating to the '890 patent from this litigation.[10]

In sum, only the '336 patent was considered by the jury at trial.

B. The '336 Patent

The '336 patent issued on September 15, 1998, and describes a microprocessor with an internal variable speed clock, or oscillator, that drives the processor's central processing unit ("CPU").[11] Traditional microprocessors use external, fixed speed crystals to clock the CPU.[12] A CPU's maximum possible processing capacity depends on process, voltage, and temperature

[6] *See* Docket Nos. 49 (denying motion to dismiss, to transfer venue, and to stay) and 88 (granting motion for leave to file motion for reconsideration and denying motion for reconsideration).

[7] *See* Docket No. 152.

[8] *See* Docket No. 561-1. Claims 1, 6, 7, 9-11, and 13-16 were asserted in the investigation. On September 6, 2013, Administrative Law Judge James Gildea issued an Initial Determination from in the ITC proceeding holding that HTC did not violate Section 337 of the Tariff Act of 1930. *See id.*

[9] *See* Docket No. 462.

[10] *See* Docket No. 594.

[11] *See* Docket No. 393-3 at 1 ("A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a Central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor.").

[12] *See id.* at 17:12-14 ("Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations.").

("PVT parameters").[13] An external clock must therefore set the timing of the CPU to suboptimal PVT conditions, resulting in waste of the CPU's processing speed under optimal conditions. The internal, variable clock described in the '336 patent claims real-time adjustment of the timing of the CPU by placing the clock on the chip itself. Thus, the CPU can perform optimally under any set of parameters.[14] The microprocessor nevertheless requires a second external clock because devices other than the CPU do not operate at variable speed.[15]

Independent claim 6 provides:

A microprocessor system comprising:

> a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;
>
> an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

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[13] *See id.* at 17:21-22 ("Speed may vary by a factor of four depending upon temperature, voltage, and process.").

[14] *See id.* at 17:32-34 ("By decoupling the variable speed of the CPU 70 from the fixed speed of the I/O interface 432, optimum performance can be achieved by each.").

[15] *See id.* at 44-53 ("The designer of a high speed microprocessor must produce a product which operate over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing. Temperature, voltage, and process all affect transistor propagation delays. Traditional CPU designs are done so that with the worse case of the three parameters, the circuit will function at the rated clock speed. The result are designs that must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse case conditions."); *id.* at 16:67-17:10 ("By deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast. For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor 50 will operate slower than normal. Since the microprocessor 50 ring oscillator clock 430 is made from the same transistors on the same die as the latches and gates, it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.").

an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.[16]

C. The Verdict: HTC Infringes

A seven-day jury trial was held to consider whether HTC infringed the '336 patent.[17] At trial, HTC did not contest the validity of the '336 patent. HTC moved for judgment as a matter of law after the close of TPL's case.[18] After two days of deliberations, the jury found that HTC and its accused products literally infringed all asserted claims: 6, 7, 9, 13, 14, and 15.[19] As to damages, the jury made the following findings:

> 3. To the extent you have found that at least one claim of the '336 patent is infringed, what has TPL proven that it is entitled to as a reasonable royalty for infringement:
>
> One-time (lump sum) payment of $958,560 for the life of the patent.[20]

Following the jury verdict HTC filed a renewed motion for judgment as a matter of law that its products do not infringe the '336 patent.[21]

II. LEGAL STANDARDS

Fed. R. Civ. P. 50(b) provides that, upon a renewed motion for judgment as a matter of law, the court may: (1) "allow judgment on the verdict, if the jury returned a verdict," (2) "order a new trial," or (3) "direct the entry of judgment as a matter of law." To grant a Rule 50(b) motion, the court must determine that "the evidence, construed in the light most favorable to the non-moving

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[16] Docket No. 393-3.

[17] *See* Docket No. 657.

[18] *See* Docket No. 647. HTC also moved for judgment as a matter of law as to willful infringement and damages. The jury returned a verdict that HTC's infringement was not willful. HTC has not renewed its motion for judgment as a matter of law on the issue of damages. *See* Docket No. 654 at 3-4.

[19] *See* Docket No. 654 at 2.

[20] *Id.* at 4.

[21] *See* Docket 671.

party, permits only one reasonable conclusion, and that conclusion is contrary to the jury's."[22] In other words, to set aside the verdict, there must be an absence of "substantial evidence" – meaning "relevant evidence that a reasonable mind would accept as adequate to support a conclusion" – to support the jury's verdict.[23] "Substantial evidence is more than a mere" scintilla;[24] it constitutes "such relevant evidence as reasonable minds might accept as adequate to support a conclusion even if it is possible to draw two inconsistent conclusions from the evidence."[25] In reviewing a motion for judgment as a matter of law, the court "must view the evidence in the light most favorable to the non-moving party and draw all reasonable inferences in its favor."[26] "In ruling on such a motion, the trial court may not weigh the evidence or assess the credibility of witnesses in determining whether substantial evidence exists to support the verdict."[27]

III. DISCUSSION

A. The Jury Considered Substantial Evidence that the Accused Products Involve An "Entire Oscillator"

HTC first disputes the sufficiency of evidence regarding practice of the "entire oscillator" limitation. The court addressed the term in its order granting-in-part summary judgment of

[22] *Callicrate v. Wadsworth Mfg.*, 427 F.3d 1361, 1366 (Fed. Cir. 2005) (*quoting Pavao v. Pagay*, 307 F.3d 915, 918 (9th Cir. 2002)) ("The Ninth Circuit upholds any jury verdict supported by substantial evidence.").

[23] *Id.*

[24] *Chisholm Bris. Farm Equip. Co. v. Int'l Harvester Co.*, 498 F.2d 1137, 1140 (9th Cir. 1974) (*quoting Consol. Edison Co. v. NLRB*, 305 U.S. 197, 229 (1938)).

[25] *Landes Constr. Co. v. Royal Bank of Canada*, 833 F.2d 1365, 1371 (9th Cir. 1987).

[26] *Transbay Auto Serv., Inc. v. Chevron U.S.A., Inc.*, Case No. 3:09-cv-04932 SI, 2013 WL 496098, at *2 (N.D. Cal. Feb. 7, 2013) (*quoting Josephs v. Pacific Bell*, 443 F.3d 1050, 1062 (9th Cir. 2006) ("We must view the evidence in the light most favorable to the nonmoving party – here, Josephs, – and draw all reasonable inferences in that party's favor.")).

[27] *Id.* (citing *Mosesian v. Peat, Marwick, Mitchell & Co.*, 727 F.2d 873, 877 (9th Cir. 1984) ("Neither the district court nor this court may weigh the evidence or order a result it finds more reasonable if substantial evidence supports the jury verdict.")).

non-infringement and no willfulness.[28] The court explained:

> The court agrees with HTC that the disputed limitations are properly understood to exclude any external clock used to generate a signal.[29] Nevertheless, there remains a factual dispute whether HTC's products contain an on-chip ring oscillator that is self-generating and does not rely on an input control to determine its frequency. While HTC's expert says that the PLLs generate the clock, TPL's expert counters that the ring oscillators generate the clock and the PLLs merely buffer or fix the frequency.[30] This is a classic factual question that requires a trial to answer.[31]

HTC argues that the record at trial was uncontroverted that the ring oscillator in all accused HTC products is a phase locked loop ("PLL") and that the frequency output from the PLL is used to clock the CPU in the accused products. In particular, the frequency generated by that PLL relies on an off-chip crystal to set the frequency which is used to clock the CPU. The court's construction teaches that if an off chip crystal is used to clock the CPU, then the accused products fall outside of the claims. Because this was the factual predicate under which the trial was held and all of the evidence at trial demonstrates the PLLs in the accused products necessarily reference an off-chip signal in order to set the frequency to clock the CPU, no reasonable jury could find infringement. At bottom, the evidence was undisputed that the signal that is used to clock the CPU cannot exist but for the existence of the off chip crystal's input – there is nothing to clock the CPU if the off chip crystal is not referenced.

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[28] *See* Docket No. 585.

[29] The patentee's arguments traversing the prior art narrowed the claims. *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 535 U.S. 722, 740 (2002) ("A patentee's decision to narrow his claims through amendment may be presumed to be a general disclaimer of the territory between the original claim and the amended claim."); *cf. Saeilo Inc. v. Colt's Mfg. Co.*, 26 F. App'x 966, 973 (Fed. Cir. 2002) ("Where an amendment narrows the scope of a claim for a reason related to the statutory requirements for patentability, prosecution history estoppel acts as a complete bar to the application of the doctrine of equivalents to the amended claim element.").

[30] *Compare* Docket No. 457 at 16 ("the oscillators in the accused products indisputably rely on an external crystal or clock generator to clock" the CPU), *with* Docket No. 470 at 14 ("Each HTC product includes a CPU/system clock – a ***ring oscillator*** within a PLL – that ***generates*** a clock signal ***on its own***, as long as it has a power supply.") (emphasis in original).

[31] Docket No. 585 at 11.

TPL counters that HTC failed to preserve the issue, and that in any event there was sufficient evidence that even if the external crystal can be used to regulate frequency clocking the CPU that is separate and distinct from the generation of the clock. TPL points to testimony from its expert, Dr. Oklobdzija, that because one could remove the crystal and still see a signal, even though that was not how the accused products operate, that suggested to him, an expert in the field, that the crystal was not being used to generate the signal.[32] Oklobdzija also opined that no off-chip crystal is relied upon to generate a clock signal.[33] Even HTC's own expert opined that the external crystal clocks were used in HTC phones as reference signals, not to actually generate the on-chip clock signal itself.[34]

As an initial matter, the court is satisfied that HTC's arguments regarding the meaning of "entire oscillator" were preserved. After the court issued its order denying HTC's motion for summary judgment of non-infringement, HTC filed a motion requesting that the court adopt a jury instruction incorporating a construction of "entire oscillator" consistent with the order. In particular, HTC asked the court to adopt a construction that included two sentences: (1) a first sentence stating that the limitation is "not satisfied by an accused system that uses any external clock to generate a signal," and (2) a second sentence specifying, among other things, that an accused product can infringe only if it "does not rely on an input control to determine its frequency."[35] The court held a hearing on HTC's motion and issued an order adopting a

[32] *See* Docket No. 641, Trial Tr. at 565:15-19 ("The ring oscillator generates the clock regardless, and it will continue to generate the clock even when you disconnect this, the crystal.").

[33] *See id.*, Trial Tr. at 565:22-25 ("Q: Does any on-chip component rely on the off-chip crystal to generate a clock signal? A: No.").

[34] *See* Docket No. 643, Trial Tr. at 1019:23-1020:3 ("Q: And have you heard of the term "Crystal Clock," or "Crystal Oscillator"? A: Yeah. Crystal Oscillator is a component that you put a voltage on the component and then it starts oscillating at a fixed frequency. It's also part of a PLL. It feeds a PLL and makes sure that the PLL has a reference signal.").

[35] Docket No. 590 at 2:19-23; *see also* Docket No. 604 (citing the intrinsic record).

construction of "entire oscillator" based on a modified version of the first sentence of HTC's proposal. The court chose not to adopt the second sentence of HTC's proposal and informed the parties that it would instruct the jury in accordance with its construction.[36]

HTC raised this issue again with the court on the day before closing arguments in the context of jury instructions on the construction of "entire oscillator." During the jury instruction conference with the court, after taking up the jury instruction on claim construction, counsel for HTC asked the court to confirm that HTC's earlier objections and arguments with respect to its proposed two-sentence construction of "entire oscillator" had been preserved for the record. The court confirmed that they were.

> Mr. Weinstein:
>
> I just want to make sure, we understand you -- we had extensive argument about the entire oscillator term. We had a hearing prior to the trial and I just wanted to make sure that the objections that we had regarding the two sentences that we wanted are still preserved.
>
> The court:
>
> They are preserved, absolutely.[37]

Second, HTC's pre-verdict JMOL motion fully raised the argument that the accused HTC products do not infringe because the oscillator in the accused HTC products relies on an input control to determine its frequency.[38] HTC's pre-verdict motion specifically argued, for example, that the "entire oscillator" limitation was not satisfied because "the output frequency of the on-chip clock is expressly calculated, in each instance, based on the input frequency provided by the external clock."[39] HTC's motion explained in detail how the frequency of the on-chip oscillator

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[36] *See* Docket No. 607 at 1.

[37] Docket No. 695-2, Ex. 16 at 1456:16-21.

[38] *See* Docket No. 647 at 4-6.

[39] *Id.* at 6.

was based on a formula that expressly relies on the frequency input from the external clock, including specific citations to the evidentiary record at trial.[40]

This was sufficient.[41]

As for the merits of the dispute, Oklobdzija took the stand and offered expert testimony that, after considering the accused products, his opinion was that the CPU was clocked by an on-chip crystal. He emphasized that a ring oscillator in an HTC accused product does not use an external crystal/clock to generate a clock signal used by the CPU. In particular, he repeatedly clarified that a ring oscillator generates a clock signal on its own, without relying on external crystals.[42] HTC's technical expert, Mr. Gafford, also admitted that it is the ring oscillator that generates the clock signal for the CPU.[43] Gafford further admits that the external crystal is not used to generate the signal. Rather, its clock is used only to compare with the phase of the ring oscillator's already generated clock signal that has been steeply divided by the frequency divider.[44] As Oklobdzija explained, the ring oscillator generates a very high frequency clock signal on its

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[40] *See id.* at 4-6.

[41] *See C.B. v. City of Sonora*, 730 F.3d 816, 824 n.5 (9th Cir. 2013) (citing *EEOC v. Go Daddy Software, Inc.*, 581 F.3d 951, 961 (9th Cir. 2009)) (In the Ninth Circuit, "Rule 50(b) 'may be satisfied by an ambiguous or inartfully made motion under Rule 50(a),' and it is given a 'liberal interpretation' to avoid overly harsh results."); *W. Union Co. v. MoneyGram Payment Sys., Inc.*, 626 F.3d 1361, 1367 (Fed. Cir. 2010) (*quoting Blackboard, Inc. v. Desire2Learn, Inc.*, 574 F.3d 1371, 1379-80 (Fed. Cir. 2009) (holding that even "a cursory motion suffices to preserve an issue on JMOL so long as it 'serves the purposes of Rule 50(a), i.e., to alert the court to the party's legal position and to put the opposing party on notice of the moving party's position as to the insufficiency of the evidence.'").

[42] *See* Docket No. 641, Trial Tr. at 565:15-19 ("The ring oscillator generates the clock regardless, and it will continue to generate the clock even when you disconnect this, this crystal."); Trial Tr. 565:22-25 ("Q: Does any on-chip component rely on the off-chip crystal to generate a clock signal? A: No.").

[43] *See* Docket No. 684, Trial Tr. at 1364:18-22 ("Q: So you've got a 2.0 gigahertz clock signal generated by the ring oscillator that's clocking the CPU, and you divide by 100, and that's what this circuitry actually does; correct? A: Yes.").

[44] *See id.*, Trial Tr. at 1364:18-1365:1 ("Q: [The 2.0-gigahertz clock signal generated by the ring oscillator is divided by 100] [t]o get a 20 megahertz signal so that you can do edge matching with the external reference crystal signal in the phase detector, correct? A: Yes.").

own, which must then be divided to obtain a lower frequency so that its phase can be compared to the phase of the external reference.[45] After that, the PLL can make adjustments to the analog voltage/current provided to the ring oscillator to regulate – but not to generate – its frequency.[46]

Even if Oklobdzija's positions were later undermined by other evidence to a degree or diminished through cross-examination, his expert testimony as corroborated by other experts provides sufficient substantial evidence as required under Rule 50(b).

B. The Jury Considered Substantial Evidence of Variation of the Processing Frequency and Entire Oscillator as a Function of PVT

HTC next argues that no reasonable jury could have found infringement because TPL did not provide substantial evidence that the processing frequency of the CPU and entire oscillator "varied as a function of process, voltage, or temperature." In support, HTC claims the accused products "are designed to maintain the target frequency across PVT variations."[47] What's more, none "of the formulae for any Qualcomm, TI or Samsung chip recites any fabrication or operational parameter variation as playing any role in the determination of the PLL output

[45] *See* Docket No. 641, Trial Tr. at 569:2-18 ("Q: Where is the digital to analog converter here? A: It says DAC. DAC means digital to analog converter, the component here (indicating). So this output operation to extend the digital signal to DAC, this DAC just makes the plain voltage out (indicating), this voltage which comes from here (indicating), and produces this voltage which will smoothly move this one in the range we want it to oscillate (indicating). Now, let me go back just one second. This is a divider (indicating), and this is a comparator (indicating). This is what is called a phase detector (indicating). Here is the reference (indicating). This reference is compared with the divided signal here, and what it does is, you can see the switches, it either moves this voltage up or down. These capacitors have been charged and they filter that voltage so it's not jumping up and down, so it's smooth, that voltage, okay, when connected.").

[46] *See id.* at 569:19-22 ("And in this case this is disconnected, but when connected, it's converted into a current some with what digital PLL does, or digital output, same thing, voltage, and it will adjust this VCO, voltage control oscillator, ring oscillator.").

[47] Docket No. 643, Trial Tr. at 1062:2-3 ("Regarding PLL's, I can tell you that PLL's are designed to maintain the target frequency across PVT variations."); Docket No. 640, Trial Tr. at 359:2-8 ("Q: Is the output frequency from the DPLL stable? A: That is part of the specification. In other words, the outer clock is always known to have a known value within a tight range. That's how the specification on the PLL is developed. So yes, the answer is correct, it's stable, it's a known value.").

frequency. The accused HTC products, therefore, do not meet the "varying" limitations as a matter of law."[48]

Again, the court finds substantial evidence supports the jury's verdict. Gafford, HTC's expert, testified that the processing frequency of the CPU and the clock rate of the on-chip oscillator must always vary in the same way.[49] Because the claim limitation is disjunctive, TPL needed to show only that such variation is a function of at least one parameter among the several fabrication or operational parameters (e.g., voltage and temperature). With respect to at least the process / fabrication parameters, TPL met its burden. Process parameters vary from chip to chip because, as Gafford testified, process parameters are the same for components of the same chip, such as the CPU and the on-chip oscillator in each HTC accused product.[50] Gafford also admitted that such process variation between chips results in variation between chips in processing frequency and the associated clock rate.[51]

[48] Docket No. 671 at 8.

[49] *See* Docket No. 684, Trial Tr. at 1387:13-1388:1 ("Q: Let me ask you this: the processing frequency of the CPU and the clock rate of the entire oscillator must always vary together; right? A: Yes, they must vary in the same way. Q: They all – they must always vary in the same way, and the reason is that the CPU gets its processing frequency from the clock rate of the entire oscillator; right? A: I believe that's the way—I believe that's how everyone has agreed we're interpreting this element. Q: Okay. Like Dr. Oklobdzija's analogy, if I'm the entire oscillator and you're the CPU and we're shaking hands and I'm moving my hand at two hertz, your hand is also moving at two hertz; correct?

[50] *See id.*, Trial Tr. at 1394:8-11 ("Q: Now, Variations in fabrication parameters, again, are from chip to chip. They're not in the same chip during operation; right? A: Yes."); Trial Tr. at 1393:16-23 ("Q: Now, you also recognized that there have to be process variations among the chips in the HTC accused products; right? A: Yes. Q: Because process variation is endemic to silicon production; correct? A: Yes. Q: You can't get away from it; right? A: Yes.)".

[51] *See id.*, Trial Tr. at 1390:2-11 ("Q: But when we're talking about fabrication variations, those are variations from chip to chip; right? A: Yes. Q: So some chips will have the ability to run faster and some chips will only be able to run at slower speeds; right? A: That's right. Q: And that's why we have a binning step in manufacturing chips; correct? A: As to its effect on the CPU speed, yes, that is what binning does."); Trial Tr. at 1394:8-11 ("Q: Now, Variations in fabrication parameters, again, are from chip to chip. They're not in the same chip during operation; right? A: Yes.").

Evidence of process variation, and therefore processing frequency and clock rate variation, between chips, was shown in all HTC accused products. Qualcomm's representative, Sina Dena, testified, for example, that for the same chip design, Qualcomm separates chips with higher clock speeds at the "high end" or "fast corner of the process," from chips with lower clock speeds at the "slower corner of the process" -- a practice called binning.[52] Qualcomm assigns different product names or designations to chips in different bins even though they have the "same design."[53] In fact, "the higher speed bin products will have potentially a different frequency plan."[54] Qualcomm charges more for such chips.[55] Gafford confirmed that "there have to be process variations among

[52] *See* Docket No. 643, Trial Tr. at 1083:5-14 ("The court: The next question has to do with binning. We've heard much discussion in this trial about binning. When you were describing binning earlier during your testimony, were you referring to binning of a single or common IC design? The witness: Yes. Basically it's – it's – it's the same design which performs, can take higher clock speeds at the high end of the process, at the fast corner of the process and versus, you know, lower clock speed at the slower corner of the process.")

[53] *See id.*, Trial Tr. at 1083:5-14 ("The court: The next question has to do with binning. We've heard much discussion in this trial about binning. When you were describing binning earlier during your testimony, were you referring to binning of a single or common IC design? The witness: Yes. Basically it's – it's – it's the same design which performs, can take higher clock speeds at the high end of the process, at the fast corner of the process and versus, you know, lower clock speed at the slower corner of the process."); Trial Tr. at 1064:14-24 ("Q: Okay. Understood so you change the PLL based on the speed bin that the chip goes in; right? A: Right. And the chips usually are going to have a different identification when they are at the higher speed versus the one that – Q: And I think you called these premium chips, the faster ones, right? A: I don't know if it's premium, but the marketing group. Q: But you're able to charge more money for those chips; right? A: Yes."); 1083:22-23 ("Now, usually when the binning is done, either product name is changed or there is some sort of designation that goes.").

[54] *See id.*, Trial Tr. at 1083:22-1084:5. ("Now, usually when the binning is done, either product name is changed or there is some sort of designation that goes. So it's -- even though you might call it the same design, the higher speed bin products will have potentially a different frequency plan, and it's very simple to manage with a single release of software that we do for these chips. Basically the software reads the fuse space, finds it, okay, this is a faster device, so I'm going to change my PLL plan to a different setting for this particular device.").

[55] *See id.*, Trial Tr. at 1064:10-24 ("A: Now, is there a market for 1.2 Gigahertz? Sure, there is if you do that. So we have a premium for the fast corner process devices, and then the frequency plan, the PLL plan is going to change for that particular group of devices. Q: Okay. Understood so you change the PLL based on the speed bin that the chip goes in; right? A: Right. And the chips usually are going to have a different identification when they are at the higher speed versus the one that – Q: And I think you called these premium chips, the faster ones, right? A: I don't know if it's premium, but the marketing group. Q: But you're able to charge more money for those chips; right? A: Yes.").

the chips in the HTC accused products," "because process variation is endemic to silicon production."[56]

As to the formulae cited by HTC, they merely show how the ring oscillator uses the external crystal clock as a reference, not how the ring oscillator actually generates the clock signal. HTC's own witness, Mr. Fichter, testified that the external crystal clock in the HTC phones serves merely as a reference signal.[57] Dena confirmed that this crystal functions as a reference for the Qualcomm chips used in the HTC phones.[58] Dr. Haroun, a corporate representative from Texas Instruments, also confirmed that the external crystal clock functions as a reference for the TI chips used in the HTC phones.[59] Because the external crystal serves merely as a reference, if that crystal

[56] *See* Docket No. 684, Trial Tr. at 1393:16-23 ("Q: Now, you also recognized that there have to be process variations among the chips in the HTC accused products; right? A: Yes. Q: Because process variation is endemic to silicon production; correct? A: Yes. Q: You can't get away from it; right? A: Yes.)".

[57] *See* Docket No. 643, Trial Tr. at 1019:23-1020:3 ("Q: And have you heard of the term "Crystal Clock," or "Crystal Oscillator"? A: Yeah. Crystal Oscillator is a component that you put a voltage on the component and then it starts oscillating at a fixed frequency. It's also part of a PLL. It feeds a PLL and makes sure that the PLL has a reference signal.").

[58] *See id.*, Trial Tr. at 1044:2-12 ("Q: And at a high level, what is the purpose of a phase lock loop? A: Phase lock loop is used to provide a fixed target frequency clock signal. Q: And generally how is that achieved? A: In the Qualcomm family of chips, basically there's a fixed reference input clock that comes to a box, phase lock loop. There are elements that go into it, we call them L, M, N, different parameters, and the output frequency of the phase lock loop would be a mathematical formula of those elements multiplied by the input reference clock frequency."), Trial Tr. at 1048:10-15 ("Q: Okay. Now, one more last question about this. This TCXO right here, is that a -- what type of signal is that (indicating)? A: It's what you call a reference clock signal fixed at 19.2 and it's extremely important for PLL operation for this signal to be fixed across variation and temperatures (indicating).").

[59] Docket No. 640, Trial Tr. at 350:14-17 ("Q: Now, all of the – now, all of the OMAP chips use PLL's with -- that have a reference signal from an external clock; correct? A: That is correct."). In fact, Dr. Haroun admitted that only the ring oscillator in the TI chips could create or generate the high frequency used to clock the CPU. *Id.* at Trial Tr. at 353:23-354:3 ("Q: Okay. Let me clarify it this way: there's no other portion in the PLL besides the ring osciallator that can create a frequency that's so much higher than the external crystal; correct? A: That is correct. That is where it's -- where the extra edges are generated, yes.").

is disconnected, the ring oscillator will still be able to generate a clock signal.[60] HTC's focus on the formulae therefore ignores the fact that differently binned chips – even if they have the same design – are set to run at different frequencies and sold for different prices.

In sum, substantial evidence supports the jury's infringement verdict.

IT IS SO ORDERED.

Dated: January 21, 2014

PAUL S. GREWAL
United States Magistrate Judge

[60] *See* Docket No. 641, Trial Tr. at 567:8-22 ("Q: So the ring oscillator will still run if you disconnect the crystal? A: Yes, because crystal is not essential to generate the clock. Crystal is not needed to generate the clock.")

would lead a competitor to believe that the patentee had disavowed" devices otherwise covered by the claim language). Thus, if an inventor defines a term or otherwise disclaims a meaning during prosecution, the inventor has acted as his own lexicographer and the term is limited to the scope of the definition or disclaimer. *Astrazeneca AB v. Mut. Pharm. Co., Inc*., 384 F.3d 1333, 1341-42 (Fed. Cir. 2004) (the inventor's reference to language in the specification as a "definition" constituted lexicography); *Schoenhaus v. Genesco, Inc*., 440 F.3d 1354, 1358-60 (Fed. Cir. 2006) (lexicography in file history by virtue of disclaimer of scope of claim term during prosecution).

IV. CLAIM CONSTRUCTION

The parties propose the following constructions of the term "an entire oscillator disposed upon said integrated circuit substrate," which is recited in asserted independent claims 6 and 13 of the '336 patent. Ex. A ('336 patent *Ex Parte* Reexamination Certificate) at 2:18-19, 3:34-35 (TPL853_00000053.)

Term	Defendants' Construction	Plaintiffs' Construction
an entire oscillator disposed upon said integrated circuit substrate	an oscillator that is located entirely on the same semiconductor substrate as the central processing unit and does not rely on a control signal or an external crystal/clock generator to cause clock signal oscillation or control clock signal frequency	An [oscillator] that is located entirely on the same semiconductor substrate as the [central processing unit].

The intrinsic evidence compels Defendants' construction because it embodies clear disclaimers of claim scope that the applicants made during the prosecution of the '336 patent to secure allowance of their claims over otherwise invalidating prior art. Defendants' construction is also consistent with the specification's teachings, its criticisms of the prior art, and the plain language of the claims. These unambiguous disclaimers and teachings in the intrinsic evidence mandate that the claimed "entire oscillator" cannot rely on any off-chip crystal, off-chip clock generator, or control signal to cause clock signal oscillation or control clock signal frequency. Defendants' construction incorporates these key disclaimers and teachings, while Plaintiffs' construction ignores them. Furthermore, as established below, by clearly incorporating these

United States Patent [19]

Magar

[11] **Patent Number: 4,503,500**

[45] **Date of Patent: Mar. 5, 1985**

[54] **MICROCOMPUTER WITH BUS INTERCHANGE MODULE**

[75] Inventor: **Surendar S. Magar**, Houston, Tex.

[73] Assignee: **Texas Instruments Incorporated**, Dallas, Tex.

[21] Appl. No.: **619,650**

[22] Filed: **Jun. 15, 1984**

Related U.S. Application Data

[63] Continuation of Ser. No. 347,860, Feb. 11, 1982.

[51] **Int. Cl.**³ **G06F 3/00**

[52] **U.S. Cl.** **364/200**

[58] **Field of Search** 364/200, 900

[56] **References Cited**

U.S. PATENT DOCUMENTS

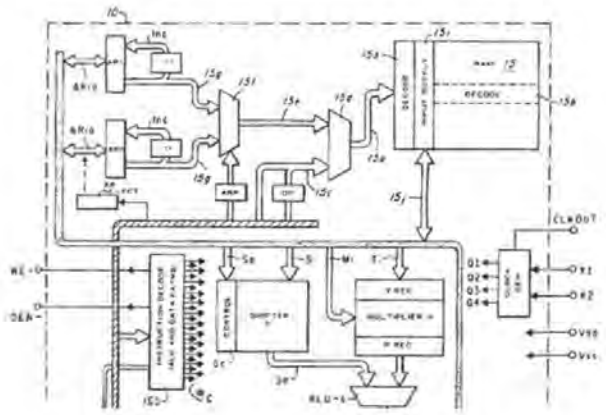
4,309,754	1/1982	Dinwiddie, Jr.	364/200
4,339,793	7/1982	Marenin	364/200
4,348,743	9/1982	Dozier	364/900
4,378,589	3/1983	Finnegan et al.	364/200

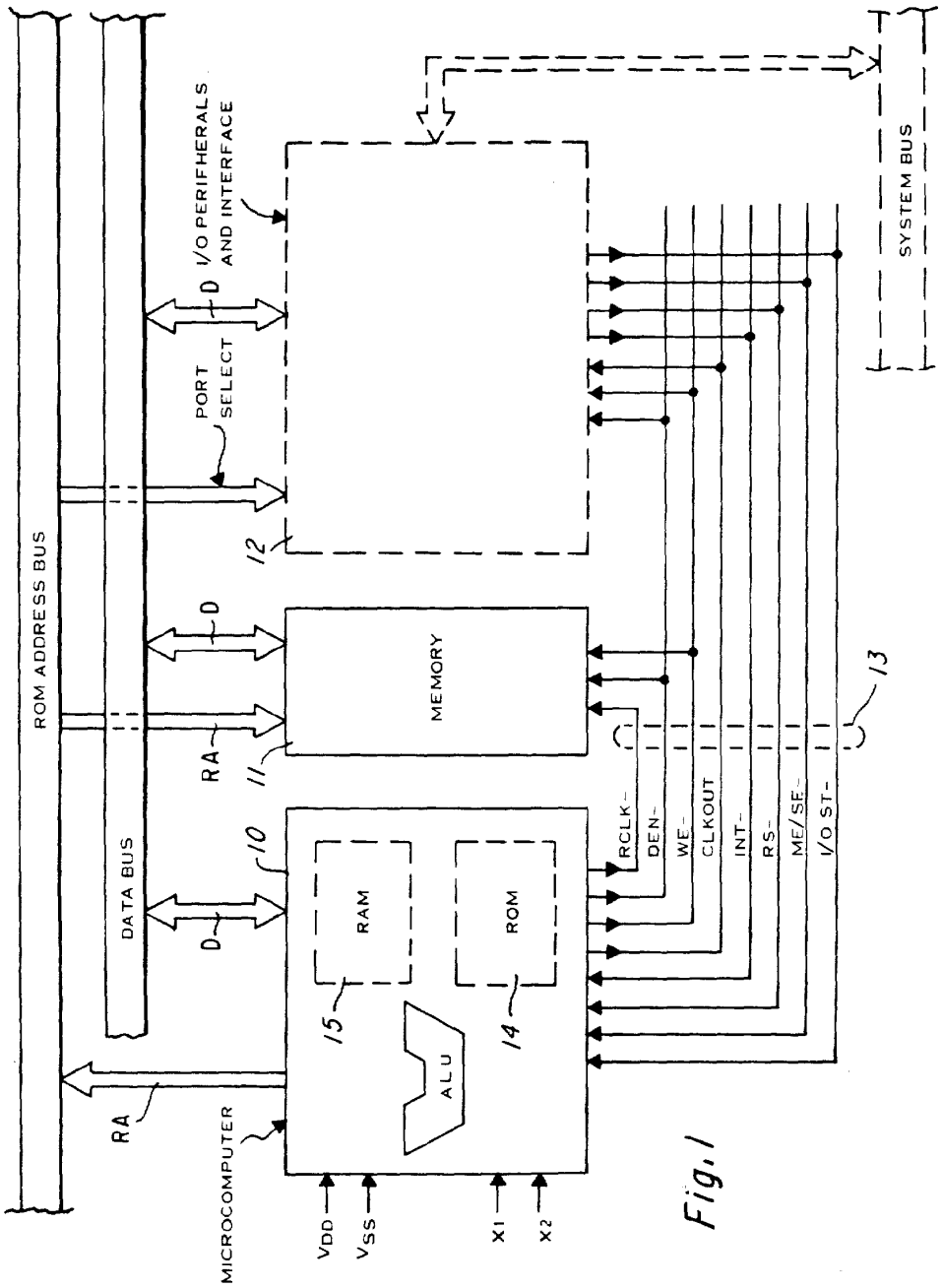
Primary Examiner—Gareth D. Shaw
Assistant Examiner—Ronni S. Malamud
Attorney, Agent, or Firm—John G. Graham

[57] **ABSTRACT**

A system for real-time digital signal processing employs a single-chip microcomputer device having separate on-chip program ROM and data RAM, with separate address and data paths for program and data. An external program address bus allows off-chip program fetch in an expansion mode, with the opcode returned by an external data bus. A bus interchange module allows transfer between the separate internal program and data busses in special circumstances. The internal busses are 16-bit, while the ALU and accumulator are 32-bit. A multiplier circuit produces a single state 16×16 multiply function separate from the ALU, with 32-bit output to the ALU. One input to the ALU passes through a 0-to-15 bit shifter with sign extension.

9 Claims, 15 Drawing Figures

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DATA BUS
I/O PERIFHERALS AND INTERFACE
PORT SELECT
SYSTEM BUS
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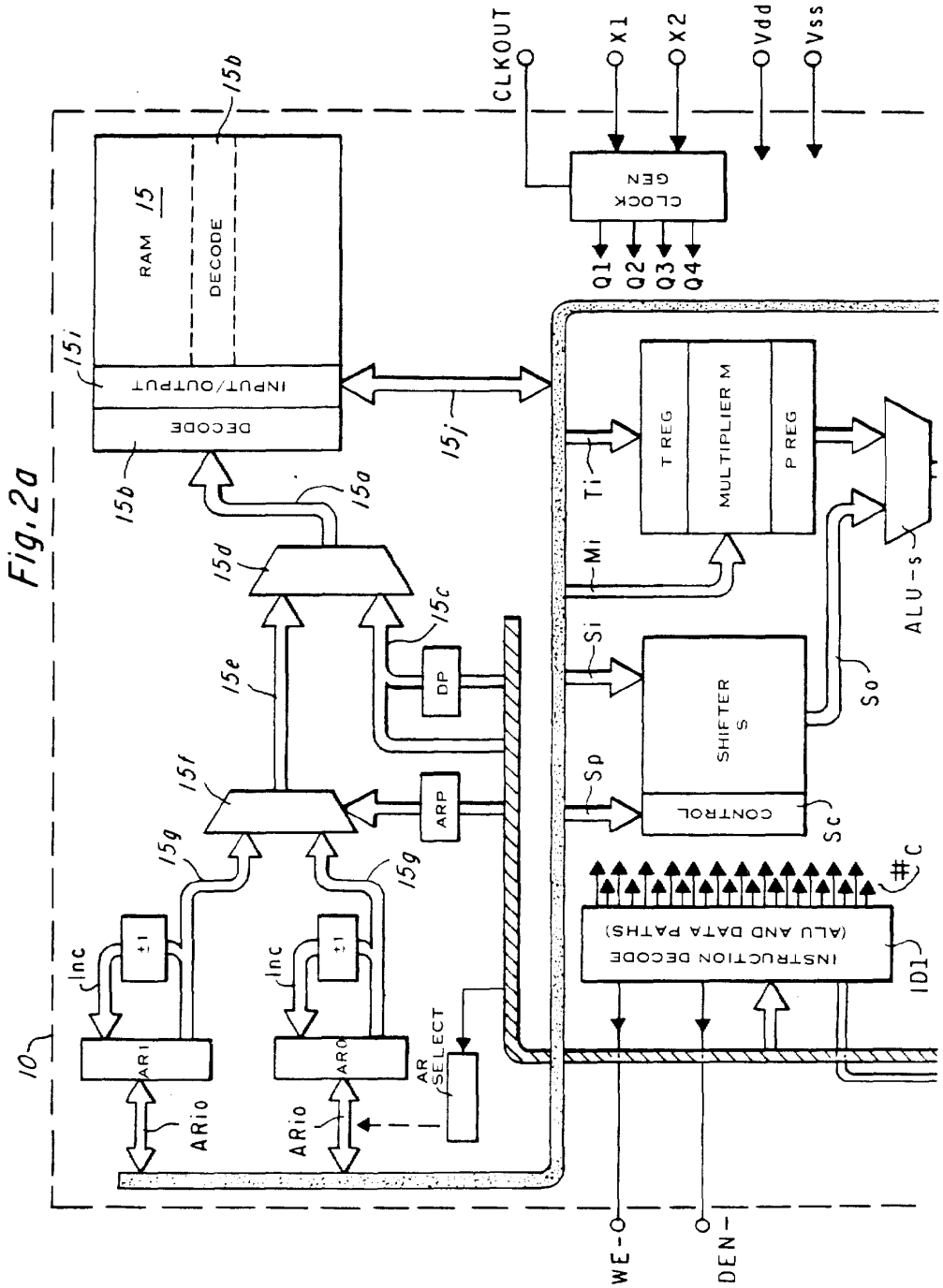
Fig. 1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DEN-

Fig. 2a

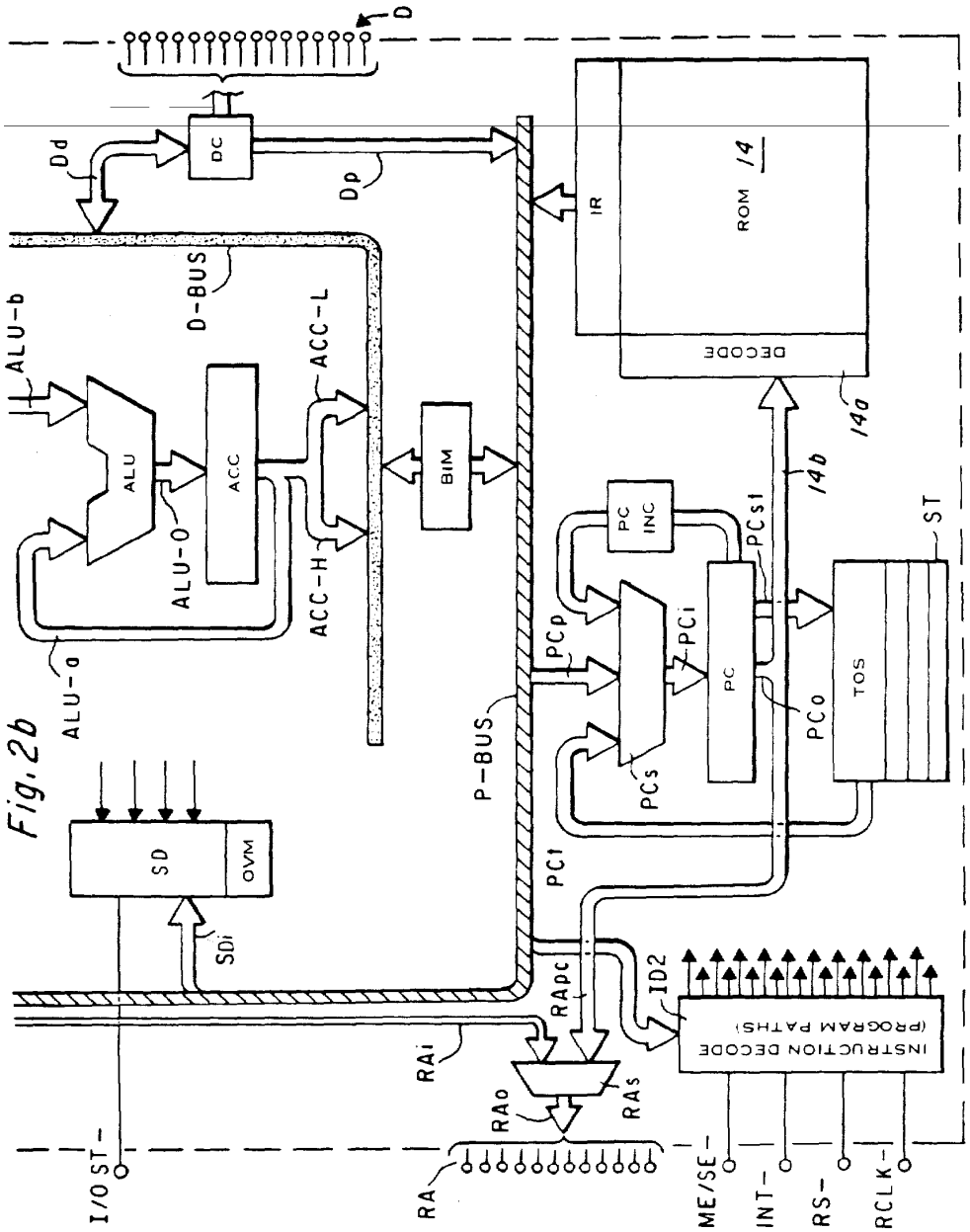

D
Dd
DC
Dp
D-BUS
ALU-b
ACC-L
ALU
ACC
ALU-0
ACC-H
BIM
ALU-a
P-BUS
IR
ROM 14
DECODE
14a
14b
PC INC
PCsi
PCp
PCi
PC
PCo
PCs
TOS
ST
PCi
SD
OVM
SDi
RApc
ID2
INSTRUCTION DECODE
(PROGRAM PATHS)
RAi
RAo
RAs
RA
I/O ST-
ME/SE-
INT-
RS-
RCLK-

Fig. 2b

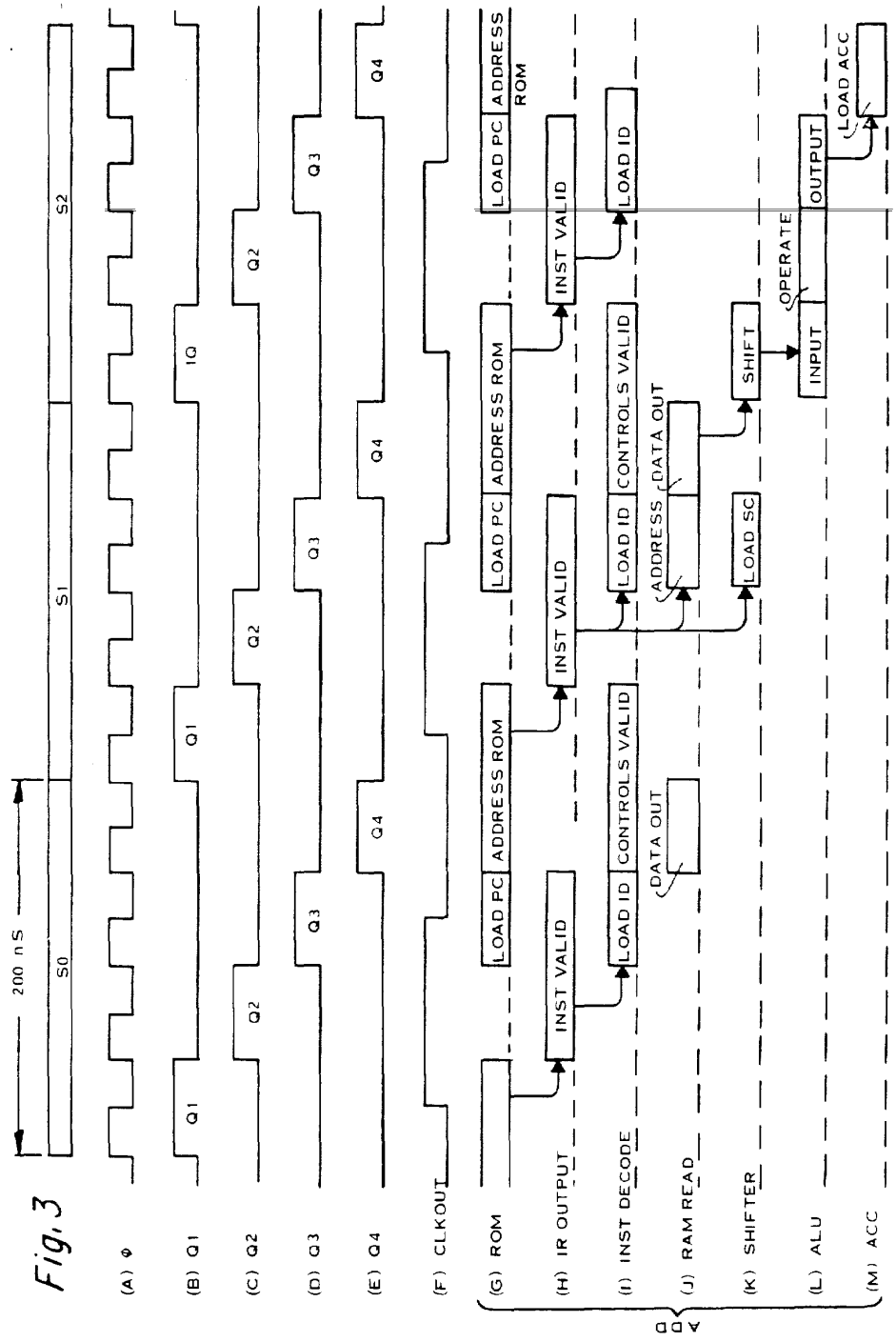


Fig. 3

TPL853_02954528

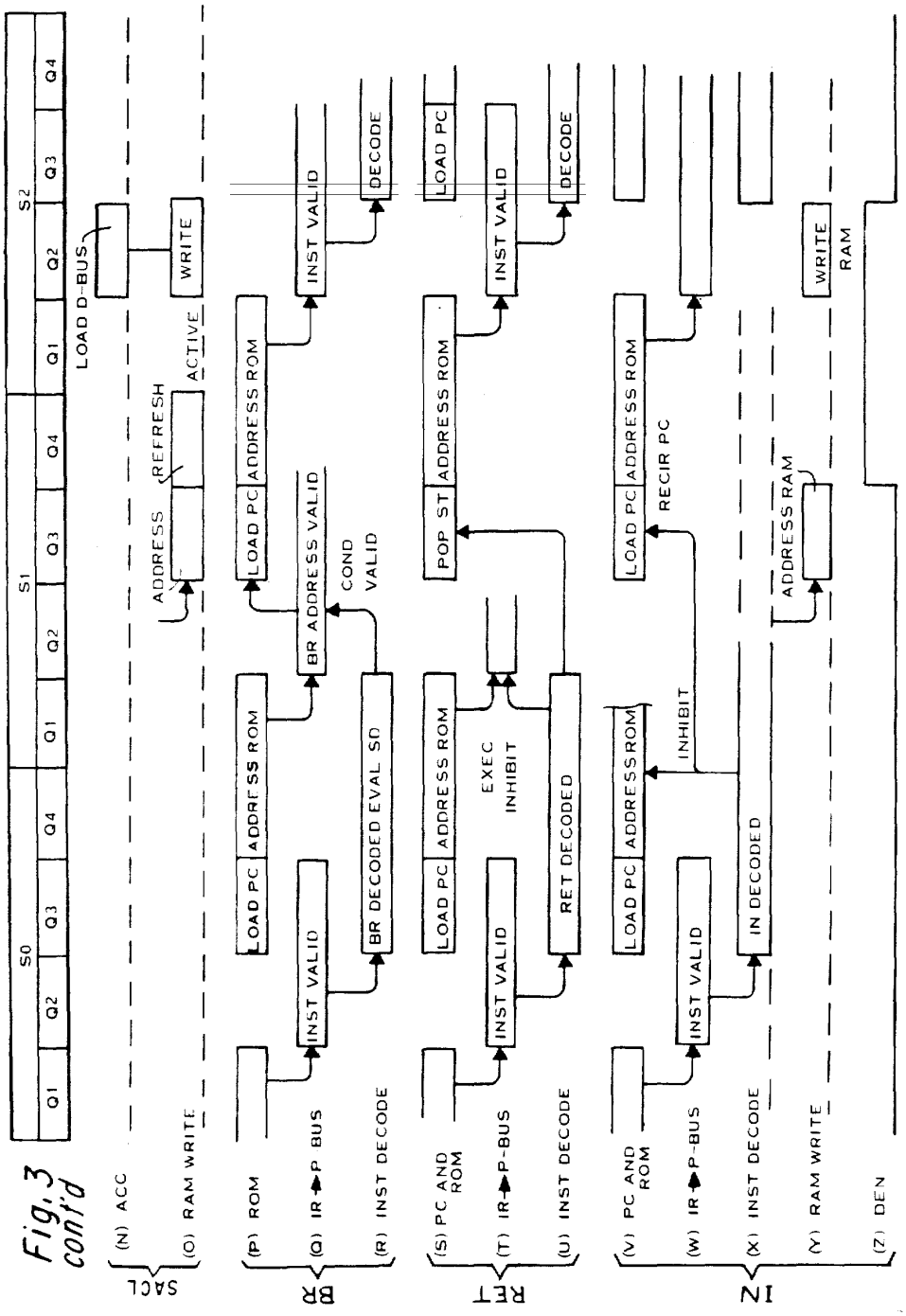


Fig. 3 cont'd

TPL853_02954529

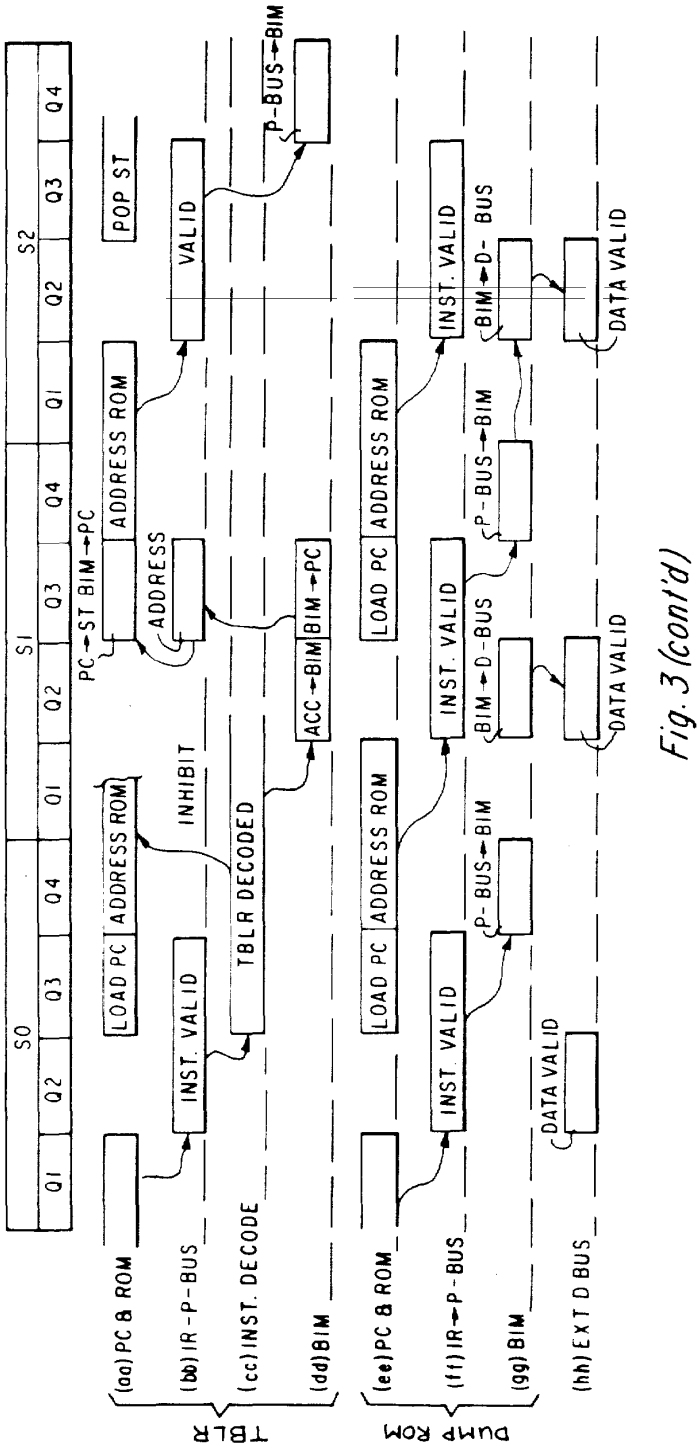

S0
S1
S2
Q1
Q2
Q3
Q4
(aa) PC & ROM
(bb) IR-P-BUS
(cc) INST. DECODE
(dd) BIM
(ee) PC & ROM
(ff) IR→P-BUS
(gg) BIM
(hh) EXT D BUS
LOAD PC
ADDRESS ROM
INST. VALID
TBLR DECODED
INHIBIT
PC→ST BIM→PC
ADDRESS
VALID
ACC→BIM BIM→PC
POP ST
P-BUS→BIM
BIM→D-BUS
DATA VALID
TBLR
DUMP ROM

Fig. 3 (cont'd)

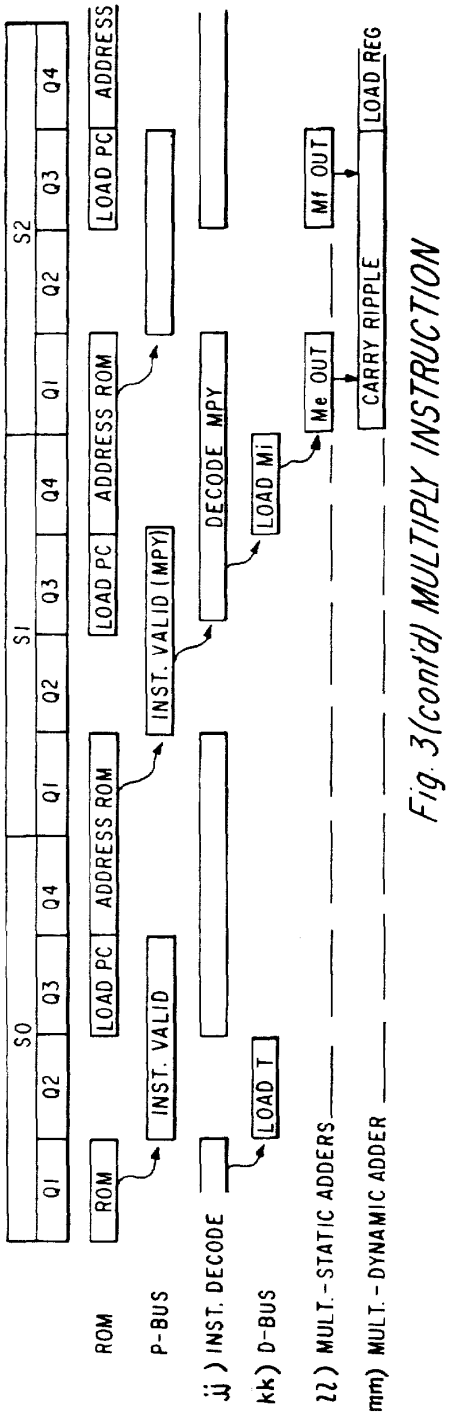


Fig. 3(cont'd) MULTIPLY INSTRUCTION

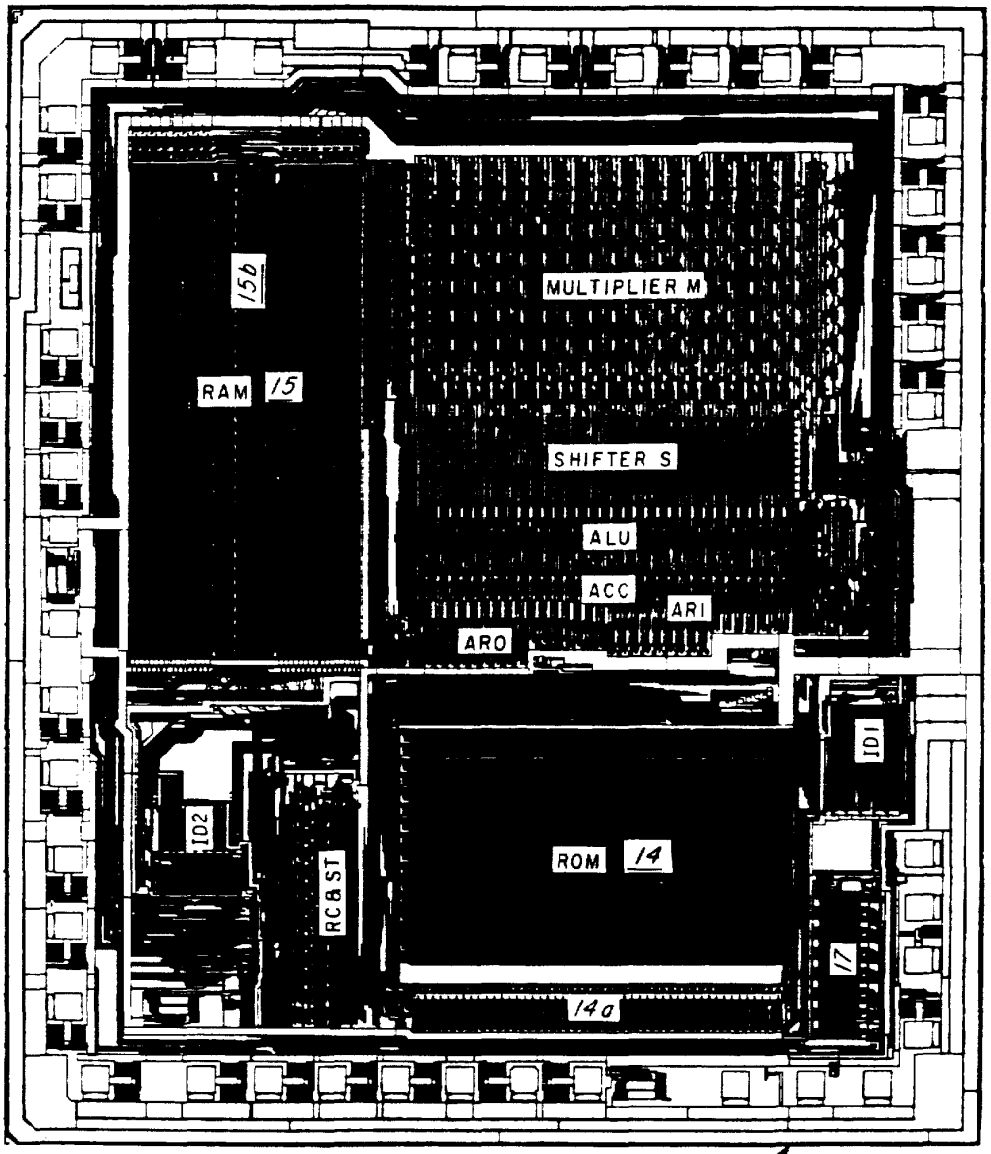

15b
MULTIPLIER M
RAM 15
SHIFTER S
ALU
ACC
ARI
ARO
ID1
ID2
RC & ST
ROM 14
17
14a

Fig. 4 10

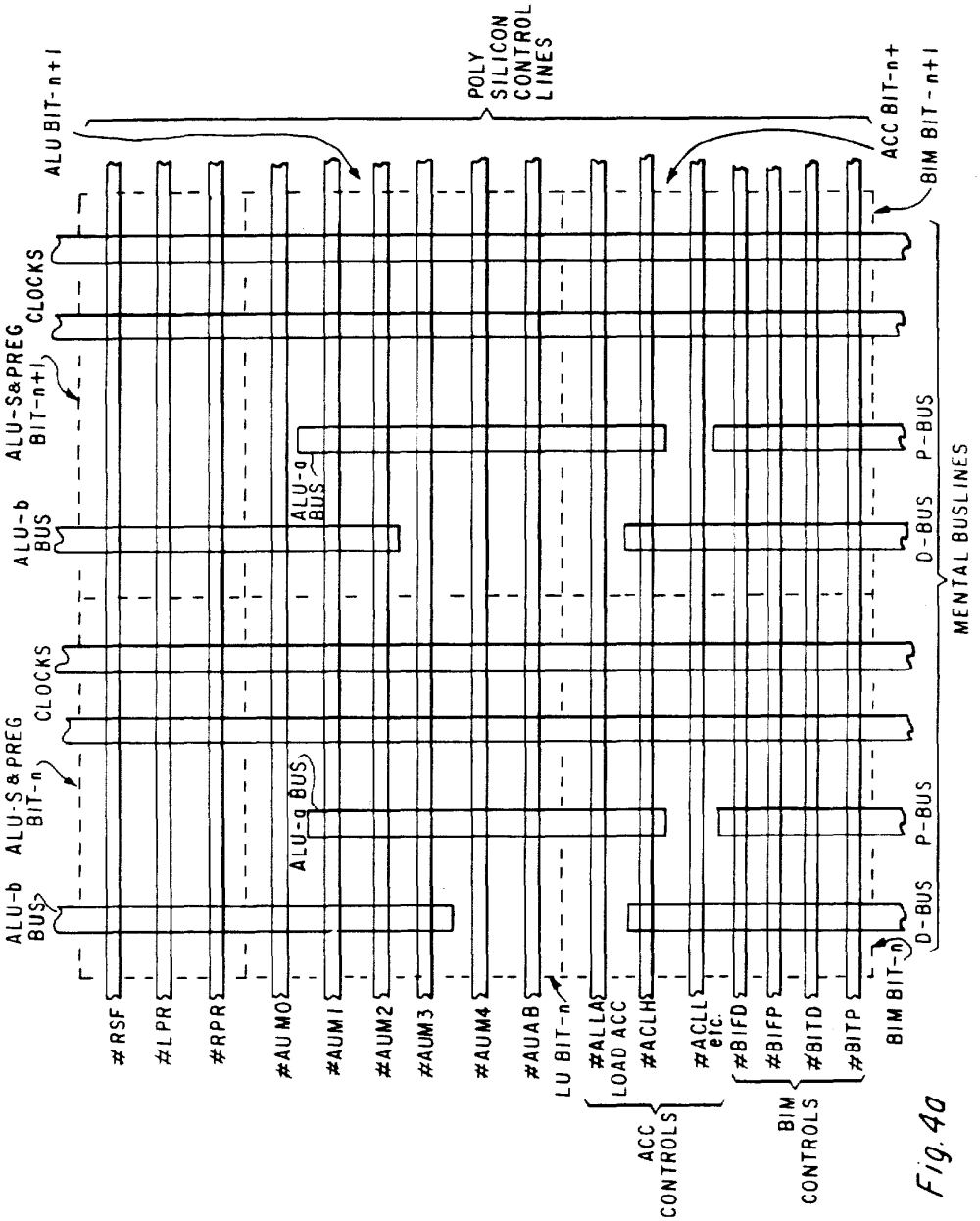


Fig. 40

TPL853_02954533

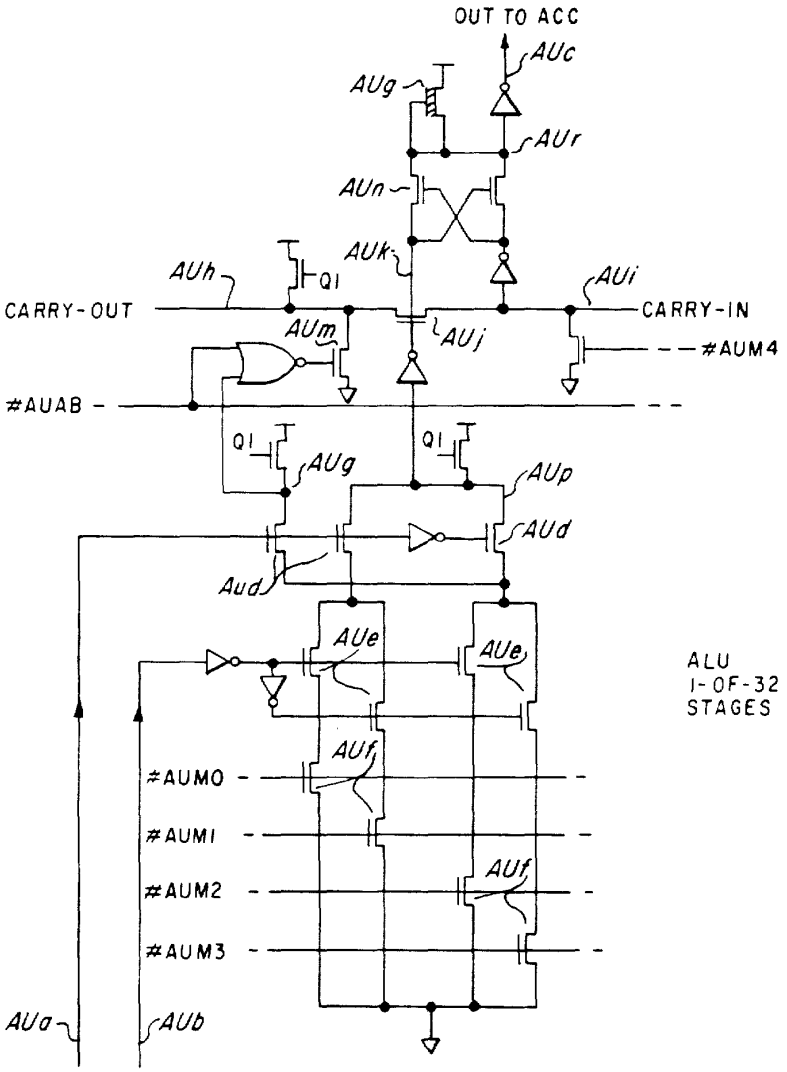

OUT TO ACC
AUc
AUg
AUr
AUn
AUk
AUh
Q1
AUi
CARRY-OUT
CARRY-IN
AUm
AUj
#AUM4
#AUAB
Q1
Q1
AUg
AUp
AUd
Aud
AUe
AUe
ALU
1-OF-32
STAGES
AUf
#AUMO
#AUM1
AUf
#AUM2
#AUM3
AUa
AUb

Fig. 5a

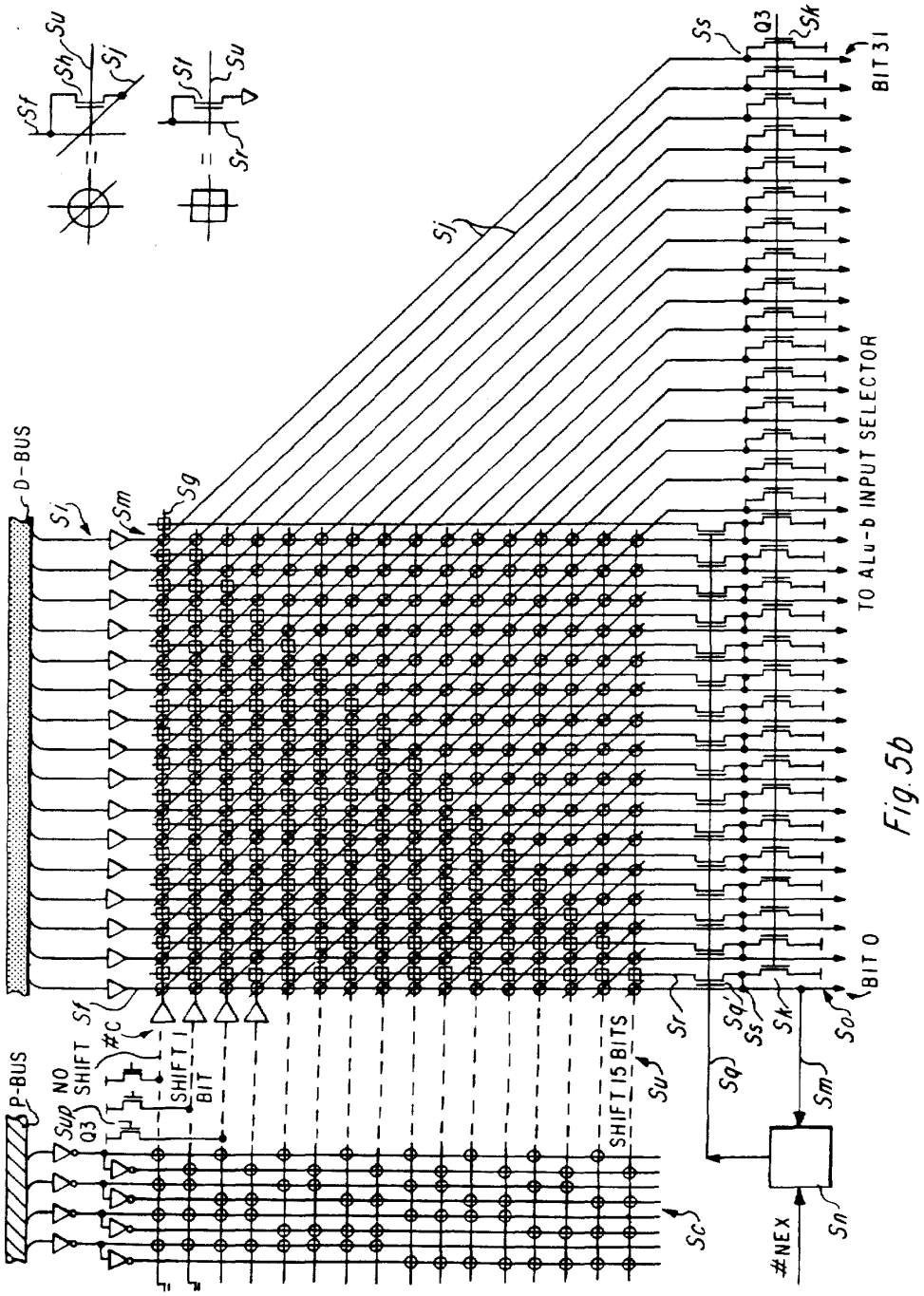
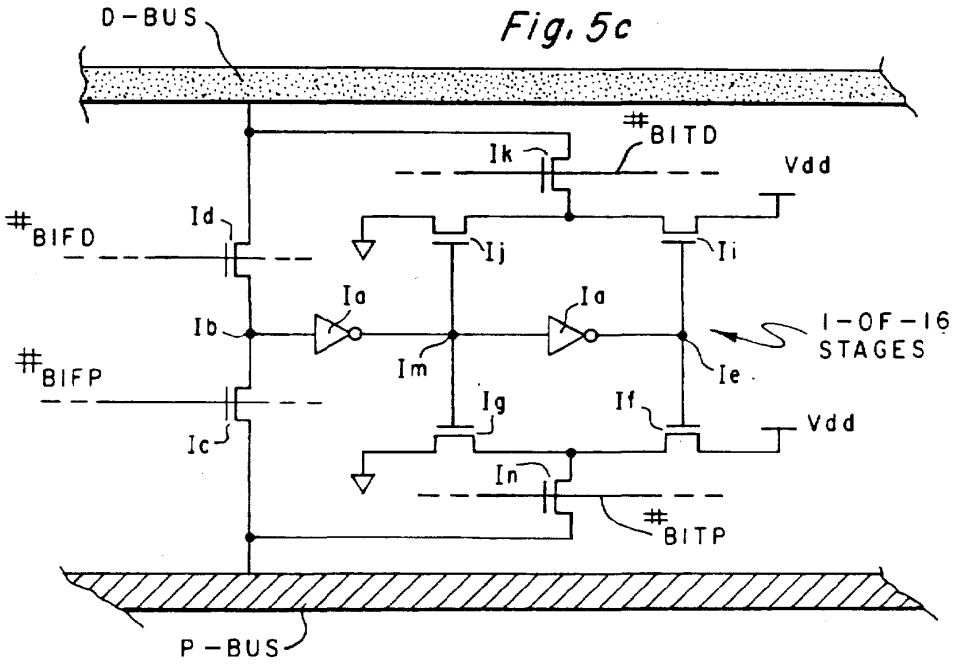

Su
Sh
Sj
Sf
Sr
Ss
Q3
Sk
BIT 31
Sj
D-BUS
Sm
Sg
TO ALu-b INPUT SELECTOR
Sf
#C
P-BUS
NO SHIFT
Sup
Q3
SHIFT 1 BIT
SHIFT 15 BITS
Su
Sr
Sq
Ss
Sk
So
BIT 0
Sq
Sm
Sc
#NEX
Sn

Fig. 5b

Fig. 5c


D-BUS
#BITD
Ik
Vdd
#BIFD
Id
Ij
Ii
Ia
Ia
Ib
I-OF-16
STAGES
#BIFP
Im
Ie
Ig
If
Vdd
Ic
In
#BITP
P-BUS

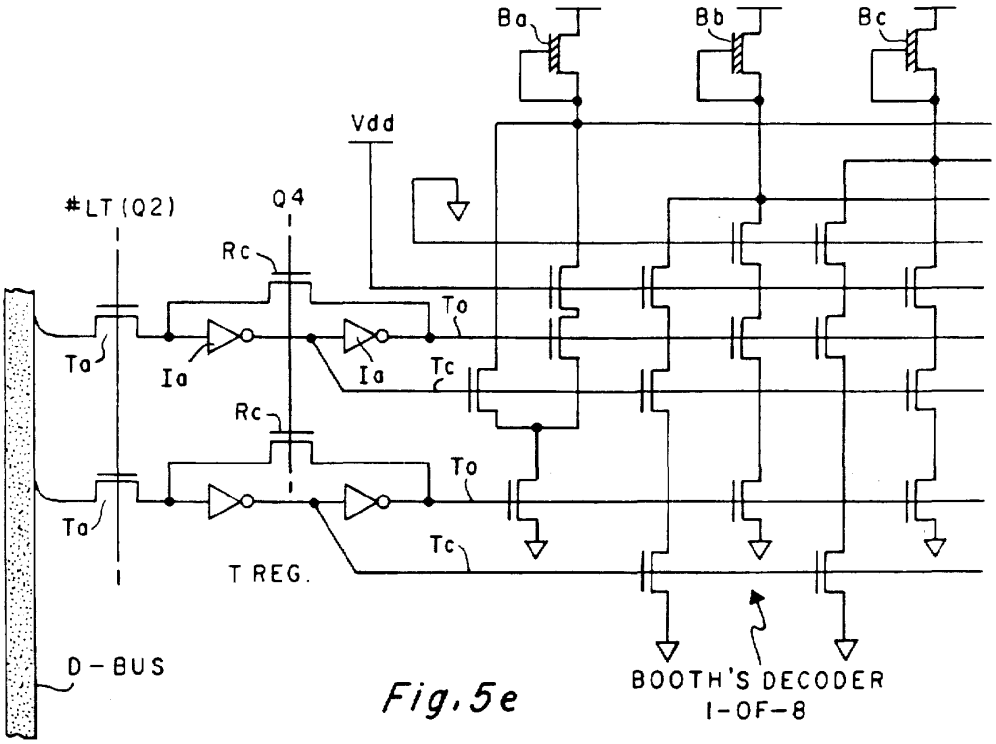

Ba
Bb
Bc
Vdd
#LT(Q2)
Q4
Rc
To
Ta
Ia
Ia
Tc
Rc
To
Ta
Tc
T REG.
D-BUS
BOOTH'S DECODER
I-OF-8

Fig. 5e

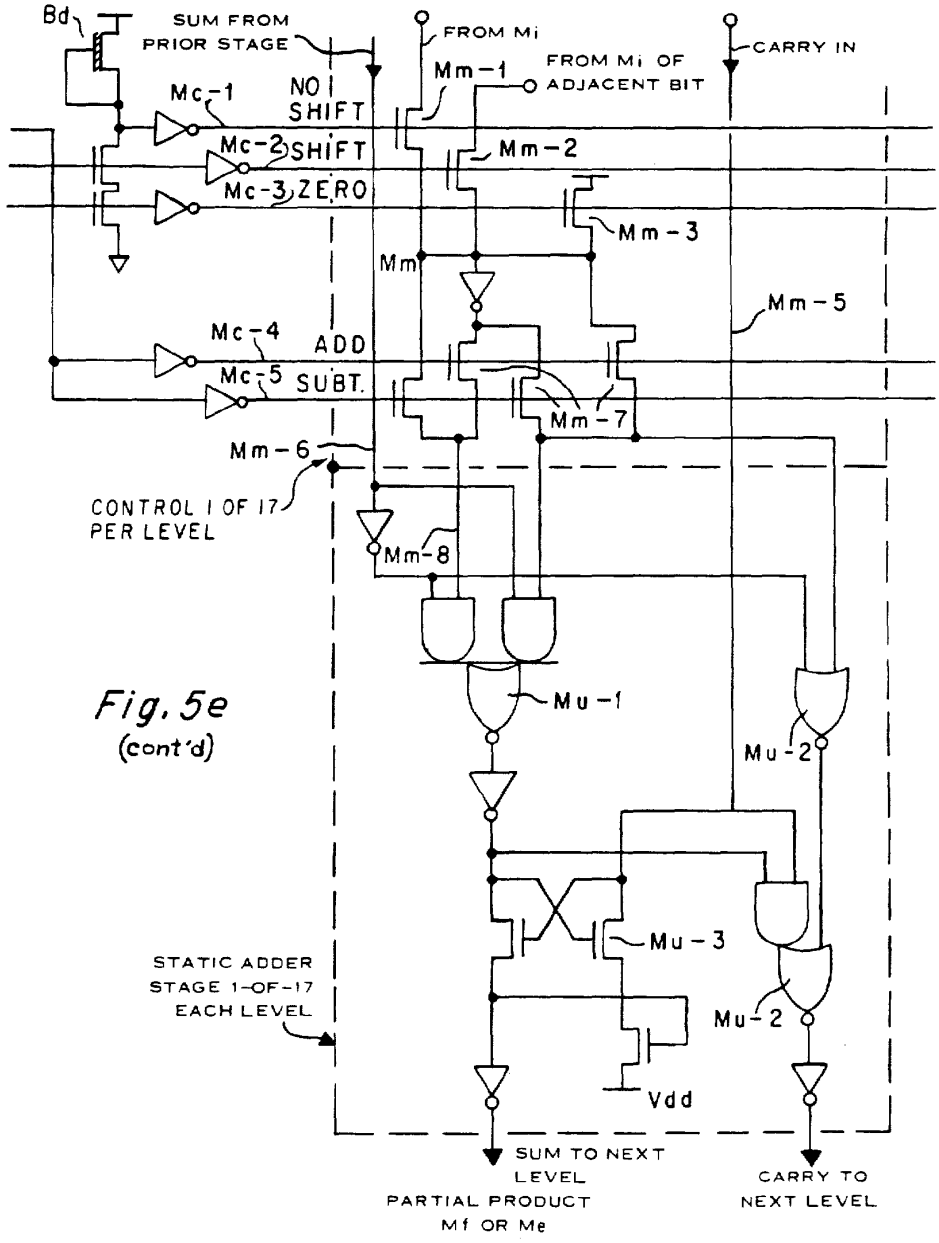
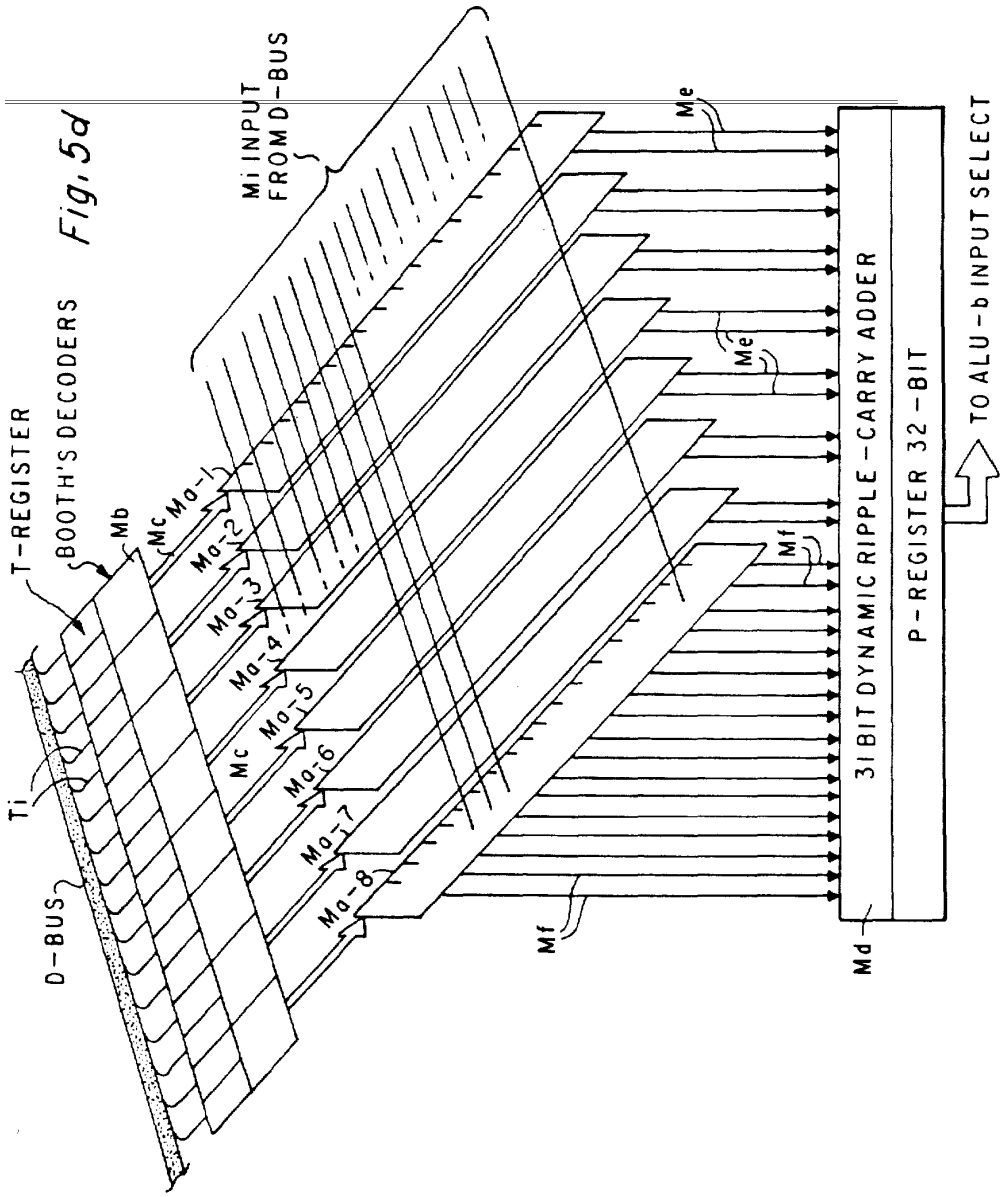

Bd
SUM FROM PRIOR STAGE
FROM Mi
FROM Mi OF ADJACENT BIT
CARRY IN
Mm-1
Mc-1
NO SHIFT
Mc-2 SHIFT
Mc-3 ZERO
Mm-2
Mm-3
Mm
Mm-5
Mc-4
ADD
Mc-5 SUBT.
Mm-7
Mm-6
CONTROL 1 OF 17 PER LEVEL
Mm-8
Mu-1
Mu-2
Mu-3
Mu-2
STATIC ADDER STAGE 1-OF-17 EACH LEVEL
Vdd
SUM TO NEXT LEVEL PARTIAL PRODUCT Mf OR Me
CARRY TO NEXT LEVEL

Fig. 5e
(cont'd)



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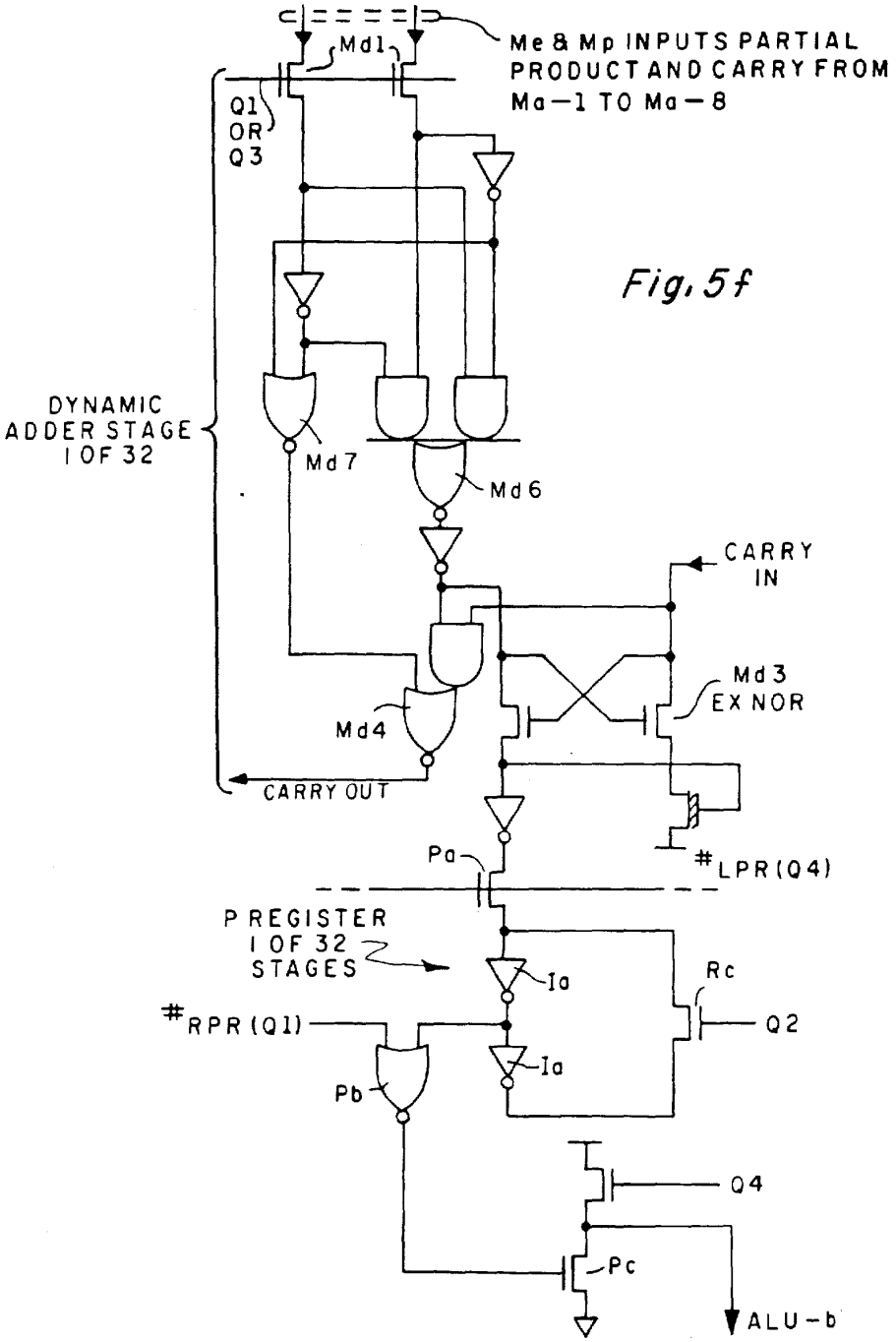

Me & Mp INPUTS PARTIAL PRODUCT AND CARRY FROM Ma−1 TO Ma−8
Md1
Q1 OR Q3
DYNAMIC ADDER STAGE 1 OF 32
Md 7
Md 6
CARRY IN
Md 3 EX NOR
Md4
CARRY OUT
Pa
#LPR(Q4)
P REGISTER 1 OF 32 STAGES
Ia
Rc
Q2
#RPR(Q1)
Ia
Pb
Q4
Pc
ALU−b

Fig. 5f

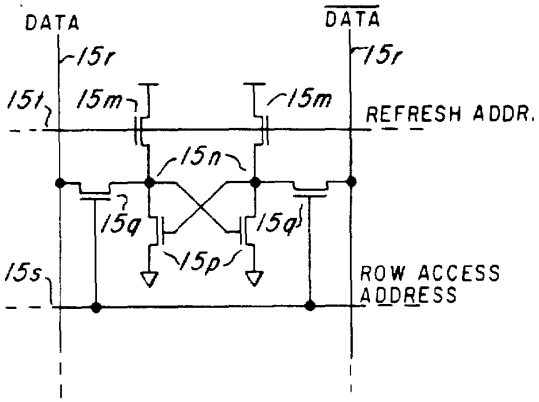

DATA
DATA
15r
15r
151
15m
15m
REFRESH ADDR.
15n
15q
15q
15p
15s
ROW ACCESS ADDRESS

Fig. 5g

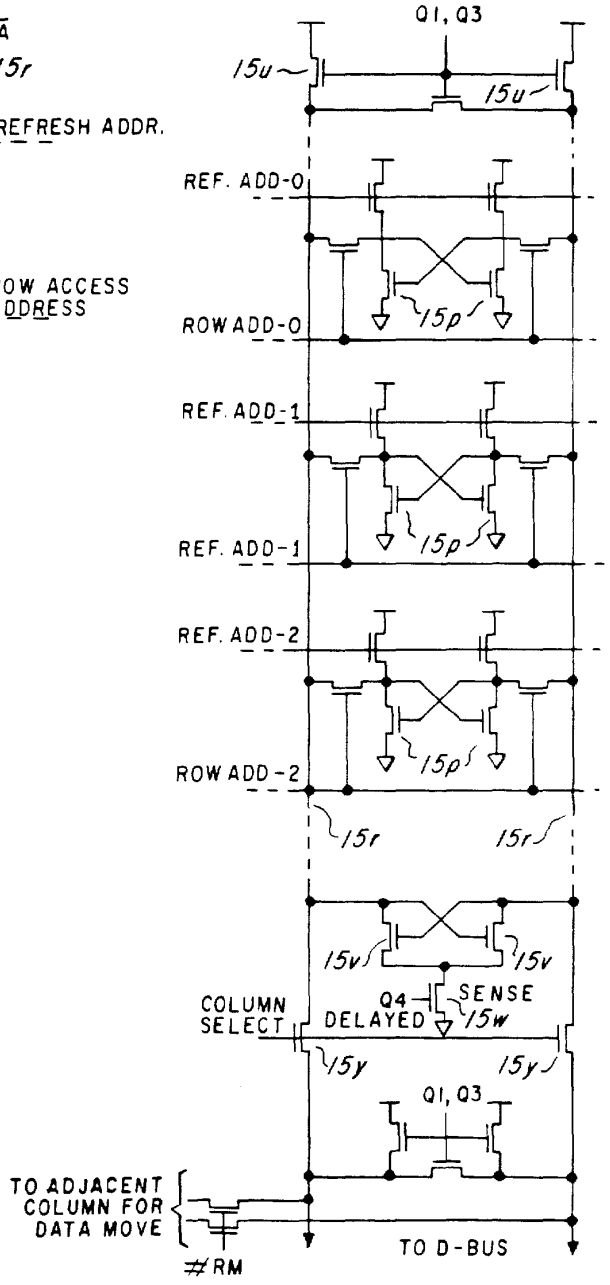

Q1, Q3
15u
15u
REF. ADD-0
15p
ROW ADD-0
REF. ADD-1
15p
REF. ADD-1
REF. ADD-2
15p
ROW ADD-2
15r
15r
15v
15v
COLUMN SELECT
Q4
SENSE
DELAYED
15w
15y
15y
Q1, Q3
TO ADJACENT COLUMN FOR DATA MOVE
TO D-BUS
#RM

Fig. 5h

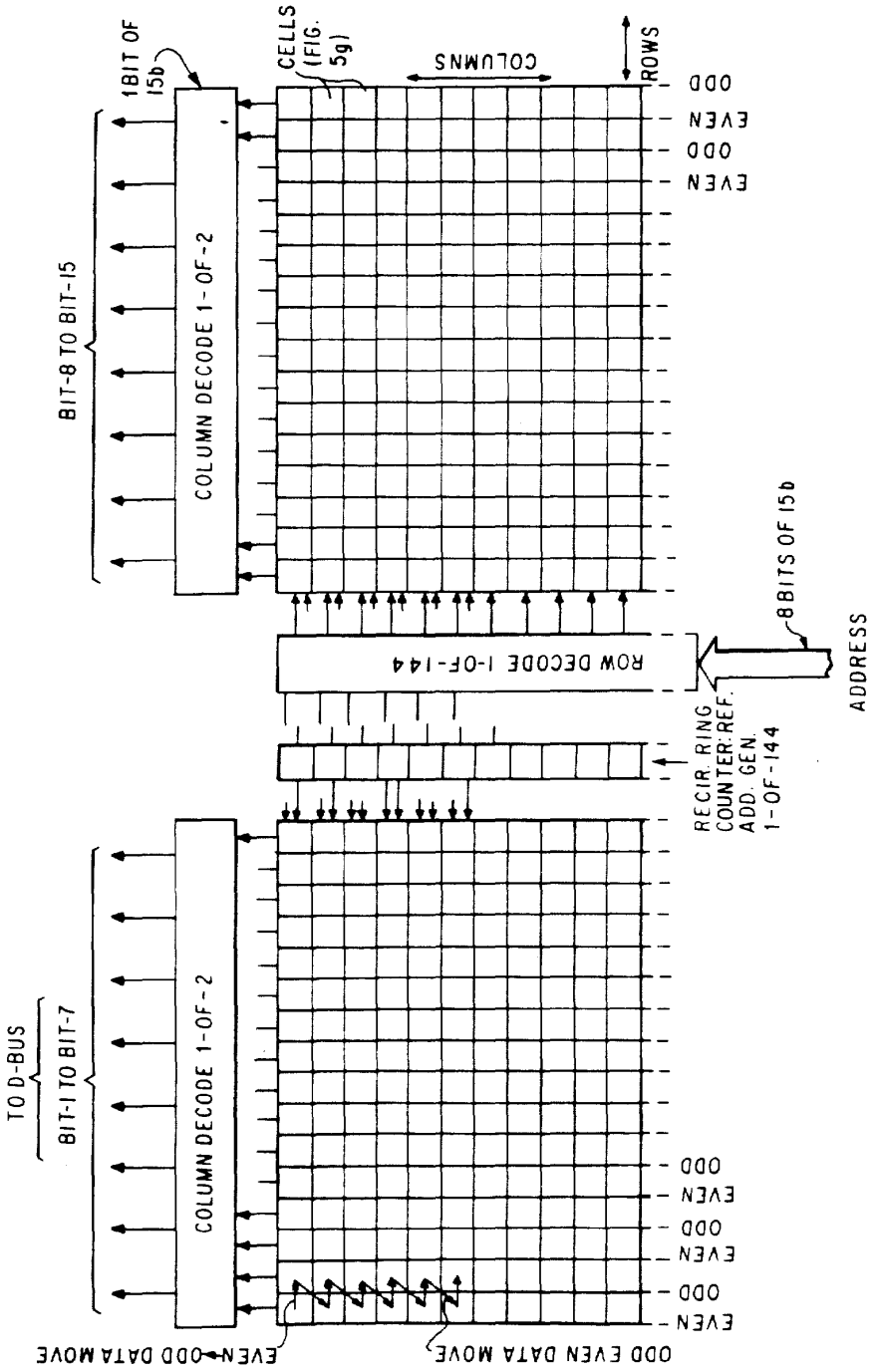

1BIT OF 15b
CELLS (FIG. 5g)
COLUMNS
ROWS
ODD
EVEN
ODD
EVEN
BIT-8 TO BIT-15
COLUMN DECODE 1-OF-2
8 BITS OF 15b
ROW DECODE 1-OF-144
ADDRESS
RECIR. RING COUNTER REF. ADD. GEN. 1-OF-144
TO D-BUS
BIT-1 TO BIT-7
COLUMN DECODE 1-OF-2
ODD
EVEN
ODD
EVEN
ODD
EVEN
EVEN-ODD DATA MOVE
ODD EVEN DATA MOVE

Fig. 5i

MICROCOMPUTER WITH BUS INTERCHANGE MODULE

This is a continuation of application Ser. No. 347,860, filed Feb. 11, 1982.

BACKGROUND OF THE INVENTION

This invention relates to integrated semiconductor devices and systems, and more particularly to a high-speed, miniaturized, electronic digital signal processing system in single-chip microcomputer form.

A microprocessor device is a central processing unit or CPU for a digital processor which is usually contained in a single semiconductor integrated circuit or "chip" fabricated by "MOS/LSI" technology, as shown in U.S. Pat. No. 3,757,306 issued to Gary W. Boone and assigned to Texas Instruments. The Boone patent shows a single-chip 8-bit CPU including a parallel ALU, registers for data and addresses, an instruction register and a control decoder, all interconnected using the Von Neuman architecture and employing a bidirectional parallel bus for data, address and instructions. U.S. Pat. No. 4,074,351, issued to Gary W. Boone and Michael J. Cochran, assigned to Texas Instruments, shows a single-chip "microcomputer" type device which contains a 4-bit parallel ALU and its control circuitry, with on-chip ROM for program storage and on-chip RAM for data storage, constructed in the Harvard architecture. The term microprocessor usually refers to a device employing external memory for program and data storage, while the term microcomputer refers to a device with on-chip ROM and RAM for program and data storage; the terms are also used interchangably, however, and are not intended as restrictive as to this invention.

Subsequent to 1971 when U.S. Pat. Nos. 3,757,306 and 4,074,351 were originally filed, many improvements have been made in microprocessors and microcomputers to increase the speed and capability of these devices and reduce the cost of manufacture, providing more circuitry and functions in less space, i.e., smaller chip size. Improved VLSI semiconductor processing and photolithographic techniques allow narrower line widths and higher resolution, providing added circuit density and higher speed, but circuit and system improvements also contribute to the goals of increased performance with smaller chip size. Some of these improvements in microcomputers are disclosed in the following U.S. Patents, all assigned to Texas Instruments: U.S. Pat. No. 3,991,305 issued to Edward R. Caudel and Joseph H. Raymond Jr.; U.S. Pat. No. 4,156,927 issued to David J. McElroy and Graham S. Tubbs; U.S. Pat. No. 3,934,233 issued to R. J. Fisher and G. D. Rogers; U.S. Pat. No. 3,921,142 issued to J. D. Bryant and G. A. Hartsell; U.S. Pat. No. 3,900,722 issued to M. J. Cochran and C. P. Grant; U.S. Pat. No. 3,932,846 issued to C. W. Brixely et al; U.S. Pat. No. 3,939,335 issued to G. L. Brantingham, L. H. Phillips and L. T. Novak; U.S. Pat. No. 4,125,901 issued to S. P. Hamilton, L. L. Miles, et al; U.S. Pat. No. 4,158,432 issued to M. G. VanBavel; U.S. Pat. No. 3,757,308 and U.S. Pat. No. 3,984,816. The devices described in these patents have been of the Harvard architecture and of the 4-bit type, particularly adapted for calculator or controller applications.

Additional examples of microprocessor and microcomputer devices in the evolutation of this technology are described in publications. In Electronics, Sept. 25, 1972, pp. 31–32, a 4-bit P-channel MOS microcomputer with on-chip ROM and RAM is shown which is similar to U.S. Pat. No. 3,991,305. Two of the most widely used 8-bit microprocessors like that of U.S. Pat. No. 3,757,306 are described in Electronics, Apr. 18, 1974 at pp. 88–95 (the Motorola 6800) and pp. 95–100 (the Intel 8080). A microcomputer version of the 6800 is described in Electronics, Feb. 2, 1978 at pp. 95–103. Likewise, a single-chip microcomputer version of the 8080 is shown in Electronics, Nov. 25, 1976 at pp. 99–105. Another single-chip microcomputer, the Mostek 3872, is shown in Electronics, May 11, 1978, at p. 105–110 and an improved version of the 6800 is disclosed in ELectronics, Sept. 17, 1979 at pp. 122–125. Sixteen-bit microprocessors based on minicomputer instruction sets evolved such as the part number TMS9900 described in a book entitled "9900 Family Systems Design", published in 1978 by Texas Instruments Incorporated, P.O. Box 1443, M/S 6404, Houston, Tex. 77001, Library of Congress Catalog No. 78-058005. The 8086, a 16-bit microprocessor evolving from the 8080, is described in Electronics, Feb. 16, 1978, pp. 99–104, while a 16-bit microprocessor identified as the 68000 (based on the 6800) is described in Electronic Design, Sept. 1, 1978 at pp. 100–107, and in IEEE Computer, Vol. 12. No. 2, pp. 43–52 (1979).

These prior 8-bit and 16-bit microprocessors and microcomputers have been general-purpose processors of the Von Neuman architecture with multiplexed address/data busses, and usually have been microcoded as described in U.S. patent application Ser. No. 209,915, filed Nov. 24, 1980 by Guttag, McDonough and Laws (now U.S. Pat. No. 4,402,043, or Ser. No. 253,624, filed Apr. 13, 1981, by Hayn, McDonough and Bellay, both assigned to Texas Instruments, and at pp. 28–34, IEEE Spectrum, March 1979, by McKevitt and Bayliss, or Proceedings 11th Annual Microprogramming Workshop, December, 1979 by Stintter and Tredenick. Microcoding, originally described by Wilkes in 1951, employs a control ROM to store microinstruction sequences entered by instruction words; the programmer works in a higher level machine code, so the number of assembly language code statements is supposedly reduced, and thus programming cost is reduced.

In contrast, a special-purpose high-speed microcomputer device according to the embodiment of the invention described herein departs from these contemporary microprocessor devices in several major respects in order to achieve substantial speed and performance advantages. This device is a non-microcoded processor of modified Harvard architecture.

It is the principal object of this invention to provide improved features of a microcomputer device and system, particularly one adapted for real-time digital signal processing. Another object is to provide a high-speed microcomputer of enhanced capabilities.

SUMMARY OF THE INVENTION

In accordance with one embodiment, features of the invention are included in a system for real-time digital signal processing employing a single-chip microcomputer device having separate on-chip program ROM and data RAM, with separate address and data paths for program and data. An external program address bus allows off-chip program fetch in an expansion mode, with the opcode returned by an external data bus. A bus interchange module allows transfer between the sepa-

rate internal program and data busses in special circumstances. The internal busses are 16-bit, while the ALU and accumulator are 32-bit. A multiplier circuit produces a single state 16×16 multiply function separate from the ALU, with 32-bit output to the ALU. One input to the ALU passes through a 0-to-15 bit shifter with sign extension.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as other features and advantages thereof, will be best understood by reference to the detailed description which follows, read in conjunction with the accompanying drawings, wherein;

FIG. **1** is an electrical diagram in block form of a microcomputer system employing features of the invention;

FIG. **2** is an electrical diagram in block form of an MOS/LSI microcomputer device (including a CPU or central processor unit) employed in the system of FIG. **1** and utilizing features of the invention;

FIGS. **3***a*–**3***mm* are timing diagrams showing voltage or event vs. time in the operation of the microcomputer of FIG. **2**;

FIGS. **4** and **4***a* are greatly enlarged plan views of a semiconductor chip containing the microcomputer of FIG. **2**, showing the physical layout of the various parts of the device;

FIGS. **5***a*–**5***i* are electrical schematic diagram of particular circuits in the microcomputer device of FIG. **2**.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENT

Microprocessor System

The microcomputer device to be described herein is primarily used for signal processing, but concepts thereof may be used in processor devices of various configurations, and these devices may be used in many different systems; in one embodiment the microcomputer is used in a system shown in generalized form in FIG. **1**. The system may be, for example, a voice communication system, a speech analysis system, a small "personal" or "home" computer, a single-board general purpose microcomputer, a word processing system, a computer terminal having local processing capability with display and typewriter keyboard, or any one of many applications of various types. The system includes a single-chip MOS/LSI central processing unit or microcomputer **10** which will be described in detail, along with a program or data memory **11** and input/output or I/O devices **12**. Usually the I/O devices **12** for the typical system include analog-to-digital and/or digital-to-analog converters, a modem, a keyboard, a CRT display, a disc drive, etc. Often the I/O **12** includes coupling to a general purpose processor; that is the microcomputer **10** is an attached processor in a larger system with interface via the I/O **12**. The microcomputer **10**, program data memory **11** and I/O **12** communicate with one another by two multibit, parallel address and data busses, D and RA, along with a control bus **13**. The microcomputer **10** has suitable supply voltage and crystal-input terminals; for example, the device employs a single +5 V Vcc supply and ground or Vss, and a crystal is connected to terminals X**1** and X**2** of the device **10** to control certain system timing. The microcomputer **10** is a very high speed device with a crystal input of 20 MHZ, providing an instruction execution rate of five million per second, in one embodiment.

The microcomputer device **10** is a general purpose microcomputer specifically aimed at serving a large class of serial signal processing problems such as digital filtering, signal handling for telecommunications modems (modulation, demodulation), data compression for linear predictive code (LPC) speech signals, fast Fourier transforms, and in general for virtually all computation intensive analog system functions, including detection, signal generation, mixing, phase tracking, angle measurement, feedback control, clock recovery, correlation, convolution, etc. It is suitable for applications which have computational requirements similar to those for control and signal processing, such as coordinate transformation, solution of linear differential equations with constant coefficients, averaging, etc. The device **10** is usually interfaced via I/O **12** to a general purpose processor such as a 99000, an 8600 or a 68000, to construct processing systems as will be explained.

It is understood that, even though described in the context of a microcomputer in the preferred embodiment, with an on-chip program ROM **14** and data RAM **15**, nevertheless, some concepts of the invention may be used in a single-chip microprocessor with all off-chip program memory and/or data memory instead of the on-chip memory illustrated. Indeed, modes of operation are provided which disable the on-chip memory. Also, a microcomputer is shown having two separate external program address and data busses instead of the multiplexed, bidirectional busses which are now common, but some features herein disclosed are applicable where busses are multiplexed. The advantage of separating the busses and separating program and data memory space is speed.

In general terms, the system of FIG. **1** functions in the following manner: the microcomputer **10** fetches an instruction word internally by accessing the ROM **14** or externally by sending out an address on the ROM address bus RA to the memory **11** (and RCLK-on control bus **13**). If external, the instruction word is received back via the data bus D from the addressed location in the memory **11**. This instruction is executed in the next machine cycle (of length of 200 ns defined by a 20 MHz clock or crystal X**1**, X**2**) while a new instruction is being fetched; execution of an instruction may include accessing the on-chip RAM **15** for an operand, or writing a result into data RAM **15**, and an arithmetic or logic operation in ALU.

In the example to be described in detail, a 12-bit instruction address applied internally to ROM **14** or externally to the RA bus directly addresses 2^{12} or 4K words of program instruction or constants in ROM **14** and memory **11**. When reading from memory **11**, a DEN– (data bus enable bar) command is asserted on control bus **13**. It is also possible to write into the memory **11**, and for this purpose a WE– (write enable bar) command is asserted by the device **10** on one of the control bus lines **13**; the memory **11** may contain read/write memory devices in some or all of the address space, so the WE– command permits a write function.

The I/O devices **12** are addressed as ports; this interface to external devices **12** is accomplished using the address and data busses RA and D and control bus **13**, but the I/O devices **12** do not occupy locations in the logical address space like the memory **11**. This is in contrast to conventional memory-mapped I/O.

Data input/output via I/O or peripherals **12** employs a 3-bit field from the bus RA to select one of eight 16-bit ports in peripheral circuitry **12**. The selected 16-bit port is then accessed for read or write via the bus D. This operation uses one of the two instructions IN or OUT, on the control bus **13**, WE− is active for write or OUT, or DEN− is active for read or IN. A ROM clock RCLK− is active on control bus **13** on every machine cycle except when either DEN− or WE− is active; that is, the memory **11** is activated by RCLK− for possible instruction word access from off-chip in each machine cycle, but if accessing peripheral **12** using DEN− or WE− then the RCLK− does not occur.

A reset signal RS− on the control bus **13** clears the program counter and address bus RA (resets to zero), sets the data bus D in a high impedance state, and the memory controls DEN−, WE− and RCLK− in an inactive (high) state. All address and temporary data registers within the microcomputer **10** are cleared by a reset routine in the ROM **14**, but the internal RAM is not cleared. In this manner, the peripheral circuitry **12** (such as a main processor) can assert control, or initiate a start-up or power-on sequence.

An interrupt signal INT− on the control bus **13** causes the microcomputer **10** to halt execution (saving the current ROM address) and go to an interrupt vector address, unless interrupts are masked by the program.

The ME/SE− line in the control bus **13** defines the memory expansion mode or systems emulator mode for the microcomputer **10**. When this pin is held high (at +Vcc), the microcomputer executes from on-chip ROM and off-chip memory **11**, but when low (Vss) the chip is in the systems emulator mode and execution is only from the memory **11** which is PROM, EPROM or RAM so the program can be easily changed.

The Microcomputer Chip

The internal architecture of the microcomputer **10** is shown in a detailed block diagram in FIG. **2**. This device is a single-chip semiconductor integrated circuit mounted in a standard dual-in-line package or a chip carrier. Sixteen pins or terminals of the package are needed for the 16-bit data bus D, twelve to sixteen are used for the address bus RA (depending upon memory size) and the remaining terminals are used for the power supply Vcc and Vss, the crystal X1, X2, and the control bus **13**.

In addition to the program and data memory **14** and **15**, the microcomputer **10** contains a central processing unit or CPU for the system of FIG. **1**, and this CPU includes a 32-bit arithmetic logic unit or ALU, a 32-bit accumulator Acc to hold operands and results, multiplier M separate from the ALU, a shifter S which is one input to the ALU, status or flag decode SD, and an instruction decoder ID1 which receives part of the current instruction word and generates the control bits for the CPU and data memory portions of the device **10**.

The program memory **14** has associated with it a program counter PC to hold the instruction address used to access the ROM **14** or sent out on bus RA to the memory **11**, an instruction register IR to receive the instruction word from ROM **14**, a stack ST to save program memory addresses, and an instruction decoder ID2 which receives part of the current instruction word and generates control bits for the program memory portion of the microcomputer.

Associated with the data memory **15** are two auxiliary address registers AR0 and AR1 for the data memory **15**, a page register ARP to select between the registers AR0 and AR1 as the data memory address, and a data page buffer DP to hold certain bits of the data memory address.

The CPU is oriented around two internal busses, a 12-bit program bus (P-Bus) and a 16-bit data bus (D-Bus). Program access and data access can thus occur simultaneously, and the address spaces are separate. A bus interchange module BIM permits loading the program counter PC from Acc, for example, or accessing ROM **14** for constants via P-Bus, BIM and D-Bus.

The two major requirements for a signal processing microcomputer are high speed arithmetic and flexibility. Performance is achieved by using separate, principally on-chip program and data memories **14** and **15**, a large single accumulator Acc and a parallel multiplier M. A special purpose operation, data move, is defined within the data memory **15** which further enhances the performance in convolution operations. Flexibility has been achieved by defining an instruction set as will be described with reference to Table A, incorporating memory expansion and a single lever of interrupt.

The device can be configured with, for example, less than 2K or 2^{11} words of on-chip program memory **14** and the architecture allows for memory expansion up to 4K or 2^{12} words by the addition of external program memory in the memory **11**. In addition, a separate mode allows the device **10** to be configured as a system emulation device; in this "system emulator" mode, the entire 4K memory space is external and the ROM **14** is not used.

The CPU

The arithmetic logic unit or ALU consists of thirty-two parallel stages, each separate stage performing an arithmetic or logic function on its two input bits and producing a one-bit output and carry/borrow. The ALU has two 32-bit data inputs ALU-a and ALU-b, and a 32-bit data output ALU-o to accumulator Acc. The ALU-a input is always from the accumulator Acc and the ALU-b input is always either from the shifter S or from a 32-bit product register P in the multiplier M. The particular function performed on data passing through the ALU is defined by the current instruction word in IR which is applied by the program bus P-Bus to an instruction decoder ID1. The source of the ALU-b input is defined by an input select circuit ALU-s which selects from these two alternatives, based upon the contents of the current instruction word, i.e., the outputs #C of the decoder ID1. The shifter S receives a 16-bit input Si from D-Bus and produces a 32-bit output So which is the input Si shifted from zero to fifteen places to the left. Left-shifted data is zero-filled, i.e., all right-hand bit positions are filled with zeros when data is shifted out to the left. A unique feature is that the high-order bit is sign extended during shift operations. The ALU operates in twos-complement. The shifter S includes a shift control Sc loaded with a four-bit value from P-Bus via lines Sp so an arithmetic instruction can directly define the number of bits shifted in the path from D-Bus to the ALU-b input.

In this description, the LSB is considered to be on the right and the MSB on the left, so left-shift is toward more significant bits. Bit-0 is the MSB and bit-**15** is the LSB. Data is always in signed 2's complement in this architecture.

The multiplier M is a 16×16 multiplier using carry feed-forward, constructed in partly dynamic and partly

static logic, to implement Booth's algorithm. One input to the multiplier M is the T register which is a 16-bit register for temporary storage of the multiplicand received from D-Bus via lines Ti. The other 16-bit input is via lines Mi from the D-Bus; this multiplier input may be from the data memory **15** or may be a 13-bit multiply-immediate value derived directly from the instruction word (loaded right-justified and sign-extended).

The ALU always receives the contents of the accumulator Acc as its ALU-a input, and always stores its output in Acc, i.e., Acc is always the destination and the primary operand. The unit will add, subtract and perform the logic operations of And, Or and Exclusive Or. The logic operation results are between the lower half of Acc (bits **16–31**) and a 16-bit value from the data memory **15**. Due to passing the data memory value through the shifter S (with zero shift), the operand for the logical operation result of the MSBs (bits **0–15**) is zero. The final 32-bit result reaching the accumulator is thus in two parts: Bits **0–15** will be Acc bits **0–15** Anded (or Or'ed, etc) with zero; bits **16–31** of the result will be Acc bits **16–31** Anded (etc.) with the data memory value. The accumulator Acc output, in addition to the 32-bit ALU-a input, includes high and low 16-bit outputs Acc-H (bits **0–15**) and Acc-L (bits **16–31**); separate instructions "store accumulator high" SACH and SACL "store accumulator low" are provided for storing high and low-order Acc bits in the data memory **15**.

The status decoder SD monitors the Acc whenever an instruction which updates Acc is executed. Four bits of SD are OV, L, G and Z. Accumulator overflow (or underflow) is indicated by the OV bit, Acc contents less than zero is indicated by the L bit, Acc greater than zero indicated by the G bit, and Acc equal zero indicated by the Z bit. Upon interrupt the OV bit is saved in an overflow flag register, but the other bits are available only up to the time the next accumulator instruction is executed.

The accumulator overflow mode is a single-bit mode register OVM (included in SD), directly under program control, to allow for saturated results in signal processing computations. When the overflow mode OVM is reset, overflow results are loaded via ALU-o into the accumulator Acc from the ALU without modification. When the overflow mode is set, overflow results are set to the largest, or smallest, representable value of the ALU and loaded into the accumulator Acc. The largest or smallest value is determined by the sign of the overflow bit. This allows a saturated Acc result in signal processing applications, modeling the saturation process of analog signals.

A separate status bit in SD monitors the condition of the currently used auxiliary register AR0 or AR1 and detects the all-zero condition of the least significant nine bits of the current auxiliary register (i.e. loop counter portion). This bit is used for a branch instruction conditioned on non-zero for the auxiliary register (BARNZ), "branch on auxiliary register non-zero."

The input/output status bit (I/O ST−) is an external pin which is part of the control bus **13** and provides "branch on I/O zero" instruction (BIOZ) to interrogate the condition of peripheral circuits **12**. A zero level on the I/O ST− pin will cause a branch when sampled by the BIOZ instruction.

The bus interchange module BIM exchanges the low-order twelve bits of the 16-bit value on the D-Bus with the twelve bits on the P-Bus. This operation is not available to the programmer as an instruction, but instead is needed as an inherent operation in instructions such as table look up (TBLR A).

PROGRAM MEMORY ADDRESSING

The program memory **14** is a ROM which is partitioned to produce a 16-bit output to instruction register IR, and this ROM employs a decoder **14***a* which selects one 16-bit instruction word based on an 11-bit or 12-bit address on input lines **14***b*. In the example embodiment, the ROM **14** contains less than 2K words, so an 11-bit address can be used, but the on-chip program memory could be expanded to 4K with a 12-bit address. The circuit of the ROM **14** is especially adapted for fast access as will be explained. The address input **14***b* is received from the program counter PC which is a 12-bit register containing the address of the instruction following the one being executed. That is, at the time when the control bits #C are valid at the outputs of the instruction decoders ID1 and ID2 for one instruction, PC contains the address of the next instruction; an address in PC goes into decoder **14***a* and the next instruction is read from ROM **14** into IR, and the program counter PC is incremented via PCinc in preparation for another instruction fetch. That is, PC is self incrementing under control of a #C control bit from ID2. The output PCo from the program counter PC is also applied via lines RApc and selector RAs (and output buffers not shown) to the external RA bus via output lines RAo and twelve output pins of the microcomputer device. The RA bus (RA0 through RA11) contains the PC output via RApc when the selector RAs is in one mode, or contains the input RAi when executing I/O instructions IN and OUT. Whenever the address in PC is above the highest address in ROM **14**, off-chip program addressing to memory **11** is assumed; however, the device is designed to operate principally with the on-chip ROM, so for many uses of the device off-chip fetches for program instructions would never be needed. The program counter PC may be loaded via input PCi and selector PCs from the P-Bus for branch or call instructions, or loaded from the accumulator Acc via Acc-L, D-Bus, BIM, P-Bus, PCp and PCi in a "call accumulator" CALLA instruction.

The register stack ST is used for saving the contents of PC during subroutine and interrupt calls. In the illustrated embodiment, the stack ST contains four 12-bit registers constructed as a first-in, last-out push-down stack, although a larger or smaller number of registers could be used. The current contents of PC are saved by "pushing" onto the top-of-stack register TOS via lines PCst. Succesive CALL instructions will keep pushing the current contents of PC onto TOS as the prior contents are shifted down, so up to four nested subroutines can be accomodated A subroutine is terminated by execution of a return instruction RET which "pops" the stack, returning the contents of TOS to PC via lines PCt, selector PCs and input PCi, allowing the program to continue from the point it had reached prior to the last call or interrupt. When TOS is popped, the addresses in lower registers of ST move up one position. Each subroutine, initiated by a call instruction or an interrupt, must be terminated by a RET instruction.

In an example embodiment, the ROM **14** contains 1536 words, so the remainder of the 4K program address space, 2560 words, is off-chip in the memory **11**. When the memory expansion control pin ME/SE− is high, at logic 1, the device interprets any program address in PC in the 0-to-1535 range as being an on-chip

address for the ROM **14**, and any address in the 1536–4095 range as being an off-chip address so that the PC contents are sent out via RApc and RAo to the RA bus. An output strobe RCLK− generated by the decoder ID2 for every machine state enables the external memory **11** (except when IN or OUT instructions are being executed). When off-chip program memory **11** is accessed, the instruction word read from memory **11** is applied to the external bus D and thus to the internal P-Bus via input/output control DC and lines Dp; this is a 16-bit instruction and, like the output of ROM **14** via IR, it is loaded into decoders ID1 and ID2 for execution, or loaded into PC via PCp, or otherwise used just as an on-chip instruction fetch.

When the ME/SE− pin is at zero the device enters the system emulator mode wherein the entire 4K program address space is off-chip, so all PC addresses are applied to the RA bus via RApc and RAo. This mode is necessary when a user is developing systems or programs, prior to arriving at a final version of code for the ROM **14**. That is, the microcomputer **10** can operate with no code permanently programmed into the ROM so that new programs (stored in RAM or EPROM in the memory **11**) can be tested and debugged, then when the final code is extablished the chips **10** are produced in large volume with this code mask-programmed into the ROM **14**.

In either mode, the first two program addresses 0000 and 0001 are used for the reset function. When the reset pin RS− is brought low, an address of all zeros is forced into the program counter PC, as will be explained. Also, the third address is reserved for an interrupt vector; when the INT− pin is brought low, an address of 0002 is forced into PC to begin an interrupt routine.

DATA MEMORY ADDRESSING

The data memory **15** in the example embodiment contains 144 16-bit words, and so an 8-bit address is needed on address input **15***a* to the RAM address decoder **15***b*. However, the RAM **15** may be constructed with up to 512 words, requiring a 9-bit address, so the addressing arrangement will be described in terms of address bits which are unused in some embodiments. Each 128 word block of the RAM **15** is considered to be a page, so a 7-bit address field in an instruction word from program memory **14** on P-Bus via input **15***c* is used to directly address up to 128 words of data memory **15**. Two auxiliary registers AR0 and AR1 are employed in the example embodiment; however, up to eight of these 16-bit registers may be used, with the particular one currently being used as the source of the address for the RAM **15** being defined by the auxiliary register pointer ARP. With two registers AR0 and AR1, the pointer ARP is only one bit, but for an embodiment with eight auxiliary registers the pointer ARP is a 3-bit register. The 16-bit auxiliary registers AR0 and AR1 are under control of store, load or modify auxiliary register instructions SAR, LAR, and MAR as will be described. Nine-bit addresses from the low-order parts of the auxiliary registers may be applied to the address input **15***a* via selector **15***d*, , lines **15***e*, selector **15***f*, and lines **15***g*. When one of the auxiliary registers is to be the source of the RAM address, the selector **15***d* uses the value on lines **15***e* as the address input **15***a*, whereas if the P-Bus is to be the source of the RAM address the selector **15***d* uses a 7-bit address from input **15***c* and a 1-bit (expandable to 3-bit or 4-bit) page address from the data page register DP. The selector **15***f* is controlled by the pointer ARP which is loaded from P-Bus as defined by an instruction. The auxiliary registers are used for indirect addressing wherein an instruction need not contain a complete address for RAM **15** but instead merely specifies that an auxiliary register is to be used for this address; such instructions can also specify increment or decrement for the auxiliary register selected, in which case the nine LSBs of AR0 or AR1 are changed by +1 or −1 via paths Inc. The auxiliary registers may be thus used as loop counters. The auxiliary registers are accessed by the D-Bus vis lines ARio so these registers may be used as miscellaneous working registers, or may be initially loaded to begin a loop count.

The data memory **15** is accessed via the D-Bus and an input/output circuit **15***i*, via lines **15***j*. Construction of the data memory is such that a data move wholly within the RAM **15** is permitted, according to an important feature of the microcomputer **10**. Under instruction control, the data at one address can be moved to the next higher location in one machine cycle without using the ALU or D-Bus. Thus during an add, for example, the accessed data can be also moved to the next higher address. INPUT/OUTPUT FUNCTIONS

Input and output of data from the microcomputer chip **10** uses the data bus D and two of the lines of the control bus **13**, these being data enable bar (DE−) and write enable bar (WE−). Two instructions, IN and OUT, are employed for the data input and output functions. The external data bus D is coupled to the internal data bus D-Bus by the input/output control and data buffers DC. The output buffers in D1 are tri-state, so the output to data bus D is always placed in a high impedence state except when IN or OUT is being executed; to this end, one of the controls #C from the instruction decode ID1 sets the output buffers in high impdence state whenever IN or OUT is not decoded. When the instruction IN is present, the control DC activates sixteen input buffers, so the external data bus D is coupled to the internal D-Bus via DC and lines Dd for data input. When the OUT instruction is decoded, a control #C from ID1 activates output buffers in DC so the internal D-Bus is coupled via Dd and DC to the external bus D.

Execution of an IN instruction will also generate a data enable DEN− strobe on line **13***a* from ID1, and will couple the D-Bus to the RAM **15** via **15***i* and **15***j*, so the data from external will be entered into on-chip data memory. The intended uses of the microcomputer as a signal processor require hundreds or thousands of accesses to RAM **15** for every off-chip reference. That is, a value will be fetched from off-chip then convolution or like operations performed using this new value and other data in the RAM **15**, so thousands of instruction executions will transpire before another off-chip reference is needed. For this reason, the architecture favors internal data manipulation over off-chip data access.

Execution of an OUT instruction causes generation of an off-chip write enable WE− strobe on line **13***b* from ID1 and outputs data from RAM **15** via **15***i* and **15***j*, D-Bus, lines Dd and buffer DC to the external bus D. Referring to FIG. **1**, this data may be written into one of the ports (selected by the 3-bit RAi value) in the peripherals **12**.

Implicit in both the IN and OUT instructions is a 3-bit port address on lines RAi from ID1. This address is multiplexed onto the three LSBs (RA9–RA11) of the external address bus RA via selector RAs. Up to eight

peripherals may thus be addressed. The remaining high order bits of the RA bus outputs are held at logic zero during these instructions.

THE INSTRUCTION SET

The microcomputer **10** of FIGS. **1** and **2** executes the instruction set of Table A. The Table shows in the first column in mneumonic or assembly language name of each instruction used in writing source code, followed in the second column by the object code in binary which is the form the code appears in the ROM **14** and in the instruction register IR. This binary code is decoded in ID1 and ID2 to generate all of the controls #C to execute the desired operation by accessing various busses and registers and setting the functions of the ALU. The Table also gives the number of cycles or machine states employed by the microcomputer in executing the instruction; note that all instructions except branches, calls, table look-up and input/output are executed in one state time. The microcomputer is not microcoded; the standard ALU instructions are executed in one state. The Table also shows the number of instruction words needed to execute each instruction; it is important to note that only branches and call direct require two instruction words. The right-hand column is a brief description of the operation for each instruction.

Most of the instructions of Table A show the low-order eight bits (bits **8–15**) as "IAAAAAAA", which is the direct or indirect RAM **15** address for one operand. If the "I" bit, bit-**8**, is 0, the direct addressing mode is used, so the "A" field of the instruction word, bits **9–15**, is employed as a direct address connected from IR through P-Bus, lines **15***c* and selector **15***d* to address input **15***a*. In this direct addressing mode, the auxiliary registers AR0–AR1 are not used.

For the instructions containing "IAAAAAA", the indirect addressing mode is specified by a 1 in the I field, bit-**8**, of these instructions. The input address on lines **15***a* for the RAM **15** will in this case be obtained from one of the auxiliary registers AR0 or AR1, and bit **15** will select which one. If bit-**15** is 0, AR0 is used; if bit-**15** is 1, AR1 is used. Thus bit-**15** coupled from IR via P-Bus controls the selector **15***f* (and can be loaded into the ARP register). Since the number of auxiliary registers is expandable to eight, bits **13–15** of these indirect-address instructions are reserved for use with a 3-bit selector **15***f* and ARP register to define one-of-eight in the indirect addressing mode. Bit-**10** to bit-**12** are controls in indirect addressing: bit-**10** causes the addressed auxiliary register to be incremented if 1, or no change if 0; bit-**11** causes the addressed AR to be decremented if 1 or no change if 0; bit-**12** if 0 causes bit-**15** to be loaded into ARP after execution of the current instruction, or if 1 leaves the ARP unchanged.

The shift code SSSS used in many instructions of Table A is a four-bit field loaded into shift control Sc via Sp to define the number of spaces (zero to fifteen) that the data coming from the RAM **15** via D-bus is left shifted as it passes through the shifter S on the way to the ALU-b input.

Although not material to the structure described herein, assembly language formats using the instruction set of Table A employ "A" to designate direct addressing and "@" to designate indirect. Thus, "ADD S,A" means add contents of memory location defined by the A field of the instruction word. "ADD A@" means add using contents of the data memory location addressed by the auxiliary register AR0 or AR1 selected by the existing contents of ARP. ADD S@+ means add using current contents of ARP to define AR then increment this auxiliary register for loop counting. ADD S@ is the same as previous except decrement by 1. ADD S@,AR is same as previous except ARP is loaded with the value of bit-**15** to define a new auxiliary register for subsequent operations.

The descriptions given in the right-hand column of Table A assume direct addressing. For indirect addressing, the above explanation applies.

The ADD instruction thus adds the 16-bit contents of RAM **15** (at location OAAAAAAA for direct, or the contents at the locations in RAM **15** selected by the chosen AR if indirect), shifted SSSS spaces left, to the 32-bit contents of the Acc, and stores the result in the Acc. ADDH does the same except only the high-order half of Acc is the source of one operand and destination of the result, and no shift is performed.

The subtract instructions SUB and SUBH subtract the addressed RAM **15** data from the accumulator and store the result in Acc, but are otherwise the same as add. The load instruction LAC loads Acc with the 16-bit data addressed by IAAAAAAA which is left-shifted by SSSS bits. Only ADD, SUB and LAC specify a shift.

There are four instructions associated with the auxiliary registers: SAR, LAR, LARK and MAR. Store auxiliary register SAR causes the contents of one of the auxiliary registers defined by RRR to be stored in the memory location IAAAAAAA; the load AR instruction LAR is the reverse of SAR. With the LARK instruction a constant K from IR (bits **8–15**) is loaded into the AR defined by RRR; this 8-bit constant K is right-justified and MSBs set to zero in the 16-bit auxiliary register. The modify auxiliary instruction MAR causes one auxiliary register to be modified by bits-**10** to **12** as above, but no add or memory **15** access is implemented. The MAR code is operative only in the indirect mode, I=1; in direct mode this instruction results in no-op.

The input/output instructions are written in assembly language as "IN PA, A" or "OUT PA, A", where PA is the 3-bit port address PPP output on bits **9–11** of the RA bus (generated from the decoder ID1 and coupled via lines RAi). IN enables DEN− and disables RCLK−, while OUT enables WE− and disables RCLK−. The peripheral devices **12** decode RA9--RA11 to select one of eight 16-bit ports or locations for read or write via the bus D. These instructions use two machine states so that the data input pins of bus D are free on the second state to allow external fetch of the next instruction from memory **11** instead of ROM **14**.

The store accumulator instructions SACL and SACH, written as "SACL X,A" in assembly, cause the low or high order bits of Acc to be left-shifted XXX places and stored in the data memory **15** at the location defined direct or indirect by IAAAAAAA. The X field is not fully implemented in the example embodiment; for SACL only X=0 is allowed and for SACH only X=0, X=1 and X=4 are allowed. This shift is implemented in the accumulator circuitry itself rather than in the shifter S.

The arithmetic and logic instructions without shift code are ADDH, ADDS, SUBH, SUBS, SUBC, ZALH, ZALS, EXOR, AND, OR and LACK. These are all written as ADDH A, for example, in assembly language. ADDH causes the 16-bit data from the defined location in RAM **15** to be added to the high-order

half of Acc and stored in the high-order half of Acc; actually the data from RAM **15** is left shifted sixteen bits in shifter S as it goes from D-Bus to the ALU-b input. The ADDS instruction means that the sign extension is suppressed in the shifter S; the data from RAM **15** defined by A is treated as a 16-bit positive number instead of a signed 2's complement integer. SUBH and SUBS correspond to ADDH and ADDS except subtract is performed in the ALU.

The conditional subtract instruction SUBC is used in divide operations. The contents of the defined location in RAM **15** are subtracted from the contents of Acc and left-shifted fifteen bits, producing an ALU output ALU-o which, if equal to zero is left-shifted by one bit and a +1 is added, with the result stored in Acc. If the ALU output is not equal to zero then it is left-shifted by one-bit and stored in Acc (the +1 is not added). SUBC is a two-cycle instruction that assumes the accumulator is not used in the following instruction. If the following operation involves Acc then a NO OP instruction should be inserted after SUBC.

The "xero accumulator load high" instruction ZALH fetches the 16-bit word at the addressed location in the RAM and loads it into the high-order half of Acc (bits **0–15**); the Acc has been zeroed, so the low-order bits **16–31** reamin zero. The shifter S is in the data path from D-Bus via ALU to Acc, so a 16-bit shift is performed in ZALH to move the data to the high-order half. The ZALS instruction fetches a word from RAM and loads it into the low-order half of the zeroed Acc, with sign extension suppressed in the shifter S.

The logic operations EXOR, AND and OR are performed in 32-bit format, even though the operand fetched is sixteen bits. For EXOR, the high-order half of Acc is Exclusive Or'ed with zeros, concatenated with Exclusive Or of the fetched data with the low-order half of Acc, both halves of the result being stored in Acc. The same applies to OR and AND.

The load accumulator instruction LACK causes an 8-bit constant contained in the eight LSB's of the instruction word to be loaded into the eight LSB's of Acc, right justified; the upper twenty-four bits of Acc are zeroed. To accomplish this operation, the instruction word on P-Bus from IR (after ID1 and ID2 are loaded, of course), is coupled to the D-Bus by BIM, and thence to the ALU-b via shifter S (with no shift). The ALU performs "pass ALU-b" or add zeros to b, leaving the constant in Acc.

The data shift or data move instruction DSHT causes the contents of the defined location in the RAM **15** to be moved to the defined location plus one. This is accomplished internal to the RAM **15** without using the ALU or data bus D-Bus. The operation cannot cross a page boundry, however.

The "load T" instructions are used to set up multiply operations. LT causes the T register to be loaded from RAM **15** with the value defined by IAAAAAAA. The "load T with data move" instruction LTD employs an operation like DSHT in the RAM; the T register is loaded with the contents of the RAM **15** location defined by IAAAAAAA, then this same value is shifted to location IAAAAAAA+1, and also the contents of Acc is added in ALU to the contents of the P register with the result going to Acc. The LTA instruction is the same as LTD but without data move; the T register is loaded from RAM **15** and the P register is added to Acc, with result to Acc.

The multiply instruction MPY causes the 16-bit contents of T register to be multiplied in multiplier M (not using ALU) by the value from RAM **15** on the input Mi from D-Bus, with the 32-bit result going to the P register. The "multiply constant" instruction MPYK causes the 16-bit contents of T register to be multiplied by a 13-bit constant C from the opcode in IR; the 32-bit result stays in P register. For MPYK, the constant is connected from IR to Mi via P-Bus, BIM and D-Bus.

The "load data page" instructions LDPK and LDP cause the data page register DP to be loaded with up to eight bits from the opcode itself or from the defined location in RAM **15**. In the embodiment shown, the DP register is only one bit, but in other embodiments with a larger RAM **15** the DP register contains up to eight bits. The page address remains the same until a new load page instruction occurs.

The load status and store status instructions LST and SST are used in call subroutine or interrupts to save the contents of the status circuits SD, or restore status SD. These instructions are used instead of hard wired circuits for performing this function.

The disable and enable interrupt instructions DINT and EINT are used to mask or unmask the interrupt capability, i.e., these instructions reset or set a latch which determines whether or not the microcomputer **10** responds to the INT− pin.

An absolute value instruction ABS functions to assure that the accumulator contains only an absolute valve, i.e., if Acc is less than zero, the absolute value of Acc is loaded into Acc, but if Acc is greater than zero there is no change. Similarly, the zero accumulator instruction ZAC clears Acc.

The overflow mode instructions RAMV and SAMV cause the overflow mode latch OVM in the status decode SD to be set to 1 or reset to 0. When set, the ALU output is set to its maximum or minimum before loading into Acc upon overflow. This simulates the effect of saturating an amplifier in an analog circuit, and is useful in signal processing.

Three P register instructions PAC, HPAC and SPAC are used in manipulating data after a multiply MPY or MPYK. PAC loads the accumulator with the contents of the P register by passing the 32-bit data through the ALU without performing any operation to modify the data; actually the ALU-a input is zeroed and an ADD is executed. The APAC instruction adds the contents of the P register to the contents of Acc, with the result going to Acc. Similarly, the SPAC subtracts the contents of P register from Acc, result to Acc.

The subroutine instructions are CALL, CALLA and RET. CALL is a two-word instruction; the first word is the opcode and the second is the absolute address of the first instruction in the subroutine. When CALL is decoded in ID2, PC is incremented to fetch the next instruction word which is the address, then the incremented contents of PC are pushed to stack ST. The subroutine ends in return RET which causes the address on TOS to be popped and loaded into PC. To save status, SST must be used before CALL, and LST inserted after RET. The CALLA instruction is unique for a Harvard architecture machine; this uses the contents of Acc as the subroutine address rather than using the next location addressed by PC+1. The low-order bits of Acc are transferred via Acc-L and BIM to the P-Bus and thus via PCp to the program counter PC. The incremented PC is saved in CALLA by pushing to ST just as in a CALL.

The table look up instructions TBLR and TBLW also employ the Acc as an address source. These instructions require three states to execute. The RAM **15** location defined by IAAAAAAA is transferred via D-Bus and BIM to P-Bus, and thus via PCp to PC, from whence this address is applied via RApc to the external RA bus, or to ROM **14**.

The branch instructions all require two words, the first being the opcode and the second at PC+1 being the address. The low-order bits **8–15** of the opcodes are unused. Unconditional branch B loads the word at PC+1 into PC as the next address. BARNZ is conditional upon whether or not a loop counter, one of the auxiliary registers defined by ARP, is not-zero. BV causes a branch if the overflow bit OV in the status decode SD is a 1. BIOZ causes a branch if the IO bit from I/O ST− is a 1 in the status decoder SD. The six instructions BLZ, BLEZ, BGZ, BGEZ, BNZ and BZ are all dependent upon the defined condition in SD reflecting the condition in Acc.

SYSTEM TIMING

Referring to FIGS. *3a–3ii*, the timing of the system of FIG. **1** and the CPU chip of FIG. **2** is illustrated in a sequence of voltage vs. time waveforms or event vs. time diagrams. The chip **10** includes a clock generator **17** which has two external pins X1 and X2 to which a crystal (or external generator) is connected. The basic crystal frequency is up to 20 MHz and is represented by a clock **0** of FIG. *3a*. This clock **0** has a period of 50 ns, minimum, and is used to generate four quarter-cycle clocks Q1, Q2, Q3 and Q4 seen in FIGS. *3b–3e*, providing the basic internal timing for the microcomputer chip **10**. A set of four quarter cycle clocks Q1 to Q4 defines one machine state time of 200 ns, minimum; the states are referred to as S0, S1, S2, in FIG. **3**. The clock generator **17** produces an output CLKOUT, FIG. *3f*, on one of the control bus lines **13**. CLKOUT has the same period as Q1, but 50% duty cycle and beginning at the midpoint of Q1. This output is used for timing or synchronizing external elements of the system of FIG. **1**.

Internally, the microcomputer **10** executes one instruction per state time for most types of instructions, so five million instructions per second are executed. Of course, some instructions such as input/output, branch, call or table look-up require two or three state times. Assuming a sequence of single-state instructions such as add, load, store, etc., a new address is loaded into PC during each Q3 as seen in FIG. *3g*, then the ROM **14** is addressed during Q4 and Q1 so an instruction word output is produced from IR onto P-Bus starting in the next Q2 and continuing through Q3, as seen in FIG. *3h*. The ROM **14** access time is thus about 100 ns. If an external instruction fetch from memory **11** is used, the same access time applies. The instruction decoders ID1 and ID2 receive the instruction word from P-Bus during Q3 as seen in FIG. *3i*, and most of the decoder outputs #C are valid during Q1, although some fast controls are available in Q4. For direct addressing of the RAM, the address on bit-9 to bit-15 of P-Bus is immediately gated into the RAM decoder **15***b* when P-Bus becomes valid, but in either direct or indirect the RAM address is valid by the beginning of Q3 as seen in FIG. *3j*. For RAM read, the data output via **15***j* to D-Bus is valid on Q4, FIG. *3j*, and this data passes through the shifter S, FIG. *3k*, and is available as an ALU input during Q1, FIG. *3l*. The ALU controls #C are valid in Q2 and ALU output ALU-o is available during Q3. The accumulator Acc is loaded from ALU in Q4, FIG. *3m*.

It is thus seen that an ADD instruction, for example, for which fetch began at Q3 of the S0 state in FIGS. *3a–3m*, will be completed, i.e., the result loaded into Acc, in Q4 of state S2. There is substantial overlap of instruction execution. A new instruction fetch begins during Q3 of each state time, so execution of two more instructions have begun before one is finished.

Not shown in FIGS. *3a–3m* is the write-RAM function. The RAM **15** is always written into during Q2. Addressing the RAM is always during Q3, however. Thus, an instruction such as "store accumulator low" SACL is illustrated in FIGS. *3n* and *3o*. The RAM address is received from the instruction register via P-Bus on Q3 of S1 (assuming the SACL instruction was fetched beginning at Q3 of S0), and the write will not occur until Q2 of state S2. During the read slot, Q4 of S1, a refresh occurs for the addressed row of the RAM, then the same address stays until Q2 of state S2 for the write. The D-Bus is loaded from Acc during this same Q2, see FIG. *3n*.

If the accumulator must perform the saturate function in the overflow mode, i.e., OVM set to **1**, this will be performed after the load accumulator function of FIGS. *3m*. That is, for the ADD instruction of FIGS. *3a–3m*, the Acc is saturated during Q1 if the next state S3, so that when the accumulator is accessed by the following instruction it will be available to load the D-Bus on Q2.

When an instruction uses the data move function within the RAM **15**, the move operation occurs during Q1 as illustrated in FIG. *3o*. Also, if the increment loop counter function is performed for the auxiliary registers AR0 or AR1, the increment (or decrement) is executed in Q1. The T register, auxiliary registers AR0 or AR1, ARP latch, DP register and stack ST registers are each loaded during Q2 of any state time if these functions are included in the current instruction.

The bus interchange module BIM always executes a transfer from D-Bus to P-Bus beginning in Q2, if this function is defined by the instruction. The transfer from P-Bus to D-Bus by BIM is begun during Q4. The D-Bus is precharged on Q3 of every cycle, so no data can carry over on D-Bus through Q3 of any state, nor can data be loaded to or from D-Bus during Q3.

The program counter PC is incremented by the PCinc path during Q3 of each state time. That is, the load PC function of FIG. *3g* is the incremented value just generated.

Execution of a branch instruction is illustrated in FIGS. *3p–3r*. If the instruction loaded into the decoders ID1 and ID2 during Q3 of state S0 is a branch, the status decode SD bits from the previous instruction are valid during Q1 of S1 so the decision of branch or not is made at this point. Meanwhile, of course, another instruction fetch has begun so if the branch condition is met the instruction delivered to P-Bus during Q2 of S1 is used as the next address; if the condition is not met, however, this instruction is discarded. Assuming the condition is met, the branch address is loaded from IR via P-Bus to PC during Q3 of S1, and the new instruction delivered to IR and P-Bus in Q2 of S2 then decoded and executed beginning at Q3 of S2, FIG. *3r*.

A CALL instruction is executed in the same time sequence as a branch, seen in FIGS. *3p–3r*, except no SD evaluation is needed, and PC+1 is pushed to stack ST during Q3 of S1.

A return instruction RET is a two cycle instruction as illustrated in FIGS. 3*s*–3*u*. If the instruction loaded into the decoders ID1 and ID2 during Q3 of state S0 is RET, the instruction fetch which began with PC+1 and load PC in Q3 of S) is discarded and a pop stack function is performed in Q3 of S1 so the next instruction fetch is to the return address. The instruction fetched during Q4 of S1 is then decoded and executed beginning at Q3 of S2.

Input (or output) instructions are executed in two cycles as illustrated in FIGS. 3*v*–3*x*. Assume the opcode loaded into the decoder ID2 in Q3 of S0 is IN. The instruction fetched beginning at Q3 of S0 is not used; execution is inhibited by the decode of IN. The contents of PC at Q3 of S1 are saved until Q3 of S2 for the next instruction fetch; that is, PC is recirculated back to PC by the increment path, but no increment is performed. The controls #C produced from decode of IN are available for two states. The RAM address is loaded from P-Bus on Q3 of S1, seen in FIG. 3*y*, and the data input reaches D-Bus on Q4 of S1 and is written into RAM 15 during Q2 of S2. The DEN− control is active from Q4 of S1 through Q2 of S2 for the IN function. An OUT instruction is executed like IN except the RAM 15 is read during Q4 of S1 and the WE− control is active instead of DEN−.

A table look up instruction is executed as shown in FIGS. 3*aa*–3*cc*. The TBLR opcode is decoded beginning at Q3 of S0 and causes the Acc to be loaded via D-Bus to BIM in Q2 of S1, then PC is loaded via P-Bus from BIM in Q3 of S1 so the content of Acc is used as the next instruction fetch address. Meanwhile, execution of the instruction fetched beginning at Q3 of S0 is inhibited by preventing a ROM read control #RR from loading IR with the ROM 14 output, at Q2 of S1. The incremented contents of PC from Q3 of S0 are pushed to ST during Q3 of S1, then popped at Q3 of S2 as the next instruction address. The data fetched from ROM 14 (or memory 11) using the address from Acc during Q4/S1 to Q1/S2 is loaded onto P-Bus during Q2 of S2 where it remains until Q4 of S2 at which time the BIM accepts the data from P-Bus and then transfers it to D-Bus on Q2 of S3, the next state. The destination address for RAM 15 loaded into decoder 15*b* from P-Bus by Q3 of S1 and remains for two states, so the RAM write occurring at Q2 of S3 will use the RAM address defined in the original TBLR opcode.

One of the problems inherent in manufacturing microcomputer devices is that of testing the parts to determine whether or not all of the elements are functional. In many microcomputers, the instruction words read from the internal ROM are not available on external busses and so the ROM cannot be checked in any way other than by executing all possible functions, which can be lengthy. The device of FIG. 2 allows the ROM 14 to be read out one word at a time using the interchange module as illustrated in FIGS. 3*ee*–3*hh*. A test mode, not part of the instruction set of Table A, is entered by holding the I/O ST− pin at above Vdd, for example 10V, and holding RS− low, producing an input to the decoders ID1 and ID2 causing a ROM output function in which the ROM 14 is accessed every cycle and PC incremented as seen in FIG. 3*ee*. The P-Bus receives the ROM output, FIG. 3*ff*, but the opcodes are not loaded into the decoders ID1, ID2. Instead, the BIM accepts the opcodes from P-Bus on Q4 of each cycle and transfers to D-Bus on the next Q2, as seen in FIG. 3*hh*.

THE CHIP LAYOUT

In FIG. 4, the microcomputer 10 of FIGS. 1 and 2 is illustrated in chip layout form. This is a top view of an MOS/LSI chip which is about 150 mils on a side. A major part of the area of the chip 10 is occupied by the memory including the ROM 14 and RAM 15 with their address decoders, and by the 16×16 multiplier M. The ROM 14 has associated with it an X address decoder 14X and a separate Y address decoder 14*y* for instruction word output; twelve address bits are used to define one of up to 4096 16-bit words in the ROM 14, although in this example only 1536 are on-chip.

The RAM 15 has an X address decoder 15*b*–*x* which selects 1-of-72 row lines, and a Y address decoder 15*b*–*y* and sense amplifiers 15*s* which select 1-of-2 column lines, so only eight bits are needed for the RAM select in this embodiment (eight bits could accomodate a 256 byte RAM).

The busses RA and D have twelve or sixteen bonding pads on the chip (total of twenty-eight) for connection to external, and the areas of the chip around these bonding pads seen in FIG. 4 are occupied by the buffers used for the ports. It will be noted that the RA bus is only used for output, so only output buffers are needed for this port, while the D-Bus requires tri-state output buffers as well as input buffers.

The multiplier M, shifter S, ALU, accumulator Acc and auxiliary registers AR0, AR1 on the chip 10 of FIG. 4 comprise a 32-bit wide "strip" which is an array of rows (parallel to control lines #C) and columns (parallel to metal bus lines such as D-Bus and P-Bus and ALU and register bits) containing all of the 16-bit and 32-bit registers, ALU bits, and the like circuitry associated with the D-Bus and related control lines #C. As set forth in U.S. Pat. No. 4,402,044 issued to McDonough and Guttag, assigned to Texas Instruments, an important feature is that the 32-bit ALU and its associated 32-bit Acc registers, the two 16-bit AR registers, the shifter S, and the bus interchange BIM as described above are laid out on the MOS/LSI chip 10 in a regular strip pattern as seen in FIG. 4. Other circuitry connected to the D-Bus and the ALU-b input and having controls #C shared by sixteen or thirty-two bits may also be in the strip, such as AR and BIM. The Acc and the ALU each contain thirty-two bits or stages which are laid out in a regular pattern like memory cells, the bits arrayed and aligned horizontally and vertically as seen in FIG. 4. D-Bus and P-Bus of FIG. 2 are each sixteen parallel metal strips on top of the cells of the ALU and registers, and all of the dozens of control lines #C are horizontal polysilicon lines typically used as the control gates for transistors in the ALU and its associated registers and like circuitry. This layout arrangement is advantageous because the multiplier ALU and registers, and perpendicular control lines #C and metal busses fit in an array with virtually none of the wasted space used merely for routing conductors in conventional contruction of microprocessors. Metal bus lines such as P-Bus and D-Bus and control lines #C are in large part routed over functional regions or cells of the chip in the strip rather than over unused silicon, and many 90 degree turns are produced inherently at functional cells rather than in conductor routing. In the prior devices, the controls, the registers, the ALU, etc. where islands of circuitry connected by busses or conductors. The enlarged view of FIG. 4*a* shows a small part of the strip, two-bits wide, illustrating the metal bus

lines and the polysilicon control lines #C for an N-channel silicon gate MOS device made generally by a single-level polysilicon process according to U.S. Pat. No. 4,055,444, assigned to Texas Instruments. Various contacts (not shown) would be made within each register bit or stage from metal to silicon or to polysilicon. It is significant to note that many of the connecting lines from registers to busses illustrated in FIG. 2 are not physically lines or elongated conductors at all but instead are merely metal-to-silicon or metal-to-poly contact areas along the metal bus lines of FIG. 4*a*. That is, routing of 16-bit or 32-bit sets of parallel conductors is minimized by the strip feature, and the size of the chip 10 is reduced. All busses are not needed in any one part of the strip, and thus the pitch or maximum width of cells of the strip is minimized since the the metal-to-metal spacing is a critical limiting factor in bit density.

The internal program of the microcomputer 10 may be modified at the gate level mask in making the chip. The macro code or program in the ROM 14 is defined by a single mask in the manufacturing process as set forth for example in U.S. Pat. Nos. 3,541,543, 4,208,726 or 4,230,504, assigned to Texas Instruments. By rewriting this user or macrocode, keeping the instruction set defined by ID1 and ID2 the same, a wide variety of different functions and operations are available.

ARITHMETIC LOGIC UNIT

A detailed schematic diagram of one bit of the 32-bit ALU is shown in FIG. 5*a*. The ALU operates under control of six of the #C commands from the instruction decode ID1, these commands being labelled #AUM-0–#AUM4 (valid on Q2) and #AUAB (valid on Q1). The ALU-a input, inverted, is on line AUa and the ALU-b input inverted, is on line AUb, both being valid on Q1, one from Acc and the other from the shifter S or P register. The ALU output is at line AUc, valid on Q4, representing one of the inverted 32-bit parallel output ALU-o to Acc. Table B shows the function produced by operation of the ALU for various combinations of the six #C commands. This ALU is generally the same as U.S. Pat. No. 4,422,143, issued to Karl M. Guttag, assigned to Texas Instruments. Propagate and generate nodes AUp and AUg are precharged on Q1 and conditionally discharged by transistors AUd controlled by the ALU-a input, transistor AUe controlled by the ALU-b input and its complement, and transistors AUf controlled by the #AUM0–#AUM3 commands, according to the functions of Table B. A carry-out node AUh and a carry-in node AUi for each bit are coupled by a propagate-carry transistor AUj controlled by a line AUk which is the propagate node AUp inverted. The carry-out node AUh is precharged on Q1 and conditionally discharged via transistor AUm which is controlled by a NOR gate having the generate node AUg as one input and the absolute value command #AUAB as the other, so if #AUAB is 1 the transistor AUm is off and carry-out bar is always 1, meaning no carry or absolute value. If #AUAB is 0, the generate signal on AUg controls. The inverted propagate signal on AUk is one input to an Exclusive Nor circuit AUn with static load AUq; the inverted carry-in bar of line AUi is the other input to the Exclusive NOR, resulting in an output AUr which inverted is the ALU output AUc. The carry-in bar node AUi is made unconditionally 0 when control #AUM4 is high for logic functions OR, AND and EXOR, so this input to circuit AUn is unconditionally 1, but for ADD, SUB, etc., the control #AUM4 is 0 and the carry-in from the node AUu of the next low-order bit of the ALU controls.

THE SHIFTER S

Referring to FIG. 5*b*, the shifter S includes a 16-bit input Si, a shift matrix Sm, a shift controller Sc, and a 32-bit output So going to the ALU-b input. The input Si is connected to receive the D-Bus at all times and to drive lines Sf in the matrix Sm through high level buffers. If no shift is to be performed, a line Sg is high, turning on all sixteen of the transistors Sh for this line, so the 16-bit data on lines Sf will appear on the sixteen right-most output lines So via diagonal lines Sj. All of the lines Sf are precharged on Q3 via thirty-two transistors Sk then conditionally discharged by the input Si. The sign bit is extended by detecting the MSB bit-0 of the input Si by the line Sm. A gate Sn also receives a #NEX not extend command from ID1 (one of the controls #C) to kill the sign extension for certain instructions of Table A. Based on the incoming sign bit Sm and #NEX, the gate Sn generates an extend command on line Sq to transistors Sq'. The transistors Sq' in series with lines Sr conditionally discharge the nodes Ss on lines Sf through transistors St. The control Sc is a 1-of-16 decoder or selector which receives the bits 4–7 of the instruction word from the P-Bus on 4-bit input Sp during Q3 and activates one of the sixteen lines Su; the lines Su are precharged in Q3 via transistors Sup and conditionally discharged during Q4 via transistors Sud and Sc'. The controls for the shifter S consist of the 4-bit value on Sp (the SSSS field of the ADD instruction, for example) defining the number of positions of left shift, and controls on lines #C for negating sign extension, etc. Since the data is usually in two's complement, the sign bit is extended to all bits to the left of the most significant data bit. The sign bit is 0 for positive and 1 for negative. If the shift is to be seven bits, for example, the seventh line Su stays high on Q4 and all others go low. This turns on all transistors Sh and St in the seventh row and all other transistors Sh and St are off. The 16-bit data coming in on lines Si thus moved via transistors Sh and lines Sj to a position on lines So seven bits to the left of the zero shift (right-most) position, and zero-filled to the right due to the prcharge Sk. To the left, the sign bit will stay 0 is the bit-0 is low, but if bit-0 is 1 then Sq is high, transistors Sq are on, allowing all bits to the left to discharge.

BUS INTERCHANGE MODULE

The bus interchange module BIM, shown in detail in FIG. 5*c*, consists of sixteen identical stages, only one of which is illustrated. Each stage has two clocked inverters Ia, with no feedback loop since data is not held in BIM longer than about half a state time. Input node Ib is connected to the respective bit of P-Bus via one of sixteen transistors Ic driven by a control bit #BIFP valid on Q4. The D-Bus is connected to the input node Ib via transistors Id driven by the control bit #BIFD (Bus Interchange From D) from decoder ID1 valid on Q2. The output node Ie is connected to the P-Bus by a push-pull stage including transistors If and Ig, and a transistor Ih driven by a control bit #TP, valid during Q2 and Q3. Likewise, output node Ie is coupled to the D-Bus via a push-pull stage having driver transistors Ii and Ij, and a transistor Ik driven by a control bit #BITD valid on Q2 and Q4. The transistors Ig and Ij are driven by node Im at the output of the first inverter Ia, providing a push-pull output. Data is transferred

from D-Bus to nodes Ib, Im, Ie on Q2, and then from these nodes to P-Bus on Q4. Similarly, data is transferred from P-Bus to nodes Ib, Im, Ie on Q4, and then from these nodes to D-Bus on Q4 on the next Q2.

THE MULTIPLIER

Referring to FIG. 5*d*, a schematic representation of the multiplier M and its T and P registers is shown, and corresponding detailed circuit diagrams are shown in FIGS. 5*e*, 5*f*. The 16-bit output of the T register is applied to a set of eight Booth's decoders Mb which produce eight sets of outputs Mc, each set including five functions: shift or no shift, and add, subtract or zero. A set of eight banks of 17-it static carry-feed-forward adders Ma-1 to Ma-8 receive the Mc inputs when the T register is loaded, and so a significant part of the multiplication function is initiated before the MPY instruction is executed. The adders Ma-1 to Ma-8 are static in that no clock Q1–Q4 is needed to cause them to operate. Each stage of each level or bank includes a control section Mm responsive to the decoder outputs Me, and the control section feeds an adder. Level Ma-2 uses half adders and levels Mc-3 to Mc-8 use full adders. The first level Mc-1 does not need an adder because there is no partial product from the prior stage, so it has only the control section. When the MPY instruction is decoded, on Q4 the second operand is applied to the static adders from D-Bus by 16-bit input Mi. As each level of the eight levels of adders Ma-1 to Ma-8 calculates the sum, the partial product is fed forward via lines Mf to the next higher level, except for the two LSBs of each level which are fed to the dynamic adders Md via lines Me. When the static adder array settles, the 17-bit output Mg from the level Ma-8 plus the seven lower level 2-bit LSB outputs Me, is applied to a carry-ripple adder MD(31-stages) to perform the final carry evaluation, producing a 31-bit product in two's complement notation. The 31-bits are sign extended to obtain a 32-bit product in the product register P.

Booth's 2-bits algorithm reduces the number of adder stages to about half the number otherwise required. When performing multiply in the classic pencil and paper method, the right or LS digit of one operand is multiplied by the other operand to produce a partial product, then the next digit is multiplied to produce another partial product which is shifted one digit with respect to the first. Booth's algorithm gave a method of multiplying in binary which allowed two bits to be treated each time, instead of one. Thus, level Ma-1 multiplies the two LSBs of T reg times all bits of D-Bus, producing a partial product Me and Mf. The second level Ma-2 multiplies the next two bits of T reg to D-Bus, adds the partial product Mf from Ma-1, and generates a new partial product Mf and two more bits Me because this operation shifts two bits each level.

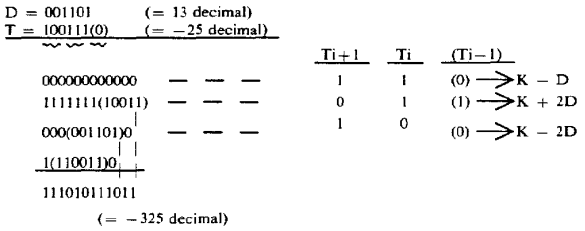
In FIG. 5*e*, one of the eight decoders Mb is shown, along with two bits of the T register. The T register stage consists of two inverters Ia with a recirculate transistor Rc clocked in Q4. The stage is loaded via transistor Ta by a #LT command from ID1 occurring on Q2 during an LT instruction. The outputs of two stages of the T register and complements are applied by lines To and Tc to one Booth decoder Mb. The decoder consists of four logic circuits, each having a static load Ba, Bb, Bc or Bd and a pattern of transistors Be with the lines To and Tc applied to the gates. Two of the terms have 1 or 0 fixed in the gates by lines Bf. Outputs Mc-1 and Mc-2 represent no-shift and shift commands and come from the logic stages Be and Bd. Outputs Mc-4 and Mc-5 are true and complement outputs from load Ba of the first of the logic circuits, and these represent add and subtract commands. The output Me-3 from Bb is the zero command.

The first level Ma-1 of the static adders is simpler than the higher levels in that only the D-Bus input Mi and the inputs Mc are involved, with no partial product. Two stages of this first level are seen in FIG. 5*g*, along with two of the seventeen stages of level Ma-2 and level Ma-3. The control sections Mm are all the same on all levels. Note that no elements are clocked.

The decoders Mb and control sections Mm with controls Mc define the Booth's two-bits at a time algorithm which reduces circuitry and increases speed by a factor of two. When two bits are interrogated successively, the only operations required are add, subtract, do nothing or shift by one bit. Considering the input from T as one operand, and from D-Bus as the other, the following table describes the function

Ti + 1	Ti	(Ti − 1)	Function	Partial Product
0	0	(0)	Do nothing	K + O
0	0	(1)	Add D	K + D
0	1	(0)	Add D	K + D
0	1	(1)	Shift D & Add	K + 2D
1	0	(0)	Shift D & Add	K − 2D
1	0	(1)	Subtract D	K − D
1	1	(0)	Subtract D	K − D
1	1	(1)	Do nothing	K + O

An example of multiplication using Booth's two bit algorithm is as follows:



In the control sections Mm the inputs Mi from the D-Bus are controlled by a transistor Mm-1 and control Mc-1, not shift. The Mi input for the adjacent bit is gated in by transistor Mm-2 and the Mc-2 shift command, providing the "2D" function as just described. The zero is provided by transistor Mm-3 and zero control Mc-3 which results in mode Mm-4 being connected to Vcc (zero in two's complement). The carry-in from

the prior stage is on line Mm-5, and the partial product from the prior stage is on line Mm-6. The add or subtract control is provided by transistors Mm-7 controlled by the Mc-4 and Mc-5 add and subtract commands. The full adder includes logic gate Mn-1 receiving the outputs of the control section, as well as gates Mn-2 and the exclusive Nor Mn-3, producing a sum on line Mn-4 and a carry on line Mn-5. Speed is increased by using carry feed forward instead of carry ripple on the same level. Level Ma-1 has no partial product or sum Mm-6 from the prior stage, nor carry-in Mn-5, so the adder is not needed, only the control, producing a sum (a difference) at mode Mn-8 and no carry. The second level Ma-2 is a half adder since no carry feed forward is received from Ma-1.

One of the adder stages of the 31-stage ripple-through carry adder is shown in FIG. 5*f*, along with one stage of the P register. The adder stage receives two inputs Me, gated on Q1 or Q3 by transistors Md1. The six LSBs of adder Md have their inputs gated in on Q1 because the static array levels Ma-1, Ma-2 and Ma-3 will have settled and outputs Me will be valid at this point, so the add and ripple through in Md can begin, although the outputs Mf are not yet valid. Thus, the more significant bits are gated on Q3 at transistors Md1. A carry input Md2 from the next lower-significant stage is applied to one input of an exclusive NOR circuit Md3, and to a carrry output gate Md4 which produces a carry output Md5 to the next higher stage. A propagate term is generated from the inputs Me and the carry-in by logic gate Md6, and a carry generate term by a logic gate Md7 with Md4. The same output Md8 is connected by line Md9 to the input of the P register stage, gated by #LPR (load P Reg) from ID1 on Q4 by transistor Pa. The P register stage consists of pair of inverters Ia and recirculate transistor Rc gated on Q2. The output is applied to the ALU-b input on Q1 by gate Pb with #NRPR (not read P Reg) from ID1 as one input, along with an inverter Pc. Transistor Pd precharges the ALU-b input on Q4.

The timing of the multiplier operation is illustrated in FIGS. 3*jj* to 3*mm*. On Q2 of So, the register is loaded and outputs Mc from the Booth's decoder become valid. The Mi inputs from D-Bus are valid at Q4 of S1, assuming the MPY instruction is valid in decoder ID1 at Q3 of S1. The lower bits of the dynamic adder Md are loaded with Me on Q1 of S2, via Md1, and the carry begins to ripple through the lower of the 31-bits, then this continues in Q3 of S2 through the output Mf of the upper levels, so P register is loaded on Q4 of S2 via Pa, where the data remains until loaded to ALU-b on Q1 of a succeeding cycle.

THE RAM

The cell used in the RAM 15 is a pseudo-static 6-transistor cell as seen in FIG. 5*g*. This cell differs from the traditional 6-transistor static cell in that refresh transistors 15*m* are used in place of polysilicon resisters or depletion transistors used as load impedences. The implanted resistors or depletion devices are larger and interpose process complexities. The storage nodes 15*n* are connected through cross-coupled driver transistors 15*p* to ground; one transistor 15*p* is on and the other off, storing a 1 or 0. Read or write is through access transistors 15*q* to data and data bar lines 15*r*, with gates of the transistors 15*q* driven by a row address line 15*s*. Refresh is accomplished when the refresh line 15*t* is pulsed high allowing the node 15*n* which is at 1 to be charged back up to a level near Vdd, while the 0 node 15*n* will conduct the pulse of current to ground through the on transistor 15*p*. The row address on 15*s* is delayed slightly from the refresh line 15*t* so that both won't begin at the same time. In the timing sequence of the FIGS. 3*a*–3*e*, particularly FIGS. 3*j* and 3*o*, the cell of FIG. 5*j* is read in Q4 of any cycle, or written into on Q2.

Referring to FIG. 5*k*, several of the cells of FIG. 5*g* are shown in a column. The data and data bar lines 15*r* are precharged to Vdd-Vt on Q1 and Q3 by transistors 15*u*. The refresh address on lines 15*t*-0, 15*t*-1 and 15*t*-2, etc., occur in sequence, one-at-a-time, generated by a ring counter; for example, if the RAM 15 is partitioned in 64 rows, then a 64 bit ring counter generates one refresh address bit each state time, refreshing the entire array once each 64 states. The refresh pulse occurs on a line 15*t* during Q3, while transistors 15*u* precharge and equallize the data and data bar lines. A row address on a line 15*s* might begin to come up to 1 during the later part of Q3 since read access is in Q4, so the sizes of the transistors are such that nodes 15*n* will not be both forced to Vdd-Vt when transistors 15*m* and 15*q* are all turned on. The on transistor in the pair 15*p* will hold the 0 node lower than the 1 node. After the refresh pulse on 15*t* goes low, for a cell addressed for both read and refresh in Q3, the delayed Q3 address line stays high momentarily to assure that the zero-going line 15*r* will discharge at least slightly through 15*q* and 15*p* for the 0 side. Then a bistable sense circuit including cross-coupled transistors 15*v* is activated by transistor 15*w* having Q4 on its gate (delayed slightly to make sure Q3 has gone to zero). This flips the data and data bar lines to full logic level, after which the column access transistors 15*y* are activated for the addressed column and data can be read out onto the D-bus. Internal shift is implemented by lines 15*x* connecting nodes 15*z* to adjacent column lines 15*r* via transistors 15*z* activated by a RAM move command #RM from decoder ID1, occuring on Q4. The data is held until Q2 of the next cycle (after Q1 precharge of all data and data bar lines 15*r*) before being applied to the adjacent column for this move operation. Meanwhile, the row address may be incremented by 1; i.e., the next higher line 15*t*-1, etc., goes high so on Q2 the data is written into the next higher location.

The sixteen bits of the RAM 15 are arranged as seen in FIG. 5*i*, with column lines (data and data bar lines) 15*r* running vertical and row lines 15*s* horizontal. The RAM is only 32-columns wide, so the column select 15*y* is merely one-of-two, even or odd. There are in this embodiment 144 row lines 15*s*. The LSB of the address 15*b* to the RAM is the column address, even or odd. To implement the data move operation, on even columns the LSB of the address buffer is complemented, but for odd columns the LSB of the address buffer is complemented and also the row decoder output on line 15*s* is incremented.

TABLE A

THE INSTRUCTION SET

Source Code	Object Code-Binary	No. of Cycles	No. of Words	DESCRIPTION
ADD	0000SSSSIAAAAAAA	1	1	Add word at RAM address A (shifted S places to left) to Acc; Result to Acc
SUB	0001SSSSIAAAAAAA	1	1	Subtract word at address A (shifted S places to left) from ACC; Result to Acc
LAC	0010SSSSIAAAAAAA	1	1	Load Acc with word at address A (shifted S places to left)
SAR	00110RRRIAAAAAAA	1	1	Store contents of Aux Reg number R at location defined by A
LAR	00111RRRIAAAAAAA	1	1	Load Aux Reg R with value at location A
IN	01000PPPIAAAAAAA	2	1	Input value on external data bus, store in A
OUT	01001PPPIAAAAAAA	2	1	Output value at address A to ext data bus
SACL	01010XXXIAAAAAAA	1	1	Store low order Acc bits in location A, shifted X places left
SACH	01011XXXIAAAAAAA	1	1	Store high order Acc bits in location A, shifted X places left
ADDH	01100000IAAAAAAA	1	1	Add value at address A to high order Acc bits; result to Acc; no shift
ADDS	01100001IAAAAAAA	1	1	Add Acc to value at address A sign extension suppressed
SUBH	01100010IAAAAAAA	1	1	Subtract value at address A from high order Acc bits; result to Acc; no shift
SUBS	01100011IAAAAAAA	1	1	Subtract with sign extension suppressed
SUBC	01100100IAAAAAAA	2	1	Conditional subtract for divide; left shift ALu output and conditional +1
ZALH	01100101IAAAAAAA	1	1	Zero Accumulator and Load High under half of Acc with addressed data
ZALS	01100110IAAAAAAA	1	1	Zero Accumlator and Load with sign Extension Suppressed
TBLR	01100111IAAAAAAA	3	1	Table Read; read data from program memory using Acc as address; store in RAM
MAR	01101000IAAAAAAA	1	1	Modify Auxiliary Registers
DSHT	01101001IAAAAAAA	1	1	Data Shift; value defined by A shifted to A+1
LT	01101010IAAAAAAA	1	1	Load T Reg with value defined by A
LTD	01101011IAAAAAAA	1	1	Load T Reg with value A; shift A to A+1; Acc+Preg Acc
LTA	01101100IAAAAAAA	1	1	Load T Reg with value defined by A; Acc+Preg Acc
MPY	01101101IAAAAAAA	1	1	Multiply T times value defined by A, result to P Reg
LDPK	01101110DDDDDDDD	1	1	Load page reg for data memory with 8-bit constant D
LDP	01101111IAAAAAAA	1	1	Load DP reg with value whose address is at A
LARK	01110RRRDDDDDDDD	1	1	Load Auxiliary Register R with 8-bit constant D; MSB's Zero
EXOR	01111000IAAAAAAA	1	1	Exclusive OR Acc with value defined by A; result to LSBs of Acc; zero MSB's
AND	01111001IAAAAAAA	1	1	AND LSB's of Acc with value defined by A; result to LSB's of Acc; (zero)-(MSB's)
OR	01111010IAAAAAAA	1	1	OR LSB's of Acc with value defined by A; result to Acc; (zero)-(MSB's of Acc)
LST	01111011IAAAAAAA	1	1	Load Status with 16-bit value found at location A in RAM
SST	01111100IAAAAAAA	1	1	Store Status in location defined by 8-bit address A in RAM
TBLW	01111101IAAAAAAA	3	1	Table Write; write the value at Ram address to program memory address in Acc
LACK	01111110DDDDDDDD	1	1	Load Accumulator with 8-bit constant from instruction word
NOOP	0111111110000000	1	1	No-operation
DINT	0111111110000000	1	1	Disenable Interrupt-masks interrupt input INT
EINT	0111111110000010	1	1	Enable Interrupt-unmasks interrupt input INT
ABS	0111111110001000	1	1	Absolute Value operation; if Acc 0, Acc Acc; else Acc Acc
ZAC	0111111110001001	1	1	Clear Accumulator; zeros Acc
RAMV	0111111110001010	1	1	Reset Overflow Mode
SAMV	0111111110001011	1	1	Set Overflow Mode
CALLA	0111111100001100	2	1	Call subroutine indirect
RET	0111111110001101	2	1	Return from Subroutine
PAC	0111111110001110	1	1	Load accumulator with contents of P Reg
APAC	0111111110001111	1	1	Add accumulator to contents of P Reg; Result to Acc
SPAC	0111111110010000	1	1	Subtract contents of P reg from Accumulator; Result to Acc
MPYK	100CCCCCCCCCCCCC	1	1	Multiply by constant C
BARNZ	11110100XXXXXXXX	2	2	Branch if Loop Counter Not Zero, to location defined PC+1
BV	11110101XXXXXXXX	2	2	Branch if Overflow Bit in ST is 1
BIOZ	11110110XXXXXXXX	2	2	Branch if IO Bit in ST (from IO pin) is 1
CALL	11111000XXXXXXXX	2	2	Call Subroutine
B	11111001XXXXXXXX	2	2	Unconditional Branch to location W at PC+1
BLZ	11111010XXXXXXX	2	2	Branch if Acc is less than zero
BLEZ	11111011XXXXXXXX	2	2	Branch if Acc is less than or equal to zero
BGZ	11111100XXXXXXXX	2	2	Branch if Acc is greater than zero
BGEZ	11111101XXXXXXXX	2	2	Branch if Acc is greater than or equal to zero
BNZ	11111110XXXXXXXX	2	2	Branch if Acc is not zero
BZ	11111111XXXXXXXX	2	2	Branch if Acc is equal to zero

TABLE B

ALU FUNCTIONS

	Control Code						Propagate Node	Generate Node	Output
	#AUM0	#AUM1	#AUM2	#AUM3	#AUM4	#AUMB			
Add	0	1	1	0	0	0	A+B	AB	$A+B+C_{in}$
Subtract	1	0	0	1	0	0	A+B	AB	$A+B+C_{in}$
Load Acc	0	1	0	1	1	0	B	X	B+1=B
Exclusive Or	1	0	0	1	1	0	A+B	X	A+B+1=A+B
Or	1	0	0	1	1	0	AB (=A+B)	X	A+B+1=A+B
And	0	1	1	1	1	0	A+AB	X	(A+AB)+1=A+B=A
Abs. Value	0	0	1	1	0	1	A	0	$A+C_{in}$

What is claimed is:

1. A microcomputer formed in a single integrated circuit comprising:

an arithmetic/logic unit having data input and data output;

a data memory having an address input and having data input/output means;

data bus means coupled to the data input and data output of the arithmetic/logic unit and coupled to the data input/output means of the data memory, the data bus means transferring multi-bit data;

a program memory having an address input and having an instruction output, the program memory storing instruction words;

program address means having an input and including incrementing means; said program address means having an output connected to said address input of the program memory means;

control means for generating controls in response to instruction words; the controls defining operation of the arithmetic/logic unit, transfer of multi-bit data to and from the data bus means, and operation of said program address means;

program bus means coupling said instruction output to an input of said control means, and to said input of said program address means, the program bus means transferring multi-bit information;

timing means for establishing repetitive operating cycles wherein during one of said operating cycles multi-bit data is transferred from the data memory to the data input of the arithmetic/logic unit via said data bus means, the program address means applies an address to the address input of the program memory, and the control means receives an instruction word from the instruction output via said program bus means;

bus interchange means within said integrated circuit and coupled to said data bus means and to said program bus means for

(a) transferring said multi-bit data from the data bus means to the program bus means and for transferring said multi-bit data from the program bus means to said input of said program address means, both during one of said operating cycles, and

(b) transferring said multibit information from said instruction output of said program memory to said program bus means and transferring said multibit information from said program bus means to said data bus means, both during one of said operating cycles,

(c) all said transferring being in response to controls received from said control means generated from a single one of said instruction words.

2. A device according to claim **1** wherein:

after transferring said multi-bit data and multi-bit information in response to said single one of said instruction words via said bus interchange means,

multi-bit information from the program bus means is valid on said data bus means during one part of said one of said operating cycles and

multi-bit data from the data bus means is valid on said program bus means during another part of a different one of said operating cycles.

3. A device according to claim **2** wherein the bus interchange means receives said multi-bit data from the data bus means only during said one part for transfer to the program bus means, and receives said multi-bit information from the program bus means during said another part for transfer to the data bus means.

4. A device according to claim **1** wherein the data output of the arithmetic/logic unit is coupled to an accumulator and an output of the accumulator is coupled to the data bus means.

5. A device according to claim **4** wherein an output of the accumulator is coupled to a data input of the arithmetic/logic unit.

6. A microcomputer formed in a single integrated circuit comprising:

an arithmetic/logic unit having data input and data output;

a data memory having an address input and having data input/output means;

data bus means coupled to the data input and data output of the arithmetic/logic unit and coupled to the data input/output means of the data memory, the data bus means transferring multi-bit data;

a program memory having an address input and having an instruction output, the program memory storing instruction words;

program address means having an input and including incrementing means; said program address having an output connected to said address input of the program memory means;

program bus means separate from the data bus means and coupled to said instruction output and to said input of said program address means, the program bus means transferring multi-bit information;

control means having an input coupled to receive instruction words from said program bus means, said control means generating sets of controls in response to the instruction words; the sets of controls defining operation of the arithmetic/logic unit, transfer of multi-bit data to and from the data bus means, transfer of multibit information to and from the program bus means, and operation of said program address means;

timing means for establishing repetitive operating cycles wherein during one of said operating cycle multi-bit data is transferred from the data memory to the data input of the arithmetic/logic unit via said data bus means, the program address means applies an address to the address input of the program memory, and the control means receives an instruction word from the instruction output via said program bus means;

bus interchange means within said integrated circuit and coupled to said data bus means and to said program bus means, the bus interchange means including:

(a) means for transferring said multi-bit data from the data bus means to the program bus means and for transferring said multi-bit information from the program bus means to said data bus means,

(b) said means for transferring and said control means operating in response to one of said instructions words to transfer multi-bit data from the data bus means via said bus interchannge means to said input of the program address means, in one of said operating cycles,

(c) said means for transferring and said control means operating in response to a given instruction word to transfer multi-bit information from said instruction output of said program memory via said bus interchange means to said data bus means, in one of said operating cycles.

7. A microcomputer according to claim **6** wherein said one instruction word is the same as said given instruction word.

8. A microcomputer according to claim 6 including address and data bus means external to said integrated circuit and coupled to said address bus means and to said data bus means, and program and data memory means external to said integrated circuit coupled to said address and data bus means.

9. A microcomputer according to claim 8 wherein said address and data bus means external to the integrated circuit include an address bus and a data bus.

* * * * *

JXM-0019

337-TA-853

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO
08/484,918	06/07/95	MOORE C	NANO-001/05U

B3M1/0403

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EXAMINER	
ENG, D	
ART UNIT	PAPER NUMBER
2315	11

DATE MAILED: 04/03/97

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☒ Responsive to communication(s) filed on 1/97

☐ This action is FINAL.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire three month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 19-21, 65-67 + 72-79 is/are pending in the application.
Of the above, claim(s) _____ is/are withdrawn from consideration.
☐ Claim(s) _____ is/are allowed.
☒ Claim(s) 19-21, 65-67 + 72-79 is/are rejected.
☐ Claim(s) _____ is/are objected to.
☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.
☐ The specification is objected to by the Examiner.
☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been
☐ received.
☐ received in Application No. (Series Code/Serial Number) _____.
☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of Reference Cited, PTO-892
☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____
☐ Interview Summary, PTO-413
☒ Notice of Draftperson's Patent Drawing Review, PTO-948
☐ Notice of Informal Patent Application, PTO-152

–SEE OFFICE ACTION ON THE FOLLOWING PAGES–

U.S. GPO: 1996-404-...

TPL853_00002433

The active claims are 19-21, 65-67 and 72-79.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 19-21, 65-67 and 72-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Magar in view of Pelgrom.

See at least Figures 1 and 2 and the corresponding description in the specification of Magar. Figure 1 shows a data processing system having a single chip microcomputer 10 and an I/O interface 12. Figure 2a shows that the microcomputer includes clock generator and a cpu (the rest of the components). Although Mager's microprocessor is fabricated on the same chip, Magar does not explicitly state that the compoents are constructed of the same process technology with corresponding manufacturing variations. See lines 40-43 in column 4 of Pelgrom. Pelgrom teaches that electronioc components would exhibit same characteristics if they are manufactured by the same process technology. Since Pelgrom's microprocessor is made of electronic components, it would have obvious, from the teahcing of Pelgrom, to a person of ordinary skill in the art to have the components of Magar' microprocessor and clock (oscillator) make of the same process for ensuring processing frequency of the cpu to track the clock rate in response to the parameter variations.

JXM-0018
337-TA-853

NANO-001/05US
N0765-2008

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on July 3, 1997.

Date: 7/3/97 By: Patricia K. Parry
Patricia K. Parry

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	Examiner: D. Eng
Charles H. Moore et al.	
Serial No. 08/484,918	Art Unit: 2315
Filed: June 7, 1995	AMENDMENT
For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK	Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Amendment is being submitted in response to the Office Action dated April 3, 1997 in the above-identified patent application.

IN THE CLAIMS

Please amend claim 73 as follows:

73(Twice Amended). A microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and [including] being constructed of a second plurality of electronic devices, thus varying the [operating characteristics] processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of [transistors] electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said

integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation.

REMARKS

The above changes to the language of claim 73 clarify that claim and eliminate an inadvertent lack of antecedent basis problem in the former wording of the claim.

Claims 19-21, 65-67 and 72-79 were rejected under 35 U.S.C. § 103 as unpatentable over Magar, U.S. Patent 4,503,500. Shortly before issuing the Office Action, the Examiner had called to indicate that certain claims were allowable over the prior art, but when the undersigned attorney returned the Examiner's call, it was indicated that new prior art had been found and that a new action would be forthcoming. It is assumed that the Magar reference relied on is that new prior art. A review of the Magar reference shows that it is apparently no more pertinent than prior art acknowledged in the application, in that the clock disclosed in the Magar reference is in fact driven by a fixed frequency crystal, which is external to the Magar integrated circuit.

The clock gen circuit shown at the lower right hand edge of Fig. 2a in the Magar patent is of the same general type as shown at 434 in Fig. 17 of the present application, but depicted differently in that it shows the clock gen circuit portion which is on the semiconductor substrate, while Fig. 17 shows the external crystal at 434, connected to I/O interface 432 in the present invention. The crystal clock 434 is thus used in the invention for synchronizing I/O timing with the outside world, while the ring counter variable speed clock 430 also shown in Figure 17 is used for generating on-chip clock signals. The clock 430 is an example of the oscillator recited in the claims, the clock rate of which varies in the same way as a function of one or more device parameters associated with the integrated circuit substrate.

The definitive statement that the clock gen circuit in Fig. 2a in the Magar patent is equivalent to the "conventional crystal clock" 434 in Fig. 17 of the present application is at col. 15, lines 26-41 of Magar:

> "The chip 10 includes a clock generator 17 which has two external pins X1 and X2 to which a crystal (or external generator) is connected. The basic crystal frequency is up to 20 MHz and is represented by a clock 0 of Fig. 3a. This clock 0 has a period of 50 ns, minimum, and is used to generate for quarter-cycle clocks Q1, Q2, Q3 and Q4, seen in FIGS. 3b-3e, providing the basic internal timing for the microcomputer chip 10. A set of four quarter cycle clocks Q1 to Q4 defines one machine state of time of 200 ns., minimum; the states are referred to as S0, S1, S2 in FIG 3. The clock generator produces an output CLKOUT, Fig. 3f, on one of the control bus lines 13. CLKOUT has the same period as

Q1, but 50% duty cycle and beginning at the midpoint of Q1. This output is used for timing or synchronizing external components of the system of FIG. 1."

This description in Magar should be contrasted with the following detailed description of an embodiment of the present invention, as shown in Fig. 17, at explained at page 32, lines 3-29:

"Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor 50 provides a dual-clock scheme as shown in Figure 17, with the CPU 70 operating asynchronously to I/O interface 432 forming part of memory controller 118 (Figure 2) and the I/O interface 432 operating synchronously with the external world of memory and I/O devices. The CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor 50 for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface 432, speed of which is controlled by a conventional crystal clock 434. The interface 432 processes requests for memory accesses from the microprocessor 50 and acknowledges the presence of I/O data. The microprocessor 50 fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. By decoupling the variable speed of the CPU 70 from the fixed speed of the I/O interface 432, optimum performance can be achieved by each. Recoupling between the CPU 70 and the interface 432 is accomplished with handshake signals on lines 436, with data/addresses passing on bus 90, 136."

From these two quotations, it is clear that the element in Fig. 17 missing from Fig. 2a in Magar is the ring counter variable speed clock 430, and that Magar is merely representative of the "most microprocessors" acknowledged as prior art in the above description from the present application, which prior art microprocessors use a "conventional crystal clock." Because the variable speed clock is a primary point of departure from the prior art, independent claims 19, 65, 73 and 78 all recite a system including a variable speed clock or a method including using a variable speed clock. In light of the prior art, of which Magar is a good example, Applicants are entitled to claims of this scope. Dependent claims 20, 66, 74 and 79 further recite a second clock, exemplified by the crystal clock 434 in Fig. 17.

Contrary to the Examiner's assertion in the rejection that "one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock vary together due to manufacturing variation, operating voltage and temperature of the IC", one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock *do not* vary together due to manufacturing variation, operating voltage and temperature of the IC in the Magar microprocessor, as taught in the above quotation from the reference. This is simply because the Magar microprocessor clock is

frequency controlled by a crystal which is also external to the microprocessor. Crystals are by design fixed-frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The Magar microprocessor in no way contemplates a variable speed clock as claimed.

In making the rejection based on Magar, the examiner appears to be confusing the multiple uses and meanings of the technical term "clock." A clock is simply an electrical pulse relative to which events take place. Conventionally, a CPU is driven by a clock that is generated by an crystal. The crystal might be connected directly to two pins on the CPU, as in Magar, and be caused to oscillate by circuitry contained in the CPU with the aid of possibly other external components. Alternatively, the crystal may be contained in a package with the oscillation circuitry, the packaged component thus called an oscillator, and connected to one pin on the CPU as in Edwards et al., U.S. Patent 4,680,698.

While an oscillator may be a clock, a clock is not usually an oscillator. An oscillator must exist someplace in the circuit from which a periodic clock is derived. In both cases, the crystal (or the entire oscillator in the second case) is external to the CPU, and the output of the oscillator circuitry is a "clock." This clock is typically modified to produce additional required clock signals for the system. The many clock signals are sometimes created by circuitry called a "clock generator." For example, see Magar, Fig. 2a. The "clock gen" connects to a crystal at external pins X1 and X2 and generates clock signals for the system Q1, Q2, Q3, Q4 and CLKOUT. Other cited reference have similar examples, see Palmer, U.S. Patent 4,338,675, Fig. 1, item 24; Pohlman et al., U.S. Patent 4, 112,490 Fig. 1, item 22. All these systems operate at a frequency determined by the external crystal. The single, fixed, oscillation frequency of the crystal is determined by how the device is manufactured, i.e., how the crystal is cut and trimmed, and other factors. Crystals are used precisely for this purpose; they oscillate at a given frequency within a tolerance determined by their manufacture. Because of the cutting and trimming required, and that the crystal slice is typically suspended by two wires to allow it to freely oscillate, crystal oscillators have never, to Applicants' knowledge, been fabricated on a single silicon substrate with a CPU, for instance. Even if they were, as previously mentioned, crystals are by design fixed-frequency devices whose oscillation frequency is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The oscillation frequency of a crystal on the same substrate with the microprocessor would inherently not vary due to variations in manufacturing, operating voltage and temperature in the same way as the frequency capability of the microprocessor on the same underlying substrate, as claimed.

Note that the term clock can refer to many different signals since the definition is broad, and that it can also refer to the oscillator that is required to generate the clock. While a crystal-controlled oscillator typically operates at a single speed, the circuitry around the crystal may be

designed so that the output of the entire oscillator circuit can be varied. Many mechanisms can be used to control the output of a variable-frequency oscillator, including manual inputs, program-controlled inputs, temperature sensors, or other devices. Non-crystal controlled oscillators are also possible, and when they are designed as variable-frequency oscillators they are typically also controlled by manual inputs, program-controlled inputs, temperature sensors and other devices.

The present invention is unique in that it applies, and can only apply, in the circumstance where the oscillator or variable speed clock is fabricated on the same substrate as the driven device. The example given is a non-crystal controlled circuit, a ring oscillator. A ring oscillator will oscillate at a frequency determined by its fabrication and design and the operating environment. Thus in this example, the user designs the ring oscillator (clock) to oscillate at a frequency appropriate for the driven device when both the oscillator and the device are under specified fabrication and environmental parameters. Crucial to the present invention is that since both the oscillator or variable speed clock and driven device are on the same substrate, when the fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together. This differs from all cited references in that the oscillator or variable speed clock and the driven device are on the same substrate, and that the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so. Like the cited references, the driven device might additionally contain clock generation circuitry to produce variations on the clock output of the oscillator or variable speed clock for the other circuitry on the device.

The remaining Bennett et al., Brantingham, Pollack, Gruner et al.and Suzuki et al. references, cited but not applied in a rejection, have been reviewed and found not pertinent to the invention as claimed.

Based on the above remarks, the rejection under 35 USC § 103 is believed to be overcome. All of the claims in the application are believed to be patentable over the prior art. This application is believed to be in condition for allowance, and allowance is solicited.

Respectfully submitted,

COOLEY GODWARD LLP

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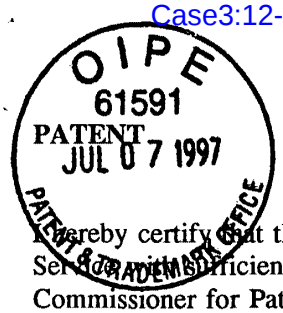
GAU 2315



Attorney Docket No. NANO-001/05US

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on July 3, 1997.

Date: 7-3-97 By: Patricia K. Parry
Patricia K. Parry

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of)
)
Charles H. Moore et al.)
)
Serial No. 08/484,918)
)
Filed: June 7, 1995)
)
For: HIGH PERFORMANCE)
MICROPROCESSOR HAVING)
VARIABLE SPEED SYSTEM)
CLOCK)
)

Examiner: David Y. Eng

Art Unit: 2315

AMENDMENT TRANSMITTAL

Palo Alto, CA 94306

RECEIVED
JUL 29 97
GROUP 2600

Assistant Commissioner for Patents
Box Non-Fee Amendments
Washington, D.C. 20231

Sir:

Transmitted herewith is an Amendment in the above-identified application.

[X] Small entity status of this Application under 37 CFR 1.9 and 1.27 has been established by a Verified Declaration previously submitted.

[ ] A Verified Declaration of Small Entity Status Under 37 CFR 1.9 and 1.27 is enclosed.

Also enclosed:

[ ] Petition for Extension of Time

[ ] Notice of Appeal

21338308

[ ] Information Disclosure Statement

[ ] Associate Power of Attorney

[ ] Other:

The fees have been calculated as shown below:

FOR:	Claims after Amend.	- Claims Prev. Paid	= Extra Claims[1]	Small Entity Rate	Fee	Other Than a Small Entity Rate	Fee	Total Claim Fee
Total Claims	20	20	0	$11		$22		$0.00
Independent Claims	4	4	0	$40		$80		$0.00
Multiple Dependent Claims Not Previously Presented					$130		$260	$0.00
TOTAL								$0.00

1 If difference is negative, enter "0"; if Total Claims is 20 or less, enter 0; if Independent Claims is 3 or less, enter 0.

[ ] A check including the amount of the above indicated TOTAL FEES is attached.

[ ] Please charge Deposit Account No. 03-3117 in the amount of $.

[X] No fee is required.

[X] Conditional Petition for Extension of Time: An extension of time is requested to provide for timely filing if an extension of time is still required after all papers filed with this transmittal have been considered.

[X] The Commissioner is hereby authorized to charge any underpayment of the following fees associated with this communication, including any necessary fees for extension of time, or credit any overpayment to Deposit Account No. 03-3117:

[X] Any filing fees under 37 CFR 1.16 including fees for the presentation of extra claims.

[X] Any patent application processing fees under 37 CFR 1.17.

A **duplicate** copy of this sheet is attached for accounting purposes.

Respectfully submitted,

COOLEY GODWARD LLP

By: _____
Willis E. Higgins
Reg. No. 23,025

Cooley Godward LLP
Five Palo Alto Square
3000 El Camino Real
Palo Alto, CA 94306
(415) 843-5000

PATENT

NANO-001/05US
N0765-2008

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 on February 6, 1998.

Date: 2/6/98 By: Patricia K. Parry
Patricia K. Parry

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of
Charles H. Moore et al.
Serial No. 08/484,918
Filed: June 7, 1995
For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

Examiner: D. Eng
Art Unit: 2784

AMENDMENT

Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Amendment is being submitted in response to the Office Action dated October 16, 1997 in the above-identified patent application.

IN THE CLAIMS

Please amend claims 19, 65, 73 and 78 as follows:

19(Three Times Amended). A microprocessor system, comprising a single integrated circuit including a central processing unit and [a] an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit.

Sub 72 65(Three Times Amended). In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:

providing [a] an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor; and

using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock.

Sub 73 73(Three Times Amended). A microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation.

Sub 74 78(Twice Amended). In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon [a] an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing [a] an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors; and

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way

E4 relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate.

REMARKS

Claims 19-21, 65-67 and 72-79 were rejected under 35 U.S.C. § 103 as unpatentable over Magar, U.S. Patent 4,503,500, in view of newly cited Pelgrom et al., U.S. Patent 4,627,082. In response, the independent claims have been rewritten to specify that the entire ring oscillator variable speed system clock, variable speed clock or oscillator be provided in the integrated circuit, in order to sharpen the distinction over the prior art. Because the prior art does not provide an entire ring oscillator variable speed system clock, variable speed clock or oscillator in the integrated circuit, in that the prior art circuits require an external crystal, the prior art fails to teach or suggest the invention as now claimed. This rejection is believed to be overcome by these changes to the claims and these remarks.

Shortly before this Office Action was mailed, Mr. George Shaw, the Assignee's technical representative, and the undersigned attorney had a phone interview with the Examiner regarding this and another of Assignee's cases. Technical distinctions of the present case over the Magar reference previously cited were discussed, as well as the benefits of the invention. Below is recited the pertinent points of that discussion, as well as rebuttal to the new Pelgrom reference.

First, the Examiner states "Pelgrom teaches that electronic components would exhibit same characteristics if they are manufactured by the same process technology", and applicant agrees that this is well known in the art. The Examiner states that, "Since Pelgrom's [Magar's?] microprocessor is made of electronic components, it would have obvious, from the teaching of Pelgrom, to a person of ordinary skill in the art to have the components of Magar' microprocessor and clock (oscillator) make of the same process for ensuring processing frequency of the cpu to track the clock rate in response to the parameter variations." Applicant agrees that the processing frequency capability of the CPU would track the clock rate capability of the clock generator, as this is controlled by the laws of physics on which the Pelgrom reference is based. However, there would be no "tracking" of the clock rate produced by the Magar clock generator, because the entire circuit is not provided on the integrated circuit. Magar's clock generator relies on an external crystal connected to terminals X1 and X2 to oscillate, as is conventional in microprocessor designs. It is not an entire oscillator in itself. And with the crystal, the clock rate generated is also conventional in that it is at a fixed, not a variable, frequency. The Magar clock is comparable in operation to the conventional crystal clock 434 depicted in Fig. 17 of the present application for controlling the I/O interface at a fixed rate frequency, and not at all like the clock on which the claims are based, as has been previously stated.

The Examiner also states that "applicants contend that Magar's clock is external to the IC." This is not the case. The "clock gen" part of the oscillator circuit is clearly on the IC, but not the crystal. Applicants note that the crystal is external, connected to X1 and X2, as Magar cites at column 15, lines 26-27,

"The chip 10 includes a clock generator 17 which has two external pins X1 and X2 to which a crystal (or external generator) is connected."

Thus while most of Magar's clock (generator) circuitry is on the IC, the entire oscillator, which because it requires an external crystal, is not.

"The Examiner further states that applicants imply a "correspondence" in application between Applicant's clock 434 and Magar's clock. This is not the case. Applicants only state that the two clocks are "of the same general type" or are "equivalent" at the circuit level, in that they both use an external crystal to fix the clock rate. They are both of conventional design and not the subject of the claims in the instant case. Clearly, either type could be used to drive a CPU, as Magar depicts the conventional case and Applicant depicts a unique design which provides a variable clock frequency or rate.

Applicant's prior comments apparently did not make clear the distinction between an oscillator and a clock as it applies to the Magar reference. As a self-contained on-chip circuit, Magar's clock gen is distinguished from an oscillator in at least that it lacks the crystal or external generator that it requires. Thus Magar's circuit is not an entirely on-chip oscillator as contemplated in the present case, it is only a clock.

As mentioned in Applicant's previous remarks, the term clock is sometimes used interchangeably with oscillator, even inappropriately, leading to confusion. And, adding to the confusion, in the instant case, 430 is both an oscillator and a clock in the conventional senses. It is an oscillator in that it oscillates without external components (unlike the Magar reference). An example of such an oscillator circuit which does not utililze external components is given in Fig. 18 of the present application. It is also a clock in Magar reference sense in that it produces the various required timing signals needed of the CPU. The signals PHASE 0, PHASE 1, PHASE 2, and PHASE 3 in Applicant's Fig 18 are synonymous with Q1, Q2, Q3, and Q4 depicted in Magar Fig. 2a. The essential difference is that the frequency or rate of the PHASE 0, PHASE 1, PHASE 2, and PHASE 3 signals is determined by the processing and/or operating parameters of the integrated circuit containing the Fig. 18 circuit, while the frequency or rate of the Q1, Q2, Q3, and Q4 signals depicted in Magar Fig. 2a are determined by the fixed frequency of the external crystal connected to the circuit portion outputting the Q1, Q2, Q3, and Q4 signals shown in Magar Fig. 2a.

To summarize, the Pelgrom reference teaches well known art as one of the fundamental principles on which IC are designed. If components did not vary in a similar manner circuit performance could not be predicted and ICs could not be designed. This does not negate

patentability in the present case because it is not the fundamental principle that is claimed but the combination in light of the fundamental principle of enumerated heretofore uncombined circuits to produce a result not obtained with the prior art that is the subject of the claims in the instant case. The Magar teaching is well known in the art as a conventional crystal controlled oscillator. It is specifically distinguished from the instant case in that it is both fixed-frequency (being crystal based) and requires an external crystal or external frequency generator.

Based on the above changes to the claims and remarks, the rejection under 35 USC § 103 is believed to be overcome. All of the claims in the application are believed to be patentable over the prior art. This application is believed to be in condition for allowance, and allowance is solicited.

Respectfully submitted,

COOLEY GODWARD LLP

Willis E. Higgins
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Telephone: (650) 843-5145

PTO/SB/17 (12-97)
Approved for use through 9/30/00. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL

Note: Effective October 1, 1997.
Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 55.00

Complete if Known	
Application Number	08/484,918
Filing Date	June 7, 1995
First Named Inventor	Charles H. Moore et al.
Group Art Unit	2315
Examiner Name	David Y. Eng
Attorney Docket Number	NANO-001/05 US

METHOD OF PAYMENT (check one)

1. ☐ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 03-3117
Deposit Account Name: Cooley Godward LLP

☒ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17
☐ Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance

2. ☒ Payment Enclosed:
☒ Check ☐ Money Order ☐ Other

FEE CALCULATION

1. FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	
106	330	206	165	Design filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 0

2. CLAIMS

		Extra		Fee from below		Fee Paid
Total Claims	-20 =		X		=	
Independent Claims	- 3 =		X		=	
Multiple Dependent Claims			X		=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim
109	82	209	41	Reissue independent claims over original patent
110	22	210	11	Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	55.00
116	400	216	200	Extension for reply within second month	
117	950	217	475	Extension for reply within third month	
118	1,510	218	755	Extension for reply within fourth month	
128	2,060	228	1,030	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,320	241	660	Petition to revive - unintentional	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	

Other fee (specify) _____

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 55.00

SUBMITTED BY				Complete (if applicable)	
Typed or Printed Name	Willis E. Higgins			Reg. Number	23,025
Signature	Willis E. Higgins	Date	1-6-98	Deposit Account User ID	

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

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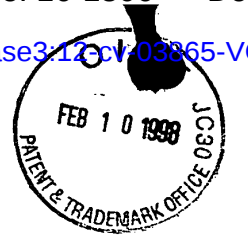


PATENT

Attorney Docket No. NANO-001/05US

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on February 6, 1998.

Date: 2/6/98 By: Patricia K. Parry
Patricia K. Parry

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Charles H. Moore et al.

Serial No. 08/484,918

Filed: June 7, 1995

For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED

Examiner: David Y. Eng

Art Unit: 2315

TRANSMITTAL FOR AMENDMENT

Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith is a Amendment in the above-identified application.

[ ] Small entity status of this Application under 37 CFR 1.9 and 1.27 has been established by a Verified Declaration previously submitted.

[ ] A Verified Declaration of Small Entity Status Under 37 CFR 1.9 and 1.27 is enclosed.

Also enclosed:

[X] Petition for Extension of Time

[ ] Notice of Appeal

21451083

TPL853_02954563

[ ] Information Disclosure Statement

[ ] Associate Power of Attorney

[ ] Other:

The fees have been calculated as shown below:

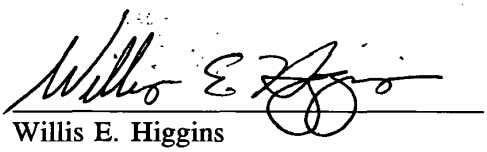
FOR:	Claims after - Amend.	Claims Prev. = Paid	Extra Claims[1]	Small Entity Rate	Small Entity Fee	Other Than a Small Entity Rate	Other Than a Small Entity Fee	Total Claim Fee
Total Claims	20	20	0	$11		$22		$0.00
Independent Claims	4	4	4	$41		$82		$0.00
Multiple Dependent Claims Not Previously Presented					$135		$270	$0.00
TOTAL								$0.00

1 If difference is negative, enter "0"; if Total Claims is 20 or less, enter 0; if Independent Claims is 3 or less, enter 0.

[X] A check including the amount of the above indicated TOTAL FEES is attached.

Respectfully submitted,

COOLEY GODWARD LLP

By: 
Willis E. Higgins
Reg. No. 23,025

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3000 El Camino Real
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(650) 843-5000

21451083

TPL853_02954564

#14

PATENT

Attorney Docket No. NANO-001/05US

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on February 6, 1998.

Date: 2/6/98 By: Patricia K. Carry
Patricia K. Carry

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Charles H. Moore et al.

Serial No. 08/484,918

Filed: June 7, 1995

For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED

Examiner: David Y. Eng

Art Unit: 2315

PETITION FOR EXTENSION OF TIME

Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicant petitions for an extension of time in which to file this response in the above-identified application. Enclosed is a check including the amount indicated below to extend the period for response from January 16, 1998, to February 16, 1998.

Extension of Time	Small Entity	Other than a Small Entity
[X] One Month	$55.00	
[ ] One Month		$110.00
[ ] Two Months	$200.00	
[ ] Two Months		$400.00

02/13/1998 GPAYNE 00000105 08484918
01 FC:215 55.00 OP

21451066

[ ] Three Months $475.00
[ ] Three Months $950.00

[ ] Four Months $755.00
[ ] Four Months $1,510.00

[ ] Five Months $1,030.00
[ ] Five Months $2,060.00

Extension of Time Fee: **$110.00**

Respectfully submitted,

COOLEY GODWARD LLP

By: _____
Willis E. Higgins
Reg. No. 23,025

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Palo Alto, CA 94306-2155
Attention: Patent Group
(650) 843-5000

84

PATENT

ANO-001/05US
N0765-2008

GP 2315

I hereby certify that this paper correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Date: 4/19/96 By: Felicia Walker

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	Examiner: D. Eng
Charles H. Moore et al.	Art Unit: 2315
Serial No. 08/484,918	
Filed: June 7, 1995	AMENDMENT
For: HIGH PERFORMANCE, LOW COST MICROPROCESSOR	Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Amendment is being submitted in response to the first Office Action in the above-identified patent application.

IN THE SPECIFICATION

At page 1, line 1, please change the title from "HIGH PERFORMANCE, LOW COST MICROPROCESSOR" to --HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK--.

110 JF 04/18/96 08484918 1 202 39.00 CK

21092053

B

1.

Please rewrite the Abstract as follows:

--A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.--

IN THE CLAIMS

Please amend claims 19-20 and 65-66 as follows:

19(Amended). A microprocessor system, comprising a single integrated circuit including a central processing unit and a ring [counter] oscillator variable speed system clock connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring [counter] oscillator variable speed system clock [being provided in a single integrated circuit] each including a plurality of electronic devices of like type, said central processing unit operating at a variable processing frequency dependent upon a variable speed of said ring oscillator variable speed system clock.

20(Amended). The microprocessor system of Claim 19 additionally comprising an input/output interface connected to exchange coupling control signals, address and data with said [input/output interface] central processing unit, and a second clock independent of said ring [counter] oscillator variable speed system clock connected to said input/output interface.

65(Amended). In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:

[which comprises fabricating] providing a ring [counter] oscillator system clock having a plurality of transistors within the integrated circuit, said plurality of transistors having operating characteristics disposed to vary similarly to operating characteristics of transistors included within the microprocessor; [and the microprocessor each having a plurality of transistors having operating characteristics which vary in the same way with variations in their fabrication,] and

using the ring [counter] oscillator system clock for clocking the microprocessor, said central processing unit operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock.

66(Amended). The method of Claim 65 additionally comprising the steps of:

providing an input/output interface for the microprocessor integrated circuit, [and]

clocking the input/output interface with a second clock independent of the ring [counter] oscillator system clock, and

buffering information within said input/output interface received from said microprocessor integrated circuit.

Please add the following new claims 71-79:

71. The microprocessor system of claim 20 further including system memory coupled to said input/output interface, said system memory being synchronized to said second clock and operating synchronously with respect to said ring oscillator variable speed system clock.

72. The method of claim 65 further including the steps of:

transferring information to and from said microprocessor in synchrony with said ring oscillator system clock, and

buffering said information to facilitate transfer of said information to and from system memory synchronously with respect to said ring oscillator system clock.

73. A microprocessor system comprising:

a central processing unit disposed upon a substrate, said central processing unit operating at a processing frequency and including a first plurality of transistors;

an oscillator disposed upon said substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and including a second plurality of transistors designed such that operating characteristics of said first plurality and said second plurality of transistors vary in the same way as a function of parameter variation in one or more operational parameters associated with said substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation.//

74. The microprocessor system of claim 73 wherein said one or more parameters are included within the set consisting of: operating temperature of said substrate, operating voltage of said substrate, and fabrication process of said substrate.

75. The microprocessor system of claim 73 further comprising:

an input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, address and data with said central processing unit;

an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

76. The microprocessor system of claim 75 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.

77. The microprocessor system of claim 73 wherein said oscillator comprises a ring oscillator.

78. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon a substrate, said central processing unit including a first plurality of transistors and being operative at a processing frequency;

clocking said central processing unit at a clock rate using an oscillator disposed upon said substrate, said oscillator being provided so as to include a second plurality of transistors with said central processing unit being clocked by said oscillator at a variable frequency dependent upon variation in one or more operational parameters associated with said substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more operational parameters associated with said substrate.

79. The method of claim 78 further comprising the steps of:

connecting an input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, address and data between said input/output interface and said central processing unit;

clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

REMARKS

This amendment responds to the first office action. Claims 19-20 and 65-66 have been amended, and new claims 71-79 have been added.

The Examiner has requested that applicants update the status of the parent application. Applicants note that the parent application Serial No. 07/389,334 has issued as U.S. Pat. No. 5,440,749. Also pursuant to the Examiner's request, a new title and new abstract more aptly descriptive of the invention have been provided.

The Examiner has rejected claims 19-21 and 65-67 under 35 U.S.C. § 112 as being indefinite. With respect to the apparatus claims, the Examiner asserted that there exists no functional relationship and interconnection between the claimed components. Similarly, the Examiner asserted that a functional relationship does not exist between the steps of the method claims, and that it is unclear what the steps try to accomplish.

Applicants note that the present invention is directed to a microprocessor system including a central processing unit and a ring oscillator variable speed system clock connected thereto. In accordance with the claimed invention, the central processing unit and the ring oscillator variable speed system clock are provided in a single integrated circuit. This allows, for example, the central processing unit to track variations in the speed of the ring oscillator variable speed system clock, since the elements of each are disposed in the same integrated circuit. By this amendment the term "ring counter" has been replaced with "ring oscillator", in order to more particularly identify the ring oscillator (FIG. 18) incorporated within a preferred implementation of the microprocessor system of the invention.

Although applicants submit that the "functional relationship" between the claimed central processing unit and system clock connected thereto is inherently clear, the apparatus and method claims have been amended in an effort to accommodate the Examiner's concerns with respect to 35 U.S.C. §112. For example, claim 19 now recites a "functional relationship" in that it is made explicit that the ring oscillator variable speed system clock is disposed to clock the central processing unit. Moreover, the central processing unit and ring oscillator variable speed system clock are described as "each including a plurality of electronic devices of like type". This allows the central processing unit to operate at a

variable processing frequency which depends upon a variable speed of the ring oscillator variable speed system clock. See, for example, the specification at page 31, line 33 to page 32, line 1:

> By deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast. For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor 50 will operate slower than normal. Since the microprocessor 50 *ring oscillator clock 430 is made from the same transistors on the same die as the latches and gates*, it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.

Method claim 65 has been similarly amended, and now recites the step of:

> fabricating a ring oscillator system clock having a plurality of transistors, said plurality of transistors having operating characteristics disposed to vary similarly to operating characteristics of transistors included within the microprocessor ... .

The method claims thus now prescribe a technique for clocking a microprocessor using a ring oscillator system clock comprised of transistors having similar operating characteristics as those within the microprocessor. This advantageously allows the processing frequency of the microprocessor to track the clock rate of the ring oscillator system clock.

The Examiner has rejected claims 19 and 65 under 35 U.S.C. § 103 as being unpatentable over Sheets. The Examiner stated that Sheets teaches a microprocessor system having a microprocessor and a variable speed clock generator. Although admitting that Sheets does not disclose that his clock is implemented using a ring oscillator, the Examiner opined that a "counter is a basis component of [a] clock generator". It was further asserted that choosing the counter to be of the ring type is merely a matter of design choice.

Applicants again observe that the present invention is directed to a system and method for clocking a central processing unit disposed *within the same integrated circuit* as a ring oscillator variable speed system clock. This allows, for example, the central processing unit to track variations in the speed of the ring oscillator variable speed system clock, since the elements of each are disposed in the same integrated circuit. That is, the operational speed of the microprocessor and ring oscillator clock are designed to vary similarly as a function of variation in temperature, processing and other parameters affecting circuit performance.

The system of Sheets effects microprocessor clocking in a way which is entirely dissimilar from that of the present invention, and in fact teaches away from Applicants' clocking scheme. In particular, Sheets describes the use of discrete, commercially available microprocessor chips, e.g., the Motorola 68000 (col. 5, line 16), driven by a separate clock (VCO 12 of FIG. 1). As is well known, such microprocessor chips include terminals or pins, such as the CLK and INT terminals of microprocessor (FIG. 1), for receiving inputs from external devices like the VCO 12 and fixed oscillator 103. Because the VCO 12 is not integral with the microprocessor 101, Sheets has proposed a technique for adjusting the frequency of VCO 12 in accordance with a desired operating frequency of the microprocessor 101. Specifically, a digital word indicative of this desired operating frequency is written by microprocessor 101 to VCO 12 by way of data bus 104 as a means of adjusting clock frequency.

The present invention does not similarly rely upon provision of frequency control information to an external clock, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, since the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance. Sheets' system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.

Although the foregoing clearly indicates the existence of a patentable distinction between the system of Sheets and the present invention, claims 19 and 65 have nonetheless been amended to advance prosecution of the application. Specifically, claims 19 and 65 now explicitly recite that the ring oscillator and microprocessor are provided within the same integrated circuit. Moreover, these claims further state that the plurality of transistors included within the ring oscillator clock have operating characteristics which vary similarly to operating characteristics of transistors included within the microprocessor, thereby enabling the processing frequency of the microprocessor to track the speed of the ring oscillator clock:

> ...The CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process.
> (page 32, lines 10-13)

Neither of these aspects of the present invention are suggested by Sheets. As discussed above, Sheets describes the use of commercially available microprocessor chips, and depicts the microprocessor 101 as being coupled to a separate clock (i.e, VCO 12) by way of a data bus 104 and address bus 105. Moreover, the VCO 12 clearly is not comprised of transistors having operating characteristics disposed to vary similarly to those of transistors within the microprocessor 101. Rather, the VCO 12 is seen to be comprised of an LC oscillator (col. 3, line 58 and FIG. 6), which clearly is not adapted to mimic variation in the speed of transistors within the microprocessor 101. Accordingly, applicant respectfully submits that amended claims 19 and 65 are patentable over Sheets, and requests that the rejection thereof under 35 U.S.C. § 103 be withdrawn.

Since Schaire does not supplement the lack of teaching within Sheets with respect to amended claims 19 and 65, it is also respectfully submitted that pending claims 20-21 and 66-67 are patentable over Sheets in view of Schaire. Further with regard to pending claims 20 and 66, it is observed that Schaire provides no indication that bus interface unit 10 is clocked by a signal from a clock different from that used to clock the host microprocessor. That is, the origin of high-speed clock signal 230 (FIG. 1) provided to bus interface unit 10 does not appear to be described. Hence, Schaire fails to teach the claimed provision of separate, independent clock signals to an input/output interface buffer and microprocessor. Accordingly, applicant respectfully requests that the outstanding rejection of claims 20-21 and 66-67 under 35 U.S.C. § 103 be withdrawn.

By this amendment new claims 71-79 have also been added to more particularly identify the invention which appears to be available for protection. In this regard new claims 71-72 point out that information is transferred to and from the microprocessor in synchrony with the ring oscillator system clock, and that this information is buffered to facilitate transfer thereof to and from system memory synchronously with respect to the ring oscillator system clock. New claims 73-79 explicitly recite that the central processing unit and ring oscillator include first and second pluralities of transistors, respectively, and that the

operating characteristics of these transistors vary in the same way as a function of variation in operational parameters (e.g., operating temperature) of the substrate. This advantageously allows a processing frequency of the central processing unit to track a clock rate of the ring oscillator as a function of substrate parameter variation.

Accordingly, in view of the above remarks, it is submitted that this application is now ready for allowance. Early notice to this effect is solicited.

If in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned at (415) 843-5000.

Respectfully submitted,

COOLEY GODWARD CASTRO
HUDDLESON & TATUM

By: _____
Willis E. Higgins
Reg. No. 23,025

Cooley Godward Castro
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3000 El Camino Real
Palo Alto, CA 94306-2155
(415) 843-5000

#5

PATENT

Attorney Docket No. NANO-001/05US
N0765-2008

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on April 11, 1996.

Date: 4/11/96 By: Felicia Wall

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Charles H. Moore et al.

Serial No. 08/484,918

Filed: June 7, 1995

For: HIGH PERFORMANCE, LOW COST MICROPROCESSOR

Examiner: David Y. Eng

Art Unit: 2315

RESPONSE TRANSMITTAL

Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith is an Amendment in the above-identified application.

[] Small entity status of this Application under 37 CFR 1.9 and 1.27 has been established by a Verified Declaration previously submitted.

[] A Verified Declaration of Small Entity Status Under 37 CFR 1.9 and 1.27 is enclosed.

Also enclosed:

[] Information Disclosure Statement

[] Declaration

[] Associate Power of Attorney

230 EK 03-3117 04/25/96 08484918
23126 215 55.00CH

21093950

The fees have been calculated as shown below:

FOR:	Claims after Amend.	- Claims Prev. Paid	= Extra Claims[1]	Small Entity Rate	Fee	Other Than a Small Entity Rate	Fee	Total Claim Fee
Total Claims	13	20	0	$11		$22		$0.00
Independent Claims	4	3	1	$39		$78		$39.00
Multiple Dependent Claims Not Previously Presented					$125		$250	$0.00
TOTAL								$39.00

1 If difference is negative, enter "0"; if Total Claims is 20 or less, enter 0; if Independent Claims is 3 or less, enter 0.

Extension of Time	Small Entity	Other than a Small Entity
[] One Month	$55.00	
[] One Month		$110.00
[] Two Months	$190.00	
[] Two Months		$380.00
[] Three Months	$450.00	
[] Three Months		$900.00
[] Four Months	$700.00	
[] Four Months		$1,400.00

Extension of Time Fee: **$**

[] Fee regarding Information Disclosure Statement:

[] Fee Under 37 CFR 1.17(p) ($220.00)

[] Petition Fee Under 37 CFR 1.17(i)(l) ($130.00)

Total Information Disclosure Statement Fee: **$**

Other fees (list individually)

(none)

Total Other Fees: **$**

21093950

TPL853_02954578

TOTAL FEES: $39.00

[] A check including the amount of the above indicated TOTAL FEES is attached.

[] Please charge Deposit Account No. 03-3117 in the amount of $.

[X] A check in the amount of $39.00 is attached.

[] No fee is required.

[X] Conditional Petition for Extension of Time: An extension of time is requested to provide for timely filing if an extension of time is still required after all papers filed with this transmittal have been considered.

[X] The Commissioner is hereby authorized to charge any underpayment of the following fees associated with this communication, including any necessary fees for extension of time, or credit any overpayment to Deposit Account No. 03-3117:

[X] Any filing fees under 37 CFR 1.16 including fees for the presentation of extra claims.

[X] Any patent application processing fees under 37 CFR 1.17.

A **duplicate** copy of this sheet is attached for accounting purposes.

Respectfully submitted,

COOLEY GODWARD CASTRO
HUDDLESON & TATUM

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TPL853_02954579

PATENT

NANO-001/05US
N0765-2008

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on January 8, 1997.

Date: 1-8-97 By: Patricia K. Carey

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of
Charles H. Moore et al.
Serial No. 08/484,918
Filed: June 7, 1995
For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

Examiner: D. Eng
Art Unit: 2315

AMENDMENT

Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Amendment is being submitted in response to the Final Rejection dated July 8, 1996 in the above-identified patent application.

IN THE CLAIMS

Please amend claims 19, 65, 66, 71, 72, 73, 74 and 78 as follows:

19(Twice Amended). A microprocessor system, comprising a single integrated circuit including a central processing unit and a ring oscillator variable speed system clock connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices [of like type] correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit [operating at a variable processing frequency dependent upon a variable speed of] and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said integrated circuit.

65(Twice Amended). In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:

providing a ring oscillator system clock [having a plurality] constructed of [transistors] electronic devices within the integrated circuit, said [plurality of transistors] electronic devices having operating characteristics [disposed to] which will, because said ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary [similarly to] together with operating characteristics of [transistors] electronic devices included within the microprocessor; and

using the ring oscillator system clock for clocking the microprocessor, said [central processing unit] microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock.

66(Twice Amended). The method of Claim 65 additionally comprising the steps of:

providing an input/output interface for the microprocessor integrated circuit, and

clocking the input/output interface with a second clock independent of the ring oscillator system clock[, and

buffering information within said input/output interface received from said microprocessor integrated circuit].

72(Amended). The method of claim 65 further including the [steps] step of:

transferring information to and from said microprocessor in synchrony with said ring oscillator system clock[, and

buffering said information to facilitate transfer of said information to and from system memory synchronously with respect to said ring oscillator system clock].

73(Amended). A microprocessor system comprising:

a central processing unit disposed upon [a] an integrated circuit substrate, said central processing unit operating at a processing frequency and [including] constructed of a first plurality of [transistors] electronic devices;

an oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and including a second plurality of [transistors] electronic devices, thus varying the [designed such that] operating characteristics of said first plurality and said second plurality of transistors [vary] in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation.

74(Amended). The microprocessor system of claim 73 wherein said one or more operational parameters [are included within the set consisting of:] include operating temperature of said substrate[,] or operating voltage of said substrate[, and fabrication process of said substrate].

78(Amended). In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon [a] an integrated circuit substrate, said central processing unit [including] being constructed of a first plurality of transistors and being operative at a processing frequency;

providing a variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors; and

clocking said central processing unit at a clock rate using [an oscillator, disposed upon said substrate, said oscillator being provided so as include a second plurality of transistors] variable speed clock with said central processing unit being clocked by said [oscillator] variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate.

Cancel claim 71.

REMARKS

Appreciation is expressed for the courteous and helpful telephone interview granted by the Examiner on January 7 and 8, 1997, with the undersigned attorney and Mr. George Shaw, representing the assignee of the application. The above changes to the claims are based on the discussion in the interview. Proposed changes to claims 19, 65 and 73 were sent by facsmile to the Examiner on January 7 to facilitate the further discussion on January 8. On January 8, the Examiner agreed that these changes merited further consideration of the application and appeared to overcome the prior art of record. The following remarks in part summarize the discussion in the interview and respond to specific points in the Final Rejection.

In the interview, the fact that operating characteristics of electronic devices in an integrated circuit will track one another depending on variations in the manufacturing process used to make the integrated circuit was discussed. This fact is described at page 31, line 1 through page 32, line 1 of this application, in the context of the microprocessor system of this invention. This fact is utilized in the present invention to provide a variable speed clock for the microprocessor, with the

clock speed varying in the same way as variations in the operating characteristics of the electronic devices making up the microprocessor. This allows the microprocessor to operate at its fastest safe operating speed, given its manufacturing process or changes in its operating temperature or voltage. In contrast, prior art microprocessor systems are given a rated speed based on possible worst case operating conditions and an external clock is used to drive them no faster than the rated speed. Under other than worst case operating conditions, the prior art microprocessors are actually capable of operating at a faster clock speed than their rated speed.

The above changes to the claims have been made to bring out the above distinction over the prior art more clearly. It is believed that they overcome the rejection of claims 19-21, 65-67 and 71-79 under 35 USC § 112, define statutory subject matter, i.e, a system implemented as a single integrated circuit having defined characteristics or a process, as well as distinguishing over the prior art of record.

In the rejection under 35 USC § 103, the Examiner contends that the Sheets reference "clearly indicates in lines 46-48 of column 2 that the system 100 shown in Figure 1 is fabricated *on a single chip* using MOS technology." Specific issue is taken with the inclusion of the italicized language in this characterization of the reference. Sheets does not say that the system 100 is on a single chip, only that it is implemented in MOS technology. At column 5, lines 15-17, a specific example of the Motorola 68000 microprocessor is given. That microprocessor is driven by an external clock that provides a clock signal to a designated pin of the microprocessor integrated circuit package. Applicants are aware of no prior art teaching or suggesting a variable speed oscillator in the same integrated circuit with a microprocessor and clocking the microprocessor with a clock speed that varies correspondingly with changes in operating characteristics of electronic devices making up the microprocessor, as a result of being in the same integrated circuit as the microprocessor, as claimed. Even if the Examiner is correct that the variable clock in Sheets is in the same integrated circuit as the microprocessor of system 100, that still does not give the claimed subject matter. In Sheets, a command input is required to change the clock speed. In the present invention, the clock speed varies correspondingly to variations in operating parameters of the electronic devices of the microprocessor because both the variable speed clock and the microprocessor are fabricated together in the same integrated circuit. No command input is necessary to change the clock frequency. The rejection under 35 USC § 103 is believed to be overcome.

All of the claims in the application are believed to be patentable over the prior art. This application is believed to be in condition for allowance, and allowance is solicited.

Respectfully submitted,

COOLEY GODWARD LLP

Willis E. Higgins
Reg. No. 23,025

Five Palo Alto Square
Palo Alto, CA 94306-2155
Telephone: (415) 843-5145

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GP2315

#8

71477 U.S

PATENT 01/13/97

Attorney Docket No. NANO-001/05US

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on January 8, 1997.

Date: 1-8-97 By: Patricia K. Carey

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED
JAN 15 1997
GROUP 2300

In re application of	
Charles H. Moore et al.	Examiner: David Y. Eng
Serial No. 08/484,918	Art Unit: 2315
Filed: June 7, 1995	
For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK	PETITION FOR EXTENSION OF TIME
	Palo Alto, CA 94306

Box AF
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicant petitions for an extension of time in which to file this response in the above-identified application. Enclosed is a check including the amount indicated below to extend the period for response from October 8, 1996, to January 8, 1997.

Extension of Time	Small Entity	Other than a Small Entity
[ ] One Month	$55.00	
[ ] One Month		$110.00
[ ] Two Months	$195.00	
[ ] Two Months		$390.00
[X] Three Months	$465.00	
[ ] Three Months		$930.00

260 NJ 01/14/97 08484918
1 217 465.00 CK

21235045

[ ] Four Months $735.00
[ ] Four Months $1,470.00

Extension of Time Fee: **$465.00**

[X] The Commissioner is hereby authorized to charge any underpayment of the following fees associated with this communication, including any necessary fees for extension of time, or credit any overpayment to Deposit Account No. 03-3117:

[X] Any filing fees under 37 CFR 1.16 for the presentation of extra claims.

[X] Any patent application processing fees under 37 CFR 1.17.

A **duplicate** copy of this sheet is attached for accounting purposes.

Respectfully submitted,

COOLEY GODWARD LLP

By: _____
Willis E. Higgins
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3000 El Camino Real
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(415) 843-5000

GP 2315
#5
3
1/17/97

PATENT Attorney Docket No. NANO-001/05US

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on January 8, 1997.

Date: 1-8-97 By: Patricia K. Carey

GROUP 2300

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	
Charles H. Moore et al.	Examiner: David Y. Eng
Serial No. 08/484,918	Art Unit: 2315
Filed: June 7, 1995	
For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK	REQUEST FOR ENTRY OF A SUBMISSION AFTER FINAL REJECTION AND WITHDRAWAL OF FINALITY UNDER 37 CFR 1.129(a)
	Palo Alto, CA 94306

BOX AF
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicant requests withdrawal of the final rejection dated July 8, 1996, and entry of Applicant's response under 37 CFR 1.116, submitted January 8, 1997.

The above-identified application has an effective pendency of at least two years as of June 8, 1995, taking into account any reference made in such application to any earlier filed application under 35 U.S.C. 120, 121, or 365(c). This submission after final rejection is being filed prior to the filing of an appeal brief and prior to abandonment. Therefore, the Applicant is entitled to have the submission after final rejection considered on the merits.

Enclosed with this request is the fee as set forth in 37 CFR 1.17(r)

260 NJ 01/14/97 08484918
1 246 385.00 CK

21235049

Processing Fee	Small Entity	Other than a Small Entity
[X]	$385.00	
[ ]		$770.00
Total Fee:	**$385.00**	

Enclosed is a check including the amount of the TOTAL FEE indicated above.

[X] The Commissioner is hereby authorized to charge any underpayment of the following fees associated with this communication, including any necessary fees for extension of time, or credit any overpayment to Deposit Account No. 03-3117:

[X] Any filing fees under 37 CFR 1.16 including fees for the presentation of extra claims.

[X] Any patent application processing fees under 37 CFR 1.17.

A **duplicate** copy of this sheet is attached for accounting purposes.

Respectfully submitted,

COOLEY GODWARD LLP

By: _____
Willis E. Higgins
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(415) 843-5000

PATENT 01/13/97

Attorney Docket No. NANO-001/05US

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on January 8, 1997.

Date: 1-8-97 By: Patricia K. Barry

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	
Charles H. Moore et al.	Examiner: David Y. Eng
Serial No. 08/484,918	Art Unit: 2315
Filed: June 7, 1995	
For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK	TRANSMITTAL FOR AMENDMENT
	Palo Alto, CA 94306

Box AF
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith is a(n) Amendment/Response in the above-identified application.

[X] Small entity status of this Application under 37 CFR 1.9 and 1.27 has been established by a Verified Declaration previously submitted.

[ ] A Verified Declaration of Small Entity Status Under 37 CFR 1.9 and 1.27 is enclosed.

Also enclosed:

[ ] Information Disclosure Statement

[ ] Declaration

[ ] Associate Power of Attorney

21235067

[X] Other: Request to Withdraw Final Rejection under 37 CFR 1.129(a)

The fees have been calculated as shown below:

FOR:	Claims after - Amend.	Claims Prev. = Paid	Extra Claims[1]	Small Entity Rate	Small Entity Fee	Other Than a Small Entity Rate	Other Than a Small Entity Fee	Total Claim Fee
Total Claims	20	15	0	$11		$22		$0.00
Independent Claims	4	4	0	$40		$80		$0.00
Multiple Dependent Claims Not Previously Presented					$130		$260	$0.00
TOTAL								$0.00

1 If difference is negative, enter "0"; if Total Claims is 20 or less, enter 0; if Independent Claims is 3 or less, enter 0.

Extension of Time	Small Entity	Other than a Small Entity
[ ] One Month	$55.00	
[ ] One Month		$110.00
[ ] Two Months	$195.00	
[ ] Two Months		$390.00
[X] Three Months	$465.00	
[ ] Three Months		$930.00
[ ] Four Months	$735.00	
[ ] Four Months		$1,470.00

Extension of Time Fee: **$465.00**

[ ] Fee regarding Information Disclosure Statement:

[ ] Fee Under 37 CFR 1.17(p) ($230.00)

[ ] Petition Fee Under 37 CFR 1.17(i)(l) ($130.00)

Total Information Disclosure Statement Fee: **$0.00**

21235067

Other fees (list individually)

Request to Withdraw Final Rejection $385.00

Total Other Fees: **$385.00**

TOTAL FEES: **$850.00**

[X] A check including the amount of the above indicated TOTAL FEES is attached.

[ ] Please charge Deposit Account No. 03-3117 in the amount of $.

[ ] A check in the amount of $ is attached.

[ ] No fee is required.

[X] Conditional Petition for Extension of Time: An extension of time is requested to provide for timely filing if an extension of time is still required after all papers filed with this transmittal have been considered.

[X] The Commissioner is hereby authorized to charge any underpayment of the following fees associated with this communication, including any necessary fees for extension of time, or credit any overpayment to Deposit Account No. 03-3117:

[X] Any filing fees under 37 CFR 1.16 including fees for the presentation of extra claims.

[X] Any patent application processing fees under 37 CFR 1.17.

A **duplicate** copy of this sheet is attached for accounting purposes.

Respectfully submitted,

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PATENT

NANO-001/05US
N0765-2008

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Charles H. Moore et al.

Serial No. 08/484,918

Filed: June 7, 1995

For: HIGH PERFORMANCE, LOW COST MICROPROCESSOR

Examiner: D. Eng

Art Unit: 2315

PROPOSED AMENDMENT

Palo Alto, CA 94306

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

This Amendment is being submitted in response to the Final Rejection dated July 8, 1996 in the above identified patent application.

IN THE CLAIMS

Please amend claims 19, 65 and 73 as follows:

19(Twice Amended). A microprocessor system, comprising a single integrated circuit including a central processing unit and a ring oscillator variable speed system clock connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices [of like type] correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit [operating at a variable processing frequency dependent upon a variable speed of] and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said integrated circuit.

65(Twice Amended). In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:

providing a ring oscillator system clock [having a plurality] constructed of [transistors] electronic devices within the integrated circuit, said [plurality of transistors] electronic devices having operating characteristics [disposed to] which will, because said ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary [similarly to] together with operating characteristics of [transistors] electronic devices included within the microprocessor; and

using the ring oscillator system clock for clocking the microprocessor, said [central processing unit] microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock.

73(Amended). A microprocessor system comprising:

a central processing unit disposed upon [a] an integrated circuit substrate, said central processing unit operating at a processing frequency and [including] constructed of a first plurality of [transistors] electronic devices;

an oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and including a second plurality of [transistors] electronic devices, thus varying the [designed such that] operating characteristics of said first plurality and said second plurality of transistors [vary] in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation.

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(Form 20426487)

17. The court has also found that a person of ordinary skill in the art reading the patent would understand that the phrase "as a function of" is describing a variable that depends on and varies with another, though not necessarily in an exact mathematical type functional relationship.

18. The term "entire oscillator" (in claims 6 and 13) is properly understood to exclude any external clock used to generate the signal used to clock the CPU.

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION and HTC AMERICA, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED,

Defendants.

Case No. 5:08-cv-00882 PSG

[Related to Case No. 5:08-CV-00877 PSG]

~~[PROPOSED]~~ ORDER GRANTING EMERGENCY MOTION FOR CLARIFICATION OF ORDER ON ADDENDUM TO JURY INSTRUCTIONS

Complaint Filed: February 8, 2008
Trial Date: September 23, 2013

Date: September 23, 2013
Time: 9:00 a.m.
Place: Courtroom 5, 4th Floor
Judge: Hon. Paul S. Grewal

Having considered Defendants' Emergency Motion for Clarification of the Order on Addendum to the Joint Proposed Jury Instructions, the record in this case and all related facts and circumstances, and good cause appearing therefor, IT IS HEREBY ORDERED THAT:

The court's final jury instructions will instruct the jury that the terms "entire ring oscillator variable speed system clock" (in claims 1 and 11), "entire oscillator" (in claims 6 and 13), and "entire variable speed clock" (in claims 10 and 16) are properly understood to exclude any external clock used to generate the signal used to clock the CPU.

IT IS SO ORDERED.

Dated: September 23, 2013

Hon. Paul S. Grewal
United States Magistrate Judge

398111 v2/CO

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

TECHNOLOGY PROPERTIES LTD. and PATRIOT SCIENTIFIC CORP., Plaintiffs,	§	
vs.	§	CIVIL ACTION NO. 2:05-CV-494 (TJW)
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD., ET AL., Defendants.	§	

MEMORANDUM OPINION AND ORDER

After considering the submissions and the arguments of counsel, the Court issues the following order concerning the claim construction issues:

I. Introduction

Plaintiffs Technology Properties Limited ("TPL") and Patriot Scientific Corp. accuse multiple defendants of infringing United States Patent Nos. 5,809,336 ("the '336 patent") entitled "High Performance Microprocessor Having Variable Speed System Clock," 6,598,148 ("the '148 patent") entitled "High Performance Microprocessor Having Variable Speed System Clock," and 5,784,584 ("the '584 patent") entitled "High Performance Microprocessor Using Instructions that Operate within Instruction Groups." This opinion resolves the parties' various claim construction disputes.

II. Background of the Technology

The '336 patent discloses a mechanism to improve the speed of microprocessor operations. First, a variable speed clock circuit is fabricated on the same chip as the microprocessor. By placing

the clock circuitry on the microprocessor, the clock will be subject to the same variations in operating conditions as the microprocessor. Second, the slower input/output clock is separated from the system clock.

The '148 patent also discloses a mechanism to improve the speed of the microprocessor. In addition to the on-chip clock described in the '336 patent, the microprocessor of the '148 patent includes memory on a majority of the microprocessor substrate.

The '584 patent addresses a bottleneck problem where the computing speed of the microprocessor depends on how quickly instructions can be loaded from memory into the instruction register of the microprocessor. Microprocessors can only process instructions as fast as the instructions can be loaded from the memory. The '584 patent discloses improvements on how to fetch and decode instructions. This is accomplished by arranging certain instructions into a group and fetching the entire group of instructions into the instruction register. As a result, the microprocessor no longer needs to wait for those instructions to be loaded from memory into the instruction register.

III. General Principles Governing Claim Construction

"A claim in a patent provides the metes and bounds of the right which the patent confers on the patentee to exclude others from making, using or selling the protected invention." *Burke, Inc. v. Bruno Indep. Living Aids, Inc.*, 183 F.3d 1334, 1340 (Fed. Cir. 1999). Claim construction is an issue of law for the court to decide. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 970-71 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996).

To ascertain the meaning of claims, the court looks to three primary sources: the claims, the specification, and the prosecution history. *Markman*, 52 F.3d at 979. Under the patent law, the

specification must contain a written description of the invention that enables one of ordinary skill in the art to make and use the invention. A patent's claims must be read in view of the specification, of which they are a part. *Id.* For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims. *Id.* "One purpose for examining the specification is to determine if the patentee has limited the scope of the claims." *Watts v. XL Sys., Inc.*, 232 F.3d 877, 882 (Fed. Cir. 2000).

Nonetheless, it is the function of the claims, not the specification, to set forth the limits of the patentee's claims. Otherwise, there would be no need for claims. *SRI Int'l v. Matsushita Elec. Corp.*, 775 F.2d 1107, 1121 (Fed. Cir. 1985) (en banc). The patentee is free to be his own lexicographer, but any special definition given to a word must be clearly set forth in the specification. *Intellicall, Inc. v. Phonometrics*, 952 F.2d 1384, 1388 (Fed. Cir. 1992). And, although the specification may indicate that certain embodiments are preferred, particular embodiments appearing in the specification will not be read into the claims when the claim language is broader than the embodiments. *Electro Med. Sys., S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 1054 (Fed. Cir. 1994).

This Court's claim construction decision must be informed by the Federal Circuit's decision in *Phillips v. AWH Corporation*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). In *Phillips*, the court set forth several guideposts that courts should follow when construing claims. In particular, the court reiterated that "the *claims* of a patent define the invention to which the patentee is entitled the right to exclude." 415 F.3d at 1312 (emphasis added) (*quoting Innova/Pure Water, Inc. v. Safari Water Filtration Systems, Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). To that end, the words used in a claim are generally given their ordinary and customary meaning. *Id.* The ordinary and customary

meaning of a claim term "is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1313. This principle of patent law flows naturally from the recognition that inventors are usually persons who are skilled in the field of the invention. The patent is addressed to and intended to be read by others skilled in the particular art. *Id.*

The primacy of claim terms notwithstanding, *Phillips* made clear that "the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." *Id.* Although the claims themselves may provide guidance as to the meaning of particular terms, those terms are part of "a fully integrated written instrument." *Id.* at 1315 (*quoting Markman*, 52 F.3d at 978). Thus, the *Phillips* court emphasized the specification as being the primary basis for construing the claims. *Id.* at 1314-17. As the Supreme Court stated long ago, "in case of doubt or ambiguity it is proper in all cases to refer back to the descriptive portions of the specification to aid in solving the doubt or in ascertaining the true intent and meaning of the language employed in the claims." *Bates v. Coe*, 98 U.S. 31, 38 (1878). In addressing the role of the specification, the *Phillips* court quoted with approval its earlier observations from *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998):

> Ultimately, the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim. The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction.

Consequently, *Phillips* emphasized the important role the specification plays in the claim construction process.

The prosecution history also continues to play an important role in claim interpretation. The prosecution history helps to demonstrate how the inventor and the PTO understood the patent. *Phillips*, 415 F.3d at 1317. Because the file history, however, "represents an ongoing negotiation between the PTO and the applicant," it may lack the clarity of the specification and thus be less useful in claim construction proceedings. *Id.* Nevertheless, the prosecution history is intrinsic evidence. That evidence is relevant to the determination of how the inventor understood the invention and whether the inventor limited the invention during prosecution by narrowing the scope of the claims.

Phillips rejected any claim construction approach that sacrificed the intrinsic record in favor of extrinsic evidence, such as dictionary definitions or expert testimony. The *en banc* court condemned the suggestion made by *Texas Digital Systems, Inc. v. Telegenix, Inc.*, 308 F.3d 1193 (Fed. Cir. 2002), that a court should discern the ordinary meaning of the claim terms (through dictionaries or otherwise) before resorting to the specification for certain limited purposes. *Id.* at 1319-24. The approach suggested by *Texas Digital*–the assignment of a limited role to the specification–was rejected as inconsistent with decisions holding the specification to be the best guide to the meaning of a disputed term. *Id.* at 1320-21. According to *Phillips*, reliance on dictionary definitions at the expense of the specification had the effect of "focus[ing] the inquiry on the abstract meaning of words rather than on the meaning of the claim terms within the context of the patent." *Id.* at 1321. *Phillips* emphasized that the patent system is based on the proposition that the claims cover only the invented subject matter. *Id.* What is described in the claims flows from the statutory requirement imposed on the patentee to describe and particularly claim what he or she has invented. *Id.* The definitions found in dictionaries, however, often flow from the editors'

objective of assembling all of the possible definitions for a word. *Id.* at 1321-22.

Phillips does not preclude all uses of dictionaries in claim construction proceedings. Instead, the court assigned dictionaries a role subordinate to the intrinsic record. In doing so, the court emphasized that claim construction issues are not resolved by any magic formula. The court did not impose any particular sequence of steps for a court to follow when it considers disputed claim language. *Id.* at 1323-25. Rather, *Phillips* held that a court must attach the appropriate weight to the intrinsic sources offered in support of a proposed claim construction, bearing in mind the general rule that the claims measure the scope of the patent grant. The court now turns to a discussion of the relevant claim terms.

IV. Discussion

Claim 1 of the '336 patent, Claim 1 of the '148 patent, and Claim 29 of the '584 patent are representative of how the terms in dispute are used in the asserted claims. Claim 1 of the '336 patent is an independent apparatus claim. It provides:

> A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.

Claim 1 of the '148 patent is an independent apparatus claim. It provides:

> A microprocessor integrated circuit comprising:
>
> a program-controlled processing unit operative in accordance with a sequence of program

instructions;

a memory coupled to said processing unit and capable of storing information provided by said processing unit;

a plurality of column latches coupled to the processing unit and the memory, wherein, during a read operation, a row of bits are read from the memory and stored in the column latch; and

a variable speed system clock having an output coupled to said processing unit;

said processing unit, said variable speed system clock, said plurality of column latches, and said memory fabricated on a single substrate, said memory using a greater area of said single substrate than said processing unit, said memory further using a majority of a total area of said single substrate.

Claim 29 of the '584 patent is a method claim. It provides:

In a microprocessor system including a central processing unit, memory, and an instruction register, a method for providing instructions and operands from said memory to said central processing unit comprising the steps of:

providing instruction groups to said instruction register from said memory wherein certain of said instruction groups include at least one instruction that, when executed, causes an access to an operand or an instruction or both, said operand or instruction being located at a predetermined position from a boundary of said instruction groups;

decoding said at least one instruction to determine said predetermined position;

locating said predetermined position; and

supplying, from said instruction groups, using the predetermined location, said operand or instruction or both to said central processing unit.

A. Agreed Construction

The parties have agreed to the construction of the following terms.

1. '336 Patent

"Oscillator" means "a circuit capable of maintaining an alternating output."

"On-chip input/output interface" means "a circuit having logic for input/output

communications, where that circuit is located on the same semiconductor substrate as the CPU (claims 1-2, 6-10) or the microprocessor (claims 3-5)."

"Integrated circuit" means "a miniature circuit on a single semiconductor substrate."

"External memory bus" means "a group of conductors coupled between the I/O interface and an external storage device."

2. '148 Patent

"Integrated circuit substrate" means "a single supporting material upon or within which is formed a miniature circuit."

3. '584 Patent

"Instruction" means "a command to a processor that tells the processor what operation to perform."

"Boundary of said instruction groups" means "beginning or end of an instruction group."

"Supplying, from said instruction groups, using the predetermined location, said operand or instruction or both to said central processing unit" means "using the results of the locating step in the step of transferring the bits from the accessed operand or instruction to the central processing unit."

"Instruction register" means "a hardware element that receives and holds an instruction group as it is extracted from memory; the register either contains or is connected to circuits that interpret the instructions in the group."

B. Disputed Constructions

1. '336 Patent

a. "central processing unit"

The first term for construction is "central processing unit." The plaintiffs propose "an electronic circuit that controls the interpretation and execution of programmed instructions." The defendants propose "the central electronic circuit in a computer that controls the interpretation and execution of programmed instructions." There are two main disputes - 1) whether the circuit needs to be in a computer and 2) whether the circuit needs to be the "central electronic circuit."

In support of their construction, the plaintiffs argue that the specification teaches that the microprocessor can be used in applications other than a computer (e.g., HDTV and automobiles). '336 patent, 9:61-10:12. The plaintiffs also observe that the specification states that the microprocessor can be part of a multiprocessor system and, therefore, no one CPU is the "central electronic circuit" for the computer. *See* '336 patent, 11:64-12:4. The defendants, on the other hand, argue that they did not intend to limit the use of the CPU to a computer. They assert, however, that a CPU must be part of a computer chip.

The parties appear to agree that one of ordinary skill in the art would understand that a computer chip or other integrated circuit can be used in various devices, such as automobiles or televisions. The Court construes the term to mean "an electronic circuit on an integrated circuit that controls the interpretation and execution of programmed instructions."

b. "microprocessor"

The plaintiffs propose "an electronic circuit that executes programmed instructions and is capable of interfacing with input/output circuitry and/or memory circuitry." The defendants propose

"an electronic circuit that uses a central processing unit to interpret and execute programmed instructions." The main disputes are whether the microprocessor must be capable of interfacing with input/output circuitry and/or memory circuitry, and whether the microprocessor needs to use a central processing unit.

The plaintiffs argue that the patent discloses a microprocessor that communicates with memory circuitry. '336 patent, 8:56-58, 11:49-54. The plaintiffs also argue that the claim language does not support the fact that a microprocessor is required to use a central processing unit because claim 3 does not recite the use of a central processing unit whereas all other independent claims require the use of a central processing unit.

The defendants argue that one of ordinary skill in the art would understand that microprocessors include a central processing unit. In addition, the defendants contend that not all microprocessors need to interface with input/output circuitry because some microprocessors communicate solely with external memory. The defendants also contend that microprocessors do not need to connect to external memory because some microprocessors rely solely on on-chip memory.

The Court is not persuaded that the additional limitations proposed by the plaintiffs or the defendants are appropriate. The input/output interface and the central processing unit limitations are included in other portions of the claims and, therefore, adding those limitations to the construction would be superfluous. *See, e.g.,* '336 patent, 32:12-13, 25-26. The Court construes "microprocessor" to mean "an electronic circuit that interprets and executes programmed instructions."

c. "ring oscillator"

The next term is "ring oscillator." The plaintiffs contend that this term means "an oscillator having a multiple, odd number of inversions arranged in a loop." The defendants propose "an [oscillator] having an odd number of inverting logic stages connected in a loop." The main dispute is whether a ring oscillator is required to have multiple inverters or whether it can have just one.

The plaintiffs argue that a single inverter would not be appropriate because it could not maintain an oscillating output. The defendants, on the other hand, rely on extrinsic evidence to support their proposed construction. Specifically, the defendants cite to a semiconductor textbook depicting a ring oscillator with only one inverter.

The plaintiffs have the better argument. The extrinsic evidence cited by the defendants also supports the plaintiffs' construction. It states that timers are built as "chains of inverters," not just one inverter. Defendants' Claim Construction Brief, Ex. U, MEAD & CONWAY, INTRODUCTION TO VLSI SYSTEMS (1980), at 234. Accordingly, the Court adopts the plaintiffs' proposed construction.

d. "an entire ring oscillator variable speed system clock in said integrated circuit"

The plaintiffs argue that this term means "a ring oscillator that generates the signal(s) used for timing the operation of the CPU, capable of operating at speeds that can change, where the ring oscillator is located entirely on the same semiconductor substrate as the CPU." The defendants' proposed construction is "a [ring oscillator variable speed system clock] that is completely on-chip and does not rely on a control signal or an external crystal/clock generator." The dispute is whether the ring oscillator may rely on a control signal or an external crystal/clock generator.

In support of their construction, the defendants argue that the applicant disclaimed use of a

control signal and a external crystal/clock generator in order to distinguish over prior art. The plaintiffs contend that it did not disclaim all types of control signals, such as voltage and current controlled oscillators; there was only a disclaimer of the more narrow "command input." In addition, the plaintiffs argue that, although an external crystal is not directly used to generate a system clock signal, the external crystal can be used as a reference signal to account for delay across certain circuit elements.

The Court agrees with the defendants that the applicant disclaimed the use of an input control signal and an external crystal/clock generator to generate a clock signal. *See* Response to Office Action, April 11, 1996, at 8; Response to Office Action, January 13, 1997, at 4; Response to Office Action, July 7, 1997, at 3-4. Accordingly, the Court construes the term to mean "a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not directly rely on a command input control signal or an external crystal/clock generator to generate a clock signal."

e. "variable speed"

The next term is "variable speed." The plaintiffs' proposed construction is "capable of operating at speeds that can change." The defendants argue that the term means "a speed (frequency) that is not tightly controlled and varies more than minimally."

The plaintiffs contend that the specification discloses a ring oscillator that is capable of operating at various speeds based on variations in operating conditions. '336 patent, 16:59-63. The plaintiffs also argue that the defendants' proposed construction is too restrictive. The defendants, on the other hand, point to the prosecution where the applicant describes fixed-frequency as a speed that is "tightly controlled" and "var[ies] minimally." Amendment, July 7, 1997, at 3-4. According

to the defendants, "variable speed" is the opposite of fixed-frequency.

Notwithstanding the defendants' arguments, one of ordinary skill in the art would understand "variable speed" to describe a component capable of operating at different speeds. Accordingly, the Court construes the term to mean "capable of operating at different speeds."

f. "system clock" and "variable speed clock"[1]

The plaintiffs propose "a circuit that generates the signal(s) used for timing the operation of the CPU." The defendants contend that the term means "a circuit that is itself responsible for determining the frequency of the signal(s) used for timing the operation of the CPU." The dispute is whether the circuit alone is responsible for determining the frequency of the signal.

A system clock does not generate the signal alone because the timing can be derived from the ring oscillator. '336 patent, 16:63-67. Accordingly, the Court adopts the plaintiffs' proposed construction.

g. "oscillator . . . clocking"

The plaintiffs contend that no construction is necessary, but if a construction is required, they propose "the oscillator generates the signal(s) used for timing the operation of the CPU." The defendants propose "an oscillator that is itself determining the frequency of the signal(s) used for timing."

The Court agrees that the term requires construction. The Court construes the term to mean "an oscillator that generates the signal(s) used for timing the operation of the CPU."

h. "processing frequency"

The plaintiffs propose "the speed at which the CPU operates." The defendants propose

[1] The parties appear to agree that these two terms should have the same construction.

"fastest safe operating speed." The issue is whether the term refers to the "fastest safe operating speed."

The plaintiffs contend that the specification uses the language "maximum possible frequency" with regard to one embodiment of the CPU. The plaintiffs also point out that "fastest safe operating speed" was mentioned in response to an office action. Response to Office Action, January 8, 1997, at 4. The response to the office action states that the present invention provides

> a variable speed clock for the microprocessor, with the clock speed varying in the same way as variations in the operating characteristics of the electronic devices making up the microprocessor. This allows the microprocessor to operate at its fastest safe operating speed, given its manufacturing process or changes in its operating temperature or voltage. *Id.* at 3-4.

According to the plaintiffs, this does not mean that the CPU must operate at the fastest safe operating speed, but that it is capable of operating at its fastest safe operating speed.

In support of their proposed construction, the defendants point to the specification which states that the "CPU will always execute at the maximum frequency possible, but never too fast." '336 patent, 17:1-2. The defendants also point to a portion of the prosecution history which states that

> these claims further state that the plurality of transistors included within the ring oscillator clock have operating characteristics which vary similarly to operating characteristics of transistors included within the microprocessor, thereby enabling the processing frequency of the microprocessor to track the speed of the ring oscillator clock: '...CPU clock 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process. Response to Office Action, April 11, 1996, at 8-9.

Frequency is not limited to the fastest safe operating speed. The portion of the prosecution history cited by the defendants refers to varying the processing frequency based on operating

conditions. In the Court's view, the applicants did not clearly define or limit the term "processing frequency." Accordingly, the Court adopts the plaintiffs' proposed construction.

i. "processing frequency capability"

The plaintiffs propose "the range of speeds at which the CPU can operate." The defendants propose "fastest safe operating speed at which the CPU can operate."

As discussed in the previous section, "processing frequency" is not limited to the "fastest safe operating speed." In addition, "capability" is not limited to a range or to the fastest speed. Accordingly, the Court construes the term to mean "the speeds at which the CPU can operate."

j. "varying together"[2]

The next term is "varying together." The plaintiffs contend that the term means "both increase or both decrease." The defendants' proposed construction is "increasing and decreasing by the same amount." The dispute is whether this term is limited to "the same amount."

The defendants claim that the only way for the invention to work is to match the clock speed to the CPU's processing speed capability. According to the defendants, if the frequency capability increased from 50 MHz to 100 MHZ but the clock rate only increased from 25 MHz to 150 MHZ, then the CPU would not be operable. In addition, the defendants argue that there are numerous statements in the prosecution history stating that the processing frequency should "track" or "vary correspondingly with" the clock rate. *See* Response to Office Action, April 11, 1996, at 6, 8; Response to Office Action, January 8, 1997, at 4.

There is no limitation in the intrinsic evidence requiring the variation between the frequency

[2] This construction would also include the terms "vary together," "varying . . . in the same way," and "varying in the same way."

capability and the clock to match exactly. The Court construes the term to mean "increasing and decreasing proportionally."

k. "second clock"

The plaintiffs' proposed construction is "a clock not derived from the first clock." The defendants contend that no construction is necessary, but if construction is necessary, then they propose "another clock."

The plaintiffs argue that the claims state that the second clock is independent of the first clock. According to the plaintiffs, a second clock derived from the first clock would not be independent as required by the claims.

The defendants appear to agree that the first clock is independent of the second clock. In any event, the independence of the second clock is required by the claim language. Accordingly, the Court declines to construe this term.

l. "external clock"

The plaintiffs propose "a clock not derived from the first clock, and which is not originated on the same semiconductor substrate upon which the entire variable speed clock is located." The defendants contend that no construction is necessary, but if a construction is necessary, then they propose "a clock not on the integrated circuit substrate."

As discussed previously, the defendants appear to agree that, like the second clock, the external clock is independent of the first clock. The plaintiffs' proposed construction includes limitations already in the claims. The Court construes "external clock" to mean "a clock not on the integrated circuit substrate."

m. "second clock independent of said ring oscillator . . . system clock" and "second clock independent of the ring oscillator system clock"

The plaintiffs propose "a change in the frequency of the ring oscillator does not affect the frequency of the second clock." The defendants propose "a second clock wherein a change in the frequency of one of the second clock or the ring oscillator system clock does not affect the frequency of the other." The dispute is whether the term "independent" means "one-way independence" or "two-way independence."

The plaintiffs argue that the specification only refers to one-way independence because it describes the situation where the I/O clock has a fixed speed while the CPU clock has a variable speed. According to the plaintiffs, there is no discussion about the situation where the I/O clock speed can be modified without affecting the CPU clock speed; the specification only states that varying the CPU clock speed would not affect the I/O clock speed.

The defendants argue that the plaintiffs' construction would conflict with the purpose of the invention of having a first clock function independently from the second clock. According to the defendants, the specification describes the first and second clock as functioning independently from one another.

The defendants have the better argument. One of ordinary skill in the art would understand the term "independence" to mean "two-way independence." Accordingly, the Court construes the term to mean "a second clock wherein a change in the frequency of either the second clock or ring oscillator system clock does not affect the frequency of the other."

n. "external clock is operative at a frequency independent of a clock frequency of said oscillator"

The plaintiffs propose "a change in the frequency of the oscillator (claims 6-9) or the variable

speed clock (claim 10) does not affect the frequency of the external clock." The defendants propose "an external clock wherein a change in the frequency of one of the external clock or oscillator does not affect the frequency of the other (claim 6)."

The Court construes the term to mean "an external clock wherein a change in the frequency of either the external clock or oscillator does not affect the frequency of the other."

o. "fixed frequency"

The plaintiffs contend that no construction is necessary, but if the court determines that a construction is needed, then they propose "a non-variable frequency." The defendants propose "having a speed that is tightly controlled and varies minimally." This term is not a technical term and can be understood according to its plain and ordinary meaning. Accordingly, the Court declines to construe this term.

2. '148 Patent

a. "processing unit"

The plaintiffs propose "an electronic circuit that controls the interpretation and execution of programmed instructions." The defendants do not appear to dispute the plaintiffs' proposal. Accordingly, the Court adopts the plaintiffs' proposed construction.

b. "memory" and "a memory"

The plaintiffs propose "all of the storage elements on the substrate and the control circuitry configured to access the storage elements." The defendants claim that this term is indefinite, but if construction is possible, they propose "an information storing array that does not include registers,

cache or column latches."[3] The main dispute appears to be whether or not memory can include registers, cache, or column latches.

The defendants contend that "memory" and "column latches" must have different meanings because when two claim terms are used, they are presumed to mean different things. *See* '148 patent, claim 1. The defendants, therefore, argue that "memory" cannot include "column latches." The defendants also point out that the specification recognizes that latches, registers and cache can exist within the CPU which is separate from the memory. *See* '148 patent, 4:5-10, 4:14-19, 5:58-60.

The plaintiffs contend that the specification describes DRAM to include registers and column latches. '148 patent, 8:65-9:4. The defendants, moreover, agree that registers, cache, and column latches may be considered part of the memory when they are included in the storage array. Defendants' Responsive Claim Construction Brief, at 34.

In the Court's view, the plaintiffs' proposal is too broad because it would include storage elements that are within the CPU. On the other hand, the defendants' proposed construction is too limiting because it would exclude registers and cache that one of ordinary skill in the art would consider to be types of memory. The claim language, however, does indicate that "memory" does not include "column latches." "Memory" and "column latches" are two distinct elements in Claim 1 of the '148 patent. The claim also states, in relevant part, that "a plurality of column latches [is] coupled to . . . the memory . . . ." '148 patent, 31:11-12. If "memory" included "column latches," then the claim would not need to specify that "column latches" are coupled to the "memory." Accordingly, the Court construes "memory" to mean "storage elements other than column latches."

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[3] The defendants do not present their arguments for indefiniteness in their claim construction briefing.

c. "total area of said single substrate" or "total area of said substrate"

The plaintiffs propose "the total surface of the supporting material upon or within which is formed an interconnected array of circuit elements." The defendants propose "area enclosed by the outermost edges of the substrate." This term is used in the context of memory which is claimed to occupy "a majority" of the "total area" of the substrate. The issue is what constitutes the "area."

The plaintiffs argue that the defendants' proposal would include areas of the substrate that are not being actively used (e.g., the sides and back of the substrate). According to the plaintiffs, the proper approach is to refer to the portion of the substrate that has active circuitry as depicted in Figure 9 of the '148 patent.

The area of the substrate refers to the top portion of the substrate, and not the sides or back. *See* '148 patent, Fig. 9. The Court construes the term to mean "the total top surface area of the substrate."

d. "area of said single substrate" or "area of said substrate"

The Court construes this term to mean "the top surface area of the substrate."

e. "variable"

This is not a technical term that requires construction and may be understood according to its plain and ordinary meaning. The Court declines to construe this term.

f. "system clock"

The Court adopts its previous construction of this term in the '336 patent. *See* Section IV(B)(1)(f).

g. "ring oscillator"

The Court adopts its previous construction of this term in the '336 patent. *See* Section IV(B)(1)(c).

h. "a ring oscillator having a variable output frequency"

The Court adopts its previous construction of "ring oscillator" in the '336 patent. *See* Section IV(B)(1)(c). No further construction of this term is necessary.

i. "the [ring oscillator] disposed on said integrated circuit substrate"

The Court adopts its previous construction of "ring oscillator" in the '336 patent. *See* Section IV(B)(1)(c). No further construction of this term is necessary.

j. "interface ports for interprocessor communication"

The plaintiffs contend that no construction is necessary. Alternatively, if a construction is needed, then the plaintiffs propose "channels through which data can be transferred between two separate processing units." The defendants propose "channels through which data is transferred between two separate processing units." The dispute is whether the interface ports may be used for purposes other than to transfer data.

The defendants argue that the plaintiffs' construction would allow the interface ports to be used for any purpose and render the words "for interprocessor communication" meaningless. The plaintiffs contend that the specification describes interface ports for use other than interprocessor communication. *See* '148 patent, 9:64-10:12.

One of ordinary skill in the art would understand that interface ports are not limited solely to the transfer of data. The Court construes the term to mean "channels through which data is allowed to be transferred between two separate processing units."

3. '584 Patent

a. "microprocessor"

The Court adopts its previous construction of this term in the '336 patent. *See* Section IV(B)(1)(b).

b. "central processing unit"

The Court adopts its previous construction of this term in the '336 patent. *See* Section IV(B)(1)(a).

c. "instruction groups"

The next term is "instruction groups." The plaintiffs' proposed construction is "sets of from 1 to a maximum number of sequential instructions, each set being provided to the instruction register as a unit and having a boundary." The defendants propose "sets of from 1 to a maximum number of sequential instructions, in which the execution of the instruction depends on each set being provided to the instruction register as a unit and in which any operand that is present must be right justified and which cannot encompass a single 32-bit traditional conventional instruction." The dispute is whether an operand that is present in the instruction group must be right justified and whether the instruction group may encompass a single 32-bit traditional conventional instruction.

The plaintiffs contend that right justified operands are a feature of the preferred embodiment. The plaintiffs also argue that the claim language was broadened during prosecution history when the language "selecting, in accordance with position in said instruction register of one of said instructions of one of said instruction groups, an operand from said one of said instruction groups" was removed from the claim. Amendment, June 12, 1997, at 6. In addition, the plaintiffs point out that the specification includes 32-bit instructions. *See* '584 patent, 20:41-42.

The defendants argue that the specification states that "operands must be right justified in the instruction register." '584 patent, 16:15-16. In addition, the defendants argue that the applicants limited operands in this manner to overcome prior art rejections. *See* Amendment, June 17, 1997, at 13; Amendment, February 5, 1998, at 7. The defendants also contend that although the specification includes 32-bit instructions, the specification never identifies a *single* 32-bit instruction as instruction *groups*. According to the defendants, the specification defines "instruction group" as "being 8-bit and 16 or 24-bit instructions." '584 patent, 23:4-7.

The specification and prosecution history refer to the fact that operands in the instruction register must be right justified. The applicants, however, did not exclude a single 32-bit instruction as an instruction group. In a preferred embodiment, a microprocessor fetches instructions "in 32-bit chunks called 4-byte instruction groups" where an "instruction group may contain from one to four instructions." '584 patent, 23:4-5, 19:18-19. If a 4-byte (or 32-bit) instruction group contains one instruction, then the instruction group may contain a single 32-bit instruction. The Court construes "instruction groups" to mean "sets of from 1 to a maximum number of sequential instructions, each set being provided to the instruction register as a unit and having a boundary, and in which any operand that is present must be right justified."

d. "operand"

The plaintiffs argue that the term means "an input to an operation specified by an instruction that is encoded as part of the instruction." The defendants propose "an input to a single operation specified by an instruction that is encoded as part of the instruction where the size of the input can vary depending on the value of the input."

The plaintiffs argue that the defendants' proposed construction would exclude a preferred

embodiment which includes fixed length operands. *See* '584 patent, 29:62-27:7. However, the plaintiffs appear to agree that the size of the input can vary.

The intrinsic evidence does not show a clear limitation where the size of the input needs to vary depending on the value of the input. The Court construes the term to mean "an input to a single operation specified by an instruction that is encoded as part of the instruction where the size of the input can vary."

e. "said instruction groups include at least one instruction that, when executed, causes an access to an operand or instruction or both"

The plaintiffs propose "the instruction being executed causes the CPU to use an immediate operand or execute a second instruction which is not the next sequential instruction." The defendants' proposed construction is "the instruction being executed causes the CPU to use data or execute a second instruction." The main dispute is whether the second instruction can be the next sequential instruction.

The plaintiffs argue that one of ordinary skill in the art would regard the normal program flow of going from one instruction to the next sequential instruction as "causing an access to an instruction." The defendants contend that the specification describes a SKIP instruction where the second instruction accessed is the next sequential instruction. '584 patent, 23:12-14. In reply, the plaintiffs contend that claim 29 refers to control flow instructions, not ordinary instructions.

The intrinsic evidence does not support the limitation proposed by the plaintiffs. Accordingly, the Court construes the term to mean "the instruction being executed causes the CPU to use an operand or execute a second instruction."

f. "said operand or instruction being located at a predetermined position from a boundary of said instruction groups"

The plaintiffs propose "the immediate operand or the instruction that is accessed has a position, relative to the beginning or end of the instruction group that includes the operand or instruction being accessed, that is determined based on a portion of an accessing instruction that identifies an operation to be performed and without reference to operand or address bits in the accessing instruction." The defendants propose "the bits forming the accessed operand or instruction either begin or end at a position defined in relation to the boundaries of the instruction group in the instruction register rather than the currently executing instruction." The principal dispute is whether the instruction group refers to the group in which the currently executing instruction is located or whether it refers to the group in which the instruction or operand being accessed is located.

The plaintiffs argue that, during prosecution, the applicants referred to the predetermined position of the *accessed* operand or instruction. *See* Supplemental Amendment, February 5, 1998, at 6-8. The plaintiffs also argue that instruction location is determined based on the particular place for instructions of that type. In addition, the plaintiffs contend that the target address specified by the instruction has no effect on the decision to begin executing at the beginning boundary of a target group.

The defendants argue that the Abstract explains the meaning of this phrase. It states

> A high-performance microprocessor system using instruction that access operands and instructions located relative to the current instruction group rather than located relative to the current instructions, as is the convention, is disclosed herein. '584 patent, Abstract.

The defendants also contend that the plaintiffs add limitations that are not supported by the intrinsic evidence.

In reply, the plaintiffs contend that the term "current" in the Abstract refers to the target group, not the accessing group. For example, one of ordinary skill in the art would, in the case of a BRANCH instruction, determine the target instruction relative to the boundary of the target group, not the accessing group.

A "predetermined position" refers to a position based on the instruction group being accessed. *See* '584 patent, 2:29-35. The Court construes the term to mean "the operand or instruction is accessed at a position defined in relation to the boundaries of the instruction group that includes the operand or instruction being accessed."

g. "decoding said at least one instruction to determine said predetermined position"

The plaintiffs contend that the term means "interpreting an instruction, in particular the portion thereof that signifies the operation to be performed, in order to identify a position relative to the beginning or end of the instruction group that includes the operand or instruction being accessed, without reference to the operand or address bits in the instruction being interpreted." The defendants propose "interpreting an instruction, in particular the portion thereof that signifies the operation to be performed, in order to identify a position relative to the beginning or end of the current instruction group."

The Court construes the term to mean "interpreting an instruction, in particular the portion therefor that signifies the operation to be performed, in order to identify a position relative to the beginning or end of the instruction group that includes the operand or instruction being accessed."

h. "locating said predetermined position"

The next term is "locating said predetermined position." The plaintiffs argue that this term

means "establishing operand or instruction supply within the instruction group that includes the operand or instruction being accessed at the predetermined position." The defendants argue that the term means "using the results of the decoding step to ascertain the address of the accessed operand or instruction by referencing the current instruction group address rather than the current executing instruction address without adding or subtracting an operand with the current Program Counter." The parties make similar arguments with regards to "predetermined position" as discussed in the previous section.

The plaintiffs oppose the additional limitation in the defendants' proposed construction of "without adding or subtracting an operand with the current Program Counter." According to the plaintiffs, this would exclude a preferred embodiment from the specification stating that the processor "treats the three operands similarly by adding or subtracting them to the current program counter." '584 patent, 11:13-15. In support of this additional limitation, the defendants argue that additions and subtractions are done only at assembly/linking and not at run time. *See* '584 patent, 20:43-50.

The defendants' construction improperly incorporates a limitation from the preferred embodiment. The Court construes the term to mean "locating the operand or instruction within the instruction group that includes the operand or instruction being accessed at the predetermined position."

V. Conclusion

The Court adopts the constructions set forth in this opinion for the disputed terms of the '336 patent, the '148 patent, and the '584 patent. The parties are ordered that they may not refer, directly or indirectly, to each other's claim construction positions in the presence of the jury. Likewise, the parties are ordered to refrain from mentioning any portion of this opinion, other than the actual

definitions adopted by the Court, in the presence of the jury. Any reference to claim construction proceedings is limited to informing the jury of the definitions adopted by the Court.

SIGNED this 15th day of June, 2007.

T. John Ward

T. JOHN WARD
UNITED STATES DISTRICT JUDGE

prior patent, U.S. Patent No. 4,503,500 ("Magar"). They said Magar does not have an oscillator integrated on the same silicon die as the CPU and therefore the patent applicants observed that the "entire oscillator" of the '336 invention needs to be physically integrated on the same silicon die as the CPU. (*Id.* at 14.)

Complainants say Respondents' construction, which precludes use of any external auxiliary crystal/clock in conjunction with the "entire ring oscillator variable speed system clock," mischaracterizes Magar and the gist of the applicants' statements in that regard because Magar's oscillator was not on the same integrated circuit as the CPU. According to the '336 invention, the claimed oscillator is an entire ring oscillator that is integrated on the same silicon die as the CPU, but there is no clear disavowal in the file history of the '336 patent that prohibits the use of an off-chip crystal for a reference signal, especially when the "entire ring oscillator" is fully integrated on the chip. (*Id.*) Similarly, according to Complainants, Respondents' attempt to add a limitation that excludes a control signal has no basis in the file history's discussion of "entire" or anywhere else in the internal record of the '336 patent. (*Id.*) Therefore, argue Complainants, there is no clear disavowal of the use of a "control signal." (*Id.*)

Respondents' arguments for their proposed construction

Respondents say the essence of the parties' dispute regarding this claim term, and those other claim terms with similar language, focuses on what the applicants needed to disclaim in order to succeed in getting their patent application issued. (RMBr. at 13.) Respondents contend that their constructions embody the clear disavowals of claim scope by the applicants during the prosecution of the '336 patent and are consistent with the teachings and criticisms of the prior art expressed in the specification. (*Id.*) These "unambiguous disclaimers and teachings" establish that the claimed "entire oscillator" and "entire clock" do not rely on any off-chip crystals, off-chip

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clock generators, or control signals. (*Id.*) Respondents say that, in contrast, Complainants' constructions ignore these clear disclaimers and teachings and fail to define what it means for a clock oscillator to be located "entirely" on the same substrate as the CPU. (*Id.*) Because the applicants clearly and unambiguously disclaimed an on-chip clock or oscillator that relies on external off-chip crystals and off-chip clock generators, Respondents argue that their construction, which embodies these disclaimers, should be adopted. (*Id.*)

Respondents say a key feature of the asserted claims is the requirement that the entire variable speed clock or oscillator be located on the same integrated circuit substrate as the CPU that is to be clocked, without having to rely on any external, fixed-frequency source, such as a crystal. (*Id.* at 14.) Consequently, the speed of the variable speed clock and the processing frequency capability of the CPU at any point in time are determined by the process, voltage, and temperature of the integrated circuit. (*Id.* (citing JXM-0001 at 16:59-60, 65-67, 17:5-10, 19-22).) The purported result of this arrangement, say Respondents, is that the performance of the CPU is optimized so that it "will always execute at the maximum frequency possible, but never too fast." (*Id.* (citing JXM-0001 at 16:67-17:2).)

Respondents say the language of the asserted claims and the teachings of the specification describe a purported improvement over the prior art method of clocking a CPU with a fixed clock whose frequency is controlled by an external fixed-speed crystal or clock generator. The specification of the '336 patent makes note that a fixed-speed clock is always set at a frequency well below the maximum potential frequency at which the CPU could operate under the optimal process, voltage, and temperature conditions because, by definition, a fixed-speed clock cannot vary in speed in response to such conditions. (*Id.* (citing JXM-0001 at 16:44-53).) This less-than-optimal design is necessary in order to adapt to instances when the CPU is operating

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under the worst of conditions with respect to process, voltage, and temperature. (*Id.*) Setting the frequency of the system at a lower-than-optimal level is inefficient, according to the teaching of the '336 patent, which the claimed invention seeks to overcome by fabricating the CPU and its clock entirely on the same substrate, so that PVT conditions will affect both the CPU and the clock alike, free of control from any external fixed-speed clocking mechanisms. (*Id.* (citing JXM-0001 at 16:44-17:10, 19-22).) Thus, the frequencies of the CPU and clock will automatically vary in response to changes in consequential PVT factors. (*Id.* at 14-15.) In light of the criticisms that were made in the '336 patent in this regard, a proper construction should account for such disclaimers because the Federal Circuit has recognized that a correct claim construction excludes from the scope of the claims those features that the specification criticizes and allegedly overcomes. (*Id.* at 15 (citing *Chicago Board Options Exch. Inc. v. Int'l Secs. Exch., LLC*, 677 F.3d 1361, 1372 (Fed. Cir. 2012)).)

Respondents point to the fact that during the prosecution of the '336 patent the applicants repeatedly distinguished their purported invention from the prior art on the basis that that their on-chip clock and oscillator do not rely on external crystals or frequency generators, as the prior art does, and therefore a proper construction should acknowledge and express this disclaimer. (*Id.*) Specifically, during the prosecution of the '336 patent the examiner issued a non-final rejection in light of Figure 2a of Magar. In his rejection, the examiner said the "CLOCK GEN" (clock generator) circuitry disclosed in that figure is fabricated on the same microprocessor substrate as the CPU, as is required in the claims of the '336 patent. (*Id.* (citing JXM-0002 at TPL-85300002433-36).) In response, the applicants attempted to distinguish Magar on the basis that an external off-chip crystal drives the clock that is disclosed in Magar. (*Id.* at 16 (citing JXM-0002 at TPL85300002426).) The applicants also emphasized that there is a difference

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between their claimed variable speed clock and the combination of a clock generator and external clock disclosed in Magar, say Respondents. (*Id.* at 16-17 (citing JXM-0002 at TPL85300002427-28).) Thus, says Respondents, in their first amendment during the course of prosecution the applicants expressly and unambiguously disclaimed clocks and oscillators that rely on an external crystal for frequency control. (*Id.* at 17.)

According to Respondents, because the patent examiner was still not convinced by this attempt to distinguish Magar, the applicants further amended their claims to explicitly require that the entire oscillator/clock be included on the same integrated circuit substrate as the CPU. (*Id.* (citing JXM-0002 at TPL85300002399-400).) Also, the applicants further attempted to distinguish Magar from their claimed invention by arguing that Magar's clock generator could not operate properly without the use of an external component, such as a crystal, and in so doing, directed the examiner to Magar's disclosure that "chip 10 includes a clock generator 17 which has two external pins, X1 and X2, to which a crystal, or external generator, is connected. (*Id.* (citing JXM-0002 at TPL85300002402).) Because Magar does not disclose what components are included in its clock generator or how it uses the signal from the crystal, the only basis for the applicants' disclaimers is Magar's reliance on the external crystal or clock generator, regardless of how the signal supplied by the external crystal or clock generator is used, say Respondents. (*Id.* at 17-18.) Further confirming the scope of their clear disclaimer, the applicants rejected any dependence on an external crystal by telling the examiner that "[w]hile most of Magar's clock (generator) circuitry is on the IC, the entire oscillator, which because it requires an external crystal, is not." (*Id.* at 18.) Once again, according to Respondents, the applicants expressly disclaimed clocks and oscillators that rely on external crystal, but this time they went even further by

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disclaiming reliance on an external crystal generally, and not just for purposes of controlling frequency. (*Id.*)

The applicants reinforced this disclaimer by explaining and characterizing "the essential difference" between Magar's fixed-frequency clock and the variable-speed clock shown in Figure 18 of the '336 patent this way:

> The signals PHASE 0, PHASE 1, PHASE 2, and PHASE 3 in Applicants Fig 18 are synonymous with Q1, Q2, Q3 and Q4 depicted in Magar Fig. 2a. The essential difference is that the frequency or rate of the PHASE 0, PHASE 1, PHASE 2 and PHASE 3 signals is determined by the processing and/or operating parameters of the integrated circuit containing the Fig. 18 circuit, while the frequency or rate of the Q1, Q2, Q3 and Q4 signals depicted in Magar Fig. 2A are determined by the fixed frequency of the external crystal connected to the circuit portion outputting the Q1, Q2, Q3, and Q4 signals shown in Magar Fig. 2a.

(*Id.* (citing JXM-0002 at TPL85300002402).) Respondents say the applicants for the'336 patent concluded their arguments to the examiner by distinguishing their invention from an external crystal used for frequency control or oscillation by saying "[t]he Magar teaching…is specifically distinguished from the instant case in that it is both fixed frequency (being crystal based) and requires an external crystal frequency generator." (*Id.* at 18-19.)

The actions of the applicants in support of the '336 patent are clear in their declarations that the invention requires an "entire" on-chip clock or oscillator, which cannot rely on an external crystal or frequency generator, say Respondents. (*Id.* at 19.) Magar's clock generator was differentiated from the '336 patent by the applicants because it is not an "entire" clock but, instead, relies on an external crystal or a frequency generator. According to Respondents, the claimed "entire" clock and "entire" oscillator cannot be construed to encompass a reliance on an external crystal or frequency generator. (*Id.* at 19-20 (citing *Southwall Tech., Inc., v. Cardinal JG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995); *Rheox, Inc.*, 276 F.3d at 1325; *Gillespie v. Dywidag, Systs. Int'l.*

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USA, 501 F.3d 1285, 1291; *Computer Docking Station Corp. v. Dell, Inc.*, 519 F.3d 1366, 1379 (Fed. Cir. 2008); *Am. Piledriving Equip. v. Geoquip, Inc.*, 634 F.3d 1324, 1336 (Fed. Cir. 2011); *Seachange Int'l, Inc. v. C-COR, Inc.*, 413 F.3d 1361, 1372-75 (Fed. Cir. 2005)).) Moreover, argue Respondents, regardless of whether either or both of these arguments was successful, or even necessary, in convincing the examiner to allow the sought-after claims, the public is entitled to rely on them. (*Id.* at 20 (citing *Elkay Mfg.*, 192 F.3d at 979).)

Respondents say that, in addition to disclaiming reliance on an external crystal or clock generator, the applicants repeatedly, clearly, and unambiguously disclaimed reliance on control signals for controlling the clock. (*Id.* at 20-21.) The first of these disclaimers concerned the examiner's rejection of the claims in light of U.S. Patent No. 4,670,837 to Sheets ("Sheets"). (*Id.* at 21.) The named inventors distinguished their invention from microprocessors that rely on frequency control information from an external clock source. (*Id.* (citing JXM-0002 at TPL85300002473).) Because the applicants referred to the "present invention" in making this disclaimer, it applies to all of the claims of the '336 patent, according to Respondents. (*Id.* (citing *Ballard Med. Prods. v. Allegiance Healthcare Corp.*, 268 F.3d 1352, 1360-62 (Fed. Cir. 2001)).)

In response to a subsequent rejection, the applicants went further and disclaimed the use of controlled oscillators altogether, regardless of whether the control is on the chip or not:

> Even if the examiner is correct that the variable clock in Sheets is in the same circuit as the microprocessor of system 100, that still does not give the claimed subject matter. In Sheets, a command input is required to change the clock speed.

(*Id.* (citing JXM-0002 at TPL85300002449).) According to the applicants' actions in this regard, simply having a CPU clock on the chip is not enough to meet the claimed invention because controlling the on-chip ring oscillator's speed by use of a command signal "does not give the claimed subject matter." (*Id.* (citing JXM-0002 at TPL85300002449).) In that same amendment,

the applicants left no doubt that, unlike "all cited references," the on-chip clock or on-chip oscillator of the invention is completely free of inputs and extra components:

> Crucial to the present invention is that …when fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together. This differs from all cited references in that…the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so.

(*Id.* at 21-22 (citing JXM-0002 at TPL85300002450).) This statement confirms the applicants' disclaimer of any reliance on control signals, argue Respondents. (*Id.* at 22.) Therefore, their constructions correctly include, and Complainants' constructions incorrectly ignore, a requirement that the clock or oscillator "not rely on…a control signal to generate a clock signal." (*Id.*)

Respondents call attention to the fact that the '336 patent was the subject of prior litigation in the United States District Court for the Eastern District of Texas, in which case the presiding judge construed the term "entire ring oscillator variable speed system clock in said single integrated circuit" as recited in claim 1 this way: "a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the CPU and does not directly rely on a command input control signal or an external crystal/clock generator to generate a clock signal." (*Id.* at 23 (citing RXM-2 at 11-12 (Markman Order in *Tech Props. Ltd. v. Matsushita Elec. Indus. Co., Ltd.*, 54 F.Supp. 2d 916, 926 (E.D. Tex. June 15, 2007))).) Respondents quote the district court judge's statement that he "agrees with the defendants that the applicant disclaimed the use of an input control signal and an external crystal/clock generator to generate a clock signal." (*Id.*) Respondents argue that their proposed construction largely mirrors the district court judge's construction. (*Id.*)

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According to Respondents, Complainant Technical Properties Limited ("TPL") has itself embraced the Texas district court judge's construction, thereby recognizing that a clear disclaimer narrows the claim scope and that the applicants disclaimed the use of an external crystal/clock or external control signals for controlling the oscillator or clock. (*Id.* at 24.) In a pending federal district court case between TPL and HTC, Acer, and Gateway in the Northern District of California (Case Nos. 5:08-cv-00877, 5:08-cv-0082, 5:08-cv-05398) TPL asked the court to adopt the Texas court judge's prior construction for the three disputed claim limitations that include the word "entire." (*Id.* (citing RXM-0003 (Joint Claim Construction Statement at Ex. B. Rows 19, 23, and 28)).) According to Respondents, it is unfairly prejudicial to them and the public for TPL to argue for construction of terms a certain way in one case and another, contrary, way in a co-pending case. (*Id.*)

Respondents say the Texas district judge's construction differs from theirs in two ways. First, it adds the word "directly" as a qualifier to the term "rely on," and second, it adds "command input" as a qualifier of "control signal." According to Respondents, the Texas court's claim construction order does not explain why its construction includes these qualifiers or what they mean; nor would a person of ordinary skill in the art understand what "directly rely on" means in the context of the claims. (*Id.* at 24-25 (citing RXM-0004 (Declaration of Dr. Vivek Subramanian in Support Respondents' Initial Markman Brief) at ¶¶ 9-10).) They argue that nothing in the prosecution history or in the patent itself limits either of the applicants' disclaimers in the manner described in the Texas court's construction, noting that the applicants explained that "Magar…is specifically distinguished from the instant case in that it is both fixed frequency (being crystal based) and requires an external crystal or external frequency generator." (*Id.* (citing JXM-0002 at TPL85300002403).) There is no suggestion of a "direct" reliance on an external crystal by reason

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of this statement, argue Respondents. (*Id.*) Similarly, they say, nothing in the following statement by the applicants limits the scope of the disclaimer to "direct" reliance on an external crystal: "one of ordinary skill in the art should readily recognize that the speed of the CPU and clock do not vary together due to manufacturing variation, operating voltage, and temperature of the IC in the Magar processor.....This is simply because the Magar microprocessor clock is frequency controlled by a crystal which is also external to the microprocessor." (*Id.* (citing JXM-0002 at TPL85300002427).) Nor, argue Respondents, does this statement limit the frequency control to direct control, and in this regard, Magar is silent as to the specific components that constitute the "clock generator" and how these components interact with the crystal inputs, much less specify that the components are controlled "directly" by control signals. (*Id.*) Similarly, when the applicants told the examiner that the "present invention...differs from all cited references in that...the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so," they disclaimed all manual or programmed control signals, not just "command input" control signals. (*Id.* at 25-26 (citing JXM-0002 at TPL85300002429).) Therefore, argue Respondents, while the Texas court correctly recognized the external crystal/clock generator and control signal disclaimers, the "directly" and "command input" qualifiers in that constructions should not be adopted for purposes of this investigation. (*Id.* at 26.)

Staff's arguments for its proposed construction

Staff notes that during prosecution of the application that resulted in the '336 patent, the applicants amended the claims so as to distinguish Magar, which discloses an on-chip clock generator that relies on an off-chip component, an external crystal, to determine clock frequency and which the applicants alleged was distinct from their invention. (SMBr. at 8 (citing JXM-0002

at TPL85300002401-02).) Similarly, in the course of distinguishing the patent to Sheets, the applicants asserted:

> The present invention does not…rely upon provision of frequency control information to an external clock, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, since the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g. temperature) affecting circuit performance.

(*Id.* (citing JXM-0002 at TPL85300002473).)

According to Staff, Complainants' proposed construction is improper to the extent it fails to reflect these disclaimers. Staff says that, while Respondents' proposed construction appears to accurately capture the applicants' clear disclaimer, Respondents still have not offered a construction of the term "entire." Staff says that incorporating a proper construction of the term "entire" excludes what was disclaimed by the applicants because the prior art that they distinguished does not disclose an entire oscillator in the same integrated circuit as a microprocessor. (*Id.* at 9.) Staff says that both Magar and Sheets disclose oscillators relying on off-chip components to determine frequency, and therefore, Staff's construction better captures the meaning of the disputed phrases as they would be understood by a person of ordinary skill in the art. (*Id.*)

Complaints' response to Respondents and Staff

Complainants maintain that the word "entire" refers to the on-chip circuitry that is used to generate the clock signal, having recognized that traditional microprocessor systems were designed such that their central processing units would operate under worse case conditions, given wide temperature and voltage swings and semiconductor processing variations. (CRMBr. at 9

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(citing JXM-0001 at 16:48-53).) Specifically, they argue, traditional CPUs relied on off-chip, fixed-speed crystals or clock generators to generate the clock signal; however, the CPU's speed capability was tied to processing variances and voltage and temperature swings. (*Id.* at 9-10.) For example, the external clock could not assume that the CPU could operate at a particular speed, because the CPUs capabilities were variable. (*Id.* at 10.) Therefore, the CPU had to be clocked at far less than its maximum operating capability to account for times when it would operate under worse case conditions. But in order to enhance CPU performance, the inventors of the '336 patent designed their microprocessor system so that the circuitry that generates the CPU clock "system clock" (ring oscillator, oscillator, variable speed clock) is fabricated on the same silicon chip as the rest of the microprocessor. (*Id.* (citing JXM-0001 at 16:57-58).) The preferred embodiment identifies the ring oscillator of the invention as the "system clock," argue Complainants. (*Id.* (citing JXM-0001 at 16:54-56).) And the terms "oscillator" and "variable speed clock" each refers to the on-chip oscillators that generate the CPU clock. (*Id.*) Because the on-chip oscillator is fabricated of transistors on the same substrate as the rest of the microprocessor, the transistors of the oscillator and the CPU will be similarly affected by manufacturing process variances, and voltage and temperature swings. (*Id.* (citing JXM-0001 at 16:63-17:10).)

Complainants say that each claim of the '336 patent includes a limitation requiring that the oscillator be deposed on the same integrated circuit as the CPU. (*Id.* at 10-11.) In each case, the claims make clear that it is the transistors or electronic components of the circuitry that generate the clock signal for the CPU that must be on the same substrate as the CPU, argue Complainants. (*Id.* at 11.) They say that during the prosecution of the '336 patent, the then-pending claims were rejected as obvious over Magar in view of U.S. Patent 4,627,082 ("Pelgrom"), and in response, the applicants, in order "to sharpen the distinction over the prior art," rewrote the independent claims

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to add the word "entire," thus "to specify that the entire ring oscillator variable speed clock, variable speed clock, or oscillator be provided in the integrated circuit." (*Id.* (citing CXM-0016 (2/8/98 Amendment) at 3).) In distinguishing the invention from the prior art, the applicants wrote this:

> Because the prior art does not provide an entire ring oscillator variable speed system clock, variable speed clock or oscillator in the integrated circuit, in that the prior art circuits require an external crystal, the prior art fails to teach or suggest the invention as now claimed.

(*Id.* (citing CXM-0016 at 3).) Therefore, reason Complainants, the phrase "entire ring oscillator variable speed system clock" in claims 1 and 11 is properly construed to mean the ring oscillator, which is inherently variable in speed, on the integrated circuit which generates the system clock. (*Id.*) This construction, they argue, is supported by the '336 patent specification, which teaches that the "[c]lock circuit is the familiar 'ring oscillator'…fabricated on the same silicon chip as the rest of the microprocessor." (*Id.* (citing JXM-0001 at 16:56-58).)

Complainants argue that, contrary to Respondents' argument, there is nothing in the patent specification that comes close to a disclaimer of all uses of off-chip crystals or clock generators; moreover, the patent does not, as Respondents contend, criticize any and all uses of the external crystals and control signals. (*Id.*) Instead, according to Complainants, the patent teaches that, by clocking the CPU using an oscillator that is disposed on the same chip as the CPU, thus enabling both components to vary with PVT parameters, the speed of the CPU need not be fixed to the worse case conditions affecting the CPU. (*Id.* at 12.)

As for the prosecution history with respect to Magar, Complainants argue that Respondents repeatedly mischaracterize the prosecution history in order to argue that all use of an external crystal and frequency generators was disclaimed by the applicants for the '336 patent. (*Id.* at

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12-13.) In particular, the Respondents assert that Magar teaches an oscillator as disclosed by an external crystal and an on-chip oscillator disclosed by the "clock gen" block. However, argue Complainants, in the file history, the applicants pointed out that Magar disclosed only one oscillator circuit, which was embodied by the external crystal. (*Id.* at 12-13.) Complainants say Respondents misuse this assertion, taken out of context, to mischaracterize the comments made by the applicants and in so doing assert that the applicants distinguished their invention from the prior art on the basis that their on-chip oscillator does not rely on an external crystal or frequency generator, without pointing out the applicants really distinguished their invention from the prior art system because Magar, unlike the invention, only had an external crystal oscillator for generating the clock signal for the system clock. (*Id.* at 13.)

Complainants say that Magar discloses an on-chip clock generator circuit "CLOCK GEN" into which is provided two signals from an off-chip crystal oscillator. (*Id.*) In a non-final rejection based on Magar, the examiner asserted that the "CLOCK GEN" circuitry was fabricated on the same microprocessor substrate as the CPU. (*Id.* (citing CXM-0015 (4/3/97 Office Action) at 2).) In response, the applicants specifically pointed out that their invention had an on-chip oscillator, unlike Magar, and was further distinguishable from Magar because an external fixed frequency crystal drives the clock disclosed in Magar: "The definitive statement that the clock gen circuit in Fig. 2a in the Magar patent is equivalent to the 'conventional crystal clock' 434 in Fig. 17 of the present application is at col. 15, lines 26-41 of Magar." (*Id.* (citing CXM-0013 (7/7/97 Amendment) at 2).)

To further clarify, argue Complainants, the applicants then quoted from their description of an embodiment of their invention which describes their variable speed clock and pointed out that "the variable speed clock is a primary point of departure from the prior art." (*Id.* (citing

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CXM-0013 at 3).) The applicants, say Complainants, explained that not only is the crystal oscillator in Magar not made on the same integrated substrate as the CPU—and therefore the Magar clock is not capable of varying with the CPU based on variations in manufacturing process, operating voltage, and temperature—but even if the crystal were formed on the same substrate, which is not possible, it would not vary in the same way as the frequency capability of the microprocessor because the oscillation frequency of the crystal oscillator is designed not to vary in response to such things as temperature, voltage, or manufacturing conditions. (*Id.*) The applicants, note Complainants, made the following statement:

> The present invention is unique in that it applies, and can only apply, in the circumstance where the oscillator or variable speed clock is fabricated on the same substrate as the driven device. The example given is a non-crystal controlled circuit, a ring oscillator. A ring oscillator will oscillate at a frequency determined by its fabrication and design and the operating environment.

(*Id.* (citing CXM-0013 at 5).) Complainants argue that the applicants went on to explain that their invention differs from the cited prior art not only because the oscillator and the CPU are on the same substrate but also because "the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so." (*Id.* (citing CXM-0013 at 5).)

According to Complainants, the applicants' remarks in response to the second office action citing Magar do not include a clear and unambiguous disclaimer. (*Id.* at 15.) Complainants argue that the patent applicants maintained that Magar disclosed only an external crystal-based oscillator, noting in their Remarks that Magar did not disclose an "entire ring oscillator variable speed system clock, variable speed clock or oscillator in the integrated circuit" and instead (and not in addition to) "the prior art circuits require an external crystal," as noted in this extract from the prosecution history:

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> Because the prior art does not provide an entire ring oscillator variable speed system clock, variable speed clock or oscillator in the integrated circuit, in that the prior art circuits require an external crystal, the prior art fails to teach or suggest the invention now claimed.

(*Id.* (citing CXM-0016 (2/8/98 Amendment) at 3).) Notably, according to Complainants, the applicants went on to emphasize that the external crystal in Magar is required for a particular purpose, oscillation of the clock:

> Magar's clock generator relies on an external crystal connected to terminals X1 and X2 to oscillate, as is conventional in microprocessor designs. It is not an entire oscillator in itself.

(*Id.* (citing CXM-0016 at 3).) The applicants also explained that in Magar the "entire oscillator" is not on the integrated circuit because "it requires an external crystal." (*Id.* (citing CXM-0016 at 4).) Then, say Complainants, the applicants pointed out that "as a self-contained on-chip circuit, Magar's clock gen is distinguished from an oscillator in at least that it lacks the crystal or external generator it requires." (*Id.*) Despite its name, Magar's "Clock Gen" is only circuitry to modify the clock speed provided by the external crystal oscillator and therefore Magar does not have an "entire" oscillator on the same circuit as the CPU because its oscillator was formed off the chip, argue Complainants. (*Id.* at 15-16.) In summarizing their points, the applicants wrote this:

> The Magar teaching is well known in the art as a conventional crystal controlled oscillator. It is specifically distinguished from the instant case in that it is both fixed-frequency (being crystal based) and requires an external crystal or external frequency generator.

(*Id.* at 16 (citing CXM-0016 at 5).) Complainants argue that the applicants were clearly pointing out that their invention does not require an external crystal oscillator or external frequency generator to generate the clock signal, and nowhere do they indicate that such components are prohibited from any embodiment that practices the invention. (*Id.*) It is clear from the file history,

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they argue, that the applicants distinguished Magar on the basis that it did not have an "entire" on-chip oscillator as claimed. Because Magar did not have any on-chip oscillator, there was no issue as to whether such an on-chip oscillator could be regulated in any fashion by external circuitry. (*Id.*) Therefore, Respondents' assertion that the applicants "clearly and unambiguously" disclaimed any reliance on an external crystal/clock generator is incorrect and should be rejected, argue Complainants.

As for Respondents' argument that the applicants clearly and unambiguously disclaimed all reliance on control signals to control the clock based on their distinction from Sheets, Complainants say this too should be rejected as an inaccurate characterization of the prosecution history regarding Sheets. (*Id.* at 16-17.) Complainants say the applicants distinguished Sheets because it did not include an on-chip oscillator because it provides frequency control information to an external clock and requires a command signal to control the external clock. (*Id.* at 17 (citing CXM-0012 (4/15/96 Amendment) at 8).) Complainants quote the following passage therefrom:

> The present invention does not simply rely upon provision of frequency control information to an external clock, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described in Sheets....Sheet's system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.

(*Id.*)

According to Complainants, the applicants made the same "requirement" distinction in response to a subsequent rejection over Sheets, wherein they said this:

> Even if the examiner is correct that the variable clock in Sheets is in the same integrated circuit as the microprocessor of system 100, that still does not give the claimed subject matter. In Sheets a command input is required to change the clock

> speed [but in] the present invention…[n]o command input is necessary to change the clock frequency.

(*Id.*)

Administrative Law Judge's findings and construction

The Administrative Law Judge finds the proposed construction of Complainants to be inadequate. They propose this definition: "a ring oscillator, variable speed system clock, wherein the ring oscillator is located entirely on the same semiconductor substrate as the central processing unit". The insertion of the two commas is not explained, as there are no commas in the patentees' syntax: "an entire ring oscillator variable speed system clock in said single integrated circuit". It appears that the Complainants are treating the phrase "variable speed system clock" which lies between the two commas as merely an appositive of the term "ring oscillator," as though the latter term is explanatory of the earlier one. This is also suggested in Complainants' arguments that the preferred embodiment identifies the ring oscillator of the invention as the "system clock," and the terms "oscillator" and "variable speed clock" each refers to the on-chip oscillators that generate the CPU clock. However, the applicants made it clear that their invention is both an oscillator and a clock:

> Applicant's prior comments apparently did not make clear the distinction between an oscillator and a clock as it applies to the Magar reference. As a self-contained on-chip circuit, Magar's clock gen is distinguished from an oscillator in at least that it lacks the crystal or external generator that it requires. Thus Magar's circuit is not an entirely on-chip oscillator as contemplated in the present case, it is only a clock.

(JXM-0016 at 4.) The applicants then said this:

> As mentioned in Applicant's previous remarks, the term clock is sometimes used interchangeably with oscillator, even inappropriately, leading to confusion. And, adding to the confusion, in the instant case, 430 is both an oscillator and a clock in the conventional senses. It is an oscillator in that it oscillates without external components (unlike the Magar reference). An example of such an

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> oscillator circuit which does not utilize external components is given in Fig. 18 of the present application. It is also a clock in Magar reference sense in that it produces the various timing signals needed of the CPU....

(*Id.*) Since, in the applicants' own words, "430," which is the "ring oscillator variable speed clock" is both an oscillator and a clock in the conventional senses, there is no reason for treating the term "variable speed system clock" as an appositive of the term "ring oscillator." Rather, the evidence points to the notion that a "ring oscillator variable speed system clock" is a grammatical unit: "both an oscillator and a clock in the conventional senses." Therefore, insofar as Complainants' insertion of the two commas is unexplained and could lead to an ambiguous and perhaps misleading construction, it is deemed improper.

The remainder of Complainants' proposed construction is found lacking because it fails to account for the actions of the applicants during the course of prosecution of the patent. They pointedly said this:

> Because the prior art does not provide an entire ring oscillator variable speed system clock, variable speed clock or oscillator in the integrated circuit, in that the prior art circuits require an external crystal, the prior art fails to teach or suggest the invention as now claimed.

(*Id.* at 3.) It is manifest therefore that the term "entire" as it was argued by the applicants to the examiner, for the very purpose of overcoming his rejection based on Magar and Pelgrom, requires that the ring oscillator variable speed system clock, as taught by the invention of the '336 patent, be on the same semiconductor substrate as the central processing unit. Magar's clock generator "is not an entire oscillator in itself" because it "relies on an external crystal connected to terminals X1 and X2 to oscillate." (*Id.*) "It is specifically distinguished from the instant case in that it is *both* fixed-frequency (being crystal based) and requires an external crystal or external frequency generator." (*Id.* at 5 (emphasis added).)

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Complainants' proposed construction does not convey the essential point made by the applicants in seeking to gain acceptance of the examiner for their purported invention by asserting that the ring oscillator variable speed clock "does not utilize external components" (JXM-0016 at 4.) On the other hand, Respondents' proposed construction does. It expresses the fact that the ring oscillator variable speed system clock is a self-contained oscillator and clock which does not utilize external components (as is disclosed in Fig. 18 of the '336 patent). Furthermore, it captures the distinction argued by the applicants in distinguishing Sheets, when they said this:

> The present invention does not similarly rely upon provision of frequency control information to an external clock, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, since the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance. Sheets' system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.

(JXM-0017 at 8.)

Although the Complainants argue that the applicants' statements during prosecution of the patent do not amount to a clear disavowal, the Administrative Law Judge finds otherwise. In *Safran v. Johnson & Johnson*, ___ F.3d___ 2013 WL 1338910 (Fed. Cir. 2012) at *7, the court said:

> To be sure, a prosecution disclaimer requires "clear and unambiguous disavowal of claim scope," *Storage Tech. Corp. v. Cisco Sys., Inc.*, 329 F.3d 823, 833 (Fed.Cir.2003), but applicants rarely submit affirmative disclaimers along the lines of "I hereby disclaim the following ..." during prosecution and need not do so to meet the applicable standard. In this case, Saffran's unqualified assertion that "the device used is a sheet" extends beyond illuminating "how the inventor understood the invention," *Phillips v. AWH Corp.*, 415 F.3d 1303, 1317 (Fed.Cir.2005) (en banc), to provide an affirmative definition for the disputed term. Given such definitive statements during prosecution, the interested public was entitled to

> conclude that the "device" recited in the claims of the '760 patent is a continuous sheet.

The same holds true here, where the applicants' unqualified statements in distinguishing Magar, Pelgrom, and Sheets support the conclusion that the entire ring oscillator is both entirely on the same semiconductor substrate as the central processing unit but also does not rely on a control signal or an external crystal/clock generator to generate a clock signal.

Although Staff's construction also addresses the point, it does so too broadly with the words "all components that determine clock frequency." How literally the word "determine" is to be applied in the context of the claim is a subject that invites further debate.

Therefore, the Administrative Law Judge concludes that the term "an entire ring oscillator variable speed system clock in said single integrated circuit" as it appears in claims 1 and 11 means "a ring oscillator variable speed system clock that is located entirely on the same semiconductor substrate as the central processing unit and does not rely on a control signal or an external crystal/clock generator to generate a clock signal".

3. Claims 6, 13—*"an entire oscillator disposed upon said integrated circuit substrate"*

The parties' proposed constructions for this term are as follows:

Respondents	Complainants	Staff
an oscillator that is located entirely on the same semiconductor substrate as the central processing unit and does not rely on a control signal or an external crystal/ clock generator to generate a clock signal	an oscillator that is located entirely on the same semiconductor substrate as the central processing unit	an oscillator that includes all components that determine oscillator frequency located on the same semiconductor substrate as the CPU

(CMBr. at 15; RMBr. at 12; SMBr. at 7.) Complainants say the parties generally agree on the construction of this phrase with the exception that the Respondents seek to add the same improper limitations as those discussed in connection with the previous claim term, and for the same reasons

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stated that:

> Magar's clock generator relies on an external crystal connected to terminals Xl and X2 to oscillate, as is conventional in microprocessor designs. It is not an entire oscillator in itself. *And with the crystal, the clock rate generated is also conventional in that it is at a fixed, not a variable, frequency. The Magar clock is comparable in operation to the conventional crystal clock* ***434*** *depicted in Fig. 17 of the present application for controlling the I/O interface at a fixed rate frequency, and not at all like the clock on which the claims are based*, as has been previously stated.
>
> ...
>
> The signals PHASE 0, PHASE 1, PHASE 2, and PHASE 3 in Applicant's Fig 18 are synonymous with Ql, Q2, Q3, and Q4 depicted in Magar Fig. 2a. *The essential difference* is that the frequency or rate of the PHASE 0, PHASE 1, PHASE 2, and PHASE 3 signals *is determined by the processing and/or operating parameters of the integrated circuit* containing the Fig. 18 circuit, while the frequency or rate of the Ql, Q2, Q3, and Q4 signals depicted in Magar Fig. 2a are *determined by the fixed frequency of the external crystal connected to the circuit* portion outputting the Ql, Q2, Q3, and Q4 signals shown in Magar Fig. 2a.
>
> The Magar teaching is well known in the art as a conventional crystal controlled oscillator. *It is specifically distinguished from the instant case in that it is* ***both*** *fixed-frequency (being crystal based)* ***and*** *requires an external crystal or external frequency generator.*

Id. at TPL853 02954559-61 (emphasis added). The patent applicants' statement in the final sentence quoted above, in particular, shows that the applicants intended to disclaim, not only an external crystal/frequency generator, but ***also*** a fixed-frequency, crystal controlled oscillator. Thus, the "entire oscillator" limitation requires both that the circuitry required to generate and/or determine (or adjust) the frequency of the oscillator's clock rate must be entirely on-chip.

The Commission, therefore, affirms the ALJ's construction of the limitation "entire oscillator" in claims 6 and 13 of the '336 patent to mean: "an oscillator that is located entirely on

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circuitry to operate." ID at 69 (emphasis added); *see also id.* at 69-73 (Respondents discussion of the so-called [ ] in the accused [ ]. The ALJ found that the so-called [ ] in the Accused Products operate only [ ] and that "[w]ithout those control signals [ ], 'oscillation unequivocally stops.'" *Id.* at 125 (citing Subramanian Tr., 1502-03).

The ALJ, however, addressed only the "current-starved" technology used in the accused [ ] chips and did not analyze the accused [ ] chips. *See* ID at 125-132. The Commission, therefore, determined to review the ID's findings concerning the "entire oscillator" limitation and posed the following question in the Notice of Review:

> With respect to the Accused Products using so-called "current-starved technology," specifically identify which accused chips are implicated, cite to the relevant evidence in the record, and discuss whether those products satisfy the "entire oscillator" limitation of claims 6 and 13 of the '336 patent.

78 *Fed. Reg.* at 71644.

b. Analysis

The parties agree that all of the [ ] chips in the Accused Products use "current-starved" technology. The parties also clarified in their submissions on review that the accused LSI chips only concerned terminated respondent Acer and are, therefore, no longer a part of the investigation. *See* 78 *Fed. Reg.* at 4 (terminating Acer). The primary dispute concerning the "entire oscillator" limitation comes down to how broadly the ALJ's construction of that limitation can be fairly read. Specifically, in responding to the Commission's request for briefing concerning the "entire oscillator" limitation, Complainants

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again argue (as they did before the ALJ) that the ring oscillators [ ] as long as they have a power supply, emphasizing the alleged difference between the PLLs in the Accused Products using an external crystal to set the frequency of the controlled oscillators and using an external crystal to generate the clock signal of the controlled oscillators.

We find that the ALJ's application of his construction of the "entire oscillator" limitation to the Accused Products was correct, including in particular his discussion of the intricate relationship between the generation and frequency of a clock signal. ID at 119-122. Specifically, the basis of the ALJ's finding concerning the reliance of the oscillators in the Accused Products on an "external crystal/clock generator" is that a "PLL controls the frequency of [a] VCO or ICO and adjusts it to match the reference frequency" and that "a PLL has circuitry that is used to set the frequency of a VCO to a multiple of another oscillator frequency functioning as a reference clock." ID at 119 (citing Oklobdzija Tr., 831, 824). The ALJ noted that Dr. Oklobdzija and his fellow authors concluded in a graduate-level textbook that, in a PLL, "the VCO generates the internal clock by virtue of a control voltage created in response to the external reference." *Id.* at 120. The ALJ found that "this process includes more than simply delivering sufficient power to enable the oscillator to oscillate[.]" *Id.* at 121. Furthermore, the ALJ found that "the process of setting the frequency of a clock signal and generating a clock signal are inseparable, because a clock signal must have a frequency, since it sole purpose is to provide a frequency for timing the operations of devices." *Id.* We affirm the ALJ's finding and analysis.

With respect to the use of "control signals," the ALJ found that "there are control signals within the PLLs themselves that are used to control the oscillation of the oscillators." *Id.* at 122

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

HTC CORPORATION AND HTC AMERICA, INC., PLAINTIFF, VS. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION AND ALLIACENSE LIMITED, DEFENDANT.	C-08-00882 PSG SAN JOSE, CALIFORNIA OCTOBER 2, 2013 VOLUME 8 PAGES 1638-1653

TRANSCRIPT OF PROCEEDINGS
BEFORE THE HONORABLE PAUL S. GREWAL
UNITED STATES MAGISTRATE JUDGE

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APPEARANCES CONTINUED ON NEXT PAGE

OFFICIAL COURT REPORTER: LEE-ANNE SHORTRIDGE, CSR, CRR
CERTIFICATE NUMBER 9595

PROCEEDINGS RECORDED BY MECHANICAL STENOGRAPHY
TRANSCRIPT PRODUCED WITH COMPUTER

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SAN JOSE, CALIFORNIA OCTOBER 2, 2013

P R O C E E D I N G S

(JURY OUT AT 9:16 A.M.)

THE COURT: MR. RIVERA, WOULD YOU CALL THE MATTER THAT'S BEEN SET FOR TRIAL?

THE CLERK: YES, YOUR HONOR. HTC CORPORATION, ET AL VERSUS TECHNOLOGY PROPERTIES LIMITED, ET AL, CASE NUMBER CV-08-882 PSG, MATTER ON FOR TRIAL.

COUNSEL, PLEASE STATE YOUR APPEARANCES.

MR. OTTESON: JIM OTTESON AND TOM CARMACK FROM AGILITY IP LAW FOR DEFENDANTS, YOUR HONOR. GOOD MORNING.

THE COURT: GOOD MORNING.

MR. LEARY: MATTHEW LEARY FOR HTC.

THE COURT: GOOD MORNING, MR. LEARY. I SEE WE HAVE THE LAST MAN STANDING.

I UNDERSTAND THAT THERE ARE SOME DEMONSTRATIVES THAT ONE OR BOTH OR ALL OF YOU WISH TO ENTER INTO THE RECORD.

MR. CARMACK?

MR. CARMACK: YES, YOUR HONOR, THANK YOU. JUST A COUPLE.

DDX-400 THROUGH DDX-403 AND DDX-71 THROUGH 74.

THE COURT: MR. LEARY, ANY OBJECTION?

MR. LEARY: NO, YOUR HONOR.

THE COURT: ALL RIGHT. THE DEMONSTRATIVES AS RECITED BY MR. CARMACK ARE AS TO BE INCLUDED IN THE RECORD, NOT

ADMITTED INTO EVIDENCE, BUT INCLUDED IN THE RECORD.

MR. CARMACK: THANK YOU, YOUR HONOR.

THE COURT: IS THERE ANYTHING ELSE I CAN HELP YOU WITH?

MR. LEARY: NO.

THE COURT: IS THAT REALLY IT?

MR. CARMACK: THAT'S IT.

THE COURT: OKAY. WELL, AS I MENTIONED YESTERDAY, YOU'RE FREE TO STAY HERE IF YOU LIKE. BUT IF YOU'D LIKE TO GO ELSEWHERE OR GET A CUP OF COFFEE, WHEREVER YOU WANT TO GO, JUST LET MR. RIVERA KNOW WHERE YOU ARE.

MR. OTTESON: THANK YOU, YOUR HONOR.

MR. LEARY: THANK YOU, YOUR HONOR.

(A RECESS WAS TAKEN PENDING THE JURY'S DELIBERATIONS.)

(JURY OUT AT 3:13 P.M.)

THE COURT: ALL RIGHT. MR. RIVERA, IF YOU WOULD CALL THE MATTER THAT'S CURRENTLY IN DELIBERATIONS?

THE CLERK: YOUR HONOR, WE ARE CALLING HTC CORPORATION, ET AL, VERSUS TECHNOLOGY PROPERTIES LIMITED, ET AL, CASE NUMBER CV-08-882 PSG.

THE COURT: ALL RIGHT. LET ME JUST ACKNOWLEDGE THE PRESENCE MR. OTTESON, MR. HOGE, MS. KEEFE, AND ALL OF THEIR COLLEAGUES. GOOD AFTERNOON.

WE HAVE TWO QUESTIONS FROM THE JURY I WANT TO REVIEW WITH YOU AT THIS TIME.

THE FIRST QUESTION IS, COURT'S DEFINITION OF "GENERATE," PAGE 26, LINES 4 AND 5.

THE SECOND QUESTION IS, CAN YOU DEFINE WHAT IS MEANT BY "OTHER PARTS" ON PAGE 29, LINE 14?

I TAKE IT THAT THE PAGE AND LINE REFERENCES IN THE QUESTIONS ARE TAKEN FROM THE WRITTEN VERSION OF THE FINAL JURY INSTRUCTIONS THAT WERE POSTED.

I WILL CONFESS, STARTING WITH THE FIRST QUESTION, THAT I AM A BIT AT A LOSS AS TO HOW MUCH FURTHER CONSTRUCTION OR META CONSTRUCTION I'M AUTHORIZED TO PERFORM TO HELP THE JURY IN THIS SITUATION.

MY UNDERSTANDING, AND I'D LIKE TO HEAR FROM EACH OF YOU, IS THAT HAVING MADE MY CONSTRUCTION IN LIGHT OF THE PROSECUTION HISTORY, THE WRITTEN DESCRIPTION AND ALL OF THAT, THE COURT'S TASK IS AT AN END AND THAT THERE'S NO AUTHORITY FROM THE FEDERAL CIRCUIT, OR ANY OTHER COURT, WHICH WOULD ALLOW THE COURT TO FURTHER DEFINE TERMS BY RE-ENGAGING IN EITHER THE INTRINSIC OR EXTRINSIC EVIDENCE.

IF EITHER OF YOU HAVE A DIFFERENT VIEW, I'M EAGER TO HEAR IT.

MR. OTTESON, I'LL LET YOU GO FIRST.

MR. OTTESON: YOUR HONOR, I THINK YOU'RE CORRECT. I THINK THE ONLY THING YOU CAN TELL THEM IS TO APPLY PLAIN AND ORDINARY MEANING.

THE COURT: OF THOSE TERMS AND CONSTRUCTION?

MR. OTTESON: OF THOSE WORDS, YES.

THE COURT: WHAT DO YOU THINK, MS. KEEFE?

MS. KEEFE: I ALSO AGREE THAT THERE'S NOTHING YOU CAN DO.

I JUST NOTE FOR THE RECORD THAT THIS IS EXACTLY WHAT WE WERE WORRIED ABOUT WHEN WE WERE ASKING FOR CLARIFICATION OF YOUR DEFINITIONS, BECAUSE IT SEEMS LIKE THE JURY IS NOW ENGAGING IN CLAIM CONSTRUCTION INSTEAD OF APPLYING FACTS.

THE COURT: YOUR PREVIOUS OBJECTION IS NOTED.

I'LL JUST MAKE THE OBSERVATION THAT THIS IS A PROBLEM INHERENT IN ANY CLAIM CONSTRUCTION, RIGHT?

MR. OTTESON: THAT'S RIGHT.

MS. KEEFE: IT CAN BE.

I THINK HERE, THOUGH, I'M NOT SURE THAT THERE IS ANYTHING THAT YOU CAN DO. IN FACT, I'M NOT SURE THAT I WOULD EVEN GO SO FAR AS TO SAY THEY HAVE TO APPLY PLAIN AND ORDINARY MEANING. I THINK YOU JUST HAVE TO SAY THAT THAT'S A QUESTION FOR THEM TO ANSWER.

THE COURT: OKAY. ALL RIGHT. WELL -- I THINK WHAT I'LL TELL THEM IS THIS, UNLESS ANYONE HAS ANY BETTER SUGGESTION. I'LL TELL THEM THAT THEY ARE TO APPLY THE DEFINITION OF "GENERATE" THAT IS CONSISTENT WITH THEIR PLAIN AND ORDINARY UNDERSTANDING OF THE TERM.

ANY OBJECTION TO THAT? I'M TRYING TO GIVE THEM SOMETHING.

MR. OTTESON: NO OBJECTION, YOUR HONOR, FROM US.

THE COURT: WHAT DO YOU THINK, MS. KEEFE?

MS. KEEFE: I THINK THE ONLY THING I MIGHT ADD IS "AND IN VIEW OF THE EVIDENCE THAT WAS PRESENTED" OR SOMETHING LIKE THAT.

OH, AND IN THE ENTIRE TERM.

MR. OTTESON: WELL, I DON'T THINK THAT'S PROPER AT ALL. I THINK THAT'S COMPLETELY IMPROPER. I THINK YOU TELL THEM TO APPLY THE PLAIN AND ORDINARY MEANING OF THE TERM IN ENGLISH.

THE COURT: ALL RIGHT. HERE'S WHAT I'LL DO: I'LL TELL THEM THAT THE COURT HAS NO FURTHER DEFINITION OF "GENERATE," PERIOD, END STOP, AND I'LL LEAVE IT AT THAT.

MS. KEEFE: THANK YOU, YOUR HONOR.

THE COURT: OKAY. AS TO THEIR SECOND QUESTION, WHICH IS, WHAT IS MEANT BY "OTHER PARTS," I'M GOING TO LOOK AT PAGE 29, LINE 14. "OTHER PARTS" KIND OF MEANS OTHER PARTS, DOESN'T IT? I'M NOT SURE WHAT ELSE I CAN SAY.

MR. WEINSTEIN: WE HAD A PROPOSAL. I THINK WHAT'S CONFUSING ABOUT -- WHAT THEY MAY BE CONFUSED ABOUT IS THAT THEY MAY NOT UNDERSTAND THAT WHEN YOUR HONOR'S INSTRUCTION IS REFERRING TO OTHER PARTS, YOU'RE REFERRING TO THINGS THAT ARE NOT RECITED IN THE CLAIM. IT'S NOT ABOUT, YOU KNOW, THE PARTS. IT'S ABOUT THINGS THAT ARE OUTSIDE THE SCOPE OF THE CLAIM.

THE PROPOSAL THAT WE HAD WAS SOMETHING ALONG THE LINES OF

1. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit, and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.

6. A microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.

7. The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

9. The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.

10. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock and wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock.

11. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology

with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein said central processing unit operates asynchronously to said input/output interface.

13. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;

an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and further wherein said central processing unit operates asynchronously to said input/output interface.

14. The microprocessor system of claim 13 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

15. The microprocessor system of claim 13 wherein said oscillator comprises a ring oscillator.

exposition thereunder, and this process includes more than simply delivering sufficient power to enable the oscillator to oscillate, as Complainants maintain.[15] The clock signal that is generated is a product of a control signal provided by the PLL and the reference frequency of the external crystal/clock. Dr. Oklobdzija and his fellow authors say a clocking system includes generation and distribution (RX-2283 at GARMIN92904), and, obviously, distribution follows generation. The distributed clocking of all of the Accused Products relies on an external crystal.

What Dr. Oklobdzija and his fellow authors said in their book coincides with Respondents' argument that the processes of setting the frequency of a clock signal and generating a clock signal are inseparable, because a clock signal must have a frequency, since its sole purpose is to provide a frequency for timing the operations of devices. (*See* RBr. at 70-71 (citing Tr. (Oklobdzija) at 1088).) Compare that with this statement from the excerpt from the book, cited above: "The phase difference between the external reference clock and the internal distributed clock is detected with the phase detector (PD), and low-pass filter (LP), to create the control voltage for the VCO, steering the oscillation frequency in order to align the external and internal clocks." Dr. Oklobdzija testified that "a clock is a control" and exerts control through repeated, periodic "start, stop, start, stop, and…do[es] it a billion times a second." (Tr. (Oklobdzija) at 413.) This periodicity is the frequency of the clock signal. In order for a clock signal to carry out its objective, it must have a frequency, which the PLL circuitry sets in reaction to a reference signal from an external crystal or clock generator. The external reference signal is integral to the generation of a clock signal, and by acknowledging that the PLL sets the

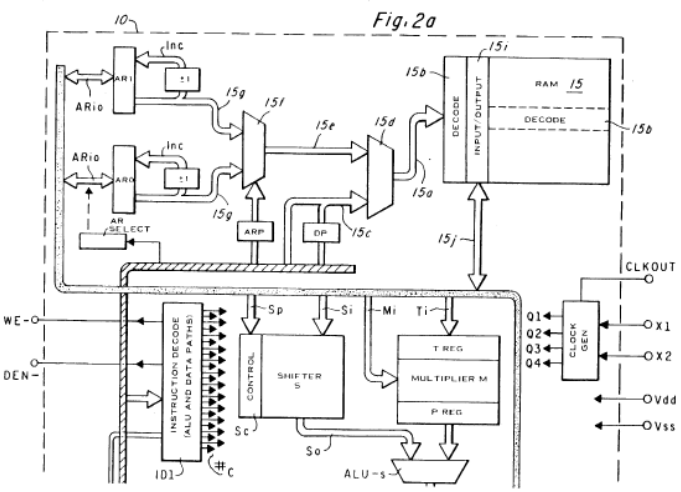
[15] The book's authors, in their Introduction, write: "The issues dealing with clock generation, frequency stability and control, and clock distribution are too numerous to be discussed in depth in this book and so they are covered only briefly." (RX-2283 at Garmin 92897.) Thus, their statements about clock generation are general, so as to provide a foundation for the principal subject of the book, but that is reason to find that their statements are fundamental to those of skill in the art in respect to clock generation, especially in light of the contrasting strictures Dr. Oklobdzija has applied to clock generation throughout this Investigation.

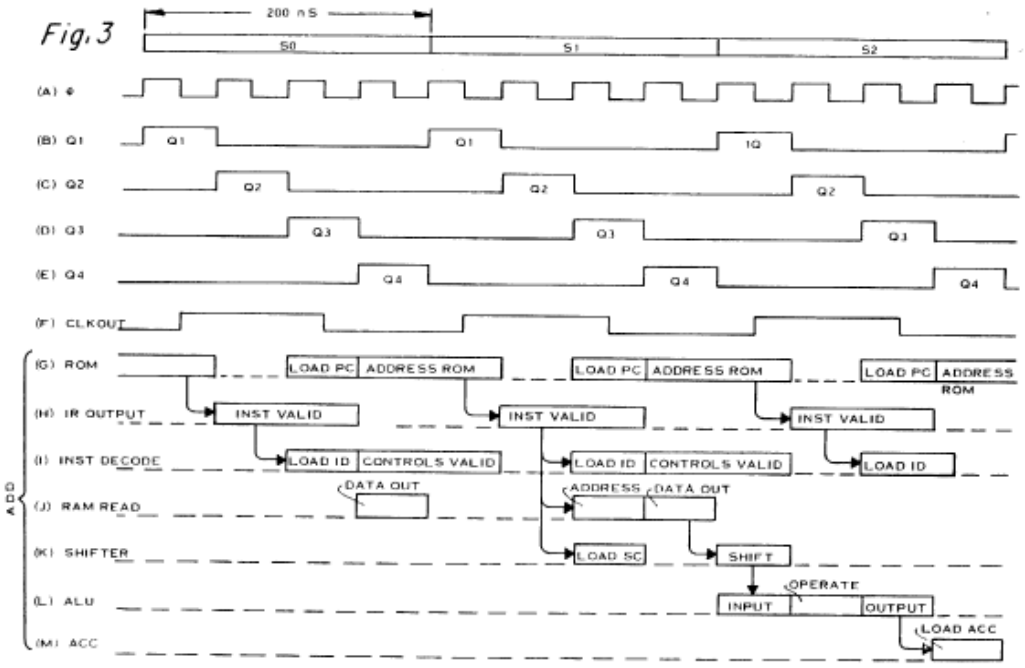
and no disclaimers were made. Without question, applicants never made any statements prohibiting the claimed on-chip oscillator that clocks the CPU from using an off-chip crystal as a reference signal, which is what Defendants seek to exclude by sleight of hand via their overly broad and vague claim construction.

1. U.S. Patent No. 4,503,500 to Magar ("Magar").

In distinguishing the claims at issue from Magar, Defendants allege that applicants disclaimed any use of an "external crystal / clock generator" to (1) "cause clock signal oscillation" or (2) "control clock signal frequency." This position, presented previously to this and other courts, is not supported by the intrinsic record. The record is clear that applicants distinguished Magar on the basis that Magar disclosed an ***external crystal*** used to ***generate*** the clock signal supplied to the CPU. Applicants further distinguished Magar on the basis that Magar's external crystal would not vary according to PVT factors.

Figures 2 and 3 of Magar demonstrate that Magar utilizes an external crystal to generate a 20MHz clock signal. That clock signal, which has a period of 50 nanoseconds, drives the on-chip "CLOCK GEN" circuitry shown below in Figure 2 and diagramed in Figure 3. Bumgardner Decl. Ex. T, U.S. Pat. No. 4,503,500 to Magar at Figs. 2a, 3, 15:23-41.





After receiving the 20MHz signal via pins X1 and X2, the "CLOCK GEN" circuitry in Magar divides the received signal from the crystal oscillator to create four quarter-cycle clocks seen in Q1-Q4. Ex. T at 15:23-35. These four, slower clock signals are each of a period of 200 nanoseconds (a 5MHz clock signal). In Magar, there is no on-chip oscillator that generates these 5MHz clock signals. Rather, the clock signal for the CPU is generated by the off-chip crystal.

In distinguishing their claims from Magar, applicants relied on limitations that are expressly included in the patent claims themselves. Specifically, applicants argued that, unlike their inventions, the oscillator detailed in Magar was not on-chip. Additionally, applicants explained that Magar's off-chip crystal and the speed of Magar's CPU would not vary together according to PVT factors. See Bumgardner Decl. Ex. U, '336 Patent, File History, Response to Office Action at 3-4 (July 7, 1997). As explained in applicants remarks, crystal oscillators do not vary (or vary minimally) due to PVT factors. Notably, both the on-chip/off-chip distinction and the PVT factor variability distinction relied upon by applicants are expressly present in the claims. Neither of these distinctions is directed to the meaning of the "entire oscillator" limitation.

In addition to the passages cited by Defendants – which when read properly show nothing more than applicants' explanation between generating a clock signal by an on-chip, electronic oscillator (as in the '336) and generating a clock signal by an off-chip crystal – applicants provided a clear, contextual meaning for their statements in the following passages:

> In making the rejection based on Magar, the examiner appears to be confusing the multiple uses and meanings of the technical term "clock." A clock is simply an electrical pulse relative to which events take place. **Conventionally, a CPU is driven by a clock that is *generated* by [a] crystal. The crystal might be connected directly to two pins on the CPU, as in Magar,** and be caused to oscillate by circuitry contained in the CPU with the aid of possible other external components . . .
>
> The present invention is unique in that it applies, and can only apply, in the circumstance *wh**ere the oscillator or variable speed clock is fabricated on the same substrate as the driven device*** . . . Thus in this example, the user designs the ring oscillator (clock) to oscillate at a frequency appropriate for the driven device when both the oscillator and the device are under specified fabrication and environmental parameters.

Id. at 4-5 (emphasis added). The critical difference explained by applicants in this passage is that the claimed oscillator used to generate clock signal is fabricated on the same chip as the CPU, and thus subject to the same PVT factors as the CPU. Nowhere in this explanation, or otherwise, do applicants state that the oscillator cannot utilize external reference signals (from fixed frequency sources or otherwise), such as in a PLL where an external crystal is used as a reference for the oscillator contained on the chip. This is consistent with Judge Grewal's previous finding that the prosecution history of the patent did not "impose a prohibition on all types of control." Bumgardner Decl. Ex. D, *HTC Corp. v. Technology Properties Ltd., et al.*, No. 3:08-cv-882, Dkt. No. 509 at 10 (August 21, 2013 - Claim Construction Order) (the "Grewal Markman Order").

After making the aforementioned argument to the examiner, the applicants again faced a rejection in light of Magar. Rather than abandon their previous arguments, applicants amended their claims to expressly require that the entire oscillator is present on the integrated circuit. This amendment clarifies the distinction that applicants were making over Magar, namely that circuitry sufficient to create a clock signal must be found on the same substrate as the CPU, thus making it subject to the same PVT factors of variability (*e.g.*, temperature). In explanation of

their amendment, applicants wrote:

> [T]he independent claims have been rewritten to specify that the ***entire*** ring oscillator variable speed system clock, variable speed clock or oscillator ***be provided in the integrated circuit***, in order to sharpen the distinction over the prior art . . . ***[T]he prior art circuits require an external crystal*** . . .
>
> ***Magar's clock generator relies on an external crystal connected to terminals X1 and X2 to oscillate***, as is conventional in microprocessor designs. It is not an entire oscillator in itself.

Bumgardner Decl. Ex. U, '336 Patent, File History, Response to Office Action at 3 (February 10, 1998).

The applicants correctly observed that Magar "requires" an external crystal to oscillate and generate a clock signal. *Id*. at 4 (Magar "***requires*** an external crystal"; Magar's "clock gen" block "lacks the crystal or external generator that it ***requires***"); *id*. at 5 (Magar "***requires*** an external crystal or external frequency generator"). Notably, applicants pointed out that the oscillator of the claims at issue must be on-chip. Thus, the file history is clear that the applicants made a critical distinction between Magar (and similar references) and the '336 invention: the oscillator that ***generates*** the CPU clock in Magar is an off-chip crystal, while the oscillator that ***generates*** the CPU clock in the '336 invention is an on-chip, electronic oscillator. The file history never discussed – much less disclaimed – the use of PLL circuitry (including an off-chip reference crystal) to adjust the frequency of a clock signal that was already ***generated*** by an on-chip oscillator.

Notably, the distinctions over Magar relied upon by the applicants are found in the claims themselves. Claim 6 expressly requires the "entire oscillator disposed upon said integrated circuit substrate and connected to said [CPU]." The parties' constructions are already in agreement that the "entire oscillator" is "located entirely on the same semiconductor substrate as the [CPU]." And claim 6 already requires PVT variability, reciting "varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated semiconductor substrate…." The point is that the claims themselves already contain the distinctions relied upon by applicants in

distinguishing Magar. There is no factual (or legal) basis for inserting the vague and broad disclaimers advocated by Defendants in the "entire oscillator" construction.

Defendants' citations to the prosecution history distort the statements actually made by applicants with regard to Magar. Regarding the first and second cited passages from the prosecution history (found on pages 8 and 9 of Defendants' Brief[3]), Defendants erroneously claim that "applicants ***expressly and unambiguously disclaimed*** oscillators that rely on an external crystal for ***frequency control.***" Defts' Brief at 9 (emphasis in original). This statement does not comport with what applicants actually said in the passages relied upon by Defendants. In the first passage cited by Defendants, applicants distinguished Magar on the basis that it used an external clock to drive the CPU:

> A review of the Magar reference shows that it is apparently no more pertinent than prior art acknowledged in the application, in that ***the clock disclosed in the Magar reference is in fact driven by a fixed frequency crystal, which is external to the Magar integrated circuit***.

Defts' Brief at 8 (emphasis in Defts' Brief). Nothing in this passage pertains to "frequency control," whatever Defendants' mean by this phrase. The clear distinction made by applicants is Magar's lack of an on-chip oscillator.

In the second passage cited by Defendants, applicants again distinguish Magar on the basis of Magar's use of an off-chip crystal:

> Contrary to the Examiner's assertion in the rejection that 'one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock vary together due to manufacturing variation, operating voltage and temperature of the IC [integrated circuit],' one of ordinary skill in the art should readily recognize that the speed of the CPU and clock ***do not*** vary together due to manufacturing variation, operating voltage, and temperature of the IC in the Magar processor . . . ***This is simply because the Magar microprocessor clock is frequency controlled by a crystal which is also external to the microprocessor***. Crystals are by design fixed frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in

[3] *Technology Properties Ltd. et al. v. Samsung Electronics, et al.*, No.3:12-cv-3877, Dkt. 94 (hereinafter "Defts' Brief).

> manufacturing, operating voltage and temperature. ***The Magar microprocessor in no way contemplates a variable speed clock as claimed***.

Defts' Brief at 8-9 (emphasis in Defts' Brief). The applicants' statement that "the Magar microprocessor clock is frequency controlled by a crystal which is also external to the microprocessor" merely points out that, unlike the claims at issue, the signal used to clock the on-chip CPU in Magar is provided by an external crystal. The portions of applicants' statements highlighted in Defendants' brief are certainly not a clear and unequivocal disclaimer pertaining to any notion of "frequency control" and cannot be extended to support Defendants' construction that the claimed oscillator does "not rely on a ***control signal*** or an external crystal clock to … ***control*** clock signal frequency." In fact, these passages say absolutely nothing about whether an on-chip oscillator (which clocks the on-chip CPU) could rely on an external crystal for "frequency control." There is simply no "unmistakable" disavowal present in these passages.

Defendants next cite to portions of the prosecution history where applicants correctly distinguish their claims from the Magar on the basis that crystals are not subject to PVT factors, such as temperature:

> ***[C]rystal oscillators have never***, to Applicants' knowledge, ***been fabricated on a single silicon substrate with a CPU***, for instance. ***Even if they were***, as previously mentioned, crystals are by design fixed-frequency devices whose oscillation frequency is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. ***The oscillation frequency of a crystal on the same substrate with the microprocessor would inherently not vary due to variations in manufacturing, operating voltage and temperature in the same way as the frequency capability of the microprocessor on the same underlying substrate, as claimed.***

Defts' Brief at 9 (emphasis in Defts' Brief). Defendants disingenuously misconstrue this passage as an "express disclaimer" that "the claims exclude oscillators using crystals to control frequency of the clock signal." *Id.* This alleged sweeping disclaimer is found nowhere in the cited passage. It is simply not there. What is stated in this prosecution history is that a crystal clock's frequency would not vary as a function of PVT like the "microprocessor on the same underlying substrate, ***as claimed***." And as set forth above, what is ***claimed*** is an "entire oscillator" whose frequency varies along with that of the CPU according to PVT factors.

In the next passage of prosecution history cited by Defendants, applicants again distinguish the claims' on-chip electronic oscillator from Magar's use of an external crystal. Defts' Brief at 10. Applicants pointed out that, in their inventions, the signals are subject to variation due to PVT factors while in Magar the signals are "determined by the fixed frequency of the external clock." Nothing in this passage remotely addresses the issue of whether the patent's "entire oscillator" may utilize an external crystal as a reference signal. Nor could this passage legally support a sweeping disclaimer as to "control of the 'frequency or rate' of the clock."

In the final passage of Magar cited by Defendants, applicants again distinguish their invention from Magar on the basis of Magar's use of an external crystal (i.e. lack of an on-chip oscillator), whose frequency is not subject to PVT factors:

> Magar's clock generator ***relies on an external crystal*** connected to terminals X1 and X2 to oscillate, as is conventional in microprocessor designs. It is not an entire oscillator in itself. And with the crystal, ***the clock rate generated is also conventional in that it is a fixed, not a variable, frequency***. The Magar clock is comparable in operation to the conventional crystal clock 434 depicted in Fig. 17 of the present application for controlling the I/O interface ***at a fixed rate frequency, and not at all like the clock on which the claims are based***, as has been previously stated.

Defts' Brief, p. 10 (emphasis in Defendants' Brief). Defendants cite this passage for the alleged disclaimer that the oscillator may not "rely on a control signal or an external crystal/clock generator to ***cause clock signal oscillation***…." But this passage makes no such disclaimer, let alone one that is clear, unambiguous and unmistakable. Applicants are merely pointing out that Magar does not disclose an on-chip oscillator.

It is not entirely clear why Defendants seek to use the language "cause clock signal oscillation," thereby deviating from this Court's jury instruction that the claims exclude "any external clock used to ***generate*** a signal." Plaintiffs strongly suspect that Defendants seek to replace "generate" with "cause clock signal oscillation" in order to lodge a non-infringement argument that goes beyond Judge Grewal's prohibition and has nothing to do with the differences between the claims at issue and Magar. In any event, there is no basis for including a vague and broad disclaimer relating to "causing clock signal oscillation" because the prosecution history

does not clearly and unmistakably include this prohibition. To the extent there is any disclaimer arising from Magar, Judge Grewal's HTC jury instruction (as well as the express claim language itself) accurately addresses the scope of the invention.

2. U.S. Patent No. 4,670,837 to Sheets ("Sheets").

Prior to facing a rejection under Magar, applicants faced a rejection based on Sheets. Like Magar, Sheets differed drastically from the claimed inventions of the '336 patent. Sheets did not contain an on-chip oscillator, and it relied upon a technique for adjusting the frequency of a voltage control oscillator by writing a "digital word" from the microprocessor to the voltage control oscillator indicative of the desired operating frequency as a means of adjusting the clock frequency.

Applicants wrote:

> The present invention does not similarly rely upon provision of frequency control information to an **external clock**, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. . . Sheets' system for providing clock control signals to an **external clock** is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.

Bumgardner Decl. Ex. V, '336 Patent, File History, Office Action Response at 8 (April 11, 1996).

In a subsequent amendment, the applicants noted that the Sheets clock "***required***" a "digital word" or "command input." By contrast, in the '336 inventions, "both the variable speed clock and the microprocessor ***are fabricated together in the same integrated circuit***. No command input is ***necessary*** to change the clock frequency." Bumgardner Decl. Ex. W, ''336 Patent, File History, Office Action Response at 4 (Jan. 7, 1997). Thus, the applicants distinguished Sheets on at least two bases: (1) unlike the '336 invention, Sheets lacked an on-chip clock/oscillator; and (2) the off-chip clock in Sheets ***required*** a "digital word"/"command input" to vary clock frequency (i.e. it did not vary according to PVT factors). These distinctions do not come close to constituting a disclaimer of any "control signal" for any purpose. Indeed, the analog voltage and/or current supplied to a ring oscillator in a PLL is nothing like the "digital

command word" in Sheets. For example, while a ring oscillator may need power to oscillate (*i.e.*, analog voltage/current), it does not have the ability to accept a "digital command word" – nor could it be "***required***" to do so. Further, as discussed above, nothing said in overcoming the Magar reference prevents the use of external reference signals.

The citations Defendants make to the prosecution history once again attempt to remove statements from the context under which they were made. The clear, contextual meaning of applicants' statements is a narrow distinction over the cited reference, not broad disclaimer as alleged by Defendants. In the first passage cited by Defendants, applicants distinguished Sheets on the basis that Sheets discloses an external clock that would not vary according to PVT factors:

> The present invention does not similarly rely upon provision of frequency control information ***to an external clock***, but instead contemplates providing a ring oscillator clock and the microprocessor ***within the same integrated circuit***. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, ***since the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance***. Sheets' system for providing clock control signals to ***an external clock*** is thus seen to be unrelated to the ***integral microprocessor/clock system of the present invention***.

Defts' Brief at 12 (emphasis added by Plaintiffs). Unlike Sheets, the claims at issue contain an on-chip electronic oscillator that naturally varies according to PVT factors. Sheets, on the other hand, apparently varied frequency according to a "digital word"/"command input." Remarkably, Defendants cite the above passage for the proposition that applicants clearly and unmistakably disclaimed all "reliance on control signals." There is no such broad disclaimer present in this passage.

In the second passage cited by Defendants, applicants again distinguished Sheets on the basis that the Sheets clock does not vary according to PVT factors:

> Even if the examiner is correct that the variable clock in Sheets is in the same circuit as the microprocessor of system 100, that still does not give the claimed subject matter. ***In Sheets, a command input is required to change the clock speed. In the present invention, the clock speed varies correspondingly to variations in operating parameters*** . . . No command input is necessary to

> change the clock frequency.

Defts' Brief, pp. 12-13 (emphasis by Plaintiffs). Once again, applicants pointed out that Sheets does not disclose a clock (whether on-chip or off-chip) whose frequency varies according to PVT factors, a requirement of the claim. There is simply no broad disclaimer of all "reliance on control signals" present in this passage.

In the final passage cited by Defendants, applicants again distinguished Sheets on the basis of PVT variation, noting that the on-chip oscillator and on-chip CPU must both vary frequencies according to PVT factors:

> ***Crucial to the present invention is that . . . when fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together***. This differs from all cited references in that . . . the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so.

Defts' Brief at 13 (emphasis by Plaintiffs). Applicants noted that Sheets, on the other hand, required "manual or programmed inputs or external or extra components" to vary its oscillator. In this passage, there is no disclaimer of "reliance on control signals." These words appear nowhere in this passage.

At the end of the day, all of Defendants' accused products contain an on-chip, electronic oscillator that varies according to PVT factors. Defendants improperly seek to exclude the accused oscillators' use of an external crystal as a reference signal by seeking a vague, broad, and improper disclaimer as to "reliance on control signals." As set forth above, applicants' response to Sheets does not make any such disclaimer, as applicants relied on express claim limitations (on-chip vs. off-chip, PVT factor variation) to distinguish the reference. It cannot be disputed that there is no unmistakable disclaimer of the on-chip, electronic oscillator using on an off-chip crystal oscillator as a reference signal in applicants' response to Sheets. Applicants' remarks regarding Sheets contain no such disclaimer.

B. The specification does not support Defendants' disclaimer arguments.

Recognizing the weakness of their prosecution history arguments, Defendants next argue that "the specification disclaims the prior art's fixed-speed clocks (which rely on a crystal, clock,

or signal to control the on-chip oscillator's frequency)…." Defts' Brief, p. 14. Defendants' specification-based disclaimer argument, however, is factually inaccurate and the case law cited by Defendants do not support a finding of disclaimer.

First, Defendants misrepresent the specification by claiming that "the specification criticizes prior art solutions that clocked a CPU with a fixed clock, such as, for example, a clock whose frequency is controlled by an external crystal." *Id.* at 13 (citing '336 patent, 16:48-53 and 17:12-23). This argument is ***highly misleading***, as ***nowhere*** in the passages cited by Defendants does the specification discuss "a clock whose frequency is ***controlled*** by an external crystal." The passages cited by Defendants merely make reference to a "traditional CPU design," which as applicants pointed out in distinguishing Magar involves the use of an off-chip crystal to ***generate*** the actual clock signal for an on-chip CPU. The specification excerpts cited by Defendants do not discuss using an off-chip crystal to ***control*** an on-chip oscillator. Therefore, this passage cannot be read to support the sweeping disclaimer advocated by Defendants. Moreover, the fact that the patent was critical of using an off-chip crystal to generate the actual clock signal for the CPU is of no consequence to this claim construction proceeding as the claims themselves clearly exclude such a scenario from infringement (*i.e.*, the "entire oscillator" must be "located entirely on the same semiconductor substrate as the [CPU]").

Second, Defendants make another misleading statement - "[r]ejecting the prior art fixed-speed clock approach (***which is the approach used in the Defendants' accused products***), the '336 patent discloses a variable-speed oscillator that is completely on the same semiconductor substrate as the CPU and whose speed freely varies with the PVT parameters of the substrate." Defts' Brief at 13-14 (emphasis by Plaintiffs). Contrary to this assertion, Defendants' accused products employ a technique called "dynamic frequency scaling", whereby the frequency of the clock signal generated by an on-chip oscillator and supplied to the CPU is increased during periods of high activity (so that the accused device can quickly respond to user inputs and be perceived as "high performance"), and decreased during periods of low activity (to conserve battery life and reduce power consumption). This oscillator is on the same semiconductor as the CPU and does vary with PVT. What Defendants hope to accomplish is to exclude the oscillators'

use of an external crystal as a reference signal. But, this situation is not addressed by the patent specification, much less disclaimed.

Third, Defendants again overplay their hand by stating that "applicants chose to use a variable speed oscillator – which varies and is 'determined by' PVT parameters – rather than the ***prior art's fixed speed clocks – which did not vary with the PVT parameters because their frequency was 'fixed' by an external crystal or control signal***." *Id.* at 14 (emphasis by Plaintiffs). Again, this statement is misleading as the prior art contemplated by the specification did not involve an on-chip oscillator "whose frequency was 'fixed' by an external crystal or control signal." In the prior art contemplated by the patent, an off-chip crystal oscillator was the oscillator that clocked the CPU. Because using a crystal oscillator to "control" a different, on-chip oscillator was not discussed or contemplated by the specification, there can certainly be no disclaimer of this scenario.

These erroneous statements by Defendants are not sufficient to meet the high bar required to show clear and unmistakable disclaimer, and the cases cited by Defendants involved far different factual scenarios. For example, in *Chicago Bd. Options Exch. Inc. v. Int'l Secs. Exch. LLC*, the court found that the specification "goes well beyond expressing the patentee's preference" and that the patentee's "***repeated derogatory statements*** … may be viewed as a disavowal of that subject matter from the scope of the Patent's claims." 677 F3d 1361, 1372 (Fed. Cir. 2012). By contrast, the '336 patent does not clearly and unambiguously criticize (much less "repeatedly criticize") use of "a control signal or an external crystal/clock generator to cause clock signal oscillation or control clock signal frequency." In fact, this situation is completely unaddressed in the passages cited by Defendants. And while the patent specification does distinguish the invention from prior art systems (like Magar) that used an external crystal to generate the signal used to clock the CPU, this type of system is specifically excluded by virtue of limitations already present in the claims (i.e., the on-chip and PVT variation limitations).

Finally, Defendants claim that the *title* of the patent controls how the Court should interpret the patent. Yet Defendants cite to no law for this proposition. Indeed they cannot – "[i]t is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the

patentee is entitled the right to exclude.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citations omitted). Here, the claims do not state that there can be no use of an external element such as an off-chip crystal as a reference for the clock. The claims only require that an entire oscillator be disposed on the same integrated circuit as the CPU and vary according to PVT factors. This is entirely consistent with the specification passages cited by Defendants, and there is no basis for finding disclaimer going beyond the limitations expressly present in the claims.

C. The Claim Language Speaks for Itself

Defendants next argue that the presence of other elements within the claim should dictate the meaning of the *entire oscillator* term. They argue that if an entire oscillator clocks a CPU at a clock rate which varies in the same way as a function of parameter variation in one or more fabrication or operation parameters associated with the integrated circuit substrate, it cannot use an external crystal or clock generator as a reference, because such reference would not permit the oscillator to vary.

As an initial matter, the argument is technically incorrect. Even if an external crystal is used to later adjust the output of an oscillator, the fact is that the frequency output by the oscillator itself does vary as a function of parameter variation. The addition of other elements, such as an external crystal, to an infringing entire oscillator, does not change the fundamental nature of the oscillator itself.

Further, the claim language speaks for itself. Whether an accused oscillator satisfies the "entire oscillator" element of the claim and also meets other claim limitations (such as the parameter variation requirements) is not an issue for claim construction, but instead a factual argument for trial. Importing the parameter variation requirements into the entire oscillator claim element is unnecessary, renders the parameter variation language redundant, and is not properly handled in the claim construction phase.

D. Defendants' Construction is Not Consistent with Prior Constructions

As explained in Plaintiffs' opening brief, adoption of the negative limitations proposed by Defendants would be a major departure from this Court's prior treatment of the *entire oscillator*

(Counsel listed on signature page)

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. HUAWEI TECHNOLOGIES CO., LTD., HUAWEI DEVICE CO., LTD., HUAWEI DEVICE USA INC., FUTUREWEI TECHNOLOGIES, INC., HUAWEI TECHNOLOGIES USA INC., Defendants.	Case No. 3:12-cv-03865-VC (PSG) **PLAINITIFFS' MOTION FOR DE NOVO DETERMINATION OF DISPOSITIVE MATTER REFERRED TO MAGISTRATE JUDGE, OR, IN THE ALTERNATIVE, MOTION FOR RELIEF FROM NONDISPOSITIVE PRETRIAL ORDER OF MAGISTRATE JUDGE** **DATE:** **Nov. 19, 2015** **TIME:** **10:00am** **PLACE:** **Courtroom 4** **JUDGE:** **Hon. Vince Chhabria**
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. ZTE CORPORATION and ZTE (USA) INC., Defendants.	Case No. 3:12-cv-03876-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. SAMSUNG ELECTRONICS CO., LTD. and SAMSUNG ELECTRONICS AMERICA, INC., Defendants.	Case No. 3:12-cv-03877-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. LG ELECTRONICS, INC. and LG ELECTRONICS U.S.A., INC., Defendants.	Case No. 3:12-cv-03880-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. NINTENDO CO., LTD. and NINTENDO OF AMERICA, INC., Defendants.	Case No. 3:12-cv-03881-VC (PSG)

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NOTICE OF MOTION AND MOTION

TO THE COURT AND ALL COUNSEL OF RECORD:

NOTICE IS HEREBY GIVEN that on November 19, 2015, at 10:00 AM, or as soon thereafter as counsel may be heard in Courtroom 4 of the above-titled court, located at 450 Golden Gate Avenue San Francisco, CA 94102, Plaintiffs will and hereby do move the Court for a *de novo* determination of dispositive matter referred to magistrate judge, or, in the alternative, motion for relief from non-dispositive pretrial order of magistrate judge, pursuant to Civil L.R. 72.

This motion is based upon this notice, the accompanying memorandum of points and authorities, the accompanying declaration of Barry Bumgardner, all pleadings, papers and records on file in this action, including the record of the *Markman* hearing held in front of Judge Paul Grewal on September 18, 2015, and any oral argument presented at the hearing on this matter.

STATEMENT OF RELIEF

For the reasons set forth below, Plaintiffs seek a *de novo* review of the Report & Recommendation of Judge Grewal regarding his construction of the term "entire oscillator."

MEMORANDUM IN SUPPORT

I. INTRODUCTION

On September 22, 2015, Judge Grewal issued a "Claim Construction Report and Recommendation" (hereinafter the "R&R") construing the term "entire oscillator disposed upon said integrated circuit substrate" of U.S. Pat. No. 5,809,336 (the "'336 Patent"). See Ex. A[1] (Dkt. 104,[2] Report & Recommendation). Judge Grewal's R&R improperly finds disclaimer associated with the "entire oscillator" term where none exists, and, importantly, has the effect of granting summary judgment of non-infringement in favor of the Defendants in each of the above-styled

[1] All exhibits cited in this brief are attached to the accompanying Declaration of Barry J. Bumgardner in Support of Plaintiffs' Motion for De Novo Determination.

[2] Unless otherwise indicated, docket numbers refer to documents from *Technology Properties Ltd., et al. v. Samsung Electronics Co., Ltd.*, Case. No. 3:12-cv-3877.

cases. In addition, even if subject matter was disclaimed during the prosecution of the '336 Patent, the disclaimer certainly is not as broad as the one described in the R&R. As a result of the dispositive nature of this issue, Plaintiffs move for a *de novo* determination of the meaning of the "entire oscillator" term. Should the Court consider the R&R to be non-dispositive, Plaintiffs move in the alternative that the Court find that Judge Grewal's R&R was clearly erroneous.

In the parties' claim construction briefing, both Defendants (who submitted a joint claim construction brief) and Plaintiffs agreed principally on the meaning of the sole disputed term, an "entire oscillator disposed upon said integrated circuit" as "an oscillator that is located entirely on the same semiconductor substrate as the central processing unit." Plaintiffs argued this should have been the complete construction of the term. Defendants, on the other hand, argued that the construction should include additional language – "and does not rely on a control signal or an external crystal/clock generator to cause clock signal oscillation or control clock signal frequency" – to reflect subject matter that was "disclaimed" during the prosecution of the '336 Patent. Ultimately, Judge Grewal agreed with the parties as to what the "entire oscillator" was – "an oscillator that is located entirely on the same semiconductor substrate as the central processing unit", but came to his own conclusion as to the disclaimer, finding that the claimed "entire oscillator" was one "that does not require a control signal and whose frequency is not fixed by any external crystal." Plaintiffs object to Judge Grewal's claim construction.

II. PROCEDURAL POSTURE

Each of the above-styled cases (collectively, the "California Actions") is a civil action alleging infringement of the '336 Patent. The suits, originally filed on July 24, 2012, were stayed pending an investigation at the International Trade Commission (the "ITC Investigation"). The ITC Investigation concluded on March 21, 2014, after which the stay was lifted in the California Actions. In addition to the ITC Investigation and California Actions, a trial was held in the Northern District of California, with Plaintiff HTC Corp. seeking a declaratory judgment of non-infringement and Defendants (the Plaintiffs in the California Actions) pursuing a counterclaim of infringement. The trial, held in front of Judge Grewal, resulted in a jury finding of infringement of certain HTC products. While on appeal, Plaintiffs and HTC settled their

dispute. On October 17, 2014, the California Actions subject to the present motion were consolidated in front of Judge Grewal for pretrial matters. See Dkt. 16.

After the parties exchanged simultaneous opening and responsive claim construction briefs (See, Exs. B-E, Dkts. 94, 95, 96, and 97), a *Markman* hearing was held on September 18, 2015, in front of Judge Grewal. On September 22, Judge Grewal issued his R&R, providing a construction of the "entire oscillator" term. As a result of this ruling, Plaintiffs and four of the five Defendants (excepting Huawei) agreed to move to stay the underlying actions, with the exception of claim construction objections, and stipulated that under the construction recommended by Judge Grewal in the R&R, "all accused products of all [moving Defendants] do not infringe the asserted claims."[3] See Ex. F, Dkt. 105 ("Joint Motion to Stay").

III. OVERVIEW OF THE '336 PATENT

The '336 Patent issued on September 15, 1998 and is based on an application filed on August 3, 1989. See Ex. H, U.S. Pat. No. 5,809,336. While pending at the United States Patent and Trademark Office ("USPTO"), the patent examiner contested the patentability of the pending claims, issuing four rejections prior to ultimately granting the patent. Applicants responded by distinguishing the claims of the '336 Patent from the cited references. After adding the limitations of a then pending dependent claim regarding a second independent clock for clocking external devices at the behest of the patent examiner, the application was allowed. The '336 Patent has been involved in litigation both in this district and the Eastern District of Texas, as well as at the ITC. It has been the subject of six reexamination requests, resulting in two reexaminations certificates. In total, the '336 Patent has already overcome more than 600 prior art references that were raised against it during prosecution and/or reexamination.

The "entire oscillator" term has been construed several times. The constructions reached by the various tribunals that have looked at the issue are found in Plaintiffs' Opening *Markman*

[3] On Friday, October 2, 2015, Judge Grewal granted a contested motion staying Plaintiffs' case against Huawei. See Ex. G, *Technology Properties Ltd., et al. v. Huawei Technologies Co., Ltd. et al.*, Case. No. 3:12-cv-3865, Dkt. 104. In each of the above cases, Plaintiffs assert independent claims 6 and 13, along with dependent claims 7, 9, 14, and 15 (the "Asserted Claims").

Brief. See Ex. C at pp. 1-5 (presenting a summary of how other tribunals have treated the "entire oscillator" term). Notably, Judge Grewal's recommended construction of "entire oscillator" does not comport with any of these prior constructions, including the one issued by Judge Grewal in the HTC case.

IV. APPLICABLE LAW

A. Objecting to a Magistrate Judge's Order

A party may object to a magistrate judge's order. FED. R. CIV. P. 72. If the matter is non-dispositive, the district judge reviews the order to determine whether the magistrate's decision was clearly erroneous. *Id.* When the magistrate judge rules on a dispositive motion, the district judge must determine *de novo* any part of the magistrate's order that was objected to. *Id.* Although 28 USC § 636(b)(1)(A) contains a list of "dispositive" motions, the list is not all-inclusive. In the 9th Circuit, courts look to the effect of an order to determine if the matter is dispositive. *United States v. Rivera-Guerrero*, 377 F.3d 1064, 1068 (9th Cir. 2004).

B. Claim Construction Law

This Court is generally familiar with the various tenets of claim construction, so a general discussion of the applicable law is not included. Prosecution disavowal/disclaimer, however, is a more nuanced subject. While the words of a claim are normally given their customary and ordinary meaning, "there are only two exceptions to this general rule: 1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows [also referred to in cases as "disclaims"] the full scope of a claim term either in the specification or during prosecution." *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012), citing *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1580 (Fed. Cir. 1996). The standard for disavowal/disclaimer of claim scope is exacting. *Thorner*, 669 F.3d at 1366. "The patentee may demonstrate intent to deviate from the ordinary and accustomed meaning of a claim term by including in the specification expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope." *Id.*

Any disclaimers that are found must be the result of statements made by the patentee/applicant during the prosecution of the patent at issue. *North Am. Container Inc. v.*

Plastipak Packaging Inc., 415 F.3d 1335, 1345-46 (Fed. Cir. 2005). As stated by Defendants in their responsive brief:

> The focus must be on the arguments applicants made to distinguish [the prior art at issue], as those are what define the disclaimer. . . . As the Federal Circuit made clear in *North Am. Container*, for example, the scope of the disclaimers must be measured by *what the applicants said during prosecution*, not by what was necessary to distinguish the claims from the prior art. 415 F.3d at 1340-41.

Ex. D, Defendants' Responsive Claim Construction Brief, Dkt. 96 at 5 (emphasis in original). Thus, in determining what, if any disavowals/disclaimers were made by patentee/applicant during the prosecution of a patent, the analysis must look to the words used by patentee/applicant, as those words "define" the disclaimer. Notably, though, to qualify as disclaimer, these statements must be "clear and unmistakable" as the Federal Circuit has "consistently rejected prosecution statements too vague or ambiguous to qualify as a disavowal of claim scope." *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1325-26 (Fed. Cir. 2003).

V. ARGUMENT

These objections are made to Judge Grewal's R&R regarding construction of the claim term "an entire oscillator disposed upon a single integrated circuit." Judge Grewal construed the "entire oscillator" term as "an [oscillator] located entirely on the same semiconductor substrate as the [central processing unit] that does not require a control signal and whose frequency is not fixed by any external crystal." The basis of Judge Grewal's construction is his erroneous finding that Applicants made certain disclaimers during the prosecution of the '336 Patent. Based upon the erroneous finding of disclaimer, Judge Grewal improperly included negative limitations into the claim construction (*i.e.*, "that does not require a control signal and whose frequency is not fixed by any external crystal"). Because Judge Grewal's claim construction (if adopted) has the effect of being case dispositive, thus the Court should review it under a standard of *de novo* review. FED. R. CIV. P. 72(b)(3). Even if this Court determines that the issue is not properly classified as dispositive, Judge Grewal's R&R should be modified because it is clearly erroneous. FED. R. CIV. P. 72(a).

A. The R&R Issued by Judge Grewal is Case Dispositive and therefore the Construction of the Entire Oscillator Term is Subject to *De Novo* Review.

The clear impact of Judge Grewal's construction of the "entire oscillator" term is summary judgment of non-infringement in favor of Defendants, thus making this a dispositive issue requiring *de novo* review. The Federal Rules distinguish between the standard of review required for objections to a magistrate judge's order on dispositive and non-dispositive matters. When an objection to a magistrate judge's order is properly made, orders which are dispositive receive a *de novo* determination by the District Judge, who may accept, reject, or modify the magistrate judge's opinion. FED. R. CIV. P. 72(b). Those issues which are non-dispositive are entitled to review by the district judge under a "clearly erroneous" standard. FED. R. CIV. P. 72(a). While Rule 72 does not indicate which matters are dispositive, 28 U.S.C. § 636(b)(1)(A) lists several motions which are considered dispositive and entitled to *de novo* review. This list is not exhaustive. In the 9th Circuit, courts look to the effect of an order to determine if the matter is dispositive to a claim or defense of a party. *Rivera-Guerrero*, 377 F.3d at 1067-68. "[W]e do not simply look to the list of excepted pretrial matters in order to determine the magistrate judge's authority. Instead, we must look to the effect of the motion, in order to determine whether it is properly characterized as 'dispositive or non-dispositive of a claim or defense of a party.'" *Id.* at 1068, citing *Maisonville v. F2 Am., Inc.*, 902 F.2d 746 (9th Cir. 1990).

The plain effect of Judge Grewal's R&R is judgment of non-infringement in favor of Defendants. Three days after Judge Grewal's issued the R&R, the parties (with the exception of Huawei), filed a joint stipulation stating that "the parties hereby stipulate that all accused products of all Defendants in this Action do not infringe the asserted claims of U.S. Patent 5,809,336 under the Entire Oscillator Construction." Dkt. 105 at ¶4. It is indisputable that the effect of the R&R is dispositive, and Plaintiff's timely objection to the R&R requires *de novo* review by this Court.

This situation is not unusual, as claim construction rulings are frequently case dispositive. In fact, Northern District Patent L.R. 4-3(c) expressly recognizes the potentially dispositive nature of claim construction, requesting the parties to identify which of the claim terms whose

construction may be dispositive. In this particular instance, Defendants identified the "entire oscillator" construction as potentially dispositive. See Ex. I, Joint P.R. 4-3 statement, Dkt. 72 at 4. Evidencing this belief, Defendants directed a significant amount of their presentation at the *Markman* hearing toward non-infringement. During the "tutorial" phase of the *Markman* hearing, Defendants spent significant time discussing the nature of their own products, a subject which had nothing to do with claim construction and everything to do with non-infringement. During the "argument" phase of the *Markman* hearing, counsel for Defendants spoke at length about the importance of this claim term toward non-infringement. Defendants also harkened to non-infringement in their opening *Markman* brief, explicitly comparing the '336 Patent to accused products. Ex. B at 13-14. Having prevailed before Judge Grewal on the "entire oscillator" construction, Defendants effectively secured a judgement of non-infringement, which requires this Court to review Judge Grewal's determination *de novo*.

B. The Applicants Did Not Make the Alleged Disclaimers

Judge Grewal's construction of "entire oscillator" is based on a finding that the Applicants made certain "disclaimers" while distinguishing their invention from two prior art references: U.S. Pat. No. 4,503,500 ("Magar") and U.S. Pat. No. 4,670,837 ("Sheets").[4] R&R at 4. Plaintiffs dispute that any disclaimer actually occurred during Applicants' correspondence with the USPTO. Indeed, several courts (as well as Judge Grewal himself) have previously construed the "entire oscillator" term, and none of them found the sweeping disclaimer advocated by Judge Grewal in his R&R. This record begs the obvious question – how can there be "clear and unmistakable" disavowal of the broad scope advocated by Judge Grewal if several, experienced patent judges have reviewed the same record as Judge Grewal and reached a different conclusion? The answer is readily apparent – no clear and unmistakable disavowal exists in the patent prosecution, and Judge Grewal's finding of clear and unmistakable disclaimer is erroneous.

Applicants distinguished Magar and Sheets on the basis of existing claim limitations. But

[4] Plaintiffs refer to those who prosecuted the '336 Patent in the USPTO as "Applicants", as the entities that owned the application that became the '336 Patent were different entities than Plaintiffs.

even if some disclaimers exist (which Plaintiffs dispute), they are not as broad as those found by Judge Grewal. As discussed in detail below, even if one does find that Applicants did disclaim "something" during the prosecution of the '336 Patent, the subject matter actually disclaimed is far less than that described in the R&R. At most, the proper scope of disclaimer should be an oscillator "that does not require command, manual, or programmed inputs to change frequency and excluding external crystals/clocks to generate a clock signal."

1. Magar

Judge Grewal's construction includes the limitation that the oscillator of the '336 Patent cannot have a frequency that is "fixed by any external crystal." The R&R purports to justify this limitation by examining the arguments made to distinguish the present invention from Magar. The statements made by the Applicants, however, do not support the construction provided, particularly if examined in light of the Magar disclosure.

Magar, attached as Ex. J, was drawn to a specialized processor that would be optimized for performing certain arithmetic tasks. Ex. J, 6:34, et seq. In explaining the specialized processor, Magar describes a particular clocking scheme that involves an external crystal and a component called "CLOCK GEN," seen in the bottom right of Figure 2a. Ex. J, Fig 2a and 15:23-41. Figures 2 and 3 of Magar, along with column 15 of Magar, demonstrate how Magar utilizes the external crystal to generate a 20MHz clock signal. That clock signal drives the on-chip "CLOCK GEN" circuitry shown in Figure 2 and diagramed in Figure 3. Ex. J at Figs. 2a, 3, 15:23-41. After receiving the 20MHz signal via pins X1 and X2, the "CLOCK GEN" circuitry in Magar creates four quarter-cycle clocks seen in Q1-Q4, having a period of 200 nanoseconds (a 5MHz clock signal). *Id.* at 15:23-35. Importantly, there is no on-chip oscillator in Magar. Rather, the clock signal for the CPU is generated by the off-chip crystal. Stated differently, Magar is a one-oscillator system. This is critical to understanding the statements made to the USPTO.

As explained in Plaintiffs' responsive brief to Judge Grewal (see Ex. E at 2-9), the statements relied upon by Defendants in their briefing and Judge Grewal in the R&R do not support a finding of disclaimer. In fact, Applicants' statements during prosecution distinguish

Magar based on existing claim limitations, and clarify that (unlike Magar) the claimed invention does not rely on an external oscillator to generate a clock signal. The oscillator in the claimed invention is on-chip – and, thus, the clock signal is generated on-chip, while Magar's clock is off-chip, a difference specifically captured by the explicit language of the claim.

Judge Grewal, however, cites four sections of Applicants' responses to Magar to support his construction, alleging that the statements made to the USPTO require a finding of disclaimer. Yet, when examined closely, the statements do not create disclaimer individually, nor do they create disclaimer when taken as a whole.

Judge Grewal first cites the Applicants' argument to the USPTO as found in their July 7, 1997 Office Action Response. *See* R&R at 4, lns. 14-18, *see also* Ex. K, July 7, 1997 Office Action Response at 3-4. Judge Grewal alleges that this paragraph is an attempt to "distinguish Magar by emphasizing that the clock disclosed in Magar was fixed by a crystal that was external to the microprocessor, unlike their on-chip variable speed clock." R&R at 4. Judge Grewal is correct that it the Applicants argued that Magar used an external crystal, and that those crystals are fixed frequency. Further, Applicants state that the microprocessor clock is frequency controlled by a crystal. But, a "clock" is not the same thing as an oscillator. See Ex. K at 4, (explaining Applicants' position that all oscillators are clocks but not all clocks are oscillators). The statement above, made in reference to Magar, makes sense because Magar did not have an on-chip oscillator, rather it only contained the on-chip CLOCK GEN circuitry. Thus, the statement above does not support Judge Grewal's construction that the "entire oscillator" is not "fixed by any off-chip oscillator" simply because the Applicants did not disclaim any interaction between an off-chip oscillator and an on-chip oscillator.

Judge Grewal continues that "applicants also argued that the Magar clock could not practice the claimed invention because of its reliance on a crystal, which by its nature cannot vary its oscillation frequency." R&R at 4. In support of this argument, Judge Grewal cites to Applicants' argument found in the R&R at 4-5. See Ex. K at 4. But once again, the statement by the Applicants does not support Judge Grewal's construction. Specifically, there is no mention of an off-chip oscillator having any involvement with an on-chip oscillator. This makes sense

because Magar is a single-oscillator system. Applicants could not have disclaimed that the '336 Patent's oscillator's frequency "is not fixed by any external crystal" because there was no opportunity to do so, and they did not make such a clear, unambiguous statement at the USPTO.

Judge Grewal notes that the USPTO "issued a second rejection based on Magar, and the Applicants responded by emphasizing again that the claimed invention did not rely on an external crystal's fixed frequency to set the clock's frequency rate." R&R at 5. Judge Grewal cites the statement from the prosecution history found in the R&R at 5, lns. 8-10 for support. *See* Ex. L, February 10, 1998 Office Action Response at 4. But, the cited passage does not support the construction promoted by Judge Grewal. Although Applicants state that the frequency originates from an external crystal, they do not say anything about fixing a frequency of an on-chip oscillator.

Lastly, Judge Grewal states that "[t]he applicants also disclaimed the use of an external crystal to cause clock signal oscillation," citing a final passage from the prosecution history for support. See R&R at 5, citing Ex. L at 3. Here, as before, there is no oscillator on the Magar chip that can be controlled by the off-chip oscillator. Applicants clarify that the "clock generator" is not an entire oscillator in itself. They argue that Magar shows a crystal which is used to generate a clock, but say nothing of an off-chip oscillator fixing the frequency of an on-chip oscillator.

In the aggregate, the four statements relied upon by Judge Grewal do not and cannot support the disclaimer featured in Judge Grewal's construction. Indeed, Applicants' statements clearly distinguish the present invention from Magar on the basis of limitations already present in the claims at issue (*e.g.*, varying frequency as a "function of parameter variation in one or more fabrication or operational parameters," such as voltage or temperature). Applicants' statements could support a construction that states that the clock signal provided to the CPU does not originate from or is not generated by an external oscillator. As discussed above, there is only a single oscillator in Magar that supplies a clock signal to the CPU, as is there in the claims of the '336 Patent. But, the construction found in the R&R contemplates the interaction of an on-chip oscillator with an off-chip one. The interaction of two oscillators was never discussed with

respect to Magar, because the reference does not contemplate such an arrangement, just as the '336 Patent does not contemplate this arrangement. Yet, Judge Grewal found that, based on Applicants' words, such subject matter was disclaimed. This is clear error: the interaction of two oscillators cannot be disclaimed if Applicants' never mentioned this subject.

Finally, if any disclaimer with respect to Magar is appropriate, it is one that prohibits a clock signal being *generated* from an off-chip oscillator. Not only would a limitation of "not generated by an off-chip oscillator" be more consistent with the arguments presented to the USPTO, it would also be consistent with prior constructions provided by the ITC, Judge Ward in the Eastern District of Texas, and Judge Grewal himself in the HTC case. See Ex. B at 16, chart listing prior claim constructions.

2. Sheets

The second disclaimer found in Judge Grewal's "entire oscillator" construction concerns statements made by the Applicant in securing allowance of the '336 Patent over Sheets. Based on these statements, Judge Grewal found that the claimed "entire oscillator" term cannot "require a control signal." But, a close review of the statements made by Applicant reveals that the Applicants made no such disavowal. Further, even if Applicant did disclaim subject matter, the scope of the disclaimer is materially narrower than what was found by Judge Grewal.

Sheets (attached as Ex. M) describes a system in which a "microprocessor controls the clock frequency [of the microprocessor] based on the present rate of required microprocessor activity." Ex. M at Abstract. Thus, the goal of the invention described in Sheets is to save energy by running the microprocessor at a lower clock speed when high performance is not needed (and hence use less power). *Id.* Due to this variable speed processor, Sheets is unlike Magar, whose clock is generated by a fixed frequency crystal.

Sheets accomplishes this goal by having the microprocessor periodically determine its processing load. If the load is low, the microprocessor will reduce the clock frequency at which it is driven. *Id.* at 1:45-57. Sheets achieves this reduction in clock frequency by operating with a digital voltage controlled oscillator ("VCO"). *Id.* at 2:54-57. This oscillator generates the clock signal used by the microprocessor in Sheets. *Id.*

In simpler terms, the computer system in Sheets can speed up or slow down based on how much work it has to do. When the system runs faster, it consumes more power, but can process more data. When it runs slower, it consumes less power, but processes less data. The processor in Sheets makes the determination of how much work is queued up, then sets the VCO (which directly determines how fast/slow the system runs) accordingly.

The processor in Sheets causes the VCO to generate a clock speed at a particular frequency by writing a "digital word" to the VCO. *Id.* at 1:60-68. As used in Sheets, a "digital word" is simply a digital value (e.g., 234). Sheets makes clear that the processor writes the digital word to the VCO in the same manner as the word would be written to RAM. So, just as the processor can write/store data to memory, it can write digital data to the VCO. This digital word is stored by the VCO and then used to compute the clock rate output by the VCO.

Judge Grewal's R&R focuses on three paragraphs from the '336 Patent's file history regarding Sheets. See R&R at 5-6, citing Ex. N, at 8, Ex. O, at 4, and Ex. K at 5. These paragraphs are the (apparent) basis for Judge Grewal's finding of disclaimer and are the same passages cited by Defendants in their briefs. Relying on these paragraphs, Judge Grewal crafted a construction that excludes oscillators that "require a control signal" from the scope of the Asserted Claims, finding that Applicants disclaimed such material.

Plaintiffs disagree that these three paragraphs evidence any disclaimer, let alone a disclaimer of the scope found by Judge Grewal. As discussed in Plaintiff's responsive brief (see Ex. E at 9-14), Applicants' statements to the USPTO regarding Sheets evidence no more than the fact that Sheets does not meet the literal language of what became the Asserted Claims. The doctrine of prosecution disclaimer is meant to exclude subject matter that would otherwise be within the scope of the claims, but for the disclaimers. In Sheets, there is no disclosure of how Sheets' oscillator can vary other than by having a digital word written to it. Thus, the Sheets processor does not vary as a function of environmental or fabrication parameters, which is explicitly required by the Asserted Claims. For this reason, Applicants' comments should not be read to disclaim subject matter that would otherwise be within the scope of the claims.

As Defendants repeatedly state, disclaimers that originate in prosecution arise from the words used by Applicants. Assuming arguendo that Applicants disclaimed subject matter in arguing for the allowance of the Asserted Claims over Sheets, the disclaimer found by Judge Grewal goes far beyond what Applicants actually stated.

This disclaimer found by Judge Grewal is defective in two important aspects. First, it applies to "control signals" generally. The universe of what can be considered a "control signal" is large when compared to the specific inputs at issue in Sheets. Plaintiffs believe it is improper to saddle Plaintiffs with the difference in scope between Sheet's signals/inputs and general "control signals" because Applicants never discussed "control signals" in the abstract, instead specifically referring to "***Sheet's system for providing*** control signals."[5] That fact alone demonstrates that Judge Grewal's finding of disclaimer with respect to all "control signals" is not proper.

Second, Judge Grewal's construction prohibits the "entire oscillator" from "requiring" a "control signal" for ostensibly any purpose. Again, as the cited arguments make clear, whatever input/signals that were being disclaimed were only being used for the purposes of changing the frequency/clock speed of the "external clock" at issue. A control signal could possibly be used in conjunction with an oscillator for a number of reasons other than to control the speed of the oscillator. Again, if Applicants' words are to form the basis of the alleged disclaimers, the scope of the disclaimers must be commensurate with what was actually said. In this case, the scope of Applicants' comments is limited to using specific inputs for changing the frequency of an oscillator. Thus, finding disclaimer for the use of "control signals" for purposes other than changing the frequency of the oscillator goes well beyond Applicants' words and is improper.

A proper disclaimer should not be based on some judicially-created abstraction of Applicants' comments. Applicants' specific statements refer to command, programmed, or manual control inputs to change the frequency of the oscillator. To the extent any clear and

[5] Applicants did refer to "Sheets' system for providing clock control signals to an external clock . . . ." in the paragraph cited in the R&R on pp. 5-6. This reference to control signals was clearly limited to the ones discussed in Sheets and not to "control signals" generally.

unmistakable disclaimer was made, which Plaintiffs strongly dispute, it would necessarily relate to only this subject matter.

Turning now to the particular words used by Applicants in discussing Sheets, the first citation relied upon by Judge Grewal distinguishes Sheets from the Asserted Claims based on the "control information" found in Sheets. The discussion in this paragraph is not a generalized discussion of "control information." Rather, it is specific to the "control information" disclosed in Sheets (*i.e.*, the digital word written by the processor to the VCO).

In the second citation relied upon by Judge Grewal, Applicants characterize the digital word of Sheets as a "command input." If a disclaimer is to be found in this citation, it must be limited to an oscillator that requires "command inputs" to change the frequency. Again, these "command inputs" refer to the disclosure in Sheets of the microprocessor writing a digital value to the VCO. In this paragraph, Applicants did not mention "control signals."

Finally, in the third and last paragraph cited by Judge Grewal with respect to Sheets, Applicants state that the oscillator described in the Asserted Claims "does not require manual or programmed inputs . . . to [vary in frequency]." Again, there is no discussion of "control signals" in this portion of Applicant's response. Rather, on the topic of "inputs", the discussion is limited to "manual or programmed inputs." Thus, like the preceding citations, the statements made by Applicants are far more limited than the disclaimer found by Judge Grewal.

In summary, the R&R finds the term "entire oscillator" does not include oscillators that require a "control signal." This finding is based on Applicants statements in distinguishing over Sheets. But, Applicants' never made such a sweeping disclaimer in the prosecution history. At most, Applicants' statements distinguished the claimed oscillator as one that does not require "command, manual, and programmed inputs" to change its frequency. But even these statements are not clear and unmistakable disclaimers.

VI. CONCLUSION

As discussed above, Judge Grewal incorrectly found that Applicants disclaimed subject matter during the prosecution of the patent application that ultimately became the '336 Patent. During that prosecution, Applicants demonstrated that Magar and Sheets both fell outside the

explicit requirements of the then pending claims. With respect to Magar, the Asserted Claims require the "entire oscillator" to reside on the same chip as the CPU and to vary with the CPU as a function of certain environmental and process related variables. The quartz oscillator in Magar is neither on-chip nor can it vary like the claimed oscillator. The same goes for Sheets - it is an off-chip oscillator that is not disclosed as varying like the oscillator recited in the Asserted Claims. For these reasons, there is simply no cause to find that Applicants disclaimed subject matter that would otherwise be captured by the Asserted Claims.

Further, despite Plaintiffs' beliefs to the contrary, if Applicants did disclaim subject matter that would otherwise be covered by the Asserted Claims, the scope of such disclaimer is much narrower than that found by Judge Grewal. A review of the statements made by Applicants demonstrates as much. With respect to Magar, Applicants' statements all centered on the fact that the off-chip quartz oscillator in Magar could not generate a clock signal like the one described in the Asserted Claims. Thus, a disclaimer finding that the claimed oscillator does not include "external crystals/clocks to generate a clock signal" is more appropriate than the one found in the R&R. With respect to Sheets, Applicants merely discussed Sheet's use of "command, manual, and programmed inputs" to "change the frequency" of the oscillator in Sheets. Accordingly, if a disclaimer is to be found with respect to Sheets, it should only exclude oscillators "that require command, manual, or programmed inputs to change frequency."

Dated: October 6, 2015

Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that, on October 6, 2015, I caused the foregoing document to be served on counsel of record via the Court's CM/ECF system.

Dated: October 6, 2015

By: /s/ *Barry J. Bumgardner*
Barry J. Bumgardner

Appx3258-3495 has been removed from the Appendix in the interest of brevity. These pages are the exhibits to Plaintiffs' Motion for De Novo Determination of Dispositive Matter Referred to Magistrate Judge, or, in the Alternative, Motion for Relief from Nondispositive Pretrial Order of Magistrate Judge, and are referred to on p. 3 of Appellants' Opening Brief in discussing the background of the district court litigation. These pages are not referred to again in any of the parties' briefs.

The exhibits can be accessed via PACER (Case No. 3:12-cv-03865-VC; Dkt. No. 105; (N.D. Cal.))

United States Patent [19]

Sheets

[11] **Patent Number: 4,670,837**

[45] **Date of Patent: Jun. 2, 1987**

[54] **ELECTRICAL SYSTEM HAVING VARIABLE-FREQUENCY CLOCK**

[75] Inventor: **Laurence L. Sheets**, St. Charles, Ill.

[73] Assignees: **American Telephone and Telegraph Company; AT&T Bell Laboratories**, both of Murray Hill, N.J.

[21] Appl. No.: **624,469**

[22] Filed: **Jun. 25, 1984**

[51] **Int. Cl.**[4] **H03K 5/04**

[52] **U.S. Cl.** **364/200**; 328/38.1

[58] **Field of Search** 364/200, 900; 328/62, 328/38; 365/222

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,453,601	7/1969	Bogert et al.	364/200
3,656,123	4/1972	Carnevale et al.	340/172.5
3,775,696	11/1973	Garth	331/57
3,922,526	11/1975	Cochran	235/152
4,037,090	7/1977	Raymond, Jr.	364/200
4,191,998	3/1980	Carmody	364/200
4,241,418	12/1980	Stanley	364/900
4,331,924	5/1982	Elliot et al.	328/38
4,414,637	11/1983	Stanley	364/569
4,438,490	3/1984	Wilder, Jr.	364/200
4,447,870	5/1984	Tague et al.	364/200
4,463,440	7/1984	Nishiura et al.	364/900

FOREIGN PATENT DOCUMENTS

0098653	6/1983	European Pat. Off. .
2248170	4/1974	Fed. Rep. of Germany .

Primary Examiner—Gareth D. Shaw
Assistant Examiner—Randy W. Lacasse
Attorney, Agent, or Firm—Ross T. Watland

[57] **ABSTRACT**

The microprocessor unit of a system implemented using metal-oxide-silicon (MOS) technology, is driven by a variable-frequency clock. The microprocessor controls the clock frequency based on the present rate of required microprocessor activity. By driving the microprocessor unit at a lower clock frequency when such activity rate is low, the energy dissipated by the microprocessor unit is reduced due to the MOS power-frequency characteristic.

7 Claims, 6 Drawing Figures

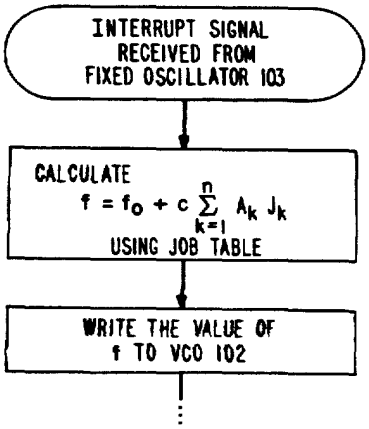


FIG. 1

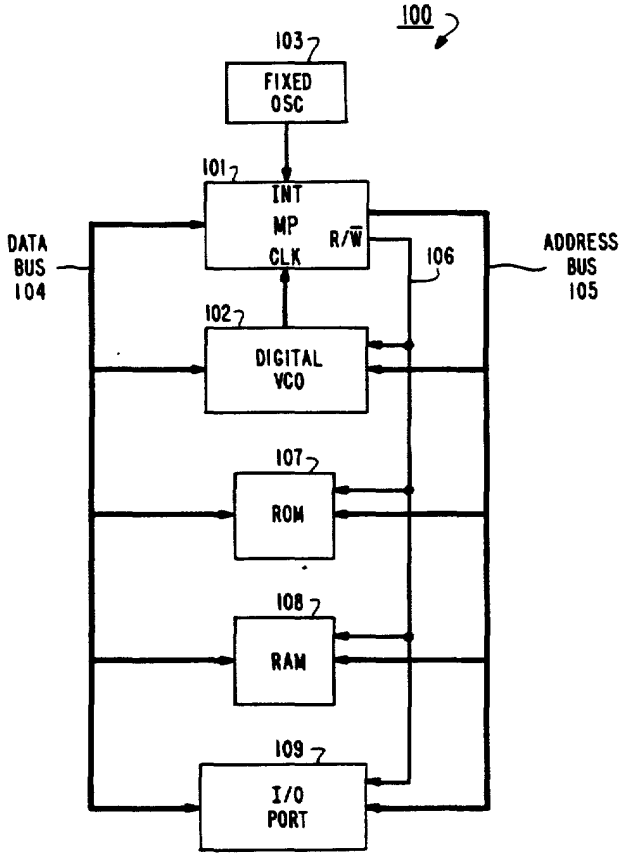

100
103
FIXED OSC
101
INT MP CLK
R/W
DATA BUS 104
ADDRESS BUS 105
106
102
DIGITAL VCO
107
ROM
108
RAM
109
I/O PORT

FIG. 2

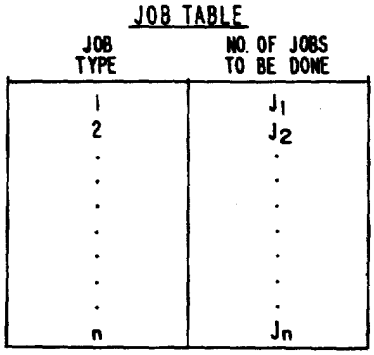


FIG. 3

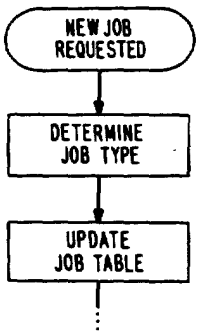


FIG. 4

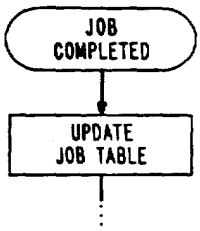
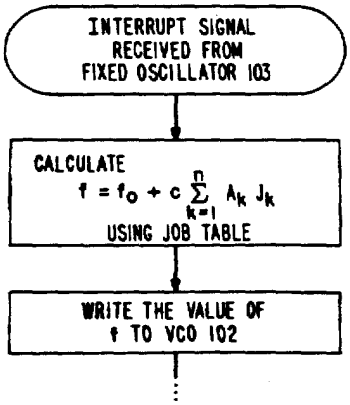


FIG. 5



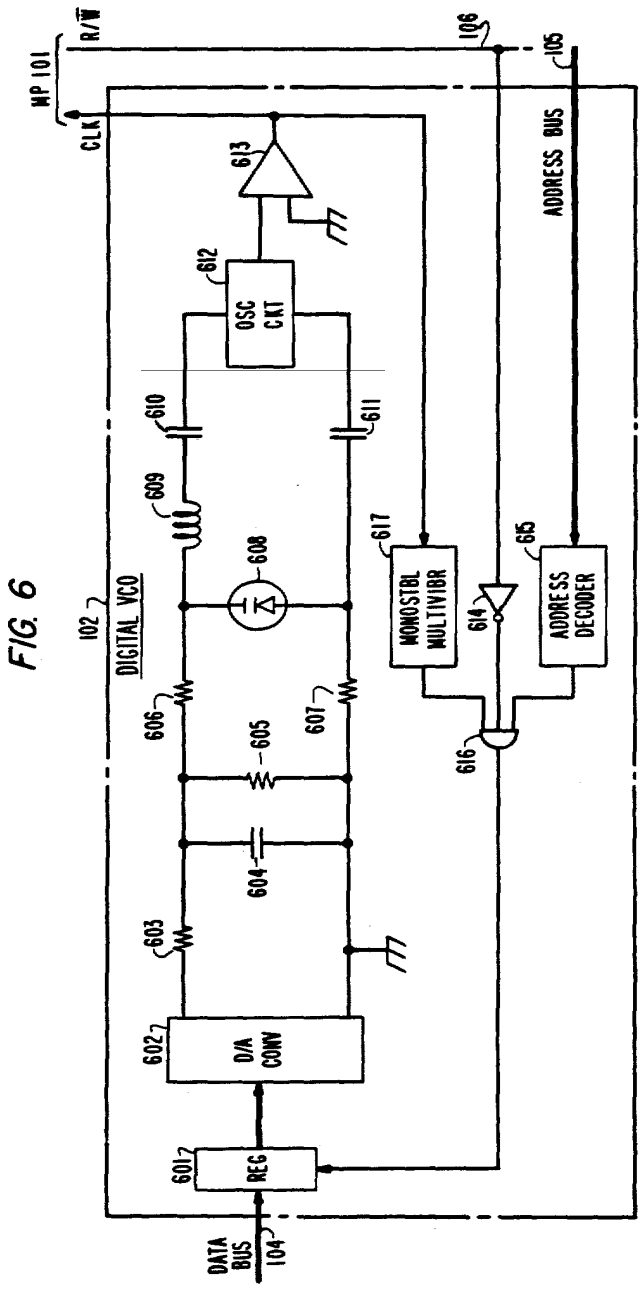

R/W
106
105
MP 101
CLK
ADDRESS BUS
613
612
OSC CKT
610
611
609
608
617
615
MONOSTBL MULTIVIBR
ADDRESS DECODER
614
102
DIGITAL VCO
606
607
605
616
604
603
602
D/A CONV
601
REG
DATA BUS
104

FIG. 6

ELECTRICAL SYSTEM HAVING VARIABLE-FREQUENCY CLOCK

TECHNICAL FIELD

This invention relates to clocked, electrical systems, and, more particularly, to microprocessor-based systems implemented using metal-oxide-silicon (MOS) technology.

BACKGROUND OF THE INVENTION

One very important aspect of the continuing evolution of silicon technology is the proliferation of microprocessors throughout our society. Because of the significant reductions in their size and cost, such processors can be economically used in many applications where the use of computers could not otherwise be justified. Even in applications where larger computers, e.g., minicomputers, have traditionally been used, the advantages of distributed processing have been obtained by using a number of microprocessors to perform the functions previously performed by a single larger processor. For example, many of the control functions previously performed by the central control unit in stored program controlled switching systems are being performed in more modern systems by a number of microprocessors which are distributed toward the system periphery and which communicate with each other to control system operation.

One countervailing factor to weigh against the established advantages of distributed processing is the large amount of power typically required to keep such distributed control processors continuously energized. This factor will become even more important as the cost of energy continues to increase. The power dissipation of microprocessors also becomes important when they are used in portable, battery-powered personal computers. In these applications and others, the ma9nitude of power required to operate microprocessor-based systems is a problem which diminishes the otherwise overall attractiveness of such systems.

SUMMARY OF THE INVENTION

The aforementioned problem is advantageously solved and a technical advance is achieved in accordance with the principles of the invention in both an electrical system driven by a variable-frequency clock and an associated system operation method which reduce the magnitude of energy required by the electrical system by determining the processing load presented to the system and then reducing the clock frequency at which the system is driven, during times when the processing load is reduced. The amount of the saving is dependent on the power-frequency characteristic associated with the particular technology with which the electrical system is implemented.

BRIEF DESCRIPTION OF THE DRAWING

A more complete understanding of the present invention may be obtained from a consideration of the following description when read in conjunction with the drawing in which:

FIG. **1** is a block diagram of a microprocessor-based system illustrating the principles of the present invention;

FIGS. **2** through **5** are diagrams illustrating a method of monitoring the processing load and computing the required clock frequency to reduce the magnitude of energy required by the system of FIG. **1**; and

FIG. **6** is a circuit diagram of a digital, voltage-controlled oscillator included in the system of FIG. **1**.

DETAILED DESCRIPTION

FIG. **1** is a block diagram of an exemplary microprocessor-based system **100** illustrating the principles of the present invention. The system is controlled by a microprocessor **101** which communicates with associated devices via a data bus **104** and an address bus **105**. For example, microprocessor **101** reads information from a read only memory (ROM) **107** via data bus **104** by transmitting a logic one signal from a control terminal $R/\overline{W}$ via a conductor **106** and transmitting on address bus **105**, an address defining both ROM **107** and the particular location of ROM **107** to be read. ROM **107** is typically used to store information such as programs to be executed by microprocessor **101** or fixed data. Microprocessor **101** reads information in like manner from a random access memory (RAM) **108**, used to store variable data, or from an input/output (I/O) port **109**, used to interface with various external devices (not shown), e.g., devices being operated under the control of microprocessor **101**. In addition, microprocessor **101** also writes information via data bus **104** to RAM **108** or I/O port **109** by transmitting a logic zero signal from control terminal $R/\overline{W}$ on conductor **106** and transmitting the appropriate address on address bus **105**.

The portion of system **100** described thus far is well known. Various other control or status signals are typically conveyed between microprocessor **101** and its associated devices to achieve correct system operation. However, since such signals are not relevant to the present invention and tend to vary depending upon the particular family of devices used in a given implementation, they are not further described herein. Microprocessor **101** and its associated devices are energized by means of a DC power source (not shown), e.g., a battery or, alternatively, a DC power supply driven from a commercial AC source. The present invention is directed to reducing the amount of energy drawn by system **100** from such a DC source. In addition to energy savings, an enhancement of long-term system reliability is also obtained.

Microprocessor-based systems such as system **100** are typically implemented using metal-oxide-silicon (MOS) technology. The magnitude of power consumed by a MOS device at a given voltage is substantially directly proportional to the frequency at which the device is operated. In the case of microprocessor **101**, which is a relatively complex MOS device, the duration of each execution cycle is defined by the signal received at a CLK terminal. In accordance with the present exemplary embodiment of the invention, a digital, voltage-controlled oscillator (VCO) **102** transmits the cycle-defining clock signal. Upon determining the amount of processing required at any given time, microprocessor **101** computes an operating frequency that is sufficient to meet the offered processing load. Microprocessor **101**, which communicates with VCO **102** via data bus **104**, address bus **105** and conductor **106** in the same manner as with RAM **108** or I/O port **109**, writes a digital word defined by the computed frequency via data bus **104** to VCO **102**. VCO **102** gradually adjusts the frequency of the clock signal transmitted to microprocessor **101** to the computed frequency in response to the digital word. Reducing the clock frequency reduces

the power consumed by microprocessor **101** and, by reducing the required access rate to the associated devices, i.e., ROM **107**, RAM **108**, and I/O port **109**, also reduces the power consumed by those devices. The power reduction is substantially directly proportional to the reduction of the clock frequency. For example, a frequency reduction from 20 megahertz to 10 megahertz will result in a saving of approximately 50%.

In system **100**, the timing of real-time events is controlled by microprocessor **101** in response to interrupt signals received at an INT terminal from a fixed-frequency oscillator **103**. For example, microprocessor **101** repeats the process of computing the required frequency based on the processing load and writing a digital word to digital VCO **102** at regular intervals as defined by the interrupt signals from fixed oscillator **103**.

In the present embodiment, microprocessor **101** determines its processing load to control the VCO **102** clock frequency at any given time by using a linear regression. All possible processing jobs expected for microprocessor **101** in a particular application, are categorized according to complexity, i.e., the number of execution cycles required for completion, into n job types, where n is a positive integer greater than one. Associated with each job type is a predetermined weighting factor A_k which defines the complexity of that job type with respect to other job types. Microprocessor **101** maintains a job table (FIG. 2) in RAM **108**. The job table lists for each job type the number, J_k, of jobs of that type presently required. As shown in FIG. **3**, when each processing job is requested, the associated job type is determined and the job table is updated by incrementing J_k by one. Jobs may be requested in a number of ways. For example, certain jobs may be required at regular intervals as defined by the interrupt signals from fixed oscillator **103**. Other jobs may be requested in response to information received from external devices and read via I/O port **109**. After each processing job is completed, the job table is updated by decrementing J_k by one for the associated job type (FIG. **4**). Thus the job table in RAM **108** is kept current at all times. As shown in FIG. **5**, each time that microprocessor **101** receives an interrupt signal from fixed oscillator **103**, microprocessor **101** reads each of the J_k values in the job table and computes the required clock frequency, f, according to

$$f = f_0 + c \sum_{k=1}^{n} A_k J_k,$$

where f_o is the lowest desired frequency and c is an appropriate scale factor. (Alternatively, the A_k weighting factors could be properly scaled to eliminate the need for the scale factor c.) A digital word defined by the computed value of f is then written to VCO **102**.

In the present embodiment, di9ital VCO **102** is implemented as an LC oscillator (FIG. **6**). When microprocessor **101** computes a new clock frequency, it transmits a digital word defined by that frequency via data bus **104** to a register **601**. Microprocessor **101** also transmits an address on address bus **105** to an address decoder **615**. Address decoder **615** responds to the particular address defining VCO **102** by transmitting a logic one signal to an AND gate **616**. Microprocessor **101** transmits a logic zero signal on conductor **106** from its $R/\overline{W}$ terminal to an inverter **614**, which in turn transmits a logic one signal to AND gate **616**. When a monostable multivibrator **617** transmits a logic one signal to a third input terminal of AND gate **616**, AND gate **616** responds by transmitting a logic one signal to register **601** which then stores the digital word from data bus **104**. A D/A converter **602** generates an analog control voltage in response to the digital word in register **601**. The analog control voltage is filtered by a low-pass filter comprised of resistors **603** and **605** and a capacitor **604**, the values of which determine a filter time constant such that the control voltage transmitted varies slowly with respect to the minimum required clock frequency. The resistor **605** is connected across capacitor **604** as a discharging means. The control voltage is then applied via a pair of decoupling resistors **606** and **607** to a varicap diode **608**, having a capacitance that varies from 25 to 100 picofarads with applied voltage. The combination of the variable capacitance of the varicap diode **608** and the inductance of an inductor **609**, e.g., 2.5 microhenries, is coupled via a pair of coupling capacitors **610** and **611** to an oscillator circuit **612**. Oscillator circuit **612**, which is implemented in the present embodiment as an amplifier circuit, transmits a sinusoidal signal at the frequency determined by the combination of varicap diode **608** and inductor **609**. The sinusoidal signal transmitted by circuit **612** is applied to one input terminal of comparator **613**, which has its other input terminal **9**rounded. Accordingly, comparator **613** transmits a square wave at the determined frequency. The square wave is transmitted to both the CLK terminal of microprocessor **101** to define its execution cycle and to monostable multivibrator **617** which responds by transmitting a logic one signal to AND gate **616** as described above. Monostable multivibrator **617** transmits a pulse of predetermined duration on the leading edge of the square wave generated by comparator **613** and is included to assure that each data word on data bus **104** is stable before AND gate transmits a logic one signal to store that data word in register **601**.

In this embodiment, the relationship between the clock frequency computed by microprocessor **101** and the digital word transmitted to VCO **102** is predetermined based on the characteristic of VCO **102**. Accordingly, when microprocessor **101** computes a given clock frequency, it transmits a digital word to VCO **102** according to the predetermined relationship such that VCO **102** generates the given clock frequency in response to that digital word.

It is to be understood that the above-described embodiment is merely illustrative of the principles of the present invention and that other embodiments may be devised by those skilled in the art without departing from the spirit and scope of the invention. For example, the LC oscillator implementation of digital VCO **102** may be replaced by a switched RC oscillator where resistors of differing resistance are switched in and out of the circuit to vary the frequency in response to the digital words received by the D/A converter. Rather than computing the frequency based on the processing backlog, the activity on data bus **104** and address bus **105** could be monitored and then used as a basis for determining the required frequency. Instead of using a continuously variable-frequency clock, selections can be made from a small number of discrete frequencies. For example, in a battery-powered personal computer with an operating system which includes a sleep state, the microprocessor CPU could be operated at a low frequency sufficient to keep any dynamic logic re-

freshed, e.g., 500 kilohertz, when the operating system is in the sleep state, and the frequency could then be increased to a nominal operating frequency, e.g., 10 megahertz, when wakeup occurs. In some applications, the desired clock frequency could be determined based on historical activity records rather than in real time. For example, the operating frequency of the distributed microprocessors used for control in a telephone switching system could be adjusted based on calling patterns observed during different times of the day or during different days of the week as a way of reducing the energy requirements of the system. It is to be recognized that any of a number of microprocessor families can be advantageously used in such systems. One specific example is the Motorola 68000 microprocessor and its associated devices. Furthermore, the invention is applicable to clocked, electrical systems other than microprocessor-based systems where power consumption is a function of clock frequency as, for example, in gate arrays.

What is claimed is:

1. In an electrical system driven by a variable-frequency clock to perform processing jobs, a method of operating said system under control of a processor to increase efficiency in power consumption comprising:

determining the processing load of said system based on all requested but uncompleted processing jobs and

adjusting the frequency of said clock basewd on the determined processing load, where each of said processing jobs is one of n types, n being a positive integer greater than one, said method further comprising

maintaining data that define a number, J_K, of jobs of type K for each integer K from one through n, to be performed by said system,

wherein said determining step further comprises reading said data and

wherein said adjusting step further comprises adjusting the frequency, f, of said clock according to

$$f = f_0 + C \sum_{K=1} A_K J_K,$$

wehrein f0 is a minimum frequency, A_K is a weighting factor associated with jobs of type K, and C is a predetermined scale factor.

2. A method in accordance with claim 1 further comprising

repeating at regular intevals said determining step and said adjusting step.

3. A method in accordance with claim 1 wherein said maintianing step further comprises

incrementing said number, J_k, by one as each job of type k is requested and

decremeting said number, J_k, by one as each job of type k is completed.

4. An electrical system comprising:

variable-frequency clock means for transmitting a clock signal of variable frequency,

electrical means for performing processing jobs at an operating frequency defined by the frequency of said clock signal, said electrical means comprising a processor

means for repetitively determining the processing load of said electrical means based on all requested but uncompleted processing jobs and

means coupled to said variable-frequency clock means for adjusting the frequency of said clock signal basedon the processing load determined by said determining means, wherein

each of said processing jobs is one of n types, n being a positive integer greater than one, said system further comprises

means for maintaining data that define a number, J_K, of jobs of type K, for each integer K from one through n, to be performed by said system,

wherein said determining means further comprises means for reading said data

wherein said adjusting means further comprises means for calculating an operating frequency, f, according to

$$f = f_0 + C \sum_{K=1} A_K J_K,$$

wherein f_0 is a minimum frequency, A_K is a weighting factor associated with jobs of type K, and C is a predetermined scale factor and

means for transmitting a digital word defined by said calculated operating frequency, f, to said variable-frequency clock means,

wherein said variable-frequency clock means is responsive to said digital word for generating said clock signal at said calculating operating frequency, f.

5. An electrical system in accordance with claim 4 wherein said variable-frequency clock means further comprises

converter means for generating an analog control voltage in response to said digital word and

oscillator means coupled to said converter means for generating said clock signal at a frequncy defined by said analog control voltage.

6. An electrical system in accordance with claim 5 further comprising

low-pass filter means interposed between said converter means and said oscillato means for filtering said analog control voltage.

7. An electrical system in accordance with claim 4 wherein said electrical means is implemented in metal-oxide-silicon technology.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 4,670,837

DATED : June 2, 1987

INVENTOR(S) : Laurence L. Sheets

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

IN THE CLAIMS

Column 5, line 30, "basewd" should be "based",
Column 5, line 47, "wehrein" should be "where",
Column 5, line 52, "intevals" should be "intervals",
Column 5, line 56, "maintianing" should be "maintaining";
Column 6, line 1, "decremeting" should be "decrementing",
Column 6, line 15, "basedon" should be "based on",
Column 6, line 48, "frequncy" should be "frequency",
Column 6, line 53, "oscillato" should be "oscillator".

Signed and Sealed this

Seventeenth Day of July, 1990

Attest:

Attesting Officer

HARRY F. MANBECK, JR.

Commissioner of Patents and Trademarks

Appx3504-3520 has been removed from the Appendix in the interest of brevity. These pages are the exhibits to Plaintiffs' Motion for De Novo Determination of Dispositive Matter Referred to Magistrate Judge, or, in the Alternative, Motion for Relief from Nondispositive Pretrial Order of Magistrate Judge, and are referred to on p. 3 of Appellants' Opening Brief in discussing the background of the district court litigation. These pages are not referred to again in any of the parties' briefs.

The exhibits can be accessed via PACER (Case No. 3:12-cv-03865-VC; Dkt. No. 105; (N.D. Cal.))

(*Counsel listed on signature page*)

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. HUAWEI TECHNOLOGIES CO., LTD., et al., Defendants.	Case No. 3:12-cv-03865-VC (PSG) **DEFENDANTS' RESPONSE TO PLAINTIFFS' MOTION FOR DE NOVO DETERMINATION OF DISPOSITIVE MATTER REFERRED TO MAGISTRATE JUDGE, OR, IN THE ALTERNATIVE, MOTION FOR RELIEF FROM NONDISPOSITIVE PRETRIAL ORDER OF MAGISTRATE JUDGE** DATE: November 19, 2015 TIME: 10:00 AM PLACE: Courtroom 4 JUDGE: Hon. Vince Chhabria
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. ZTE CORPORATION, et al., Defendants.	Case No. 3:12-cv-03876-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. SAMSUNG ELECTRONICS CO., LTD., et al., Defendants.	Case No. 3:12-cv-03877-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. LG ELECTRONICS, INC., et al., Defendants.	Case No. 3:12-cv-03880-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. NINTENDO CO., LTD, et al. Defendants.	Case No. 3:12-cv-03881-VC (PSG)

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I. INTRODUCTION

Judge Grewal's recommended construction of the "entire oscillator" limitation is correct and should be adopted by the Court without modification because it accurately reflects two clear and unambiguous disclaimers made by the applicants for the '336 patent during prosecution. First, to overcome rejections based on the Magar prior art reference, the applicants repeatedly distinguished their claimed "entire oscillator" from Magar's oscillator on the basis that the frequency of Magar's oscillator was fixed by an external crystal. As a result, Judge Grewal correctly construed "entire oscillator" to mean, in part, "an oscillator . . . whose frequency is not fixed by an external crystal." September 22, 2015, Claim Construction Report and Recommendation ("R&R"), Dkt. 104, at 2, 4-5, 10.[1] Second, to overcome a rejection based on the Sheets prior art reference, the applicants repeatedly distinguished their claimed "entire oscillator" from Sheets on the basis that the Sheets system required control signals. Thus, Judge Grewal also correctly construed "entire oscillator" to mean, in part, "an oscillator . . . that does not require a control signal." R&R at 2, 5-6, 11.

Accordingly, Judge Grewal's recommended construction is correct and should be adopted by the Court.

II. OVERVIEW OF U.S. PATENT NO. 5,809,336

U.S. Patent No. 5,809,336 (the "'336 patent") is directed to a variable-speed clock (the "entire oscillator") that controls the speed of a CPU and that is incorporated on the same integrated circuit substrate as the CPU. Ex. A ('336 patent) at cover & 16:54-17:10.[2] The variable-speed oscillator adjusts its frequency in real time based upon the microprocessor's physical and environmental characteristics, including temperature, voltage and semiconductor manufacturing process quality, to track the then-existing processing capabilities of the CPU. *Id.*

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[1] Unless otherwise indicated, all docket numbers cited in this brief refer to *Technology Properties Ltd., et al. v. Samsung Electronics Co., Ltd. et al.*, Case No. 12-cv-03877-VC (PSG).

[2] All exhibits cited in this brief are attached to the accompanying Declaration of Aaron Wainscoat in Support of Defendants' Response to Plaintiffs' Motion for *De Novo* Determination.

at 16:54-17:10; R&R at 3-4. In other words, the on-chip oscillator's frequency varies together with the frequency capability of the CPU. *Id.*

The '336 patent issued as a divisional patent from a specification that describes several different purported inventions. Ex. A at cover ("Division of Ser. No. 389,334, Aug. 3, 1989, Pat. No. 5,440,749"); R&R at 3. As a result, the '336 patent's "Summary of the Invention" section contains material that is largely irrelevant to the asserted claims, with only lines 27 through 35 of column 3 pertaining to the alleged invention. Ex. A at 3:27-35. Similarly, the "Detailed Description of The Invention" includes much extraneous material, with the only parts describing the '336 patent's purported invention being found in the last 25 lines of column 16 and the first 37 lines of column 17, under the sub-headings "Optimal CPU Clock Scheme" and "Asynchronous/Synchronous CPU." *Id.* at 16:43-17:37; R&R at 3.

In the parts of the specification that are relevant to the alleged invention claimed in the '336 patent, the specification explains that a high speed microprocessor must "operate over wide temperature ranges, wide voltage swings, and wide variations in semiconductor processing" that "all affect transistor gate propagation delays." Ex. A at 16:44-48; R&R at 4. These three parameters, "processing," "voltage" and "temperature," are referred to as "PVT" parameters.

As the specification explains, traditional prior art microprocessor systems are designed with a single fixed speed clock for all parts of the system. Ex. A at 16:48-50, 17:12-13; R&R at 3. By design, this conventional fixed speed clock (which includes an off-chip crystal and on-chip components) always operates at a speed that is slow enough to ensure error-free operation during those times when worst case PVT parameter conditions may exist. *Id.* As a result, the traditional prior art microprocessor systems "must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse [sic] case conditions" to ensure that a user always experiences error-free operation. Ex. A at 16:48-53.

To avoid the constrained speed of the prior art and to always operate at or near its maximum performance capabilities for the existing PVT parameter conditions, the '336 patent replaces the prior art's external fixed-speed crystal clock which controls the CPU's speed with an on-chip "ring counter variable speed system clock" (also referred to as a "ring oscillator variable

speed system clock") that adjusts its speed in real time as a function of existing PVT parameters to match the CPU's maximum frequency capability under those parameters. Ex. A at 3:26-34, 16:54-17:10, 17:19-22; R&R at 3-4. In other words, the oscillator's frequency varies together with the frequency of the CPU. Ex. A at 3:26-34, 16:60-17:2.

Unlike a fixed clock's speed, the frequency of the claimed internal variable speed oscillator varies significantly as a function of PVT parameters. Ex. A at 16:59-60 ("The ring oscillator frequency is determined by the parameters of temperature, voltage, and process"). For example, the '336 patent's specification discloses that the speed of the variable speed clock will be 100 megahertz at room temperature, but will slow to 50 megahertz if the temperature rises to 70°C (*i.e.*, 158° F). *Id.* at 16:59-63. The oscillator's speed may vary, according to the patent, by as much as a factor of four (*i.e.*, by as much as 400%) depending on all three PVT parameters. *Id.* at 17:21-22.

According to the '336 patent, the "optimum performance" of the variable speed oscillator supposedly results from fabricating and locating the variable speed oscillator on the same semiconductor substrate as the CPU, so that the same PVT parameters affect both the oscillator and the CPU. Ex. A at 16:57-58, 16:63-17:10. For example, if the temperature of the substrate rises, then the processing speed capability of the CPU decreases. But because the oscillator and CPU are fabricated on the same substrate, this rise in temperature also causes the speed of the variable speed oscillator to decrease, so that the oscillator leads the CPU to a slower maximum speed at which it can operate properly. *Id.* As the specification explains, this ensures that the CPU "will always execute at the maximum frequency possible, but never too fast." *Id.* at 16:67-17:2.

Because certain devices which communicate with the CPU cannot tolerate a variable speed clock, the system requires a second clock that is independent of the variable speed oscillator. Ex. A at 17:22-34; R&R at 4. The independent second clock is connected to the input/output (I/O) interface, as illustrated in Figure 17 of the '336 patent, with the second clock on Figure 17 being a conventional "crystal clock" 434:

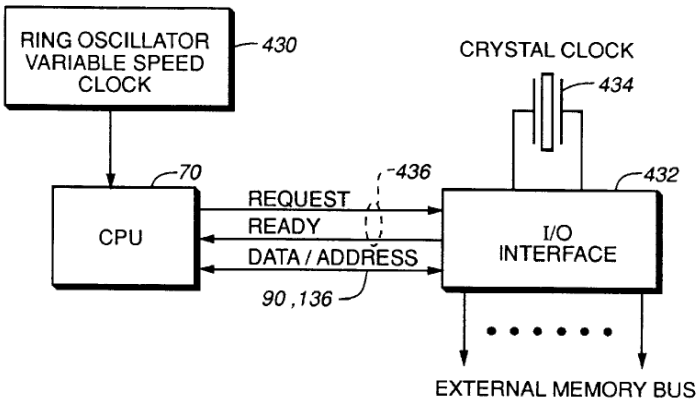

FIG._17

Each independent claim of the '336 patent (including asserted claims 6 and 13) provides for a fixed-speed, independent second clock that is connected to an input/output ("I/O") interface. Ex. A at 17:14-34. The frequency of the second clock is fixed to allow the I/O interface to interact with off-chip memory and other off-chip components, and to perform operations that require a fixed frequency, such as "video display updating and disc drive reading and writing." *Id.* at 17:14-34. By connecting the variable speed oscillator to the CPU while separately connecting the independent fixed speed clock to the I/O interface, the variable speed CPU is decoupled from the fixed speed I/O interface. *Id.* at 17:32-34. This configuration optimizes the performance of the system by allowing the CPU to run as fast as possible under the current PVT conditions while maintaining the I/O interface 432 at a stable fixed speed. *Id.* at 17:32-34.

III. APPLICABLE LAW

A. Claim Construction

When construing claim terms, the Federal Circuit emphasizes the importance of intrinsic evidence such as the language of the claims themselves, the specification, and the prosecution history. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-17 (Fed. Cir. 2005) (*en banc*). Claim terms "are generally given their ordinary and customary meanings as understood by a person of ordinary skill in the art when read in the context of the specification and prosecution history." *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). There are

two circumstances where a claim is not entitled to its plain and ordinary meaning: "1) when a patentee sets out a definition and acts as his own lexicographer, or 2) when the patentee disavows the full scope of a claim term either in the specification or during prosecution." *Id*. Courts may also consider "extrinsic evidence," which "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises." *Phillips*, 415 F.3d at 1317 (quotation and citation omitted). However, such evidence is "less significant than the intrinsic record in determining the legally operative meaning of claim language." *Id*. (quotation and citation omitted).

Of particular importance here, the scope of a claim term must be limited if the applicant argued during prosecution that the claim has a limited scope in order to obtain the patent from the PTO. *Southwall Techs., Inc., v. Cardinal IG Co*., 54 F.3d 1570, 1576 (Fed. Cir. 1995) ("Claims may not be construed one way in order to obtain their allowance and in a different way against accused infringers."); *Abbott Labs. v. Sandoz, Inc.*, 566 F.3d 1282, 1289 (Fed. Cir. 2009) (*en banc*) ("'the prosecution history can often inform the meaning of the claim language by demonstrating . . . whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be.'") (quoting *Phillips*, 415 F.3d at 1317).

While a prosecution history disclaimer must be "clear and unambiguous," the Federal Circuit recognizes that "applicants rarely submit affirmative disclaimers along the lines of 'I hereby disclaim the following…' during prosecution." *Saffran v. Johnson & Johnson*, 712 F.3d 549, 559 (Fed. Cir. 2013). Thus, "[e]xplicit arguments made during prosecution to overcome prior art can lead to a narrow claim interpretation because '[t]he public has a right to rely on such definitive statements made during prosecution.'" *Rheox, Inc. v. Entact, Inc*., 276 F.3d 1319, 1325 (Fed. Cir. 2002) (quoting *Digital Biometrics, Inc. v. Identix, Inc*., 149 F.3d 1335, 1347 (Fed. Cir. 1998)); *see also Saffran*, 712 F.3d at 559 (holding that explicit statements distinguishing prior art during prosecution constitute a disclaimer of claim scope); *Am. Piledriving Equipment, Inc. v. Geoquip, Inc.*, 637 F.3d 1324, 1336 (Fed. Cir. 2011) (holding that the applicants' arguments distinguishing prior art during prosecution constituted a disavowal of claim scope even though the applicant distinguished the prior art on other grounds as well).

In short, "[t]he patentee is held to what he declares during the prosecution of his patent." *Gillespie v. Dywidag Systs. Int'l, USA*, 501 F.3d 1285, 1291 (Fed. Cir. 2007) (reversing district court's construction and determination of literal infringement because patentee's "construction was negated during prosecution."); *Computer Docking Station Corp. v. Dell, Inc*., 519 F.3d 1366, 1379 (Fed. Cir. 2008) (holding that "the sum of the patentees' statements during prosecution would lead a competitor to believe that the patentee had disavowed" devices otherwise covered by the claim language). Thus, if an inventor defines a term or otherwise disclaims a meaning during prosecution, the inventor has acted as his own lexicographer and the term is limited to the scope of the definition or disclaimer. *Schoenhaus v. Genesco, Inc*., 440 F.3d 1354, 1358-60 (Fed. Cir. 2006) (lexicography in file history by virtue of disclaimer of scope of claim term during prosecution).

B. Standard of Review

Pursuant to 28 U.S.C. § 636(b)(1)(B) and Federal Rule of Civil Procedure 72(b), a pretrial matter that is dispositive of a claim or defense may be assigned to a magistrate judge for a recommended disposition. If a party timely files specific written objections to the magistrate's proposed findings and recommendations, a district court judge "shall make a *de novo* determination of those portions of the report or specified proposed findings or recommendations to which objection is made." 28 U.S.C. § 636(b)(1)(C); *see also* Fed. R. Civ. P. 72(b)(3). In the matter before the Court, Plaintiffs' motion purports to object to the R&R as a dispositive pretrial matter pursuant to FRCP 72(b), and seeks *de novo* review of the R&R. Defendants understand the Court agrees the R&R is subject to FRCP 72(b).

Regardless of the standard of review employed, the reasons herein confirm that Judge Grewal's claim construction is correct.

IV. ARGUMENT

Judge Grewal construed "entire oscillator" to mean "an [oscillator] located entirely on the same semiconductor substrate as the [central processing unit] that does not require a control signal and whose frequency is not fixed by any external crystal." R&R at 1. This construction is correct because it accurately captures, as it must, the clear and unambiguous prosecution history

disclaimers made by the applicants in order to gain allowance of the '336 patent.

A. The Applicants Disclaimed Oscillators Whose Frequency Is Fixed By An External Crystal.

As Judge Grewal properly concluded, the applicants for the '336 patent clearly and unambiguously disclaimed oscillators whose frequency is fixed by an external crystal. Specifically, faced with repeated rejections of their patent claims by the examiner in the face of the prior art Magar patent (Ex. B, U.S. Patent No. 4,503, 500, "Magar"), the applicants again and again distinguished Magar by arguing that, unlike their claimed invention, Magar used an external crystal to fix the frequency of the oscillator. These repeated, clear arguments constitute clear disclaimers that must be reflected in the proper construction of the "entire oscillator" limitation. R&R at 4-5, 10.

1. Judge Grewal Correctly Concluded That The Applicants' Arguments Distinguishing Magar Constitute Disclaimers.

Every court that has addressed this issue has found that there was a disclaimer of claim scope by the applicants in their efforts to distinguish the Magar reference.[3] Plaintiffs nevertheless assert, as their initial argument, that there was no disclaimer whatsoever. Plaintiffs' Motion for *De Novo* Determination, Dkt. 107 ("Mot.") at 1, 7, 9. Plaintiffs are incorrect.

The examiner's first rejection over Magar noted that Magar disclosed a "clock generator" that is located on the same substrate as the central processing unit as shown in Figure 2a of Magar, reproduced below (annotations added):

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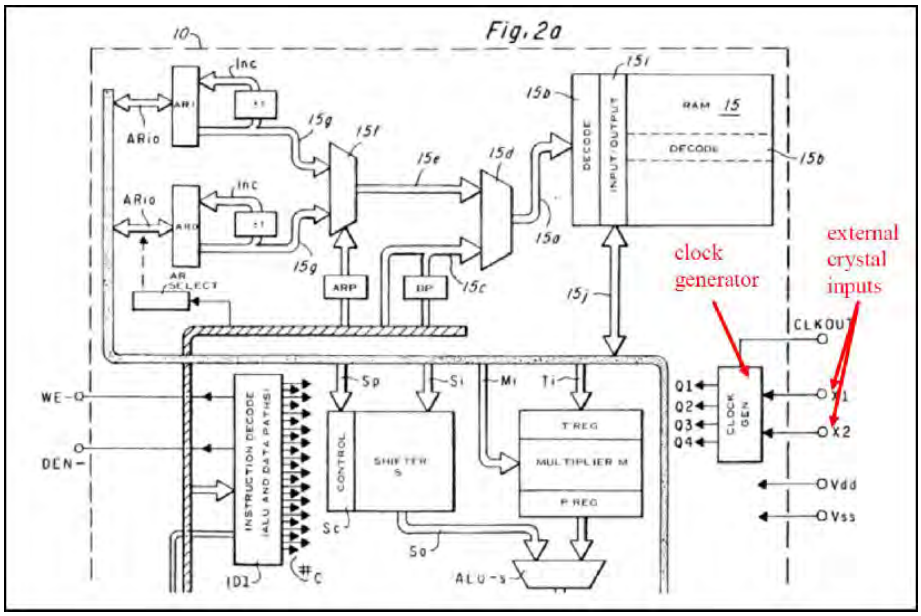
[3] R&R at 7; Ex. L (*Technology Properties Ltd. v. Matsushita Electric Industrial Co., Ltd.*, U.S.D.C., E.D. Tex., Civ. Action No. 2:05-CV-494 (TJW) (the "Texas Action"), Dkt. No. 259, June 15, 2007, Memorandum and Order) at 12 (finding disclaimer); Ex. M (*Certain Wireless Consumer Electronics Devices and Components Thereof*, Inv. No. 337-TA-853 (the "ITC Action"), April 18, 2013, Order No. 31) at 38-40 (finding disclaimer); Ex. N (ITC Action, March 21, 2014, Commission Opinion) at 24 (finding disclaimer); Ex. O (*HTC Corporation v. Technology Properties Ltd.*, U.S.D.C., N.D. Cal., Case No.: 5:08-cv-00882-PSG (the "HTC Action"), Dkt. No. 585, September 17, 2013, Order) at 11 and n.24.



Ex. C (April 3, 1997 Rejection) at 2 (TPL853_0002434). In response, applicants distinguished Magar by asserting that an external, fixed-frequency crystal controlled the frequency of the Magar clock:

> A review of the Magar reference shows that it is apparently no more pertinent than prior art acknowledged in the application, in that ***the clock disclosed in the Magar reference is in fact driven by a fixed frequency crystal, which is external to the Magar integrated circuit.***

Ex. D (July 7, 1997, Amend.) at 2 (TPL853_0002426).[4] In the same amendment, applicants emphasized that their claimed on-chip variable speed clock differs from the Magar clock because the Magar clock was "frequency controlled" by a "fixed frequency" external crystal that did not permit variations in oscillation speed due to PVT parameters, whereas the speed of the claimed variable speed clock varied with PVT parameters:

[4] Unless otherwise indicated, all emphasis in this brief is added by Defendants.

> Contrary to the Examiner's assertion in the rejection that 'one of ordinary skill in the art should readily recognize that the speed of the cpu and the clock vary together due to manufacturing variation, operating voltage and temperature of the IC [integrated circuit],' one of ordinary skill in the art should readily recognize that the speed of the CPU and clock ***do not*** vary together due to manufacturing variation, operating voltage, and temperature of the IC in the Magar processor . . . ***This is simply because the Magar microprocessor clock is frequency controlled by a crystal which is also external to the microprocessor.*** *Crystals are* ***by design fixed frequency devices*** *whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature.* ***The Magar microprocessor in no way contemplates a variable speed clock as claimed.***

Id. at 3-4 (TPL853_00002427-28) (first emphasis in original). By stating that the Magar microprocessor "in no way contemplates a variable speed clock as claimed" because the Magar clock is frequency controlled by an external fixed frequency crystal, the applicants clearly disclaimed, as Judge Grewal's construction states, a clock "whose frequency is fixed by an external crystal." R&R at 4, 10.

Although the above two statements themselves require a finding of disclaimer, the applicants did not end there. The applicants then told the examiner, in the same amendment, that even if the crystal that fixed the frequency of the Magar oscillator were located entirely on the same chip as the CPU, Magar ***still*** would not practice the claimed invention because the Magar clock could not vary with PVT parameters:

> ***[C]rystal oscillators have never***, to Applicants' knowledge, ***been fabricated on a single silicon substrate with a CPU***, for instance. ***Even if they were***, as previously mentioned, crystals ***are by design fixed-frequency devices*** whose oscillation frequency is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. ***The oscillation frequency of a crystal*** on the same substrate with the microprocessor ***would inherently not vary*** due to variations in manufacturing, operating voltage and temperature in the same way as the frequency capability of the microprocessor on the same underlying substrate***, as claimed.***

Ex. D (July 7, 1997 Amend.) at 4 (TPL853_00002428); R&R 4-5. This express disclaimer could not be clearer: the claims exclude oscillators using crystals that fix the frequency of the clock.

The PTO was not convinced by the applicants' arguments and issued a second rejection based on Magar. In response, the applicants amended their claims to explicitly require that the

"entire oscillator" be on the same integrated circuit substrate as the CPU. Ex. E (Feb. 10, 1998 Amend.) at 1-2 (TPL853_02954557-58).[5] Along with this amendment, the applicants again distinguished Magar, stating that the ***"essential difference***" between the claimed "entire oscillator" and the Magar oscillator is that the frequency of Magar's clock signals was determined (*i.e.*, fixed) by an external crystal:

> The ***essential difference*** is that the ***frequency or rate of the*** . . . ***signals*** [in the claimed invention] ***is determined by the processing and/or operating parameters of the integrated circuit*** containing the Fig. 18 circuit, ***while the frequency or rate of the*** . . . ***signals depicted in Magar Fig. 2a are determined by the fixed frequency of the external crystal*** . . . shown in Magar Fig. 2a.

Id. at 4 (TPL853_02954560). Again, this disclaimer could not have been clearer: the "essential difference" between Magar's oscillator and the claimed "entire oscillator" is that the frequency of Magar's oscillator is "determined by the fixed frequency of the external crystal," whereas the frequency of the claimed entire oscillator varies with PVT parameters. R&R at 5, 10.

Later in the same amendment, the applicants continued to distinguish Magar from their claimed invention on the ground that the frequency of the Magar oscillator was fixed by an external crystal, and made an additional disclaimer, *i.e.*, that their invention differed from Magar because the Magar oscillator also relied on the external crystal to oscillate:

> Magar's clock generator ***relies on an external crystal*** connected to terminals X1 and X2 ***to oscillate***, as is conventional in microprocessor designs. It is not an entire oscillator in itself. And with the crystal, ***the clock rate generated is also conventional in that it is a fixed, not a variable, frequency***. The Magar clock is comparable in operation to the conventional crystal clock 434 depicted in Fig. 17 of the present application for controlling the I/O interface ***at a fixed rate frequency, and not at all like the clock on which the claims are based***, as has been previously stated.

Id. at 3 (TPL853_02954559); R&R at 5 (finding that "[t]he applicants also disclaimed the use of

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[5] For example, prosecution claim 73, which ultimately issued as claim 6, was amended to recite "an entire oscillator disposed upon said integrated circuit substrate." Ex. E (Feb. 10, 1998 Amend.) at 1-2 (TPL853_02954557-558) (underlined text indicating addition through amendment).

an external crystal to cause clock signal oscillation").

The statement that Magar's clock is conventional in that its rate (*i.e.*, frequency) is fixed by the external crystal, and thus "not at all like the clock on which the claims are based," is yet another disclaimer of clocks whose frequencies are fixed by external crystals. That the applicants also disclaimed reliance on an external crystal "to oscillate" does not negate the effect of the applicants' repeated disclaimer of oscillators whose frequencies are fixed by external crystals because, as Judge Grewal correctly stated, a correct claim construction must reflect all disclaimers made during prosecution, not just some of them. R&R at 11 and n.43 (citing *Krippelz v. Ford Motor Co.*, 667 F.3d 1261, 1267 (Fed. Cir. 2012), *Am. Piledriving*, 637 F.3d at 1336, and *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 979 (Fed. Cir. 1999)); *see also Andersen Corp. v. Fiber Composites, LLC*, 474 F.3d 1361, 1374 (Fed. Cir. 2007).

Confirming, again, that they were disclaiming claim scope, the applicants concluded their arguments about Magar by "specifically distinguish[ing]" the claimed entire oscillator from Magar on the same two bases: (1) the frequency of the Magar oscillator was fixed by the crystal; and (2) the Magar oscillator required the crystal to oscillate:

> The Magar teaching . . . is specifically distinguished from the instant case in that it is both ***fixed frequency*** (*being crystal based*) and *requires an external crystal or external frequency generator*.

Ex. E (Feb. 10, 1998 Amend.) at 5 (TPL853_02954561).

The applicants' disclaimers regarding Magar were clear: they repeatedly told the examiner the claimed "entire oscillator" does not include oscillators whose frequencies are fixed by an external crystal (as well as that the claimed oscillator does not require an external crystal to oscillate). As established above, longstanding Federal Circuit precedent requires that the applicants' disclaimers be reflected in the Court's claim construction. Judge Grewal was thus correct in concluding that there was a disclaimer and, in particular, that the "applicants surrendered any oscillator that like Magar's is fixed by an off-chip crystal." R&R at 2, 10-11. Judge Grewal was therefore also correct in construing "entire oscillator" to mean, in part, "an oscillator . . . whose frequency is not fixed by an external crystal." *Id*. at 2.

2. Plaintiffs' Criticisms Of Judge Grewal's Construction Lack Merit.

Plaintiffs' criticisms of Judge Grewal's construction are flawed throughout. First, Plaintiffs incorrectly re-cast Judge Grewal's construction and then challenge the incorrectly characterized construction. In particular, Plaintiffs argue that the statements made by applicants in their July 7, 1997 amendment do "not support Judge Grewal's construction that the 'entire oscillator' is not 'fixed by any off-chip ***oscillator***' . . ." Mot. at 9. However, that is not Judge Grewal's construction; rather, consistent with the applicants' actual disclaimers, Judge Grewal's construction excludes oscillators whose frequency is "fixed by any external ***crystal***." R&R at 2. Thus, Plaintiffs' arguments regarding whether Magar included an "off-chip oscillator" are misplaced. *See* Mot. at 9 ("there is no mention of an off-chip oscillator"), 10 ("controlled by the off-chip oscillator"), 10 ("but say nothing of an off-chip oscillator fixing the frequency").

Second, Plaintiffs' criticisms of Judge Grewal's construction are largely premised upon their ***current*** characterization of the design of Magar. Mot. at 8-10. This line of criticism is fundamentally flawed, both factually and legally. As an initial matter, Plaintiffs' arguments are premised upon their litigation counsel's assertion that Magar had no on-chip oscillator and that the clock signal in Magar was generated by the off-chip crystal. *Id*. at 8. However, as established above, the examiner cited the ***on-chip*** "clock generator" shown in Fig. 2a of Magar in his claim rejection. *See* Ex. C (April 3, 1997 Rejection) at 2 (TPL853_0002434). Plaintiffs' counsel's current argument that Magar had no on-chip oscillator is just that – attorney argument.

Moreover, controlling Federal Circuit precedent precludes arguments, like Plaintiffs' current arguments, where the patentee attempts to avoid a finding of disclaimer by arguing, in the infringement litigation, about what the prior art does and does not disclose. Rather, the disclaimers must be measured by what the applicants ***actually said*** during prosecution, ***not what they arguably could have said*** instead. *North Am. Container Inc. v. Plastipak Packaging Inc.*, 415 F.3d 1335 (Fed. Cir. 2005).

In *North Am. Container*, the claim term at issue was "wherein said inner wall portions are generally convex." *Id*. at 1341. The applicants in that case made the following argument to the examiner during prosecution to overcome two prior art patents, Jakobsen and Dechenne:

> The shape of the base as now defined in the claims differs from those of both the Dechenne patent, wherein the corresponding wall portions 3 are *slightly concave* . . . and the Jakobsen patent, wherein the entire re-entrant portion is clearly *concave in its entirety*. This is also generally true of all of the prior art known to the applicant and/or referred to by the examiner.

Id. at 1340. A special master in subsequent district court litigation determined that the plain meaning of the "generally convex" limitation was broad enough to include walls with some straight and some concave points, so long as the majority of points were convex. However, notwithstanding that determination, the special master further concluded that the correct construction of "generally convex" required an additional negative limitation due to the above-stated argument made by the applicants during prosecution: the wall must have "***no concave points***." *Id*. at 1342-43 (emphasis added). In affirming this construction, the Federal Circuit rejected the argument that the scope of the disclaimer was limited to walls that were entirely concave and therefore could encompass walls with some concave points:

> We are not persuaded by NAC's argument that the applicant intended only to distinguish his invention from the prior art on the basis that the inner walls in the prior art bottles are entirely concave. ***Although the inner walls disclosed in the Dechenne and Jakobsen patents may be viewed as entirely concave, that is not what the applicant argued during prosecution to gain allowance for his claims.*** The applicant stressed the difference in the extent of the concavity between the Dechenne and Jakobsen patents, noting that Dechenne is "slightly concave," whereas Jakobsen is "clearly concave in its entirety." Such a distinction would have been unnecessary if the only point that the applicant intended to make was that both prior art patents disclosed inner walls that are entirely concave.

Id. at 1345-46.

Thus, the Federal Circuit made clear in *North Am. Container* that the scope of the disclaimer is measured by the words used by the patentee, and can be broader than what is necessary to overcome the prior art. This holding was and remains in accord with well-established Federal Circuit precedent. *See, e.g.*, *Atofina v. Great Lakes Corp.*, 441 F.3d 991, 998 (Fed. Cir. 2006) ("[t]hat the applicants only needed to surrender nickel-chromium catalysts to avoid a prior art reference does not mean that its disclaimer was limited to that subject matter"); *Marctec LLC v. Johnson & Johnson*, 394 Fed. App'x 685, 687 (Fed. Cir. 2010) ("[l]imitations clearly adopted by the applicant during prosecution are not subject to negation during litigation, on the argument that the limitations were not really needed in order to overcome the reference");

Saffran, 712 F.3d at 559 (holding that arguments made to distinguish prior art "preformed chamber" constitute a disclaimer of not only the prior art "preformed chamber" but also a broader disclaimer of anything other than a "sheet.").[6]

As established above in detail, the applicants for the '336 patent repeatedly argued that their claimed "entire oscillator" was different from Magar's oscillator because the frequency of the Magar clock was fixed by an external crystal. *See, e.g.*, Ex. D (July 7, 1997 Amend.) at 2-4 (TPL853_00002426-28) ("the clock disclosed in the Magar reference is in fact driven by a fixed frequency crystal, which is external to the Magar integrated circuit"; "the Magar processor clock is frequency controlled by a crystal which is also external to the microprocessor"; Ex. E (Feb. 10, 1998 Amend.) at 3-5 (TPL853_02954559-61) ("the essential difference is that . . . the frequency or rate of [the clock] signals depicted in Magar Fig. 2a are determined by the fixed frequency of the external crystal"; "[a]nd with the crystal, the clock rate generated is also conventional in that it is a fixed, not variable, frequency"; "[t]he Magar teaching . . . is specifically distinguished from the instant case in that it is . . . fixed frequency (being crystal based)"). The scope of the applicants' disclaimer must be measured – as Judge Grewal correctly did – by these statements, and not by the characterization of the prior art that Plaintiffs are now making in this litigation.

3. Plaintiffs' Proposed Alternative Construction Is Both Incorrect And Invites Confusion And Further Argument.

Perhaps recognizing the error of their "no disclaimer" position, Plaintiffs close their argument regarding Magar by stating: "Finally, if any disclaimer with respect to Magar is appropriate, it is one that prohibits a clock signal being *generated* from an off- chip oscillator." Mot. at 11 (emphasis in original); *see also id.* at 10 ("Applicants' statements could support a construction that the clock signal provided to the CPU does not originate from or is not generated by an external oscillator"). This alternative construction – which Plaintiffs are now proposing for

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[6] *See also* R&R at 9 (quoting *Norian Corp. v. Stryker Corp.*, 432 F.3d 1356, 1361 (Fed. Cir. 2005) for the proposition that "[t]here is no principle of patent law that the scope of surrender of subject matter made during prosecution is limited to what is absolutely necessary to avoid a prior art reference that was the basis for an examiner's rejection.").

this first time in this (or any other) litigation – must be rejected because it fails to fully and accurately capture the applicants' prosecution history disclaimers, which, as established above, is contrary to well-established Federal Circuit precedent. The construction also should be rejected because prior litigation over this patent has shown that the word "generate" is unclear, is likely to cause jury confusion, and invites continued argument over its meaning and scope.

First, Plaintiffs' substitution of "off-chip oscillator" in their proposed construction for "off-chip crystal" improperly narrows the scope of the prosecution history arguments made by the applicants. As established above, each of the above-cited disclaimers refers to an external *crystal*, not an external *oscillator*. The construction should therefore be phrased in terms of an "external crystal" as those were the words used by the applicants. *North Am. Container*, 415 F.3d at 1345-46; *Atofina*, 441 F.3d at 998; *Marctec*, 394 Fed. App'x at 687; *Saffran*, 712 F.3d at 559.

Second, the term "generated" should not be used in place of "fixed." As shown above, the term "fixed" is used throughout the disclaimers (in the phrases "fixed frequency" and "fixed rate frequency"), and the disclaimers also use the comparable words "controlled" (in the phrase "controlled frequency") and "determined" (in the phrase "the frequency or rate of the [clock] signals . . . are determined"). Each of these terms reflects the applicants' disclaimer of frequency rate control by the external crystal, which is the essence of the applicants' main disclaimer in Magar. The "generation" of the clock signal does not as directly reflect this disclaimer as does the term "fixed," and Plaintiffs do not tie their proposed use of the term "generated" to the actual words of applicants' disclaimers.

Moreover, the word "generated" more closely aligns with the applicants' further disclaimer that "Magar's clock generator relies on an external crystal . . . to oscillate." Ex. E (Feb. 10, 1998 Amend.) at 3 (TPL853_02954559). As established above, this disclaimer is in addition to the applicants' more specific fixed frequency disclaimer. While Judge Grewal recognized this additional disclaimer in the body of his report and recommendation ("The applicants also disclaimed the use of an external crystal to cause clock signal oscillation"), this disclaimer is not expressly reflected in Judge Grewal's construction. It would be incorrect to inject the term "generated" into the frequency control disclaimer that is expressly reflected in

Judge Grewal's construction, when that term instead more directly pertains to the second disclaimer that is not expressly reflected in the construction. R&R at 5.[7]

Furthermore, the prior litigation history concerning this patent demonstrates that the use of the word "generate" in the claim constructions is problematic. In the prior ITC Action, Administrative Law Judge Gildea adopted a construction that included the word "generate." Ex. M (ITC Claim Construction Order) at 21-40. TPL then proceeded to argue that the process of generating a clock signal did not include fixing the frequency of the signal. *See, e.g.*, Ex. Q (ITC Initial Determination) at 108-110. As a result, this issue required further litigation, which led to the ALJ ultimately making clear that his "generate" construction excluded oscillators whose frequency was fixed by an external crystal: "the process of setting the frequency of a clock signal and generating a clock signal are inseparable, because a clock signal must have a frequency, since its sole purpose is to provide a frequency for timing the operation of devices." *Id*. at 121-122. The Commission agreed. Ex. N (ITC Final Determination) at 24 ("The patent applicants' statement in the final sentence quoted above, in particular, shows that the applicants intended to disclaim, not only an external crystal/frequency generator, but also a fixed frequency, crystal controlled generator.").

Likewise, in the prior HTC Action, Judge Grewal provided the jury with an instruction that the "entire oscillator" claim term "is properly understood to exclude any external clock used to generate the signal used to clock the CPU." Ex. J (Dkt. No. 646 jury instructions) at 26; Ex. K (Dkt. No. 616 Order re Emergency Motion) at 2. However, during deliberations, the jury expressed uncertainty as to the meaning of the word "generate" in the jury instruction and sought clarification of this term. Ex. P (Trial Tr.) at 1641:21–1644:14.

Accordingly, the use of the term "fixed" in Judge Grewal's construction both more accurately reflects the applicants' actual disclaimers, and will avoid potential future argument and

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[7] Reflecting the two disclaimers in the prosecution history, Defendants proposed a construction to Judge Grewal that stated, in part, that the claimed oscillator "does not rely on . . . an external crystal . . . to cause clock signal oscillation or control clock signal frequency." R&R at 8.

confusion over the meaning and scope of the word "generate."

B. The Applicants Disclaimed Oscillators That Require A Control Signal.

In addition to disclaiming oscillators whose frequency is fixed by an external crystal, the applicants clearly and unambiguously disclaimed oscillators that require a control signal, as Judge Grewal correctly concluded. R&R at 1, 5-6, 11. These disclaimers were made by the applicants in attempting to distinguish their claimed "entire oscillator" from the prior art Sheets patent (Ex. H, U.S. Pat. No. 4,670,837, "Sheets"). Sheets discloses a voltage controlled oscillator whose frequency is set by writing a control word to the voltage controlled oscillator. Ex. H (Sheets) at col. 2, ll. 54-68.

1. The Applicants' Arguments Regarding Sheets Constitute Disclaimers.

Although Plaintiffs argue there was no control signal disclaimer during prosecution, such a disclaimer was found to exist not only by Judge Grewal, but also in the Texas Action and the ITC Action.[8] This is because applicants distinguished their "present invention" from Sheets' voltage controlled oscillator on the basis that Sheets' voltage controlled oscillator requires (*i.e.*, relies upon or needs) frequency control information from the on-chip microprocessor:

> The ***present invention does not similarly rely upon provision of frequency control information to an external clock***, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, since the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance. ***Sheets' system for providing clock control signals to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention***.

Ex. F (April 11, 1996 Amend.) at 8 (TPL853_02954574); R&R at 5. Because the applicants referred to the "present invention" in this statement, their disclaimer of clock control signals applies to all claims. *See, e.g., Ballard Med. Prods. v. Allegiance Healthcare Corp.*, 268 F.3d

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[8] R&R at 7; Ex. L (Texas Action, Dkt. No. 259, June 15, 2007, Memorandum and Order) at 11-12; Ex. M (ITC Action, April 18, 2013, Order No. 31) at 40-41.

1352, 1360-62 (Fed. Cir. 2001); R&R at 6 n.15.

When the examiner thereafter continued to maintain the rejection based upon Sheets, the applicants went even further and disclaimed the use of controlled oscillators altogether, regardless of whether the oscillator is on-chip or not:

> Even if the examiner is correct that the variable clock in Sheets is in the same circuit as the microprocessor of system 100, ***that still does not give the claimed subject matter. In Sheets, a command input is required to change the clock speed.*** In the present invention, the clock speed varies correspondingly to variations in operating parameters . . . ***No command input is necessary to change the clock frequency***.

Ex. G (January 8, 1997 Amend.) at 4 (TPL853_00002449); R&R at 6. Thus, according to the applicants, controlling even an on-chip oscillator's speed using a command signal generated on the chip "does not give the claimed subject matter." *Id*. Indeed, in a later amendment, the applicants left no doubt that, unlike "all cited references," the claimed oscillator is completely free of inputs and extra components:

> ***Crucial to the present invention*** is that . . . when fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together. ***This differs from all cited references in that . . . the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so.***

Ex. D at 5 (TPL853_00002429); R&R at 6.[9]

Thus, as Judge Grewal correctly concluded, the "applicants distinguished Sheets repeatedly on the ground that Sheets requires control signals, frequency control information or command inputs." R&R at 11. These arguments, distinguishing the claimed "entire oscillator" from Sheets, constitute clear and unambiguous disclaimers that must be reflected in the claim construction. *Am. Piledriving*, 637 F.3d at 1326. Accordingly, Judge Grewal correctly construed

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[9] When a patentee uses terms such as "crucial to" and "in the present invention," this use has a special effect on the scope of the claim. *See Microsoft Corp. v. Multi-Tech. Sys., Inc.*, 357 F.3d 1340, 1351-52 (Fed. Cir. 2004) (construing claim to require a feature that was "central to the functioning of the claimed invention").

"entire oscillator" to exclude oscillators "that require a control signal." R&R at 1, 5-6, 11; *Southwall Techs.*, 54 F.3d at 1576; *Rheox*, 276 F.3d at 1325.

2. Plaintiffs' Criticisms Of Judge Grewal's Construction Lack Merit.

Plaintiffs criticize the control signal portion of Judge Grewal's construction on three grounds. First, Plaintiffs characterize how the system described in Sheets allegedly works (Mot. at 11-12), and then offer their current attorney argument as to why Sheets is distinguishable from the claimed invention of the '336 patent. *Id*. at 12. However, as established above in connection with the Magar reference, Federal Circuit law is clear that disclaimer is measured by what the applicants actually said during prosecution, not by what they could have said instead during prosecution, or by what the patentee argues during litigation. *See* § IV.A.2, *supra*.

Second, Plaintiffs assert that the construction is too broad because it applies to "control signals generally," and that the disclaimer should instead be limited to "command, programmed or manual control inputs." Mot. at 13. However, as established above, the specific language the applicants actually used to distinguish Sheets includes not only "command input" and "manual or programmed inputs," but also "clock control signals" and "control information." Again, the scope of the disclaimer must be determined by what the applicants actually said, and Plaintiffs' proposed alternative does not cover the full breadth of the applicants' disclaimers. *See* §§ III and IV.A.2, *supra*.

Third, Plaintiffs argue that Judge Grewal's construction prohibits the entire oscillator from requiring a control signal "for ostensibly any purpose." Mot. at 13. However, it is clear from Judge Grewal's Report and Recommendation that the prohibition on requiring control signals relates to requiring control signals to control or change frequency. *See* R&R at 5 ("the applicants distinguished their 'present invention' from microprocessors that rely on ***frequency control information*** from an external source"); 6 ("Thus, according to applicants, ***controlling the on-chip oscillator's speed*** using a command signal 'does not give the claimed subject matter.'"). These statements are consistent with the construction that Defendants proposed to Judge Grewal, which provided in relevant part that the claimed oscillator "does not rely on a control signal . . . to . . . control clock signal frequency." R&R at 8.

Moreover, Plaintiffs' proposed alternative construction – excluding oscillators "that require command, manual, or programmed inputs to *change* frequency" (Mot. at 15) – is incorrect. First, as established above, the applicants' disclaimers were not limited to "command, manual or programmed inputs." Second, Plaintiffs' proposed construction is limited to "changing frequency" and omits "controlling" the frequency. This is incorrect as the applicants also distinguished Sheets on basis of the "frequency control." Ex. F (April 11, 1996 Amend.) at 8 (TPL853_02954574); R&R at 5.

V. CONCLUSION

Judge Grewal's construction of the "entire oscillator" limitation of the asserted claims of the '336 patent is correct and should be adopted by the Court because it accurately reflects the clear and unambiguous disclaimers made by applicants during prosecution.

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ATTESTATION

I, Aaron Wainscoat, am the ECF User whose ID and password are being used to file this Defendants' Response to Plaintiffs' Motion for *De Novo* Determination. In compliance with Civil Local Rule 5-1(i)(3), I hereby attest that the signatories listed above have read and approved the filing of this brief.

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Appx3550-4337 has been removed from the Appendix in the interest of brevity. These pages are the exhibits to Defendants' Response to Plaintiffs' Motion for De Novo Determination of Dispositive Matter Referred to Magistrate Judge, or, in the Alternative, Motion for Relief from Nondispositive Pretrial Order of Magistrate Judge, and are referred to on p. 3 of Appellants' Opening Brief in discussing the background of the district court litigation. These pages are not referred to again in any of the parties' briefs.

The exhibits can be accessed via PACER (Case No. 3:12-cv-03865-VC; Dkt. No. 106; (N.D. Cal.))

to discuss the basics of microprocessors and electronic devices.

THE COURT: Before you get to your discussion, Mr. Cecil, may I just ask, is the '336 the subject of any current proceedings at the PTO that you're aware of?

MR. CECIL: No, your Honor.

THE COURT: All right. Go ahead.

MR. CECIL: So an electronic device typically would have some sensors such as a camera, some memory, and then most importantly a microprocessor. And that -- that microprocessor, the CPU, is going to be comprised of various transistors which are used to build the logic gates employed inside the processor.

An interesting point to remember about the transistors is that from one microchip to another, even though manufactured with the same mass or blueprints, there's -- there's going to be an variations or there may be some variations in the speed of the transistors.

For example, each transistor is going to be subject to speed differences based on, for example, the voltage or the temperature or the manufacturing process. So even transistors that are manufactured in the same week at the same facility could have some -- some differences based on the humidity in the room that day.

So today, when -- when these -- when these chips are

manufactured --

(Demonstrative displayed.)

MR. CECIL: -- the manufacturers will sort of sort individual chips on a particular wafer into different bins. You know, they probably say, "good," "better," and "best" instead of "slow," "medium," and "fast." But then they sell those at different prices to device manufacturers and -- and others that use the chips.

THE COURT: Mr. Smith may correct me, but I seem to recall a slide that looked almost exactly like this one in the trial.

MR. CECIL: This one is very familiar. I won't run the animation because I -- I think you might recall it.

THE COURT: I do.

MR. SMITH: It was identical, your Honor.

THE COURT: Thank you.

MR. CECIL: So because of the differences in the speed capabilities of the transistors that make up a microprocessor, it's explained in the specification of the '336 that electronic manufacturers in the past were restricted to designing for the worst-case scenario. So when selecting a clock frequency for the processor, they would need to design a chip that would only operate at what is sort of the bottom of the operational range.

THE COURT: The so-called rate-limiting factor.

MR. CECIL: That's -- That's right, your Honor.

Otherwise, if you provided a clock that was too fast, it would result in some computing errors. A change in transistor state wouldn't have time to propagate before the next clock cycle came in and so you'd get collisions and some "badness," as we said in engineering school.

Oftentimes, in the prior art, microprocessor clock signals were provided by this -- this quartz crystal. This image probably also looks familiar.

(Demonstrative displayed.)

MR. CECIL: So this quartz crystal operates at a fixed frequency when a voltage is -- is applied across it. And, importantly, that crystal is going to be external to the silicon that the integrated circuit's on since it's impossible to grow quartz on silicon --

THE COURT: Can I ask one question about that quartz crystal, Mr. Cecil, which has been on my mind for some time?

When we say that the frequency of the crystal is fixed when a voltage is applied across it, in reality, there's some modest variation going on, but it's -- is it fair to say that it's sufficiently fixed for purposes of use as a reference signal?

MR. CECIL: It is, your Honor, because, in fact, that's how it is used.

THE COURT: Okay.

MR. CECIL: So --

(Demonstrative displayed)

MR. CECIL: -- we can see that this is -- this is what quartz crystal looks like. You put it into a particular circuit, and it works sort of like a tuning fork. When you apply that voltage, it resonates at a consistent frequency.

(Demonstrative displayed.)

MR. CECIL: So the -- the patent claims of the '336 are a little bit different. What they do is they involve the use the of an on-chip oscillator -- so rather than the crystal that we saw before, the -- the '336 envisions an oscillator that's on the chip so that the circuitry which generates the signal that's used to clock the CPU is going to be subject to the same types of parameter variations that we talked about earlier, so when the --

THE COURT: Voltage, temperature?

MR. CECIL: That's right. That's right, your Honor. So when --

(Demonstrative displayed.)

MR. CECIL: This might also look familiar. When the -- When the CPU runs fast, the -- the clock's going to run fast. And the same thing when it runs slow, the clock will run slow.

(Video animation playing.)

(Pause in the proceedings.)

root for the SEC or the Pac 12.

DR. SUBRAMANIAN: I root for the SEC.

THE COURT: I can't hold that against you.

Go ahead.

DR. SUBRAMANIAN: So I -- I believe that handouts have been given to you.

THE COURT: I have them.

DR. SUBRAMANIAN: I'll go ahead and start.

Good morning, your Honor. I'm Vivek Subramanian, and I'll be providing an overview of various technological underpinnings that are relevant for your consideration.

(Demonstrative displayed.)

DR. SUBRAMANIAN: And I'm going to talk about four topics. The first three topics, specifically microprocessors, clocking of microprocessors, and phase-locked loops are really to give you the technological background at the time prior to and as of the '336 patent, so that will sort of set the stage.

And then I'll talk about the '336 patent specifically and, again, discuss the technological underpinnings of that patent.

THE COURT: Sure.

DR. SUBRAMANIAN: So to begin, I'm going to talk about microprocessors. And I think they actually use the same demonstrative and -- but I'm going to focus on a specific aspect.

And the top left of slide 4, what you see is a die photo

of an arbitrary microprocessor. Now, this die photo is actually -- it's a colorized version of an optical image you could take -- if you were to peel back a microprocessor and look at it, it would look like this.

In terms of dimensions, it's on the order of several -- several millimeters to a couple of centimeters on a side. And within this microprocessor, depending on the age of the microprocessor, the first microprocessors which were developed in the 1970's had a couple of thousand transistors on them.

At the time of the patent, they were hundreds of thousands of transistors to up about a million transistors on a die. So there's a million transistors sitting on this die spread across this two-dimensional surface. And each of these transistors is involved in implementing various functions.

So some of the transistors may be involved in computations. Some may be involved in speaking to the external world. You'll notice if you look at the bottom right, what you see is the microprocessor is on a board, and there's other components on that board.

And that's pretty typical of a computational system, is you'll have a microprocessor, and it may have to talk to the external world and in addition, has to talk to other parts of the microprocessor as well.

Now, one of the really important consequences of having so many transistors performing so many functions in a

microprocessor is that timing gets very important. In other words, a transistor on the top left, if it's performing some operation, has to do that operation at the correct time such that some transistor on the bottom right is able to respond at the right time. And so timing ends up being very important, and that's why we get to the next topic I'm going to talk about which is clocking.

(Demonstrative published.)

DR. SUBRAMANIAN: And really what I'm going to talk about in clocking is how we achieve that timing. The key idea is I want to synchronize all my operations such that --

(Demonstrative published.)

DR. SUBRAMANIAN: -- an operation that's on the top left of the microprocessor is in a deterministic way timed to match the requirements of something happening somewhere else on that microprocessor.

So going on, then, to slide 6 --

(Demonstrative published.)

DR. SUBRAMANIAN: -- I'll talk about how we achieve the timing. And the way we achieve the timing is we use a chock signal. And fundamentally, a clock signal has two important characteristics that we care about. A clock signal is an electrical signal, and it's an oscillating electrical signal and it's periodic. In other words, it goes between two values typically.

So for example here on slide 6, it's shown as going between a 0 and a 1. Now, that 0 and the 1 is a digital -- it's sort of a nomenclature. In fact, what that means is it's going from a low voltage to a high voltage. So in a battery-operated system, it might go from 0 volts to 3 volts as an example and then back down again.

And there's a periodicity to it. In other words, there's a repetition rate so it's described by the frequency. And that frequency is what's used to establish the timing of the whole system.

THE COURT: And frequency is one over period, if I remember correct?

DR. SUBRAMANIAN: That's right frequency is one over period. So period is in terms of time. Frequency is in terms of hertz.

And the way we achieve this synchronization is we design the circuitry to respond to that period -- periodic up-and-down nature of the clock. So I might design a circuit that in the top left of the -- my microprocessor perform some operation at this first rising edge, and then some other circuit which is very far away from it, maybe several millimeters away, several hundred thousand transistors away, will know that that operation was performed on that edge so it will be able to respond accordingly.

And so this is why we care about these clocks, because

THE COURT: Please.

(Demonstrative published.)

(Demonstrative published.)

DR. SUBRAMANIAN: Okay. So now how do we generate clocks? Well, the standard way of generating clocks for decades at this point -- in fact, this predated semiconductors. These were used even when we were using vacuum tubes, is using quartz crystals.

Now, the quartz crystal is a crystalline material, so it's a single crystal of quartz, and it is actually a mechanical tuning fork. If you hit with it a hammer, it will vibrate. And its frequency of vibration is dependent on the mass of crystal, so the larger crystal vibrates at a lower frequency, a smaller crystal vibrates at a high frequency.

So in the case of making these quartz crystals --

(Demonstrative published.)

DR. SUBRAMANIAN: -- they are cut to very precise dimensions to get very precise control of the mass.

THE COURT: So that either when the same pressure is applied, the same frequency results or the same voltage is applied.

DR. SUBRAMANIAN: Correct. So we haven't --

THE COURT: More consistency.

DR. SUBRAMANIAN: -- stimulate it. Yes, that's right. But the key is you knock it with a hammer or with a

to protect the crystal from the external environmental. Since it depends on mass, if I just left it exposed to air, a dust particle falling on the crystal would change the oscillation frequency so that's why we have it inside this can.

And now, once we've done that, it becomes a very useful timing reference.

Now, your Honor, you asked previously how precise are they, modern crystals are -- in fact, crystals for the last 40 years have been available with variances on the order of tens of parts per million. That's the typical range. In fact, you can get lower than that today -- they tend to be more expensive the more precise you want them, but typical range is tens of parts per millions.

THE COURT: And so for all purposes that we care about today anyway, I should understand that these are no or so extremely low variance crystals that the -- that the frequency from one moment to the next is constant.

DR. SUBRAMANIAN: That's correct. Within -- Within the orders of tens of parts per million. That's right.

So that's what I show on slide 8.

(Demonstrative published.)

DR. SUBRAMANIAN: Now, the crystal is not on the semiconductor chip. It's built separately. For various reasons. For one thing, it's very hard to deposit single-crystal quartz on silicon. In fact, it's effectively

THE COURT: Go ahead.

(Demonstrative published.)

DR. SUBRAMANIAN: So now going on to the next piece, I've already mentioned the voltage-controlled oscillator -- well, let me show you what a voltage-controlled oscillator looks like, the internal.

(Demonstrative published.)

DR. SUBRAMANIAN: So this is on slide 21, and a voltage -- one type of voltage-controlled oscillator that exists is a voltage-controlled oscillator that's implemented using a ring circuit but a specific type of ring circuit.

So what I have here is -- and your honor's seen this before. You've seen a -- generically a ring oscillator before. And a ring oscillator is an odd number of inverters connected in a loop. So when you have an odd number of inverters connected in a loop, it's inherently unstable.

And the reason is the following. Let's say my left-most inverter on slide 21 has an input of 0, output is 1. Second, inverter, output is 0; third inverter, output is 1. So I initial condition was this was a 0, now the feedback is a 1, so it's unstable.

So what causes it to oscillate is the delay across each of those inverters means that the signal takes a little while to move through the system. And so when the 0 is going to flip to the 1, the time it takes to flip to the 1 is dependent on

the delay across each of these elements.

In a voltage-controlled oscillator, that delay is set by the controlled voltage.

THE COURT: And is the delay also a function of the number of inverters?

DR. SUBRAMANIAN: The total delay is, indeed, a function of the number of inverters, so for --

THE COURT: And a total number of inverters always has to be an odd number.

DR. SUBRAMANIAN: It as always has to be an odd number; that's right. So, for example here, I have three inverters, and let's say arbitrarily I've set my VCO to run at two gigahertz. If I went to 5 inverters, all else being equal, it will be slow.

THE COURT: Okay.

DR. SUBRAMANIAN: So that's the general idea here, and so you'll notice in this VCO, what you have is actually you have two different voltage nomenclatures. You will still have a supply voltage because electronic circumstances need power supplies to operate. But specifically in these voltage-controlled oscillators, there is a control voltage that is used. And that, of course, in the PLL is based on the crystal. So that's what we see in slide 21.

(Demonstrative published.)

DR. SUBRAMANIAN: Now, there are other types of

(*Counsel listed on signature page*)

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. HUAWEI TECHNOLOGIES CO., LTD., et al., Defendants.	Case No. 3:12-cv-03865-VC (PSG) **STIPULATION FOR ENTRY OF FINAL JUDGMENT BASED ON THE COURT'S CLAIM CONSTRUCTION**
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. ZTE CORPORATION, et al., Defendants.	CASE NO. 3:12-cv-03876-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. SAMSUNG ELECTRONICS CO., LTD., et al., Defendants.	Case No. 3:12-cv-03877-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. LG ELECTRONICS, INC., et al., Defendants.	Case No. 3:12-cv-03880-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. NINTENDO CO., LTD, et al. Defendants.	Case No. 3:12-cv-03881-VC (PSG)

WHEREAS, Plaintiffs Technology Properties Limited LLC, Phoenix Digital Solutions LLC, and Patriot Scientific Corporation's (collectively, "Plaintiffs") asserted that Defendants Huawei Technologies Co., Ltd., Huawei Device Co., Ltd., Huawei Device USA, Inc., Futurewei Technologies, Inc., Huawei Technologies USA, Inc., ZTE Corporation, ZTE (USA) Inc., Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., LG Electronics, Inc., LG Electronics U.S.A., Inc., Nintendo Co., Ltd., and Nintendo of America Inc. (collectively, "Defendants") in the above-titled and numbered civil cases (collectively, "this Action") infringe at least one claim of U.S. Patent No. 5,809,336 (the "'336 patent"); and

WHEREAS, this Court construed the term "an entire oscillator disposed upon said

integrated circuit substrate" used in the asserted claims of the '336 patent in its Order Adopting Magistrate Judge's Report and Recommendation on claim construction, dated November 9, 2015 (the "Claim Construction Order");

Plaintiffs and Defendants (together, the "Parties"), by and through their undersigned counsel, hereby stipulate and agree as follows:

1. The term "an entire oscillator disposed upon said integrated circuit substrate" appears in asserted independent claims 6 and 13 of the '336 patent.

2. All asserted claims ultimately depend from either claim 6 or claim 13 and, therefore, include the term "an entire oscillator disposed upon said integrated circuit substrate."

3. In the Claim Construction Order, the Court construed the term "an entire oscillator disposed upon said integrated circuit substrate" as "an [oscillator] located entirely on the same semiconductor substrate as the [central processing unit] that does not require a control signal and whose frequency is not fixed by any external crystal" (the "Entire Oscillator Construction").

4. As a result of the Court's Claim Construction Order, the Parties agree that all of the accused products of all Defendants in this Action do not infringe the asserted claims of the '336 patent under the Entire Oscillator Construction.

5. Based on the above, the Parties request that the Court enter a final judgment of non-infringement against Plaintiffs and for Defendants with respect to all accused products of all Defendants on all asserted claims of the '336 patent, subject to the Parties' right to appeal.

6. The Parties also request that the Court enter a final judgment for Defendants and against Plaintiffs on Defendants' respective counterclaims seeking declaratory judgment of non-infringement and Defendants' respective affirmative defenses of non-infringement, and declare the '336 patent not infringed by Defendants.

7. The Parties agree that all other claims, counterclaims, defenses, or other matters which have been asserted, including Defendants' counterclaims of patent invalidity, are dismissed without prejudice, and Plaintiffs will not oppose any attempt by Defendants to assert any such defenses or counterclaims following any remand.

8. The parties intend to preserve the status quo on all other issues in the event an appeal results in remand for further proceedings in this Court. Following any remand, the Parties will request that the Court order a Case Management Conference to determine the schedule for further proceedings.

9. The Parties respectfully request that the Court enter the Final Judgment attached hereto.

10. Each party shall bear its own costs and attorneys' fees.

IT IS SO STIPULATED.

Dated: November 12, 2015

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ATTESTATION

I, Aaron Wainscoat, am the ECF User whose ID and password are being used to file this STIPULATION FOR ENTRY OF FINAL JUDGMENT BASED ON THE COURT'S CLAIM CONSTRUCTION. In compliance with Civil Local Rule 5-1(i)(3), I hereby attest that the signatories listed above have read and approved the filing of this brief.

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ATTACHMENT

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. HUAWEI TECHNOLOGIES CO., LTD., et al., Defendants.	Case No. 3:12-cv-03865-VC (PSG) **FINAL JUDGMENT**
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. ZTE CORPORATION, et al., Defendants.	Case No. 3:12-cv-03876-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. SAMSUNG ELECTRONICS CO., LTD., et al., Defendants.	Case No. 3:12-cv-03877-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. LG ELECTRONICS, INC., et al., Defendants.	Case No. 3:12-cv-03880-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs v. NINTENDO CO., LTD, et al. Defendants.	Case No. 3:12-cv-03881-VC (PSG)

Based upon this Court's construction of the term "an entire oscillator disposed upon said integrated circuit substrate" as "an [oscillator] located entirely on the same semiconductor substrate as the [central processing unit] that does not require a control signal and whose frequency is not fixed by any external crystal" in U.S. Patent No. 5,809,336 (the "'336 patent") pursuant to the Claim Construction Report and Recommendation, dated September 22, 2015, and this Court's Order Adopting Magistrate Judge's Report and Recommendation, dated November 9, 2015, Plaintiffs Technology Properties Limited LLC, Phoenix Digital Solutions LLC, and Patriot Scientific Corporation (collectively, "Plaintiffs") and Defendants Huawei Technologies Co., Ltd.,

Huawei Device Co., Ltd., Huawei Device USA, Inc., Futurewei Technologies, Inc., Huawei Technologies USA, Inc., ZTE Corporation, ZTE (USA) Inc., Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., LG Electronics, Inc., LG Electronics U.S.A., Inc., Nintendo Co., Ltd., and Nintendo of America, Inc. (collectively, "Defendants") (together, the "Parties") have stipulated that all Defendants are entitled to a judgment of non-infringement as a matter of law as to all of Plaintiffs' asserted claims of the '336 patent in the above-titled and numbered civil cases (collectively, "this Action").

Accordingly, the Court enters Judgment as follows:

Judgment is entered against Plaintiffs and for Defendants as to Plaintiffs' claims for patent infringement with respect to the '336 patent, subject to the parties' right to appeal.

Subject to the parties' right to appeal, the Court further enters judgment for Defendants and against Plaintiffs on Defendants' respective counterclaims seeking declaratory judgment of non-infringement and Defendants' respective affirmative defenses of non-infringement, and declares the '336 patent not infringed by Defendants. Plaintiffs shall take nothing from Defendants with respect to the asserted claims of the '336 patent.

All other claims, counterclaims, defenses, or other matters which have been asserted, including Defendants' counterclaims of patent invalidity, are dismissed without prejudice.

Each party shall bear its own costs and attorneys' fees.

IT IS SO ORDERED

Dated: November __, 2015

VINCE CHHABRIA
United States District Judge

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. HUAWEI TECHNOLOGIES CO., LTD., Et al., Defendants.	Case No. 3:12-cv-03865-VC (PSG) **NOTICE OF APPEAL**
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. ZTE CORPORATION, et al., Defendants.	Case No. 3:12-cv-03876-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. SAMSUNG ELECTRONICS CO., LTD., et al., Defendants.	Case No. 3:12-cv-03877-VC (PSG)
TECHNOLOGY PROPERTIES LIMITED LLC, et al., Plaintiffs, v. LG ELECTRONICS, INC., et al. Defendants.	Case No. 3:12-cv-03880-VC (PSG)

TECHNOLOGY PROPERTIES LIMITED LLC, et al.,

Plaintiffs,

v.

NINTENDO CO., LTD., et al.

Defendants.

Case No. 3:12-cv-03881-VC (PSG)

Notice is hereby given that Plaintiffs Technology Properties Limited LLC, Phoenix Digital Solutions LLC, and Patriot Scientific Corporation (collectively, "Plaintiffs") hereby appeal to the United States Court of Appeals for the Federal Circuit from the Final Judgment of Non-Infringement (Dkt. No. 113)[1] entered in the above-captioned matters on or about November 13, 2015, and all orders that are intertwined with, that are related to, or that resulted in such Judgment including, but not limited to:

- Claim Construction Report and Recommendation (Dkt. No. 104), entered on September 22, 2015; and
- Order Adopting Magistrate Judge's Report and Recommendation (Dkt. No. 111), entered on November 9, 2015.

Included is payment of the $5 filing fee required by 28 U.S.C. § 1917 and the $450 docketing fee required by Federal Circuit Rule 52(a)(3)(A), paid to this Court pursuant to Federal Rule of Appellate Procedure 3(e) and Federal Circuit Rule 52(a)(2).

[1] Unless otherwise indicated, docket numbers refer to documents from *Technology Properties Ltd., et al. v. Samsung Electronics Co., Ltd.*, Case No. 3:12-cv-3877.

Dated: December 7, 2015

Respectfully Submitted,

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CERTIFICATE OF SERVICE

I hereby certify that, on December 7, 2015, I caused the foregoing document to be served on counsel of record via the Court's CM/ECF system.

Dated: December 7, 2015

By: /s/ *Barry J. Bumgardner*
Barry J. Bumgardner

CERTIFICATE OF SERVICE

I hereby certify that on July 5, 2016, an electronic copy of the Corrected Joint Appendix was filed with the Clerk of the Court for the United States Court of Appeals for the Federal Circuit by using the CM/ECF system. The undersigned also certifies that the following participants in this case are registered CM/ECF users and that service of the Corrected Joint Appendix will be accomplished by the CM/ECF system:

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Upon acceptance by the Court of the e-filed document, six paper copies will filed with the Court, via Federal Express, within the time provided in the Court's rules.

/s/ Barry J. Bumgardner
Barry J. Bumgardner