(Counsel listed on signature page)

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

TECHNOLOGY PROPERTIES LIMITED LLC, et al.,

Plaintiffs,

v.

LG ELECTRONICS, INC. and LG ELECTRONICS U.S.A., INC.,

Defendants.

Case No. 3:12-cv-03880-VC

PLAINTIFFS' SECOND AMENDED INFRINGEMENT CONTENTIONS

I. INTRODUCTION

Plaintiffs' second amended infringement contentions ("Supplemental Contentions") are a supplement to the ones supplied to LG Electronics, Inc. and LG Electronics U.S.A., Inc., (collectively, "Defendants") on July 27, 2015 ("First Amended Contentions") and are being served pursuant to Defendants' requests for these contentions and the Court's recent order (see Dkt. 142). These contentions set forth Plaintiffs' positions regarding the construction of the term "entire oscillator" as established in the Federal Circuit's recent opinion (see Federal Circuit Case No. 16-1306, Doc. 99-2 ("the Fed. Cir. Opinion").

In that Opinion, the Federal Circuit found that the proper construction for the claim term "entire oscillator disposed upon said integrated circuit substrate" is "an oscillator located entirely on the same semiconductor substrate as the central processing unit that [a] does not require a command input to change the clock frequency and [b] whose frequency is not fixed by any external crystal." Fed. Cir. Opinion at 16.

Plaintiffs challenge Defendants' bald assertion that Plaintiffs' First Amended Contentions "cannot be correct under the [District] Court's original [but now amended] construction [of the term "entire oscillator"] given the stipulated judgment of non-infringement." *See* Case No. 3:12-

cv-03877-VC, Dkt. 123 at 4, (Defendants' Case Management Statement). Plaintiffs' First Amended Contentions, served before the District Court's construction, are not incorrect. At worst, they are not up-to-date as they do not address the disclaimers found by the District Court or the Federal Circuit, since neither of those courts had ruled on the construction of the "entire oscillator" term when the First Amended Contentions were served. In the First Amended Contentions, Plaintiffs correctly identified the ring oscillators in Defendants' accused products as corresponding to the "entire oscillator" claim element. Plaintiffs stand by this portion of the First Amended Contentions as well as the rest of the First Amended Contentions. Nevertheless, Plaintiffs' contentions were based on Judge Grewal's previous construction of "entire oscillator" from a prior case and did not address the negative limitations later placed on the "entire oscillator" element (*i.e.*, the Federal Circuit's disclaimers). These Supplemental Contentions, therefore, add to the First Amended Contentions and are consistent with the theories of infringement presented therein.

Accordingly, these Supplemental Contentions will address the two disclaimers found by the Federal Circuit that are directed to claim elements 6.c and 13.b in the First Amended Contentions. The construction that requires "an oscillator located entirely on the same semiconductor substrate as the central processing unit" is addressed in the First Amended Contentions. The First Amended Contentions set forth Plaintiffs' theories of infringement against accused products that are identified in Column A of Exhibit A (the "Accused Products"). These Supplemental Contentions are directed to the same Accused Products as the First Amended Contentions.

For reference and to avoid any misunderstandings arising from the inconsistent use of terminology in describing a PLL clocking system, a PLL system that is representative of the PLL systems found in each of the Accused Products is attached hereto as Exhibit B (referred to in its entirety as the "Representative Clocking System"), with certain features labeled. For the avoidance of doubt, Plaintiffs contend that each component and signal shown in the Representative Clocking System is present in each of the Accused Products. These labels will be used below in describing the Plaintiffs' positions. Specific implementations of PLLs used in

various Accused Products are found in the Qualcomm, NVidia, IBM, and Texas Instruments document productions. *See, e.g.*, QTPL2PDS0063576, QTPL2PDS005450, QTPL2PDS0054987, QTPL2PDS0017582, QTPL2PDS007614, TI-0165418, and PDSND128219-22. Further, Plaintiffs' expert, Dr. Vojin Oklobdzija, explained the general operation of a particular PLL within a related product at trial. *See generally HTC Corp. v. Tech. Props. Ltd.*, Case No: C-08-00882-PSG, Trial Tr. vol. 3, 552:5-565:25, Sept. 25, 2013.

Ring Oscillator frequencies depend entirely on PVT (processing, voltage, and temperature). The Ring Oscillator corresponds to the "entire oscillator" in claim elements 6.c and 13.b because it is the part of the circuit that oscillates naturally in response to PVT. The specifics of this oscillator are not believed to be necessary to these contentions, as the claims simply require an "entire oscillator."

The voltage of the Ring Oscillator, which is illustrated in Ex. B, in the Accused Products may be controlled either by a current control or voltage control. The PLL Control Signal, as illustrated in Ex. B, is an analog signal from the PLL Control Circuit to the Ring Oscillator. If the Ring Oscillator is a current controlled ring oscillator, the PLL Control Signal may adjust the current supplied to the Ring Oscillator. If the Ring Oscillator is a voltage controlled ring oscillator, the PLL Control Signal may adjust the voltage supplied to the Ring Oscillator. Again, this difference is not believed to be important to these Supplemental Contentions. As such, the PLL Control Signal of the Accused Products may control the current or voltage source to the Ring Oscillator.

As shown in Ex. B, the Programmable Divisor is a storage element that contains a value that is used to divide down the frequency of the signal on the Feedback Loop input to the Divisor. This behavior is well known in the art. *See, e.g.*, Fractional/Integer-N PLL Basics, Technical Brief SWRA029, Texas Instruments, 2010 (attached hereto as Exhibit C). For example, the Programmable Divisor may contain the value 8. In the instance that the frequency of the signal on the Feedback Loop was 800 MHz, the frequency of the signal on the Feedback Loop when it exited the Programmable Divisor would be 100 MHz.

The other elements in shown in Ex. B are also well known in the art and are not further explained here.

II. AN OSCILLATOR . . . THAT DOES NOT REQUIRE A COMMAND INPUT TO CHANGE THE CLOCK FREQUENCY

Plaintiffs' position regarding disclaimer (a) is that using a command input to change the frequency of the Ring Oscillator found in the Accused Products is allowable, but it cannot be the sole means by which the frequency of the oscillator's oscillations are changed. In other words, the claim language having this disclaimer is met as long as something other than a command input can change the frequency of the Ring Oscillator. Moreover, since a ring oscillator is by nature inherently variable in response to process, voltage and temperature ("PVT") changes, no command input is ever *required* to change the clock frequency. *See also HTC Corp. v. Tech. Props. Ltd.*, Case No: C-08-00882-PSG, Trial Tr. vol. 3, 627:25-629:11, Sept. 25, 2013 (testimony of Dr. Oklobdzija regarding the "well-known fact" that chips vary due to process, voltage, and temperature).

The Federal Circuit explained that each of the statements made during prosecution were made in such a way to explain that the architecture of the chip "eliminates the need for a command input to change clock frequency" but that "none of [the prosecution history] statements disclaim an entire oscillator receiving a command input for any purpose." *See* Fed. Cir. Opinion at 16. The opinion highlights that the Patentee argued that Sheets' clock system was "unrelated" to the claimed invention, that "'no command input was necessary to change the clock frequency,'" and that the claims did not "rely upon the provision of frequency control information to an external clock." *Id.* (underlining added). The Federal Circuit intentionally used the word *require* rather than *utilize*, *use*, or *include*, which makes clear that the Federal Circuit held that while the entire oscillator may also have a command input which changes the frequency, it may not be the sole means of doing so.

As discussed in the subsections below, the clock frequency of the Ring Oscillators in the processors of the Accused Products can be changed by mechanisms other than by "command inputs." *See* Ex. A, where the processors are listed in Column B and referred to herein as

"Accused Products' Processors." As an example and assuming *arguendo* that the writing of a value to the Programmable Divisor on the Feedback Loop of the PLL System is a "command input," the frequency of oscillation of the Ring Oscillators in the Accused Products' Processors contained in the Accused Products of Ex. A can change by means other than "command inputs" reprogramming the Programmable Divisor.

A. The PLL Control Circuit Manages the Frequency Range of the Oscillators in the Accused Products

Plaintiffs contend that the PLL Control Circuit, shown in Ex. B and found in the Accused Products' Processors, makes adjustments to the PLL Control Signal to adjust the frequency at which the Ring Oscillator oscillates even when the Programmable Divisor is at a constant value and the PLL circuit as a whole is "locked." By definition, a Ring Oscillator requires only a supply voltage to oscillate, and thus adjustments are made by regulating voltage. These adjustments are used to keep the frequency of the Ring Oscillator within a predetermined range as conditions surrounding the Ring Oscillator change (e.g., electrical and temperature conditions). Neither voltage supply variations to the Ring Oscillator nor environmental or temperature changes of the Oscillator is a "command input" used to change the clock frequency, yet these factors affect the frequency at which the Oscillator oscillates.

In the case where the frequency of the Ring Oscillator decreases when the temperature of the Ring Oscillator increases, as the temperature increases, the PLL Control Circuit will, at some point, determine that the frequency of the signal on the Feedback Loop has drifted outside the predetermined range of the PLL. In a hypothetical example, at Point in Time A, the temperature of the Ring Oscillator is at 23 °C (room temperature), the Oscillator is oscillating at 200 MHz, the frequency of the Reference Signal is 50 MHz, and the voltage of the Control Signal is at 0.5V. Later, at Point in Time B, the temperature of the Ring Oscillator has risen to 24 °C which causes the Oscillator to oscillate at 199.5 MHz (with all other values being the same as at Point in Time A). In this situation, the PLL Control Circuit will increase the voltage of the Control Signal to 0.6 V, which will then cause the Oscillator to again start oscillating at 200 MHz (the desired value).

In actuality, the adjustments described in the preceding paragraph occur nearly in real time and may be much smaller in magnitude than described above. In other words, there are many, many small sporadic adjustments to the Control Signal. But, the cumulative adjustments made to the frequency of the Ring Oscillator through the PLL Control Signal may be in the tens or hundreds of megahertz as the temperature of the Ring Oscillator changes. PLLs experience both long-term (hours, days, months) and short-term (seconds or less) instability.

Exhibit D is a document titled "Thermal Analysis of CMOS Voltage-Controlled Oscillators" by Maciej Frankiewicz and Andrzej Kos (the "Kos Article"). Figure 6 of the Kos Article shows how the frequency of the ring oscillator described in the article varies as a function of temperature, with the control voltage being held steady. Looking at the top curve, the particular ring oscillator being discussed operates at approximately 1.35 MHz at 10 °C and operates at approximately 1.29 MHz at 90 °C. If one wished to hold the frequency of this oscillator relatively constant through the use of a PLL Control Circuit, such a Circuit would have to provide a cumulative upward adjustment to the ring oscillator described in the Kos Article of 60 MHz (1.35-1.29 MHz) as the circuit's temperature increased from 10 to 90 °C. Such adjustments would, most likely, be in the form of increasing the tuning voltage of the ring oscillator. *See also* Exhibit E, which is a document titled "Low Power, Temperature and Process Compensated CMOS Ring Oscillator" by Mihai Eugen Marin and Razvan Cristian Marin at 1 (stating "Without any compensation scheme the central frequency drift of the CMOS [ring] oscillator can be up to 100% when the temperature is varied.").

Further, the only way the PLL Control Circuit would know to make such adjustments would be due to the fact that it has sensed that the frequency of the Ring Oscillator has moved outside the predetermined range of the PLL. In other words, the PLL Control Circuit first detects that the frequency of the Ring Oscillator has moved outside the predetermined range, and then adjusts it (higher or lower as required) back into the predetermined range.

Plaintiffs contend that the Ring Oscillators in the Accused Products' Processors previously identified in the First Amended Infringement Contentions function in a similar manner. The frequency of the Ring Oscillators in the Accused Products' Processors vary as a

result of electrical and environmental variations, but for sporadic adjustments to the frequency of the oscillator by a control signal - which signal has been stimulated by the changing frequency of the Ring Oscillator. Thus, the PLL Control Circuit can and does sporadically adjust the frequency of the Ring Oscillator in the Accused Products Processors in the absence of anything that could be considered a "command input."

B. Variation of the Ring Oscillator Prior to Phase Lock

During power up and state changes of the PLL (e.g., when the Programmable Divisor is altered), the frequency range in which the Ring Oscillators oscillate is not "phase locked" to the Reference Signal. Ring Oscillators, like most physical devices, cannot move from one state to another instantly. In the specific case of Ring Oscillators, they cannot change instantly from oscillating at 0 Hz (at power-up) to 400 MHz instantaneously. Likewise, they cannot change from 400 MHz to 1000 MHz in an instant. Instead, it takes a finite amount of time for the Ring Oscillators to reach the desired frequency and to settle at that frequency. During this period of time, the frequency at which the Ring Oscillators are oscillating will not be related to the Reference Signal by the PLL Control Circuit. Plaintiffs contend these variations in frequency of the Ring Oscillators are not in response to a "command input."

C. Variation of the Oscillator during Phase Lock

Plaintiffs contend that the frequency at which the Ring Oscillators in the Accused Products' Processor oscillate varies due to the inherent nature of the Ring Oscillators to change frequency as a result of temperature and voltage and process variations, even when the Ring Oscillators are phase locked by the PLL Control Circuit. As discussed in the '336 Patent, ring oscillators, in general, tend to vary as a result of process, voltage, and temperature variations. The function of the PLL Control Circuit in the Accused Products' Processors is to manage the inherent and unavoidable frequency variations of the Ring Oscillators from varying as much as they would in the absence of the PLL Control Signal. But, keeping this range overly small can make a PLL System more expensive and consume more power. The optimal range is one that allows for some natural variations of the frequency of the Ring Oscillator, yet is not so great as to introduce errors into the CPU which is being clocked by the Ring Oscillator. The range of

variation over which the Ring Oscillators in the Accused Products' Processor oscillate is evidence that the frequency of oscillation of the Ring Oscillator varies in the absence of a "command input."

Furthermore, the management of the Ring Oscillators' frequency occurs no more than once every cycle of the Reference Signal. In an exemplary case, where the frequency of the Reference is 20 MHz and the frequency of the Ring Oscillator is 1.28 GHz (64 times that of the Reference Signal), adjustments (if any) to the frequency of the Ring Oscillator will occur no more often than once every 64 cycles of the Ring Oscillator (i.e., once for every cycle of the Reference Signal). For the intervening cycles, the Ring Oscillator will be free running and will not be controlled by the PLL Control Circuit. During these intervening cycles, the frequency of the Ring Oscillator can change and is additional evidence that the frequency of the Ring Oscillator does not require a "command input" to change frequency.

D. Thermal Throttling of the Accused Products' Processors

Plaintiffs contend that modern phones and tablets implement a technique called "thermal throttling" which reduces the operating frequency of the phone/tablet's processor if the temperature of the processor becomes too high. *See* "Just Enough is More: Achieving Sustainable Performance in Mobile Devices under Thermal Limitations" by Onur Sahin, Paul Thomas Varghese, Ayse K. Coskun at 1 (attached hereto as Exhibit F, the "Coskun Article") (stating "modern mobile systems adopt CPU throttling techniques that adaptively reduce the operating frequency of the mobile processor to mitigate thermal emergencies."). Reducing the operating frequency of the mobile processor means that the frequency at which the ring oscillator in the mobile system oscillates is lowered to reduce the heat generated by the processor (the higher a frequency a processor operates, the more energy it consumes and the higher the temperature of the processor (all other things being constant)).

The Coskun Article illustrates in Fig. 1 how the frequency at which a Qualcomm MDP8974 processor operates decreases over time as the processor is forced to operate a lower frequencies to meet thermal constraints. Coskun Article, Fig. 1 at 2. Plaintiffs believe that the behavior of the MDP8974 processor is representative of all of the Accused Products' Processors,

to the extent that they can sense temperature and reduce the operating frequency of the processor if the temperature becomes too high. As shown in Fig. 1, the operating frequencies of the MDP8974 vary from 2.1 GHz to 1.2 GHz.

Plaintiffs contend that, to the extent that this thermal throttling is accomplished by some means other than altering the value of the Programmable Divisor in the PLL System of a particular Accused Product, that this throttling demonstrates how the frequency at which the oscillator in an Accused Product can be changed other than through the use of a command input.

Information about how the Accused Products' Processors implement thermal throttling is within the possession of the manufacturers of such Processors, namely Qualcomm, IBM, Texas Instruments, NVidia, and Samsung. Plaintiffs are awaiting this information through discovery requests served prior to this lawsuit being appealed to the Federal Circuit.

III. AN OSCILLATOR . . . WHOSE FREQUENCY IS NOT FIXED BY ANY EXTERNAL CRYSTAL

Plaintiffs contend that the frequency at which the Ring Oscillators in the Accused Product's Processors oscillate is *never* fixed (by anything), but rather is by nature inherently variable.

These Ring Oscillators oscillate at various frequency ranges to serve a variety of use cases. One use case is that the Ring Oscillators oscillate at low frequencies when the Accused Products are not in use (*e.g.*, standby mode, low-power mode, etc.), which lowers the power consumed by the Accused Products' Processors. In turn, this will lower the power consumption in general, including the power drawn from the batteries of the Accused Products. Additional side effects of drawing lower power will be that the Products will operate at lower temperatures which may lengthen the life of the Processors and other components in the Accused Products.

A separate use case is when the Accused Products are required to perform some computationally intensive tasks and/or have a number of tasks to perform at one time. In such cases, the Ring Oscillators oscillate at higher frequency ranges to provide an enhanced user experience (*i.e.*, the Accused Products will "feel" responsive and fast).

Evidence that the Ring Oscillators in the Accused Products' Processors operate at a variety of frequencies, spanning from approximately 400 MHz to over 1500 MHz (in some cases), is found in the documents/pages listed in Column C of Ex. A.

Plaintiffs' interpretation of the term "fixed", as used in the disclaimer found by the Federal Circuit, is "not fluctuating or varying", "definite", or "predetermined and not subject to or able to be changed" (*e.g.*, a fixed interest rate or a fixed period of time). *See* Exhibit G for a list of dictionary definitions of the term "fixed."

Given that the Ring Oscillators in the Accused Products' Processors are variable in frequency and not fixed, Plaintiffs contend that the frequencies of the oscillators are not fixed by any component or device, including an external crystal. Plaintiffs agree that the frequency range of a Ring Oscillator is determined, in part, by the frequency of an external crystal. But, the crystal reference is merely sampled as a basis for comparison, and does not propagate past the PLL Control Circuit. But, by altering the value in the Programmable Divisor, the frequency range of the Ring Oscillator in the Accused Products' Processors is varied during the normal use of the Accused Products.

Furthermore, since the Ring Oscillators in the Accused Products' Processors are by nature, inherently variable in response to PVT and are never fixed, Plaintiffs contend that the frequencies of the Oscillators are not fixed by any component or device, including an external crystal. By definition, a Ring Oscillator requires only a supply voltage to oscillate, and thus adjustments are made by regulating voltage. The external crystal is not a voltage supply.

Finally, the variations of frequency described above in Section II further demonstrate that the ring oscillators in the Accused Products' Processors are not "fixed" by an external crystal.

Dated: June 16, 2017

Respectfully submitted,

/s/ Barry J. Bumgardner

NELSON BUMGARDNER, P.C.
Edward R. Nelson, III (*Pro Hac Vice*)
ed@nelbum.com
Brent Nelson Bumgardner (*Pro Hac Vice*)
brent@nelbum.com
Barry J. Bumgardner (*Pro Hac Vice*)

barry@nelbum.com
Thomas Christopher Cecil (*Pro Hac Vice*)
tom@nelbum.com
John Murphy (*Pro Hac Vice*)
murphy@nelbum.com
3131 West 7th Street, Suite 300
Fort Worth, Texas 76107
[Tel.] (817) 377-9111
[Fax] (817) 377-3485

Attorneys for Plaintiff
PHOENIX DIGITAL SOLUTIONS, LLC

/s/ William L. Bretschneider (with permission)
SILICON VALLEY LAW GROUP
William L. Bretschneider (SBN 144561)
wlb@svlg.com
50 W. San Fernando Street, Suite 750
San Jose, California 95113
[Tel.] (408) 573-5700
[Fax] (408) 573-5701

Attorneys for Plaintiff
TECHNOLOGY PROPERTIES LIMITED, LLC

CERTIFICATE OF SERVICE

I hereby certify that on June 16, 2017, I caused the foregoing document to be served on counsel of record via the Court's CM/ECF system.

Dated: June 16, 2017

By: */s/ Barry J. Bumgardner*
Barry J. Bumgardner

Exhibit "A"

EXHIBIT A

Column A **Accused Products**	**Column B** **Accused Products' Processors**	**Column C** **Citations**
LG D820 Nexus 5 NA TD-LTE 16GB	32bit Qualcomm Snapdragon 800 MSM8974AA v2	QTPL2PDS001336, QTPL2PDS0080648, QTPL2PDS0080682, QTPL2PDS0080690, QTPL2PDS0080976, QTPL2PDS0014827, QTPL2PDS0015274-275, QTPL2PDS001352, QTPL2PDS001352
LG Incite CT810	32bit Qualcomm MSM7201A	QTPL2PDS0042530, QTPL2PDS0042565
LG P930 Nitro HD	32bit Qualcomm Snapdragon S3 APQ8060	QTPL2PDS0005912, QTPL2PDS000596, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798
LG D725 G3 Vigor / G3 S LTE-A (LG B2 Mini)	32bit Qualcomm Snapdragon 400 MSM8926	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0078918
LG P509 Optimus T / P504	32bit Qualcomm MSM7227	QTPL2PDS004389, QTPL2PDS0084161, QTPL2PDS0084333, QTPL2PDS0085583, QTPL2PDS0085658, QTPL2PDS0085661-62, QTPL2PDS0015662, QTPL2PDS0015666
LG G2 D801 4G LTE	32bit Qualcomm Snapdragon 800 MSM8974AA v2	QTPL2PDS001336, QTPL2PDS0080648, QTPL2PDS0080682, QTPL2PDS0080690, QTPL2PDS0080976, QTPL2PDS0014827, QTPL2PDS0015274-275, QTPL2PDS001352, QTPL2PDS001352
LG US740 Apex	32bit Qualcomm MSM7627	QTPL2PDS0084161, QTPL2PDS0084161, QTPL2PDS0084333, QTPL2PDS0085583, QTPL2PDS0085658, QTPL2PDS0085661-62

LG AS680 Optimus 2	32bit Qualcomm MSM7627T	QTPL2PDS0084161, QTPL2PDS0084333, QTPL2PDS0085583, QTPL2PDS0085658, QTPL2PDS0085661-62, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798
LG US730 Splendor	32bit Qualcomm Snapdragon S2 MSM8655	QTPL2PDS0060696-97, QTPL2PDS0060574, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798
LG G3 VS985 LTE-A (LG B2)	32bit Qualcomm Snapdragon 801 MSM8974AC v3	QTPL2PDS001336, QTPL2PDS0080648, QTPL2PDS0080682, QTPL2PDS0080690, QTPL2PDS0080976, QTPL2PDS0014827, QTPL2PDS0015274-275, QTPL2PDS001352, QTPL2PDS001352
LG VS930 Spectrum 2 / Optimus LTE 2	32bit Qualcomm Snapdragon S4 MSM8960	QTPL2PDS0019673, QTPL2PDS0004585, QTPL2PDS0004706, QTPL2PDS0004735,QTPL2PDS0004384
LG D415 Optimus L90 / L Series III L90 (LG W7)	32bit Qualcomm Snapdragon 400 MSM8226	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415,QTPL2PDS0078918
LG MS910 Esteem 4G (LG Bryce)	32bit Qualcomm Snapdragon S2 MSM8655	QTPL2PDS0060696-97, QTPL2PDS0060574, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798

LG AS695 Optimus Plus	32bit Qualcomm MSM7627A	QTPL2PDS0084161, QTPL2PDS0084333, QTPL2PDS0085583, QTPL2PDS0085658, QTPL2PDS0085661-62, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798
LG E980 Optimus G Pro 5.5 4G LTE	32bit Qualcomm Snapdragon 600 APQ8064T	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0076265
LG G3 LS990 TD-LTE (LG B2)	32bit Qualcomm Snapdragon 801 MSM8974AC v3	QTPL2PDS001336, QTPL2PDS0080648, QTPL2PDS0080682, QTPL2PDS0080690, QTPL2PDS0080976, QTPL2PDS0014827, QTPL2PDS0015274-275, QTPL2PDS001352, QTPL2PDS001352
LG LS720 Optimus F3 4G LTE	32bit Qualcomm Snapdragon S4 MSM8960 Lite	QTPL2PDS0019673, QTPL2PDS0004585, QTPL2PDS0004706, QTPL2PDS0004735, QTPL2PDS0004378, QTPL2PDS0004384
LG D631 G Vista / G Pro 2 Lite LTE-A (LG B1 Lite)	32bit Qualcomm Snapdragon 400 MSM8926	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0078918
LG L55C Optimus Q (LG Gelato Q)	32bit Qualcomm MSM7627T	QTPL2PDS0084161, QTPL2PDS0084333, QTPL2PDS0085583, QTPL2PDS0085658, QTPL2PDS0085661-62, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798
LG VS415PP Optimus Zone 2 / L Series III L40 CDMA	32bit Qualcomm Snapdragon 200 MSM8210/MSM8610	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415
LG US670 Optimus U	32bit Qualcomm MSM7627	QTPL2PDS0084161, QTPL2PDS0084161, QTPL2PDS0084333, QTPL2PDS0085583, QTPL2PDS0085658, QTPL2PDS0085661-62

LG UK410 G Pad 7.0 LTE (LG E7)	32bit Qualcomm Snapdragon 400 MSM8926	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0078918
LG V400 G Pad 7.0 (LG E7)	32bit Qualcomm Snapdragon 400 MSM8226/APQ8026	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415,QTPL2PDS0078918
LG V500 G Pad 8.3 WiFi	32bit Qualcomm Snapdragon 600 APQ8064T	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0076265
LG LW770 Optimus Regard	32bit Qualcomm Snapdragon S4 MSM8960 Lite	QTPL2PDS0019673, QTPL2PDS0004585, QTPL2PDS0004706, QTPL2PDS0004735, QTPL2PDS0004378, QTPL2PDS0004384
LG E970 Optimus G 4G LTE (LG Gee)	32bit Qualcomm Snapdragon S4 Pro APQ8064	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0076265
LG LW690 Optimus C	32bit Qualcomm MSM7627	QTPL2PDS0084161, QTPL2PDS0084161, QTPL2PDS0084333, QTPL2PDS0085583, QTPL2PDS0085658, QTPL2PDS0085661-62
LG C729 DoublePlay	32bit Qualcomm Snapdragon S2 MSM8255	QTPL2PDS0060696-97, QTPL2PDS0060574, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798
LG P870 Escape 4G	32bit Qualcomm Snapdragon S3 APQ8060	QTPL2PDS0005912, QTPL2PDS000596, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798

LG VS920 Spectrum 4G	32bit Qualcomm Snapdragon S3 MSM8660	QTPL2PDS0010976-77, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798
LG LS740 Volt 4G TD-LTE / F90	32bit Qualcomm Snapdragon 400 MSM8926	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0078918
LG VS840PP Optimus Exceed	32bit Qualcomm Snapdragon S3 MSM8660	QTPL2PDS0010976-77, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798
LG VK700 G Pad 10.1 4G LTE	32bit Qualcomm Snapdragon 400 MSM8926	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0078918
LG C900 Optimus 7Q (LG Pacific)	32bit Qualcomm Snapdragon S1 QSD8250	QTPL2PDS0109783, QTPL2PDS01 09788-91, QTPL2PDS0109801, QTPL2PDS0015662, QTPL2PDS0015666
LG LG730 Venice	32bit Qualcomm Snapdragon S2 MSM8655	QTPL2PDS0060696-97, QTPL2PDS0060574, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798
LG VS870 Lucid 2	32bit Qualcomm Snapdragon S4 MSM8960 Lite	QTPL2PDS0019673, QTPL2PDS0004585, QTPL2PDS0004706, QTPL2PDS0004735, QTPL2PDS0004378, QTPL2PDS0004384

LG L45C Optimus Net	32bit Qualcomm MSM7627T	QTPL2PDS0084161, QTPL2PDS0084333, QTPL2PDS0085583, QTPL2PDS0085658, QTPL2PDS0085661-62, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798
LG E960 Nexus 4 (LG Mako)	32bit Qualcomm Snapdragon S4 Pro APQ8064	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0076265
LG G Flex 2	Qualcomm Snapdragon 810	PDSND165482
LG Optimus F7 US780	32bit Qualcomm Snapdragon S4 MSM8960	QTPL2PDS0019673, QTPL2PDS0004585, QTPL2PDS0004706, QTPL2PDS0004735,QTPL2PDS0004384
LG MS323 L Series III L70 (LG W5)	32bit Qualcomm Snapdragon 200 MSM8210	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415
LG MS659 Optimus F3 4G LTE	32bit Qualcomm Snapdragon 400 MSM8930	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0097028-30, QTPL2PDS0097587
LG VM720 Optimus F3 4G LTE	32bit Qualcomm Snapdragon S4 MSM8960 Lite	QTPL2PDS0019673, QTPL2PDS0004585, QTPL2PDS0004706, QTPL2PDS0004735, QTPL2PDS0004378, QTPL2PDS0004384
LG Optimus F7 LG870	32bit Qualcomm Snapdragon S4 MSM8960	QTPL2PDS0019673, QTPL2PDS0004585, QTPL2PDS0004706, QTPL2PDS0004735,QTPL2PDS0004384
LG P925 Thrill 4G	32bit Texas Instruments OMAP 4430	See generally PDSND136955-137050, and particularly PDSND136959-136968
LG VK810 G Pad 8.3 4G LTE	32bit Qualcomm Snapdragon 600 APQ8064T	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0076265
LG LS995 G Flex TD-LTE	32bit Qualcomm Snapdragon 800 MSM8974AA v2	QTPL2PDS001336, QTPL2PDS0080648, QTPL2PDS0080682, QTPL2PDS0080690, QTPL2PDS0080976, QTPL2PDS0014827, QTPL2PDS0015274-275, QTPL2PDS001352, QTPL2PDS001352

LG D520 Optimus F3Q 4G LTE (LG FX3)	32bit Qualcomm Snapdragon 400 MSM8930	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0097028-30, QTPL2PDS0097587
LG G3 D851 LTE-A (LG B2)	32bit Qualcomm Snapdragon 801 MSM8974AC v3	QTPL2PDS001336, QTPL2PDS0080648, QTPL2PDS0080682, QTPL2PDS0080690, QTPL2PDS0080976, QTPL2PDS0014827, QTPL2PDS0015274-275, QTPL2PDS001352, QTPL2PDS001352
LG VN270 Cosmos Touch	Qualcomm QSC6055	QTPL2PDS0015662, QTPL2PDS0015666
LG MS840 Connect 4G (LG Cayman)	32bit Qualcomm Snapdragon S3 MSM8660	QTPL2PDS0010976-77, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798
LG MS870 Spirit 4G	32bit Qualcomm Snapdragon S4 MSM8960 Lite	QTPL2PDS0019673, QTPL2PDS0004585, QTPL2PDS0004706, QTPL2PDS0004735, QTPL2PDS0004378, QTPL2PDS0004384
LG LS860 Mach 4G LTE (LG Cayenne)	32bit Qualcomm Snapdragon S4 MSM8960 Lite	QTPL2PDS0019673, QTPL2PDS0004585, QTPL2PDS0004706, QTPL2PDS0004735, QTPL2PDS0004378, QTPL2PDS0004384
LG VS980 G2 4G LTE	32bit Qualcomm Snapdragon 800 MSM8974AA v2	QTPL2PDS001336, QTPL2PDS0080648, QTPL2PDS0080682, QTPL2PDS0080690, QTPL2PDS0080976, QTPL2PDS0014827, QTPL2PDS0015274-275, QTPL2PDS001352, QTPL2PDS001352
LG E960 Nexus 4 16GB (LG Mako)	32bit Qualcomm Snapdragon S4 Pro APQ8064	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0076265
LG D959 G Flex	32bit Qualcomm Snapdragon 800 MSM8974AA v2	QTPL2PDS001336, QTPL2PDS0080648, QTPL2PDS0080682, QTPL2PDS0080690, QTPL2PDS0080976, QTPL2PDS0014827, QTPL2PDS0015274-275, QTPL2PDS001352, QTPL2PDS001352
LG Ally VS740	32bit Qualcomm MSM7627	
LG G3 D850 LTE-A (LG B2)	32bit Qualcomm Snapdragon 801 MSM8974AC v3	QTPL2PDS001336, QTPL2PDS0080648, QTPL2PDS0080682, QTPL2PDS0080690, QTPL2PDS0080976, QTPL2PDS0014827, QTPL2PDS0015274-275, QTPL2PDS001352, QTPL2PDS001352

LG V909 Optimus Pad / G-Slate	32bit NVIDIA Tegra 2 250 T20	PDSND128215
LG Fathom VS750	32bit Qualcomm Snapdragon S1 QSD8650	QTPL2PDS0109783, QTPL2PDS01 09788-91, QTPL2PDS0109801, QTPL2PDS0015662, QTPL2PDS0015666
LG MS690 Optimus M	32bit Qualcomm MSM7627	QTPL2PDS0084161, QTPL2PDS0084161, QTPL2PDS0084333, QTPL2PDS0085583, QTPL2PDS0085658, QTPL2PDS0085661-62
LG LS970 Optimus G / Eclipse 4G (LG Gee)	32bit Qualcomm Snapdragon S4 Pro APQ8064	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0076265
LG D500 Optimus F6	32bit Qualcomm Snapdragon 400 MSM8930	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0097028-30, QTPL2PDS0097587
LG LS696 / VM696 Optimus Elite	32bit Qualcomm MSM8655	QTPL2PDS0060696-97, QTPL2PDS0060574, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798
LG VS810PP L Fino LTE	32bit Qualcomm Snapdragon 200 MSM8212	QTPL2PDS0092329, QTPL2PDS0092422, QTPL2PDS0092467, QTPL2PDS0092474, QTPL2PDS0092628, QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415
LG P769 Optimus L9	32bit Texas Instruments OMAP 4430	See generally PDSND136955-137050, and particularly PDSND136959-136968
LG G4	Qualcomm Snapdragon 808	PDSND165482
LG VS880 G Vista / G Pro 2 Lite LTE-A (LG B1 Lite)	32bit Qualcomm Snapdragon 400 MSM8926	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0078918

LG V700 G Pad 10.1 WiFi	32bit Qualcomm Snapdragon 400 APQ8026	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415
LG V410 G Pad 7.0 LTE (LG E7)	32bit Qualcomm Snapdragon 400 MSM8926	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0078918
LG LS980 G2 TD-LTE	32bit Qualcomm Snapdragon 800 MSM8974AA v2	QTPL2PDS001336, QTPL2PDS0080648, QTPL2PDS0080682, QTPL2PDS0080690, QTPL2PDS0080976, QTPL2PDS0014827, QTPL2PDS0015274-275, QTPL2PDS001352, QTPL2PDS001352
LG G2 D800 4G LTE	32bit Qualcomm Snapdragon 800 MSM8974AA v2	QTPL2PDS001336, QTPL2PDS0080648, QTPL2PDS0080682, QTPL2PDS0080690, QTPL2PDS0080976, QTPL2PDS0014827, QTPL2PDS0015274-275, QTPL2PDS001352, QTPL2PDS001352
LG VM701 Optimus Slider (LG Gelato Q)	32bit Qualcomm MSM7627T	QTPL2PDS0084161, QTPL2PDS0084333, QTPL2PDS0085583, QTPL2PDS0085658, QTPL2PDS0085661-62, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798
LG LS840 Viper 4G LTE	32bit Qualcomm Snapdragon S3 MSM8660	QTPL2PDS0010976-77, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798
LG MS695 Optimus M+	32bit Qualcomm MSM7627A	QTPL2PDS0084161, QTPL2PDS0084333, QTPL2PDS0085583, QTPL2PDS0085658, QTPL2PDS0085661-62, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798

LG VS660 Vortex	32bit Qualcomm MSM7627	QTPL2PDS0084161, QTPL2PDS0084161, QTPL2PDS0084333, QTPL2PDS0085583, QTPL2PDS0085658, QTPL2PDS0085661-62
LG MS395 F60 4G LTE	64bit Qualcomm Snapdragon 410 MSM8916	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0092826, QTPL2PDS0092947,
LG LS670 Optimus S	32bit Qualcomm MSM7627	QTPL2PDS0084161, QTPL2PDS0084161, QTPL2PDS0084333, QTPL2PDS0085583, QTPL2PDS0085658, QTPL2PDS0085661-62
LG LS855 Marquee	32bit Texas Instruments OMAP 3630	See generally PDSND133115-177, and particularly PDSND133125-132
LG VS700 Enlighten (LG Gelato Q)	32bit Qualcomm MSM7627T	QTPL2PDS0084161, QTPL2PDS0084333, QTPL2PDS0085583, QTPL2PDS0085658, QTPL2PDS0085661-62, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798
LG LS885 G3 Vigor TD-LTE (LG B2 Mini)	32bit Qualcomm Snapdragon 400 MSM8926	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0078918
LG VS950 Intuition / Optimus Vu	32bit Qualcomm Snapdragon S4 MSM8960	QTPL2PDS0019673, QTPL2PDS0004585, QTPL2PDS0004706, QTPL2PDS0004735,QTPL2PDS0004384
LG V510 G Pad 8.3 WiFi Google Play Edition	32bit Qualcomm Snapdragon 600 APQ8064T	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0076265
LG VS890 Enact (LG FX3)	32bit Qualcomm Snapdragon 400 MSM8930	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0097028-30, QTPL2PDS0097587

LG VS876 Lucid 3 / F90 LTE	32bit Qualcomm Snapdragon 400 MSM8926	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0078918
LG G3 US990 LTE-A / AS990 (LG B2)	32bit Qualcomm Snapdragon 801 MSM8974AC v3	QTPL2PDS001336, QTPL2PDS0080648, QTPL2PDS0080682, QTPL2PDS0080690, QTPL2PDS0080976, QTPL2PDS0014827, QTPL2PDS0015274-275, QTPL2PDS001352, QTPL2PDS001352
LG UN270 Attune	Qualcomm QSC6055	QTPL2PDS0015662, QTPL2PDS0015666
LG VS910 Revolution 4G	32bit Qualcomm Snapdragon S2 MSM8655	QTPL2PDS0060696-97, QTPL2PDS0060574, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798
LG MS770 Motion 4G	32bit Qualcomm Snapdragon S4 MSM8960 Lite	QTPL2PDS0019673, QTPL2PDS0004585, QTPL2PDS0004706, QTPL2PDS0004735, QTPL2PDS0004378, QTPL2PDS0004384
LG AS740 Axis	32bit Qualcomm MSM7627	QTPL2PDS0084161, QTPL2PDS0084161, QTPL2PDS0084333, QTPL2PDS0085583, QTPL2PDS0085658, QTPL2PDS0085661-62
LG GW820 eXpo (LG Monaco)	32bit Qualcomm Snapdragon S1 QSD8650	QTPL2PDS0109783, QTPL2PDS01 09788-91, QTPL2PDS0109801, QTPL2PDS0015662, QTPL2PDS0015666
LG VS410PP Optimus Zone / Optimus L3	32bit Qualcomm MSM7625A	QTPL2PDS0022015, QTPL2PDS0022032, QTPL2PDS0023960, QTPL2PDS0023965, QTPL2PDS0023969-72, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798
LG MS500 Optimus F6	32bit Qualcomm Snapdragon 400 MSM8930	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0097028-30, QTPL2PDS0097587

LG VM670 Optimus V	32bit Qualcomm MSM7627	QTPL2PDS0084161, QTPL2PDS0084161, QTPL2PDS0084333, QTPL2PDS0085583, QTPL2PDS0085658, QTPL2PDS0085661-62
LG D950 G Flex	32bit Qualcomm Snapdragon 800 MSM8974AA v2	QTPL2PDS001336, QTPL2PDS0080648, QTPL2PDS0080682, QTPL2PDS0080690, QTPL2PDS0080976, QTPL2PDS0014827, QTPL2PDS0015274-275, QTPL2PDS001352, QTPL2PDS001352
LG LS660 Tribute 4G TD-LTE / LS660P	32bit Qualcomm Snapdragon 400 MSM8926	QTPL2PDS0014190-95, QTPL2PDS0013205, QTPL2PDS0014399, QTPL2PDS0014404, QTPL2PDS0014415, QTPL2PDS0078918
LG VS840 Lucid 4G (LG Cayman)	32bit Qualcomm Snapdragon S3 MSM8660	QTPL2PDS0010976-77, QTPL2PDS0050684, QTPL2PDS0050688, QTPL2PDS0013875-76, QTPL2PDS0013878, QTPL2PDS0013882-85, QTPL2PDS0013907, QTPL2PDS0013842-43,QTPL2PDS0016441, QTPL2PDS0004798

Exhibit "B"

Exhibit B

Representative Clocking System

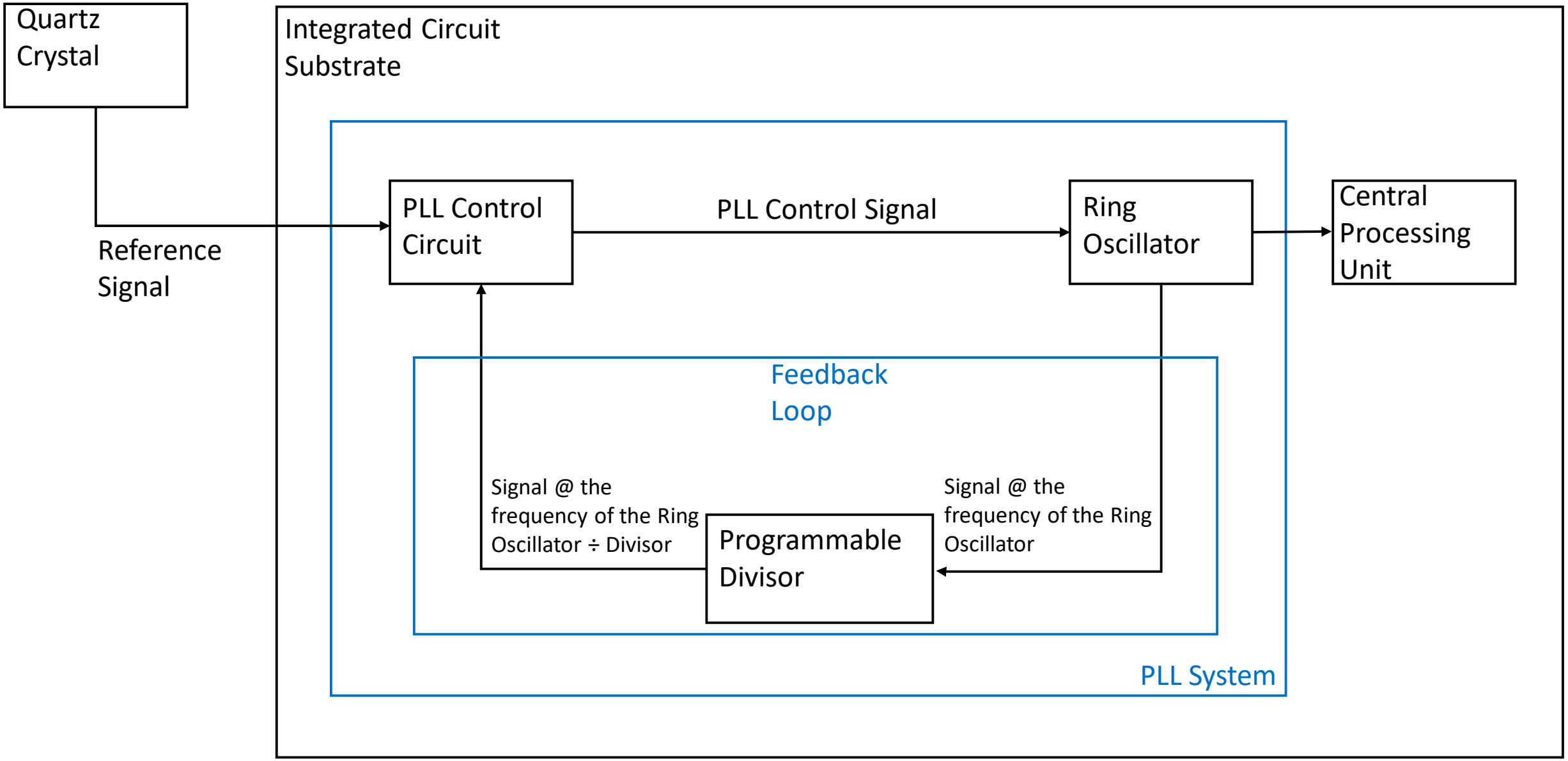


Exhibit "C"

Texas Instruments

Technical Brief
SWRA029

Fractional/Integer-N PLL Basics

Edited by Curtis Barrett *Wireless Communication Business Unit*

Abstract

Phase Locked Loop (PLL) is a fundamental part of radio, wireless and telecommunication technology. The goal of this document is to review the theory, design and analysis of PLL circuits. PLL is a simple negative feedback architecture that allows economic multiplication of crystal frequencies by large variable numbers. By studying the loop components and their reaction to various noise sources, we will show that PLL is uniquely suited for generation of stable, low noise tunable RF signals for radio, timing and wireless applications.

Some of the main challenges fulfilled by PLL technology are economy in size, power and cost while maintaining good spectral purity.

This document details basic loop transfer functions, loop dynamics, noise sources and their effect on signal noise profile, phase noise theory, loop components (VCO, crystal oscillators, dividers and phase detectors) and principles of integer-N and fractional-N technology. The approach will be mainly heuristic, with many design examples.

This document is written for designers, technicians and project managers. Design procedures, equations, performance interpretation, CAD and examples are included to help those who have little experience. A list of reference books and articles is also included.

Contents

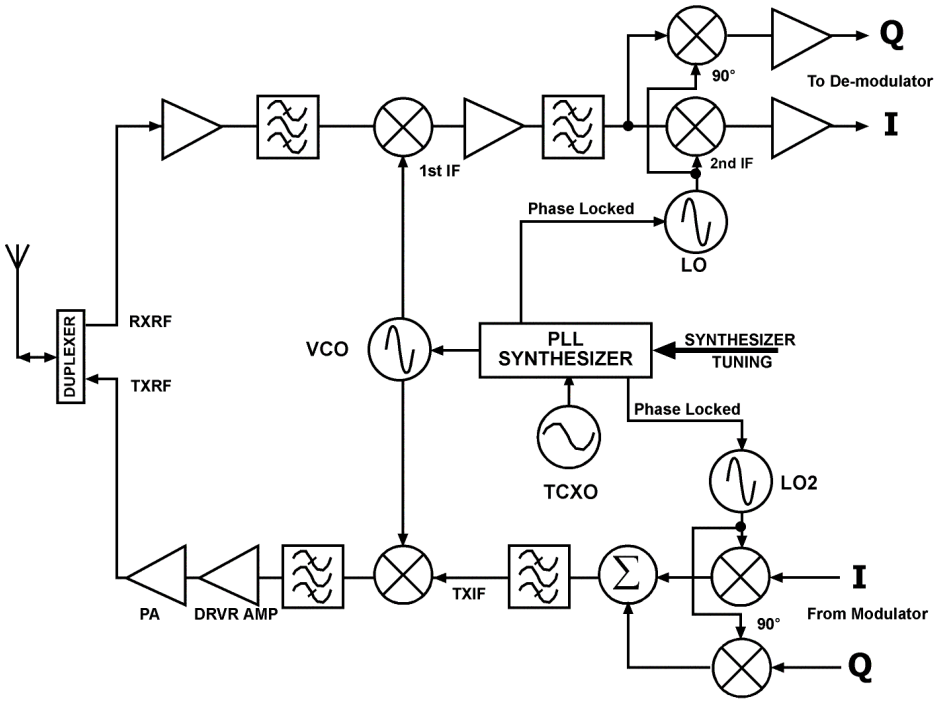
Figures

Tables

Introduction to Phase Locked Loop (PLL)

Until DSP technology is capable of directly processing and generating the RF signals used to transmit wireless data, traditional RF engineering will remain a fundamental part of wireless communication systems design. As it stands, wireless transceivers must still be able to generate a wide range of frequencies in order to upconvert the outgoing data for transmission and downconvert the received signal for processing (see Figure 1).

Figure 1. General Transceiver Block Diagram



Although there are a variety of frequency synthesis techniques, phase locked loop (PLL) represents the dominant method in the wireless communications industry. PLL, like most wireless communication technologies, is relatively new and has matured only in the last decade. The ability to execute all PLL functions on a single integrated circuit (IC) has created an economical, mass production solution to meet the needs of industry. Current PLL ICs are highly integrated digital and mixed signal circuits that operate on low supply voltages and consume very low power. These ICs require only an external crystal (Xtal) reference, voltage controlled oscillators (VCO), and minimal external passive components to generate the wide range of frequencies needed in a modern communications transceiver. Although a proven technology, PLL is still changing and evolving to keep pace with the wireless revolution.

The problems associated with operating a wireless communications system have become especially acute in the last few years with the advance of cellular telephony and the emergence of wireless data networks. Because there are more users now, most operating at progressively higher data rates, both interference and signal-to-noise-ratio have become key considerations in system design. Phase noise and spurious emissions contribute significantly to both of these issues and are largely dependent on the performance of the PLL IC. Minimizing phase noise and spurs of the frequency synthesizer while staying within power consumption, size, and cost restraints is one of the challenges for today's RF design engineers. We will see later how an emerging PLL technology called fractional-N synthesis has made this task more manageable.

The purpose of this document is to illustrate practical PLL signal generation techniques, review PLL basic building blocks, explain various phase noise sources and their measurement, and compare integer-N and fractional-N PLL technologies. The focus will be on basic principles, synthesis parameters, phase noise and its measurement, as well as design trade-off. This document is intended for design, system, and test engineers as well as technicians and technical managers.

Frequency Synthesis

Frequency Synthesis is the engineering discipline dealing with the generation of multiple signal frequencies, all derived from a common reference or time base. The time base used is typically a Temperature Compensated Crystal Oscillator (TCXO). The TCXO provides a reference frequency to the synthesizer circuit so that it may accurately produce a wide range of signals that are stable and relatively low in phase noise.

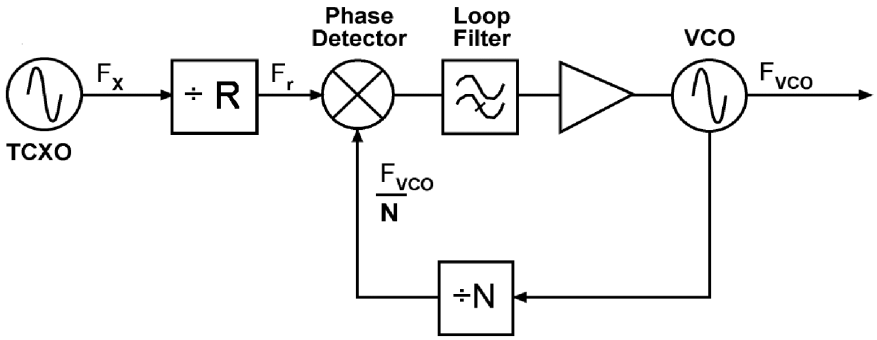
Digital PLL Synthesis

Among the many different frequency synthesis techniques, the dominant method used in the wireless communications industry is the digital PLL circuit. While there are some benefits to using other synthesis techniques, they are outside the scope of this document and will not be discussed here.

Integer-N PLL

Compared to the analog techniques used in the infancy of frequency synthesis, the modern PLL is now a mostly digital circuit. Figure 2 shows a typical block diagram of a PLL implemented with a TCXO reference.

Figure 2. Integer-N (classical) PLL Block Diagram



This traditional digital PLL implementation will be termed “integer-N” to avoid confusion due to the addition of fractional-N technology. The PLL circuit performs frequency multiplication, via a negative feedback mechanism, to generate the output frequency, Fvco, in terms of the phase detector comparison frequency, Fr.

$$Fvco = N \bullet Fr \qquad \text{(Equation 1)}$$

To accomplish this, a reference frequency must be provided to the phase detector. Typically, the TCXO frequency (Fx), is divided down (by R) “on-board” the PLL IC. The phase detector utilizes this signal as a reference to tune the VCO and, in a “locked state,” it must be equal to the desired output frequency, Fvco, divided by N.

$$Fvco / N = Fx / R = Fr \qquad \text{(Equation 2)}$$

Thus, the output frequency that the synthesizer generates, Fvco, can be changed by reprogramming the divider N to a new value. By changing the value N, the VCO can be tuned across the frequency band of interest. The only constraint to the frequency output of the system is that the minimum frequency resolution, or minimum channel spacing, is equal to Fr.

$$Channel\ spacing = Fvco / N = Fr \qquad \text{(Equation 3)}$$

When the PLL is in unlocked state (such as during initial power up or immediately after reprogramming a new value for N) the phase detector will create an error voltage based on the phase difference of the two input signals. This error voltage will change the output frequency of the VCO so that it satisfies Equation 2. As long as the system is in a locked condition the VCO will have the same frequency accuracy as the TCXO reference. If the crystal accuracy is 1 part-per-million (ppm), the output frequency of the synthesizer will also be accurate to 1 ppm.

Specifically, if Fr = 30 kHz and N = 32000, the only way for this circuit to be in a stable state (locked) is when Fvco = 960 MHz. If N were changed to 32001, a frequency and phase error will develop at the input of the phase detector that will, in turn, retune the VCO frequency until a locked state has been reached. The locked state will be reached when Fvco = 960.03 MHz and, if the TCXO has an accuracy of 1ppm, the output of the VCO will be accurate to ~ +/- 960 Hz.

Fractional-N PLL

An unavoidable occurrence in digital PLL synthesis is that frequency multiplication (by N), raises the signal’s phase noise by 20Log(N) dB. The main source of this noise is the noise characteristics of the phase detector’s active circuitry. Because the phase detectors are typically the dominant source of close-in phase noise, N becomes a limiting factor when determining the lowest possible phase noise performance of the output signal. A multiplication factor of N = 30,000 will add about 90 dB to the phase detector noise floor. 30,000 is a typical N value used by an integer PLL synthesizer for a cellular transceiver with 30 kHz channel spacing. It would seem that we could radically reduce the close-in phase noise of our system by reducing the value of N but unfortunately the channel spacing of an integer-N synthesizer is dependent on the value of N (see Equation 3.) Due to this dependence, the phase detectors typically operate at a frequency equal to the channel spacing of the communication system.

A phase detector is a digital circuit that generates high levels of transient noise at its frequency of operation, Fr. This noise is superimposed on the control voltage to the VCO and modulates the VCO RF output accordingly. This interference can be seen as spurious signals at offsets of +/- Fr (and its harmonics) around Fvco. To prevent this unwanted spurious noise, a filter at the output of the charge pumps (called the loop filter) must be present and appropriately narrow in bandwidth. Unfortunately, as the loop filter bandwidth decreases, the time required for the synthesizer to switch between channels increases.

For a 2nd order loop with natural frequency (loop bandwidth) ωn and damping factor ξ, the switching speed (Tsw) is proportional to the inverse of their product.

$$Tsw \propto 1/\omega n\xi \qquad \text{(Equation 4)}$$

If N could be made much smaller, Fr would increase and the loop filter bandwidth required to attenuate the reference spurs could be made large enough so that it does not impact the required switching speed of our system. Once again, however, the upper limit of Fr is bound by our channel spacing requirements. This illustrates how our desires to optimize both switching speed and spur suppression directly conflict with each other.

A newly emerging PLL technology has made it possible to alter the relationship between N, Fr, and the channel spacing of the synthesizer. It is now possible to achieve frequency resolution that is a fractional portion of the phase detector frequency. This is accomplished by adding internal circuitry that enables the value of N to change dynamically during the locked state. If the value of the divider is “switched” between N and N+1 in the correct proportion, an average division ratio can be realized that is N plus some arbitrary fraction, K/F. This allows the phase detectors to run at a frequency that is higher than the synthesizer channel spacing.

$$Fvco = Fr\ (N + K / F)\ N, K, F \text{ are integers} \qquad \text{(Equation 5)}$$

Where: F = The fractional modulus of the circuit (i.e. 8 would indicate a 1/8th fractional resolution.)
K = The fractional channel of operation.

PLL Parameters

There are several important parameters for signals generated by a PLL circuit.

Frequency range, or tuning bandwidth - the frequency band needed for the application. Most cellular, PCS and Satcom applications are narrow band (covering 3-10% bandwidth.) As an example North American cellular standards, AMPS, TDMA or CDMA, cover 25 MHz in the 900 MHz band.

Step size or frequency resolution - the smallest frequency increment possible. It is Fr for integer-N and Fr/F for fractional-N. In the North American cellular system, step size is 30 kHz. In China, Japan and the Far East it is 25 kHz. In Europe, the GSM cellular system requires a 200 kHz step. In FM broadcasting radio, the step size is 100 kHz.

Phase noise - an indicator of the signal quality. Phase noise and jitter are manifestations of the same phenomena (the former in the frequency domain, the later in time domain.) Clean signals have low jitter, which results in much of their total energy being “concentrated” close to the center frequency of operation. Phase noise is specified in a variety of ways: time jitter (nsec rms), degrees rms, FM noise (Hz rms) or spectral distribution density L(fm).

Spurious signal level - a measure of the discrete, deterministic, periodic interference "noise" in the signal spectrum. Spurious signals are part of the signal's "noise spectrum" and represent any discrete spectral line not related to the signal itself. Harmonics (and sometimes sub-harmonics) are usually not considered as spurious signals and are dealt with separately.

Loop bandwidth - a measure of the dynamic speed of the feedback loop. Since the PLL acts as a narrow-band tracking filter, this parameter indicates this filter's single sideband bandwidth. For many designers, this bandwidth is synonymous with the loop's natural frequency $\omega n/2\pi$ or the frequency in which the open loop gain equals 1. ωn is always a design parameter when optimizing for phase noise, switching speed, or spur suppression.

Switching speed - a measure of the time it takes the PLL circuit to re-tune the VCO from one frequency to another. This parameter usually depends on the size of the frequency step. Because the synthesizer output frequency approaches the intended frequency asymptotically, switching speed is typically measured by the time it takes to settle to within a specified tolerance from the final frequency.

Other parameters deal with size, power, supply voltage, interface protocol, temperature range and reliability. A detailed discussion of these parameters is beyond the scope of this document.

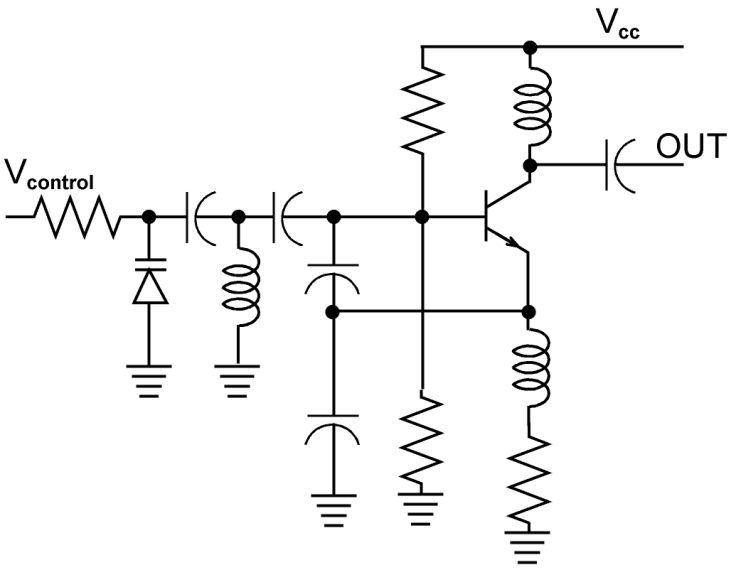
PLL Components

The four basic components of a PLL circuit are the VCO, the phase-frequency detector, the main and reference dividers, and the loop filter. Typically, the PLL IC integrates the dividers and phase detectors onboard. The reason for excluding the VCO and loop filter is to prevent the noise associated with the digital dividers and phase detectors from coupling with the VCO's active circuitry. This also allows the IC more flexibility in application.

Voltage Controlled Oscillators (VCO)

The VCO generates the output signal from the synthesizer. Voltage controlled oscillators are positive feedback amplifiers that have a tuned resonator in the feedback loop. Oscillations occur at the resonant frequency, which is typically changed, or tuned, by varying the resonator capacitance. VCOs are oscillators whose resonant tank circuit can be tuned via a control voltage that is applied across a varactor in the tank circuit. In the cellular and PCS bands, most VCOs are "negative resistance" types, with a resonator in the transistor base or emitter. Though different designers have their own schemes, they are quite similar in structure. Figure 3 shows a typical VCO design example.

Figure 3. L-Band VCO Schematics



The theoretical transfer function of a VCO is given by $ks/(s^2+\omega o^2)$. In practice, the Q of the resonator must be finite and the transfer function poles will be slightly to the left of the imaginary axis on the complex plane (poles to the right or on the imaginary axis would yield a signal with infinite energy, which is not achievable).

Varying the DC voltage across the varactor diode, which is part of the tank circuit, controls the VCO frequency. The inductor and the varactor both limit the Q of the tank circuit.

Table 1. Typical Q for Inductors and Varactors in the 800-2000 MHz Range

Type of component	Typical Q
Microstrip line on Fr-4	6-12
Air-coil	20-50
Ceramic materials	50-200
Saw resonator	400-2000
Varactor (2-6 pF)	40-100

A VCO can be specified by its tuning gain, Kv. This is the amount of frequency deviation (in MHz) that results from a 1-volt change in the control voltage. It is measured in units of MegaHertz per Volt (MHz/V). The noise level on the VCO control line is determined by active devices and is not typically variable in a given application. Therefore, a lower Kv will generate a lower phase noise. For example, 1μV of noise on the control line will generate 20 Hz FM noise for Kv = 20 but only 2 Hz FM noise for Kv = 2. Typically, if we raise the Q of the tank circuit, we will improve the phase noise characteristics by reducing Kv (and ultimately the tuning bandwidth) of the VCO. Kv linearity is also very important because of its effect on loop dynamics. As we will see ahead in Equation 8, Kv directly affects the loop transfer function, and therefore its bandwidth. A nonlinear change in Kv across the frequency band of interest will have an affect on loop bandwidth, phase noise, and switching speed that cannot be easily accounted for by the system designer.

Oscillator design can be accomplished by analyzing either the open loop transfer functions, or the closed loop s-parameters. In the open loop analysis, oscillation will occur at the frequency where the open loop phase shift is 360 degrees and the open loop gain is greater than 1 (see Figure 4 and Figure 5).

Figure 4. Oscillator Open Loop Gain Model

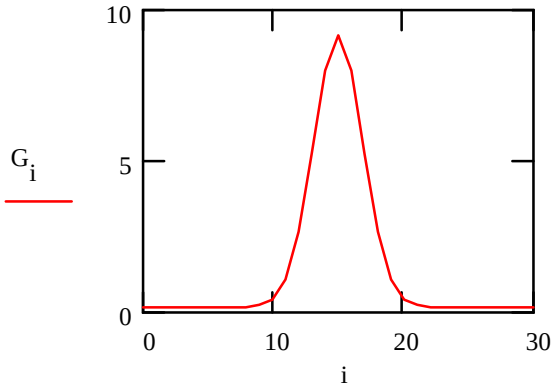
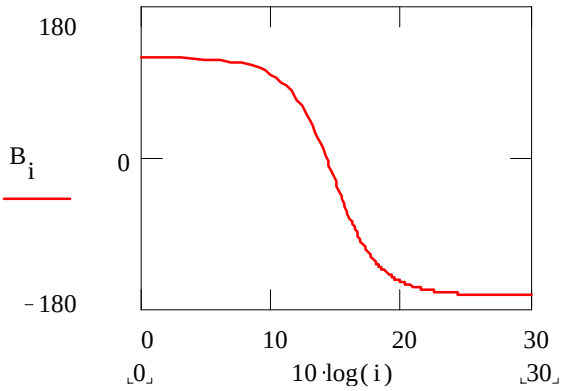


Figure 5. Oscillator Open Loop Phase Model



A VCO will start to oscillate as a consequence of background noise in the circuit. This background noise is due to the noise figure of the amplifier, the resistors, and the finite Q of the resonator. When the VCO is initially powered up, noise that is present within the frequency band of the resonator is amplified until the circuit reaches saturation. When the amplifier reaches saturation, the amplitude of the noise will stabilize and the oscillator will reach a steady state condition. If G(s) is the VCO transfer function, then the output spectrum will be given by:

$$S_0(f) = F \bullet kT \bullet |G(s)|^2 \qquad \text{(Equation 6)}$$

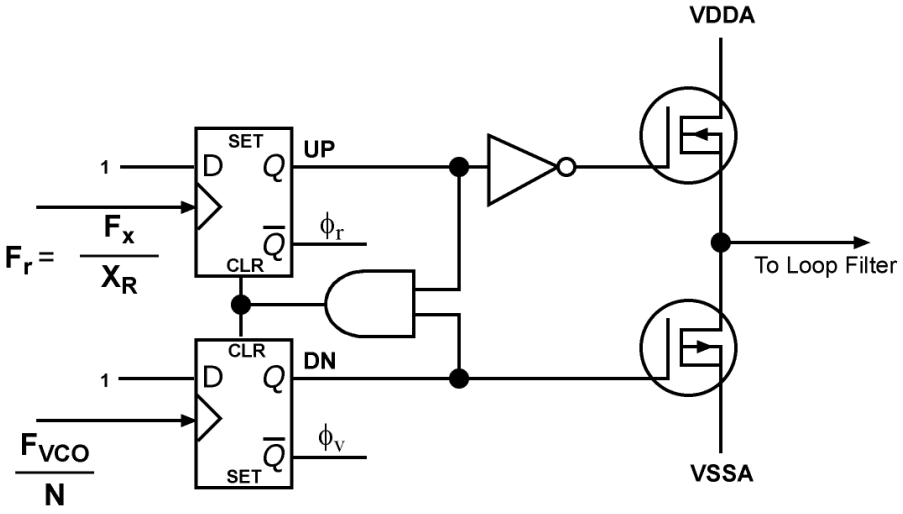
Where: k is Boltzman's constant
T is the ambient temperature in degrees Kelvin
F is the total noise figure.

The output spectrum of a VCO is therefore composed of bandpass amplified noise. The loaded Q of the resonator determines the “quality” of this noise (that is, how “narrow band” this noise is). For convenience, we model this noise signal as a sinusoid plus some arbitrary amount of noise. Almost all models use the Leeson approximation.

Phase Frequency Detectors (PFD)

The phase detector generates the error signal required in the feedback loop of the synthesizer. The majority of PLL ASICs use a circuit called a Phase Frequency Detector (PFD) similar to the one shown in Figure 6. Compared with mixers or XOR gates, which can only resolve phase differences in the +/- π range, the PFD can resolve phase differences in the +/- 2π range or more (typically “frequency difference” is used to describe a phase difference of more than 2π, hence the term “phase frequency detector.” This circuit shortens transient switching times and performs the function in a simple and elegant digital circuit.

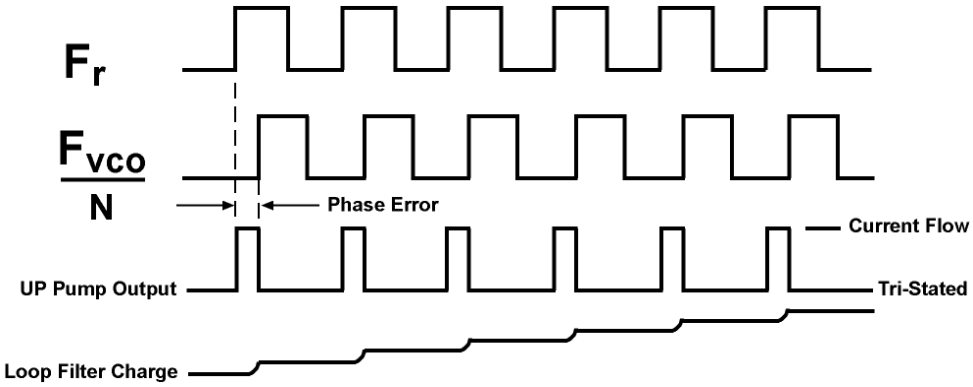
Figure 6. Phase Frequency Detector Schematic



The PFD compares the reference signal Fr with that of the divided down VCO signal (Fvco/N) and activates the charge pumps based on the difference in phase between these two signals. The operational characteristics of the phase detector circuitry can be broken down into three modes: frequency detect, phase detect, and phase locked mode. When the phase difference is greater than ±2π, the device is considered to be in frequency detect mode. In frequency detect mode the output of the charge pump will be a constant current (sink or source, depending on which signal is higher in frequency.) The loop filter integrates this current and the result is a continuously changing control voltage applied to the VCO. The PFD will continue to operate in this mode until the phase error between the two input signals drops below 2π.

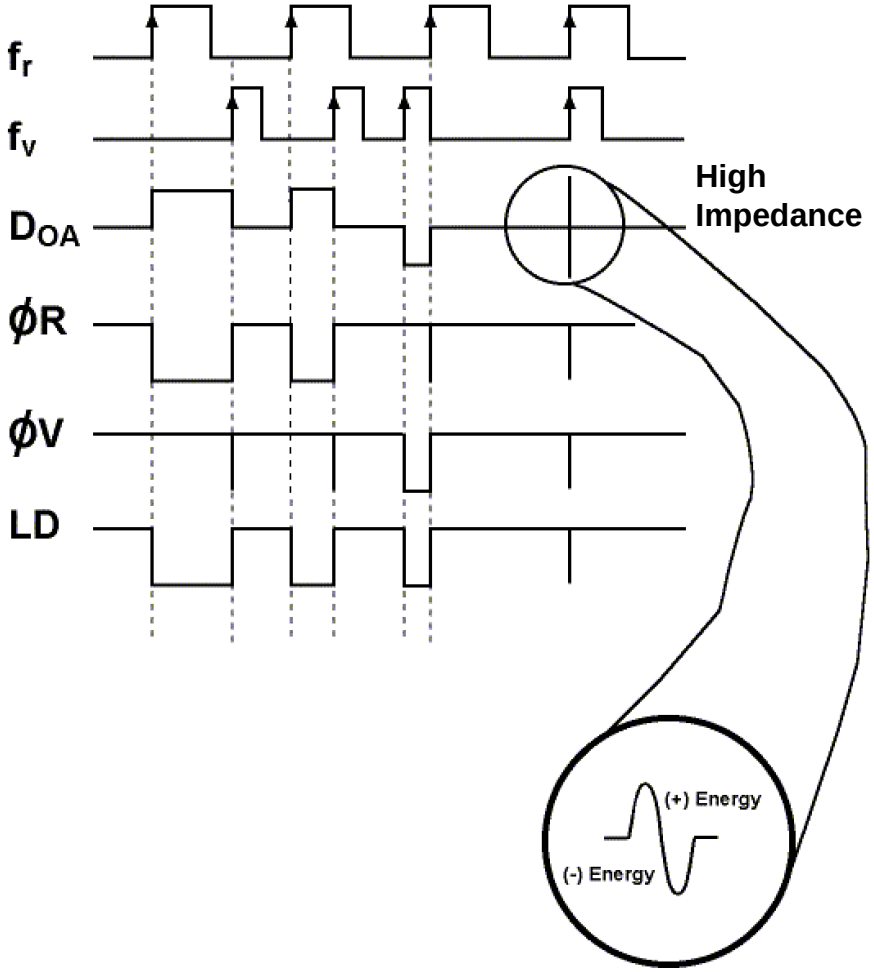
Once the phase difference between the two signals is less than 2π, the PFD begins to operate in the phase detect mode. In phase detect mode the charge pump is only active for a portion of each phase detector cycle that is proportional to the phase difference between the two signals (see Figure 7). Once the phase difference between the two signals reaches zero, the device enters the phase locked state (see Figure 8.)

Figure 7. Phase Detector Output (Voltage, Current) Waveforms, for Fv/N<Fr



In the phase locked state, the PFD output will be narrow “spikes” that occur at a frequency equal to Fr. These current spikes are due to the finite speed of the logic circuits (see Figure 8, D_{OA} blowup) and will have to be filtered so they do not modulate the VCO and generate spurious signals.

Figure 8. Phase Detector Timing Waveforms



Dividers

Dividers constitute a main function in PLL circuits. A PLL circuit needs to cover a very wide range of continuous divisions for the crystal reference and for the VCO (see Figure 2). Two types of dividers are used, high speed and low speed.

High Speed Dividers

For the high-frequency VCO's (200-2500 MHz), dual modulus dividers are employed to achieve a simple continuous division mechanism. For example, an AMPS phone needs to cover 25 MHz with 30 kHz steps. This requires the generation of about 850 contiguous N values

A "P / P+1" dual modulus divider will divide by either P or P+1 based upon external command. It has a Modulus Control (MC) input port (typically TTL or CMOS) controlling the number of times to divide by P or P+1. The lowest contiguous divide ratio for a dual modulus device is given by $P^2 – P$. Specifically, a 16/17 divider allows generation of contiguous divider values above N = 239.

Example

A divide values of N = 960 is accomplished by dividing the input signal by 16 a total of 60 consecutive times. Changing N to 961 requires that we divide the signal by 16 a total of 59 times and then divide the signal by 17 once, and so on. If we need to generate divisions in the 100-150 range using a 16/17 device there will be some numbers that can not be generated. A divide ratio of 100 can be gained by dividing twice by 16 and 4 times by 17 (17 * 4 + 16 * 2 = 100). However, there is no combination of 16 and 17 that can generate the number 103. To generate contiguous division numbers in this range would require a lower dual modulus (8/9, 10/11, etc). Dual modulus devices typically employ bipolar technology due to current consumption and speed requirements.

To run high division numbers and allow lower divisions (lower than P^2-P), tri-modulus and even quad-modulus circuits are used. One common configuration, 64/65/72, is used in a few PLL chips. For a tri-modulus P/(P+1)/(P+R) divider, the minimum continuous divide number, Nmin, is given by:

$$Nmin = (P/R + R + 1) * P + R \qquad \text{(Equation 7)}$$

For a 64/65/72 divider Nmin = 1096, compared with Nmin = 4032 for a 64/65 divider.

Low Speed Dividers

The second type of divider is the regular programmable counter. These counters typically use CMOS technology, run at frequencies up to 100 MHz, and consume very low power. These counters are used as the reference divider and also as dual modulus control counters.

A complete PLL "N" divider is typically implemented using a dual modulus divider controlled by two programmable counters, usually described as the "A counter" which determines the number of times the input is divided by P+1 and the "M counter" which determines the number of times the input is divided by P.

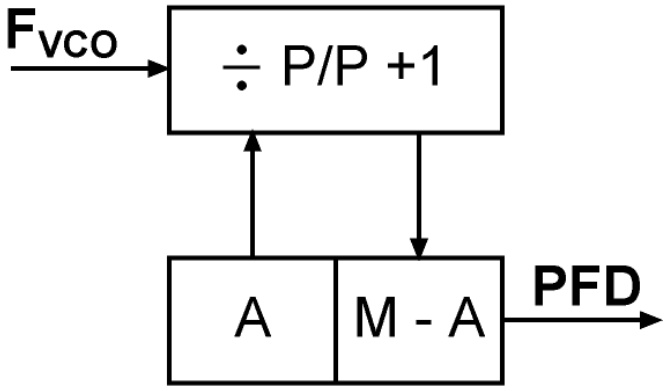
The total division ratio for the divider is given by:

$N = P \bullet A + (P+1) \bullet (M-A)$.

Note that when A is incremented by 1, M-A decreases by 1 and the total division ratio, N, increases by 1.

Note also that the minimum required bit size of the A counter is equal to the bit size of P. For 64/65, the A counter has to be of no more than 6 bits ($64=2^6$). A block diagram of a programmable divider using a dual modulus divider is shown in Figure 9.

Figure 9. Programmable Divider Using Dual Modulus



Loop Filter

There are two types of loop filters, active and passive. Active loops use op-amps, are usually differential, and allow the synthesizer to generate tuning voltage levels higher than the PLL IC can generate on-chip. The op-amp itself provides the DC amplification necessary to develop a control voltage that is higher than the on-chip supply of the phase detector. Active loops are used in wide band applications that require wide DC voltages to control the VCO. Passive filters are mainly R, C (resistor, capacitor) elements that connect directly between the PLL ASIC and VCO. Most PLL ASICs use a current source for the output to generate the control voltage. This output is proportional to the phase error (for example: +/- 1mA for +/- 2π phase error). This " current source" loop filter configuration is the most popular for wireless, narrow-band applications (see Figure 15).

The Simple Math of PLL

In this section, we present a short review of basic feedback loop principles and theory, and develop transfer functions to study the effect of various noise sources on output noise. But first we must state a most important synthesis principle: "multiplication of a given frequency by N increases the signal's phase noise by N or 20log(N)." Division, conversely, reduces the phase noise by this same factor. This effect can impact the communications system drastically. In the US AMPS or TDMA standard, multiplication by 30000 is required to generate signals in the 900 MHz range from a 30 kHz phase detector frequency. The signal's phase noise is therefore increased by 20log(30000) $\approx$ 90 dB. To put this in perspective, the phase noise of the RF signal (compared to the reference signal) has increased by a factor of one billion!

The following example helps the reader visualize the mechanism of this effect: suppose that a 1 MHz signal has a time jitter (noise) of 1 psec rms. When this signal is multiplied 1000 times to 1 GHz, the output jitter (assuming noiseless counters) stays at 1 psec, but the signal time period has decreased from 1μs to 1ns. Thus the period-to-jitter ratio has degraded 1000 times or 60dB.

Feedback Loop Analysis

We can now derive the loop equations by following the closed loop (Figure 2) path in the Laplace domain as follows:

Let φr represent the reference phase (Fr) and φo the output phase (Fo). We'll denote the loop filter network as H(s). Then, the output of the phase detector is given by:

$E(s) = (\varphi_r - \varphi_o/N)Kd$ Volts

$\varphi_o(s) = E(s)H(s)Kv/s$ (remember the VCO has a transfer function Kv/s)

Solving for $\varphi_{0/}\varphi_r$, (the effect of the input on the output), we get:

$$\varphi_{o/}\varphi_r(s) = \frac{KvKdH(s)/s}{1+KvKdH(s)/sN} = H1(s) \qquad \text{(Equation 8)}$$

For K = KvKd, we get H1(s) = KH(s)/[s+KH(s)/N] or

$$H1(s) = \frac{NKH(s)}{sN + KH(s)} \qquad \text{(Equation 9)}$$

Generally, from linear feedback control theory, we know that the transfer function for a specific input anywhere in the loop is given by the forward loop gain (from that input to the output point) divided by "1+ the open loop gain". The effect of different inputs (noise or modulation originating from anywhere in the circuit) can be calculated easily using these relations.

Example: If we add a signal E_ϕ after the phase detector to represent the phase detector additive noise, then we can obtain its effect on the output by noting that from this point to the output the forward gain is given by: KvH(s)/s:

$$\varphi_o/E_\phi(s) = \frac{KvH(s)}{s+KH(s)/N} = H2(s)$$

$$H2(s) = \frac{NKvH(s)}{sN + KH(s)}$$

The composite phase noise of the signal we generate with our synthesizer can be easily calculated by the sum effect of all noise sources on the output.

Another function of interest is the error function, defined by $(\varphi o-\varphi r)/\varphi r$, and given by:

$$H_E(s) = \frac{sN}{sN+KH(s)} = 1-H1(s)$$ and has a "high pass" characteristic.

Interpretation of the basic transfer function H1(s):

For low frequencies where s << KH(s)/N), H1(s) is approximately equal to N. The loop then behaves as a multiplier (by N) which is exactly what we wanted to achieve. However, when s >> KH(s)/N, the transfer function value diminishes, thus acting like a "low pass filter". Beyond a certain frequency which we describe as the loop bandwidth, the output will not follow, or track, the reference phase φ_r. We will see later that this is an advantage which allows us to shape the output noise profile. The circuit operates as a multiplier, but we can decide where we want to de-couple the output from the reference noise.

Generally, the transfer function H1(s) has a spectral shape similar to a low pass filter, multiplied by N (see Figure 10).

The error function, H_E, tells us that at low frequencies (relative to the loop bandwidth), the error will be low; the VCO will be "locked" to the reference. This is exactly what we wish since we want the VCO to acquire the stability of the reference frequency (crystal).

Overall, these transfer functions show that a PLL "locks" the VCO to the crystal (for accuracy and stability) while rejecting VCO noise close to the carrier. It does this by "shaping" the circuit noise in a low pass manner that decouples the VCO spectral profile from other noise sources.

For loop stability (an important issue in 3rd and 4th order loops), it is necessary that at the frequency where the open loop gain is unity, there will be sufficient phase margin (>45 degrees) to prevent oscillations. Phase margin is the open loop phase difference from 180 degrees (see Figure 16 and Figure 17).

The Laplace and Fourier Transform

We will use the Laplace and Fourier transformations throughout the analysis for the same reason we use them in all electronics circuits: they turn differential equations into polynomials, and allow easy interpretation of circuits and their frequency response. The Fourier transform is used for calculating steady state ($s = j\omega$) and the Laplace transform is used for transient analysis.

Fourier transform definition:

$F(\omega)=\int f(t)e^{-j\omega t}\,dt$ and the inverse:

$f(t)=\int F(\omega)e^{j\omega t}\,dt$

The integral limits are from $-\infty$ to $+\infty$.

The steady state (Fourier) response of H1(s), for H(s) = 1 (indicating no loop filter), is calculated to be: ($s = j\omega$)

$$H1(s) = \frac{K}{j\omega + K/N}$$

This is similar to a simple R/C circuit with a pole at ω = K/N

Laplace transform:

$F(s) = \int f(t)\, e^{-st}\, dt$

The integral is from 0 to ∞.

Both transformations are linear.

Loop Transfer Function

Let us interpret the meaning of H1(s) of the previous section, no loop filter. The response is similar to a simple R/C circuit with a pole at ω = K/N. (This is expected because we have just a single integrator in the loop, the VCO). The transfer function implies that while the (phase) frequency will be multiplied by N, the reference (φr) noise affects the output spectrum in a "controlled" way (Figure 10).

Example

Assume K = Kv * Kd = 28*10E6 sec^{-1}, and the crystal has a noise density of -165 dBC at an offset of 0.1 MHz from the carrier. For N=1000, the output noise at this offset due to crystal noise calculates to:- 105 dBC/Hz. However, because of the loop's ability to filter this noise, it can be much better than -105 dBC/Hz. The loop starts to attenuate this noise above 4400 Hz (K/N = 28*10E6/(2π•1000)) from the carrier at 6dB/octave. At 100 kHz offset, the loop will attenuate this noise by more 26dB to below -131 dBC/Hz.

We can conclude from this analysis that a PLL is a narrow band multiplier, having the characteristics of a tracking filter. We shall see later that we can easily control the bandwidth of this filter, also known as the loop bandwidth.

Viewing the error transfer function $H_E(s)$, shows that it has "high-pass" characteristics. Therefore, we can conclude that the loop "resists" low frequency changes; it "tries to acquire" the characteristics of the reference source. If we try to inject a signal in order to modulate the VCO (say in FM applications), the loop will resist this disturbance, (see figure 10). Therefore, many FM systems, and especially those used in cellular applications, must use a very narrow band loop, so that the voice (300-3400 Hz) spectrum is significantly above the frequency where the loop has an effect (typical 20-30 Hz).

VCO noise can be modeled as additive; this noise will be rejected by the loop within the loop bandwidth.

Loop Filter Design

We saw before that when there is no loop filter, H(s)=1, the loop parameters were determined by K and N. This way, our control of the loop parameters is very limited and has already been set by K and N.

To gain complete control of loop parameters, (mainly bandwidth, noise characteristics and speed), the more common (2nd order) and in fact the most popular loop structure uses (at least) another integrator, having a transfer function given by:

$$H(s) = \frac{1 + sT2}{sT1} \qquad \text{(Equation 10)}$$

where: T1=R1C, T2=R2C (see Figure 13).

Now, the new loop transfer function is given by:

$$H1(s) = \frac{K(1+sT2)/T1}{s^2 + K(1+sT2)/NT1}$$

Lets define: $\omega n=(K/NT1)^{.5}$ and $\xi=\omega nT2/2$, then:

$$H1(s) = N \bullet \frac{2s\omega n\xi + \omega n^2}{s^2 + 2\omega n\xi s + \omega n^2} \qquad \text{(Equation 11)}$$

This is the most common loop transfer function in PLL theory. The loop is of second order (has two integrators) and enables control of its dynamic characteristics, bandwidth and damping, via T1, T2, resistors and capacitor. This structure, with minor modifications, is used in most frequency synthesizer designs.

Natural Frequency and Loop Bandwidth

A normalized second order transfer function is shown in Figure 10**.**

ωn is referred to as the natural frequency, and ξ is the damping factor, both terms borrowed from control theory. For low values of ξ, the loop tends to oscillate. This is the reason for not using a pure integrator as a loop filter. Most designers use a damping factor between 0.7 and 2. The loop behavior is similar to many natural phenomena described by similar (second order) differential equations. There is a great body of literature covering this loop behavior, see the References and Further Reading section at the end of this document.

The solution of the denominator polynomial shows that:

$$S_{1,2} = -\xi\omega n +/- \omega n \sqrt{\xi^2 - 1}$$

For $\xi > 1$, settling to lock state will be asymptotic. For $\xi < 1$, it will be asymptotic with oscillation, or “ringing”, occurring at a frequency of $\omega n \bullet \sqrt{1-\xi^2}$.

The following is a review of the characteristics of this loop (see Figure 10).

The loop behaves like a low pass filter that is centered on the carrier instead of DC. (Actually, it is a bandpass tracking filter). This filter’s integrated bandwidth (also referred to as noise bandwidth), is given by:

$$B_L = \left(\int |H1(j\omega)|^2 \, d\omega\right)^{.5} = \omega n\,(\xi + 1/4\xi)/2 \qquad \text{(Equation 12)}$$

This is shown below, in Figure 10.

Figure 10. 2nd Order Loop Transfer Function. ξ = 0.7

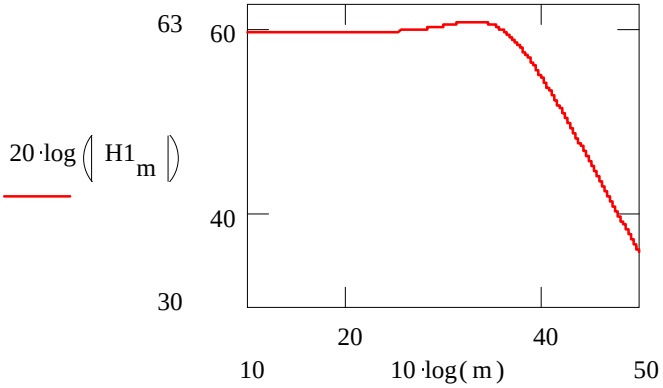
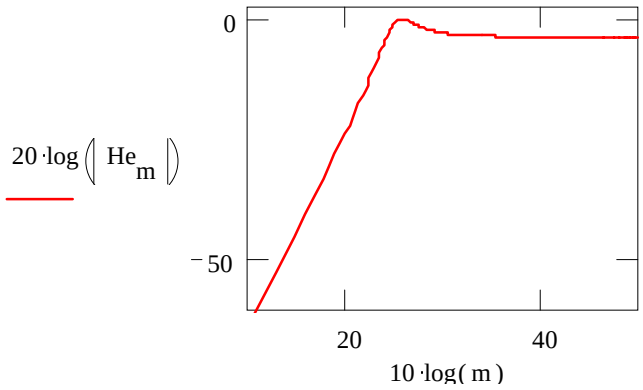


Figure 11. 2nd Order Error Transfer Function. ξ = 0.7



Minimum value for this function is for $\xi = 0.5$, there $B_L = \omega n/2$.

Figure 12. B_L Function of ξ ($j = 100\xi$)

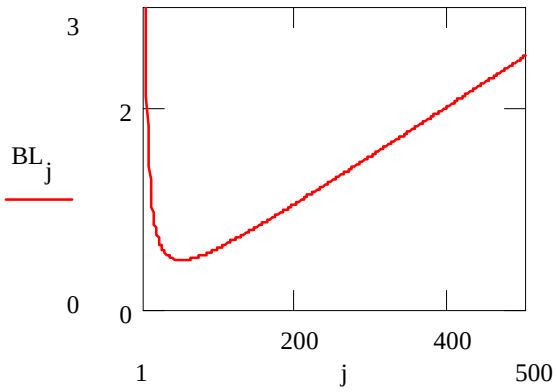


Figure 13. Active 2nd Order Loop Filters

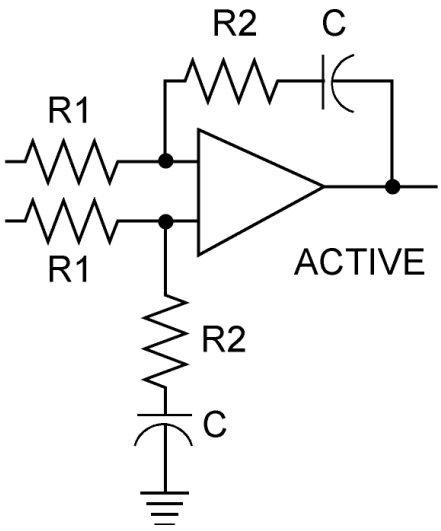
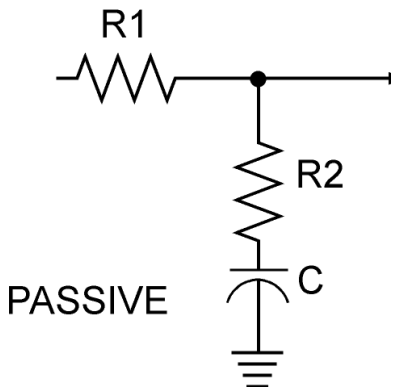


Figure 14. Passive 2nd Order Loop Filters



Though ωn is the natural frequency (the frequency at which the critically damped loop will oscillate when disturbed from equilibrium), it is also an indication of the loop bandwidth; a measure of its dynamic ability to track and follow the carrier as well as reject noise sources. Many designers refer to $\omega n/2\pi$ as the loop bandwidth. A more fundamental parameter, but not often used, is ωp, the frequency in which the open loop gain equals 1.

The loop bandwidth also indicates loop dynamics and the speed with which it will lock. The speed relationship (asymptotic behavior) depends on how far the new frequency we change to is, as well as other parameters (among them phase detector characteristics, ξ). Generally, loops with higher ωn will lock faster. Some of the speed up mechanisms actually increase ωn for the duration of the lock up (acquisition) time, to speed up the acquisition process.

Note that when ξ is very large, the 2nd order approximates 1st order characteristics as the effect of the capacitor is reduced (for very large R2, the op-amp transfer function approximates R2/R1). This is used in timing circuits to reduce “peaking” in the response.

Passive Loops and Charge Pump

In many applications, economics forbid the use of an active loop; also an active loop might not be necessary. For example, cellular synthesizers cover only 25 MHz, a 4% bandwidth. With a VCO that has a Kv = 12 MHz/V, there is no need to use any active interface between the phase detector and the VCO. Passive loops are then used and take the form of a lead-lag network such as the one shown in Figure 15.

The transfer function of this network [(R2+1/sC)/(R1+R2+1/sC)] is given by:

$$H(s) = \frac{1 + sT2}{1 + s(T1 + T2)} \qquad \text{(Equation 13)}$$

As a consequence, the difference in the loop equations is as follows:

$$\omega n^2 = \frac{K}{N(T1+T2)} \qquad \xi = \omega n(T2 + 1/K)/2 \qquad \text{(Equation 14)}$$

In high gain loops, (1/K<<T2), the equations of the active and passive loops converge.

Most common for wireless applications, the phase detector output is a current source (also referred to as charge pump) rather than voltage source. The design equations for the 2nd order loop (shown in Figure 15) are then given by:

$$\omega n = (K/NC1)^{0.5}$$
$$R = 2\xi(N/KC1)^{0.5} \qquad \text{(Equation 15)}$$

where Kv is in Hz/V
Kd is in A/rad
K = KvKd has dimensions 1/sec*Ohm. (Note: Ohm*Farad = Sec)

This network (R/C in parallel with an ideal current source) response is given by:

Vo/I = R+1/sC1

Therefore, the current to voltage transfer function Z(s) = Vo/I, is given by (1+sRC1)/sC1 (perfect integrator) and the closed loop denominator takes the form:

$s^2 + KRs/N + K/NC1$ (Equation 16)

Now ωn and ξ (shown above) are easy to derive.

Most PLL ASICs use a current source output for the following reasons:

1) It is the most convenient way to generate the analog output function of the phase detector with digital three-state devices (current sources, charge pump structure).

2) Assuming an ideal current source, the design has a real 2nd integrator (1/s) in the loop, compared with the voltage passive network.

3) Reference spurious signal attenuation by a 3rd order loop structure is easily attained by the addition of a single capacitor, (C2 in Figure 15).

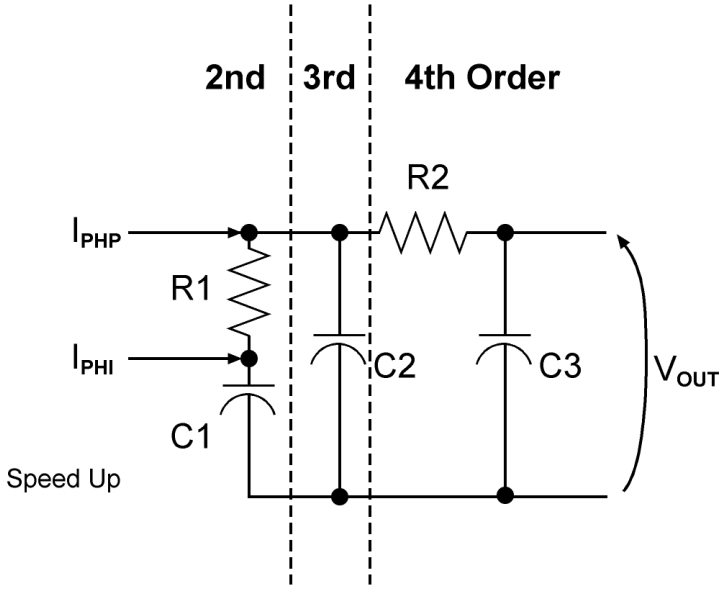
4) A single ended filter structure provides economy, compared to a differential circuit, for active loops.

As mentioned, most practical designs add a shunt capacitor (C2) between the current source output and ground (3rd order loop) to help attenuate spurious signals caused by reference spikes leaking out. The new network impedance transfer function is given by:

$$Z(s) = \frac{1+sRC1}{s^2\,RC1C2+s(C1+C2)}$$ (Equation 17)

For third order loops, (and higher), we must calculate the loop phase margin, to insure stability. (Note that 2nd order PLLs are inherently stable, if $\xi > 0$). 4th order loops add an extra R/C for additional spurious filtering.

Figure 15. Loop Filter for Current Source (Charge Pump) Phase Detector



Lock-up Time and Speed Up

Initial Lock-up

Because of the importance lock time has gained in the last few years, special techniques and circuits have been devised to improve this parameter. A PLL circuit, being a feedback loop, theoretically never achieves steady state, but always approaches that state asymptotically. Thus lock time is usually defined by approaching the final state to within some defined margin (i.e. +/- 1 kHz). In digital modulation applications, the receiving modem always has some frequency and phase tracking capability, so the frequency error tolerance is based on overall system performance requirements.

In second and third order loops, it can be shown that switching speed depends on ωn and ξ. When hopping by “dF” Hz and settling to “df” Hz away from the new frequency, the system will asymptotically converge to zero error such that $\delta f/\delta F$ is proportional to $e^{-t\omega n\xi}$, thus the switching time, Tsw, is given by:

$$Tsw = -\ln(\xi\delta)/\omega n\xi \qquad \text{(Equation 18)}$$

Example

Let:	df = 1 kHz
	dF = 20 MHz
	$\xi = 1$
Then:	$\delta = 1/20000$
	$Tsw = -\ln(1/20000)/\omega n \approx 10/\omega n$

The VCO will settle in $10/\omega n$ seconds to within 1KHz of the final frequency when hopping 20 MHz.

The speed with which the synthesizer can hop from one frequency to another is an increasingly important parameter. It is applicable as a diversity technique (narrow band signals suffer fading effects that are frequency dependant, hopping frequencies can attenuate this effect) as well as a networking protocol. Rather than operating in Frequency Division Multiplex mode in which each channel has a dedicated frequency, all channels are changed periodically in frequency to reduce the effects of multipath and external interference.

Speed Up Mechanisms

We saw that the loop parameters, ωn and ξ, determine speed. In most cases, the loop is designed for bandwidth and phase noise profiles. Sometimes, the outcome does not provide sufficient speed. To improve this parameter, simple and effective speed up mechanisms have been added to many ASICs (see the data sheets for Texas Instruments TRF2020, TRF2050 and TRF2052 circuits). Improvements of up to 5:1 are possible using simple circuitry.

One speed up mechanism performs “pre-tune” of the VCO to the desired frequency. This will expedite the time it takes the VCO to slew up (or down) and will bring it to lock proximity, where the loop can start settle and lock fast. Another technique is to increase ωn for a short time and speed up the “acquisition” time. This can be done by charging the largest capacitor in the loop filter directly, or even increasing the charge current in this short time, to expedite the charging process. One popular technique is to create a separate port that charges the capacitor in the transition. The “PHI” terminal of the TRF 2052 is a good example of this. Another method is implemented by an analog switch that bypasses the shunt resistor and allows charging of the capacitor directly. Terminal “SWM” in TRF 2020 is an example of this method. Speed up mechanisms can improve lock times by a factor of 1.5-5. Note that in the speed up mode, care must be taken to insure that the loop remains stable.

Loop Order and Type

Loop order is the number of poles in the closed loop equation denominator. Loop type is the number of poles at “0” in the open loop denominator. The 3rd order loop filter we demonstrated in Figure 8, has the open loop transfer function:

$K(1+sT2)/s^2(1+sT1)$ and is of type 2 and order 3. (Equation 19)

Loop Stability and Phase Margin

Control theory shows that for stability, the open loop phase at gain = 1 (0 dB) must be in excess of 180 degrees.

Intuition: since the feedback is negative, there is a feedback inversion of 180 degrees. The 2 poles of the 3rd order loop denominator shift the signal by another 180 degrees $\{(j\omega)^2=-\omega^2\}$, for a total of 360 degrees. Therefore an extra phase shift is necessary. Careful location of the extra pole and zero [(1+sT2)/(1+sT1)], will insure stability.

Phase margin is defined as the open loop phase difference from 180 degrees at the frequency at which the open loop amplitude gain is unity. To ensure loop stability, the usual requirement is that the system have at least 40-45 degrees of phase margin. If C2<C1/10, this condition is easily met and is the reason this rule of thumb exists.

The two controlling time constants are now T1=R1C1 and T2= R1C1C2/(C1+C2). The open loop transfer function is:

$H_{OL}(s) = T1K(1+sT2)/[s^2 \bullet C2N(1+sT1)T2]$ (Equation 20)

The phase margin is given by:

$$\phi_M = 180 + tg^{-1}(\omega T2) - tg^{-1}(\omega T1) \quad \text{(Equation 21)}$$

Sometimes, the 3rd order structure does not provide sufficient reference spurious signal rejection. One option is to add an additional R/C circuit to further attenuate the reference spectral line. This will make the loop a 4th order type. Stability requires that the pole of this additional R/C structure be at least 10 times ωn; thus we require $1/(R2*C3)>10\omega n$ (see Figure 15). Following this rule insures an additional phase shift of no more than 4-5 degrees. A simulation program is useful to calculate the total open loop transfer function and its phase shift before the design is implemented. This will insure that at the frequency where gain is 1 the phase margin is still at least 40-45 degrees, including manufacturing tolerances. Equation 22, below, is the transfer equation.

$$H4(s) = \frac{T1K(1+sT2)}{T2s^2\, N(1+sT1)\,(1+sR2C3)} \qquad \text{(Equation 22)}$$

Figure 16. Open Loop Phase of a 3rd Order Loop

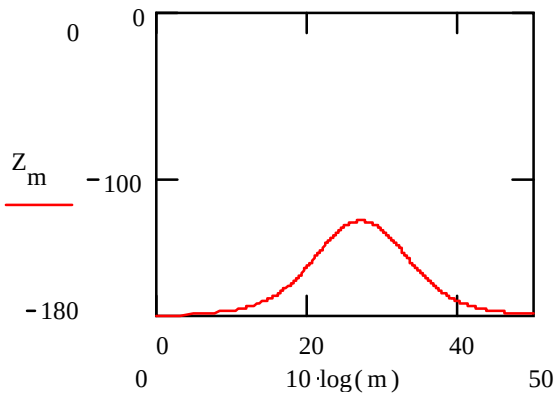
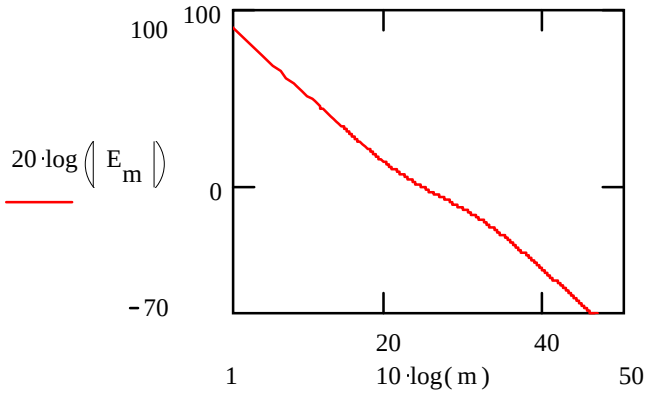


Figure 17. Open Loop Gain of a 3rd Order Loop



Active and Passive Loops Summary

The following is a short summary of various loop structures and design procedures. When possible, passive loops are used for simplicity and economy; otherwise, active loops using op-amps must be employed. In most cellular and PCS applications, the overall bandwidth is narrow (3-5%) and the output voltage from the PLL chip is sufficient to cover the band (including manufacturing tolerances). These use passive 3rd and 4th order loops. If wide-band synthesizers are necessary, (Satcom applications require 10-15 V for the VCO control) a larger (than PLL chip supply) control voltage must be generated and op-amp integrators are used. When using op-amps, differential connection is implemented. Low noise op-amps will not add significant noise to the PLL circuit.

Below is a summary of the design equations.

For 3rd order passive PLL design (most wireless applications):
Given Kv in rad/secV and Kϕ in A/rad
$\omega n = (KvK\phi/NC1)^{0.5}$
$\xi = .5 \bullet R1(KvK\phi C1/N)^{.5}$

and C2<C1/10

Tsw, switching time for convergence to df for a dF excursion is given by:
$Tsw = -\ln(\xi df/dF)/\xi\omega n$

If another R/C is required to further attenuate reference spurious signals, make sure that:
$R2C3 < 1/10\omega n$

Phase margin for a 3rd order loop:
$\phi_M(\omega) = tg^{-1}(\omega T2) - tg^{-1}(\omega T1) + 180$

For 2nd order active loop:
$\omega n = (KvKd/NT1)^{.5}$
$\xi = \omega n \bullet T2/2$
Here, Kv is in rad/secV and Kd in V/rad.

Modulation

Amplitude Modulation (AM) and Phase Modulation (PM) are usually performed outside of the phase locked loop. AM is performed by multiplying the carrier, $Sin(\omega_0 t)(1+msin\omega_m t)$, using mixers or other analog multipliers. PM is performed by complex multiplying, using quadrature modulators. This yields:

$Sin(\omega_0 t)R(t) + Cos(\omega_0 t)R\text{-}(t)$

R(t) and R-(t) are the quadrature components of the baseband information.

Generally, R-(t) will be the Hilbert transform of R(t). A variety of monolithic wide band quadrature modulators are available from various manufacturers. (The TRF 3040, soon to be released from TI, is a fractional-N monolithic PLL ASIC with an on-board quadrature modulator). R(t) and R-(t) are usually generated from a ROM or other digital memory that calculates the exact values and generates the analog signal for modulation via a Digital to Analog Converter, DAC.

Frequency Modulation (FM) can be performed by modulating the VCO directly. If a signal, V_{FM}, is injected after the loop filter on the input control line to the VCO, its transfer function is:

$$\varphi_0/V_{FM} = Kv/s/(1+KH(s)/sN) = NKv/(sN+KH(s)) = H_{FM}(s) \quad \text{(Equation 23)}$$

For a second order loop, calculating (frequency) $df_0 = sd\varphi_0/2\pi$:

$$sH_{FM}(s)/2\pi = s^2 G_L/(s^2 + 2\omega n\xi s + \omega n^2) \quad \text{(Equation 24)}$$

where G_L is a constant.

Within the loop bandwidth, the modulating signal will be attenuated (s^2 in the denominator). Two options can be utilized to compensate for the loop attenuation, depending on the application:

1) The loop is made very narrow, as in cellular FM. Beyond the loop bandwidth the transfer function becomes GL, (for $s>>\omega n$, $s^2/(s^2+2\xi\omega n+\omega n^2) \approx 1$) a constant, and will not affect the modulator. In FM cellular, the voice spectrum is >300 Hz, and loop bandwidth in the order of 30-50 Hz.

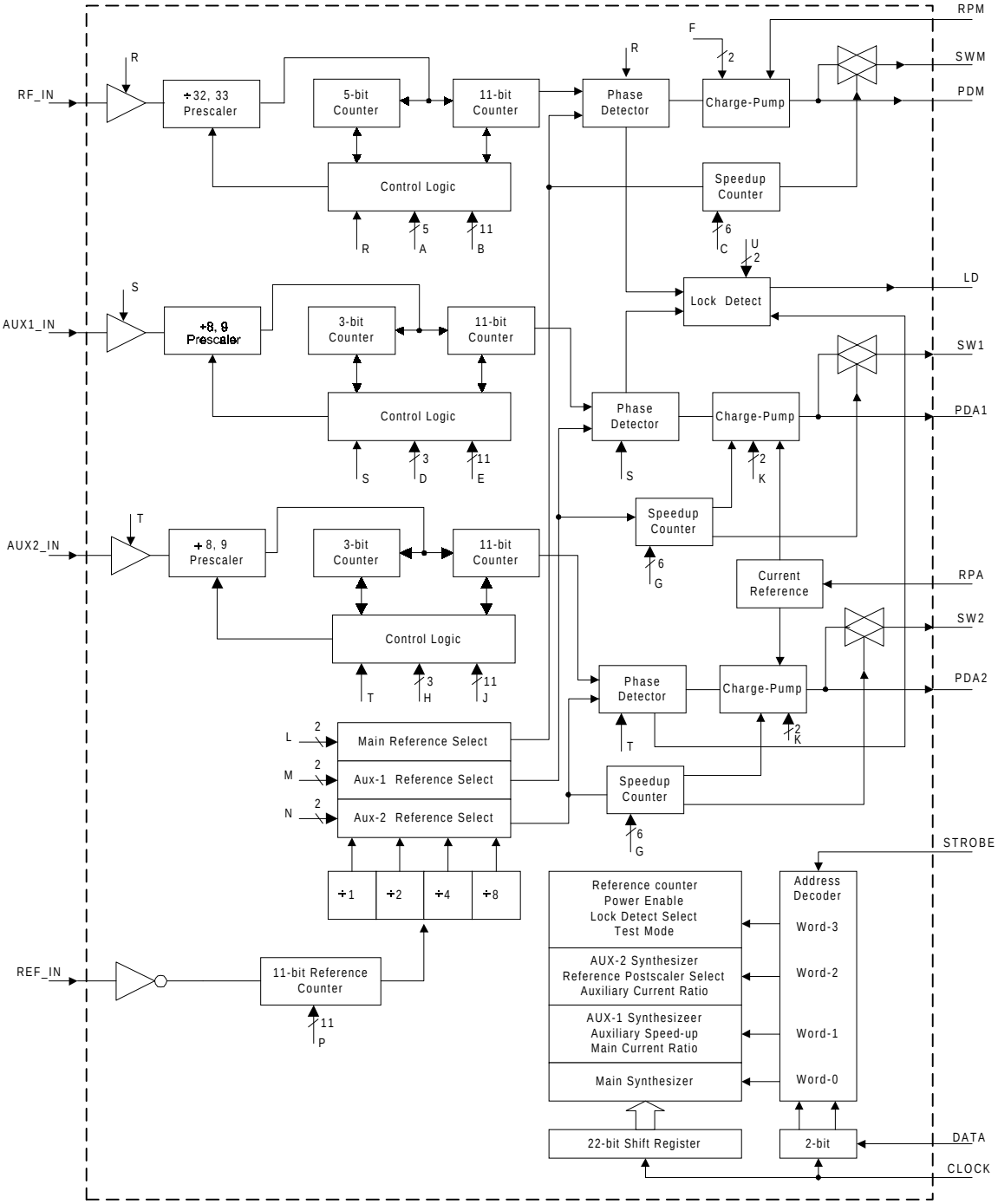
5) If the loop must be kept somewhat wide (more than 15 - 20% of the modulating frequency), then the effect of the loop must be compensated. This can be done by passing the modulating signal through a network that compensates (pre-distorts) for the transfer function. Usually, this takes the form of an integrator. More complex schemes can be applied to improve low frequency response by modulating (injecting signals) at more than one point (VCO input and PFD output).

Integer-N PLL

Concept

We can now describe in detail the “nuts and bolts” of classical, integer-N, PLL circuits. Let us review detailed functionality by describing the Texas Instruments TRF2020 PLL ASIC which is equipped with all necessary functions (see Figure 18). Let’s review the operation of the main RF synthesizer, shown in the upper part of the schematics in Figure 18, below.

Figure 18. Integer-N PLL Circuit Detail



Basic Operation

The RF section of the PLL circuit consists of the following basic blocks:

- A control interface that allows the setting of parameters (such as counters, current source values, switch mode, sleep, others) and controlling the synthesizers using an external computer/controller
- Crystal oscillator input for reference generation
- Dual modulus device (32/33)
- Reference, Fx, and main, M, A, counters. [Total divisor N is A•(P+1)+(M-A)•P. A and M are controlled by the interface.]
- Phase Frequency Detector
- Lock indicator - monitors when the loop is locked (or out of lock)
- Speed up circuit
- Power down mode (usually with a few μA current draw in this mode)
- Separate power supply pins for phase detectors allow running the device at low supply with higher output voltage from the phase detectors to control VCO across a wider range.

Functional Description

The synthesizer is set by the three wire standard interface for a specific reference frequency (the division needed from the crystal frequency to generate the reference Fr) and the division ratio of the VCO such that Fvco/N = Fv = Fr. A detailed interface protocol is available with the data sheet. The crystal reference signal is connected to the Ref input and divided by R (the P counter in the drawing). The reference (Fr = Fx/R) is compared to the VCO signal after division (Fvco/N) in the phase detector and the error signal then connects via a loop network to the VCO.

The RF signal from the VCO is first amplified (to internal logic levels) and buffered before being connected to the dual modulus divider. The input amplifier provides sensitivity (-15 dBm) and buffering from the divider (otherwise divider generated spurious signals will show at the output).

The total division (N) is determined by the number of times the dual modulus divides by P or P+1 (it is 32/33 in this case). The phase detector is a current source (charge pump) output and was designed for passive loop applications in wireless designs. Though the dual modulus device operates dynamically, dividing by 32 (M-A times) and by 33 (A times), the signals arriving at the phase detector inputs are periodic and therefore “orderly” (compared with fractional-N architectures that are not). In lock conditions, the frequency and phase (rising or falling edge) of Fr and Fvco/N will coincide (see Figure 8).

Phase Interpretation

Since there are “N” VCO clock ticks in every Fr cycle, a VCO tick counts as 360/N degrees completing a cycle (2π of Fr) in N ticks. For example, when generating 900 MHz from a 30 kHz reference (N = 30000), every VCO cycle is only 360/30000 = .012 degrees of Fr.

Divider control: for the generation of total division of 30,000, M = 937 and A = 16. This way, 16•33+(937-16)•32 = 30000.

The general formula can be derived easily:
30000/32 = 937.5.
So M = 937 and A = .5x32 = 16.

This way, a controller can easily calculate any number desired.

The supply voltage, VDD, operates all functions and can be as low as 2.7V. The phase detector supply has a separate pin that can operate up to 5.5V and allows wider VCO control range. The output of the Phase Frequency Detector controls the current sources and, in lock, will generate a DC signal. The most common loop network consists of a shunt capacitor and a R/C network, a 3rd order structure. Assuming an ideal current source, the R/C transfer function was given already. For an ideal current source (infinite output impedance), the network will represent a perfect integrator. In reality, the current source has finite impedance, Ro, and the accurate 2nd order transfer function can be modified from:
(1+sT1)/sT1
to
Ro(1+sT1)/(1+sT1+sCRo), known as a “bleeding” integrator.

Usually, an extra capacitor is added to filter out Fr pulses that show in the phase detector output pin. The time constants which determine the pole and zero frequencies of the transfer functions are defined as T2 = R1C1C2/(C1+C2) and T1 = R1C1. For C2<C1/10, T2 $\approx$ R1C2. This is the most common configuration for loop filters in wireless applications. T1 and T2 are set independently and C2 on the output port (the phase detector output) helps attenuate spurious signals. The popularity of this configuration is due to the fact that compared to an active loop, no operational amplifier is necessary and the loop is single ended, thus providing simplicity and economy.

Phase detector output (PDM in this device) current can be controlled by the function RPM. RPM can be one of four levels, up to +/- 2mA (K_ϕ = .002/2π A/rad). The SWM function (in the PFD output) allows speed up of lock time by pumping more current during the transition (charging the capacitors faster) with a capability of up to 2mA (2mA will charge a .01μF capacitor to 2V in 10μsec). When activated, the phase detector output, SWM, connects directly to the capacitor, bypassing the external loop resistor R1 (see Figure 18) and often pumping more than the PFD nominal current. After the switching transient, the SWM port goes to a high-impedance (Z) state, operating like an analog switch for the duration of the transient. The programmable speed up counter, field G, controls how long the speed up lasts (in number of reference clock cycles), so its total time is: 2*G / Fr where 0<G<64. For G = 40, with Fr = 30 kHz, speed up lasts 80/30,000 = .26 ms. In some PLL chips the speed up time in controlled by the width of the LE programming pulse.

The two Auxiliary PLL functions, AUX1 and AUX2, are very similar to the functionality of the Main PLL, except that both use a dual modulus prescaler of 8/9, compared to 32/33 of the main loop.

Advantages and Limitations

A circuit like the TFR2020 is a typical integer-N synthesizer chip. Other PLL chips in the market offer single or dual similar functions. These provide functionality, low power, space saving and economy. The device will synthesize one RF and one or two IF frequencies in a wireless radio applications for IF processing or clocking. Such devices have become the basis of wireless synthesizer technology, operating at low voltage and low current. Switching speed can be enhanced to the sub-millisecond range. One major deficiency (when critical) is the high division ratio (when generating high frequencies with small step size), thus causing significant degradation in phase noise performance. Integer-N PLL chips in the market have phase detector (PFD) noise floors of -165 to -145 dBC/Hz with 10-100 kHz Fr reference. (Noise levels usually increase with an increase in Fr). For most analog systems (FM), phase noise of such levels is sufficient. However digital technologies are more sensitive to phase noise and require more stringent control of spectral noise. Most QPSK modulations require phase jitter of <2° rms.

Some manufacturers specify PFD performance as a function of Fr speed. A general rule of thumb is that phase detector noise will increase 10 dB per decade-increase in Fr. Phase noise increases with Fr speed due to the following relationship: the time in which the phase detector (charge pump) is active (during lock) is fixed and due solely to the device architecture and speed. As the reference frequency increases, the phase detectors are active more often (their duty cycle increases) over a given time period. This adds more noise to the circuit. Other parameters have effect too like circuit symmetry, switching speed, and current output.

Fractional-N PLL

Concept

Fractional-N architecture allows frequency resolution that is a fractional portion of the reference frequency, Fr. Therefore Fr can be higher than the step size and overall division (by N) can be reduced.

The main motive for using fractional-N architecture is to improve phase noise; however, increasing Fr makes it possible to improve switching speed as well by increasing loop bandwidth.

The output frequency in fractional-N designs is given by Fvco = Fr (N+K/F), where F is the fractional resolution of the device with respect to the reference frequency.

Example: If we require 30 kHz channel spacing and have a fractional resolution of 16, Fr can be 480 kHz and N is reduced by a factor of 16.

This reduction of N implies a theoretical reduction of 20log(16) = 24 dB in phase noise performance. For a 900 MHz design, the total division ratio, N, will be ~1800 rather than 30,000 for integer-N architecture. The concept of fractional-N is achieved by generating a divider that is a fractional number rather than an integer. This is done by changing the divider in the loop dynamically, between the values N and N+1 in such a way that the “average” division becomes a fraction N+K/F. If out of F cycles, we divide by N+1 K times and by N, F-K times, then the average division is N+K/F. The principle of fractionality is therefore a result of averaging, as there is no device that can divide by a fraction.

Functional Description

Fractional-N architecture is very similar to integer-N, with the addition of an accumulator. The accumulator is a simple state machine that changes the main divider value (between N and N+1) during a locked condition. The accumulator varies the divide number between N and N+1 dynamically in such a way as to provide an averaged divide ratio that is a fractional number between N and N+1. This function enables the generation of an average division that is a fractional number.

For example: If N = 2000 and Fr = .48 MHz, the output frequency is as follows

Fvco = 2000•(.48) = 960 MHz.

In order to achieve 30 kHz resolution (generate 960.03 MHz for example), the accumulator must dynamically change N from 2000 to 2001 one out of every 16 reference cycles. Thus the division will be set to 2000 for 15 cycles of Fr and set to 2001 for one cycle of Fr. Therefore, the average division will be 2000+1/16.

(15•2000+1•2001)/16 = 2000+1/16. Here F = 16 and K = 1.

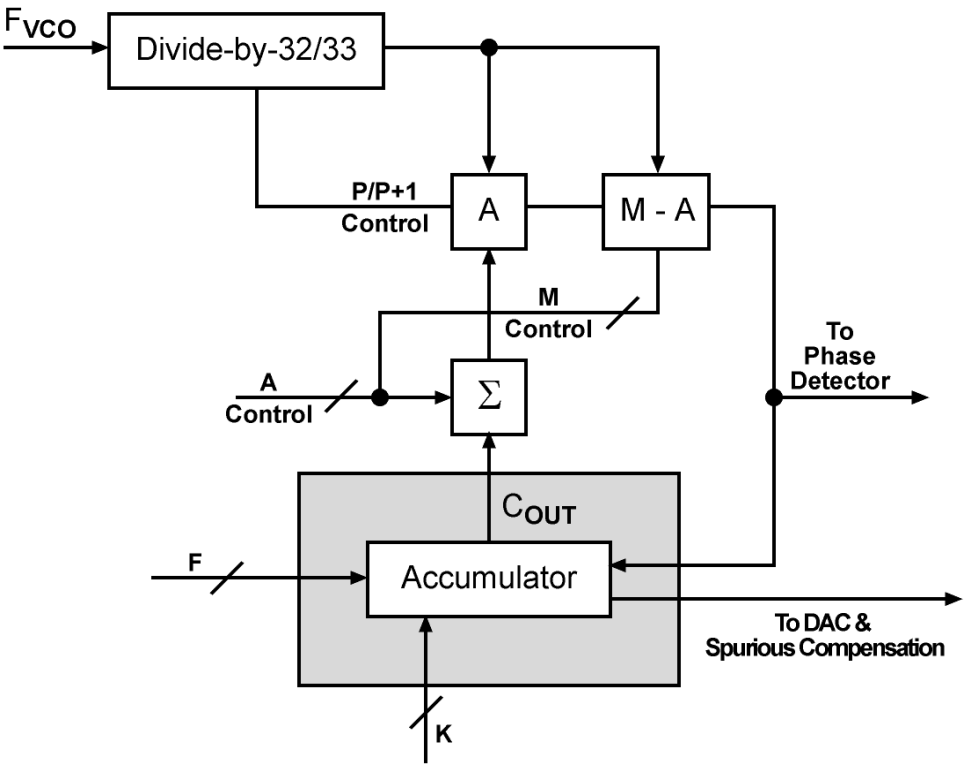
So far, we have created a fractional divider. However, rather than generating a smooth N+K/F ratio, it was done in an abrupt manner. This will cause spurious signals in the output. A spurious compensation circuit is added to reduce these spurious signals to a practical minimum.

Divider Dynamics

In integer-N PLL, the division ratio N is fixed. Every reference cycle period, 1/Fr sec, the VCO frequency is divided by N. In fractional-N, an average division of N+K/F is achieved by dynamically changing the division in such a way that in F reference cycles, K times the divider is N+1 rather than N. Thus, over F reference cycles, the total division is N*=K(N+1)+(K-F)N, and the average N*/F=N+K/F. Because there is no device that can divide by a fraction, the fractional divider value is achieved by averaging.

The elements of fractional-N (dual modulus, counters M, A) already exist in integer-N, but they need to be implemented and expanded. Remember that in integer-N, the total division is reached by commanding the dual modulus to divide A times by P+1 and M-A times by P so that N=A(P+1)+(M-A)P. Now, if from time to time, K times in F cycles, the value of A is incremented by 1, N also increments by 1 [note that (A+1)(P+1)+P(M-A-1)=N+1]. All we need to do is to add the mechanism to dynamically change the value of the A counter. The fractional accumulator performs this function (see Figure 19).

Figure 19. Fractional-N Accumulator (will change N to M)



Fractional Accumulator

Every fractional-N PLL contains a block of circuitry that is referred to as a fractional accumulator. This accumulator enables the IC to dynamically change the N divisor value *during* the locked state of the PLL (see Figure 19). The timing of the accumulator is clocked by the VCO signal (after division by N). Each time the accumulator overflows, the carry out goes from LOW to HIGH and the counter N is commanded to increment to N+1. In a system sense, K is the programmable value that is equal to the number of times the device will divide by N+1 in a full fractional divide cycle and F is the value that determines the number of reference cycles that are in each full fractional divide cycle. In actuality, F represents the size of the counter in the accumulator (i.e. F = 16 means the counter is a 4-bit counter that can count from 0000 to 1111) and K is the value that is added to this counter at the end of each reference cycle.

For example: with F = 16, and K = 3, the value of the accumulator over a full fractional divide sequence will be (see Figure 20):

0, 3, 6, 9, 12, 15, (↑2), 5, 8, 11, 14, (↑1), 4, 7, 10, 13, (↑0)

A total of 3 carry-outs (↑) occur over 16 reference cycles. Because each carry out forces the N divider to divide by N+1 for one reference cycle, the average divide ratio becomes N + 3/16.

In general, when writing to the accumulator the value K, the average division is as follows:

(N(F-K)+(N+1)K)/F = N+K/F=N* (Equation 25)

When the value at the accumulator output is not 0, (say 3 or 6), it indicates that there is a phase error between the reference (Fr) and the feedback, Fvco/N*. This phase error increases proportionally with the accumulator value (i.e. 3, 6, 9, 12, and 15) until an overflow occurs and the main divider is incremented by 1.

Note two important principles: first, we wish to increment the VCO carrier by K•2π each F cycles of Fr. The accumulator performs this function. Second, an accumulator is a digital integrator. Over F cycles, it will accumulate the value K•F, and will therefore generate precisely K carry-outs (hence a duty cycle of K/F).

The result of incrementing (by one) the value of the N divider for one reference cycle is that a full cycle of the VCO (2π), is “swallowed” and the phase error between Fr and Fvco/N is decreased by 2π. The accumulator insures that this phase error is never above 2π. After the “swallowing”, the phase error continues to accumulate. The actual instantaneous phase error between Fr and Fvco/N* can be calculated at the end of any reference cycle using the following equation:

Phase Error (radians) = (2π/F) • accumulator value

The end of a full fractional divide cycle occurs when the carry over value is equal to zero. Therefore the period of a fractional cycle is every (Fr/F) Hz.

This means that the periodicity of the phase detector output is equivalent to that of integer-N designs (with equal channel spacing), though the reference spur is now at Fr Hz away from the carrier.

Of course the abrupt change in phase associated with N being incremented by one on a periodic basis will also cause a spurious signal. This spur is called the fractional spur and can be located as close as (Fr/F) Hz away from the carrier. Although the PLL has generated the correct “average” phase slope to lock to the fractional channel, it has done so via abrupt changes in the phase slope that must be quantized in integer multiples of 2π. This spur will be of greater magnitude than a typical reference spur and also reside on the adjacent channels in worst case channel settings [1/F and (F-1)/F fractional channels]. In general applications, the fractional spur must be suppressed in some manner other than by the loop filter for this technology to be useful.

Fractional Spurious Signals and Compensation

The spurious signals generated by the accumulator can be calculated exactly by convolution of the PLL loop filter response with the Fourier series coefficients of the abrupt waveform described above. With no loop filter (i.e. infinite bandwidth), spurious signals can be approximated as 20log(2π/2√2)=7 dBC. In this case, the fractional spur will be 7 dB higher than the carrier signal. This is much larger than the typical reference spur generated by an integer-N device.

If the fractional resolution (Fr/F) is large relative to the loop bandwidth, the spurs can be easily filtered out by the loop with the addition of low pass or notch filters. For the general case of wireless communications (typically 10 kHz to 200 kHz channel spacing) traditional loop filtering will not be sufficient and the fractional architecture we described loses appeal as a synthesis method. A very narrow loop filter would result in excess phase noise and very poor lock times, offsetting any other merits the fractional architecture has. Fortunately, the fractional spurs generated by the accumulator can be reduced by as much as 40 dB (prior to loop filtering) through compensation circuitry.

The following discussion shows how the designer can compensate for these spurious signals (second order fractional) without lowering loop bandwidth.

So far we have used only the accumulator carry out to adjust for the phase error of the signal. This limits our resolution to 2π and prevents us from further attenuating the fractional spurs. If we review the accumulator content (not just the carry out), we observe that it represents the exact phase error at the end of every reference cycle. Therefore, the contents of the accumulator can be used to correct the instantaneous phase error; theoretically, we could generate a spurious free signal.

Let's consider the case for F = 8 and K = 1. Now, after the first Fvco/N cycle, the phase error (between the reference and VCO signals) is $2\pi/8$ radians, after the second cycle it will be $2*2\pi/8$ radians, and after i reference cycles the phase error will be $i \bullet 2\pi/8$ radians. It is no coincidence that i is the exact value that the accumulator holds at the end of each reference divide cycle. The same process holds true for any value of K.

To summarize, the accumulator with size F will generate K carry out transitions in F cycles. The accumulator content will represent the exact phase error necessary to be compensated at the end of each phase detector cycle:

$$\text{Phase error} = i \bullet 2\pi/F \qquad \text{(Equation 26)}$$

Where: i is the value in the accumulator
F is the fractional resolution of the device

Thus the information needed in order to compensate for the phase error is in the accumulator contents and the quality of the compensation depends only on the accuracy of the analog mechanism used to implement the correction.

For a binary accumulator, the carry out signifies 360 degrees, MSB bit represents 180 degrees, second MSB represents 90 degrees and so on. Generally, bit B from MSB represents phase $180x2^{-B}$ degrees. This is similar to the phase weight in DDS accumulators (for those unfamiliar with DDS synthesis operation see Reference 1, listed on page 54).

Table 2. Bit Weighting in a Binary Accumulator

Bit	Phase weight (degrees)
MSB	180
MSB-1	90
MSB-B	$180x2^{-B}$

For a general F size accumulator, (not necessarily binary), each increment value in the accumulator has a weight of 360/F degrees of phase error. For example, if F = 5, each bit has a phase weight of 360/5 = 72 degrees. These phase values (360*i/F) can be used to shift the VCO phase by pumping the corrective current value to the phase detector output.

Because the charge pumps “push” and “pull” current in order to change the phase of the VCO, the accumulator contents must be converted to current. The current must be scaled appropriately to correct the phase error at the end of each reference divide cycle. This current must then be added to the output of the phase detector (see Figure 22 and Figure 23). If the accuracy of this current correction is perfect, the phase correction interpolation is equal to the exact phase increments needed and all spurious signals will be cancelled (see Figure 20). Any error in the exact current used to compensate for the phase error will be periodic and will generate spurious signals with a level proportional the amount of error. Since this is an open loop analog circuit, careful design must be exercised to ensure amplitude and timing accuracy as well as temperature stability.

Figure 20. Fractional Spurious: Accumulator Only (2π Jumps Broken Line) and Analog Compensation (Straight Broken Line)

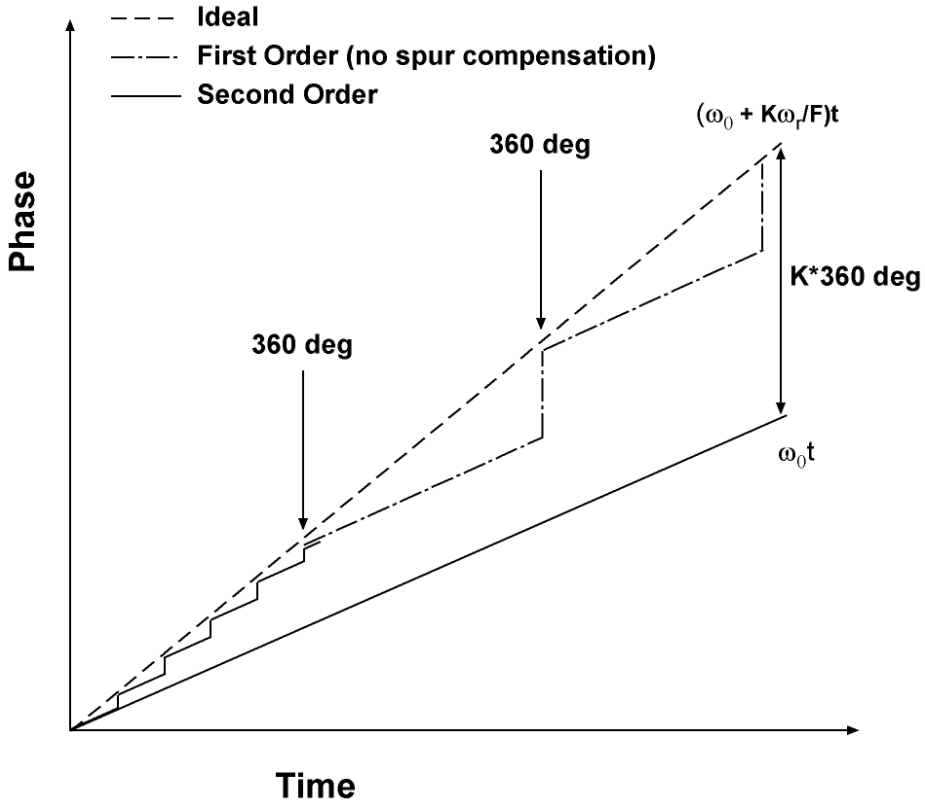
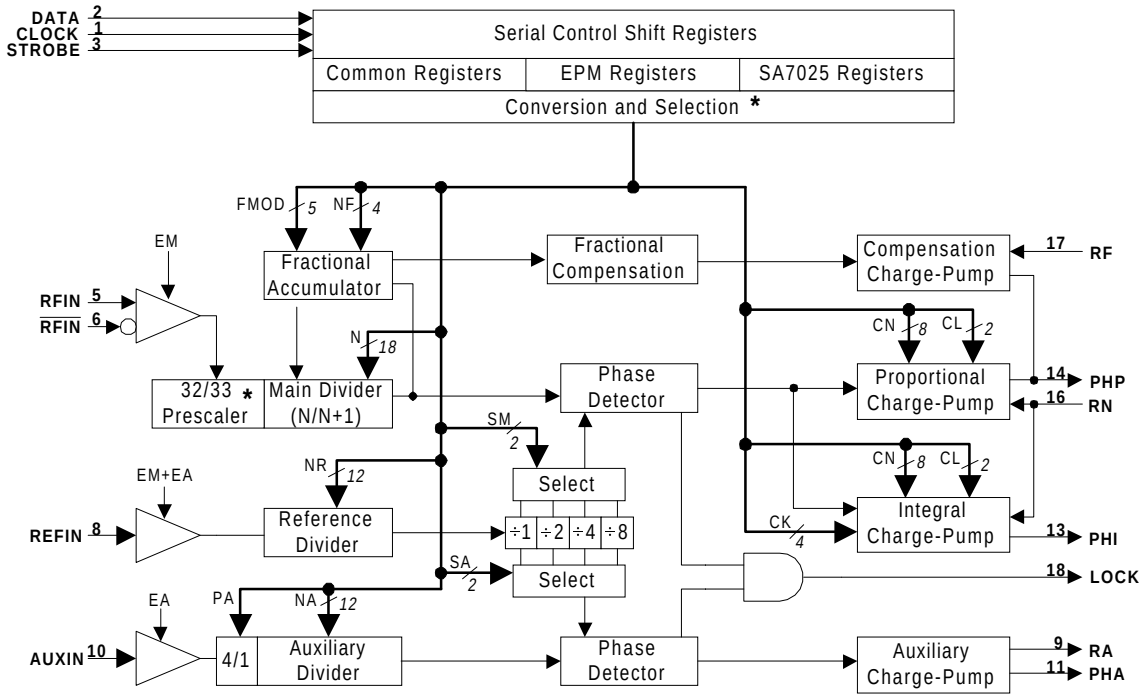


Figure 21. Fractional-N PLL - TI Model TRF2050



There are a variety of ways to implement such a compensation circuit. In a typical implementation, the accumulator (NF = 4 bits) can be any arbitrary value between 1 and 16. Its carry out connects to the main divider via an adder to allow a change in the total division ratio every time the phase error reaches 2π. The accumulator contents bits are connected via a digital to analog converter (DAC), in the Fractional Compensation block, to the output of the phase detector. If perfectly compensated, the DAC current will perfectly interpolate the phase increments at the 1/Fr time intervals. In reality, the cancellation is limited to overall accuracy, stability, aging, and temperature variation of the analog parts controlling the mechanism. The best case reduction in spurious signals is typically never better than -40 dBC. The loop filter (low pass) will further attenuate and help bring this level down to the -70 dBC range.

To improve user control of ASIC tolerances, the TRF2050 provides compensation correction control via software field CN (8-bit resolution), which helps optimize the compensation current value without the use of adjustable devices (potentiometers). This provides manufacturing convenience and economy.

Let us follow a specific detailed example for clarification.

Suppose N = 2000, F = 16 (4 bit binary accumulator) and K = 5, using Fr = 480 kHz. F = 16 indicates that the synthesizer step size is Fr /16 = 30 kHz. K = 5 indicates a desired output frequency given by: 0.48(2000+5/16) = 960.15 MHz.

Starting with an empty accumulator, after the first Fr cycle (1/.48 ≈ 2.08 μsec), the uncorrected VCO output develops a phase error given by 2π•5/16 radians. The content of the accumulator is exactly five. The following chart shows the phase error sequence (in multiples of 2π/16):

0, 5, 10, 15,↑ 4, 9, 14, ↑3, 8, 13, ↑2, 7, 12, ↑1, 6, 11, ↑0 ...

The DAC will compensate by extrapolating the abrupt phase change, and eliminate most spurious signals by feeding forward this error to the phase detector. Spurious signal compensation must be very accurate. (Phase accuracy has to be in the 1 degree range, translated at 900 MHz it is equivalent time accuracy of 3-4 psec and DAC current accuracy of 4-5 μA).

A detailed timing drawing is shown in Figure 22 (for K = 3). Complete functionality is shown in Figure 21. Note that when K and F have a common divisor higher than 1, (say Greatest Common Divisor GCD(K,F) = g) periodicity will be gFr/F, and spurious signals will show only there. Example: for F = 16 and K = 4, the spurious signals will show only in Fr/4 and its harmonics. If Fr = 240 kHz, F = 8 (step is 30 kHz) and K = 2, spurious signals will show at 60 kHz and120 kHz but not at 30 kHz since GCD(8,2) = 2.

Figure 22. Fractional-N Phase Detector Ripple for 3/8 Channel

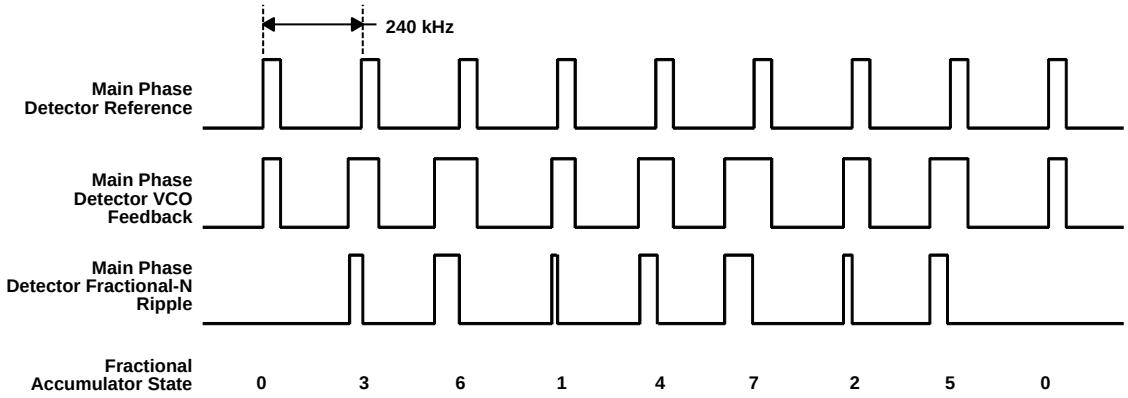
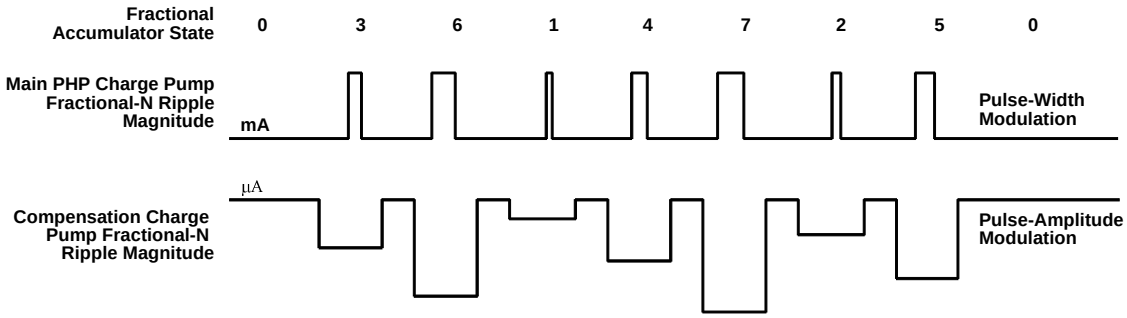


Figure 23. Main PHP and Compensation Charge Pump Fractional-N Waveforms for 3/8 Channel



Advantages and Limitation

Fractional-N architecture represents a rather simple but significant evolutionary progress of PLL architectures and does not have any major disadvantages. The additional complexity is modest, having minimal impact on power and cost, and the effect of the compensation circuit on phase detector noise density is minimal.

New fractional-N chips in the market are the products of the most advanced mixed signal IC technology. The limitations in spurious signal cancellation are mainly in the accuracy of the analog compensation circuit and its stability with time, process, and temperature changes. However, the technology already delivers spurious suppression levels of 30-40 dB prior to loop filtering. The mechanism is open loop and does not contain inherent correction. However, Texas Instruments (and others) provide programmable compensation, CN, to allow optimal control of the spurious signal levels in any given application and loop gain. Since the whole circuit is on a single die, temperature changes affect all circuits simultaneously and temperature stability is improved.

General advantages of fractional-N are the lowering of the division ratio, lowering phase noise, and improving dynamics by increasing the reference frequency. There is the potential to improve switching speed due to faster phase detector frequencies and possibly wider loop bandwidths.

When using fractional-N, while increasing Fr, we also increase the 1/F noise generated by the PFD. Therefore, we do not gain the theoretical 20log(F) in noise reduction. Typical gains are about half of that, 10log(F), which is very significant. Fractional compensation, being an analog open loop process, has achieved remarkable performance and should not be considered a limitation (as it used to be in the past). The ability to use higher reference frequencies opens the technology to applications not possible before, and allows very high frequency resolution that previously required multi-loop design.

Comparison

Fractional-N PLL represents significant progress in PLL technology. Compared to integer-N architectures, fractional-N requires a slight increase in complexity, (10-25 % in silicon area) but offers significant potential improvement in phase noise performance via reduction in division ratio. The use of higher reference frequency (Fr) offers an opportunity to widen loop bandwidth and achieve significant improvement in switching speed.

In addition, fractional-N offers high resolution in applications that would not be possible with integer-N. When step size needs be very low, integer-N collapses due to very high division ratios. This requires the use of multi-loop designs that are typically complex and expensive. Fractional-N design, due to the compensation accuracy, allows economical single loop solutions. For a 900 MHz design and 2 kHz frequency resolution, integer-N requires a division ratio of 450,000 that will result in ~116 dB in noise corruption. Such a design will have to use a very narrow loop bandwidth (< 20 Hz) to reject spurious signals and will become very sensitive to mechanical vibration. With fractional-N, with Fr = 32 kHz, and F = 16, the frequency resolution can be achieved using cellular design parameters (loop bandwidth of 200 Hz and more).

The compensation technology has matured to the point that fractional spurs (at Fr/F and its harmonics) are significantly lower than the reference spur. In fractional-N, Fr is no longer on the adjacent channel frequencies and therefore easy to filter.

The integer and fractional technologies complement one another. The statements above do not imply that fractional-N is going to replace integer-N. However, fractional-N advantages are significant, and will affect PLL evolution and market share.

Speed up is available in both techniques; however, fractional-N will usually result in faster lock times (for equal loop bandwidth) because of higher Fr. Fractional-N can be much faster as it allows the possibility of a wider loop bandwidth for similar spur suppression requirements.

All PLL devices discussed are comparable in power consumption, package size and cost. Fractional-N has a more complex phase detector and might lose some noise performance; however, this should not be significant. As a rule of thumb, fractionality (F) improves noise performance by 10log(F). Therefore from the practical standpoint, fractionality will improve phase noise by one half (in dB) of the theoretical potential. This might improve as PFD technology and device speeds improve.

We dare to predict that fractional-N is the future direction of PLL technology.

Table 3. Short Summary of TRF2050 Parameters

Parameter	Main	Auxiliary
Frequency (MHz)	1200	250
Supply	2.9 - 5.1 VDC	2.9 - 5.1 VDC
PD supply	Same	Same
Current (total)	7.5 mA	
Std. By Current (total)	<200uA	
Speed Up	Yes	No
PD Current (PHP)	2.5 mA	
PD Current (PHI)	6.0 mA	
Sensitivity (dBm)	-20	200 mV ptp
PD Current		0.25 - 0.5 mA
Ref input (MHz)	40	
Fractionality	0 to 16, programmable	No

Phase Noise

Phase noise is probably the major technical concern of frequency synthesis design. An overall radio specification will impose significant requirements on size, power dissipation, voltage requirements, cost and spectral purity. Of all the requirements, phase noise is the most challenging to the synthesizer designer. This chapter describes the definition of various interpretations of phase noise, derives the equations necessary to calculate various noise sources and offers techniques to reduce phase noise and its effect on communication channel performance.

Definitions and Conversions

Ideal deterministic waveforms, expressed as $s(t)=A \bullet \sin(\omega_0 t)$, do not exist in the real world. All real signals are narrow band noise. Thus, phase noise is our method of expressing the signal's spectrum. An ideal signal has a spectral representation of $S(\omega)=A\delta(\omega-\omega_0)$; its total energy is concentrated in a singular frequency. Real signals have a spectral distribution, and their energy is spread. The better the signal's quality, the more energy is concentrated close to the carrier.

Typically, we describe signals as $S(t)=A(t)\sin(\phi(t))$. Amplitude noise, A(t), can usually be contained to relatively low levels, with a noise density lower than -150 dBC/Hz. The more critical issue is phase noise, $\phi(t)$. The terminology (-dBC/Hz) suggests that signal perturbations caused by noise have a statistical spectral density measured in relative power to the signal's total power. –150 dBC/Hz means that in 1 Hz bandwidth at specified offset (Hz) from the carrier, the (single sideband) noise power is 10^{-15} of the total signal power. Low frequency offset noise (from DC to 100 Hz offset from the carrier in wireless) is generally attributed to the crystal oscillator slow drift caused by aging, temperature and flicker factors. This is the "long term" noise, mostly caused by crystal stability and noise, which we deal with by temperature compensation, crystal aging or using higher tolerance crystals. This noise can be tracked by the receiving end, which is always equipped with some phase and frequency tracking capability. We must be more concerned with what can be called "short-term" noise. Short-term noise contains dynamic spectral characteristics that the receiver cannot deal with and thus becomes part of the communication system noise. Phase noise can also be viewed as a type of frequency modulation. When detected, there will be low and high frequency components. One can determine what threshold of FM noise can be tolerated simply by the communications application. In voice applications, frequency modulation less than 20 Hz is not audible so we can set our noise threshold at 20 Hz. Of course, if noise were to affect our communications system from a 1 Hz or even a 0.1 Hz offset, the requirements of signal purity would increase. The higher the signal purity, the more concentrated the signal energy is at the exact carrier frequency. In a statistical sense, a lower noise signal will have a lower standard deviation in frequency or phase perturbation.

Signal spectrum is (commonly) defined by its Single Side Band (SSB) noise density, the function L(fm). Note that since the noise spectrum is symmetrical around the vertical axis, the total noise is actually twice the single sided noise density. In the time domain, phase noise is expressed as jitter, and usually measured in radians, degrees, or seconds (psec) rms. FM theory provides an intuitive description of this effect. Suppose a signal is phase or frequency modulated by a sine-wave given by:

$$S(t)=\sin(\omega_0 t+m\sin(2\pi * fm * t)), \qquad \text{(Equation 27)}$$

where ω_0 is the carrier
fm is the modulating frequency
m is the index of modulation defined as the ratio between the maximum frequency deviation and fm, (m = dfmax / fm)

We know that the sideband (noise) power spectrum of such a signal is determined by Bessel functions and depends only on the index of modulation, m. When m is very small (< 0.1), the Bessel coefficients of higher order (>1) become negligible. Then the magnitudes of the two significant sideband spectral lines that appear around the carrier are m/2 (voltage) or $m^2/4$ (power) each.

We can calculate the jitter of the carrier ω_0 when corrupted by msin($2\pi f_m t$). Since m is the peak phase deviation level in radians, this will calculate to $m^2/2$ rad^2 rms jitter. Note that the total power of the two sidebands, (showing at offset of +/- fm from the carrier, each being $m^2/4$), is $m^2/2$. So without laborious math, we can infer that for small values of m, i.e. m < .1, the (integrated) power density of the noise is equal to its phase jitter in rad^2.

We can extend the argument from spectral lines to continuous spectral noise distribution with no loss of generality. The SSB phase noise density of the signal expressed by the function $L(f_m)$, is exactly what we measure on a spectrum analyzer when we watch the signal spectrum (see Figure 24). From this graph we can easily integrate the noise to determine the phase jitter.

Example:

A 1000 MHz signal is FM modulated by a 10 kHz signal with peak deviation of 300 Hz. We can calculate the spurious signal level and the jitter directly:

Let m = 300/10000 = 0.03

$S(t) = \sin(2\pi\omega_0 t + .03\sin(\omega_m t))$ has a jitter of +/- .03 radians peak. Therefore jitter is calculated as follows:

$\phi_N = .03/\sqrt{2} = .021$ rad rms

The signal spectrum will consist of a carrier (1000 MHz) and two sidebands, at +/- 10 kHz from the carrier, both with a relative level of:

$10\log(m^2/4) = -36.5$ dBC

Total sideband noise is -33.5 dBC = 20log(.021)

Thus we infer that for low m, the phase jitter can be calculated directly from the noise spectrum, phase noise or spurious signals.

Example:

If the carrier has 6 spurious signals at different offsets from the carrier, each at -40 dBC, we can calculate phase jitter as:

$\phi_N^2 = -40+10\log(6) = -32.2$ dBC.

Therefore the rms phase jitter will be:

$\phi_N = -32.2/2 = -16.1$dBC $\Rightarrow 10^{-1.61} = 0.0245$ rad or 1.4 degree rms.

Time jitter can be calculated from phase jitter as ϕ_N/ω_0. In this case $.0245/2\pi$ nsec = 3.89 psec. Thus the zero crossings of the signal, ideally exactly at 1000 psec interval, will have now a 3.89 psec rms jitter.

We have developed a method to derive time or phase jitter from the sideband or noise spectrum. This noise can be discrete (spurious) or distributed (phase noise) and the phase jitter will be given by the integral under the noise curve as follows:

$\phi_N = \sqrt{2}\int L(f_m)df$	rad rms	or	(Equation 28)
$\phi_N = 180\sqrt{2}\int L(f_m)df/\pi$	degrees rms		
Tj (time jitter) = ϕ_N/ω_0	sec		(Equation 29)

The multiplication by • 2 (Equation 28) is to account for the total noise energy (L(fm) is single sideband).

Remember that noise distribution or spurious are always relative to the carrier power. If the synthesizer has a noise distribution of -100 dBC/Hz at 10 kHz offset from the carrier, and if the carrier total power is +10 dBm, then this noise distribution is +10-100=-90 dBm/Hz at 10 kHz from the carrier.

Division and Multiplication Effect

One of the cardinal principles mentioned already, is that multiplication by N causes loss of 20log(N) in phase noise performance; division improves by the same number. If a 100 kHz crystal signal is multiplied by PLL (or any other way) to 1000 MHz, the multiplication ratio is 10,000 and the corruption in phase noise will be 80 dB.

When divided down by a digital divider, the divider improves jitter by N times or 20log(N) in noise power. The main reason for using fractional-N architecture, is to lower N, thus lowering the value of 20log(N).

Phase Noise Measurements

In the following, we will expand on practical calculations and measurements of phase noise parameters. Let's first estimate some practical numbers.

A North American cellular design that generates 900 MHz with a reference of 30 kHz (US cellular) has a multiplication N of 30,000 which calculates to 20log(30000)=90 dB. If the phase detector in a PLL has a noise density $L(f_m)$ that is flat, with level of -150 dBC/Hz, it will generate an output spectrum that, within the loop bandwidth, is corrupted by 90 dB. Thus, within the loop bandwidth, the effective PFD noise will be approximately -150 + 90 = -60 dBC/Hz. Such numbers can be measured directly on any synthesized spectrum analyzer. Other measurement methods include comparing (mixing) the signal to a better one in quadrature and measuring the resulting noise or by comparing the signals with its replica delayed (see Figure 28).

Sometimes FM noise is specified. This can be calculated (from offset f1 to f2, in Hz rms) by:

$$\delta f\ (\text{rms}) = \sqrt{2} \int fm^2\,(fm)\ dfm \quad \text{Hz} \qquad \text{(Equation 30)}$$

In the above example, this works out to 9.8 Hz rms (given: from 100 to 10KHz offset, loop bandwidth 600 Hz, using a micro-strip resonator VCO).

For an FM system with peak deviation of 2 kHz, the signal to noise ratio, (assuming both receive and transmit synthesizers are of same quality), caused by phase noise alone (with no additional channel noise) is: $20\log[(2000/9.8\sqrt{2})^2/2] \approx 40$ dB.

The Noise Distribution Function L(fm)

When the theory of phase noise started developing some 30 years ago, there were attempts to describe phase noise in phase variation, spectral representation and even in time domain. Time domain checks the signal time jitter, then calculates its noise spectrum. This is referred to as the Allan Variance. The measurement is complicated and requires high resolution and accurate computing counters. The industry eventually converged to spectral measurements, as every synthesizer designer has a spectrum analyzer. The function L(fm) is exactly the noise level seen on the spectrum analyzer, provided that the signal is not cleaner than the analyzer (in such case, we'll measure the analyzer phase noise). Typical good quality analyzers achieve phase noise better than -90 dBC/Hz at 100 Hz offset, -100 to -105 at 10KHz and -120 at 100 kHz offset. Most analyzers can not measure phase noise with 1 Hz bandwidth directly. The measurement has to subtract the resolution bandwidth (in dB) from the value.

Example:

Let offset = 5 kHz,
difference between center frequency and offset is 70 dB
resolution bandwidth is 100 Hz,

Then L(fm) will be approximately -70 - 20 = -90 dBC/Hz.

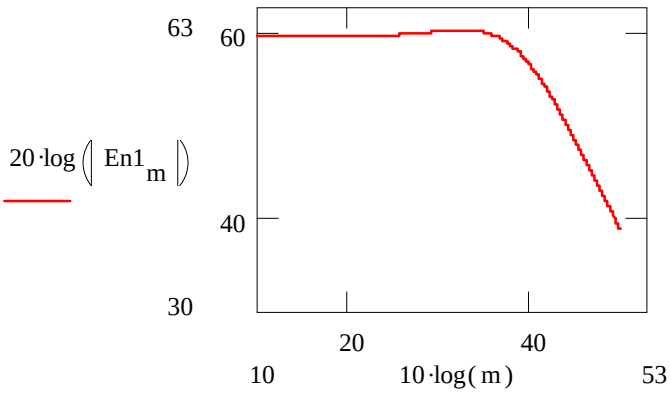
The analyzer has some correction factors that need be added, usually in the +/- 2 dB range. These emerge as a result of the type of detector in use (the spectrum analyzer detector is set to measure CW signals, noise measurement requires a correction factor) and bandwidth. Resolution noise bandwidth is not exactly that indicated by the instrument (a 100 Hz resolution filter can have 120 Hz noise bandwidth; this will cause 1 dB of measurement error).

Noise Sources in PLL

There are three cardinal noise sources in PLL circuits. Crystal oscillator phase noise affects performance very close to the carrier, usually below 10-100 Hz. Phase detector noise affects from 10-50 Hz to the loop bandwidth. Thereafter VCO noise becomes the dominant noise factor. The transfer functions for the crystal and the phase detector noises are very similar, and are given by the loop transfer function. Both will be multiplied by N within the loop bandwidth, and attenuated beyond (see Figure 23).

Note that the crystal reference Fr, usually derived from a crystal oscillator running at R * Fr, will be divided by R, thus gaining 20log(R) dB phase noise. A 30 kHz reference derived from a 9.6 MHz crystal gains 20log(9.6/.03)=50 dB. Even if the crystal phase noise at 10 Hz from carrier is only -100 dBC/Hz, after division it will be improved to –150 dBC/Hz, which is close to the phase detector noise. At higher offsets, the phase detector will have the dominant noise, with levels ranging from -135 to -165 dBC/Hz, depending on reference frequency and device in use. Phase detector noise increases with increasing Fr, at approximately 10 dB per decade rate. Both noises, crystal and phase detector, will be amplified by 20 log(N)dB within the loop bandwidth. Beyond loop bandwidth, (say $>2\omega n$), they will be attenuated by the loop transfer function (see Figure 26) and the VCO noise will become dominant.

Figure 24. Crystal and Phase Detector Noise Transfer Function, N=1000



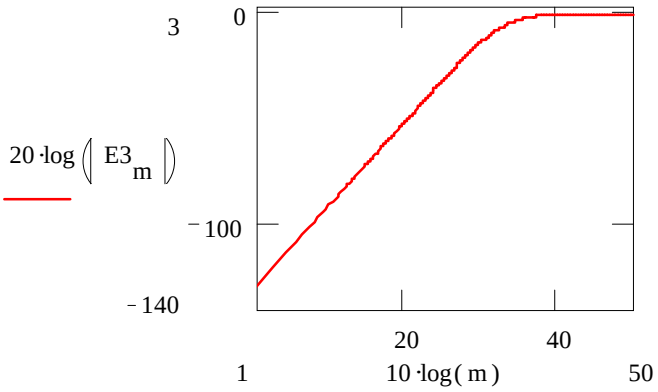
The VCO noise is multiplied by the transfer function:

$H_3(s) = s^2/(s^2+2s\xi\omega_n+\omega_n^2)$

(VCO noise contribution will be composed of the VCO noise profile multiplied by this function).

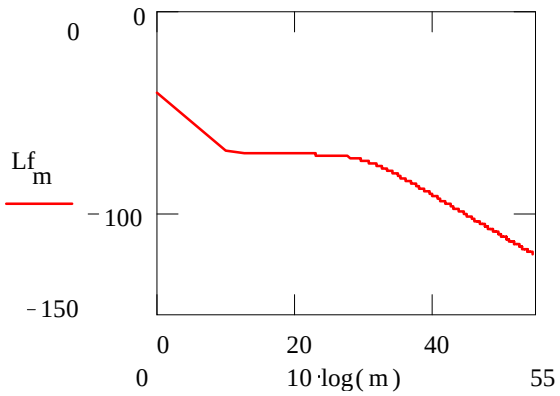
The transfer function that affects the VCO noise contribution $H_3(s)$, approaches unity for high offsets ($\omega > 2\omega_n$) but attenuates per $(\omega/\omega_n)^2$ for $\omega << \omega_n$. A simulation of VCO noise transfer function is shown in Figure 25. This is one of the more important features of PLL.

Figure 25. VCO Noise Transfer Function



While the VCO can be very noisy close to the carrier, this noise will be significantly attenuated within the loop bandwidth. Thus, for a VCO noise of -45 dBC/Hz at 100 Hz offset, the loop will contribute (in the case above) another 35 dB of attenuation, for a total of -80 dBC/Hz, significantly lower than the equivalent phase detector noise. Composite PLL phase noise is shown in Figure 26.

Figure 26. PLL Composite Phase Noise



The different noise sources show very clearly. Close to the carrier, the crystal is dominant, then from ≈ 50 Hz to the loop bandwidth, it's mainly the phase detector. At high offsets, ω>ωn, all other sources are attenuated and VCO noise controls the spectrum.

Spurious Suppression

Spurious signals are periodic interference, caused by radiation, power supply noise, mixing products, and reference (Fr) leakage. Reference signals generated in the phase detector (see Figure 8) modulate the VCO control line, causing spurious signals at the reference frequency Fr and its harmonics. There is a strict requirement on their suppression level as they interfere with the channel and corrupt adjacent spectra.

When multiplied by N, spurious signal levels increase by 20log(N) but their offset location from carrier stays the same. A 1 kHz spurious signal (say -100 dBC) on the reference (say 1 MHz), when multiplied by N=1000 times, will generate a 1 kHz offset spurious signal at the 1 GHz output frequency (with level -40 dBC).

Extra filtering is sometimes required to reduce spurious signal levels. This is the main reason for the common use of 3rd and 4th order loops.

Miniaturization of circuits puts a limit to the isolation between the digital circuits in the radio and RF sections, and some of the higher harmonics of the digital might leak, as might ground currents. Eliminating these effects requires expertise in circuit layout and grounding and shielding techniques. Detailed discussion of these issues is beyond the scope of this document.

Reference Spurious Signals

When in lock, the integer-N circuit's phase detector (being a digital part with limited speed) generates fast spikes that will leak and modulate the VCO control line, generating spurious signals at the reference frequency, Fr, and its harmonics. The spikes are short, usually in the 10nsec range, thus generating a spectrum of lines, Fr being the first and the hardest to filter. Harmonics of the line will also appear if not filtered sufficiently. Extra filtering (in most cases) is required for the 1st and 2nd harmonics. Higher harmonics are usually filtered out by the loop response.

Fractional Spurious Signals

In fractional-N circuits, because the compensation is not perfect, spurious signals will be generated at Fr and also at Fr/F and its harmonics. For Fr=480 kHz and F=16, the hardest spurious signal to filter will not be the reference F_r (which is quite high in frequency), rather it will be the 30 kHz spurious signal, (Fr/F, 480/16 = 30 kHz). Good fractional-N ASICs will compensate to -40 dBC or better. Additional filtering will be necessary. This is usually provided by the loop response. Also, the manufacturer may provide compensation adjustment. This may be manual, via a pin connected to potentiometer, or in software, to allow optimization in use. (The TI TRF2050 provides such a mechanism. See function CN on the chip). Fr is mostly attenuated by the 3rd order structure, providing significant extra filtering at the higher frequencies.

Spurious Signal Suppression

Few filtering techniques are needed to suppress spurious signals. In most cases a 3rd order loop is sufficient. If not, an extra R/C filter or sometimes two are added, and even notch filtering might be considered. These can be either LC type or twin-T structure.

External Filtering Techniques

The most common loop structure for cellular applications is the 3rd order loop shown in Figure 8. The capacitor C2 attenuates the current impulse spikes. Overall attenuation is achieved by the combination of the loop filter rejection and the external network. The attenuation level can be calculated by imposing the loop transfer function onto the impulse spectrum. Twin-T notch filters use resistor/capacitor components only and can be used as well. They will add 30-40 dB of attenuation.

Active Spurious Signal Cancellation

We have discussed so far two main methods for cancellation of spurious signals, one using filtering and one using feed forward current for fractional-N compensation. There is another fractional-N technology, (3rd order) using Sigma-Delta modulation approximation that is similar to the method used in audio CD players. This method enables spurious signal reduction via complex DSP operation, over sampling, and noise shaping. There are no such devices in the market at this time (early 1999), and the details of this method are beyond the scope of this document.

The Effect of Phase Noise on System Performance

Phase noise is a critical wireless issue because of its effect on the total communication system and network performance. Let us summarize the arguments we have raised so far in this document:

- ❒ Phase noise is part of the communication channel noise. Excess phase noise causes potential errors and adds to the channel noise.
- ❒ Channeling, accuracy and co-channeling are major considerations in wireless networks.
- ❒ Frequency re-use and low mutual interference is the basis for all cellular telephony.
- ❒ Spurious signals and excess phase noise can cause interference with other users.

- Spectral density and the scarcity of bandwidth force government regulators and communications designers to open up higher frequency bands (an example is the PCS band in response to the crowded cellular band.) At these higher frequencies, the phase noise requirements are more difficult to achieve mainly due to the higher multiplication ratios.

Loop Response Simulation

All loop response, transfer function, stability and spurious signal analysis can be accurately simulated. Most of the transfer functions and spurious signal rejection calculated in this document have been simulated on MATHCAD. Other math software as well as specific PLL software tools are available for design and analysis from COMPACT, HP, EAGLEWARE and others.

The EAGLEWARE software package has a comprehensive CAD tool designed specifically for PLL simulations.

Multi-Loop Design

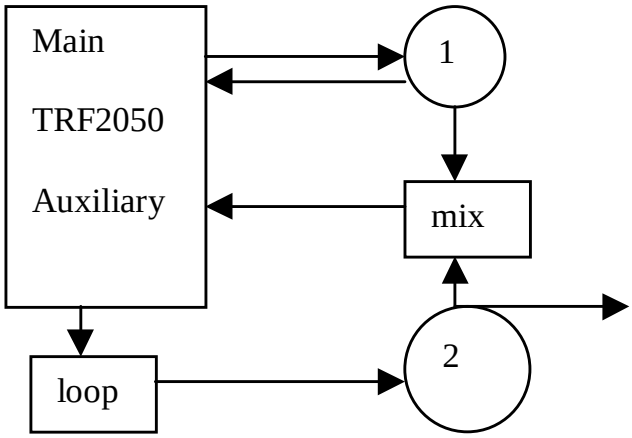
What alternatives are available for even lower phase noise? Sometimes the simple single loop design will not be sufficient even with fractional-N technology. In this event we must consider using multiple loops to reduce the division ratio.

Very complex schemes can be employed to reduce the division ratio resulting in very substantial phase noise improvement. It is possible, at least in theory, to design the circuit to perform at a noise level equal to the noise level of the multiplied crystal (at 1 GHz, loss of no more than 40 dB if the reference is 10 MHz). An example using the TI TRF 2052 is shown below (see Figure 27).

VCO1 is an auxiliary, using the main PLL section and a high reference frequency, say, 480 kHz. The loop can be wide, and we achieve excellent phase noise performance, some 15-20 dB better than with a lower reference. Then VCO2, the one used to generate the output frequency, is mixed down with VCO1 to generate a low frequency, say 9.6-10.05 MHz. The product then is connected to the Auxiliary input, where it is compared with Fr =30KHz to produce a 30 kHz step in the output. If VCO1 covers say, 960 (.48x2000) to 979.2 (.48x2040) MHz then the combined output will generate 969.6 to 989.25 MHz with 30 kHz step.

The division ratio of the main loop has been reduced to 2000 and the auxiliary loop to (320 - 335), significantly lower than a single loop (division will be in the 960/.03=32000 range). Phase noise improvement will be in the 20dB range. The price, of course, is an increase in complexity and cost. There are a variety of dual and multi-loop designs. This specific example is also referred to as “mix and count-down” architecture.

Figure 27. Mix and Count-Down Dual PLL



Measurements Techniques

We have already mentioned that some of the synthesizer parameters require special measurement techniques. We'll focus on phase noise, spurious signals and switching speed measurements.

Phase Noise

The easiest way to measure phase noise is to use a spectrum analyzer. In the case where the PLL circuit noise is lower than the analyzer's, there are alternative phase noise measurement systems. Comparing the Device Under Test (DUT) in quadrature to a low noise source (known to be much lower than the DUT) and calculating phase noise at the output of the mixer using an FFT analyzer is one method. Yet another way is to measure the phase of frequency error on a modulation analyzer.

A new set of instruments has emerged in the last few years which implement a frequency discriminator by mixing the signal with itself delayed (delay line of 200 nsec or so, using a coaxial cable). This method enables measuring free running VCO phase noise, but is limited to -45 dBC/Hz at 10 Hz offset. The measurement is a very quick and practical method for wireless applications (see Figure 28).

The simple math is as follows:
after the mixer,
$\sin(\omega t+\varphi(t))\sin(\omega(t+\tau+\phi)+\varphi(t+\tau)) \Rightarrow \sin(\omega(\tau+\phi)+\varphi(t+\tau)-\varphi(t))$
where ϕ is just a phase shifter to bring the two signals to quadrature
$\varphi(t)$ is the noise, a random process with an average of 0 and some standard deviation.

Thus the calibrated output will be $\sin(\varphi(t)-\varphi(t+\tau)) \approx \tau(d\varphi/dt)$.

A more detailed analysis yields phase difference at phase detector given by:
$\delta\phi=\omega_0 t+\sin(\pi ft)\sin(2\pi f(t-\tau/2)2\delta f/f$,

and after approximations, the voltage at the output of the discriminator dV given by:
$dV=2\pi K\phi \bullet df \bullet \tau$ (for $f\tau$ <<1) (Equation 31)
where: df is the offset from carrier,
$K\phi$ is the mixer constant.

Actually, the new constant, Kd, the frequency discriminator constant, can be expressed as:
$Kd=2\pi K\phi\tau$ and $\delta V=K*d\delta f$

At low offset, sensitivity is poor, thus the practical limitation of -45 dBC/Hz at 10 Hz offset.

Example, using a mixer with $K\phi$=0.1V/rad and τ=100 nsec, this calculates to:
Kd=0.06 μV/Hz and at 10 Hz offset, dV=0.6 μV/Hz.

Using a larger delay line (usually coax cable, not more than .5 μsec) will improve sensitivity, but the amount of improvement is limited.

Initially, the system is calibrated so that all gain stages, including phase detector loss are computed, Kd. Then the delayed carrier is brought to quadrature with the signal, and the product is processed on an FFT analyzer. Measurement is very fast, in the 5-10 second time frame.

Spurious Signals

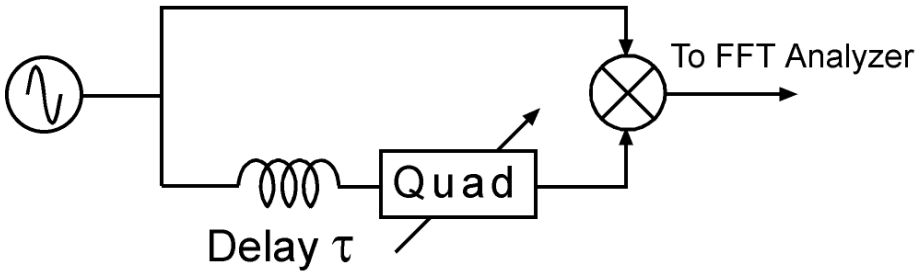
Spurious signal measurements are done directly on a Spectrum Analyzer. Any discrete line not related to the signal (excluding harmonics of the signal itself) is considered a spur. These include power supply noise (multiples of 60 Hz in North America and multiples of 50 Hz in Europe), reference Fr spurs (mainly 1st and 2nd harmonics), TCXO noise, Fx, as well as mixing products and any other spectral lines that might emerge as part of the radio design.

Switching Speed

There are few ways to measure speed:

- Use a modulation analyzer and set the measurement to be within a specified kHz from final frequency.
- Mix the hopping signal with a fixed reference set to the target frequency and check that the phase (in quadrature) is settled to within 0.1 radian or whatever the specification is.
- Use a pulse counter and check frequency after the specified speed (say 500 μsec).

Figure 28. Delay-Line Phase Noise Measurement



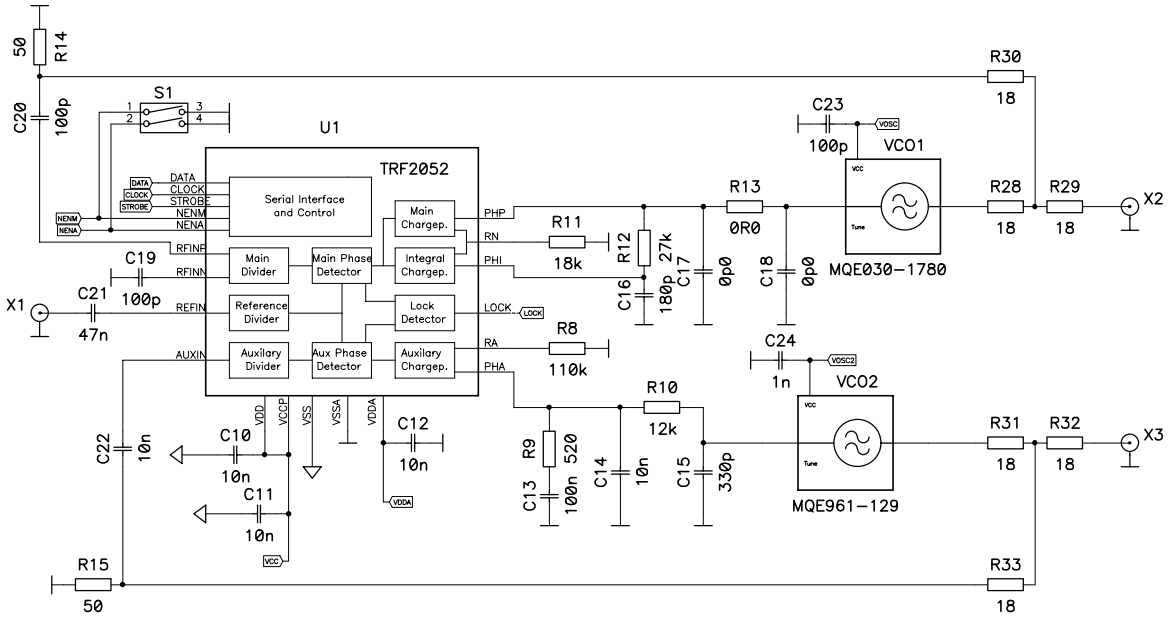
The TI Family of PLL ASICs

Texas Instruments is currently offering three PLL ASICs; two Integer-N types (TRF 2020, 2052), and one Fractional-N type (TRF 2050). The TRF2050 and TRF2052 are dual devices; they have a main and an auxiliary function, main to 1.2 GHz and auxiliary to 250 MHz. The TRF2020 is a triple device, main to 1.2 GHz and the auxiliaries to 250 MHz. One auxiliary was designed specifically for GSM internal clock generation.

For complete data sheets, please turn to our Web page. TI's Semiconductor Product Information Center at http://www.ti.com/cgi-bin/sc/support.cgi will assist you with your technical product inquiries. Our experts will provide you with accurate and prompt responses to your design-in and development needs.

Figure 29 shows the TRF2052 connected using both PLL functions and generating two signals used in wireless applications. The VCOs are from Murata (or Vari-L, Emheiser, Modco, Z-COM, and many others). Both loops use 4th order structure to attenuate the reference sidebands better.

Figure 29. Dual Synthesizer Using TRF2052



Summary and FAQ

PLL is a mature technology, yet continues to evolve rapidly. This document is a demonstration of TI's technical support and commitment to excellence in wireless technology. A second PLL document will be available dealing with design issues. Data sheets can be accessed on the Internet and evaluation boards are available from TI, including complete hardware and control software. The new PLL chips from TI represent a new dimension in functionality, density and performance. PLL circuits require an external crystal, VCO and loop filter; otherwise, all functions are performed internally.

All signals are narrow band noise. Noise shape can be controlled by loop parameters but within the loop bandwidth, will be corrupted by 20log(N).

A better noise spectrum can be achieved by lowering N. This can be done by either using fractional-N architecture or multi-loop designs.

The most popular PLL structure for wireless applications is the 3rd order loop, for which the following equations apply (see Figure 8):
$\omega n=(KvK\phi/NC1)^{0.5}$
$\xi=R/2(N/KvK\phi C1)^{2}$

Tsw, switching time to df for a dF excursion, is given by:
$Tsw = -\ln(\xi df/dF)/\xi\omega n$

For these equations, Kv is in rad/secV, and $K\phi$ is in A/rad

Detailed data sheets, application notes, evaluation cards and tech briefs, along with staff support, is available from Texas Instruments at TI's Semiconductor Product Information Center, on the Web at http://www.ti.com/cgi-bin/sc/support.cgi.

Some of the FAQs:

How do I further attenuate reference spurious signals?
Additional filtering can be achieved by adding R/C or notch filters. Loop stability must be calculated and phase margin should be at least 40 degrees.

How can I improve my phase noise performance?
The best approach is to start to use fractional-N technology and reduce the division ratio.

Why does phase noise lose 20logN within the loop bandwidth?
Because PLLs operate as a frequency multiplier by N.

How much performance do we lose due to the fact that phase error is measured only at zero crossings?
Almost none. All timing information is contained in the zero crossings.

How do we calculate phase jitter from phase noise?
You must use a computer program; it involves an integration process. See the PHAZNOIZ program, available from Texas Instruments.

What speed improvement can we expect from speed up?
Up to ratio of 10:1.

Why does lowering loop bandwidth reduce phase noise performance?
Usually, for low loop bandwidth, the VCO noise rejection is poor. Close to the carrier, this will add, and corrupt overall phase noise performance.

Glossary

AM	amplitude modulation
AMPS	Advanced Mobile Phone Service/System
dB	decibel
dBC/Hz	power relative to total signal power
dBm	decibel relative to 1 mW (1mW = 0 dBm)
Er	error, noise
f_m, ω_m	modulating frequency
F	fractionality, noise figure
FM	frequency modulation
Fr	reference frequency
Fo	VCO output frequency
Fx	crystal frequency
F(s), H(s)	transfer function
GCD(x,y)	greatest common divisor
Kv	VCO constant, usually in MHz/Volt
Kd	phase detector constant, usually V/rad or mA/rad
L(fm)	single sideband noise density
LD	lock detect
LSB	list significant bit
M, A, N	PLL counters
MSB	most significant bit
m	index of modulation
MC	modulus control
N	division ratio
P	dual modulus basic divider
PFD	phase frequency detector
R	crystal divider
PM	phase modulation
SSB	single side band

VCO	Voltage Controlled Oscillator
T, t, τ	time or time delay
TCXO	Temperature Compensated Crystal Oscillator
ξ	damping factor
ϕ, φ	phase
ϕ_M	phase margin
ωn	natural frequency
ω_0	center or carrier frequency
ωp	frequency where open loop gain equals 1

References and Further Reading

1) Bar-Giora Goldberg: Digital Techniques In Frequency Synthesis, McGraw Hill, 1996.

2) Floyd M. Gardner: Phaselock Techniques, Wiley, 1980.

3) Ulrich Rhode: Digital PLL Frequency Synthesizers: Theory and Design, Prentice-Hall, 1993.

4) Roland E. Best: PLL Theory, Design and Applications, McGraw-Hill, 1984.

5) William Egan: Frequency Synthesis by PLL, Krieger publishing, 1990.

6) James Crawford: Frequency Synthesizer Design Handbook, Artech, 1994.

7) B. Miller and B. Conley: A Multiple Fractional Divider, 42nd AFCS.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Exhibit “D”

THERMAL ANALYSIS OF CMOS VOLTAGE-CONTROLLED OSCILLATORS

Maciej Frankiewicz, Andrzej Kos
AGH University of Science and Technology, Department of Electronics

Abstract. *The paper presents impact of chip temperature on frequency generated by Voltage-Controlled Oscillators. Three different CMOS structures have been tested. Resonant cross-coupled oscillator was designed and fabricated in AMS 0.35 μm (3.3 V) technology and has at ambient temperature the frequency range from 2.2 to 2.5 MHz. Two different ring oscillators were designed in UMC 0.18 μm (1.8 V) technology and have at ambient temperature the frequency range respectively from 0.6 to 2.8 GHz and from 0.4 to 1.9 GHz. All circuits were designed using full-custom technique. Influence of temperature to tuning range and power consumption has been investigated.*

Keywords: VCO, LC, RO, CMOS, temperature

ANALIZY TERMICZNE GENERATORÓW PRZESTRAJANYCH NAPIĘCIEM

Streszczenie. *Artykuł przedstawia wpływ temperatury na działanie generatorów przestrajanych napięciem VCO. Przebadane zostały trzy różne struktury układów CMOS. Generator rezonansowy został zaprojektowany i sfabrykowany w technologii AMS 0,35 μm (3,3 V) i w temperaturze pokojowej generuje częstotliwości z zakresu od 2,2 do 2,5 MHz. Dwa odmienne generatory pierścieniowe zostały zaprojektowane w technologii UMC 0,18 μm (1,8 V) i generują częstotliwości z zakresu odpowiednio od 0,6 do 2,8 GHz oraz od 0,4 do 1,9 GHz. Wszystkie układy zostały zaprojektowane techniką full-custom. Przetestowane zostało oddziaływanie termiczne na zakres przestrajania oraz pobór mocy generatorów.*

Słowa kluczowe: VCO, układy rezonansowe, generatory pierścieniowe, CMOS, temperatura

Introduction

Work of every circuit depends on its temperature [5]. This impact is very important in case of integrated circuits where all elements are in the same silicon die and few elements dissipating large amount of power can influence big number of other elements. Because of that reason designers must take into account thermal aspects of circuit work.

Temperature dependence is especially significant factor in designing Temperature-Controlled Oscillators (TCOs). In these structures Voltage-Controlled Oscillators (VCOs) are tuned by the signal from temperature sensors. If frequency produced by generator is tuned by the chip temperature thermal behaviour of generator itself must be known. Favorable situation is when generated frequency changes with temperature monotonically, then this change can be predicted and included to design process. If so three cases are possible:

- frequency rising with temperature growth – generally higher clock frequency means higher dynamic power losses in the circuit and as a consequence higher die temperature. Such positive feedback is undesirable effect and must be compensated,
- frequency constant with temperature growth – very rare effect when generator work does not depend on thermal conditions, but can be obtained in some situations what will be presented in next sections,
- frequency falling with temperature growth – effect desirable in most of Dynamic Power Management (DPM) systems which can be combined with other methods, for example Dynamic Frequency Scaling (DFS) or Dynamic Voltage Scaling (DVS).

Another important issue is impact of temperature to power consumption of the generator.

In next sections three different CMOS generators will be described. First is LC cross-coupled structure and next are two ring oscillators. Resonant circuit was fabricated and tested in thermal chamber while in case of ring oscillators simulation results are presented. Some temperature dependencies will be defined. Obtained results can be helpful for engineers in designing TCOs or temperature-independent generators.

1. Resonant oscillator

Resonant cross-coupled generator was designed and fabricated in AMS 0.35 μm technology with 3.3 V supply voltage. LC circuits are widely used because of low phase noise and high frequency but they cover big area of the chip which can be a problem for some applications. Presented structure consists of 4 PMOS and 3 NMOS transistors. Resonant circuit is built of a spiral metal geometry which works as an inductor L, a capacitor between two polysilicon layers C_{CONST} and two varactors C_{VAR}.

Schematic diagram is presented in Fig. 1 [3, 6]. At each moment only one arm of the circuit is working and charging the LC circuit. Frequency generated by the structure is equal (1) and *C* represents combination of constant capacitance C_{CONST} and variable one C_{VAR}. In order to maximize tuning range part of the capacity coming from varactors should be more important [1].

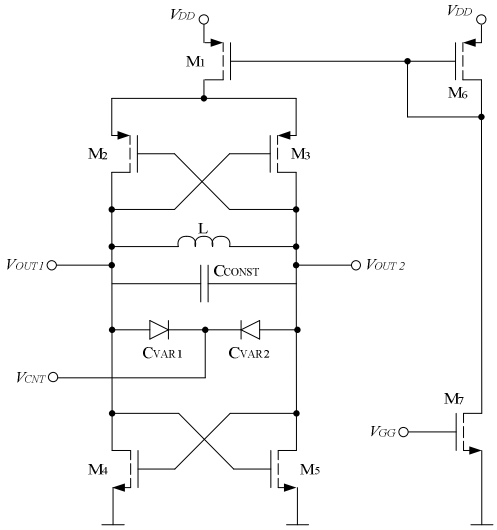


Fig. 1. Schematic diagram of the resonant VCO

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{1}$$

Measurements in thermal chamber showed that frequency generated by resonant VCO is not constant with changes of the chip temperature. Rising temperature caused higher frequency of oscillations. This can be only result of changes of LC elements parameters. Change of the transistors parameters was visible as smaller amplitude of the oscillations at hotter chip. Tuning characteristics of resonant VCO at different temperatures

Artykuł recenzowany *otrzymano: 07.07.2012r., przyjęto do druku: 23.10.2012r.*

are presented in Fig. 2. At higher temperatures oscillations started fading. The shape of the characteristic is caused by the change of varactors capacity and is nonmonotone. Useful part of it which can be took under consideration while designing the circuit is o rising range from about 1.1 to 2.3 V. Temperature dependence of this part will be investigated in next parts of the paper.

Tuning parameters of presented VCO are gathered in Table 1. For low and medium temperature relative tuning range is approximately constant an equals 11 to 13% while for higher temperatures it starts to drop below 10%. At the same time range of tuning voltage is getting narrower with rising temperature and as a consequence the characteristics are more steep. This effect must be taken into account when designing VCO working at non-constant temperature of the chip.

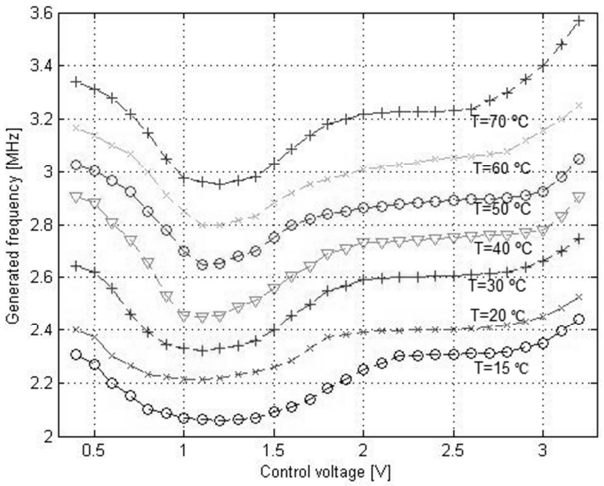


Fig. 2. Tuning characteristics of the resonant VCO for different temperatures

Table 1. Parameters of the resonant VCO for different temperatures

Temperature [°C]	Tuning range [MHz]	Relative tuning range [%]
15	0.244	11.84
20	0.278	13.11
30	0.282	12.16
40	0.291	11.88
50	0.228	8.60
60	0.238	8.50
70	0.278	9.42

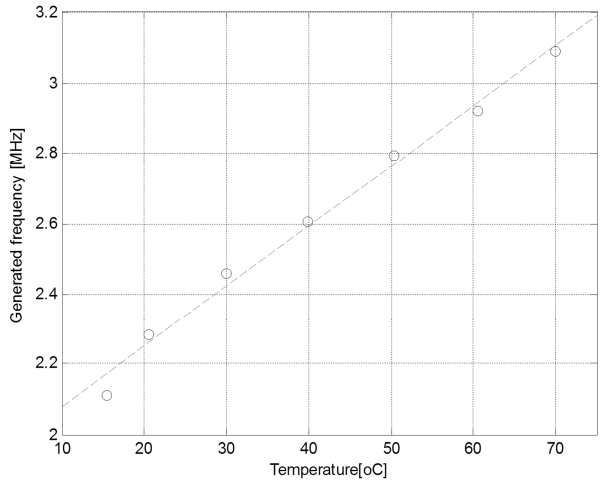


Fig. 3. Temperature dependence of frequency generated by the resonant generator for constant tuning voltage (1.6 V)

For constant tuning voltage characteristic of temperature dependence of generated frequency can be plotted, Fig. 3. This dependence is a linear function and can be described by (2) based on knowledge of frequency f_{T_A} at ambient temperature T_A = 20°C, where α and γ are proportionality coefficients.

$$f = \gamma\left(f_{T_A} + \alpha T\right) \tag{2}$$

In presented case $\gamma \approx 0.677$ and $\alpha \approx 0.116$ MHz/°C. This data can be used to calculate frequency generated by presented oscillator at every chip temperature without necessity of additional measurements.

2. Ring oscillators

Ring oscillators were designed and in UMC 0.18 µm technology with 1.8 V supply voltage. The structure consists of odd number (2n-1) of inverters connected in series, as presented in Fig. 4 [4]. Such circuit generates square wave of frequency described by (3). This frequency can be tuned by change of number of inverters N in the ring or by change of single inverter propagation time t_P.

$$f_0 = \frac{1}{2Nt_P} \tag{3}$$

Designed circuit consisted of five CMOS inverters which propagation time was controlled by change of their supply voltage. Lowering the supply value changes the time of recharging the parasitic capacitances of the structure and causes lowering of the oscillation frequency. For too low supply the oscillations will fade. Obviously on the output of the ring there has to be another inverter with constant supply which acts as a buffer for stable magnitude of output wave. Tuning characteristic of the ring oscillator for different temperatures (from 10 to 90ºC with 10ºC step) is presented in Fig. 5. Direction of temperature change is also marked.

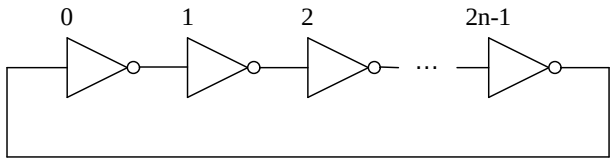


Fig. 4. Schematic diagram of the ring oscillator

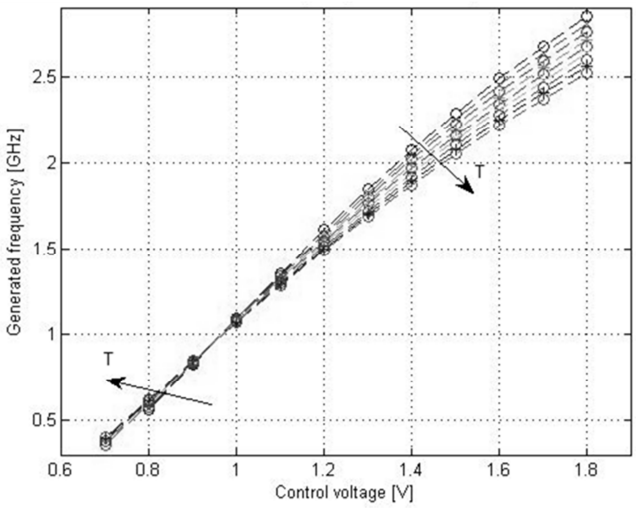


Fig. 5. Tuning characteristics of the ring oscillator for different temperatures

Thermal behaviour of the ring oscillator is quite complex issue. With change of the temperature parasitics change but also the carriers mobility changes (which affects currents). As an effect the direction of the characteristic change is not monotone. What is more, for higher temperatures the tuning range is narrower. Tuning ranges for different temperatures are gathered in Table 2. Despite the fact that they are getting narrower with temperature growth, they are still much larger then in case of resonant oscillator which is a great advantage of such ring oscillator. For higher control voltages the generated frequency is getting smaller with temperature growth. Such situation is desired for Dynamic Power Management systems to ensure thermal safety of the circuit. On the other hand at low control voltages the frequency is slightly rising. Special attention has to be paid to this region while designing the circuit. Between them there is a single point at about 0.93 V where generated frequency is independent on temperature. This information is very useful when integrated circuit designer wants to implement stable oscillator in the circuit with changing thermal conditions. In such situation presented ring oscillator with proper control voltage can be used. Dependence between generated frequency and temperature for three different control voltages is presented in Fig. 6. Every presented curve in figure below can be described by (2) because they are linear but for every temperature the coefficients α and γ would differ.

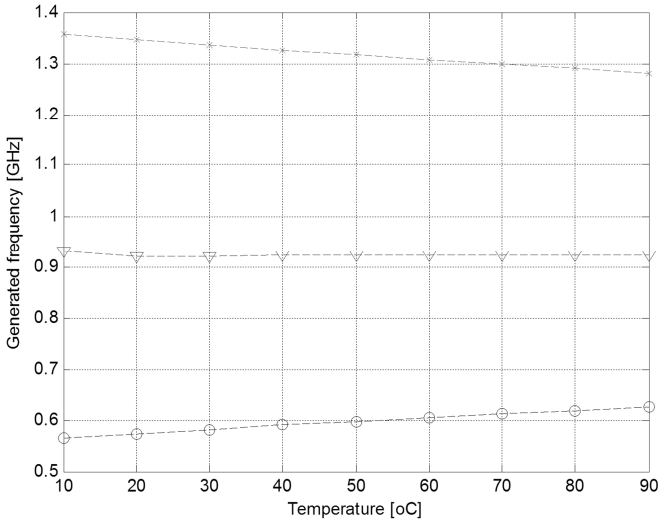


Fig. 6. Temperature dependence of frequency generated by the ring oscillator for constant tuning voltage (1.1 V - top; 0.93 V - middle; 0.8 V - bottom)

Table 2. Parameters of the ring oscillator for different temperatures

Temperature [°C]	Tuning range [GHz]	Relative tuning range [%]
10	2.286	80.21
20	2.231	79.56
30	2.178	78.94
40	2.127	78.28
50	2.078	77.68
60	2.030	77.04
70	1.984	76.43
80	1.940	75.84

Another important feature is relation between power consumption of the generator and temperature. It is crucial because too high power dissipated in the circuit can cause self-heating and further changes in circuit behavior. Fig. 7 presents gathered maximum power dissipated in the circuit in dependence of control voltage for different temperatures. Presented values are maximum ones, which can be observed only in short moments of changing the inverters state. Shape of the figure is tightly connected to tuning characteristic. Faster work of the circuit means higher power consumption.

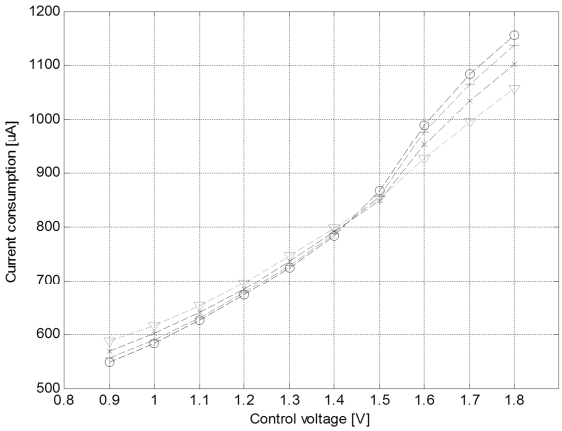


Fig. 7. Dependence of total power consumption with control voltage change of the ring oscillator for different temperatures (10ºC - top; 25ºC; 50ºC; 90ºC - bottom)

Because of power consumption minimization usage of circuit other than inverter in ring oscillator structure is possible [2]. For this reason five stage ring oscillator based on CMOS XNOR gates was implemented in UMC 0.18 □m technology. Schematic of such gate is presented in Fig. 8. When one of input of the XNOR gate is connected to the ground the circuit behaves like an inverter but without having direct path between supply and ground which results with power consumption decrease.

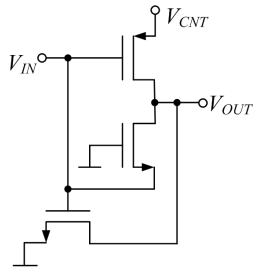


Fig. 8. Schematic diagram of the CMOS XNOR gate

The circuit Works very similar to previous one. Temperature change of tuning characteristic, presented in Fig. 9, is also not monotone – generated frequency is falling with temperature growth at higher control voltages and increasing with lower control voltages. The thermally stable point of the characteristic is about 0.9 V and 585 MHz. This dependence is clearly seen in Fig. 10. Tuning range is slightly smaller than in inverter-based structure and getting narrower for higher temperatures but still much larger than in resonant structure. Values of tuning ranges for different temperatures for XNOR ring oscillator are gathered in Table 3.

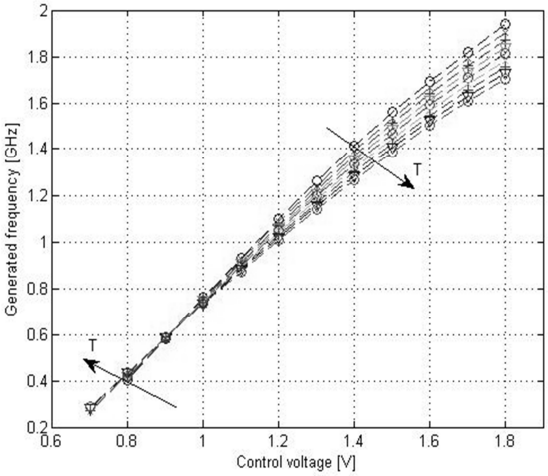


Fig. 9. Tuning characteristics of the XNOR ring oscillator for different emperatures

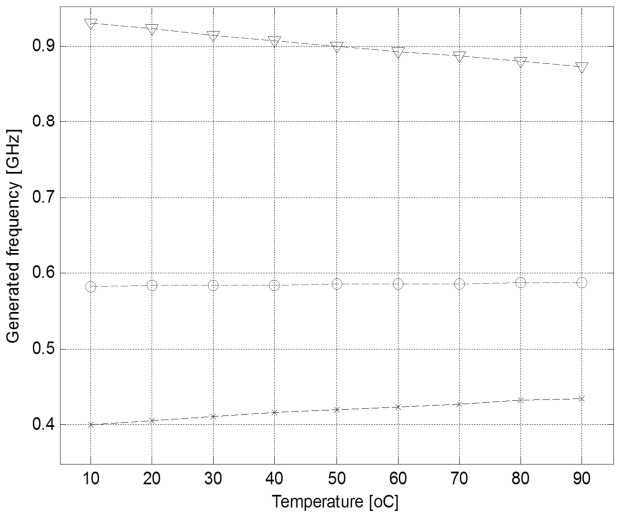


Fig. 10. Temperature dependence of frequency generated by the XNOR ring oscillator for constant tuning voltage (1.1 V - top; 0.9 V - middle; 0.8 V - bottom)

Table 3. Parameters of the XNOR ring oscillator for different temperatures

Temperature [°C]	Tuning range [GHz]	Relative tuning range [%]
10	1.536	79.30
20	1.498	78.68
30	1.462	78.06
40	1.426	77.42
50	1.393	76.83
60	1.360	76.23
70	1.329	75.64
80	1.298	75.03
90	1.269	74.47

Shape of the XNOR ring oscillator current consumption characteristic, Fig. 11, is similar to inverter-based case. The difference is that while using XNOR gates the circuit is less power-hungry which means smaller heat dissipation and less problems with self-heating of the structure. For this reason usage of presented structure is favorable choice.

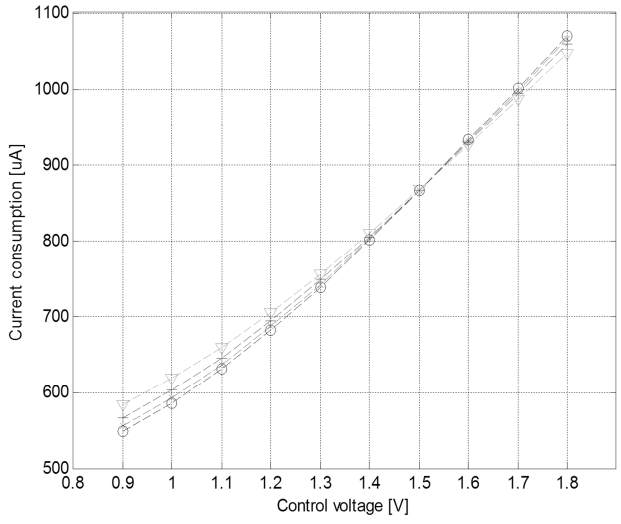


Fig. 11. Dependence of total power consumption with control voltage change of the XNOR ring oscillator for different temperatures (10ºC - top; 25ºC; 50ºC; 90ºC -bottom)

3. Summary

The paper presented thermal analysis of three different CMOS voltage-controlled oscillators. Resonant cross-coupled structure was designed and fabricated in AMS 0.35 µm technology. Frequency generated by this circuit is approximately linearly decreasing with temperature growth. The tuning range of LC oscillator is slightly narrower for higher temperatures. Two ring oscillator structures (inverter- and XNOR-based) were designed in UMC 0.18 µm technology. Thermal response of this structure is not monotone. For higher control voltages the generated frequency is decreasing while for lower control voltages is increasing with temperature growth. There is a single point on the tuning characteristic which is thermally independent. Tuning range of ring oscillators is getting narrower for higher temperatures but is a very large in comparison to resonant structure. Because of power consumption aspect the XNOR-based structure seems reasonable choice in comparison to inverter-based one.

Presented results will be used in authors work including design of dynamic power management systems using voltage-controlled oscillators. Obviously, the precise values of parameters would differ for each new design but the principles and direction of characteristics change should stay the same. As a result the presented measurements can be good reference for future works.

Acknolegements

The work was supported by the National Science Center (Narodowe Centrum Nauki), research project NCN N N515 500340.

Literature

[1] Frankiewicz M., Gołda A., Kos A.: *Design of CMOS Analog and Digital Phase-Locked Loops Based on Resonant VCO*. Proceedings of the 17th International Conference Mixed Design of Integrated Circuits and Systems MIXDES'2010, pp. 247-250

[2] Kumar M., Arya S.K., Pandey S.: *Voltage Controlled Ring Oscillator Design with Novel 3 Transistors XNOR/XOR Gates*. Circuits and Systems 2/2011, pp. 190-195

[3] Moon Y.-J., Roh Y.-S., Jeong C.-Y., Yoo C.: *A 4.39-5.26 GHz LC-Tank CMOS Voltage-Controlled Oscillator with Small VCO-Gain Variation*. IEEE Microwave and Wireless Components Letters, Vol. 19 No. 8, 2009, pp. 524-526

[4] Mroszczyk P., Gołda A., Kos A.: *Niskomocowy generator pierścieniowy CMOS sterowany napięciem*. Materiały IX Krajowej Konferencji Elektroniki KKE'2010, str. 114-119

[5] Sapatnekar S.S.: *Temperature as a First-Class Citizen in Chip Design*. Proceedings of the 15th International Workshop on Integrated Circuits and Systems THERMINIC'2009, pp. 1

[6] Zihir S., Tasdemir F., Dinc T., Gurbuz Y.: *A New Resonant Circuit for 2.45 GHz LC VCO with Linear Frequency Tuning*. Proceedings of the 6th European Microwave Integrated Circuits Conference EuMIC'2011, pp. 390-393

M. Sc. Maciej Frankiewicz
e-mail: frankiew@agh.edu.pl

Received MSc in electronics at AGH University of Science and Technology in Cracow, Poland in 2010. Currently PhD student at Department of Electronics, AGH University of Science and Technology in Cracow, Poland. Author of over 10 papers published in journals and international conferences proceedings. Area of interest includes temperature-aware designing of integrated circuits and systems.

Prof. Andrzej Kos
e-mail: kos@agh.edu.pl

Received PhD in 1983 at AGH University of Science and Technology in Cracow, Poland in electronics, professor title since 2001. Since 1995 head of the Micro- and Nanoelectronics Systems Team in Department of Electronics, AGH University of Science and Technology. Author of over 190 articles, international conference papers and patents, author of 3 books including one printed in United Kingdom. Scientific interests focus on thermal issues in integrated circuits design and testing. Member of the Committee of Electronics and Telecommunication of Polish Academy of Sciences, many scientific committees. European Commission and Polish Ministry of Science and Higher Education expert.

Exhibit “E”

Low power, temperature and process compensated CMOS ring oscillator

Mihai Eugen MARIN, Răzvan Cristian MARIN
Universitatea "Politehnica" Bucureşti. Splaiul Independenţei 313 Bucharest, Romania;
mihai.marin@ieee.org

Abstract. The modern communication technologies require the use of CMOS monolithic oscillators because of their small manufacturing costs and high integration capabilities. The disadvantages of CMOS ring oscillators can be compensated through the use of a VCO architecture. The control voltage of this VCO should compensate for the frequency drift due to process and temperature.

1 Introduction

Although the more common quartz crystal oscillators is still preferred because of the stability with variations in supply voltage, temperature and process recent advances in the compensation techniques transform the integrated CMOS ring oscillator into a suitable replacement. Without any compensation scheme the central frequency drift of the CMOS oscillator can be up to 100% when the temperature is varied. The process corners also influence the central frequency of an oscillator. Process corners are determined by variations in oxide thickness, threshold voltage and deviations of the physical dimensions of the transistor (dW and dL). In this paper an on-chip ring oscillator is considered. The compensation can be done through the use of a simple microcontroller that has a DAC an ADC and a temperature sensor. The digital part of the voltage generation is simulated in the Cadence environment using a Verilog model for the control voltage generator. This voltage generator accounts not only for the Fast n-channel, Fast p-channel (FF) and Slow n-channel, Slow p-channel (SS) corners but also for the Fast n-channel, Slow p-channel (FS) and Slow n-channel, Fast p-channel (SF)

2 The Ring Oscillator

The ring oscillator considered has 4 differential delay cells; the first 3 cells are in a inverting connexion and the fourth is connected as a buffer. Using this connexion scheme (Fig1) 4 signals with 0°, 90°, 180°, 270° phase shift are generated.

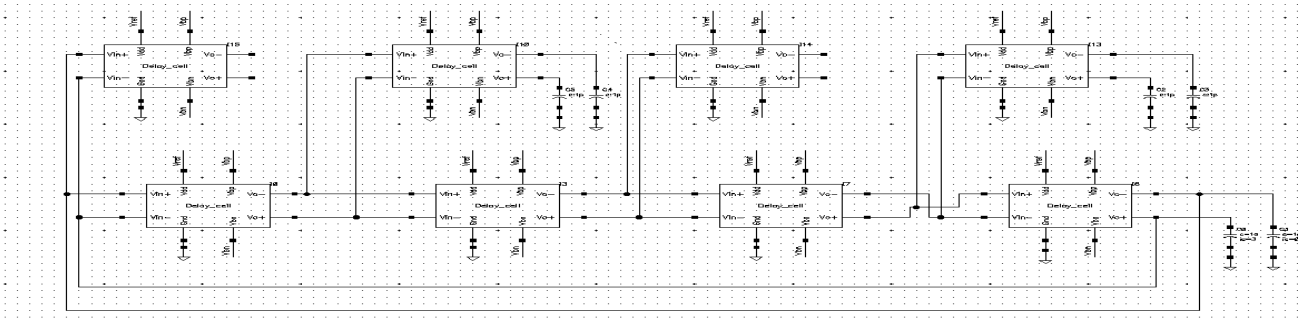


Figure 1: Oscillator core.

The differential delay cell is based on the delay cell proposed by Maneatis [1] and [2], (Fig. 2). The biasing of the circuit is done using a half buffer replica boosted dynamic bias (Fig 3) in order to reduce the supply noise [3]. Two half buffer circuits are used in order to isolate the control voltage input from the gate of the PMOS transistors in the oscillator.

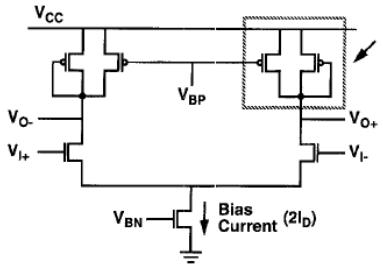


Figure 2: Delay cell [1].

Between the bias points of the PMOS and NMOS a bypass capacitor is introduced in order to prevent oscillations.

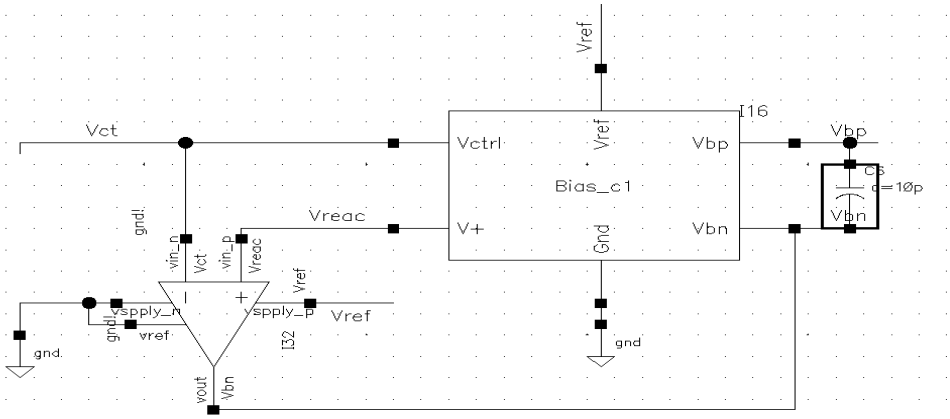


Figure 3: Bias circuit.

The output frequency of the ring oscillator is approximately represented in (1)

$$F = \frac{I_d}{2NC_oV_{SW}} = \frac{k_p\frac{W_p}{L_p}(V_{ref} - V_{Tp} - V_{ctrl})^2}{2NC_o(V_{ref-}V_{ctrl})} \tag{1}$$

3 Compensation of the ring oscillator

We want to see what happens when a temperature variation occurs. From the Bsim3.3V model [4] the threshold voltage has a linear variation with the temperature

$$V_{Tp} = V_{Tp0} + kt\left(\frac{T}{T_0} - 1\right) \tag{2}$$

where kt has a negative value.

The electron mobility also varies with the temperature

$$\mu(T) = \mu_0\left(\frac{T}{T_0}\right)^n \tag{3}$$

Considering C_{OX} temperature variation the same as for the output capacitance, then:

$$F = \frac{\mu_{p0} T_0^{\,n}\, C_{OX} \frac{W_p}{L_p} \left(V_{ref} - V_{Tp0} - V_{ctrl} + kt - kt\frac{T}{T_0}\right)^2}{2NC_O\left(V_{ref} - V_{ctrl}\right)T^n} \tag{4}$$

In Fig 4 the schematic of the corner detector is presented. The output voltage of this detector varies with temperature and process. An NMOS threshold detector architecture is preferred to the PMOS architecture presented in [5] and [6] because the generated values are unique.

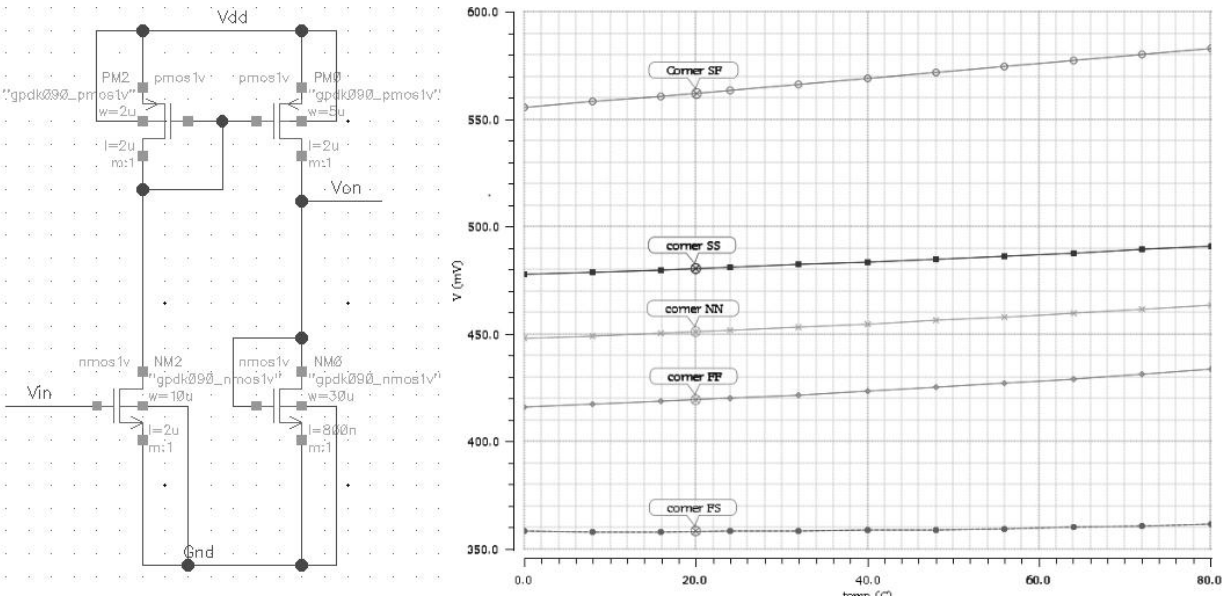


Figure 4: Process corner detector and output voltage.

Using this detector the corner is detected and the appropriate slope for the voltage can be generated.

4 Results

The oscillator was designed using the 90nm GPDK in Cadence. The supply voltage was set at 2.2V and the central frequency of the oscillator is 1GHz, Fig 5. The circuit draws a current of about 10mA so the power consumption without the control circuit of the circuit is about 22mW which qualifies the circuit as low power. In order to compensate the frequency across temperature and process the control voltage must take values between 0.7V and 1.5V. Using a resolution of 10mV a compensation of ± 3% is obtained over corners and a temperature variation of 0°-80°. This can be obtained using a 8-Bit DAC.

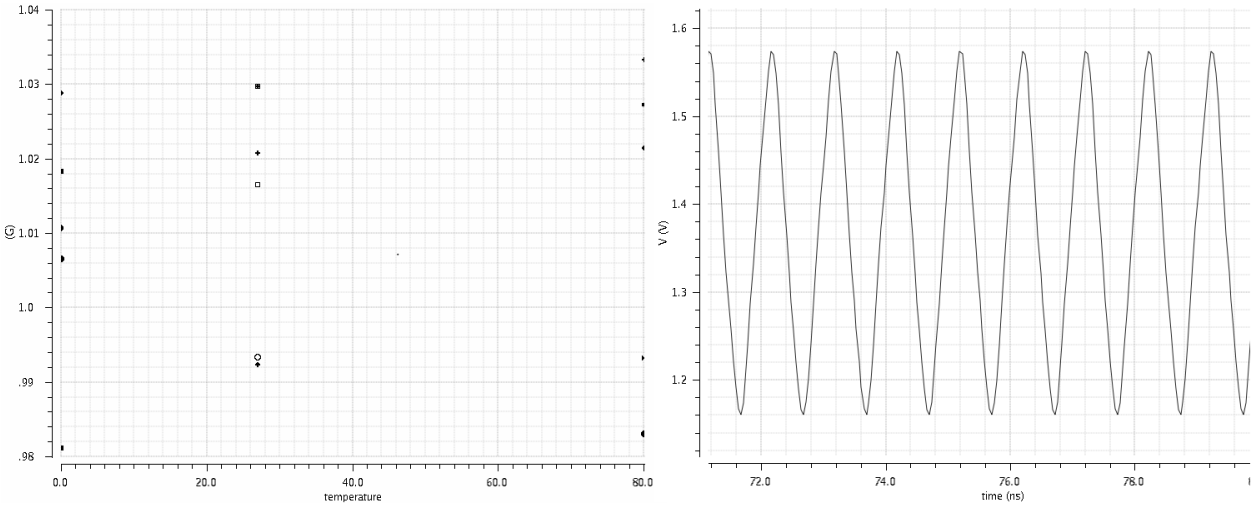


Figure 5: Oscillator frequency vs. temperature and output voltage at 25°C.

5 Conclusions

- In this paper a digital technique for the compensation of a ring oscillator is proposed
- A Verilog model is used in order to simulate the digital part of the circuit
- The proposed solution does not require calibration because the circuit generates the correct control voltage based on the output voltage of the threshold detector and the temperature reading.
- A variation of ± 3% is obtained over the temperature range of 0°-80° and the 4 corners.

References

[1] J.G Maneatis. Low-jitter process-independent DLL and PLL based on self-biased techniques, *IEEE Journal of Solid-State Circuits*, vol.31, no.11, pp.1723-1732, Nov 1996.

[2] J.G. Maneatis, M.A. Horowitz. Precise delay generation using coupled oscillators *IEEE Journal of Solid-State Circuits*, vol.28, no.12, pp.1273-1282, Dec 1993.

[3] J. Carnes, I.Vytyaz, P.K. Hanumolu, K. Mayaram, Un-Ku Moon. Design and Analysis of Noise Tolerant Ring Oscillators Using Maneatis Delay Cells, *14th IEEE International Conference on Electronics, Circuits and Systems, ICECS 2007*, vol., no., pp.494-497, 11-14 Dec. 2007.

[4] W. Liu, X. Jin, X. Xi, J. Chen, M.-C. Jeng, Z. Liu, Y. Cheng, K. Cn, M. Chan, K. Hui, J. Huang, R. Tu, P. K. Ko, C. Hu, Manual BSIM3v3.3 MOSFET Model Users, Department of Electrical Engineering and Computer Sciences University of California, Berkeley, CA 94720, 2005.

[5] J. Tang; F. Tang; , Temperature and process independent ring-oscillator using compact compensation technic, *2010 International Conference on Anti-Counterfeiting Security and Identification in Communication (ASID)* , vol., no., pp.49-52, 18-20 July 2010.

[6] K. Sundaresan, P. E. Allen, Process and temperature compensation in a 7-MHz CMOS clock oscillator, IEEE JSSC, Vol. 41, NO. 2, pp. 433-442, Feb. 2006.

Exhibit “F”

Just Enough is More: Achieving Sustainable Performance in Mobile Devices under Thermal Limitations

Onur Sahin, Paul Thomas Varghese, Ayse K. Coskun
Electrical and Computer Engineering Department, Boston University, Boston, MA, USA
{sahin, vpaul, acoskun}@bu.edu

***Abstract*—With the integration of high-performance multicore processors and multiple accelerators into modern mobile system-on-chips (SoCs), power densities have grown substantially. As a result, thermal management policies, which ensure operation at thermally safe conditions, became essential components of state-of-the-art mobile systems. Traditional thermal throttling approaches aim at maximum utilization of the available thermal headroom to minimize the performance loss and maximize user performance. This paper demonstrates that, in a mobile platform, such greedy techniques can lead to significant degradation in the quality-of-service (QoS) levels as the duration of device activity increases, leading to inconsistent user experience over time. We demonstrate that incorporating user/application QoS requirements into mobile power management to provide "just enough" performance (instead of always maximizing performance) allows for more efficient usage of the thermal headroom, which translates to substantially extended durations of sustainable performance. We propose a closed-loop QoS control policy, including an efficient dynamic voltage and frequency scaling (DVFS) state scheduling technique, to minimize the thermal impact for extending the *sustainability of desired QoS levels*. Experiments on a modern smartphone show that the proposed technique provides up to 74% longer sustainable performance while meeting the target QoS demands for a variety of real-life applications.**

I. Introduction

Mobile devices have been growing in popularity and have become essential parts of our daily lives. Growing user demand for faster processing and enhanced visual quality have been fulfilled by the increased computational capabilities of state-of-the-art mobile devices. Modern mobile system-on-chips (SoCs) have grown in complexity and processing power by integrating high-performance multicore processors and various accelerators (Graphics Processing Unit, Digital Signal Processor, etc.), resulting in excessive power densities. Higher power densities lead to elevated temperatures, which downgrade device reliability [2] and energy efficiency due to increased leakage power [17]. Incorporating multiple heat generating components such as battery, display and CPU into a small form-factor device with limited cooling makes maintaining safe chip temperatures even more challenging. Thus, modern mobile systems adopt CPU throttling techniques that adaptively reduce the operating frequency of the mobile processor to mitigate thermal emergencies. Thermal throttling, however, incurs performance drops and may impair user satisfaction in mobile systems where a satisfactory QoS level should be delivered to the user.

Existing power and thermal management techniques in mobile devices greedily exhaust the available thermal headroom to improve performance in case of increased computational demand. Although this approach works well for improving the QoS in relatively short applications, rapidly elevated temperatures can significantly increase the performance impact of throttling as the durations of the mobile device (phone, tablet, etc.) activity get longer. More aggressive thermal throttling induces larger performance degradations and leads to inconsistent performance levels during the application run. While current power management techniques in mobile devices favor short term performance, mobile system users also demand consistent performance for the applications that run for minutes or longer (i.e., consistent frame rate in gaming/video streaming [21] or webpage rendering time in browsing [30]). In fact, users have already reported significant performance drops in new generation high performance smarphones during extended durations of use [4][14]. Therefore, power management solutions in mobile devices need to address *performance sustainability*, as opposed to traditional short term performance oriented design, in face of the growing thermal limitations.

This paper addresses the problem of providing the user with sustainable performance levels over extended durations of mobile system use. We present real-life experiments to demonstrate the impact of thermal limitations on achieving performance sustainability using a modern smartphone platform. We observe that the available thermal headroom could be utilized more efficiently for longer durations by restricting the short term performance to a level that is "just enough" to meet the user's QoS demand. Based on this observation, we propose a novel QoS tuning technique that takes the target QoS goal as the primary performance constraint and attempts to sustain this target for the maximum duration by efficiently tuning the processor power level.

Our work makes the following specific contributions:

- We demonstrate the potential behind trading off short term performance in mobile devices for minimizing heat generation and achieving extended durations of sustainable performance.
- We propose a closed-loop QoS control policy integrated with an efficient DVFS state scheduler that achieves fine-grained CPU power control for meeting a wide range of possible QoS targets with minimal thermal impact.

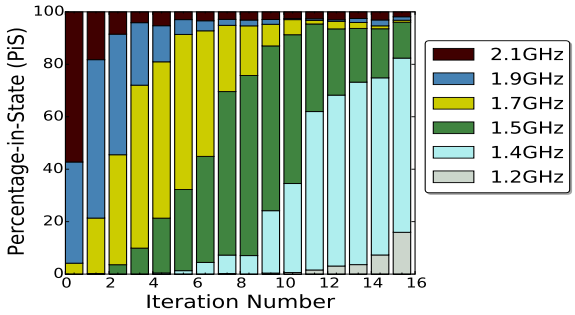


Fig. 1: Frequency residencies over time on a MDP8974 smartphone during continuous use. Performance impact of throttling increases over time as the CPU is forced to use lower frequencies to meet the thermal constraints.

- We evaluate our approach under both processor and skin temperature constraints using a variety of real-life applications with different QoS metrics. Our experiments on a modern smartphone show up to 74% longer durations of sustainable performance using the proposed technique.

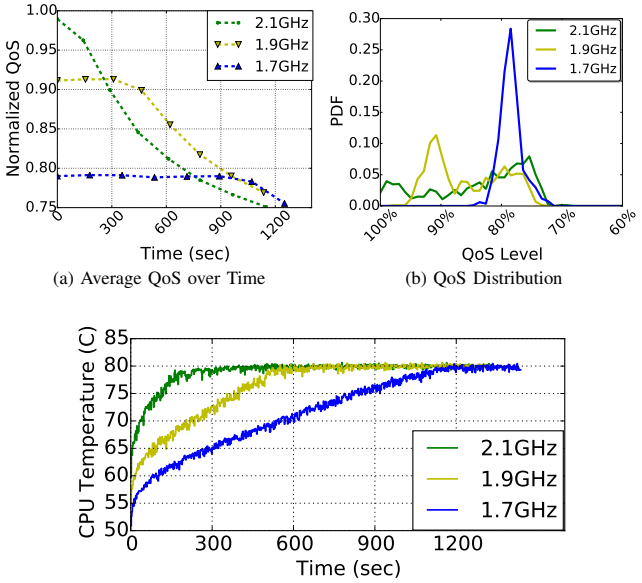
The rest of this paper starts by motivating the need for QoS-awareness in mobile thermal management to improve performance sustainability. Section III provides an overview and also the design details of our QoS tuning framework. Section IV presents the experimental methodology and integration on a real smartphone platform. Section V evaluates our technique. Section VI discusses the related work and Section VII concludes the paper.

II. Motivation

To exemplify the impact of extended application durations on sustained performance, Figure 1 shows the frequency residencies when the FFT application from Scimark Java benchmark suite [22] is repeatedly run on a Qualcomm Snapdragon MDP8974 smartphone [23]. The baseline CPU frequency scaling governor[1] scales the frequency to the highest level to boost performance and, initially (iterations 1-2), the application is able to operate below the thermal limit by throttling down to lower two frequencies only (1.9-1.7GHz). It should be noted that, in this example, frequencies lower than 2.1GHz level are enforced due to thermal throttling rather than by the power management scheme. In the later iterations, there is a clear shift towards utilizing lower frequencies due to more aggressive throttling applied by the baseline thermal management policy[1], which significantly reduces performance over time. For instance, in the last iteration, more than 80% of the running time is spent at 1.4GHz and 1.2GHz, while the application was well able to run without scaling down to those two frequencies initially. This example illustrates that *greedily utilizing the thermal headroom to boost short term performance can lead to significant performance loss over extended durations*.

We present another experimental scenario to point to the potential trade-off between the instant short term performance and sustainable performance. Figure 2 presents an experiment

[1]In the given experiment, default ondemand governor is used. The baseline thermal throttling policy is a PID controller with 80 °C thermal set-point that operate hierarchically with the ondemand governor.



(a) Average QoS over Time (b) QoS Distribution

(c) CPU Temperature Trace

Fig. 2: An illustration of the effect of trading off the short term performance on performance sustainability. The experiment corresponds to a repetitive run of bodytrack application [7] at 3 static frequency settings and QoS values are normalized to maximum QoS.

that corresponds to a repetitive run of the bodytrack application [7] at three different static frequency levels. Note that the system can still throttle the frequency below the assigned static level to avoid thermal violation. Figure 2a shows the average QoS for each iteration of the application over time. The maximum static frequency setting, 2.1GHz, gives the highest QoS initially. The QoS level, however, sharply reduces after the CPU reaches its thermal limits at around 220 seconds, as shown in Figure 2c. The QoS level continues to downgrade as a result of more aggressive thermal throttling and, at the end of the execution, QoS degrades to 25% of the initial maximum. The QoS drops below 90%[2] at around 300 seconds when using the aggressive 2.1GHz setting, while setting the frequency at 1.9GHz frequency allows to sustain the QoS level above 90% for 450 seconds. Figure 2b shows the QoS distribution for this experiment. The highest power setting results in wider distribution of the QoS while the 1.9GHz setting is able to rein the QoS distribution towards the 90% range (indicating longer duration of execution time spent around the 90% QoS). These results indicate that *lowering the short term performance requirements to "barely" meet the target QoS level, can enable longer sustainability of desired QoS goals*.

III. QoS Tuning Framework

In this section, we introduce our runtime framework and policies for efficiently tuning the QoS to "barely" match the target levels in the pursuit of achieving longer durations of sustainable performance. Figure 3 presents an overview of the framework that we have integrated into our platform. Our design comprises of three main components. The *closed-loop controller* takes the runtime tunable QoS level as a

[2]We choose 90% as an example acceptable QoS level to explain our motivation

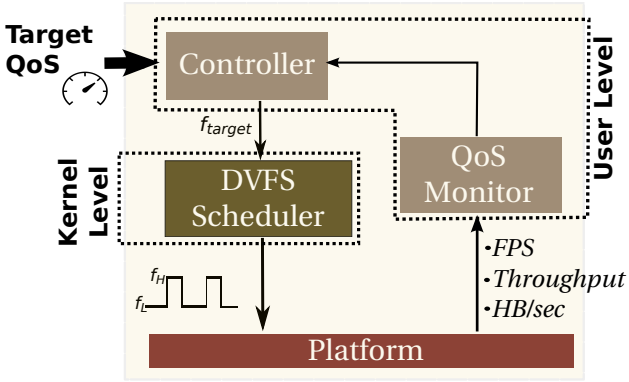


Fig. 3: Overview of the implementation framework. Frames per second (FPS), throughput and heartbeat per second (HB/sec) correspond to the QoS metrics for our applications that are listed in Section IV-B.

performance target and determines the operating frequency of the processor. The *DVFS scheduler unit* converts the continuous target frequency provided by the controller into a time-scheduled sequence of available discrete DVFS levels to efficiently match the continuous target frequency with minimal thermal impact. The *QoS monitoring unit* periodically monitors the frames-per-second (FPS), throughput, or heartbeats/second (HB/sec). We leave the discussion on platform integration of this framework to Section IV-C, and proceed with the implementation details of the controller and the DVFS scheduler in the following sections III-A and III-B, respectively.

A. Closed-loop QoS Controller

We design a feedback controller for dynamically adjusting the CPU speed to converge QoS towards desired levels. The controller tracks the progress of the application towards the target QoS by interacting with the *QoS Monitoring Unit* at every control interval. We use the following performance model, which represents the QoS level for the next time interval ($Q[k+1]$) as a fraction of the maximum achievable QoS (Q_{max}) at the highest frequency setting:

$$Q[k+1] = Q_{max}u[k] \tag{1}$$

$$e[k] = Q_{target} - Q[k] \tag{2}$$

The control signal $u[k]$ ranges between 0 to 1 and corresponds to the frequency scaling factor which determines the QoS level at time $k+1$. Since the goal of the controller is to minimize the difference between the target and current QoS levels, the error term $e[k]$ simply corresponds to this difference. The transfer function of the Equation 1 in the z-domain is given by:

$$F_1(z) = \frac{Q(z)}{U(z)} = \frac{Q_{max}}{z} \tag{3}$$

We find the transfer function $F_2(z)$ that defines the correspondence between the control signal and the error term by setting the following global transfer function of the closed-loop control system to $1/z$:

$$G(z) = \frac{F_1(z)F_2(z)}{1 + F_1(z)F_2(z)} \tag{4}$$

We obtain the discrete-time representation of the controller equation by substituting the $F_2(z)$ and taking the inverse z-transform as follows:

$$F_2(z) = \frac{U(z)}{E(z)} = \frac{z}{Q_{max}(z-1)} \tag{5}$$

$$u[k+1] = u[k] + e[k]/Q_{max} \tag{6}$$

We examine the stability and convergence of this control system by analyzing the global closed-loop transfer function $G(z)$ in z-domain. The closed-loop transfer function of $1/z$ has only one pole located at zero, which lies within the unit circle, ensuring the stabilization around the target QoS. Convergence to the target QoS level can be examined by evaluating the $G(z)$ at $z = 1$ and verifying a unit gain. Since $G(z) = 1/z$ evaluates to 1 at $z = 1$, the system has unit gain at the steady state and converges to the target QoS. The settling time of the controller is a function of the largest pole (a) of the closed-loop transfer function [12], approximated by $-4/log(a)$. Since the $G(z)$ has its single pole located at 0, the controller can converge instantly, limited by the controller invocation period in practice.

B. DVFS State Scheduler

The controller provides a continuous output signal while the CPU can only support discrete DVFS levels. We propose a DVFS state scheduler which divides the controller period into bins and switches between two neighbor frequency levels to produce an average frequency that matches the controller output. We also demonstrate the potential to minimize the thermal impact by making thermally-aware scheduling decisions to further extend the durations of sustainable performance.

Minimizing the Thermal Impact with Efficient DVFS Scheduling. We use the following discretized version of a lumped RC thermal model similar to prior research [25] to demonstrate the intuition behind our scheduling approach for minimizing the peak temperature of the CPU:

$$T[n+1] = T[n] + S(R_{th}P_k[n] - T[n])/R_{th}C_{th} \tag{7}$$

$$T[n+1] = c_1T[n] + c_2\hat{T}_k \tag{8}$$

where S is the sampling period, R_{th} and C_{th} are the thermal resistance and capacitance, $T[n]$ is the temperature at sampling interval n, $P_k[n]$ is the power level corresponding to DVFS state k, and $\hat{T}_k = R_{th}P_k[n]$ is the steady-state temperature for the power level P_k.

Consider the case where the scheduler estimates M bins to be scheduled with the higher frequency state in the following control interval, and those high frequency states are applied at distances of L. Next, we show that scheduler can reduce the peak temperature by increasing the distance L. Using Equation 8, we write the peak temperature at the end of the M^{th} high frequency state as follows:

$$T_p = c_1^{ML} T[0] + c_2 \sum_{i=0}^{M-1} c_1^{iL} \hat{T}_h + c_2 \sum_{i=0}^{(M-1)} \sum_{j=iL+1}^{(iL+L+1)} c_1^{j} \hat{T}_l \quad (9)$$

Since c_1 and c_2 are less than zero, when the distance between the high frequency states (L) is increased, the last term dominates and temperature approaches lower steady state temperature $\hat{T}_l$. Thus, distributing the high frequency states furthest from each other reduces the increase in temperature. Based on this intuitive observation, our scheduler implements maximum spatial distribution of the high frequency state bins within the control interval.

Impact of DVFS Granularity on Temperature. As a result of thermal time constants, temperature exhibits a "gradual" increase or decrease than a step thermal response. Thus, in addition to efficient DVFS scheduling, applying the DVFS state decisions faster, or increasing the number of switches within the interval, can also reduce maximum temperature due to the thermal buffer provided by the thermal time constants [9]. We exploit such benefits of the fast DVFS within the limitations of our experimental platform as pointed out in Section IV-C.

IV. Experimental Methodology

A. Target Platform

Our target experimental platform is a state-of-the-art Qualcomm Snapdragon MSM8974 smartphone [23] that hosts a Snapdragon 800 SoC (used in many modern smartphones, e.g., Nexus 5 and Galaxy S4). The Snadragon 800 SoC consists of a Quad Core Krait 400 CPU along with an Adreno 330 GPU, 2GB LPDDR3 RAM and is powered by a 1,600mAh Li-ion battery. The phone runs Android KitKat version 4.4.2 and Linux 3.4.0 kernel. The Krait 400 CPU supports 12 operating frequencies ranging from 300MHz to 2.1GHz. Temperature measurements can be done on a per-core basis via on-chip thermal sensors. Sensor readings for the CPU cores, battery and skin temperature are performed using the thermal virtual file system provided by the Linux kernel (i.e., /sys/class/thermal) with $\pm 1^{\circ}$C accuracy. We use the *logcat* system debugging tool available as part of the Android framework for monitoring the frames per second and use *perf_event* kernel API for accessing hardware performance counters. Our phone allows for measuring only the overall power consumption using the voltage and current sensors. For the CPU applications that do not require graphical interface, we turn-off the LCD display throughout the measurements. We leave the LCD display on for the GPU applications.

B. Application Set

Mobile systems run a broad range of applications and a single performance metric cannot gauge performance of all applications. Thus, we construct a benchmark set for our experiments by combining applications from various domains and evaluate them using different QoS metrics as summarized in Table I. The LU application, a common kernel in many image/video processing and mobile healthcare applications, is selected from Scimark 2.0 [22], which is a benchmark suite for testing Java based platforms. A video encoding (H.264) and an artificial intelligence application (Sjeng) are chosen from the SPEC CPU2006 [13]. We use two online graphics applications created with WebGL, Aquarium [1] and Pearl Boy [3]. The Aquarium shows an animation of fishes in a tank, while the Pearl Boy is an interactive application requires directing a boat in the sea. To ensure consistency between the runs, we automate the user interaction by applying the same sequence of *input swipe* commands for each experiment through a lightweight background shell program. We also use Heartbeats [15] instrumented version of the bodytrack computer vision application from the PARSEC suite [7]. Heartbeat framework allows to monitor application-specific QoS using a standardized interface and, for the bodytrack application, this framework emits a heartbeat whenever the processing of one scene is completed. Since the Heartbeats framework could be applied to a wider domain of applications for QoS monitoring and tuning purposes, we find value in demonstrating the applicability of our techniques on a representative Heartbeat-instrumented application.

Application	Category	QoS Metric
Sjeng	Artificial Intelligence	Throughput
H.264	Media Processing	Throughput
LU	Math	Throughput
Pearl Boy	Graphics/WebGL	Frames per second
Aquarium	Graphics/WebGL	Frames per second
Bodytrack	Computer Vision	Heartbeats/sec

TABLE I: Summary of applications and respective QoS evaluation metrics.

C. Baselines and Implementation Strategy

In this section, we provide the implementation details of our framework and summarize the baseline policies that we have used in our platform for comparisons against our policy.

Baseline Policies. The default CPU frequency scaling policy in our phone (and in most state-of-the-art Android devices) is the *ondemand governor* [20], which adjusts the CPU frequency based on the CPU load. Thus, we use the ondemand governor as our baseline power management scheme in our experiments.

Thermal throttling policies operate hierarchically with the CPU frequency governors and assign maximum frequency limits for ensuring operation below a thermal set-point. The CPU governors cannot use the frequencies that are above the assigned limit. Since the control-theoretic thermal management solutions are among the most commonly used techniques for maintaining the maximum temperature at a given threshold, we use a DVFS-based PID controller as the baseline CPU throttling mechanism. Modern smartphones also incorporate skin temperature management policies to keep the outer device temperature within the human comfort levels. Thus, performance degradations can occur due to increased skin temperatures as well. Since our MSM8974 device does not provide a skin temperature management policy by default, we implement the skin thermal management scheme available in the Nexus 5 smartphones. This policy assigns a maximum

		H264			Bodytrack			Sjeng			LU			
		ondemand & DTM	QT90	QT80	ondemand & DTM	QT90	QT80	ondemand & DTM	QT90	QT80	ondemand & DTM	QT90	QT80	QT70
Before Throttling	Average QoS	0.99	0.89	0.80	0.96	0.902	0.804	1.01	0.896	0.805	0.995	0.903	0.806	0.707
	Standard Deviation of QoS	0.035	0.042	0.037	0.02	0.028	0.043	0.086	0.059	0.065	0.107	0.109	0.075	0.074
Overall Execution	Average QoS	0.85	0.85	0.79	0.871	0.872	0.803	0.85	0.84	0.79	0.723	0.756	0.732	0.695
	QoS Degradation	27.2%	16.6%	**0.3%**	18.3%	11.3%	**0.1%**	28%	18%	4%	35%	30%	22%	7.4%
	Time Spent in Throttling	85.4%	55.5%	**6.8%**	59.4%	48.3%	**0%**	86.9%	61.7%	26.1%	87.7%	86.6%	73.9%	**45.4%**
	Average Power	0.99	0.97	0.88	0.92	0.97	0.86	0.99	0.96	0.89	0.97	1.02	0.97	0.91
	Energy Consumption	1.01	0.98	0.94	0.91	0.97	0.93	1.01	0.98	0.96	1.02	1.01	0.99	0.97
	QoS/Watt	0.99	1.02	1.05	1.09	1.04	1.08	0.99	1.013	1.03	0.997	0.994	1.006	1.03

TABLE II: A summary of results for the CPU applications. QT(X) represents proposed QoS tuning policy with X% target QoS. Average QoS, power, energy and QoS/Watt values are normalized to the highest static frequency setting (2.1GHz). QoS degradation corresponds to the percentage of QoS loss from the first to last iteration of the application run. Time spent in throttling results corresponds to the percentage of execution time thermal throttling is incurred.

Trip Point	Frequency Limit
40°C	1.9GHz
42°C	1.5GHz
44°C	1.2GHz

TABLE III: Temperature thresholds and target frequency limits of the baseline skin temperature controller.

CPU frequency limit whenever a skin temperature trip point is reached, as described in Table III. Both thermal throttling mechanisms poll the thermal sensors and assign frequency limits every 100ms to enable non-intrusive (less than %1 execution overhead) thermal management while maintaining sufficient time granularity to avoid thermal emergencies.

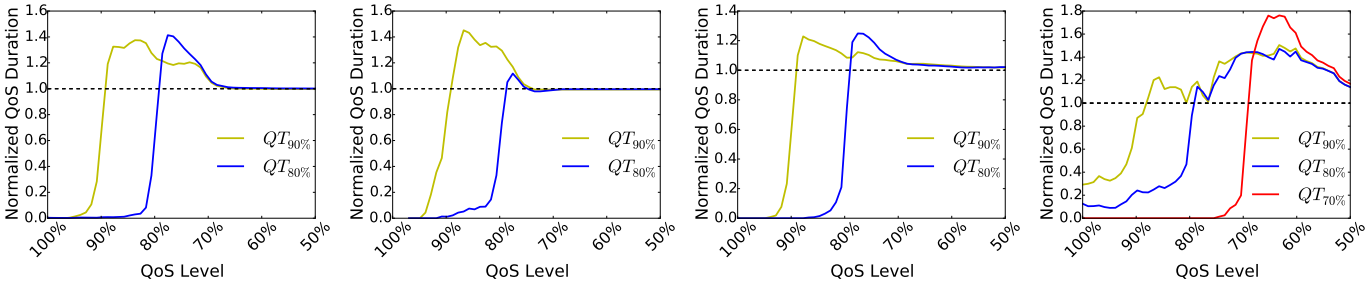
Implementation of the QoS Tuning Framework. We implement the closed-loop controller as a user-level program that regularly monitors the QoS level and passes the target frequency to the kernel-level DVFS scheduler. The controller is invoked every 200ms for the CPU applications and every 1 second for the GPU applications. We have observed noise in the FPS values when sampling at finer granularity. We implement our DVFS scheduler in the kernel-level as a new CPU governor with a *sysfs* interface to allow for assigning target frequency levels from the user space. The governor based implementation allows users to easily enable/disable our QoS tuning policy. The DVFS scheduler applies the frequency decisions at the granularity of 20 miliseconds via the *cpufreq* [8] interface. We have measured the frequency transition latency in our system to be 186.4 microseconds by wrapping the *cpufreq_driver_target* call in our kernel module with timing utilities. We have found 20 miliseconds to be the finest DVFS granularity that could be applied without introducing noticeable overhead (<1%) in our system. The maximum performance overhead of our framework is less than 1.3% across all the applications in our benchmark set.

V. Results & Evaluation

In this section, we present a thorough evaluation of the QoS tuning policy that we have proposed in this paper and demonstrate the benefits of our approach for achieving longer durations of sustained performance. We evaluate the CPU applications with the CPU temperature triggered dynamic thermal management policy (DTM_{cpu}), which is the PID controller based throttling scheme described in Section IV-C. For the graphics applications, we have observed that CPU temperatures did not reach to critical limits while the skin temperatures kept increasing over time. Thus, we also provide an evaluation of our QoS tuning policy with the skin temperature controller (DTM_{skin}) running as the throttling mechanism on our platform. We aim to show the benefits of our QoS tuning approach from the performance sustainability perspective under both processor and device-level skin temperature constraints.

Extended Sustainability with QoS Tuning on CPU applications. For the CPU applications, we explore three target QoS levels which are set to 90%, 80% and 70% of the average QoS achieved when the application is run at the highest static frequency setting on an initially cold system. For clarity, we do not present results for the 70% cases if the application QoS does not degrade to this level using the highest static frequency setting. We emulate extended application durations by repetitively running the applications for a fixed number of iterations. We determine the number of iterations based on a maximum battery temperature limit of 50 °C.

Table II gives a detailed overview of our experimental results where QT(X) corresponds to the proposed QoS tuning technique at the target QoS level of X%. All the values except for the QoS degradation and the time spent in throttling are normalized to the highest static frequency setting. We evaluate the phases of the execution without throttling (indicated by "before throttling" in Table II) separately to examine the controller's ability to meet QoS goals without the interference of the throttling policy. Overall, our controller is able to effectively meet the given QoS targets with less than 0.06 average deviation. In most cases, average QoS of the overall execution is lower than the "before throttling" phase due to the performance impact of the throttling. However, bodytrack and h264 applications are able to sustain the performance close to 80% QoS level throughout the whole execution as little or no thermal throttling is incurred at that level for these two applications. The highest QoS degradation is observed for the LU application, which spends 45% of time in throttling even in the lowest QoS target of 70%. This degradation is due to the power hungry nature of this CPU intensive computing kernel that quickly reaches the CPU thermal limits. For all benchmarks, the baseline *ondemand* policy continuously seeks



(a) H264 (b) Bodytrack (c) Sjeng (d) LU

Fig. 4: Normalized duration of time spent above a QoS level by the proposed QoS tuning policy for different target QoS level. "$QT_{X\%}$" represents the proposed QoS tuning policy with X% QoS goal. A data point in the figure corresponds to (Time spent above a QoS with QT)/(Time spent above a QoS with (DTM_{cpu}+ondemand).

to convert the thermal headroom into performance by scaling the frequency to high levels and incurs the highest QoS degradation due to the increased percentage of time spent in throttling. The QoS tuning policy with 90% target level achieves 38.6% reduction in throttling duration on average and consistently provides lower QoS degradation for all benchmarks. The QoS tuning also provides up to 14% and 7% reductions in power and energy, respectively.

Figure 4 presents the improvements in performance sustainability for our CPU applications. The figure shows the duration of time spent above a QoS level with the proposed QoS tuning (QT) policy as normalized to the baseline. The proposed technique provides substantially longer execution time around the given QoS target. This could be observed in Figure 4a,4b and 4c where the the curves start to rise significantly above the dashed line (normalized baseline) when approaching the the given QoS goals. For the h264, bodytrack and sjeng applcations, an average of 37% and 26.7% longer sustainability is achieved for the 90% and 80% QoS levels, respectively. Improvement by the QoS tuning on the bodytrack application for the 80% QoS level is lower (11%) as the QoS drops to 80% range for only a short duration of time with the baseline policy. The LU application, as shown in Figure 4d, provides the peak improvements in sustainability with 74% longer duration the 70% QoS target is sustained. This application has the highest power consumption among our applications and quickly reaches to thermal limits with the baseline setting. Therefore, using higher frequency settings results in higher QoS degradation for this application. In fact, the proposed policy is also unable to sustain the QoS around the target range for the higher 90% and 80% target levels and QoS distribution shifts towards a lower range.

Fine-grained QoS Control with DVFS scheduler. The DVFS state scheduler converts the continuous frequency targets into a time-scheduled distribution of two discrete frequency states that are neighbours of the continuous target frequency. This scheme enables fine-grained tuning of the QoS for accurately matching to the target levels. Figure 5 compares the proposed combined QoS controller and DVFS scheduler technique against two performance aware static frequency settings, 1.9GHz and 1.5GHz. We refer to such static frequency selection as performance aware since those two frequencies provide the nearest average QoS to 90% and 80% levels, respectively. Using the static frequency settings fails to precisely meet the target QoS goals. For instance, in Figure 5, 1.9GHz setting provides higher QoS than 90% goal while 1.5GHz setting provides 5% lower QoS than the target 80% level. Besides, since the static 1.9GHz setting provides higher QoS than the target level and consumes extra power for this offset, the QoS drops below the 90% level prior to proposed fine-grained QoS tuning technique due to earlier invocation of thermal throttling.

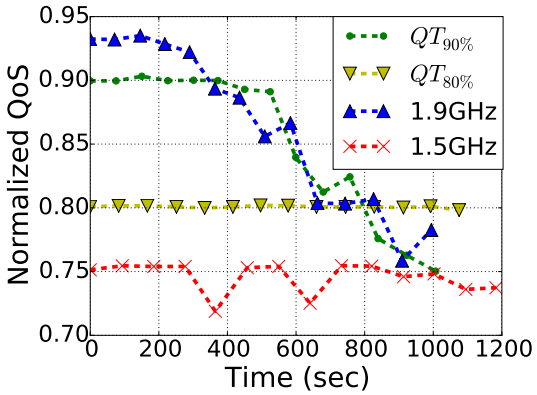


Fig. 5: Average QoS per iteration over time for the H264 application with the proposed QoS tuning and performance aware static frequency selection policy.

The DVFS state scheduler also aims to achieve the maximum spatial distribution of the higher frequency states to minimize thermal impact. Figure 6 shows the effect of such distributed scheme on the temperature trace of the h264 application. Undistributed scheme simply switches from low frequency state to high frequency state only once during the control period while the distributed policy applies finer granularity switching with maximum possible low frequency periods between the high frequency states, both providing the same average frequency. As annotated by the two arrows in Figure 6, the distributed policy allows for longer execution without reaching to the thermal limit.

Dynamic Adaptation to Changes in QoS Requirements. The target QoS requirements for an application could change during runtime for various reasons (upon user request, remaining battery level etc). Therefore, a good control policy should

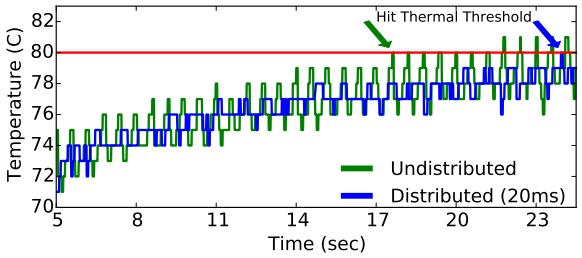


Fig. 6: Temperature traces for two DVFS scheduling schemes. Undistributed scheme simply switches from lower to higher frequency only once during the control interval (1 sec). Distributed scheme gains more thermal headroom by applying fine grain DVFS and scheduling high states farthest possible from each other. The duty-cycle is 33% high.

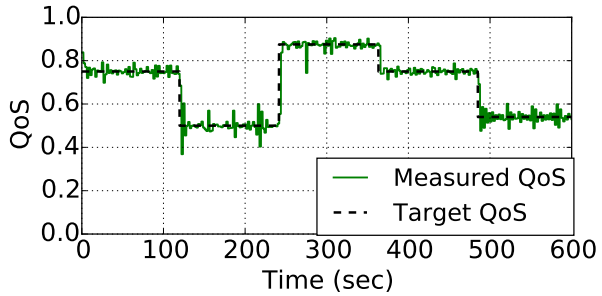
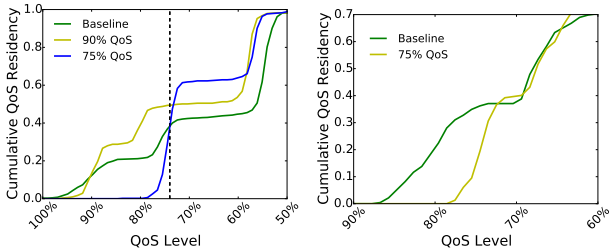


Fig. 7: QoS trace for the Aquarium WebGL application as the policy adapts to QoS requirements during runtime. The values are normalized to the maximum achievable FPS and QoS targets are arbitrarily modulated every 2 minutes.

respond to such changes in the performance requirements. In order to exercise our proposed framework with dynamically changing QoS goals, we design an experiment where the target QoS is arbitrarily modulated every two minutes during a 10 minute run of the aquarium graphics application. Figure 7 presents the QoS trace as the policy adapts to the changing target QoS levels. The closed-loop controller with DVFS scheduler enables fine-grained QoS tuning and is able to precisely meet the arbitrary QoS goals. We have measured the root mean square tracking error of our policy to be 0.088 in this experiment.

Performance Sustainability Under Skin Temperature Constraints. We further investigate the applicability of our motivation and QoS tuning technique under skin temperature constraints for extending the durations of target FPS levels using two graphics applications. Figure 8 shows the cumulative distribution of the QoS for both applications during a 15 minutes of continuous execution. 100% QoS corresponds to 40 FPS for the Aquarium application and 60 FPS for the Pearl Boy application. A data point corresponds to the fraction of the overall execution time spent above the corresponding QoS level. For the Pearl Boy application, QoS tuning with 75% target level improves the sustainability by 9%, from 36% to 40% of the execution time spent above the target. We do not show the 90% case as the baseline policy provides a QoS range below 88%. Figure 8a shows the cumulative QoS distribution for the Aquarium application and the dashed line corresponds to the 30 FPS limit which is pointed by prior research to be the lowest frame rate in the user tolerable range [21][29]. The QoS tuning policy with 75% target (30 FPS) increases the



(a) Aquarium (b) Pearl Boy

Fig. 8: Cumulative QoS distribution for the two WebGL graphics applications. Dashed line in the left figure shows the 30FPS limit. The baseline policy corresponds to ondemand+DTM$_{skin}$.

sustainability of this QoS level from 40% of the execution time to 62%, *providing 55% longer duration that the user can be provided with an acceptable FPS level.*

VI. Related Work

Thermal management of multicore CPUs and MPSoCs is a well studied subject for conventional computer systems. Control theoretic DVFS techniques provide effective temperature control while maximizing performance [6][25] and predictive techniques (e.g., [28]) have been applied to project thermal emergencies for minimizing temperature violations. There has been a recently growing effort towards thermal modeling and analysis of the mobile devices in particular. Xie et al. propose a resistance network based thermal simulation framework for obtaining component level steady-state temperatures [26] and derive an RC model of the thermal coupling between the battery and the application processor [27]. Singla et al. [24] present a temperature prediction and power budgeting methodology for heterogeneous mobile SoCs and show power savings compared to fan-based and reactive policies. ARM's new *Intelligent Power Allocation* [19] scheme aims to maximize performance under thermally limited scenarios by shifting the power between the heterogeneous CPU cores and GPU based on the expected performance return. Unlike the previous work, we do not attempt to improve performance under temperature constraints. Instead, we consider the target QoS levels as performance-wise sufficient and aim to sustain that QoS level for maximum duration.

Power management for meeting performance goals have been studied for various computing platforms. Ayoub et al. [16] propose a DVFS management technique for meeting throughput requirements in a server system. Lo et al. [18] present PEGASUS, which utilizes the Intel's *Running Average Power Limiter* for enabling fine-grained CPU power tuning in web clusters to match query latency requirements. Kadjo et al. [5] reduce the QoS requirements in memory bound applications and achieve platform level power savings in a mobile system. Pathania et al. [21] propose a CPU-GPU power budgeting algorithm to meet a frames-per-second constraint in mobile games. While the above techniques do not consider the sustainability of performance targets and thermal impacts, a recent study [11] points to the performance measurement flaws that occur due power level differences in the boosting

mode and the throttling mode in Intel's TurboBoost enabled processors. Other recent work [29] proposes to trade-off QoS within the user tolerable range for energy minimization in event-based mobile web applications while we present the case for trading off the QoS for thermal headroom to achieve longer sustainable performance.

Several studies addressed the scheduling of discrete DVFS states with thermal considerations in real-time systems domain. Applying faster switching between the discrete DVFS levels have been formally shown to maximize the workload under a thermal threshold [9] and minimize the peak temperature [10] in hard real-time systems. Inspired by those techniques in real-time systems domain, we utilize DVFS scheduling to enable fine-grained CPU power tuning and meet the target QoS constraints with minimal use of the thermal headroom for improved performance sustainability.

Overall, our work differs from the prior research by the following aspects: (1) we address performance (un)sustainability in mobile devices that arises due to thermal limitations; (2) we show the performance drawbacks of existing thermal management approach due to the pursuit of favoring short term performance; (3) we propose tuning the power management policies in mobile systems to match the target QoS demands for creating efficient usage of thermal headroom, enabling extended durations of sustainable performance; (4) we run all experiments on real-life systems.

VII. Conclusion

In this paper, we addressed the drawbacks of greedily exhausting the thermal headroom to boost short term performance in mobile devices that actively grow in power densities under limited cooling capabilities. Through experiments on a real-life platform, we demonstrated that existing thermal management approach leads to considerably lower performance as the duration of device activity increases, as a consequence of the increasing performance impact of thermal throttling. Diminishing performance imperils the user-experience in thermally limited modern mobile devices that must guarantee satisfactory quality-of-service (QoS) levels. In order to meet the user demand in the face of thermal limitations, we propose to trade-off performance for thermal headroom while meeting target QoS goals in a mobile system. We present a runtime framework with a closed-loop QoS controller and a DVFS state scheduler that enables fine-grained power tuning. Our results show that, utilizing the proposed framework for tuning the user performance to a "just enough" level to meet the minimum QoS requirement, allows for more efficient usage of the thermal headroom and extends the durations of sustained QoS levels by up to 74%.

References

[1] Aquarium. https://www.chromeexperiments.com/experiment/webgl-aquarium.

[2] Failure mechanisms and models for semiconductor devices, JEDEC publication JEP122C. http://www.jedec.org.

[3] Pearl Boy. https://www.chromeexperiments.com/experiment/pearl-boy.

[4] When benchmarks aren't enough: Cpu performance in the nexus 5. [online] http://arstechnica.com/gadgets/2013/11/when-benchmarks-arent-enough-cpu-performance-in-the-nexus-5.

[5] R. Z. Ayoub et al. Os-level power minimization under tight performance constraints in general purpose systems. In *Proceedings of the 17th IEEE/ACM International Symposium on Low-power Electronics and Design (ISLPED)*, 2011.

[6] A. Bartolini, M. Cacciari, A. Tilli, and L. Benini. A distributed and self-calibrating model-predictive controller for energy and thermal management of high-performance multicores. In *Design, Automation Test in Europe Conference Exhibition (DATE), 2011*, March 2011.

[7] C. Bienia, S. Kumar, J. P. Singh, and K. Li. The parsec benchmark suite: Characterization and architectural implications. In *Proceedings of the 17th International Conference on Parallel Architectures and Compilation Techniques (PACT)*. ACM, 2008.

[8] D. Brodowski. Linux kernel cpufreq subsystem. *URL http://www. kernel. org/pub/linux/utils/kernel/cpufreq/cpufreq. html*.

[9] T. Chantem, X. S. Hu, and R. P. Dick. Online work maximization under a peak temperature constraint. In *ISLPED*. ACM, 2009.

[10] V. Chaturvedi, H. Huang, and G. Quan. Leakage aware scheduling on maximum temperature minimization for periodic hard real-time systems. In *IEEE 10th International Conference on Computer and Information Technology (CIT)*, June 2010.

[11] L. Emurian et al. Pitfalls of accurately benchmarking thermally adaptive chips. *Power (W)*, 5:10, 2014.

[12] J. L. Hellerstein et al. *Feedback control of computing systems*. John Wiley & Sons, 2004.

[13] J. L. Henning. Spec cpu2006 benchmark descriptions. *ACM SIGARCH Computer Architecture News*, 34(4):1–17, 2006.

[14] J. Ho and A. Frumusanu. Revisiting SHIELD Tablet: Gaming Battery Life and Temperatures. [online] Available: http://www.anandtech.com/show/8329/revisiting-shield-tablet-gaming-ux-and-battery-life.

[15] H. Hoffmann et al. Application heartbeats: a generic interface for specifying program performance and goals in autonomous computing environments. In *Proceedings of the 7th international conference on Autonomic computing*, pages 79–88. ACM, 2010.

[16] D. Kadjo et al. Towards platform level power management in mobile systems. In *International System-on-Chip Conference (SOCC)*, 2014.

[17] N. S. Kim et al. Leakage current: Moore's law meets static power. *Computer*, 36(12), 2003.

[18] D. Lo, L. Cheng, R. Govindaraju, L. A. Barroso, and C. Kozyrakis. Towards energy proportionality for large-scale latency-critical workloads. In *Proceeding of the 41st Annual International Symposium on Computer Architecuture (ISCA)*, 2014.

[19] M. Muller. Power constraints: From sensors to servers. [online] http://www.hotchips.org/wp-content/uploads/hc_archives/hc26/HC26-11-day1-epub/HC26.11-1-Z-Keynote1-Power-epub/HC26.11.190-Keynote1-Power-Muller-ARM-MM-v8.pdf.

[20] V. Pallipadi and A. Starikovskiy. The ondemand governor. In *Proceedings of the Linux Symposium*, volume 2, pages 215–230, 2006.

[21] A. Pathania, Q. Jiao, A. Prakash, and T. Mitra. Integrated cpu-gpu power management for 3d mobile games. In *51st ACM/EDAC/IEEE Design Automation Conference (DAC)*, June 2014.

[22] R. Pozo and B. Miller. Scimark 2.0. *URL: http://math. nist. gov/scimark2*, 2000.

[23] Qualcomm Developer Network. [online] Snapdragon MSM8974 MDP. https://developer.qualcomm.com/snapdragon-mobile-development-platform-mdp, 2014.

[24] G. Singla et al. Predictive dynamic thermal and power management for heterogeneous mobile platforms. In *DATE*. IEEE, 2015.

[25] K. Skadron et al. Control-theoretic techniques and thermal-rc modeling for accurate and localized dynamic thermal management. In *Proceedings of the 8th International Symposium on High-Performance Computer Architecture (HPCA)*, Washington, DC, USA, 2002.

[26] Q. Xie, M. J. Dousti, and M. Pedram. Therminator: A thermal simulator for smartphones producing accurate chip and skin temperature maps. In *ISLPED*, 2014.

[27] Q. Xie et al. Dynamic thermal management in mobile devices considering the thermal coupling between battery and application processor. In *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 2013.

[28] I. Yeo, C. C. Liu, and E. J. Kim. Predictive dynamic thermal management for multicore systems. In *DAC*, 2008.

[29] Y. Zhu, M. Halpern, and V. J. Reddi. Event-based scheduling for energy-efficient qos (eqos) in mobile web applications. In *HPCA*, 2015.

[30] Y. Zhu and V. J. Reddi. High-performance and energy-efficient mobile web browsing on big/little systems. In *HPCA*, 2013.

Exhibit “G”

Fixed - definition of fixed by The Free Dictionary

fixed

Also found in: **Thesaurus**, **Medical**, **Legal**, **Financial**, **Acronyms**, **Idioms**, **Encyclopedia**, **Wikipedia**.
Related to fixed: **Fixed stars**, **fixed cost**

fixed (fĭkst)

adj.

1. Firmly in position; stationary: *a fixed dwelling.*
2. Determined; established; set: *at a fixed time; a fixed price.*
3. Not subject to change or variation; unchanging: *pensioners on a fixed income.*
4. *Chemistry*
   a. Not readily evaporating; nonvolatile.
   b. Being in a stable, combined form: *fixed nitrogen.*
5.
   a. Firmly, often dogmatically held: *fixed beliefs.*
   b. Persistently occurring in the mind; obsessive: *a fixed, delusive notion.*
6. Supplied, especially with funds. Often used in combination: *a well-fixed bachelor.*
7. Illegally prearranged as to outcome: *a fixed election.*

fix′ed·ly (fĭk′sĭd-lē) *adv.*

fix′ed·ness *n.*

fixed (fɪkst)

adj

1. attached or placed so as to be immovable
2. not subject to change; stable: *fixed prices*.
3. steadily directed: *a fixed expression*.
4. established as to relative position: *a fixed point*.
5. not fluctuating; always at the same time: *a fixed holiday*.
6. (of ideas, notions, etc) firmly maintained
7. (Chemistry) (of an element) held in chemical combination: *fixed nitrogen*.
8. (Chemistry) (of a substance) nonvolatile
9. arranged
10. (Astrology) *astrology* of, relating to, or belonging to the group consisting of the four signs of the zodiac Taurus, Leo, Scorpio, and Aquarius, which are associated with stability. Compare **cardinal**[9], **mutable**[2]
11. *informal* equipped or provided for, as with money, possessions, etc
12. *informal* illegally arranged: *a fixed trial*.

fixedly *adv*

ˈ**fixedness** *n*

fixed (fɪkst)

adj.

1. attached or placed so as to be firm and not readily movable; stationary; rigid.
2. rendered stable or permanent, as color.
3. set or intent upon something; steadily directed: *a fixed stare.*
4. definitely and permanently placed: *a fixed buoy.*
5. not fluctuating or varying; definite: *fixed income.*
6. supplied with or having enough of something necessary or wanted, as money.
7. coming each year on the same calendar date.
8. put in order.
9. arranged in advance privately or dishonestly: *a fixed race.*
10.
    a. (of a chemical element) taken into a compound from its free state.
    b. nonvolatile, or not easily volatilized: *a fixed oil.*

[1350–1400]

fix•ed•ly (ˈfɪk sɪd li, ˈfɪkst li) *adv.*

fix′ed•ness, *n.*

fixed

One of the three qualities; associated with stability, determination and consistency.

Thesaurus

Legend: 〓 Synonyms ↔ Related Words ≠ Antonyms

Switch to **new thesaurus**

Adj. 1. fixed - (of a number) having a fixed and unchanging value

↔ **determinate** - precisely determined or limited or defined; especially fixed by rule or by a specific and constant cause; "a determinate distance"; "a determinate number"; "determinate variations in animals"

2. **fixed** - fixed and unmoving; "with eyes set in a fixed glassy stare"; "his bearded face already has a set hollow look"- Connor Cruise O'Brien; "a face rigid with pain"

〓 **set**, **rigid**

↔ **nonmoving**, **unmoving** - not in motion

3. **fixed** - securely placed or fastened or set; "a fixed piece of wood"; "a fixed resistor"

↔ **secure** - not likely to fail or give way; "the lock was secure"; "a secure foundation"; "a secure hold on her wrist"

≠ **unfixed** - not firmly placed or set or fastened

4. **fixed** - incapable of being changed or moved or undone; e.g. "frozen prices"; "living on fixed incomes"

≡ **frozen**

↔ **unchangeable** - not changeable or subject to change; "a fixed and unchangeable part of the germ plasm"-Ashley Montagu; "the unchangeable seasons"; "one of the unchangeable facts of life"

fixed

adjective

1. ≡ **inflexible**, **set**, **steady**, **resolute**, **unwavering**, **unflinching**, **unblinking**, **unbending**, **undeviating** *people who have fixed ideas about things*

inflexible ≠ **varying**, **wavering**, **inconstant**

2. ≡ **immovable**, **set**, **established**, **secure**, **rooted**, **permanent**, **attached**, **anchored**, **rigid**, **made fast** *Nato was concentrating on hitting buildings and other fixed structures.*

immovable ≠ **moving**, **mobile**, **bending**, **pliant**, **motile**, **unfixed**

3. ≡ **false**, **fake**, **feigned**, **insincere** *I had a fixed grin on my face.*

4. ≡ **agreed**, **set**, **planned**, **decided**, **established**, **settled**, **arranged**, **resolved**, **specified**, **definite** *The deal was settled at a prearranged fixed price*

5. ≡ **mended**, **going**, **sorted**, **repaired**, **put right**, **in working order** *The vehicle was fixed.*

6. *(Informal)* ≡ **rigged**, **framed**, **put-up**, **manipulated**, **packed** *Some races are fixed.*

fixed *adjective*

1. Firmly in position:

≡ **immobile**, **immovable**, **stationary**, **steadfast**, **steady**, **unmovable**, **unmoving**.

2. Having distinct limits:

≡ **definite**, **determinate**, **limited**.

3. In a definite and final form; not likely to change:

≡ **certain**, **firm**, **flat**, **set**.

4. On an unwavering course of action:

≡ **bent**, **decided**, **determined**, **intent**, **resolute**, **set**.

Translations

Select a language: Spanish / Español

fijo **amañado** **arreglado** **seguro**

fixed [fɪkst]

A. *ADJ*

1. (= *permanent, invariable*) [*amount, number, rate*] → **fijo**

of no fixed abode or address (*Jur*) → sin **domicilio fijo**

2. (= *prearranged*) → **establecido**

at a fixed time → a una **hora establecida**

there's no fixed agenda → no hay un **orden del día fijo**

3. (= *immovable*) [*smile*] → **inamovible**; [*stare*] → **fijo**

she kept a fixed smile on her face → **mantuvo** una **sonrisa inamovible**

to keep one's eyes fixed on sth → **mantener** la **mirada fija** en algo

4. (= *inflexible*) [*opinion*] → **firme**, **rígido**

he has very fixed ideas → es de **ideas fijas**

B. *CPD* **fixed assets** *NPL* → **activo** *msing* **fijo**

fixed charge *N* → **cargo** *m* **fijo**

fixed costs *NPL* → **costos** *mpl* **fijos**

fixed price *N* → **precio** *m* **fijo**

fix (fiks) *verb*

1. to make firm or steady. *He fixed the post firmly in the ground; He fixed his eyes on the door.***fijar, clavar**

2. to attach; to join. *He fixed the shelf to the wall.***fijar, clavar**

3. to mend or repair. *He has succeeded in fixing my watch.***arreglar**

4. to direct (attention, a look *etc*) at. *She fixed all her attention on me.***fijar, clavar, poner**

5. (*often with* **up**) to arrange; to settle. *to fix a price; We fixed (up) a meeting.***fijar**

6. to make (something) permanent by the use of certain chemicals. *to fix a photgraphic print.***fijar**

7. to prepare; to get ready. *I'll fix dinner tonight.***arreglar, organizar**

noun

trouble; a difficulty. *I'm in a terrible fix!***apuro, aprieto**

fixˈation *noun*

a strong idea or opinion for or against something that one does not or cannot change. *She has a fixation about travelling alone.***fijación, obsesión**

fixed *adjective*

1. arranged in advance; settled. *a fixed price.***fijo**

2. steady; not moving. *a fixed gaze/stare.***fijo**

3. arranged illegally or dishonestly. *The result was fixed.***amañado**

fixedly (ˈfiksidli) *adverb*

steadily. *He stared fixedly.***fijamente**

fixture (ˈfikstʃə) *noun*

1. a fixed piece of furniture *etc*. *We can't move the cupboard – it's a built-in fixture.***instalación fija**

2. an event, *especially* sporting, arranged for a certain time. *The football team has a fixture on Saturday.***encuentro**

fix on

to decide on, choose. *Have you fixed on a date for the wedding?***decidir, fijar**

fix (someone) up with (something)

to provide (someone) with (something). *Can you fix me up with a car for tomorrow?***proveer, conseguir algo para alguien**

fixed → fijo

Multilingual Translator © HarperCollins Publishers 2009

fixed

a. fijo-a; decidido-a [*resolved*] resuelto; arreglado-a, determinado-a; compuesto-a;
___ **fee** → honorario ___ o definido;
___ **term** → plazo ___.

English-Spanish Medical Dictionary © Farlex 2012

fixed *adj* fijo

English-Spanish/Spanish-English Medical Dictionary Copyright © 2006 by The McGraw-Hill Companies, Inc. All rights reserved.

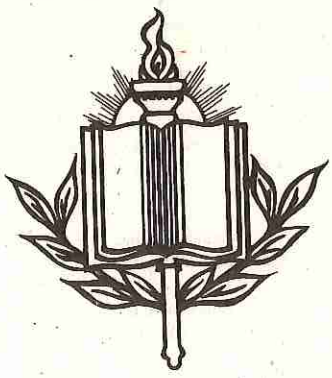
WEBSTER'S ENCYCLOPEDIC UNABRIDGED DICTIONARY OF THE ENGLISH LANGUAGE

- Over 300,000 entries based on the up-to-date Second Edition of *The Random House Dictionary of the English Language*
- Over 2,000 Spot Maps and Illustrations
- Easy to use with thumb indexes

UPDATED
REVISED
DELUXE
EDITION

WEBSTER'S ENCYCLOPEDIC UNABRIDGED DICTIONARY OF THE ENGLISH LANGUAGE

WEBSTER'S ENCYCLOPEDIC UNABRIDGED DICTIONARY OF THE ENGLISH LANGUAGE



The dictionary entries are based on the Second Edition of
The Random House Dictionary of the English Language

GRAMERCY BOOKS
New York • Avenel

Acknowledgments and Permissions

The "A Dictionary of the English Language" section of this book (*Webster's Encyclopedic Unabridged Dictionary*) is based on the second edition of *The Random House Dictionary of the English Language, the Unabridged Edition*, copyright © 1993, 1987.

This 1996 edition is published by Gramercy Books,
a division of Random House Value Publishing, Inc.,
40 Engelhard Avenue, Avenel, New Jersey 07001.

Gramercy Books and colophon are trademarks of
Random House Value Publishing, Inc.

Random House
New York • Toronto • London • Sydney • Auckland

Printed and bound in the United States

Library of Congress Cataloging-in-Publication Data
Webster's encyclopedic unabridged dictionary of the English language—
New rev. ed.
p. cm.
"The dictionary entries are based on the second edition of
The Random House dictionary of the English language."
1. English language—Dictionaries.
PE1625.W46 1994
423dc20 94-48137
CIP

OLD ISBN: 0–517–11888–2
New Deluxe Edition: 0–517–15026–3

10 9 8 7 6 5 4 3 2 1

chiefly an informal ... and South.

fix·ate (fik′sāt), *v.t.* **-ated, -at·ing.** —*v.t.* **1.** to fix; make stable or stationary. **2.** *Psychoanal.* to develop a fixation; suffer an arrest of one's emotional or sexual development. [1880–85; < L *fix(us)* fixed, firm (see FIX) + -ATE¹]

fix·a·tion (fik sā′shən), *n.* **1.** the act of fixing or the state of being fixed. **2.** *Chem.* **a.** reduction from a volatile or fluid to a stable or solid form. **b.** the process of converting atmospheric nitrogen into a useful compound, as a nitrate fertilizer. **3.** *Photog.* the process of rendering an image permanent by removal of light-sensitive silver halides. **4.** *Psychoanal.* a partial arrest of emotional and instinctual development at an early point in life, due to a severe traumatic experience or an overwhelming gratification. **5.** a preoccupation with one subject, issue, etc.; obsession: *All her life she had a fixation on stories of violent death.* [1350–1400; ME *fixacion* < ML *fixātiōn-* (s. of *fixātiō*) a reduction to a fixed state. See FIX, -ATION]

fix·a·tive (fik′sə tiv), *adj.* **1.** serving to fix; making fixed or permanent. —*n.* Also, **fix·a·tif** (fik′sə tif, -tēf′). **2.** a fixative substance, as a gummy liquid sprayed on a drawing to prevent blurring, or a solution for killing, hardening, and preserving material for microscopic study. **3.** Also called **fixer.** *Photog.* a chemical substance, as sodium thiosulfate, used to promote fixation. **4.** a substance that retards evaporation, as in the manufacture of perfume. [1635–45; FIX + -ATIVE]

fix·a·tor (fik′sā tər), *n.* a device incorporating a metal bar and pins that is used in stabilizing difficult bone fractures. Also, **fix′at·or.** [1870–75; FIX + -ATOR]

fixed (fikst), *adj.* **1.** fastened, attached, or placed so as to be firm and not readily movable; firmly implanted; stationary; rigid. **2.** rendered stable or permanent, as color. **3.** set or intent upon something; steadily directed: *a fixed stare.* **4.** definitely and permanently placed: *a fixed buoy; a fixed line of defense.* **5.** not fluctuating or varying; definite: *a fixed purpose.* **6.** supplied with or having enough of something necessary or wanted, as money. **7.** coming each year on the same calendar date: *Christmas is a fixed holiday, but Easter is not.* **8.** put in order. **9.** *Informal.* arranged in advance privately or dishonestly: *a fixed horse race.* **10.** *Chem.* **a.** (of an element) taken into a compound from its free state. **b.** nonvolatile, or not easily volatilized: *a fixed oil.* **11.** *Math.* (of a point) mapped to itself by a given function. Cf. **Brouwer fixed-point theorem.** [1350–1400; ME; see FIX, -ED²] —**fix·ed·ly** (fik′sid lē, fikst′lē), *adv.* —**fix′·ed·ness,** *n.*

—**Syn. 3.** constant, steady, unvarying, unwavering, firm.

fixed′ ac′tion pat′tern, *Ethology.* a highly stereotyped pattern of behavior that is characteristic of a particular species. [said to be a trans. of G *Erbkoordination,* term used by Konrad Lorenz]

fixed′ as′set, any long-term asset, as a building, tract of land, or patent. Also called **capital asset.** [1895–1900]

fixed′ bridge′, *Dentistry.* a partial denture that is secured permanently in the mouth by being cemented to the adjacent teeth or roots.

fixed′ cap′ital, capital goods, as machinery and tools, that are relatively durable and can be used repeatedly in the production of goods. Cf. **circulating capital.** [1840–50]

fixed′ charge′, **1.** an expense that cannot be modified. **2.** a periodic obligation, as taxes, interest on bonds, etc. **3. fixed charges,** such charges as depreciation, rent, interest, etc., arising out of the maintenance of fixed assets. [1890–95, *Amer.*]

fixed′ cost′, a cost unvarying with a change in the volume of business (distinguished from *variable cost*).

fixed′-do′ sys′tem (fikst′dō′), *Music.* a system of solmization in which the syllable *do* is always C, regardless of the key. Cf. **movable-do system.**

fixed′-fo′cus cam′era (fikst′fō′kəs), a camera with an unadjustable focal length and with a relatively large depth of field. [1890–95]

fixed′ ide′a, a persistent or obsessing idea, often delusional, that can, in extreme form, be a symptom of psychosis. [1820–30]

fixed-in·come (fikst′in′kum), *adj.* gaining or yielding a more or less uniform rate of income. [1855–60]

fixed′ invest′ment trust′. See **unit trust** (def. 1).

fixed-length (fikst′lengkth′, -length′), *adj. Computers.* referring to a field, record, computer word, or other entity whose length does not vary.

fixed′ liabil′ity, a liability, as a mortgage or debenture, that will not mature for a relatively long time.

fixed′ oil′, *Chem.* a natural vegetable or animal oil that is nonvolatile, as lard oil, linseed oil, etc. Also called **fatty oil.** [1790–1800]

fixed′ price′, a price established by a seller, by agreement or by authority, as the price to be charged invariably. [1905–10] —**fixed′-price′,** *adj.*

fixed′-rate mort′gage (fikst′rāt′), a home mortgage for which equal monthly payments of interest and principal are paid over the life of the loan, usually for a term of 30 years.

fixed′ sign′, *Astrol.* any of the four astrological signs, Taurus, Leo, Scorpio, or Aquarius, that are grouped together because of their placement midway between solstices and equinoxes and characterized by identification of those born under the sign with the shared attribute of motivation through subjective values toward a well-defined goal. Cf. **quadruplicity.**

fixed′ star′, *Astron.* any of the stars which apparently always retain the same position in respect to one another. [1555–65]

craft that derive lift from the motion of ... aerodynamically designed surfaces that are rigidly and permanently attached to the fuselage.

fix·er (fik′sər), *n.* **1.** a person or thing that fixes. **2.** *Informal.* a person who arranges matters in advance through bribery or influence. **3.** *Photog.* fixative (def. 3). **4.** *Slang.* a person who sells narcotics to addicts. [1840–50; FIX + -ER¹]

fix·er-up·per (fik′sər up′ər), *n. Informal.* **1.** a person who is handy at making repairs. **2.** a rundown dwelling offered at a bargain price and suitable for improvement by a new owner, often with the object of resale at a considerable profit. [*fix up* + -ER¹, pleonastically suffixed to both words]

fix·ing (fik′sing), *n.* **1.** the act of a person or thing that fixes. **2. fixings.** Also, **fix·in's** (fik′sinz). *Informal.* **a.** the necessary ingredients: *salad fixings.* **b.** the appropriate accompaniments; trimmings: *turkey with all the fixings.* **3.** See **gold fixing.** [1425–75; late ME; see FIX, -ING¹]

fix·it (fiks′it′), *adj. Informal.* of, pertaining to, doing, or involving repairs, adjustments, or improvements: *a fix-it shop; a political fix-it man.* Also, **fix′it′.**

fix·i·ty (fik′si tē), *n., pl.* **-ties** for 2. **1.** the state or quality of being fixed; stability; permanence. **2.** something fixed, stable, or permanent. [1660–70; < NL *fixitās.* See FIX, -ITY]

fixt (fikst), *v.* a pt. and pp. of **fix.**

fix·ture (fiks′chər), *n.* **1.** something securely, and usually permanently, attached or appended, as to a house, apartment building, etc.: *a light fixture; kitchen fixtures.* **2.** a person or thing long established in the same place or position. **3.** *Mach.* **a.** any of various devices for holding work in a machine tool, esp. one for machining in a straight line, as in a planer or milling machine. **b.** any of various devices for holding parts in certain positions during welding, assembly, etc. **4.** *Law.* a movable chattel, as a machine or heating plant, that, by reason of annexation to real property and adaptation to continuing use in connection with the realty, is considered a part of the realty. **5.** *Fox Hunting.* one of a series of meets scheduled by a hunt to take place at a time and location listed on a card (**fix′ture card′**) that is sent, usually once a month, to each member of a hunt. **6.** the act of fixing. **7.** *Brit.* an event that takes place regularly. [1590–1600; var. of obs. *fixure* (< LL *fixūra;* see FIX, -URE), with *-t-* from MIXTURE] —**fix′ture·less,** *adj.*

fix-up (fiks′up′), *n.* repair; improvement: *fix-ups that will make the house more salable.* [1825–35, *Amer.*; n. use of v. phrase *fix up*]

Fi·zeau (fē zō′), *n.* **Ar·mande Hip·po·lyte Louis** (ärmänd′ ē pô lēt′ lwē), 1819–96, French physicist.

fiz·gig (fiz′gig′), *n.* **1.** a type of firework that makes a loud hissing sound. **2.** a whirling toy that makes a whizzing noise. **3.** fishgig. **4.** *Australian.* a police informer. [1520–30; earlier *fisgig,* equiv. to *fis* (late ME *fise* term of abuse; akin to ON *fīsa* to break wind; cf. FIZZLE) + *gig* (ME *gigge* girl; see GIGGLE)]

fizz (fiz), *v.i.* **1.** to make a hissing or sputtering sound; effervesce. —*n.* **2.** a fizzing sound; effervescence. **3.** effervescent water. **4.** an iced soda water or other effervescent water. **4.** an iced mixed drink made of liquor, lemon juice, sugar, and soda: *gin fizz.* **5.** *Brit. Informal.* champagne. [1655–65; back formation from FIZZLE] —**fizz′er,** *n.*

fiz·zle (fiz′əl), *v.,* **-zled, -zling,** *n.* —*v.i.* **1.** to make a hissing or sputtering sound, esp. one that dies out weakly. **2.** *Informal.* to fail ignominiously after a good start (often fol. by *out*): *The reform movement fizzled out because of poor leadership.* —*n.* **3.** a fizzling, hissing, or sputtering. **4.** *Informal.* a failure; fiasco. [1525–35; earlier *fysel* to break wind, freq. of **fise* < ON *fīsa* to break wind; akin to FEIST]

—**Syn. 2.** miscarry, collapse, founder.

fizz·wa·ter (fiz′wô′tər, -wot′ər), *n.* effervescent water; soda water. [FIZZ + WATER]

fizz·y (fiz′ē), *adj.,* **fizz·i·er, fizz·i·est.** bubbly; fizzing. [1850–55; FIZZ + -Y¹]

fjeld (fyeld; *Norw.* fyel), *n.* a rocky, barren plateau of the Scandinavian peninsula. [1855–60; < Norw; see FELL²]

fjord (fyôrd, fyōrd; *Norw.* fyōr, fyôər), *n.* **1.** a long, narrow arm of the sea bordered by steep cliffs: usually formed by glacial erosion. **2.** (in Scandinavia) a bay. Also, **fiord.** [< Norw; see FIRTH] —**fjord′ic,** *adj.*

FL, 1. Florida (approved esp. for use with zip code). **2.** foreign language.

fl, foot-lambert.

fl, *Sports.* flanker.

Fl., 1. Flanders. **2.** Flemish.

fl., 1. floor. **2.** florin. **3.** flourished. [< L *flōruit*] **4.** fluid. **5.** (in the Netherlands) guilder; guilders. [< D *florin*]

Fla., Florida.

flab (flab), *n.* **1.** flabby flesh; unwanted fat: *Daily exercise will get rid of the flab around your waist.* **2.** the condition of being flabby: *Most of the new recruits had run to flab in civilian life.* [1920–25; back formation from FLABBY]

flab·ber·gast (flab′ər gast′), *v.t.* to overcome with surprise and bewilderment; astound. [1765–75; var. of *flabagast* (perh. FLABB(Y) + AGHAST)] —**flab′ber·gast′·er,** *n.*

—**Syn.** amaze, astonish, stagger, nonplus, confound; perplex, confuse, mystify.

flab·by (flab′ē), *adj.,* **-bi·er, -bi·est.** **1.** hanging loosely or limply, as flesh or muscles; flaccid. **2.** having such flesh. **3.** lacking strength or determination. [1690–1700; appar. expressive alter. of earlier *flappy,* with same sense; see FLAP, -Y¹; cf. late ME *flabband* (attested once),

shaped. Also, **fla·bel·li·form** ... < L *flabell(um)* fan + -ATE¹]

fla·bel·late (flə bel′āt), *adj.* combining form of **flabellum:** *flabelliform.*

fla·bel·lum (flə bel′əm), *n., pl.* **-bel·la** (-bel′ə). **1.** a fan, esp. one used in religious ceremonies. **2.** a fan-shaped part. [1865–70; < L *flābellum* fan, dim. of *flābra* breezes, equiv. to *flā(re)* to BLOW² + *-bra,* pl. of *-brum* n. suffix of means; see CASTELLUM for formation]

flac·cid (flak′sid, flas′id), *adj.* **1.** soft and limp; not firm; flabby: *flaccid biceps.* **2.** lacking force; weak: *flaccid prose.* [1610–20; < L *flaccidus* flabby, equiv. to *flacc(ēre)* to grow weak, languish + *-idus* -ID⁴] —**flac·cid′i·ty, flac′cid·ness,** *n.* —**flac′cid·ly,** *adv.*

flack¹ (flak), *n. Sometimes Disparaging.* **1.** See **press agent. 2.** publicity. —*v.i.* **3.** to serve as a press agent or publicist: *to flack for a new rock group.* —*v.t.* **4.** to promote; publicize: *to flack a new record.* [1935–40; said to be after Gene *Flack,* a movie publicity agent]

flack² (flak), *n.* flak.

flack·er·y (flak′ə rē), *n. Sometimes Disparaging.* publicity and promotion; press-agentry. [FLACK¹ + -ERY]

flac·on (flak′ən; *Fr.* flA kôN′), *n., pl.* **flac·ons** (flak′ənz; *Fr.* flA kôN′). a small bottle or flask with a stopper, esp. one used for perfume. [1815–25; < F; see FLAGON]

flag¹ (flag), *n., v.,* **flagged, flag·ging.** —*n.* **1.** a piece of cloth, varying in size, shape, color, and design, usually attached at one edge to a staff or cord, and used as the symbol of a nation, state, or organization, as a means of signaling, etc.; ensign; standard; banner; pennant. **2.** *Ornith.* the tuft of long feathers on the legs of falcons and most hawks; the lengthened feathers on the crus or tibia. **3.** *Hunting.* the tail of a deer or of a setter dog. **4.** *Journalism.* **a.** the nameplate of a newspaper as printed on the editorial page. **5.** a tab or tag attached to a page, file card, etc., to mark it for attention. **6.** *Music.* hook (def. 12a). **7.** *Motion Pictures, Television.* a small gobo. **8.** Usually, **flags.** the ends of the bristles of a brush, esp. a paintbrush, when split. **9.** *Computers.* a symbol, value, or other means of identifying data of interest, or of information forming later parts of a program what conditions earlier parts have encountered. **10. strike the flag, a.** to remove linquish command, as of a ship. **b.** to submit or surrender: *His financial situation is growing worse, but he'll not ready to strike the flag.* Also, **strike one's flag.** —*v.t.* **11.** to place a flag or flags over or on; decorate with flags. **12.** to signal or warn (a person, automobile, etc.) with or as if with a flag (sometimes fol. by *down*): *to flag a taxi; to flag down a passing car.* **13.** to communicate (information) by or as if by a flag. **14.** to decoy, as game, by waving a flag or the like to excite attention or curiosity. **15.** to mark (a page in a book, file card, etc.) for attention, as by attaching protruding tabs. **16.** (of a brush) to split the ends of the bristles [1475–85; perh. b. FLAP (n.) and FAG³ (n.) in obs. sense "flap"] —**flag′ger,** *n.* —**flag′less,** *adj.*

flag² (flag), *n.* **1.** any of various plants with long sword-shaped leaves, as the sweet flag. **2.** See **blue flag. 3.** the long, slender leaf of such a plant or of cereal. [1350–1400; ME *flagge*]

flag³ (flag), *v.i.,* **flagged, flag·ging.** **1.** to fall off in vigor, energy, activity, interest, etc.: *Public enthusiasm flagged when the team kept losing.* **2.** to hang loosely or limply; droop. [1535–45; perh. b. of FLAP (v.) and FAG (v.) in obs. sense "to droop". See FLAG¹]

—**Syn. 1.** dwindle, wilt, slump, sag, wane.

flag⁴ (flag), *n., v.,* **flagged, flag·ging.** —*n.* **1.** flagstone (def. 1). **2. flags,** flagstones [1400–50; late ME *flagge* piece of sod; akin to ON *flaga* slab] —**flag′ger,** *n.*

flag′ day′, (*sometimes caps.*) *Brit.* See **tag day.** [1910–15]

Flag′ Day′, June 14, the anniversary of the day (June 14, 1777) when Congress adopted the Stars and Stripes as the national flag of the United States.

fla·gel·la (flə jel′ə), *n.* a pl. of **flagellum.**

flag·el·lant (flaj′ə lənt, flə jel′ənt), *n.* **1.** a person who flagellates or scourges himself or herself for religious discipline. **2.** a person who derives sexual pleasure from whipping or being whipped by another person. **3.** (*often cap.*) one of a medieval European sect of fanatics who practiced scourging in public. —*adj.* **4.** flagellating. **5.** severely criticizing: *a flagellant attack on opposition party.* [1555–65; < L *flagellant-* (s. of *flagellāns*) whipping, prp. of *flagellāre.* See FLAGELLUM, -ANT] —**flag′el·lant·ism,** *n.*

fla·gel·lar (flə jel′ər), *adj. Biol.* of or pertaining to a flagellum. [1885–90; FLAGELL(UM) + -AR¹]

Flag·el·la·ta (flaj′ə lā′tə), *n.* Mastigophora. [< neut. pl. of L *flagellātus* FLAGELLATE]

flag·el·late (*v.* flaj′ə lāt′; *adj., n.* flaj′ə lit, -lāt′), **-lat·ed, -lat·ing,** *adj., n.* —*v.t.* **1.** to whip; scourge; lash. —*adj.* **2.** Also, **flag′el·lat′ed.** *Biol.* having flagella. **3.** *Bot.* producing filiform runners or runnerlike branches, as the strawberry. **4.** pertaining to or caused by flagellates. —*n.* **5.** any protozoan of the class (or class) Mastigophora, having one or more flagella. See illus. on next page. [1615–25; < L *flagellātus* of *flagellāre* to whip. See FLAGELLUM, -ATE¹] —**flag′el·la′tion,** *n.* —**flag·el·la·to·ry** (flaj′ə lə tôr′ē, -tōr′ē, flag′ə lə-), *adj.*

See Also:

Five-Year Plan
fivefold
fivepins
fiver
fives
fix
fix up
fixate
fixation
fixative
fixed
fixed assets
fixed oil
fixed satellite
fixed star
fixed-point representation
fixer
fixing
fixity
fixture
fizgig

Settings:

Click on word:
gets translation
does nothing

Recent searches:
Save history
fixed
View All

Links:

Abbreviations
Pron. Symbols
Forums
Support WR
Suggestions

fixed

LISTEN: US /fɪkst/

in Spanish | in French | in Italian | English synonyms | in context | images

WordReference Random House Learner's Dictionary of American English © 2017

fixed /fɪkst/
adj.

1. attached or placed so as to be firm and immovable; stationary:
   fixed fortifications.
2. set or intent upon something;
   steadily directed:
   a fixed stare. [*before a noun*]
3. not fluctuating or varying:
   fixed income.
4. having the outcome arranged dishonestly in advance: Informal Terms
   a fixed race.

fix•ed•ly /ˈfɪksɪdli, ˈfɪkstli/ **adv.:**
I stared fixedly into the fire.

WordReference Random House Unabridged Dictionary of American English © 2017

fixed (fikst),
adj.

1. fastened, attached, or placed so as to be firm and not readily movable; firmly implanted;
   stationary;
   rigid.
2. rendered stable or permanent, as color.
3. set or intent upon something;
   steadily directed:
   a fixed stare.
4. definitely and permanently placed:
   a fixed buoy; a fixed line of defense.
5. not fluctuating or varying;
   definite:
   a fixed purpose.
6. supplied with or having enough of something necessary or wanted, as money.
7. coming each year on the same calendar date:
   Christmas is a fixed holiday, but Easter is not.
8. put in order.
9. arranged in advance privately or dishonestly: Informal Terms
   a fixed horse race.
10. Chemistry
    - (of an element) taken into a compound from its free state.
    - nonvolatile, or not easily volatilized:
      a fixed oil.
11. (of a point) mapped to itself by a given function. Cf. **Brouwer fixed-point theorem.** Mathematics

fix•ed•ly (fik′sid lē, fikst′lē), **adv.**
fix′ed•ness, n.

Etymology
→ 1350–1400; Middle English; see FIX, -ED[2]

Synonyms
3. constant, steady, unvarying, unwavering, firm.

Collins Concise English Dictionary © HarperCollins Publishers::

fixed /fikst/

ADJ

1. attached or placed so as to be immovable
2. not subject to change; stable: *fixed prices*
3. steadily directed: *a fixed expression*
4. established as to relative position: *a fixed point*
5. not fluctuating; always at the same time: *a fixed holiday*
6. (of ideas, notions, etc) firmly maintained
7. (of an element) held in chemical combination: *fixed nitrogen*
8. (of a substance) nonvolatile
9. arranged
10. INFORMAL equipped or provided for, as with money, possessions, etc
11. INFORMAL illegally arranged: *a fixed trial*

- **fixedly** /ˈfiksɪdlɪ/

  ADV

- ˈ**fixedness**

  N

'**fixed**' also found in these entries:

A, a - American plan - Aquarius - B, b - activator - ad valorem - aeroplane - affirm - airplane - albumin color - allowance - alphabet - ambulatory - amerce - anchor - anchor bolt - angle of incidence - anniversary reaction - annuity - answer - ante - anthracite - anthropometer - anvil - appliqué - appointment - arch head - around - ar ˈticu ˌlator - assembly district - assets - astronomical frame of reference - asynchronous - attached - automatic - axis - axletree - azeotrope - bad - bait - ball valve - bank rate - bar clamp - basifixed - basket - bathtub - be - beacon - bearing - bed stone

Synonyms: rigid, immovable, firm, mended, repaired, more...

Forum discussions with the word(s) "fixed" in the title:

<took> you to get your squeaker fixed
a fixed location clutching a handful of textbooks
a fixed payment amount made vs. a fixed amount of payment made
a fixed phrase such as a prepositional phrase and a verb phrase is used as a noun
a more fixed job.
a simple competition for a fixed amount of food
a smile fixed/with a smile fixed
a word that survives only one (or several) fixed expression(s)?
about having our kitchen fixed
Alphabetical with post fixed ", The" or ", A"
arbitrary scale fixed
at his fine lineaments fixed in study
At that point Karl fixed the captain as hard as he could
Beyond repair vs. can't be fixed
can we use progressive infinitive for fixed plans?
cavity fixed or filled?
clean fixed
come first / fixed in the rotations
Contractual term for fixed period
dog has been fixed
engage someone at the astounding rate - have a fixed home
eyes fixed on beautiful girl
Fix or Fixed
fixed
Fixed Assets

Fixed at one place
fixed by someone's gaze
fixed compass points
Fixed costs,by way of maintenance, will increase by $1000 per month
fixed eight board
more...

- Visit the English Only Forum.
- Help WordReference: Ask in the forums yourself.

Look up "fixed" at Merriam-Webster
Look up "fixed" at dictionary.com

In other languages: Spanish | French | Italian | Portuguese | German | Swedish | Dutch | Russian | Polish | Romanian | Czech | Greek | Turkish | Chinese | Japanese | Korean | Arabic

MACMILLAN DICTIONARY

fixed - definition and synonyms

ADJECTIVE /fɪkst/

Using the thesaurus

Contribute to our Open Dictionary

1 something such as an amount, date, or time that is fixed has been agreed on and will not change
a fixed price
The contract is for a fixed period of three years.
The interest rate on the loan is fixed.

Synonyms and related words

Unlikely or impossible to change: *unchanging*, *firm*, *rigid*...

Explore Thesaurus

a. a fixed expression on someone's face does not change or look natural
a fixed smile

Synonyms and related words

Words used to describe facial expressions:
absent, *appealing*, *beatific*...

Explore Thesaurus

b. a fixed idea or opinion does not change although it may be wrong
My mother has fixed ideas about how to bring up children.

Synonyms and related words

Words used to describe thoughts, beliefs and ideas:
deterministic, *abstract*, *central*...

Explore Thesaurus

Related words

fix VERB
fixed-rig ADJECTIVE
fixed asset NOUN
fixed cost NOUN
fixed capital NOUN
fixed income NOUN

2 something that is fixed is fastened in one position so that it does not move

Make sure bookcases are securely fixed to the wall in case of earthquake.

Synonyms and related words

Tight and held firmly in place: *tight*, *firm*, *steady*...

Explore Thesaurus

3 if something such as a game or election is fixed, it is dishonestly arranged so that it has the result that someone wants

Synonyms and related words

Words used to describe plans and preparations: *strategic*, *tactical*, *workable*...

Explore Thesaurus

PHRASES

- how someone is fixed for something

From the Blog

What is a mugwump?

Quiz – British and American English

Word of the Day: schmuck

Wake up and smell the petrichor

Language tip of the week: surprising

BuzzWord

gaslight

to manipulate someone psychologically so that they begin to question their own perceptions and memories

BuzzWord Article

More BuzzWords

creep	defriend	black swan
occupy	marmite	oversharing
slow	optics	solutionism

BuzzWord archive

Open Dictionary

Dunning-Kruger effect

the phenomenon by which an incompetent person is too incompetent to understand his own incompetence

add a word

More submissions

kompot	shire	gibbous
potica	RAC	golden buzzer
siloviki	Sheng	biohacking

view entries

Blog

fixed

[fikst]

Synonyms Examples Word Origin

See more synonyms on Thesaurus.com (http://www.thesaurus.com/browse/fixed)

adjective

1. fastened, attached, or placed so as to be firm and not readily movable; firmly implanted; stationary; rigid.

2. rendered stable or permanent, as color.

3. set or intent upon something; steadily directed:
   a fixed stare.

---

4. definitely and permanently placed:
   a fixed buoy; a fixed line of defense.

5. not fluctuating or varying; definite:
   a fixed purpose.

6. supplied with or having enough of something necessary or wanted, as money.

7. coming each year on the same calendar date:
Christmas is a fixed holiday, but Easter is not.

Origin of fixed

Middle English (http://www.dictionary.com/browse/middle-english)

1350-1400

Middle English word dating back to 1350-1400; See origin at fix (http://www.dictionary.com/browse/fix), -ed (http://www.dictionary.com/browse/-ed)[2]

Related forms

fixedly [**fik**-sid-lee, **fikst**-lee] (Show IPA), adverb

fixedness, noun

semifixed, adjective

Synonyms

See more synonyms on Thesaurus.com (http://www.thesaurus.com/browse/fixed)

3. constant, steady, unvarying, unwavering, firm.

fix

[fiks]

verb (used with object), **fixed** or **fixt, fixing.**

1. to repair; mend.

2. to put in order or in good condition; adjust or arrrange:
She fixed her hair in a bun.

3. to make fast, firm, or stable.

4. to place definitely and more or less permanently:
to fix a circus poster to a wall.

5. to settle definitely; determine:
   to fix a price.

6. to direct (the eyes, the attention, etc.) steadily:
   His eyes were fixed on the distant ship.

7. to attract and hold (the eye, the attention, etc.).

---

verb (used without object), **fixed** or **fixt, fixing.**

21. to become fixed.

22. to become set; assume a rigid or solid form.

23. to become stable or permanent.

24. to settle down.

25. *Slang.* to inject oneself with a narcotic.

26. *Chiefly Southern U.S.* to prepare; plan (usually followed by an infinitive):
   I was just fixing to call you. We're fixing to go to Colorado this summer.

noun

27. *Informal.* a position from which it is difficult to escape; predicament.

28. *Informal.* a repair, adjustment, or solution, usually of an immediate nature:
   Can you think of a fix for the problem?

29. *Navigation.*
   a. a charted position of a vessel or aircraft, determined by two or more bearings taken on landmarks, heavenly bod-ies, etc.
   b. the determining of the position of a ship, plane, etc., by mathematical, electronic, or other means:
      The navigator took a fix on the sun and steered the ship due north.

30. a clear determination:
   Can you get a fix on what he really means?

31. *Slang.*
   a. an injection of heroin or other narcotic.
   b. the narcotic or amount of narcotic injected.
   c. a compulsively sought dose or infusion of something:
      to need one's daily fix of soap operas on TV.

32. *Slang.*
   a. an underhand or illegal arrangement, especially one secured through bribery or influence.
   b. a contest, situation, etc., whose outcome is prearranged dishonestly.

Verb phrases

33. **fix on/upon,** to decide on; determine:
   We won't be able to fix on a location for the banquet until we know the number of guests.

34. **fix up,** *Informal.*
   a. to arrange for:
      to fix up a date.

b. to provide with; furnish.
c. to repair; renew.
d. to smooth over; solve:
They weren't able to fix up their differences.

Idioms

35. **fix one's wagon,** *Informal.* to exact retribution for an offense; treat someone vengefully:
I'll dock his pay and that will fix his wagon.

36. **in a fix,** *Older Slang.* pregnant.

Origin

1350-1400; 1900-05 for def 29; 1935-40 for def 31; Middle English *fixen* (v.) < Medieval Latin *fixāre,* derivative of Latin *fixus* fixed, past participle of *figere* to fasten

Related forms

fixable, adjective

fixability, noun

overfix, verb

refix, verb (used with object), **refixed, refixing.**

unfixable, adjective

Synonyms

See more synonyms on Thesaurus.com (http://www.thesaurus.com/browse/fix)

1. correct, amend. **3, 4.** fasten, secure, stabilize. Fix, establish imply making firm or permanent. To fix is to fasten in position securely or to make more or less permanent against change, especially something already existing: *to fix a bayonet on a gun; fix a principle in one's mind.* To establish is to make firm or permanent something (usually newly) originated, created, or ordained: *to establish a business, a claim to property.* **5.** establish, define. **27.** dilemma, plight, quandary.

Usage note

Fix meaning "to repair" appears to have been used first in America, but it is long established and has been used in England since the early 19th century: *The engineer quickly fixed the faulty valve.* The verb use is fully standard in all varieties of speech and writing, and objections to it on the grounds of style merely reflect personal prejudice, not the practice of educated speakers and writers. The noun fix meaning "repair, adjustment" is informal.
Fix (to) meaning "to prepare, plan (to)" is another Americanism: *We're fixing to go to town.* It once occurred in all the eastern coastal states, but it is

---

Examples from the Web for fixed

Contemporary Examples

These are houses that were *fixed* up and improved by their purchasers that are sitting empty, with lawns unmowed.

Meltdown on the Message Boards (http://www.thedailybeast.com/articles/2008/10/10/meltdown-on-the-message-boards.html?source=dictionary)
(http://www.thedailybeast.com?source=dictionary)
The Daily Beast (http://www.thedailybeast.com/contributors/the-daily-beast.html?source=dictionary)
October 9, 2008

The handicap, after some needling back and forth, was *fixed* at eight strokes.

Portrait of the Consummate Con Man (http://www.thedailybeast.com/articles/2014/05/17/the-stacks-portrait-of-the-consummate-con-man.html?source=dictionary)
(http://www.thedailybeast.com?source=dictionary)
John Lardner (http://www.thedailybeast.com/contributors/john-lardner.html?source=dictionary)
May 16, 2014

I hate to burst your *fixed* idea that Tomasky surely comes from a long line of elitists.

A Note to Conservative Readers (http://www.thedailybeast.com/articles/2012/06/20/a-note-to-conservative-readers.html?source=dictionary)
(http://www.thedailybeast.com?source=dictionary)
Michael Tomasky (http://www.thedailybeast.com/contributors/michael-tomasky.html?source=dictionary)
June 19, 2012

I believe the market for books is not *fixed*, meaning for every e-book sold, one less print book would be sold.

British Dictionary definitions for fixed

fixed

/fɪkst/

adjective

1. attached or placed so as to be immovable

2. not subject to change; stable: *fixed prices*

fix

/fɪks/

verb (**mainly transitive**)

1. (**also intransitive**) to make or become firm, stable, or secure

2. to attach or place permanently: *fix the mirror to the wall*

Word Origin and History for fixed

fix

n.

"position from which it is difficult to move," 1809, American English, from fix (/browse/fix) (v.). Meaning "dose of narcotic" is from 1934, shortened from *fix-up* (1867, originally in reference to liquor).

fix

v.

late 14c., "set (one's eyes or mind) on something," probably from Old French **fixer*, from *fixe* "fixed," from Latin *fixus* "fixed, fast, immovable, established, settled," past participle of *figere* "to fix, fasten," from PIE root **dhigw-* "to stick, to fix."

Sense of "fasten, attach" is c.1400; that of "settle, assign" is pre-1500 and evolved into "adjust, arrange" (1660s), then "repair" (1737). Sense of "tamper with" (a fight, a jury, etc.) is 1790. As euphemism for "castrate a pet" it dates from 1930. Related: *Fixed*; *fixedly* (1590s); *fixing*.

n.

"position from which it is difficult to move," 1809, American English, from fix (/browse/fix) (v.). Meaning "dose of narcotic" is from 1934, shortened from *fix-up* (1867, originally in reference to liquor).

fixed in Science

fix (fĭks) (http://content.dictionary.com/help/dictionary/ahsd/pronkey.html)

1. To convert inorganic carbon or nitrogen into stable, organic compounds that can be assimilated into organisms. Photosynthetic organisms such as green plants fix carbon in carbohydrates as food; certain bacteria fix nitrogen as ammonia that can be absorbed directly or through nitrification by plant roots. See more at carbon fixation (http://www.dictionary.com/browse/carbon-fixation), nitrogen fixation.
2. To convert a substance, especially a gas, into solid or liquid form by chemical reactions.
3. To kill and preserve a tissue specimen rapidly to retain as nearly as possible the characteristics it had in the living body.

Slang definitions & phrases for fixed

fixed

adjective

1. Having the outcome prearranged*: the World Series is fixed*
2. Neutered*: fixed cats*
3. Intoxicated or drugged

fix

noun

1. A fight, game, etc, of which the winner has been fraudulently predetermined*: The World Series that year was a blatant fix (1890s+)*

2. (also fix-up) A dose of a narcotic, esp an injection of heroin; blast (/browse/blast)*: afixto calm her jittery nerves (1930s+ Narcotics)*

3. Anything needed to appease a habitual need or craving •One of the common transfers of narcotics terms, like junkie*: He had to have his daily fix*

Idioms and Phrases with fixed

fix

fix someone's wagon (/browse/fix-someone-s-wagon)
fix up (/browse/fix--up)

also see:
get a fix (/browse/get-a-fix)
get a fix on (/browse/get-a-fix-on)
if it ain't broke don't fix it (/browse/if-it-ain-t-broke-don-t-fix-it)
in a fix (/browse/in--a--fix)

fixed

adjective | \ˈfikst\

Popularity: Bottom 40% of words

Examples: FIXED in a Sentence

Definition of FIXED

1 **a** : securely placed or fastened : STATIONARY
b (1) : NONVOLATILE (2) : formed into a chemical compound
c (1) : not subject to change or fluctuation • a *fixed* income (2) : firmly set in the mind • a *fixed* idea (3) : having a final or crystallized form or character (4) : recurring on the same date from year to year • *fixed* holidays
d : IMMOBILE, CONCENTRATED • a *fixed* stare

2 : supplied with something (such as money) needed • comfortably *fixed*

—**fixedly** \ˈfik-səd-lē, ˈfikst-lē\ *adverb*

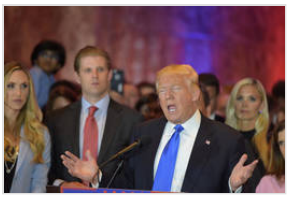
—**fixedness** \ˈfik-səd-nəs, ˈfiks(t)-nəs\ *noun*

See *fixed* defined for English-language learners

See *fixed* defined for kids

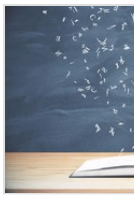
Explore Merriam-Webster

May 2017 Words of the Day Quiz



Trending: Kasowitz: Trump feels 'Vindicated'

'Recur' and 'Reoccur': A Subtle Difference



Becon Dictio

Examples of FIXED in a Sentence

a small mirror *fixed* to the wall

That day remains *fixed* in my memory.

First Known Use of FIXED

14th century

14th Century

Synonyms

certain, determinate, final, firm, flat, frozen, hard, hard-and-fast, inexpugnable, set, settled, stable

Phrases Related to FIXED

Related Phrases

fixed for

fixed for life

have one's hopes/sights fixed on

no fixed abode

FIXED Defined for English Language Learners

fixed

adjective | \ˈfikst\

Definition of FIXED for English Language Learners

having something needed

FIXED Defined for Kids

fixed

adjective | \ˈfikst\

Definition of FIXED for Students

1 : not changing : SET
- … Phoebe wore a *fixed* expression … — Sharon Creech, *Walk Two Moons*

2 : firmly placed • A mirror is *fixed* to the wall. • That day is *fixed* in my memory.

—**fixedly** \ˈfik-səd-lē\ *adverb* • She was staring *fixedly* at me.

Learn More about FIXED

See words that rhyme with *fixed*
Thesaurus: All synonyms and antonyms for *fixed*
Spanish Central: Translation of *fixed*
Nglish: Translation of *fixed* for Spanish speakers
Britannica English: Translation of *fixed* for Arabic speakers

Seen and Heard

What made you want to look up *fixed*? Please tell us where you read or heard it (including the quote, if possible).

+ SHOW 9 COMMENTS

WORD OF THE DAY

penchant

a strong and continued inclination

Get Word of the Day daily email!

Your email address SUBSCRIBE

2 salacious
A synonym of 'lascivious' or 'lecherous'

3 cloche
Your definition is served

4 literature
The times, they are a changin', but the definitions, they are not

5 humdinger
One doozy of a headline

SEE ALL

BROWSE DICTIONARY

fixation

fixative

fixed

fixed accent

fixed ammunition

WORD GAMES

Take a 3-minute break and test your skills!

alt-5746713d76276

Which is a synonym of **skosh**?

prude | smidgen

bushel | elegance

True or

Test your knowledge - and maybe learn something along the way.

Definition of 'fixed'

Learner: fixed
American: fixed
English: fixed
Example sentences
Trends
Translations
Useful links
Comments
Word Frequency

fixed (fɪkst)

1. adjective
You use fixed to describe something which stays the same and does not or cannot vary.
They issue a fixed number of shares that trade publicly.
Many restaurants offer fixed-price menus.
2. adjective
If you say that someone has fixed ideas or opinions, you mean that they do not often change their ideas and opinions, although perhaps they should.
...people who have fixed ideas about things.
3. adjective
If someone has a fixed smile on their face, they are smiling even though they do not feel happy or pleased.
I had to go through the rest of the evening with a fixed smile on my face.
4.
no fixed address
5. See also fix

Word Frequency

fixed in American English (fɪkst ; fikst)

adjective
1.
firmly placed or attached; not movable
2.

te

sition relative to the earth

he mind and tending to control the thoughts and actions; obsessive

le oil

compound from its free state, as atmospheric nitrogen

bric dye

needed, specif. money

estly arranged beforehand

li ; fikˈsidlē)

Word Frequency

fixed (fɪkst)

adjective
1.
attached or placed so as to be immovable
2.
not subject to change; stable
fixed prices
3.
steadily directed
a fixed expression
4.
established as to relative position
a fixed point
5.
not fluctuating; always at the same time
a fixed holiday
6.
(of ideas, notions, etc) firmly maintained
7.
(of an element) held in chemical combination
fixed nitrogen
8.
(of a substance) nonvolatile
9.
arranged
10. astrology
of, relating to, or belonging to the group consisting of the four signs of the zodiac Taurus, Leo, Scorpio, and Aquarius, which are associated with stability
Compare cardinal (sense 9), mutable (sense 2)

11. informal
equipped or provided for, as with money, possessions, etc
12. informal
illegally arranged
a fixed trial

ces containing 'fixed'

fixed two Tom Collins with lots of ice.
MPANY OF STRANGERS (2002)
ing stare, then turned my attention to her mother.
THAN THIS (2002)
are of shade under a tarpaulin fixed to the side of my dead car.
MENTS OF DARKNESS (2002)
artificial island or structure, fixed or permanent.
ACUDA 945 (2002)

Synonyms of 'fixed'

inflexible, set, steady, resolute
immovable, set, established, secure
false, fake, feigned, insincere
agreed, set, planned, decided
mended, going, sorted, repaired
rigged, framed, put-up, manipulated
More Synonyms of fixed

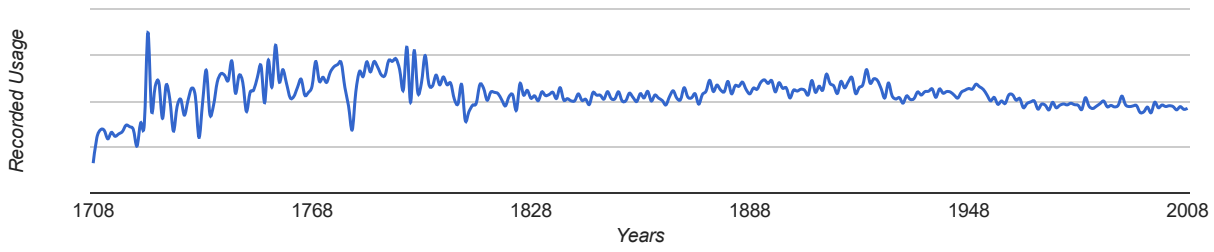
Word Lists

astrology, Edible oils

Trends of 'fixed'

View usage over:

Since Exist ▼



· 'fixed'

ɪst/ ADJECTIVE
something which stays the same and does not vary....fixed house prices.

se: fixado *fixada*

ěnný

fijo *fija*
ikoillaan

ος *στερεωμένη*

rwały
fixada

- Romanian: fix *fix, fixă, ficși, fixe*
- Russian: неизменный
- Spanish: fijo *fija*
- Swedish: lagad *lagat*
- Thai: คงที่
- Turkish: sabitlenmiş
- Ukrainian: закріплений
- Vietnamese: cố định

Translate your text for free

Useful links

Nearby words of 'fixed'

- fixation
- fixative
- fixature
- fixed
- fixed asset
- fixed assets
- fixed charge
- All ENGLISH words that begin with 'F'

Related Terms of 'fixed'

- fix
- fixed oil
- fixed asset
- fixed costs

Search English

Definition of “fixed” - English Dictionary

American-English dictionary

Contents

“fixed” in American English

See all translations

fixed

adjective [not gradable] • US /fɪkst/

★ **not changing:**

a fixed stare

a fixed address

fixedly

adverb [not gradable] US /ˈfɪk·sɪd·li/

She stared fixedly at the screen.

(Definition of “fixed” from the **Cambridge Academic Content Dictionary** © Cambridge University Press)

Translations of “fixed”

in Arabic

ثابِت...

Need a translator?

What is the pronunciation of fixed?

browse

- fixate
- fixated
- fixation
- fixative
- fixed
- fixed annuity
- fixed asset
- fixed assets

Contents

More meanings of “fixed”

All Phrasal Verbs Idioms

fixed penalty

fixed-wing

fixed assets

fixed-term

fix *sb* up

fixed star

fix

See all meanings ›

Word of the Day

seahorse

a small fish that swims in a vertical position and has a head like that of a horse

About this ›