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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/008,227	09/21/2006	6598148	069974-0158	6167

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EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 12/21/2007

Please find below and/or attached an Office communication concerning this application or proceeding.

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EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/008,227*.

PATENT NO. *6598148*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Ex Parte Reexamination Communication	Control No. 90/008,227	Patent Under Reexamination 6598148	
	Examiner Joseph R. Pokrzywa	Art Unit 3992	

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS ACTION IS SET TO EXPIRE 2 MONTH(S) FROM THE MAILING DATE OF THIS LETTER. EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c). If the specified period for response is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.

Joseph R. Pokrzywa
Primary Examiner
Art Unit: 3992

cc: Requester (if third party requester)

Office Action in Ex Parte Reexamination	Control No. 90/008,227	Patent Under Reexamination 6598148	
	Examiner Joseph R. Pokrzywa	Art Unit 3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

a☐ Responsive to the communication(s) filed on _____ . b☐ This action is made FINAL.
c☒ A statement under 37 CFR 1.530 has not been received from the patent owner.

A shortened statutory period for response to this action is set to expire 2 month(s) from the mailing date of this letter. Failure to respond within the period for response will result in termination of the proceeding and issuance of an *ex parte* reexamination certificate in accordance with this action. 37 CFR 1.550(d). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).** If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☒ Information Disclosure Statement, PTO/SB/08.
3. ☐ Interview Summary, PTO-474.
4. ☐ _____.

Part II SUMMARY OF ACTION

1a. ☒ Claims *4,7,8 and 10* are subject to reexamination.
1b. ☒ Claims *1-3,5,6,9 and 11-13* are not subject to reexamination.
2. ☐ Claims _____ have been canceled in the present reexamination proceeding.
3. ☐ Claims _____ are patentable and/or confirmed.
4. ☒ Claims *4,7,8 and 10* are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ The drawings, filed on _____ are acceptable.
7. ☐ The proposed drawing correction, filed on _____ has been (7a)☐ approved (7b)☐ disapproved.
8. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
   a)☐ All b)☐ Some* c)☐ None of the certified copies have
   1☐ been received.
   2☐ not been received.
   3☐ been filed in Application No. _____ .
   4☐ been filed in reexamination Control No. _____.
   5☐ been received by the International Bureau in PCT application No. _____.
   * See the attached detailed Office action for a list of the certified copies not received.
9. ☐ Since the proceeding appears to be in condition for issuance of an *ex parte* reexamination certificate except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte* Quayle, 1935 C.D. 11, 453 O.G. 213.
10. ☐ Other: _____

Joseph R Pokrzywa

JOSEPH R POKRZYWA
PRIMARY EXAMINER
CRU - AU 3992

cc: Requester (if third party requester)

DETAILED ACTION

Reexamination

1. **Claims 4, 7, 8, and 10** of U.S. Patent 6,598,148 (hereafter "the '148 Patent) are subject to reexamination.

2. This action is directed only to the claims for which reexamination was requested. With respect to such claims, the Third Party Requester has alleged that a substantial new question of patentability (SNQ) exists, and upon review, it has been determined that the alleged SNQ in fact is present for claims 4, 7, 8, and 10. No determination was made with respect to the existence or nonexistence of an SNQ with respect to any claim for which reexamination was not specifically requested.

Information Disclosure Statement

3. The prior art references listed in the Information Disclosure Statement submitted on 9/24/07 have been considered by the examiner (see attached PTO/SB/08A).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 4, 7, 8, and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Number 4,689,581, issued to Talbot, Gerald R. (hereafter "Talbot'581") in view of European Patent Publication EP 0 113 516, issued to May, Michael D., being European Patent Application No. 83307078.2 (hereafter noted as "May'516").

Regarding independent ***claim 4***, Talbot'581 teaches of a microprocessor integrated circuit [see Fig. 1, silicon chip 1, col. 2, lines 43-46] comprising:

a processing unit disposed upon an integrated circuit substrate [col. 2, lines 43-52, wherein "the logic device 2 is shown to be a microcomputer, and, for example, could be a microcomputer of the type described in our copending European Patent application No. 83307078.2 filed Nov. 18, 1983 which is fabricated on a single silicon chip."]; and

a ring oscillator having a variable output frequency [oscillator circuit 12, being part of the timing circuit 4, col. 3, lines 26-36, wherein "it is the amplitude of the voltage signal applied to the oscillator circuit 12 which determines the frequency of the oscillations and hence the frequency of the signal appearing at the output 5 of the timing apparatus 4"],

wherein the ring oscillator provides a system clock to the processing unit [col. 8, lines 50-53, "It is intended that the output of the oscillator circuit shown in Fig. 3 be used as a high frequency clock signal, for example for a processor or microcomputer"],

the ring oscillator disposed on said integrated circuit substrate [col. 3, lines 1-4, wherein "all of the components of the timing apparatus 4 are on the single silicon chip and the timing apparatus 4 has been designed such that it does not require any components external to the chip 1"].

However, Talbot'581 does not expressly state if:

said processing unit operates in accordance with a predefined sequence of program instructions and

a memory coupled to said processing unit and capable of storing information provided by said processing unit, said memory occupying a larger area of said integrated circuit substrate than said processing unit said memory further occupying a majority of a total area of said single substrate.

Contrarily, Talbot'581 does state in col. 2, lines 43-52, that the microcomputer "could be a microcomputer of the type described in our copending European Patent Application No. 83307078.2 filed Nov. 18, 1983 which is fabricated on a single silicon chip", whereby as noted above, is referred to as "May'516". With this, May'516 is seen as teaching of:

a microprocessor integrated circuit [page 3, lines 45-48] comprising:

a processing unit disposed upon an integrated circuit substrate [page 4, lines 11-19],

said processing unit operating in accordance with a predefined sequence of program instructions [page 2, lines 42-56];

a memory coupled to said processing unit and capable of storing information provided by said processing unit [page 35, line 50-page 36, line 4],

said memory occupying a larger area of said integrated circuit substrate than said processing unit said memory further occupying a majority of a total area of said single substrate [page 35, lines 43 through 51, and page 4, lines 21-30].

Talbot'581 and May'516 are combinable because they are from the same field of endeavor, being similarly designed microprocessors. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the teachings of May'516 with the system taught by Talbot'581. The suggestion/motivation for doing so would have been that the system of Talbot'581 would avoid the need for separate store allocation for lists or tables indicating subsequent processes to be executed, as recognized by May'516 on page 2, lines 25-31. Further, since Talbot'581 states in col. 2, lines 43-52, that the disclosed microcomputer "could be a microcomputer of the type described in our copending European Patent Application No. 83307078.2 filed Nov. 18, 1983 which is fabricated on a single silicon chip", Talbot'581 effectively envisioned the combination. Therefore, it would have been obvious to combine the teachings of May'516 with the system of Talbot'581 to obtain the invention as specified in claim 4.

Regarding ***claim 7***, Talbot'581 and May'516 disclose the microprocessor integrated circuit discussed above in claim 4, and May'516 further teaches that said memory is capable of supporting read and write operations [see page 2, lines 42-56; also seepage 3, lines 48-50].

As discussed above, Talbot'581 and May'516 are combinable because they are from the same field of endeavor, being similarly designed microprocessors. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the further teachings of May'516 with the system taught by Talbot'581. The suggestion/motivation for doing so would have been that the system of Talbot'581 would avoid the need for separate store allocation for lists or tables indicating subsequent processes to be executed, as recognized by May'516 on page 2, lines 25-31. Further, since Talbot'581 states in col. 2, lines 43-52, that the disclosed microcomputer "could be a microcomputer of the type described in our copending European Patent Application No. 83307078.2 filed Nov. 18, 1983 which is fabricated on a single silicon chip", Talbot'581 effectively envisioned the combination. Therefore, it would have been obvious to combine the teachings of May'516 with the system of Talbot'581 to obtain the invention as specified in claim 7.

Regarding independent ***claim 8***, Talbot'581 teaches of a microprocessor integrated circuit [see Fig. 1, silicon chip 1, col. 2, lines 43-46] comprising:

a processing unit having one or more interface ports for interprocessor communication, said processing unit being disposed on a single substrate [col. 2, lines 43-52, wherein "the logic device 2 is shown to be a microcomputer, and, for example, could be a microcomputer of the

type described in our copending European Patent application No. 83307078.2 filed Nov. 18, 1983 which is fabricated on a single silicon chip."]; and

a ring oscillator having a variable output frequency [oscillator circuit 12, being part of the timing circuit 4, col. 3, lines 26-36, wherein "it is the amplitude of the voltage signal applied to the oscillator circuit 12 which determines the frequency of the oscillations and hence the frequency of the signal appearing at the output 5 of the timing apparatus 4"],

wherein the ring oscillator provides a system clock to the processing unit [col. 8, lines 50-53, "It is intended that the output of the oscillator circuit shown in Fig. 3 be used as a high frequency clock signal, for example for a processor or microcomputer"],

the ring oscillator disposed on said substrate [col. 3, lines 1-4, wherein "all of the components of the timing apparatus 4 are on the single silicon chip and the timing apparatus 4 has been designed such that it does not require any components external to the chip 1"].

However, Talbot'581 fails to expressly disclose of:

a memory disposed upon said substrate and coupled to said processing unit, said memory occupying a greater area of said substrate than said processing unit, said memory further comprising a majority of a total area of said substrate.

Further, Talbot'581 does state in col. 2, lines 43-52, that the microcomputer "could be a microcomputer of the type described in our copending European Patent application No. 83307078.2 filed Nov. 18, 1983 which is fabricated on a single silicon chip.", whereby as noted above, this reference is referred to as "May'516".

With this, May'516 is seen as teaching of a microprocessor integrated circuit [page 3, lines 50-53] comprising:

a processing unit having one or more interface ports for interprocessor communication [Figs. 1 and 11, and page 3, lines 50-53],

said processing unit being disposed on a single substrate [page 4, lines 11-19]; and

a memory disposed upon said substrate and coupled to said processing unit [memories 19 and 20, Figs. 1, 11, and 17, and page 35, line 43-page 36, line 4],

said memory occupying a greater area of said substrate than said processing unit [page 35, lines 50-51],

said memory further comprising a majority of a total area of said substrate [page 4, lines 21-30, and page 35, lines 50-51].

Talbot'581 and May'516 are combinable because they are from the same field of endeavor, being similarly designed microprocessors. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the further teachings of May'516 with the system taught by Talbot'581. The suggestion/motivation for doing so would have been that the system of Talbot'581 would avoid the need for separate store allocation for lists or tables indicating subsequent processes to be executed, as recognized by May'516 on page 2, lines 25-31. Further, since Talbot'581 states in col. 2, lines 43-52, that the disclosed microcomputer "could be a microcomputer of the type described in our copending European Patent Application No. 83307078.2 filed Nov. 18, 1983 which is fabricated on a single silicon chip", Talbot'581 effectively envisioned the combination. Therefore, it would have been obvious to combine the

teachings of May'516 with the system of Talbot'581 to obtain the invention as specified in claim 8.

Regarding ***claim 10***, Talbot'581 and May'516 disclose the microprocessor integrated circuit discussed above in claim 8, and May'516 further teaches of including memory controller means [interpreted as the memory interface 14 and the sync logic 10, seen in Figs. 1 and 2, also see page 4, lines 34-40, wherein "Each serial link 25 has an input pin 26 and an output pin 27 each of which can be used to forma single pin to pin connection to corresponding output and input pins respectively of a further microcomputer. Each serial link is connected to a synchronisation logic unit 10 comprising process scheduling logic..."] coupled to said memory for performing direct memory access data transfer through said one or more interface ports [see Fig. 2, whereby sync logic 10 directly connects with the serial links 25 and the memories 19 and 20; also see page 5, lines 39-45; also see "direct" functions, shown on page 7].

As discussed above, Talbot'581 and May'516 are combinable because they are from the same field of endeavor, being similarly designed microprocessors. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the further teachings of May'516 with the system taught by Talbot'581. The suggestion/motivation for doing so would have been that the system of Talbot'581 would avoid the need for separate store allocation for lists or tables indicating subsequent processes to be executed, as recognized by May'516 on page 2, lines 25-31. Further, since Talbot'581 states in col. 2, lines 43-52, that the disclosed microcomputer "could be a microcomputer of the type described in our copending European

Patent Application No. 83307078.2 filed Nov. 18, 1983 which is fabricated on a single silicon chip", Talbot'581 effectively envisioned the combination. Therefore, it would have been obvious to combine the teachings of May'516 with the system of Talbot'581 to obtain the invention as specified in claim 10.

Conclusion

6. Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that *ex parte* reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extensions of time in *ex parte* reexamination proceedings are provided for in 37 CFR 1.550(c).

7. In order to ensure full consideration of any amendments, affidavits or declarations, or other documents as evidence of patentability, such documents must be submitted in response to this Office action. Submissions after the next Office action, which is intended to be a final action, will be governed by the requirements of 37 CFR 1.116, after final rejection and 37 CFR 41.33 after appeal, which will be strictly enforced.

8. The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent No. 6,598,148 throughout the course of this reexamination proceeding.

NOTICE RE PATENT OWNER'S CORRESPONDENCE ADDRESS

Effective May 16, 2007, 37 CFR 1.33(c) has been revised to provide that:

The patent owner's correspondence address for all communications in an *ex parte* reexamination or an *inter partes* reexamination is designated as the correspondence address of the patent.

> *Revisions and Technical Corrections Affecting Requirements for Ex Parte and Inter Partes Reexamination*, 72 FR 18892 (April 16, 2007)(Final Rule)

The correspondence address for any pending reexamination proceeding not having the same correspondence address as that of the patent is, by way of this revision to 37 CFR 1.33(c), automatically changed to that of the patent file as of the effective date.

This change is effective for any reexamination proceeding which is pending before the Office as of May 16, 2007, including the present reexamination proceeding, and to any reexamination proceeding which is filed after that date.

Parties are to take this change into account when filing papers, and direct communications accordingly.

In the event the patent owner's correspondence address listed in the papers (record) for the present proceeding is different from the correspondence address of the patent, it is strongly encouraged that the patent owner affirmatively file a Notification of Change of Correspondence Address in the reexamination proceeding and/or the patent (depending on which address patent owner desires), to conform the address of the proceeding with that of the patent and to clarify the record as to which address should be used for correspondence.

Telephone Numbers for reexamination inquiries:

Reexamination and Amendment Practice	(571) 272-7703
Central Reexam Unit (CRU)	(571) 272-7705
Reexamination Facsimile Transmission No.	(571) 273-9900

9. ALL correspondence relating to this ex parte reexamination proceeding should be directed as follows:

Please mail any communications to:

Attn: Mail Stop "Ex Parte Reexam"
Central Reexamination Unit
Commissioner for Patents
P. O. Box 1450
Alexandria VA 22313-1450

Please FAX any communications to:

(571) 273-9900
Central Reexamination Unit

Please hand-deliver any communications to:

Customer Service Window
Attn: Central Reexamination Unit
Randolph Building, Lobby Level
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

Signed:

Joseph R. Pokrzywa
Primary Examiner
Central Reexamination Unit 3992
(571) 272-7410

Conferees :

OPQA

ROLAND G. FOSTER
CRU EXAMINER-AU 3992