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Attorneys for Plaintiffs and Counterdefendants
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CORPORATION and GATEWAY, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED,

Defendants.

TECHNOLOGY PROPERTIES LIMITED and PATRIOT SCIENTIFIC CORPORATION,

Counterclaimants

v.

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC.,

Counterdefendants.

Case No. 5:08-cv-00877 JF

PLAINTIFF ACER, INC.'S RESPONSE IN OPPOSITION TO DEFENDANTS' MOTION UNDER CIVIL LOCAL RULES 6-3 AND 7-11 TO CONTINUE TRIAL DATE AND CORRESPONDING DATES

INTRODUCTION

Acer opposes TPL's motion for a continuance. TPL's motion should be denied because TPL failed to show good cause to continue the trial date. If the Court believes any scheduling change is justified, it should hold a case management conference rather than reset the schedule on this administrative motion.

TPL's motion is a thinly-disguised effort to have this Court reconsider the scheduling issues that were already argued and decided at the September 4, 2012 Case Management Conference. There, the parties discussed TPL's filing of an ITC action against Acer, HTC, and Barco respecting the '336 patent at issue here. TPL pushed for an extended trial schedule. Acer, HTC, and Barco refused to stipulate to stay their cases. Ultimately, the Court rejected TPL's arguments based on the concurrent ITC action and set the case for trial for June 24, 2013.

Now, immediately after this Court's determination on certain claim construction issues, TPL again asks the Court for delay, seeking to continue the trial date due to an alleged scheduling "conflict" with the ITC schedule, a schedule known to all parties for over two months. TPL offers no explanation for not seeking relief from the schedule earlier and provides no good cause for the requested four month continuance. Moreover, the scheduling "conflict" is of TPL's own making: TPL chose to file the ITC complaint with full knowledge that, absent a stay, the two schedules would necessarily overlap. TPL's counsel is well-versed in ITC practice and knew or should have known the trial schedule. Additionally, the alleged "conflict" is really in the nature of a schedule overlap, no more burdensome than the overlaps busy lawyers routinely deal with because they have more than one action on their plate at a time. Indeed, the parties have already been simultaneously engaged in both actions for months. Finally, the ITC trial and this trial are set for different times, so no one has to be in two places at the same time.

ADDITIONAL PROCEDURAL HISTORY

TPL's recitation of the procedural history is incomplete. Acer initiated this declaratory relief action on February 8, 2008.[1] On April 25, 2008, based on a later-filed complaint, TPL

[1] This matter was one of three related cases. *See Barco, N.V. v. Technology Properties Ltd.*,

filed a motion to transfer this case to the Eastern District of Texas or, in the alternative, to stay proceedings pending resolution of that case. Docket # 19. On October 21, 2008, Judge Fogel denied TPL's motion. Docket # 47.

On September 4, 2012, this Court held a Case Management Conference. At that conference Acer proposed a schedule that would keep the case moving forward, while TPL proposed that the case should not proceed beyond the claim construction phase until the defendants in newly-filed related cases had an opportunity to appear and be heard. Walker Decl., Ex.A, p.5. The Court and the parties specifically addressed the issue of staying these proceedings. Walker Decl. ¶ 5. On September 14, 2012, the Court issued a Case Management Order (CMO) that set the trial date for June 24, 2013. Docket # 350.

Also on September 4, 2012, ALJ Gildea issued Order No. 3 in TPL's ITC case, outlining a proposed trial schedule and setting the hearing date for June 3, 2012. Declaration of James C. Otteson in support of Motion to Continue (Otteson Decl.), ¶ 4. On October 1, 2012, ALJ Gildea issued Order No. 7, confirming the hearing date of June 3-14, 2013. *Id.* On December 12, 2012, TPL filed this Motion to Continue Trial Date to October 2013. Doc. 383. Thus, TPL knew prior to the CMC in this case the timing of the ITC hearing and post-trial briefing schedule.

ARGUMENT

A. TPL Fails to Show Good Cause to Continue the Trial Date

1. TPL failed to diligently pursue a continuance.

TPL relies on a purported scheduling conflict as good cause to continue the trial date. Mot. pp. 1:16-17, 3:12-16. But TPL has known of the "conflict" between the trial in this case and post-trial briefing in its ITC case for over seventy days. ALJ Gildea notified the parties of the hearing date on September 4, and issued a final scheduling order on October 1, 2012, yet TPL waited until December 12, 2012 to file its motion for a continuance. *Id.* TPL offers no explanation for this two month delay. Mot. pp. 1:16-17, 3:12-16. The only substantive

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et al. 08-05398-PSG; *HTC v. Technology Properties Ltd., et al.* 08-00882-PSG. The *Barco* case was recently dismissed.

development since October 1, 2012, was this Court's December 4, 2012 Order regarding claim construction issues. Docket # 381. TPL's delay in seeking a continuance and failure to explain the reasons for that delay undercuts the supposed urgency with which it now seeks to prevent this case from going to trial as scheduled.

2. The purported "conflict" does not warrant a four month continuance.

The purported conflict is not a sufficient basis for any continuance, and no basis whatsoever for the four month continuance sought. The ITC hearing and the trial of this action are set for different times. The ITC hearing is scheduled to conclude on June 14, 2013, 10 days before the trial date in this case. Counsel for TPL is not required to be in two places at once; nor are any witnesses required to be in two places at once.

Instead, as virtually all busy lawyers must do, counsel for TPL and Acer must plan to do some briefing in another matter while the current case is being tried. That the other matter is related really has no bearing on the merits of TPL's request. There has been no adequate showing that it is unreasonable to expect TPL to find a way to staff the post-trial briefing for another matter 6 months from now.[2] Indeed, TPL *has* engaged the assistance of additional counsel in a separate ITC investigation, which also involves Acer. Walker Decl., ¶ 6. There is no justifiable reason why it cannot do the same here.

Even if some relief were justified, a four months delay is not. TPL's motion is explicit that the four month continuance is not just to clear post-trial briefing but also to allow the ITC to reach a decision. Mot. p. 4:21-22. TPL's request is a bald effort to put TPL's action in its preferred forum—the ITC—ahead of the forum Acer chose first, the Northern District of California. This is a replay of TPL's earlier effort to change venue to the Eastern District of Texas based on a later-filed complaint, and it should again be rejected.

[2] TPL complains about the perceived difference in resources among the parties, ignoring that it was TPL, not Acer, that chose to bring the ITC action. This argument is also disingenuous, failing to tell the Court the amount of royalties (allegedly in excess of $300 million dollars) TPL claims to have collected on the asserted patents. Walker Decl., Ex.B.

TPL illogically argues that allowing the ITC to reach a decision will somehow narrow the issues for trial in this case, but admits that in fact the ITC action will have no preclusive effect on this action. Mot. p. 4:23-5:3. Since the ITC action has no preclusive effect, it cannot narrow any issues in this case.

3. Past delays are not a basis for additional delays.

TPL attempts to rely on past delays as somehow providing good cause for a new delay. Mot. p. 4:10-18. If anything, the past delays make timely resolution of this case more urgent.

TPL accuses Acer of intentionally delaying the prosecution of its own case. *Id.* at 4:12-14. TPL mischaracterizes the stay for reexaminations, and its argument that that stay somehow justifies a further continuance is without merit. The only examples of delay that TPL provides are the reexamination requests (by parties other than Acer) and the corresponding motion to stay. *Id.* Acer made the motion to stay before a trial date was set and before even a claim construction hearing was set. Walker Decl., ¶ 3. Moreover, the purpose of that stay was to narrow the scope of the claims. This is consistent with judicial policy in favor of issuing stays pending reexamination where the case is in the initial stages of litigation and there has been little discovery. *ASCII Corp. v. STD Enm't USA, Inc.*, 844 F. Supp. 1378, 1381 (N.D. Cal. 1994). Indeed, the reexaminations resulted in claims being canceled and amended. Walker Decl., Exs.C, D, E and F.

Moreover, TPL has introduced its share of delays to this case. For example, as noted above, this case was delayed for six months while TPL fought venue. At the first case management conference after filing the ITC complaint, TPL sought an extended schedule. Walker Decl., Ex.A, Joint Case Management Conference Statement, pp. 4:8-5:10, Docket # 346. The Court should deny TPL's latest dilatory tactic and deny its motion for a continuance.

4. A continuance based on the overlapping schedule with the ITC case is inconsistent with the policy of 28 U.S.C. § 1659.

Granting a continuance at the request of TPL due to the alleged burden of simultaneously litigating the same patent in the ITC is inconsistent with the policy of 28 U.S.C. § 1659. As TPL correctly recognizes, Section 1659 only allows a *respondent* to an ITC investigation to seek a

stay of any related proceedings in the district courts. Mot. p. 4:2-6. Section 1659 does not permit a petitioner to seek a stay. Congress did not see fit to protect an ITC petitioner from the self-inflicted burdens of conflicting schedules between the ITC and a related district court action. This Court should likewise deny TPL's attempt to continue these proceedings simply to avoid a conflict of its own making.

C. A Continuance Will Prejudice Acer

This case will have been on the Court's docket for more than five years by the time the parties finally go to trial in June 2013. TPL's new proposed delay will prejudice Acer by moving the decision at the ITC ahead of a verdict in this action. Acer has waited more than four years to try this case. It should not be made to wait any longer.

CONCLUSION

TPL has not shown good cause to continue the trial date where the conflict at issue is of its own design and does not require anyone to be in two places at the same time. To the extent that this Court decides that any schedule change may be warranted, however, it should not change the schedule without first holding an additional Case Management Conference so the parties can be fully heard on the scope of any time extensions and the impact to the trial schedule.

Dated: December 17, 2012

K&L GATES LLP

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC.,

Plaintiffs,

v.

TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED,

Defendants.

TECHNOLOGY PROPERTIES LIMITED and PATRIOT SCIENTIFIC CORPORATION,

Counterclaimants

v.

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC.,

Counterdefendants.

Case No. 5:08-cv-00877 JF

DECLARATION OF TIMOTHY P. WALKER IN SUPPORT OF PLAINTIFF ACER, INC.'S RESPONSE IN OPPOSITION TO DEFENDANTS' MOTION UNDER CIVIL LOCAL RULES 6-3 AND 7-11 TO CONTINUE TRIAL DATE AND CORRESPONDING DATES

I, Timothy P. Walker, declare:

1. I am an attorney licensed to practice law before all courts in the State of California, and the United States District Court for the Northern District of California. I am a partner at K&L Gates LLP in its San Francisco, California office, and I, along with other attorneys at K&L Gates LLP, am attorney of record for Acer Inc., Acer America Corporation and Gateway, Inc. (collectively "Plaintiffs" or "Acer"). Pursuant to Local Rule 6-3(b), I submit this declaration in support of Acer, Inc.'s Response in Opposition to Defendants' Motion Under Civil Local Rules 6-3 and 7-11 to Continue Trial Date and Corresponding Dates ("Motion to Continue").

2. I have personal knowledge of the matters set forth herein and if called as a witness could competently testify thereto.

3. While this action was pending before Judge Fogel, Acer made a motion to stay this action pending reexaminations of the patents in suit. At the time of making the motion for stay, no trial date was set and no claim construction hearing was set.

4. Attached as Exhibit A is a copy of the joint case management conference statement filed by the parties before the September 4, 2012 case management conference.

5. I attended the September 4, 2012 case management conference in this action. Among the issues discussed was the ITC action filed by TPL and whether Acer, HTC or Barco would stipulate to a stay until the ITC action was resolved. None of Acer, HTC or Barco agreed to a stay.

6. TPL has associated the Simon Law Firm P.C. to provide assistance in its separate and related ITC investigation, 337-TA-841. That case also involves Acer.

7. TPL's ITC complaint (public version) alleges that its MMP licensing program has generated in excess of $300 million dollars in licensing fees to date. Attached as Exhibit B is a copy of the portion of TPL's ITC complaint that sets forth that allegation.

8. Attached hereto as Exhibit C is a copy of the reexamination certificate of the '336 patent.

9. Attached hereto as Exhibit D is a copy of the reexamination certificate of the '749 patent.

10. Attached hereto as Exhibit E is a copy of the reexamination certificate of the '148

patent.

11. Attached hereto as Exhibit F is a copy of the reexamination certificate of the '890 patent.

I declare under penalty of perjury pursuant to the laws of the United States that the foregoing is true and correct.

Executed on December 17, 2012, at San Francisco, California.

By: /s/ Timothy P. Walker
Timothy P. Walker

Exhibit A

[See Signature Page for Information on Counsel for Plaintiffs and Defendants]

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00877 PSG **JOINT CASE MANAGEMENT CONFERENCE STATEMENT** [RELATED CASES] Date: September 4, 2012 Time: 2:00 pm. Dept: Courtroom 5, 4th Floor Judge: Hon. Paul S. Grewal
HTC CORPORATION, HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00882 PSG
BARCO N.V., a Belgian corporation, Plaintiff, v. TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORP., ALLIACENSE LTD., Defendants.	Case No. 5:08-cv-05398 PSG

The parties from the three above-captioned actions, Plaintiffs Acer Inc., Acer America Corp., and Gateway, Inc. (collectively "Acer"), HTC Corporation and HTC America Inc. (collectively "HTC") and Barco, N.V. ("Barco"), and Defendants Technology Properties Limited, Patriot Scientific Corporation, and Alliacense Limited (collectively "TPL" or "Defendants"), respectfully submit this Joint Case Management Conference Statement ("CMC Statement") pursuant to the Court's August 21, 2012 order (Docket No. 344 in the *Acer* action) setting the case management conference on September 4, 2012.

I. PROCEDURAL HISTORY AND PATENTS-IN-SUIT

Acer and HTC filed their respective declaratory judgment actions on February 8, 2008, while Barco filed its declaratory judgment action on December 1, 2008 as follows:

(1) The *Acer* Action (Case No. 5:08-cv-00877);

(2) The *HTC* Action (Case No. 5:08-cv-00882); and

(3) The *Barco* Action (Case No. 5:08-cv-05398).

All three actions above were related and originally assigned to Judge Fogel. Upon Judge Fogel's departure in October 2011, this case was reassigned to Chief Judge Ware. Because of Judge Ware's pending retirement in August 2012, this case has now been reassigned to this Court per consent of the parties.

The four Patents-in-Suit in the *Acer* and *HTC* actions are U.S. Patent Nos. 5,809,336 (the "'336 Patent"), 5,440,749 (the "'749 Patent"), 5,530,890 (the "'890 Patent") and 6,598,148 (the "'148 Patent") (collectively "Patents-in-Suit"). Three of the four patents—the '336 Patent, the '749 Patent, and the '890 Patent—are at issue in the *Barco* action.

The four Patents-in-Suit, which share the same specification, are directed to different aspects of a microprocessor system. Generally speaking, the '336 Patent is directed to the microprocessor system's clocking mechanisms, while the '749 and '890 Patents are directed to the microprocessor system's architectural features. The '148 Patent generally relates to the microprocessor system's memory.

II. CURRENT STATUS OF THE CASE

The actions are currently in the claim construction stage. Judge Ware conducted a

Markman hearing in January 2012 on ten claim terms. On June 12, 2012, Judge Ware issued a First Claim Construction Order (*Acer* Dkt. No. 336). In the Order, Judge Ware requested supplemental briefing with respect to two of the terms. There may be other unresolved claim construction issues, and the parties may seek clarification or reconsideration on certain terms.

On July 2, 2012 and pursuant to the First Claim Construction Order, the parties submitted a further Joint Statement regarding competing proposals for the supplemental claim construction briefing and possible discovery. (*Acer* Dkt. No. 337). However, Judge Ware did not issue any order regarding further claim construction briefing before the reassignment to this Court. The Parties' Proposed Schedule in the section below therefore includes a proposed briefing schedule for the supplemental briefs specified in the First Claim Construction Order.

On July 24, 2012, Defendants filed eleven additional suits in this District, asserting infringement of three of the four Patents-in-Suit (the '749, '890, and '336 patents). Thus, in total, there are fourteen separate actions pending in this District involving at least these three patents.

On August 24, 2012, the U.S. International Trade Commission ("ITC") published in the Federal Register its intention to institute an investigation of infringement of the '336 patent by thirteen of the fourteen parties to the pending district court actions. *See* 77 FR 51572 (Investigation No. 337-TA-853). In addition to Acer and HTC, the ITC respondents include Amazon.com, Barnes & Noble, Garmin, Huawei, Kyocera, LG Electronics, Nintendo, Novatel Wireless, Samsung, Sierra Wireless, and ZTE.

III. PARTIES' PROPOSED SCHEDULE

The parties have met and conferred, and hereby largely agree on a schedule for the remainder of the claim construction briefing (save for one disagreement over the need for additional expert depositions). However, Defendants believe that judicial economy would be best served by waiting for the defendants in the newly-filed actions to answer the complaints, and possibly consolidating these matters for purposes of discovery and claim construction.

A. Plaintiffs' Position.

Plaintiffs believe that judicial economy would not be best served by waiting for the defendants in the newly-filed actions for several reasons. First, Plaintiffs' declaratory judgment

("DJ") actions have been pending for over four and a half years – they are entitled to have the pending issues in their DJ actions, including claim construction, resolved in a timely manner without having to wait for ***eleven*** additional groups of accused infringers to catch up to the schedule. Plaintiffs have already expended enormous resources to have their DJ actions resolved, and waiting months or a year longer would unfairly prejudice Plaintiffs and burden them with additional litigation expenses while awaiting the coordination of eleven separate actions.

Second, clarification and additional construction by this Court on the remaining claim terms would actually improve judicial economy by narrowing the issues in the subsequently filed actions, likely encouraging informal resolution due to the certainty provided by additional claim construction from this Court.

Third, Plaintiffs believe that it would be improper to consolidate the newly-filed actions because the current actions are far enough along that further delay would be prejudicial to the existing parties to the litigation. The newly added accused infringers sell a diversity of products that bear little relationship to the products accused in Plaintiffs' DJ actions. The parties in the DJ actions have all agreed to the Magistrate Judge for all proceedings, whereas the additional eleven accused infringer groups may not do so, thus making consolidation speculative at best, even if permissible. *See Body Science LLC v. Boston Scientific Corp.*, 846 F. Supp.2d 980, 991 (N.D. Ill. Mar. 2012) (refusing to consolidate cases where there were a multitude of different products and determining that consolidation would not promote judicial economy or efficiency); *see also One-E-Way Inc. v. Plantronics Inc. et al.*, 2:11-cv-06673, Dkt. No. 80 at 2 (CD Cal. January 19, 2012) (finding that consolidation was inappropriate because "the defendants – who may have competing interests and strategies – also are entitled to present individualized assaults on questions of non-infringement, invalidity, and claim construction").

Fourth, the remaining claim construction issues are narrow and readily resolvable by the Court.[1] The issues can readily be briefed by the parties already in the DJ actions, and have been

[1] The claim construction issues that remain for resolution were raised in claim construction briefs filed in late 2010 and early 2011, when the case was before Judge Fogel. The case was subsequently reassigned to Judge Ware, and then upon his retirement, to this court. These events were out of the control of Plaintiffs, but the effect of these events has been an undue delay in

largely identified in Judge Ware's First Claim Construction Order. There would not be significant resources spent resolving these remaining claim construction issues.

Should the Court be inclined to stay further claim construction for months to see if the cases can be consolidated and a joint scheduled reached, it should be on the condition that TPL agree to waive past damages from the time of filing of the newly filed actions. Otherwise, the current Plaintiffs would be prejudiced by ongoing delay in the resolution of their DJ actions and face continued uncertainty as to their rights.

B. Defendants' Position.

Plaintiffs misunderstand Defendants' proposal. As shown by the proposed schedule below, Defendants are amenable to this Court taking up claim construction issues left open by Judge Ware; indeed, Defendants stipulated to having this Court do just that.

However, there are now eleven new cases involving the same patents, the same claim construction issues, and the same invalidity defenses. The risk of inconsistent rulings and substantial duplication of judicial effort cannot be ignored. *See Interactive Fitness Holdings, LLC v. Icon Health & Fitness, Inc.*, 10-CV-04628 LHK, 2011 WL 1302633, at *3 (N.D. Cal. April 5, 2011) (granting motion to transfer to avoid duplicative and potentially inconsistent claim construction and infringement analyses that would inevitably result); *see also Micron Tech. Inc. v. Rambus Inc.*, 645 F.3d 1311 (Fed. Cir. 2011) and *Hynix Semiconductor Inc. v. Rambus Inc.*, 645 F.3d 1336 (Fed. Cir. 2011) (attempting to reconcile inconsistent factual determinations by two district courts but ultimately remanding for further proceedings). For this reason, the Federal Circuit has observed that "judicial economy plays a paramount role in trying to maintain an orderly, effective, administration of justice and having one trial court decide all of these claims clearly furthers that objective." *In re Google, Inc.*, 412 F. App'x 295, 296 (Fed. Cir. 2011).

Consequently, the parties propose the following schedule with disagreements noted by shading:

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resolving the parties' well-distilled claim construction disputes. Further delay would unduly prejudice Plaintiffs.

Event	Date	
Exchange of expert declarations for supplemental briefing	Sept. 14, 2012	
Completion of expert discovery	**Plaintiffs** Sept. 28, 2012	**Defendants** Defendants do not believe that further expert depositions are necessary or helpful. The experts have already been deposed on claim construction issues.
Exchange of opening supplemental claim construction briefs	October 5, 2012	
Exchange of responsive supplemental claim construction briefs	October 26, 2012	
Tutorials and hearing, if ordered by the Court	Approximately 15 days after exchange of responsive supplemental claim construction briefs	
Final infringement contentions[2]	**Plaintiffs** 30 days after the final claim construction ruling	**Defendants** Defendants believe judicial economy will be served by waiting until the defendants in the newly-filed cases have had the opportunity to appear and be heard
Final invalidity contentions[3]	50 days after the final claim construction ruling	
Defendants to serve willfulness documents; opinion of counsel		

[2] [2] These two deadlines for final infringement and final invalidity contentions only apply to case nos. 5:08-cv-0877 (*Acer v. TPL*) and 5:08cv-0882 (*HTC v. TPL*). Case no. 5:08-cv-05398 (*Barco v. TPL*) was filed in December 2008 and operates under the Patent Local Rules that were in effect after March 2008, which do not provide for final infringement or invalidity contentions absent leave from Court.

Event	Date
Close of fact discovery	Six months after the final invalidity contentions
Initial expert reports	30 days after the close of fact discovery
Rebuttal expert reports	30 days after the initial expert reports
Close of expert discovery	Two weeks after the rebuttal expert reports
Trial	To be determined

IV. LEGAL ISSUES

The principal legal issues that the Parties dispute are:

a. The construction of the claims of the Patents-in-Suit;

b. Whether the Plaintiffs infringe any of the Patents-in-Suit;

c. Whether any infringement by Plaintiffs, if proven, was willful;

d. Whether the Patents-in-Suit are invalid and/or unenforceable; and

e. Whether Intervening Rights are applicable due to amendments to the asserted claims during reexamination of the Patents-In-Suit.

f. The amount of damages, if any, due to Defendants and potential entry of an injunction.

V. MOTIONS AND ANTICIPATED MOTIONS

Barco previously filed a motion for summary judgment of non-infringement of the '336 Patent on December 1, 2010. (*Barco* Dkt. No. 112.) Judge Fogel subsequently denied the motion without prejudice on March 8, 2011. (*Barco* Dkt. No. 167.)

HTC previously filed a motion for partial summary judgment of non-infringement of the '749, the '336 and the '148 Patents on April 8, 2011 prior to claim construction. (*HTC* Dkt. No. 293.) The motion was subsequently denied by Judge Ware as premature and without prejudice to

renewal after claim construction. (*HTC* Dkt. No. 361.)

Plaintiffs will be renewing these motions and will be filing additional motions for summary judgment following the resolution of outstanding claim construction disputes.

VI. AMENDMENT OF PLEADINGS

The parties do not anticipate filing any further amended pleadings at this time.

VII. EVIDENCE PRESERVATION

All parties have been advised by their counsel to preserve all relevant evidence, including electronically stored information, if any.

VIII. DISCLOSURES

The parties have complied with the initial disclosure requirements of Fed. R. Civ. P. 26.

IX. CLASS ACTIONS

This is not a class action case.

X. RELATED CASES THAT HAVE BEEN RESOLVED

(1) The ASUSTeK Action (Case No. 5:08-cv-00884); and

(2) The Sirius XM Action (Case No. 3:10-cv-00816).

XI. RELIEF

Plaintiffs seek a declaratory judgment against Defendants that they do not infringe any asserted claim of the Patents-in-Suit, and that the asserted claims are invalid and/or unenforceable. Defendants seek damages for alleged patent infringement and injunctive relief.

XII. SETTLEMENT AND ADR

Acer, HTC and TPL have engaged in mediation, but have not settled the disputes to date. *See Acer* Dkt. No. 49 and *HTC* Dkt. No. 50. Barco was exempted from the mediation process. *See Barco* Dkt. No. 53.

XIII. CONSENT TO MAGISTRATE JUDGE FOR ALL PURPOSES

The Parties have jointly consented to Magistrate Judge Grewal for all further proceedings including trial and entry of judgment. (*See Acer* Dkt. No. 339.)

XIV. OTHER REFERENCES

The parties do not believe that this case is suitable for reference to binding arbitration, a

special master, or the Judicial Panel on Multidistrict Litigation.

XV. NARROWING OF ISSUES

The Parties anticipate filing one or more dispositive motions, such as motions for summary judgment, seeking to narrow the issues in this case.

XVI. EXPEDITED SCHEDULE

The Parties agree that this case is not suitable for expedited handling at this time.

XVII. TRIAL

The case will be tried to a jury. Parties expect the duration of the trial will depend on numerous factors, including the dispositions of the pending and anticipated summary judgment motions that cannot be determined at this stage of the proceedings.

XVIII. DISCLOSURE OF NON-PARTY INTERESTED ENTITIES OR PERSONS

The Parties have filed Corporate Disclosure Statements pursuant to Fed. R. Civ. P. 7-1.

XIX. STATUS OF DISCOVERY

The parties have conducted claim construction discovery and are engaged in fact discovery. Defendants have also initiated discovery with a number of third-party suppliers, including some foreign-based third-parties. Given the complexity of the issues in this case, it is expected that additional document and deposition discovery will be needed after the issuance of the claim construction order. The parties have previously agreed to close fact discovery six months after the final invalidity contentions are due, which must be served 50 days after the issuance of the final claim construction order. (*See*, *e.g.*, *Acer* Dkt. No. 288.)

XX. OTHER MATTERS

There are no other matters that the parties believe need to be addressed at this time.

Respectfully submitted,

[SIGNATURE BLOCKS START ON THE NEXT PAGE]

Dated: August 28, 2012

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ATTESTATION PER GENERAL ORDER 45

I, Harold H. Davis, am the ECF User whose ID and password are being used to file this Joint Case Management Conference Statement. In compliance with General Order 45, X.B., I hereby attest that the counsel listed above have concurred with this filing.

Dated: August 28, 2012

By: /s/ Harold H. Davis /s/

Attorneys for Acer, Inc., Acer America Corp. and Gateway, Inc.

Exhibit B

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

In the Matter of **CERTAIN WIRELESS CONSUMER ELECTRONICS DEVICES AND COMPONENTS THEREOF**	**Investigation No. 337-TA-_____**

COMPLAINT OF TECHNOLOGY PROPERTIES LIMITED LLC UNDER SECTION 337 OF THE TARIFF ACT OF 1930, AS AMENDED

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160. TPL has contacted over four hundred (400) potential licensees in furtherance of the licensing of its MMP Portfolio, which includes the Asserted Patent. Hannah Decl., ¶ 24 & Confidential Exhibit 39-K. TPL has also been successful in licensing the MMP Portfolio. Hannah Decl., ¶ 25. As evidence of the success of TPL's licensing program, a list of entities licensed under the MMP Portfolio, including the Asserted Patent, is attached to the Hannah Decl. *See* Hannah Decl., ¶ 25 & Confidential Exhibit 39-L. The MMP licensing program has generated in excess of $300 million in licensing fees to date. Hannah Decl., ¶ 25.

161. As required by Commission precedent, including *Multimedia Display*, 337-TA-694 (Comm'n Opin., July 22, 2011), there is a strong nexus between the asserted '336 Patent and TPL's substantial domestic investments in the licensing of its MMP Portfolio.

162. The '336 Patent is closely related to the other patents in the MMP Portfolio. This demonstrates that the Asserted Patent fits together congruently with the other patents in the MMP Portfolio because they all cover specific fundamental microprocessor technology. The majority of the MMP Portfolio, including the '336 Patent, resulted from one fundamental patent application: Application No. 07/389,334, filed on August 3, 1989, which issued on August 8, 1995 as U.S. Patent No. 5,440,749 ("the '749 Patent").

163. The inventors of the '749 Patent were Charles H. Moore and Russell H. Fish III. The application for the '749 Patent is an "ancestor" application for the '336 Patent, and both share the same specification. The '336 Patent includes the same two inventors as the '749 Patent. In addition, the '749 application is an "ancestor" application for all the other issued U.S. patents in the MMP Portfolio. Thus, the '336 Patent is closely related to all of the other issued U.S. patents in the MMP Portfolio.

164. As discussed above, the Asserted Patent is directed to technology that is closely related to the subject matter of the other MMP patents. The '336 Patent teaches the use of two independent clocks in a microprocessor system: (1) an on-chip first clock to time the CPU; and (2) a second independent clock to time the input/output (I/O) interface, which allows the clocks

Exhibit C

US005809336C1

(12) EX PARTE REEXAMINATION CERTIFICATE (7235th)

United States Patent

Moore et al.

(10) Number: US 5,809,336 C1

(45) Certificate Issued: Dec. 15, 2009

(54) **HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK**

(75) Inventors: **Charles H. Moore**, Woodside, CA (US); **Russell H. Fish, III**, Mt. View, CA (US)

(73) Assignee: **Patriot Scientific Corporation**, San Diego, CA (US)

Reexamination Request:
No. 90/008,306, Oct. 19, 2006
No. 90/008,237, Nov. 17, 2006
No. 90/008,474, Jan. 30, 2007

Reexamination Certificate for:
Patent No.: **5,809,336**
Issued: **Sep. 15, 1998**
Appl. No.: **08/484,918**
Filed: **Jun. 7, 1995**

Certificate of Correction issued May 22, 2007.

Related U.S. Application Data

(62) Division of application No. 07/389,334, filed on Aug. 3, 1989, now Pat. No. 5,440,749.

(51) **Int. Cl.**

G06F 7/76	(2006.01)
G06F 7/48	(2006.01)
G06F 12/08	(2006.01)
G06F 7/78	(2006.01)
G06F 9/30	(2006.01)
G06F 9/32	(2006.01)
G06F 15/76	(2006.01)
G06F 15/78	(2006.01)
G06F 7/52	(2006.01)
G06F 9/38	(2006.01)
G06F 7/58	(2006.01)

(52) **U.S. Cl.** **710/25**; 711/E12.02; 712/E9.016; 712/E9.028; 712/E9.046; 712/E9.055; 712/E9.057; 712/E9.058; 712/E9.062; 712/E9.078; 712/E9.08; 712/E9.081

(58) **Field of Classification Search** ..... None
See application file for complete search history.

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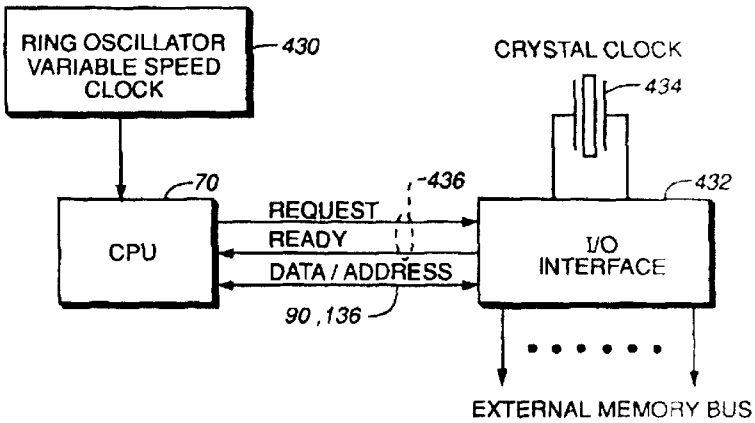
Plaintiffs Technology Property Limited's and Patriot Scientific Corporation's Claim Construction Brief filed Mar. 19, 2007 in 2:05–CV–494 (TJW).

(Continued)

Primary Examiner—Sam Rimell

(57) **ABSTRACT**

A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.



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EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

ONLY THOSE PARAGRAPHS OF THE SPECIFICATION AFFECTED BY AMENDMENT ARE PRINTED HEREIN.

Column 17, lines 12–37:

Most microprocessors derive all system timing from a single clock. The disadvantage is that different parts of the system can slow all operations. The microprocessor **50** provides a dual-clock scheme as shown in FIG. **17**, with the CPU **70** operating **[**a synchronously**]** *asynchronously* to I/O interface **432** forming part of memory controller **118** (FIG. **2**) and the I/O interface **432** operating synchronously with the external world of memory and I/O devices. The CPU **70** executes at the fastest speed possible using the adaptive ring counter clock **430**. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor **50** for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface **432**, speed of which is controlled by a conventional crystal clock **434**. The interface **432** processes requests for memory accesses from the microprocessor **50** and acknowledges the presence of I/O data. The microprocessor **50** fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access. By decoupling the variable speed of the CPU **70** from the fixed speed of the I/O interface **432**, optimum performance can be achieved by each. Recoupling between the CPU **70** and the interface **432** is accomplished with handshake signals on lines **436**, with data/addresses passing on bus **90**, **136**.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

Claims **3**–**5** and **8** are cancelled.

Claims **1**, **6** and **10** are determined to be patentable as amended.

Claims **2**, **7** and **9**, dependent on an amended claim, are determined to be patentable.

New claims **11**–**16** are added and determined to be patentable.

1. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, *wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.*

6. A microprocessor system comprising:

a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an *off-chip* external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an *off-chip* external clock, independent of said oscillator, connected to said input/output interface wherein said *off-chip* external clock is operative at a frequency independent of a clock frequency of said oscillator *and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.*

10. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an **[**on chip**]** *on-chip* input/output interface between said central processing unit and an *off-chip* external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an *off-chip* external clock wherein said *off-chip* external clock is operative at a frequency independent of a clock frequency of said variable speed clock *and wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock.*

11. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein said central processing unit operates asynchronously to said input/output interface.

12. The microprocessor system of claim 11, in which said second clock is a fixed frequency clock.

13. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;

an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and further wherein said central processing unit operates asynchronously to said input/output interface.

14. The microprocessor system of claim 13 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

15. The microprocessor system of claim 13 wherein said oscillator comprises a ring oscillator.

16. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock, wherein said central processing unit operates asychronously to said input/output interface.

* * * * *

US005809336C2

(12) EX PARTE REEXAMINATION CERTIFICATE (7887th)

United States Patent
Moore et al.

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(45) **Certificate Issued: Nov. 23, 2010**

(54) **HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK**

(75) Inventors: **Charles H. Moore**, 410 Star Hill Rd., Woodside, CA (US) 94062; **Russell H. Fish, III**, Mt. View, CA (US)

(73) Assignee: **Charles H. Moore**, Incline Village, NV (US)

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(51) **Int. Cl.**

G06F 7/76	(2006.01)
G06F 7/48	(2006.01)
G06F 12/08	(2006.01)
G06F 7/78	(2006.01)
G06F 9/30	(2006.01)
G06F 9/32	(2006.01)
G06F 15/76	(2006.01)
G06F 15/78	(2006.01)
G06F 7/52	(2006.01)
G06F 9/38	(2006.01)
G06F 7/58	(2006.01)

(52) **U.S. Cl.** **710/25**; 711/E12.02; 712/E9.016; 712/E9.028; 712/E9.046; 712/E9.055; 712/E9.057; 712/E9.058; 712/E9.062; 712/E9.078; 712/E9.08; 712/E9.081

(58) **Field of Classification Search** ..... None
See application file for complete search history.

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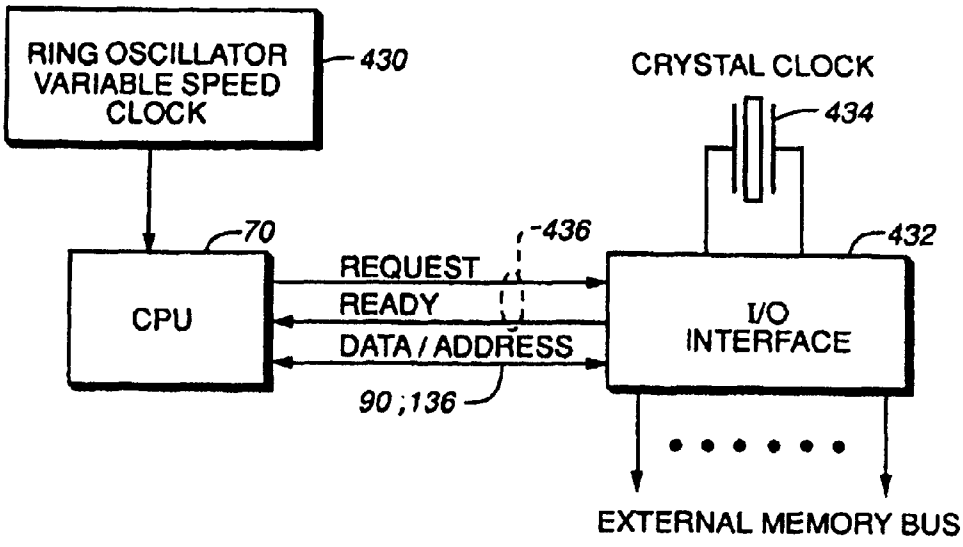
Primary Examiner—B. James Peikari

(57) **ABSTRACT**

A high performance, low cost microprocessor system having a variable speed system clock is disclosed herein. The microprocessor system includes an integrated circuit having a central processing unit and a ring oscillator variable speed system clock for clocking the microprocessor. The central processing unit and the ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface connected to exchange coupling control signals, address and data with the central processing unit. The input/output interface is independently clocked by a second clock connected thereto.



EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

NO AMENDMENTS HAVE BEEN MADE TO THE PATENT

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claims **1**, **2**, **6**, **7** and **9-16** is confirmed.

Claims **3-5** and **8** were previously cancelled.

* * * * *

Exhibit D

US005440749C1

(12) EX PARTE REEXAMINATION CERTIFICATE (8294th)

United States Patent

Moore et al.

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(54) **HIGH PERFORMANCE, LOW COST MICROPROCESSOR ARCHITECTURE**

(75) Inventors: **Charles H. Moore**, Woodside, CA (US); **Russell H. Fish, III**, Mt. View, CA (US)

(73) Assignee: **Charles H. Moore**, Incline Village, NV (US); TTE, UTD 3/21/2006 The Equinox Trust

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G06F 9/40 (2006.01)

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(58) **Field of Classification Search** ..... None
See application file for complete search history.

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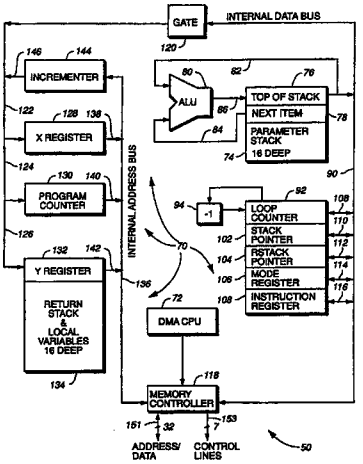
(57) **ABSTRACT**

A microprocessor (**50**) includes a main central processing unit (CPU) (**70**) and a separate direct memory access (DMA) CPU (**72**) in a single integrated circuit making up the microprocessor (**50**). The main CPU (**70**) has a first 16 deep push down tack (**74**), which has a to item register (**76**) and a next item register (**78**), respectively connected to provide inputs to an arithmetic logic unit (ALU) (**80**) by lines (**82**) and (**84**). An output of the ALU (**80**) is connected to the top item register at (**82**) is also connected by line (**88**) to an internal data bus (**90**). CPU (**70**) is pipeline free. The simplified CPU (**70**) requires fewer transistors to implement than pipelined architectures, yet produces performance which matches or exceeds existing techniques. The DMA CPU (**72**) provides inputs to the memory controller (**118**) on line (**148**). The memory controller (**118**) is connected to a RAM by address/data bus (**150**) and control lines (**152**). The DMA CPU (**72**) enables the CPU (**70**) to execute instructions four times faster than the RAM speed by fetching four instructions in a single memory cycle.



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EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claims **21-29** is confirmed.

Claims **8** and **9** are cancelled.

Claims **1**, **5**, **7**, **10**, **13**, **18** and **19** are determined to be patentable as amended.

Claims **2-4**, **6**, **11**, **12**, **14-17** and **20**, dependent on an amended claim, are determined to be patentable.

New claims **30** through **59** are added and determined to be patentable.

1. A microprocessor system, comprising a central processing unit integrated circuit, a memory external of said central processing unit integrated circuit, a bus connecting said central processing unit integrated circuit to said memory, and means connected to said bus for fetching instructions for said central processing unit integrated circuit on said bus from said memory, said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle, said bus having a width at least equal to a number of bits in each of the instructions times a number of the instructions fetched in parallel, said central processing unit *integrated circuit* including an arithmetic logic unit and a first push down stack connected to said arithmetic logic unit, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input and means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input, a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack, said arithmetic logic unit having an output connected to said means for storing a top item;

wherein

the microprocessor system comprises an instruction register configured to store the multiple sequential instructions and from which instructions are accessed and decoded; and wherein

the means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to the central processing unit integrated circuit during a single memory cycle comprises supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched.

5. The microprocessor system of claim **1** **[**additionally comprising an**]** *wherein said* instruction register for the multiple instructions *is* connected to said means for fetching instructions, means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession, means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions, said counter being connected to said means for decoding to receive incrementing and reset control signals from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and to supply a control signal to said means for fetching instructions in response to a SKIP instruction in the multiple instructions.

7. The microprocessor system of claim **1** **[**additionally comprising an**]** *wherein said* instruction register for the multiple instructions and a variable width operand to be used with one of the multiple instructions *is* connected to said means for fetching instructions, means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession,

means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions, said counter being connected to said means for decoding to receive incrementing and reset control signals from said means for decoding, said means for decoding being configured to control said counter in response to an instruction utilizing the variable width operand stored in said instruction register, and means connected to said counter to select the variable width operand for use with the instruction utilizing the variable width operand in response to said counter.

10. The microprocessor system of claim **[9]** *59* additionally comprising a second push down stack, said means for storing a top item being connected to provide an input to said second push down stack and a control means connected between said means for storing a top item and said second push down stack for controlling provision of the input to said second push down stack.

13. The microprocessor system of claim **12** **[**additionally comprising an**]** *wherein the* instruction register for the multiple instructions *is* connected to said means for fetching instructions, means connected to said instruction register for supply the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supplying the multiple instructions in succession, means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions, said counter being connected to said means for decoding to receive incrementing and reset control signals from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and to supply a control signal to said means for fetching instructions in response to a SKIP instruction in the multiple instructions.

18. The microprocessor system of claim **[9]** *59* additionally comprising a programmable read only memory contain-

ing instructions connected to said bus, means connected to said bus for fetching instructions for said central processing unit on said bus, said means for fetching instructions including means for assembling a plurality of instructions from said programmable read only memory, storing the plurality of instructions in said dynamic random access memory and subsequently supplying the plurality of instructions from said dynamic random access memory to said central processing unit on said bus.

19. The microprocessor system of claim **[9]** *59* additionally comprising a direct memory access processing unit having the capacity to request and execute instructions, said bus connecting said direct memory access processing unit to said dynamic random access memory, said dynamic random access memory containing instructions for said central processing unit and said direct memory access processing unit, said direct memory access processing unit being connected to means for fetching instructions for said central processing unit on said bus and for fetching instructions for said direct memory access processing unit on said bus.

30. The microprocessor system of claim 1 wherein said central processing unit integrated circuit includes a prefetch circuit configured to request a fetch of a next set of multiple sequential instructions when no unexecuted instruction in the instruction register requires a memory access.

31. The microprocessor system of claim 1 wherein said central processing unit integrated circuit is configured to access an operand located in a first instruction location of the instruction register in response to an instruction of the multiple sequential instructions in a second instruction location of the instruction register distinct from the first instruction location.

32. The microprocessor system of claim 31 wherein said central processing unit integrated circuit is configured to access the operand in response to an op-code of the instruction in the second instruction location.

33. The microprocessor system of claim 1 wherein the instruction register is configured to store the multiple sequential instructions in corresponding instruction locations including a particular location for storing an instruction to be executed, the central processing unit integrated circuit being configured to respond to content of an instruction of the multiple sequential instructions by accessing the particular location of the instruction register.

34. The microprocessor system of claim 33 wherein the central processing unit integrated circuit is configured to respond to content of the instruction of the multiple sequential instructions by accessing the particular location of the instruction register after the means for fetching fetches next multiple sequential instructions.

35. The microprocessor system of claim 33 wherein the central processing unit integrated circuit is configured to respond to content of the instruction of the multiple sequential instructions by accessing the first-execution location of the instruction register without the fetching means fetching next multiple sequential instructions.

36. The microprocessor system of claim 33 wherein the content is an op-code.

37. The microprocessor system of claim 1 wherein the multiple sequential instructions comprise a first plurality of sequential instructions arranged from beginning to ending positions of the first plurality of sequential instructions, the central processing unit integrated circuit being configured to respond to content of a first instruction of the first plurality of sequential instructions stored in said instruction register by accessing a second instruction in a second plurality of sequential instructions arranged from beginning to ending positions of the second plurality of sequential instructions, the second instruction being in the beginning position of the second plurality of sequential instructions.

38. The microprocessor system of claim 37 wherein the second plurality of sequential instructions is distinct from the first plurality of sequential instructions.

39. The microprocessor system of claim 37 wherein the second plurality of sequential instructions is the first plurality of sequential instructions and the first instruction is disposed in a position other than the beginning position of the first plurality of instructions.

40. The microprocessor system of claim 37 wherein the content is an op-code.

41. The microprocessor system of claim 1 wherein the instruction register has a plurality of instruction locations for storing the multiple sequential instructions according to an order, the plurality of instruction locations including a first location to be accessed before any other of the plurality of instruction locations, the central processing unit integrated circuit further including means for accessing a next instruction out of the order, the next instruction being located at the first location.

42. The microprocessor system of claim 1 wherein the instruction register has a plurality of instruction locations for storing the multiple sequential instructions, the plurality of instruction locations including a first location to be accessed before any other of the plurality of instruction locations, the central processing unit integrated circuit further including means, responsive to content of an instruction of the multiple sequential instructions in a location other than the first location, for accessing a next instruction at the first location.

43. The microprocessor system of claim 1 wherein said central processing unit integrated circuit a program counter comprising address bits, said fetching means configured to locate the multiple sequential instructions using the address bits from the program counter.

44. The microprocessor system of claim 43 wherein the address bits are a most significant bit portion from the program counter.

45. The microprocessor system of claim 44 wherein the central processing unit integrated circuit is configured to increment the address bits of the program counter after said means for fetching multiple sequential instructions fetches the multiple sequential instructions.

46. The microprocessor system of claim 44 wherein the most significant bit portion is 30 of 32 bits of the program counter.

47. The microprocessor system of claim 44 wherein the instruction register has a plurality of instruction locations for storing the multiple sequential instructions, and multiplexer means connected to said instruction register for selectively supplying multiple instructions from said instruction register.

48. The microprocessor system of claim 44 wherein the multiple sequential instructions comprise a first plurality of sequential instructions, the central processing unit integrated circuit being configured to respond to content of a first instruction of the first plurality of sequential instructions by accessing a second plurality of sequential instructions using an address specified by the address bits.

49. The microprocessor system of claim 48 wherein the second plurality of sequential instructions is distinct from the first plurality of sequential instructions.

50. The microprocessor system of claim 48 wherein the content is an op-code.

51. The microprocessor system of claim 44 wherein the instruction register has a plurality of instruction locations

ordered from a beginning instruction location to an ending instruction location, wherein the central processing unit integrated circuit is configured to respond to content in an instruction location other than the beginning instruction location by accessing the beginning instruction location.

52. The microprocessor system of claim 1 in which said microprocessor system is configured to provide different memory access timing for different storing capacity sizes of said external memory by including a sensing circuit and a driver circuit, and an output enable line connected between said external access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level after a memory read operation as a function of different capacitance on said bus as a result of the different storing capacity sizes of said external memory, said microprocessor system being configured so that driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

53. The microprocessor system of claim 52 in which the predetermined electrical level is a predetermined voltage.

54. The microprocessor system of claim 1 in which said microprocessor system is configured to operate at a variable clock speed; said microprocessor system additionally comprising a ring counter variable speed system clock connected to said central processing unit integrated circuit, said central processing unit integrated circuit and said ring counter variable speed system clock being provided in a single integrated circuit, said ring counter variable speed system clock being configured to provide different clock speed to said central processing unit integrated circuit as a result of transistor propagation delays, depending on at least one of temperature of said single integrated circuit, voltage and microprocessor fabrication process for said single integrated circuit.

55. The microprocessor system of claim 54 additionally comprising an input/output interface connected between said microprocessor system and an external memory bus to exchange coupling control signals, addresses and data between said central processing unit integrated circuit and said input/output interface, and a second clock independent of said ring counter variable speed system clock connected to said input/output interface to provide clock signals for operation of said input/output interface asynchronously from said central processing unit.

56. The microprocessor system of claim 55 in which said second clock is a fixed frequency clock.

57. The microprocessor system of claim 1 in which said first push down stack has a first plurality of stack registers having stack memory elements configured as latches, a second plurality of stack registers having stack memory elements configured as a random access memory, said first and second plurality of stack registers and said central processing unit integrated circuit being provided in a single integrated circuit with a top one of said second plurality of stack registers being connected to said a bottom one of said first plurality of stack registers, and a third plurality of stack registers having stack memory elements configured as a random access memory external to said single integrated circuit, with a top one of said third plurality of stack registers being connected to a bottom one of said second plurality of stack registers, said microprocessor system being configured to operate said first, second and third plurality of stack registers hierarchically as interconnected stacks.

58. The microprocessor system of claim 57 additionally comprising a first pointer connected to said first plurality of stack registers, a second pointer connected to said second plurality of stack registers, and a third pointer connected to said third plurality of stack registers, said microprocessor system being configured to operate said first, second and third plurality of stack registers hierarchically as interconnected stacks by having said central processing unit integrated circuit being connected to pop items from said first plurality of stack registers, said first stack pointer being connected to said second stack pointer to pop a first plurality of items from said second plurality of stack registers when said first plurality of stack registers are empty from successive pop operations by said central processing unit, said second stack pointer being connected to said third stack pointer to pop a second plurality of items from said third plurality of stack registers when said second plurality of stack registers are empty from successive pop operations by said central processing unit.

59. The microprocessor system of claim 9 wherein the microprocessor system comprises an instruction register configured to store the multiple sequential instructions and from which instructions are accessed and decoded; and wherein

the means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to the central processing unit during a single memory cycle comprises supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched.

* * * * *

Exhibit E

US006598148C1

(12) EX PARTE REEXAMINATION CERTIFICATE (8511th)

United States Patent
Moore et al.

(10) **Number: US 6,598,148 C1**
(45) **Certificate Issued: Sep. 6, 2011**

(54) **HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK**

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(73) Assignee: **Charles H. Moore**, Incline Village, NV (US); TTE, UTD March 21, 2006 The Equinox Trust

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(51) **Int. Cl.**
G06F 15/00 (2006.01)

(52) **U.S. Cl.** **712/32**; 711/E12.02; 712/E9.016; 712/E9.046; 712/E9.055; 712/E9.057; 712/E9.058; 712/E9.062; 712/E9.078; 712/E9.08; 712/E9.081

(58) **Field of Classification Search** ..... None
See application file for complete search history.

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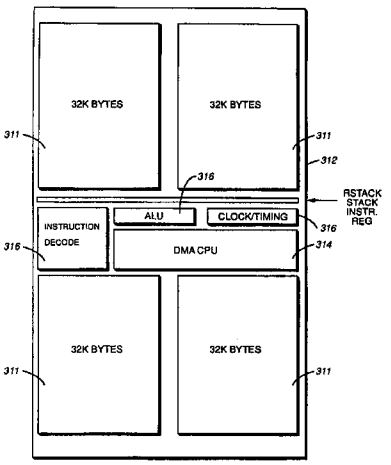
(57) **ABSTRACT**

A microprocessor integrated circuit including a processing unit disposed upon an integrated circuit substrate is disclosed herein. The processing unit is designed to operate in accordance with a predefined sequence of program instructions stored within an instruction register. A memory, capable of storing information provided by the processing unit and occupying a larger area of the integrated circuit substrate than the processing unit, is also provided within the microprocessor integrated circuit. The memory may be implemented using, for example dynamic or static random-access memory. A variable output frequency system clock, such as generated by a ring oscillator, is also disposed on the integrated circuit substrate.



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EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claims **4**, **6**, **7**, **11** and **13** is confirmed.

Claims **8** and **10** are cancelled.

Claims **1-3**, **5**, **9** and **12** were not reexamined.

* * * * *

Exhibit F

US005530890C1

(12) EX PARTE REEXAMINATION CERTIFICATE (8052nd)

United States Patent
Moore et al.

(10) **Number: US 5,530,890 C1**
(45) **Certificate Issued: Mar. 1, 2011**

(54) **HIGH PERFORMANCE, LOW COST MICROPROCESSOR**

(75) Inventors: **Charles H. Moore**, Woodside, CA (US); **Russell H. Fish, III**, Mt. View, CA (US)

(73) Assignee: **Patriot Scientific Corporation**, San Diego, CA (US)

Reexamination Request:
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Patent No.: **5,530,890**
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(51) **Int. Cl.**
G06F 15/76 (2006.01)

(52) **U.S. Cl.** **712/32**; 711/E12.02; 712/E9.016; 712/E9.028; 712/E9.046; 712/E9.055; 712/E9.057; 712/E9.058; 712/E9.062; 712/E9.078; 712/E9.08; 712/E9.081

(58) **Field of Classification Search** ..... None
See application file for complete search history.

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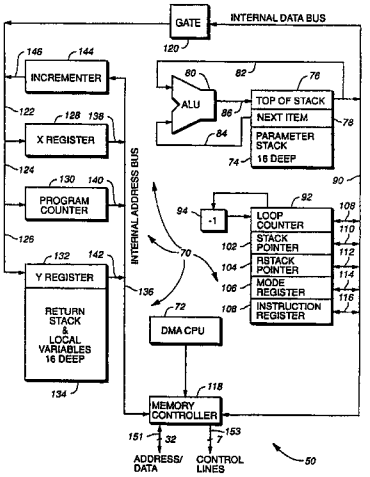
Primary Examiner—Joseph R. Pokrzywa

(57) **ABSTRACT**

A microprocessor (**50**) includes a main central processing unit (CPU) (**70**) and a separate direct memory access (DMA) CPU (**72**) in a single integrated circuit making up the microprocessor (**50**). The main CPU (**70**) has a first 16 deep push down stack (**74**), which has a top item register (**76**) and a next item register (**78**), respectively connected to provide inputs to an arithmetic logic unit (ALU) (**80**) by lines (**82**) and (**84**). An output of the ALU (**80**) is connected to the top item register (**76**) by line (**86**). The output of the top item register (**82**) is also connected by line (**88**) to an internal data bus (**90**). A loop counter (**92**) is connected to a decrementer (**94**) by lines (**96**) and (**98**). The loop counter (**92**) is birectionally connected to the internal data bus (**90**) by line (**100**). Stack pointer (**102**), return stack pointer (**104**), mode register (**106**) and instruction register (**108**) are also connected to the internal data bus (**90**) by lines (**110**), (**112**), (**114**) and (**116**), respectively. The internal data bus (**90**) is connected to memory controller (**118**) and to gate (**120**). The gate (**120**) provides inputs on lines (**122**), (**124**), and (**126**) to X register (**128**), program counter (**130**) and Y register (**132**) of return push down stack (**134**). The X register (**128**), program counter (**130**) and Y register (**132**) provide outputs to internal address bus (**136**) on lines (**138**), (**140**) and (**142**). The internal address bus provides inputs to the memory controller (**118**) and to an incremeter (**144**). The incrementer (**144**) provides inputs to the X register, program counter and Y register via lines (**146**), (**122**), (**124**) and (**126**). The DMA CPU (**72**) provides inputs to the memory controller (**118**) on line (**148**). The memory controller (**118**) is connected to RAM by address/data bus (**150**) and control lines (**152**).



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EX PARTE REEXAMINATION CERTIFICATE ISSUED UNDER 35 U.S.C. 307

THE PATENT IS HEREBY AMENDED AS INDICATED BELOW.

Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.

AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:

The patentability of claims **5-10** is confirmed.

Claims **1-4** are cancelled.

New claims **11-20** are added and determined to be patentable.

11. A microprocessor, which comprises a main central processing unit and a separate direct memory access central processing unit in a single integrated circuit comprising said microprocessor, said main central processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus, said internal data bus being bidirectionally connected to a loop counter, said loop counter being connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register, said stack pointer pointing into said first push down stack, said internal data bus being connected to a memory controller, to a Y register of a return push down stack, an X register and a program counter, said Y register, X register and program counter providing outputs to an internal address bus, said internal address bus providing inputs to said memory controller and to an incrementer, said incrementer being connected to said internal data bus, said direct memory access central processing unit providing inputs to said memory controller, said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory.

12. The microprocessor of claim 11 in which said memory controller includes a multiplexing means between said central processing unit and said address/data bus, said multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus.

13. The microprocessor of claim 11 in which said memory controller includes means for fetching instructions for said central processing unit on said address/data bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle.

14. The microprocessor of claim 13 additionally comprising means connected to said means for fetching instructions for determining if multiple instructions fetched by said means for fetching instructions require a memory access, said means for fetching instructions fetching additional multiple instructions if the multiple instructions do not require a memory access.

15. The microprocessor of claim 13 in which said microprocessor and a dynamic random access memory are contained in a single integrated circuit and said means for fetching instructions includes a column latch for receiving the multiple instructions.

16. The microprocessor of claim 11 in which said microprocessor includes a sensing circuit and a driver circuit, and an output enable line for connection between the random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level, said microprocessor being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

17. The microprocessor of claim 11 additionally comprising a ring oscillator variable speed system clock connected to said main central processing unit, said main central processing unit and said ring oscillator variable speed clock being provided in a single integrated circuit.

18. The microprocessor of claim 17 in which said memory controller includes an input/output interface connected to exchange coupling control signals, addresses and data with said main central processing unit, said microprocessor additionally including a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.

19. The microprocessor of claim 11 in which said first push down stack has a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit.

20. The microprocessor of claim 19 additionally comprising a first pointer connected to said first plurality of stack elements, a second pointer connected to said second plurality of stack elements, and a third pointer connected to said plurality of stack elements, said central processing unit being connected to pop items from said first plurality of stack elements, said first stack pointer connected to said second stack pointer to pop a first plurality of items from said second plurality of stack elements when said first plurality of stack elements are empty from successive pop operations by said central processing unit, said second stack pointer being connected to said third stack pointer to pop a second plurality of items from said third plurality of stack elements when said second plurality of stack elements are empty from successive pop operations by said central processing unit.

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