UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORPORATION, ALLIACENSE LTD., Defendants.	Case No. 5:08-cv-00877 PSG **(Re: Docket Nos. 356, 357, 358, 374)**
HTC CORPORATION, HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORPORATION, ALLIACENSE LTD., Defendants.	Case No. 5:08-cv-00882 PSG **(Re: Docket Nos. 385, 387, 388, 403)**

CLAIM CONSTRUCTION ORDER

In this patent infringement suit, Plaintiffs Acer, Inc., Acer America Corp., Gateway, Inc., and Plaintiffs HTC Corp. and HTC America, Inc. (collectively "Plaintiffs") seek a declaratory

judgment that they do not infringe patents owned by Defendants Technology Properties Ltd., Patriot Scientific Corp., and Alliacense Ltd. (collectively "Defendants").[1] Consistent with Pat. L.R. 4-3(c), the parties seek further construction of terms and phrases in claims in the patents-in-suit.[2] Plaintiffs and Defendants each also seek reconsideration of Judge Ware's earlier constructions of certain terms.[3]

As part of those motions for reconsideration, Plaintiffs seek to file a sur-reply on the grounds that Defendants' reply to their motion for reconsideration introduced new arguments and new evidence.[4] The court GRANTS Plaintiffs' motion to file the sur-reply.

In light of this case's long history and the trial date set for June 24, 2013, the court does not wish to add any further delay to the constructions by its preparation of a complete opinion setting forth its reasoning and analysis. To that end, the court at this time will simply issue its constructions without any significant reasoning and analysis:

CLAIM TERM	**CONSTRUCTION**
"instruction register"	Register that receives and holds one or more instructions for supplying to circuits that interpret the instructions
"ring oscillator"	an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment
"separate DMA CPU"	a central processing unit that accesses memory and that fetches and executes instructions directly and separately of the main central processing unit
"supply the multiple sequential instructions"	provide the multiple sequential instructions in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during

[1] Unless otherwise noted, the docket citations refer to Case No. 5:08-cv-00882 PSG.

[2] *See* Docket Nos. 387, 394.

[3] *See* Docket Nos. 385, 388.

[4] *See* Docket No. 403.

	a single memory cycle
"clocking said CPU"	Providing a timing signal to said central processing unit

The parties should rest assured that the court arrived at these constructions with a full appreciation of not only the relevant intrinsic and extrinsic evidence, but also the Federal Circuit's teaching in *Phillips v. AWH Corp.*,[5] and its progeny. So that the parties may pursue whatever recourse they believe is necessary, a complete opinion will issue before entry of any judgment.

IT IS SO ORDERED.

Dated: December 4, 2012

PAUL S. GREWAL
United States Magistrate Judge

[5] 415 F.3d 1303, 1312-15 (Fed. Cir. 2005).