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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case Nos. 5:08-cv-00877 **DEFENDANTS' REPLY IN SUPPORT OF ITS MOTION FOR RECONSIDERATION OF CERTAIN ASPECTS OF CLAIM CONSTRUCTION**

HTC CORPORATION and HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED, Defendants.	Case No. 3:08-cv-00882 PSG
BARCO, N.V., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED, Defendants.	Case No. 3:08-cv-05398 PSG

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Introduction

Defendants' instant Motion seeks reconsideration of the Court's construction of the phrase "separate direct memory access central processing unit" ("DMA CPU") in claim 11 of U.S. Patent No. 5,530,890 ("the '890 patent").[1] The Court construed that phrase to mean:

> a central processing unit that accesses memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit.

(Order [Dkt. No. 336] at 13). However, the Court's reasoning only took into account the first of two embodiments described in the '890 patent's specification. As a result, the Court's construction of DMA CPU improperly limited that term to that first embodiment and excluded the second embodiment. Defendants respectfully submit that their originally proposed construction of DMA CPU—"**electrical circuit for reading and writing to memory that is separate from a main CPU**"—is the proper construction for this term in view of the intrinsic record evidence. This construction avoids improperly limiting the claims to a single embodiment to the exclusion of others.

The '890 patent discloses two distinct embodiments. The first embodiment, shown in Figs. 1-8, includes a microprocessor 50 with a DMA CPU 72 (detailed in Fig. 5) possessing "the ability to fetch and execute instructions [that] operates as a co-processor to the main CPU." *See* '890 patent, 8:1; Fig. 5; 8:22-24. DMA CPU 72 of the first embodiment was referred to in Defendants' motion as a DMA co-processor. *See* Mot. at 1. In contrast, the second embodiment, shown in Fig. 9, includes a different microprocessor 310 with a "***more traditional DMA Controller 314***," which has replaced the DMA CPU 72 "[t]o keep chip size as small as possible" because the microprocessor 310 is "on an already crowded DRAM die." DMA 314 is referred to interchangeably in the specification as "DMA controller 314" or "***DMA CPU 314***." *See* '890

[1] Claim 11, which resulted from the reexamination proceeding, is identical to originally issued claim 1 except for the addition of the phrase "said stack pointer pointing into said first push down stack."

patent, 12:61-65; Fig. 9; 10:52; 13:3-4. DMA CPU 314 of the second embodiment was referred to as a conventional DMA controller in Defendants' motion. *See* Mot. at 1. The Court's construction of the DMA CPU, which requires a unit capable of fetching and executing instructions independently from the CPU, includes the DMA CPU 72 of the first embodiment but excludes DMA CPU 314 of the second embodiment.

In their Motion for Reconsideration, Defendants cited two portions of the intrinsic record—(1) a restriction requirement of the parent application, and (2) reexamination proceedings—not discussed during claim construction as additional evidence that the conventional DMA controller (DMA CPU 314) of the '890 patent's second embodiment is within the scope of the DMA CPU recited in claim 11. Both the restriction requirement and the reexamination proceedings are consistent with the overall intrinsic record that the claimed DMA CPU should be construed to cover the conventional DMA controller of the second embodiment.

Plaintiffs argue in opposition that the restriction requirement is irrelevant to the construction of DMA CPU. Plaintiffs are wrong. The restriction requirement further confirms that the DMA CPU (identically recited in claims 1 and 11) was not limited to a DMA co-processor ***that fetches and executes instructions***, as the Court held. *See* Order at 13. Moreover, Plaintiffs' arguments that restriction requirements should be given no weight or consideration for claim construction is directly contradicted by binding Federal Circuit precedent in a factually similar case. *See Rambus Inc. v. Infineon Techs. AG*, 318 F.3d 1081, 1095 (Fed. Cir. 2003).

Plaintiffs' arguments that the reexamination proceedings provide no basis for reconsideration are also incorrect. The reexamination proceedings are relevant as part of the intrinsic record of the '890 patent, and positions taken by the patent examiner during those proceedings support Defendants' proposed construction of DMA CPU. Plaintiffs attempt to argue that those positions taken during the reexamination proceedings are not relevant by claiming that they were never adopted by the patent examiner, but those claims are demonstrably false. The examiner not only agreed with and adopted the third-party requester's arguments, citing the exact same portions of the underlying prior art references, but also expressly

incorporated those arguments in the order determining that a substantial question of patentability existed and instituting the reexamination proceedings.

Finally, independent of the restriction requirement and the reexamination proceedings, the '890 patent's specification and other intrinsic evidence demonstrate that the construction Defendants urge is correct. For all of these reasons, the Court should grant Defendants' motion and change its construction of DMA CPU to "electrical circuit for reading and writing to memory that is separate from a main CPU," as Defendants originally argued.

Argument

I. THE RESTRICTION REQUIREMENT IS RELEVANT AND SUPPORTS DEFENDANTS' PROPOSED CONSTRUCTION.

The original application upon which the '890 patent claims priority was subject to a ten-way restriction requirement, which supports Defendants' proposed construction. Group III, which was pursued in a separate divisional and eventually abandoned, was "drawn to a microprocessor system having a DMA ***for fetching instruction for*** a CPU and ***itself***." Chen Decl. [Dkt. No. 368-1], Ex. 6 [Dkt. No. 368-7] at 2 (emphasis added). In other words, Group III was limited to a microprocessor system having a DMA co-processor of the type described in connection with the specification's first embodiment (*e.g.*, DMA CPU 72). *See* '890 patent, 8:1; Fig. 5; 8:22-24 ("The DMA CPU 72 controls itself and has the ability to fetch and execute instructions.").

Group VIII, which became the subject of the '890 patent, on the other hand, was more broadly "drawn to a microprocessor architecture." Chen Decl., Ex. 6 at 3. Importantly, Group VIII was never limited to a DMA co-processor. Unlike Group III, Group VIII did not specify that that the DMA be capable of fetching or executing instructions for a CPU or itself. The broader scope of Group VIII was consistent with the specification, which describes two distinct microprocessor architectures:

> (1) microprocessor 50 described in connection with Figs 1-8, which uses a DMA co-processor DMA CPU 72 capable of fetching and executing its own instructions (*see* '890 patent, 8:1; Fig. 5; 8:22-24); and

(2) microprocessor 310 described in connection with Figure 9, which uses "a more traditional DMA controller 314" also referred to as "DMA CPU 314," in order "[t]o keep chip size as small as possible" (*see* '890 patent, 12:61-66; Fig. 9; 10:52; 13:3-4).

There is nothing in the file history that limits the claims of Group VIII to one of these two architectures. Hence, Group VIII should cover both embodiments described in the specification, absent some limiting language in the file history. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005) (*en banc*) ("[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments."). The Court construction of the DMA CPU in a way that limits it to the first embodiment is improper. *Id*.

Plaintiffs argue that the restriction requirement is "irrelevant to the construction of DMA CPU." Opp. at 3-6. In support of their argument, Plaintiffs cite an un-reported, non-binding 2002 case from the District of Oregon that says that "[r]estriction requirements do not constitute a substantive claim construction doctrine." *See id.*, at 5 (quoting *Michaels of Oregon Co. v. Clean Gun, LLC*, No. Civ. 01-1158, 2002 WL 21496414, at *8 (D. Or. July 9, 2002)).[2] Plaintiffs are incorrect. Courts can and should consider restriction requirements in claim construction proceedings where relevant, as more recent binding Federal Circuit precedent makes clear.

In *Rambus v. Infineon*, the Federal Circuit overturned a district court's decision where the district court's narrow construction of the term "bus" was contradicted by a restriction requirement and the patent holder's response to it. *Infineon*, 318 F.3d at 1095. The patents at issue in *Infineon* involved a ten-way restriction requirement followed by a two-way restriction requirement. *Id*. In the two-way restriction requirement, the Patent and Trademark Office ("PTO") divided the claims "into two distinct groups: a multiplexing bus group (Group I) and a latency invention group (Group II)." *Id*. The patent at issue was based on the claims from Group II, which recited the term "bus" without referencing multiplexing. *Id*. The district court

[2] Plaintiffs also cite the *Amerham* case in support of their argument (*see* Opp. at 3, 5-6), which is inapposite and distinguished below.

construed the term "bus" to require a multiplexing bus, even though the claims were not part of the "multiplexing bus group (Group I)," and did not include any language about multiplexing. *Id.* . The Federal Circuit reversed, holding that "the district court erred in its construction of each of the disputed claim terms." *Id.* . In addition to noting that the elected claim group was not directed to multiplexing, the Court also noted the patent holder in that case "did not redefine 'bus' to be a multiplexing bus in the patents-in-suit" and that none of the patent holder's statements "constitute[d] a clear disavowal of claim scope. *Id.* .

Infineon's similarities to this case are striking. In *Infineon*, the specification supported multiple embodiments such that the claim term at issue ("bus") could be interpreted multiple ways (*i.e.*, a "multiplexing bus" and a "'bus' that is not limited to a multiplexing bus"). *Id.* Similarly, the '890 patent's specification includes multiple embodiments such that the DMA CPU term at issue is susceptible to multiple interpretations including (1) DMA CPU 72 shown in Fig. 5 with the ability to fetch and execute instructions, and (2) DMA CPU 314, the conventional DMA controller shown in Fig. 9. In *Infineon*, the restriction requirement included a group of claims that involved one specific embodiment of the invention that required limiting the claim term at issue to just one of possible interpretations (*i.e.*, Group I limiting "bus" to a "multiplexing bus"), but the patent at issue resulted from another group that did not so limit the term (*i.e.*, Group II not limited to a "multiplexing bus"). *Infineon.*, 318 F.3d at 1095. Similarly, in this case, the restriction requirement included a group of claims (Group III) that involved one specific embodiment that uses a DMA CPU that is able to fetch instructions for itself, but the patent at issue resulted from another group (Group VIII) that did not so limit the DMA CPU claim term. Also, as in *Infineon*, there has not been—and the Court did not point to—any "disclaimer or disavowal of claim scope" that would limit the claimed DMA CPU to one of the described embodiments. *Id.* .; *See Phillips*, 415 F.3d at 1316. In this case, the Court improperly limited the DMA CPU claim term at issue to a specific embodiment associated with a group of claims not pursued in the patent at issue. *See* Mot. at 13. Similarly, the district court in *Infineon* improperly limited the claim term at issue ("bus") to the specific embodiment associated with the group of claims not pursued in the patents at issue ("multiplexing bus"). As a result, the Federal

Circuit held the "district court erred in its construction of each of the disputed terms," when it unnecessarily limited the claim term at issue. *Infineon*, 318 F.3d at 1095.

Contrary to Plaintiffs' arguments against the relevance of the restriction requirement, other courts have also relied on restriction requirements for the purposes of claim construction. For example, the Northern District of Illinois relied on the group of claims selected by a patentee in response to a restriction requirement to construe the patent claims. *Albecker v. Contour Products, Inc.*, No. 09 C 0631, 2010 WL 1839803, at *8 (N.D. Ill. May 3, 2010). The *Albecker* court refused to import an additional limitation in its claim construction where the patentee had elected and pursued a claim group that did not include that limitation. *Id*. This case presents a similar situation where the group elected and pursued (Group VIII) did not include the additional limitation that the DMA be capable of fetching instructions for a CPU and itself, unlike Group III. *See also Acumed LLC v. Stryker Corp.*, 483 F.3d 800, 805–06 (Fed. Cir. 2007) (rejecting attempt to limit claim construction to single embodiment and noting that examiner had restricted out narrower claims directed to that embodiment), *cert. denied*, 552 U.S. 1022 (U.S. 2007); *LG Elecs., Inc. v. Bizcom Elecs., Inc.*, 453 F.3d 1364, 1373 (Fed. Cir. 2006), *rev'd on other grounds*, 553 U.S. 617 (U.S. 2008) (district court erred reading requirement into claims from embodiment restricted out by examiner and pursued in divisional application).

The cases Plaintiffs cite are readily distinguishable and do not compel a contrary result. Plaintiffs cite *Rambus v. Hynix* as supporting the idea that restriction requirements are of limited evidentiary significance. *See* Opp. at 3 (citing *Rambus Inc. v. Hynix Semiconductor Inc.*, 569 F. Supp. 2d 946, 962 (N.D. Cal. 2008)). However, contrary to Plaintiffs' suggestions that the restriction requirements at issue in *Hynix* were not relevant to claim construction, the Federal Circuit considered some of the very same restriction requirements in the related *Infineon* case discussed above, and specifically used those restriction requirements as a partial basis for determining that the district court had erred in its claim construction. *See Infineon*, 318 F.3d at 1095. Restriction requirements are relevant to claim construction issues. Plaintiffs' citation of *Amerham Pharmacia* is unavailing because, unlike *Amerham*, Defendants in this case are not trying to use a restriction requirement to "controvert the plain language of the claim." *See* Opp.

at 3, 5-6 (citing *Amerham Pharmacia Biotech, Inc. v. Perkin-Elmer Corp.*, No. C 97-CV-4203 CRB, 2000 WL 34204509, at *15-16 (N.D. Cal. Feb. 28, 2000)). To the contrary, the restriction requirement in this case ***confirms*** that the claim includes both embodiments described in the specification, and is not limited to just one embodiment pursued in a divisional application. *See Infineon*, 318 F.3d at 1095. Plaintiffs' citation to *Honeywell* is similarly unavailing because the *Honeywell* decision turned on the fact that the patentee had expressly limited the claim term at issue, "fuel injection system component," to "fuel filter" in at least four places in the written description. *Honeywell Int'l, Inc. v. ITT Indus., Inc.*, 452 F.3d 1312, 1318 (Fed. Cir. 2006)). There is no such express limitation in the '890 patent's specification that could be used to limit the claim scope of that patent. *See Phillips*, 415 F.3d at 1316. Instead, the '890 patent's specification expressly refers to two different embodiments involving different types of DMA CPUs: DMA CPU 72 and DMA CPU 314.

Finally, Plaintiffs' straw-man argument about the overlapping subject matter of claims from different independent claim groups identified in the restriction requirement is misplaced. *See* Opp. at 4-5. Plaintiffs argue that Defendants' motion for reconsideration is flawed because Group III and Group VIII, as well as other groups identified in the restriction requirement may recite common features. *Id.* Plaintiffs' argument misses the point. Defendants are not arguing that Group VIII cannot include the DMA CPU 72 of the first embodiment—to the contrary, Defendants argued and continue to argue that the restriction requirement supports Defendants' original claim construction position, which has always encompassed both embodiments and "does not limit the construction of DMA CPU to only one of the two disclosed microprocessor architecture embodiments (Figs. 2 and 9)." Mot. at 7.

Like the rest of the intrinsic record, the restriction requirement supports Defendants' proposed construction of DMA CPU.

II. THE REEXAMINATION PROCEEDINGS ARE RELEVANT AND SUPPORT DEFENDANTS' PROPOSED CONSTRUCTION.

The reexamination proceeding cited in Defendants' Motion for Reconsideration further supports Defendants' proposed claim construction. Specifically, the reexamination proceedings

confirm that the claimed DMA CPU was understood throughout those proceedings to mean a conventional DMA controller. *See* Mot. at 5-6. In other words, the reexamination proceedings confirm that the proper construction of DMA CPU must include the conventional DMA controller (DMA CPU 314) of the second embodiment, and not be limited to just the DMA co-processor (DMA CPU 72) of the first embodiment. Specifically, Defendants noted that the third-party reexamination requester indicated that the claimed DMA CPU would have been considered obvious because the prior art reference Tsuchiya (U.S. Patent No. 4,783,764) describes a microprocessor that includes a conventional DMA controller on a single integrated circuit with a CPU. *Id*. at 6. Defendants also pointed out that the PTO granted the reexamination partially on the basis of Tsuchiya describing this feature using a conventional DMA controller. *Id*.

Plaintiffs attempt to minimize the reexamination proceedings by arguing that the statements cited in the Motion are merely "statements of an anonymous third party reexamination requester—which were not adopted by either the patent owner or the Examiner." Opp. at 6. Plaintiffs further argue that "the third party requester's statements regarding the 'DMA CPU' were not adopted by either the Examiner or TPL, and thus should carry no weight in claim construction." This argument is demonstrably false.

The patent examiner not only adopted these arguments, equating a conventional DMA controller to the claimed DMA CPU, but the examiner actually expressly ***incorporated them by reference*** into the order he issued granting the reexamination request. After considering the reexamination request, the examiner found that the reexamination request raised three substantial new questions of patentability ("SNQs") with respect to the '890 patent. Breit Decl., Ex. A (Order Granting Reexamination) at 4, ¶ 6. As the Order states, with respect to the third SNQ, the examiner adopted the third-party requestor's argument that "Tsuchiya describes a microprocessor further including a separate direct memory access central processor unit," and cited to the same Tsuchiya selection referenced in the reexamination request. *Id*., at 7, ¶ 11 (citing Tsuchiya at "col. 4, line 51 – col. 5, line 52") *compare* Chen Decl., Ex. 7 (Reexamination Request) [Dkt. No. 368-8] at 11-12 (citing Tsuchiya at "Col. 4, line 51 to Col. 5, line 52"). The examiner went further, incorporating by reference additional discussion of this and other

arguments in the reexamination request, which formed the basis of the examiner's determination that substantial new questions of patentability existed and a reexamination should be ordered:

> The additional passages regarding the limitations of claim 1, as described in May and Tsuchiya, pointed out in the Request for Reexamination in the claim chart on pages 26 through 32, ***are hereby incorporated by reference*** for their explanation of the teaching provided in May and Tsuchiya, which were not present in the prosecution of the application which became the '890 Patent. Further, there is substantial likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the claim is patentable. Accordingly, May and Tsuchiya raise a substantial new question of patentability as to independent claim 1 [and claims 2-10].

Breit Decl., Ex. A (Order Granting Reexamination) at 8, ¶ 11 (emphasis added).

The portion of the reexamination request that was incorporated by reference into the order granting reexamination, and which formed the partial basis for the examiner's finding that a substantial new question of patentability existed, discussed the claimed DMA CPU at length. *See* Chen Decl., Ex. 7 at 26-27. That incorporated portion of the request stated that "[a]t the time of filing, the use of an on-chip DMA controllers [*sic*] was well known in the art." *Id*. at 26. The request then cited passages from a number of patents as examples, including the same portion of the Tsuchiya patent cited in the request and the order (*i.e.*, col. 4, line 51 – col. 5, line 52), and stated that "it would have been obvious to one skilled in the art to include an on-chip DMA controller with the processor taught by May." *Id*. at 27. The request then goes on to describe the "Direct Memory Access controller" of the Tsuchiya reference, which the requestor said was "just one of many patents which demonstrate that the DMA controllers were conventionally placed on the same chip" as the CPU at the time of the '890 patent. *Id*.

Contrary to Plaintiffs' arguments, these are ***the patent examiner's*** positions, taken on behalf of the PTO, ***expressly incorporated by reference in the PTO's order*** finding a substantial new question of patentability in and granting reexamination of the '890 patent's claims. *See* Breit Decl., Ex. A at 8, ¶ 11. In other words, this is part of the intrinsic record of the '890 patent, and not merely a collection of statements made by an anonymous third-party requester. Moreover, during the reexamination proceedings, the Examiner also relied on U.S. Patent No. 4,989,113 to Hull, another reference cited in the section the examiner incorporated by reference as teaching a conventional DMA controller in subsequent office actions in the reexamination

proceedings. *See* Breit Decl., Ex. B (Non-Final Office Action) at 4, ¶ 6 (noting the Hull reference teaches the use of on-chip DMA controllers and can be interpreted as teaching other claim features). In fact, the examiner goes so far as to equate the conventional DMA controller (DMA Control 22 of Fig. 1) of Hull with the claimed "separate direct memory access central processing unit." *Id*. at 5, ¶ 8. When finally rejecting the claim, the examiner incorporating the same section again equated the claimed DMA CPU to the conventional DMA controller of Hull. *See* Breit Decl., Ex. C (Final Office Action) at 3, ¶ 4.

This reexamination proceeding—a part of the intrinsic record—further underscores the fact that the claimed DMA CPU includes both the DMA co-processor of the first embodiment in the '890 patent (DMA CPU 72) ***as well as the conventional DMA controller of the second embodiment*** (DMA CPU 314). There is nothing in the intrinsic record that suggests the claimed DMA CPU should be limited to the first embodiment as the Court held in its claim construction order. *See* Order at 13 (limiting the claimed DMA CPU to "a central processing unit that accesses memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit.").

Like the rest of the intrinsic record, the reexamination proceeding supports Defendants' proposed construction of DMA CPU.

III. THE INTRINSIC RECORD AS A WHOLE SUPPORTS DEFENDANTS' PROPOSED CONSTRUCTION.

Beyond just the restriction requirement and the reexamination proceeding, the entire intrinsic record supports Defendants' proposed construction of DMA CPU, which encompasses both embodiments of the DMA CPU described in the '890 patent's specification. As the Federal Circuit has recognized, a district court is welcome to "revisit and alter its interpretation of the claim terms as its understanding of the technology evolves." *Pfizer, Inc. v. Teva Pharm., USA, Inc.*, 429 F.3d 1364, 1377 (Fed. Cir. 2005); *see also Utah Med. Prods., Inc. v. Graphic Controls Corp.*, 350 F.3d 1376, 1381-82 (Fed. Cir. 2003) (district court did not err amending claim construction during oral arguments for pretrial motions nearly two years after original construction). Indeed, when parties raise actual disputes regarding claim scope, the Court must

resolve that dispute. *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351, 1360 (Fed. Cir. 2008).

As explained above, the '890 patent's specification discloses and describes two embodiments involving two different microprocessors, each of which involves a distinct type of DMA CPU. The first embodiment involves microprocessor 50 shown in connection with Figures 1-8 of the '890 patent and involves the DMA co-processor DMA CPU 72. "Details of the DMA CPU 72 are provided in FIG. 5." '890 patent, 8:1. The specification expressly states that the DMA CPU 72 "operates as a co-processor to the main CPU." '890 patent, 8:23-24. In particular, the specification points out that the "DMA CPU 72 controls itself and has the ability to fetch and execute instructions." '890 patent, 8:22-23.

The specification also describes a second embodiment, which uses a different microprocessor 310 and a traditional DMA controller 314, which differs from the DMA co-processor DMA CPU 72. The specification expressly calls out this second embodiment shown and described in connection with Fig. 9. '890 patent at 4:60-62 ("FIG. 9 is a layout diagram of ***a second embodiment of a microprocessor in accordance with the invention*** in a data processing system on a single integrated circuit.") In particular, the specification notes that the microprocessor 310 is used on "an already crowded DRAM die 312." '890 patent, 8:61-62. Because of the tight quarters associated with this second embodiment, the patent notes that "[t]o keep chip size as small as possible, the DMA processor 72 of the microprocessor 50 ***has been replaced with a more traditional DMA controller 314***." '890 patent, 8:62-65 (emphasis added). In other words, the second embodiment uses a more traditional DMA controller, which is shown as DMA CPU 314 in Fig. 9. That more traditional DMA controller associated with the second embodiment is referred to interchangeably as "DMA controller 314" or "***DMA CPU 314***" in the specification. *See, e.g.*, '890 patent, 12:61-65; Fig. 9; 10:52; 13:3-4. Unlike the DMA co-processor DMA CPU 72 of the first embodiment, the DMA CPU 314 of the second embodiment is not described as fetching or executing its own commands independent of the CPU. *Cf.* '890 patent, 8:22-23. Instead, the specification states that the DMA controller 314 of the second embodiment "is used ***with the microprocessor 310***" to perform certain functions, such as video

output, multiprocessor serial communications, and 8-bit parallel I/O. '890 patent, 12:65-13:2. The specification makes clear that this "more traditional DMA controller 314" of the second embodiment—unlike the self-sufficient DMA co-processor 72 of the first embodiment—can only function when controlled by and "used with the microprocessor 310" to accomplish functions "supported by the microprocessor 310." *See* '890 patent, 12:65-13:12.

The Court's construction of the term DMA CPU encompasses the first embodiment described in the '890 patent, but excludes the second embodiment. Specifically, the Court's opinion held that the term "separate direct memory access central processing unit" of claim 11 of the '890 patent means "a central processing unit that access memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit." Order [Dkt. No. 336] at 12. In other words, the Court's construction would include the DMA CPU 72 of Figures 1-8, "which controls itself and has the ability to fetch and execute instructions" ('890 patent, 8:22-23), but would not include the DMA CPU 314, which is "a more traditional DMA controller" and functions only when "used with the microprocessor 310" in a way "supported by the microprocessor 310." *See* '890 patent, 8:62-65; 12:65-13:12. This exclusion of the second embodiment, which appears to be unintentional, is unnecessary and improper.

The Court's claim construction order reasoned that, because the phrase being construed included the term "central processing unit" or CPU, it would be understood to mean a unit of a computing system that fetches, decodes, and executes programmed instructions. *See* Order at 12 & n.26 (citing Modern Dictionary of Electronics 107 (7th ed. 1999)). The Court goes on to observe that the '890 patent specification uses the term CPU consistently with this meaning, citing to a selection in the patent that refers to the DMA CPU 72 of the first embodiment. *See* Order 12 & n.27 (citing '890 patent, 8:22-24). However, the Court's reasoning relies exclusively on the DMA of the first embodiment (DMA CPU 72) without regard to the second embodiment, which replaces "the DMA processor 72 . . . with a more traditional DMA controller 314." '890 patent, 12:61-65. Although the Court correctly recognized that the DMA CPU 72 of the first

embodiment is described consistently with the dictionary definition of CPU that it relied on, the Court failed to account for the DMA CPU 314 of the second embodiment, which is different.

The DMA CPU 314 is different from the DMA CPU 72 of the first embodiment. The Court correctly recognized that the DMA CPU 72 of the first embodiment was considered advantageous because it "does not require use of the main CPU during DMA requests and responses . . . which provides very rapid DMA response with predictable response times." Order at 12 & n. 29. However, the Court's reasoning only takes into account the specification's discussion of the advantages of the first embodiment, which uses the DMA CPU 72, and ignores the second embodiment of the invention described in connection with Figure 9, which uses "a more traditional DMA controller 314" instead of the DMA co-processor DMA CPU 72. *See* '890 patent, 12:61:65. The patent states that the second type of microprocessor 310 of the second embodiment (distinguished from microprocessor 50 of the first embodiment) is used because it resides on a more crowded DRAM die." *Id*. Because of this more crowded arrangement, the second embodiment uses the more traditional DMA controller 314 "[t]o keep chip size as small as possible." *Id*. This is directly in line with several "objects" of the invention recited in the specification but not explicitly acknowledged in the Court's claim construction order. *See e.g.*, '890 patent, 1:61-63 ("to provide a microprocessor with a reduced pin count and cost compared to conventional microprocessors"); '890 patent, 1:65-67 ("to provide a high performance microprocessor that can be directly connected to DRAMs without sacrificing microprocessor speed"). Indeed, the second embodiment shown in Figure 9 is presented as a "solution to the bandwidth/bus path problem" associated with the microprocessor 50 of the first embodiment. *See* '890 patent, 8:60-9:1.

Patent claims "must be read in view of the specification, of which they are a part." *Phillips*, 415 F.3d at 1315 (citing *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995)). "The proper definition is the 'definition that one of ordinary skill in the art could ascertain from the intrinsic evidence in the record.'" *Id.* at 1314 quoting *Unitherm Food Sys., Inc. v. Swift–Eckrich, Inc.*, 375 F.3d 1341, 1351 (Fed.Cir.2004). One of ordinary skill in the art

would understand the term DMA CPU consistent with the two embodiments of the '890 patent discussed above. *See Phillips*, 415 F.3d at 1315-16.[3]

Defendants respectfully submit that the intrinsic record in this case—including the specification and the file history (which includes the restriction requirement and reexamination proceeding)—support Defendants' proposed construction for DMA CPU of "electrical circuit for reading and writing to memory that is separate from a main CPU." Only this construction avoids improperly limiting the claim to a particular embodiment. On the other hand, the Court's construction limits the claim to the first embodiment, which is improper. *Phillips*, 415 F.3d at 1323 ("[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments.") (citations omitted); *see also DSW, Inc. v. Shoe Pavilion, Inc.*, 537 F.3d 1342, 1348 (Fed. Cir. 2008) ("[W]hen claim language is broader than the preferred embodiment, it is well-settled that claims are not to be confined to that embodiment."). Indeed, even if a patent only describes a single embodiment, it is well settled that the claims need not be limited to that embodiment alone. *Gemstar-TV Guide Int'l, Inc. v. Int'l Trade Comm'n*, 383 F.3d 1352, 1366 (Fed. Cir.2004). Here, however, the case is even clearer, because the patent described multiple embodiments. The claim should not be limited to a single embodiment.

Accordingly, in view of the specification and other intrinsic record evidence, Defendants submit that the DMA CPU of claim 11 of the '890 patent should be construed according to Defendants' proposed construction.

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[3] It is fundamental that an inventor may act as his or her own lexicographer. Thus, the Court's reliance on a technical dictionary definition that is consistent with one embodiment but inconsistent with another may be misplaced. *See* Order at 12 n.26 (citing Modern Dictionary of Electronics 107 (7th ed. 1999)). Indeed, the Federal Circuit has stated that in cases where the specification reveals that the inventor gave a claim term a special meaning that differs from the meaning it might otherwise possess, "***the inventor's own lexicography governs***." *Phillips*, 415 F.3d at 1318 (emphasis added), citing *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed.Cir.2002). Consistent with this principle, the Federal Circuit has "repeatedly warned against confining the claims to [particular] embodiments." *Phillips*, 415 F.3d at 1323.

Conclusion

For the reasons set forth above, Defendants respectfully submit that the Court should reconsider its construction of the term "separate direct memory access central processing unit" (or "DMA CPU" as it is referred to throughout this brief). Defendants further respectfully submit that the Court should construe this term according to Defendants' originally proffered claim construction to mean "electrical circuit for reading and writing to memory that is separate from a main CPU." Only Defendants' proposed claim construction is consistent with the intrinsic record as a whole and avoids unnecessarily limiting the claim term to a single embodiment of the '890 patent to the exclusion of others.

Dated: November 9, 2012

Respectfully submitted,

AGILITY IP LAW, LLP

By: /s/ Michelle G. Breit
Michelle Breit

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and ALLIACENSE LIMITED

KIRBY NOONAN LANCE & HOGE

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Attorneys for Defendant
PATRIOT SCIENTIFIC CORPORATION

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case Nos. 5:08-cv-00877 **DECLARATION OF MICHELLE G. BREIT IN SUPPORT OF DEFENDANTS' REPLY IN SUPPORT OF ITS MOTION FOR RECONSIDERATION OF CERTAIN ASPECTS OF CLAIM CONSTRUCTION**

HTC CORPORATION and HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED, Defendants.	Case No. 3:08-cv-00882 PSG
BARCO, N.V., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED, Defendants.	Case No. 3:08-cv-05398 PSG

I, Michelle G. Breit, hereby declares and state as follows:

1. I am a partner at the law firm Agility IP Law, LLP counsel of record for Defendants Technology Properties Limited ("TPL") and Alliacense Limited in the above-captioned action. I am licensed to practice law and am admitted before this Court. I have personal knowledge of the facts set forth in this declaration, and if called to do so, I could and would competently testify thereto. I submit this declaration in support of Defendants' Reply in Support of its Motion for Reconsideration of Certain Aspects of Claim Construction.

2. Attached as Exhibit A is a true and correct copy of an Order Granting Request for *Ex Parte* Reexamination issued by the United States Patent and Trademark Office (the "PTO") in connection with U.S. Patent No. 5,530,890 and Control No. 90/009,388, and mailed on April 8, 2009.

3. Attached as Exhibit B is a true and correct copy of a non-final office action in an *Ex Parte* Reexamination issued by the PTO in connection with U.S. Patent No. 5,530,890 and Control No. 90/009,388, and mailed on November 5, 2009.

4. Attached as Exhibit C is a true and correct copy of a final office action in an *Ex Parte* Reexamination issued by the PTO in connection with U.S. Patent No. 5,530,890 and Control No. 90/009,388, and mailed on April 29, 2010.

I declare under penalty of perjury that the foregoing is true and correct and that this declaration was executed this 9th day of November, 2012, at Scottsdale, Arizona.

/s/ Michelle G. Breit
Michelle G. Breit

EXHIBIT A

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/009,388	01/16/2009	5530890	24567-0002RX3	7136

40972 7590 04/08/2009

HENNEMAN & ASSOCIATES, PLC
714 W. MICHIGAN AVENUE
THREE RIVERS, MI 49093

EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 04/08/2009

Please find below and/or attached an Office communication concerning this application or proceeding.

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APR 08 2009

CENTRAL REEXAMINATION UNIT

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/009,388*.

PATENT NO. *5530890*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Order Granting / Denying Request For Ex Parte Reexamination	Control No.	Patent Under Reexamination	
	90/009,388	5530890	
	Examiner	Art Unit	
	JOSEPH R. POKRZYWA	3992	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

The request for *ex parte* reexamination filed *16 January 2009* has been considered and a determination has been made. An identification of the claims, the references relied upon, and the rationale supporting the determination are attached.

Attachments: a)☐ PTO-892, b)☐ PTO/SB/08, c)☒ Other: *PTO-1449*

1. ☒ The request for *ex parte* reexamination is GRANTED.

RESPONSE TIMES ARE SET AS FOLLOWS:

For Patent Owner's Statement (Optional): TWO MONTHS from the mailing date of this communication (37 CFR 1.530 (b)). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).**

For Requester's Reply (optional): TWO MONTHS from the **date of service** of any timely filed Patent Owner's Statement (37 CFR 1.535). **NO EXTENSION OF THIS TIME PERIOD IS PERMITTED.** If Patent Owner does not file a timely statement under 37 CFR 1.530(b), then no reply by requester is permitted.

2. ☐ The request for *ex parte* reexamination is DENIED.

This decision is not appealable (35 U.S.C. 303(c)). Requester may seek review by petition to the Commissioner under 37 CFR 1.181 within ONE MONTH from the mailing date of this communication (37 CFR 1.515(c)). **EXTENSION OF TIME TO FILE SUCH A PETITION UNDER 37 CFR 1.181 ARE AVAILABLE ONLY BY PETITION TO SUSPEND OR WAIVE THE REGULATIONS UNDER 37 CFR 1.183.**

In due course, a refund under 37 CFR 1.26 (c) will be made to requester:

a) ☐ by Treasury check or,

b) ☐ by credit to Deposit Account No. _____, or

c) ☐ by credit to a credit card account, unless otherwise notified (35 U.S.C. 303(c)).

cc:Requester (if third party requester)

DETAILED ACTION

Response to Request for *ex parte* Reexamination

1. Reexamination has been requested for claims 1-10 of United States Patent Number 5,530,890.

2. A substantial new question of patentability affecting claims 1-10 of U.S. Patent Number 5,530,890 (hereafter "the '890 Patent") is raised by the Third Party's request for *ex parte* reexamination.

3. The '890 Patent issued on June 25, 1996, from U.S. Application 08/480,206, being filed on June 7, 1995, being a Division of U.S. Application 07/389,334, filed August 3, 1989, now U.S. Patent 5,440,749.

Listing of Prior Art

4. In the request for reexamination, the Third Party Requester alleges that the '890 Patent claims 1-10 are anticipated or unpatentable in light of the following references:

a. D. MacGregor *et al.*, "The Motorola MC68020", IEEE Micro, Vol. 4, issue 4, August 1984, pages 101-118 (noted as "MacGregor");

b. MC68020 32-Bit Microprocessor User's Manual, Motorola, Prentice-Hall, 1984 (noted as "User's Manual", hereafter "MC68020 User's Manual");

c. U.S. Patent Number 4,783,764, issued to Tsuchiya et al. (noted as "Tsuchiya");

d. U.S. Patent Number 4,665,495, issued to Thaden (noted as "Thaden");

e. MOSTEK 1981 3870/F8 MicrocomputerData Book, February1981, pages III-76 - VI-11 (noted as "Mostek");

f. F8/3870 F6800 Bit-Slice Fairchild Microcomputers, United Technical Publications, IC Master, 1980, pages 2016-2040 (noted "IC Master");

g. U.S. Patent Number 4,766,567, issued to Kato (noted as "Kato");

h. U.S. Patent Number 4,758,948, issued to May *et al.* (noted as "May");

i. U.S. Patent Number 4,680,698, issued to Edwards et al. (noted as "Edwards");

j. U.S. Patent Number 4,969,091, issued to Muller (noted as "Muller");

k. "80386 Programmer's Reference Manual", Intel, 1986 (noted as "Intel");

l. "Transputer Reference Manual", INMOS, Prentice Hall, 1988 (noted as "INMOS", hereafter "INMOS Transputer"); and

m. U.S. Patent Number 4,571,709, issued to Skupnjak *et al.* (noted as "Skupnjak").

5. Continuing, the aforementioned newly cited references of MacGregor, MC68020 User's Manual, Tsuchiya, Mostek, IC Master, Kato, May, Edwards, Muller, Intel, and Skupnjak are not of record in the file of the '890 Patent and are not cumulative to the art of record in the original file. The references of Thaden, and the INMOS Transputer were both cited in the original prosecution, but neither reference was discussed or utilized in any rejection within the original prosecution. Additionally, upon review of the prosecution history of the parent application of the '890 Patent (being U.S. Application 07/389,334), the Intel reference was cited in the parent application, but not discussed or utilized in any rejection.

Requester's Position

6. The request indicates that the Third Party Requester alleges that:

SNQ#1. Claims 1-5 of the '890 Patent to be anticipated MacGregor;

SNQ#2. Claims 6-10 of the '890 Patent to be rendered obvious over MacGregor in view of various noted prior art teachings included within the references of Skupnjak, Kato, Mostek, and Muller;

SNQ#3. Claims 1-10 of the '890 Patent to be rendered obvious over May in view of various prior art teachings included within the references of Tsuchiya, Edwards, Thaden, the INMOS Transputer, Skupnjak, Kato, Mostek, and Muller, with limitations of claim 1 discussed as being taught by May in view of Tsuchiya.

Discussion of Original Prosecution History

7. In the original prosecution of U.S. Application 08/480,206, which became the '890 Patent, a first-action Notice of Allowance was mailed on 12/12/1995. In this Notice of Allowance, the original examiner stated "Claims 48-57 are allowable over the references of record in that [n]one of the references teach a microprocessor having an architecture as recited in the claims." This is the only discussion of the claims that appears in the prosecution record for application, and there is no discussion of any of the cited references that are also in the prosecution history in the application that matured into the '890 Patent. Further, the '890 Patent cites the same references that appear in the parent application of the '890 Patent, being application 07/389,334, which matured into the U.S. Patent Number 5,440,749, whereby the original examiner noted the references cited in the parent application in a Notice of References Cited that was mailed with the Notice of Allowance dated 12/12/1995.

8. Continuing, the parent application appears to be deemed allowable based on features that describe "a first push down stack connected to said arithmetic logic unit", being similar to limitations found in the instant claim 1 of the '890 Patent. Thus, for the '890 Patent, it appears that claim 1, being the only independent claim, was deemed allowable for the features that define "a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit". However, as noted above, while the original examiner stated that the prior art of record does not teach of a microprocessor having the claimed architecture, the original examiner included no discussion that elaborates on the specific features that made the claims allowable over the prior art of record, and within the prosecution history,

there were no rejections made to the claims with the prior art of record, nor were any of the cited prior art in the record expressly discussed. Thus, the specific allowable features of claims 1-10 of the '890 Patent in the original prosecution are unclear.

Discussion of Substantial New Question of Patentability

9. First, the examiner notes that MPEP 2240 [R-5] states, in part:

> 37 CFR 1.515. Determination of the request for ex parte reexamination.
>
> (a) Within three months following the filing date of a request for an *ex parte* reexamination, an examiner will consider the request and determine whether or not a substantial new question of patentability **affecting any claim of the patent** is raised by the request and the prior art cited therein, with or without consideration of other patents or printed publications. The examiner 's determination will be based on the claims in effect at the time of the determination, will become a part of the official file of the patent, and will be mailed to the patent owner at the address as provided for in § 1.33(c) and to the person requesting reexamination. [Emphasis added.]

10. With this, with respect to the first proposed SNQ noted above, it is agreed that the consideration of MacGregor raises a substantial new question of patentability as to independent claim 1 of the '890 Patent. The reference of MacGregor appears to teach of a microprocessor having similar architecture as that required in claim 1 of the '890 Patent, being what was noted as allowable over the prior art of record in the original prosecution of the '890 Patent. Particularly, MacGregor is seen as teaching of a microprocessor (MC68020, see Fig. 1 on page 108 and Fig. 2 on page 109) having a main central processing unit having an arithmetic unit (included in "three arithmetic units", see page 101, col. 2), a first push down stack with a top

item register and a next item register, connected to provide inputs to said arithmetic unit (see Figs. 1 and 2 on page 104). The additional passages regarding the system described in MacGregor, pointed out in the Request for Reexamination in the claim chart on pages 11 though 15, are hereby incorporated by reference from the request for reexamination for their explanation of the teaching provided in MacGregor, which was not present in the prosecution of the application which became the '890 Patent. Further, there is a substantial likelihood that a reasonable examiner would consider this teaching important in deciding whether or not the claims are patentable. Accordingly, MacGregor raises a substantial new question of patentability as to independent claim 1, which question has not been decided in a previous examination of the '890 Patent. Further, because MacGregor is seen to raise an SNQ with respect to independent claim 1, the reference of MacGregor is additionally seen to raise an SNQ with respect to claims 2-10, which are each directly or indirectly dependent on claim 1, and which include each of the limitations of independent claim 1 by virtue of their dependency.

11. Continuing, with respect to the proposed SNQ#3, noted above, it is also agreed that the May reference in view of Tsuchiya raise a substantial new question of patentability as to independent claim 1 of the '890 Patent. The May reference describes a microprocessor (see Fig. 1) having an arithmetic logic unit connected to a push down stack register (see Fig. 2, A, B, and C registers). Further, as pointed out by the Third Party Requester, Tsuchiya describes a microprocessor further including a separate direct memory access central processing unit (see col. 4, line 51-col. 5, line 52). Thus, the combination, as proposed by the Third Party Requestor, would appear to teach the limitation that requires a microprocessor having the claimed

architecture. The additional passages regarding the limitations of claim 1, as described in May and Tsuchiya, pointed out in the Request for Reexamination in the claim chart on pages 26 through 32, are hereby incorporated by reference from the request for reexamination for their explanation of the teaching provided in May and Tsuchiya, which were not present in the prosecution of the application which became the '890 Patent. Further, there is a substantial likelihood that a reasonable examiner would consider these teachings important in deciding whether or not the claim is patentable. Accordingly, May and Tsuchiya raise a substantial new question of patentability as to independent claim 1, which question has not been decided in a previous examination of the '890 Patent. Further, because May and Tsuchiya are seen to raise an SNQ with respect to independent claim 1, the references of May and Tsuchiya are additionally seen to raise an SNQ with respect to claims 2-10, which are each directly or indirectly dependent on claim 1, and which include each of the limitations of independent claim 1 by virtue of their dependency.

Waiver of Right to File Patent Owner Statement

12. In a reexamination proceeding, Patent Owner may waive the right under 37 C.F.R. 1.530 to file a Patent Owner Statement. The document needs to contain a statement that Patent Owner waives the right under 37 C.F.R. 1.530 to file a Patent Owner Statement and proof of service in the manner provided by 37 C.F.R. 1.248, if the request for reexamination was made by a third party requester, see 37 C.F.R 1.550(f). The Patent Owner may consider using the following statement in a document waiving the right to file a Patent Owner Statement:

WAIVER OF RIGHT TO FILE PATENT OWNER STATEMENT

Patent Owner waives the right under 37 C.F.R. 1.530 to file a Patent Owner Statement.

Extensions of Time

13. Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that *ex parte* reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extensions of time in *ex parte* reexamination proceedings are provided for in 37 CFR 1.550(c).

Amendment in Reexamination Proceedings

14. Patent owner is notified that any proposed amendment to the specification and/or claims in this reexamination proceeding must comply with 37 CFR 1.530(d)-(j), must be formally presented pursuant to 37 CFR 1.52(a) and (b), and must contain any fees required by 37 CFR 1.20(c). See MPEP § 2250(IV) for examples to assist in the preparation of proper proposed amendments in reexamination proceedings.

Submissions

15. In order to insure full consideration of any amendments, affidavits or declarations or other documents as evidence of patentability, such documents must be submitted in response to the first Office action on the merits (which does not result in a close of prosecution). Submissions after the second Office action on the merits, which is intended to be a final action, will be governed by the requirements of 37 CFR 1.116, after final rejection and by 37 CFR 41.33 after appeal, which will be strictly enforced.

Conclusion

16. **Claims 1-10** of U.S. Patent Number 5,530,890 are subject to reexamination.

17. The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent No. 5,530,890 throughout the course of this reexamination proceeding. See MPEP §§ 2207, 2282 and 2286.

18. ALL correspondence relating to this ex parte reexamination proceeding should be directed as follows:

Please mail any communications to:

Attn: Mail Stop "Ex Parte Reexam"
Central Reexamination Unit
Commissioner for Patents
P. O. Box 1450
Alexandria VA 22313-1450

Please FAX any communications to:

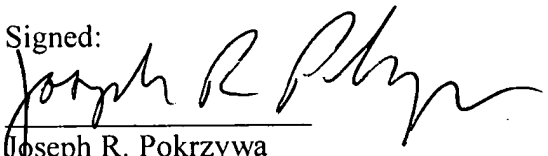
(571) 273-9900
Central Reexamination Unit

Please hand-deliver any communications to:

Customer Service Window
Attn: Central Reexamination Unit
Randolph Building, Lobby Level
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

Signed:



Joseph R. Pokrzywa
Primary Examiner
Central Reexamination Unit 3992
(571) 272-7410

Conferees: */Sue Lao/* */Roland G. Foster/*

Sue Lao

EXHIBIT B

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/009,388	01/16/2009	5530890	0081-011D1X1	7136

40972 7590 11/05/2009

HENNEMAN & ASSOCIATES, PLC
70 N. MAIN ST.
THREE RIVERS, MI 49093

EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 11/05/2009

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CENTRAL REEXAMINATION UNIT

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/009,388*.

PATENT NO. *5530890*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Office Action in Ex Parte Reexamination	Control No. 90/009,388	Patent Under Reexamination 5530890	
	Examiner JOSEPH R. POKRZYWA	Art Unit 3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

a☐ Responsive to the communication(s) filed on _____ . b☐ This action is made FINAL.
c☐ A statement under 37 CFR 1.530 has not been received from the patent owner.

A shortened statutory period for response to this action is set to expire 2 month(s) from the mailing date of this letter. Failure to respond within the period for response will result in termination of the proceeding and issuance of an *ex parte* reexamination certificate in accordance with this action. 37 CFR 1.550(d). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).** If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☐ Information Disclosure Statement, PTO/SB/08.
3. ☐ Interview Summary, PTO-474.
4. ☐ _____.

Part II SUMMARY OF ACTION

1a. ☒ Claims 1-10 are subject to reexamination.
1b. ☐ Claims _____ are not subject to reexamination.
2. ☐ Claims _____ have been canceled in the present reexamination proceeding.
3. ☒ Claims 9 and 10 are patentable and/or confirmed.
4. ☒ Claims 1-8 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ The drawings, filed on _____ are acceptable.
7. ☐ The proposed drawing correction, filed on _____ has been (7a)☐ approved (7b)☐ disapproved.
8. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
   a)☐ All b)☐ Some* c)☐ None of the certified copies have
   1☐ been received.
   2☐ not been received.
   3☐ been filed in Application No. _____ .
   4☐ been filed in reexamination Control No. _____.
   5☐ been received by the International Bureau in PCT application No. _____.
   * See the attached detailed Office action for a list of the certified copies not received.
9. ☐ Since the proceeding appears to be in condition for issuance of an *ex parte* reexamination certificate except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte* Quayle, 1935 C.D. 11, 453 O.G. 213.
10. ☐ Other: _____

cc: Requester (if third party requester)

DETAILED ACTION

Brief Summary of Proceedings

1. Claims 1-10 originally issued in U.S. Patent 5,530,890 (hereafter "the '890 Patent") on Jun. 25, 1996. On 1/16/2009, the Third Party requested *ex parte* reexamination of claims 1-10 of the '890 Patent. On 4/8/2009, an order for reexamination of claims 1-10 was mailed. The examiner notes that claim 1 is the only independent claim of the '890 Patent.

Discussion of Prior Art of Record

2. The examiner notes that the Third Party Requester cites in the Request for Reexamination dated 1/16/2009 two main primary references, with the first being the article "The Motorola MC68020", authored by MacGregor *et al.*, and published in August 1984 (noted as "MacGregor"), and the second being U.S. Patent Number 4,758,948, issued to May *et al.* (noted herein as the "May'948 Patent"). However, both of these references are seen to fall short of teaching each of the limitations of the specific claimed architecture of independent claim 1 of the '890 Patent.

3. For instance, there is no specific disclosure in the MacGregor reference of a push down stack that "is connected to provide inputs to said arithmetic logic unit, an output of the ALU being connected to the top item register in the push down stack, with the top item register also

being connected to provide inputs to an internal data bus". The disclosure of MacGregor is unclear of teaching of the specific connections required in the current claim language. Thus, the reference by itself falls short of anticipating the claim language. Further, both the MacGregor reference and the May reference are unclear if the microprocessor comprises a main CPU and a separate DMA CPU in a single integrated circuit.

4. The specification of the '890 Patent describes this feature as being "another unusual aspect to the high performance microprocessor 50", and describes the on-chip RAM gives a performance equal to that obtained with the use of static RAMs, at a quarter of the cost. Thus, the examiner notes that this is believed to be a key feature in the invention claimed in the '890 Patent. The reference of MacGregor states on page 107 that "The reduced bus utilization by the MC68020 also increases system performance by providing more bus bandwidth for other masters such as DMA devices." However, with this statement, MacGregor does not specify and is not clear that a DMU CPU is included in a single integrated circuit as the main CPU within a microprocessor. Similarly, the reference of the May'948 Patent does not disclose of a DMA CPU being on the same integrated circuit as a main CPU. The Third Party Requester stated in the Request that "Onc skilled in the art would have understood that he May transputer system had a MEM REQUEST pin that was specifically configured to be coupled to a DMA controller." However, with this, there is still no specific disclosure within the May'948 Patent itself that expressly states of a DMA controller being on the same integrated circuit as a main CPU.

5. However, upon review of the references submitted in the Request for Reexamination, the examiner notes that the reference of the "Transputer Reference Manual", published by Inmos Ltd., 1988 (hereafter the "Transputer Manual"), is seen to describe an on-chip DMA controller. Thus, a rejection of independent claim 1 follows that utilizes the May'948 Patent, which incorporates by reference the reference of U.S. Patent Number 4,680,698, issued to Edwards *et al.* (hereafter the "Edwards'698 Patent"), and further in view of the "Transputer Reference Manual", published by Inmos Ltd., 1988 (hereafter the "Transputer Manual").

6. Further, also upon review of the references cited in the Request for Reexamination on page 11 (as well as pages 26 and 27) that teach of on-chip DMA controllers, the examiner notes that the reference of U.S. Patent 4,989,113, issued to Hull, Jr. *et al.* can be interpreted as teaching the other features that are required by the current claim language. Thus an additional rejection follows which utilizes this reference, and is discussed more fully below.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. **Claims 1-6** are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Number 4,989,113, issued to Hull, Jr. *et al.* (hereafter "Hull").

Regarding ***claim 1***, Hull Jr. discloses a microprocessor [see Abstract], which comprises

a main central processing unit [CPU 12 and controller 14] and a separate direct memory access central processing unit [DMA control 22] in a single integrated circuit comprising said microprocessor [see Fig. 1],

said main central processing unit [CPU 12 and controller 14] having an arithmetic logic unit [see Fig. 2, ALU 48],

a first push down stack [data registers 50a through 50h, collectively referred to as registers 50] with a top item register [data register 50a] and a next item register [data register 50b], connected to provide inputs to said arithmetic logic unit [see Fig. 2; also see col. 8, lines 51-55],

an output of said arithmetic logic unit being connected to said top item register [see Fig. 2],

said top item register also being connected to provide inputs to an internal data bus [see col. 8, lines 51-55],

said internal data bus being bidirectionally connected to a loop counter [see col. 9, lines 54-67],

said loop counter being connected to a decrementer [see col. 9, lines 54-67, whereby "CPU 12 interprets the absence of a displacement signal as an increment or decrement the contents of register 54 used in repetitive operation."],

said internal data bus being bidirectionally connected to a stack pointer [see col. 16, lines 23-55, whereby the system utilizes a "pipelining" of the instruction codes], return stack pointer [see col. 9,lines 36-67], mode register [index registers 68a and 68b, se col. 10, lines 33-55] and instruction register [auxiliary register 54, see col. 9, lines 4-61],

said internal data bus being connected to a memory controller [controller 14, see Figs. 1 and 4],

to a Y register of a return push down stack [registers 68, see col. 10, line 33-col. 11, line 14],

an X register [register 205] and a program counter [program counter 92, see col. 16, line 22-col. 18, line 9],

said Y register, X register and program counter providing outputs to an internal address bus [see Figs. 1, 2, and 4],

said internal address bus providing inputs to said memory controller and to an incrementer [see col. 17, line 60-col. 18, line 9],

said incrementer being connected to said internal data bus [see col. 16, lines 38-55],

said direct memory access central processing unit [DMA control 22] providing inputs to said memory controller [controller 14, see Figs. 1 and 4, also see col. 18, lines 10-53],

said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory [see Fig. 1, RAMs 16 and 18].

Regarding ***claim 2***, Hull, Jr. discloses the microprocessor discussed above in claim 1, and further teaches that said memory controller includes a multiplexing means [interface ports 24 and 26] between said central processing unit and said address/data bus [see Figs. 1 and 3], said multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus [see col. 13, line 38-col. 14, line 46].

Regarding ***claim 3***, Hull, Jr. discloses the microprocessor discussed above in claim 1, and further teaches that said memory controller includes means for fetching instructions for said central processing unit on said address/data bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle [see col. 13, lines 26-37].

Regarding ***claim 4***, Hull, Jr. discloses the microprocessor discussed above in claim 3, and further teaches of means connected to said means for fetching instructions for determining if multiple instructions fetched by said means for fetching instructions require a memory access [see col. 13, lines 26-37], said means for fetching instructions fetching additional multiple instructions if the multiple instructions do not require a memory access [see col. 13, lines 26-37].

Regarding ***claim 5***, Hull, Jr. discloses the microprocessor discussed above in claim 3, and further teaches that said microprocessor and a dynamic random access memory are contained in a single integrated circuit [see Fig. 1] and said means for fetching instructions includes a column latch for receiving the multiple instructions [instruction cache 36, see Fig. 1; also see col. 5, line 41-col. 6, line 12].

Regarding ***claim 6***, Hull, Jr. discloses the microprocessor discussed above in claim 1, and further teaches that said microprocessor includes a sensing circuit and a driver circuit [interrupt logic 250], and an output enable line for connection between the random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level [see col. 18, lines 10-53], said microprocessor being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal [see col. 18, lines 10-53].

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claims 1-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Number 4,758,948, issued to May *et al.* (hereafter "May'948"), which incorporates by reference the reference of U.S. Patent Number 4,680,698, issued to Edwards *et al.* (hereafter Edwards'698 Patent"), further in view of the "Transputer Reference Manual", published by Inmos Ltd., 1988 (hereafter the "Transputer Manual").

Regarding ***claim 1***, May'948 discloses a microprocessor [see Fig. 1], which comprises

a main central processing unit [CPU 12, see Figs. 1 and 2] and *a separate memory access processing unit* [external memory interface 23, seen in Fig. 1] in a single integrated circuit comprising said microprocessor [see Fig. 1],

said main central processing unit [CPU 12, see Figs. 1 and 2] having an arithmetic logic unit [see Fig. 2, ALU 30, also see col. 4, lines 52 and 53, wherein "The CPU 12 incorporates an arithmetic logic unit (ALU)..."],

a first push down stack [see Fig. 2, whereby the A, B and C registers 54, 55, and 56, respectively, within the Priority 1 register bank operate as a first push down stack] with a top item register [A register 54] and a next item register [B register 55], connected to provide inputs to said arithmetic logic unit [see col. 8, lines 47-56, wherein "The A, B, and C register stack 54,

55, and 56 are the sources and destinations for most arithmetic and logical operations. They are organised as a stack so that the loading of a value into the A register is preceded by relocating the existing contents of the B register into the C register and from the A register into the B register. Similarly storing a value derived from the A register causes the contents of the B register to be moved into the A register and the contents of the C register into the B register."],

an output of said arithmetic logic unit being connected to said top item register [see Fig. 2, whereby the Z bus includes an output from the ALU 30 and an input to the A register 54],

said top item register also being connected to provide inputs to an internal data bus [see Fig. 2, whereby the data bus 31 is connected to the A register 54],

said internal data bus [data bus 31] being bidirectionally connected to a loop counter [being interpreted as the workspace pointer WPTR REG register 51 and the O REG register 57, seen in Fig. 3, whereby the Edwards'698 Patent states on cols. 15 and 16 within the procedure "load from workspace and increment (function code 3)", the purpose of the function includes "to facilitate the use of workspace locations as loop counters, incrementing towards zero", and includes the definition "WPTR + OREG := AREG + 1"],

said loop counter being connected to a decrementer [the Edwards'698 Patent states on cols. 15 and 16 within the procedure "load from workspace and increment (function code 3)", the purpose of the function includes "to facilitate the use of workspace locations as loop counters, incrementing towards zero", thereby effectively acting as a decrementer],

said internal data bus [data bus 31] being bidirectionally connected to a stack pointer [see Fig. 3 IPTR S 65, also see col. 9, lines 59-68, wherein "Location 65 is used when a process is not the current process to hold a pointer (IPTR) to the next instruction to be executed by the process when it becomes the current process."], return stack pointer [see Fig. 3, LINK S 66, also see col. 9, lines 59-68, wherein "Location 66 is used to store a workspace pointer of a next process on a link list or queue of processes awaiting execution."], mode register [see Fig. 3, STATE S 67, also see col. 9, lines 59-68, wherein "Location 67 is normally used to contain an indication of the state of a process performing an alternative input operation or as a pointer for copying of a block of data."; additionally see col. 7, line 69-col. 8, line 7, wherein "PRI FLAG" is a "1 bit register or flag 47 for indicating the priority 0 or 1 of the currently executing process."] and instruction register [IB Reg 34, also see col. 7, lines 29-31, wherein "Each instruction derived from the program sequence for the process is fed to an instruction buffer 34."],

said internal data bus being connected to a memory controller [memory interface 14],

to a Y register of a return push down stack [BPTR REG 52, see Figs. 2 and 4],

an X register [FPTR REG 53, see Figs. 2 and 4] and a program counter [byte counter 111, see Fig. 12],

said Y register, X register and program counter providing outputs to an internal address bus [Z bus 81, see Figs. 2, 12, and 13],

said internal address bus providing inputs to said memory controller and to an incrementer [see col. 12, lines 35-54, wherein "the pointer register 122 incorporates an

incrementor so that as each byte is received the pointer increments to the memory destination address for the next byte of the input message."; also see Fig. 13],

said incrementer being connected to said internal data bus [see Fig. 13],

s*aid memory access processing unit* [external memory interface 23, seen in Fig. 1] providing inputs to said memory controller [see Fig. 1 and 2, whereby external memory interface 23 provides inputs to the memory interface 14],

said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory [see Fig. 10, whereby memory interface 14 has an address/data bus 33 and 31, and also a plurality if control lines providing input to RAM, see Fig. 1].

However, the May'948 Patent does not expressly state if the *separate memory access processing unit* is a separate direct memory access central processing unit being in a single IC with the main central processing unit, and subsequently, if said direct memory access central processing unit provides inputs to said memory controller.

The Transputer Manual discloses a microprocessor [see Figure 1.1 on page 108], which comprises

a main central processing unit [32 bit Processor, see Figure 1.1 on page 108] and a separate direct memory access central processing unit [see page 150, wherein "DMA may also inhibit an internally running program from accessing external memory....DMA allows a bootstrap program to be loaded into external RAM ready for execution after reset."; also see pages 132-151, which shows various configurations of the EMI] in a single integrated circuit

comprising said microprocessor [see page 150, whereby the External Memory Interface allows for the programmed control of direct memory access; see Figure 1.1 on page 108],

said main central processing unit having a first push down stack [the A, B, and C registers, seen in Figs. 3.1 and 3.3; also see page 11, wherein "The A, B and C registers which form an evaluation stack."] with a top item register [Register A] and a next item register [B register], connected to provide inputs to said arithmetic logic unit [see page 111, wherein A, B, and C are sources and destinations for most arithmetic and logical operations. Loading a value into the stack pushes B into C, and A into B, before loading A."],

an internal data bus being bidirectionally connected to a loop counter [see page 115, wherein "This uses a workspace locator as a counter of the parallel construct components which have still to terminate. The counter is initialized to the number of components before the process is started. Each component ends with an end process instruction which decrements and tests the counter. For all but the last component, the counter is non-zero and the component is descheduled. For the last component, the counter is zero, and the main process continues."],

said loop counter being connected to a decrementer [see page 115],

said direct memory access central processing unit [being the External Memory Interface, seen in Fig. 1.1 on page 108] providing inputs to said memory controller [see page 108, whereby the External Memory Interface provides an input to the 32-bit Processor],

said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory [see Fig. 1.1 on page 108].

The May'948 Patent & the Transputer Manual are combinable because they are from the same field of endeavor, both being drawn to an Inmos Transputer microprocessor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the DMA teachings described in the Transputer Manual within the system described the May'948 Patent. The suggestion/motivation for doing so would have been that the system described in the May'948 Patent would be easily adapted to incorporate the direct memory access controller teachings described in the Transputer Manual, as the components and systems appear to be identical. Therefore, it would have been obvious to combine the teachings of the Transputer Manual with the system of the May'948 Patent to obtain the invention as specified in claim 1.

Regarding ***claim 2***, the May'948 Patent and the Transputer Manual disclose the microprocessor discussed above in claim 1, and the May'948 Patent further teaches that said memory controller includes a multiplexing means [condition multiplexor 36, seen in Fig. 2] between said central processing unit and said address/data bus [see Fig. 2], said multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus [see col. 7, lines 32-35]. Additionally, the Transputer Manual further teaches of including a multiplexing means [see Fig. 7.8 on page 140, Row/Column address multiplexer], with said multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus [see Fig. 7.8 on page 140, Row/Column address multiplexer].

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the multiplexer teachings described in the Transputer Manual within the system described the May'948 Patent. The suggestion/motivation for doing so would have been that the system described in the May'948 Patent would be easily adapted to incorporate the further teachings described in the Transputer Manual, as the components and systems appear to be identical. Therefore, it would have been obvious to combine the further teachings of the Transputer Manual with the system of the May'948 Patent to obtain the invention as specified in claim 2.

Regarding ***claim 3***, the May'948 Patent and the Transputer Manual disclose the microprocessor discussed above in claim 1, and the May'948 Patent further teaches that said memory controller includes means for fetching instructions for said central processing unit on said address/data bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle [see col. 6, lines 4-24; also see col. 7, lines 15-39].

Regarding ***claim 4***, the May'948 Patent and the Transputer Manual disclose the microprocessor discussed above in claim 3, and the May'948 Patent further teaches of means connected to said means for fetching instructions for determining if multiple instructions fetched by said means for fetching instructions require a memory access [see col. 6, lines 4-24; also see col. 7, lines 15-39], said means for fetching instructions fetching additional multiple instructions

if the multiple instructions do not require a memory access [see col. 6, lines 4-24; also see col. 7, lines 15-39].

11. **Claims 7 and 8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hull, Jr. in view of Kato *et al.* (U.S. Patent Number 4,766,567).

Regarding ***claim 7***, Hull, Jr. discloses the microprocessor discussed above in claim 1, and further teaches of **a system clock** to said main central processing unit, said main central processing unit and **said system clock** being provided in a single integrated circuit [see Figs. 1 and 4, being clock generator 200, seen in Fig. 4, and read in col. 15, lines 7-27].

However, Hull, Jr. does not expressly describe the system clock as being a ring oscillator variable speed system clock connected to said main central processing unit, with the main central processing unit and the ring oscillator variable speed system clock being provided in a single integrated circuit.

Kato discloses a microprocessor having a ring oscillator variable speed system clock connected to said main central processing unit, said main central processing unit and said ring oscillator variable speed system clock being provided in a single integrated circuit [clock generator 4, see Figs. 1 and 4; also see col. 10, line 51-col. 11, line 7].

Hull, Jr. & Kato are combinable because they are from the same field of endeavor, being semiconductor systems having two distinct clock generators. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the ring oscillator teachings of Kato in the system taught by Hull, Jr. The suggestion/motivation for doing so would have been that the clock generator of Hull, Jr. would become more efficient, as using a ring oscillator would lower output frequency in proportion to the speed of the data processing circuit which is also lowered due to the drop of power supply voltage, being a characteristic of using a ring oscillator recognized by Kato on col. 11, lines 2-7. Therefore, it would have been obvious to combine the ring oscillator teachings of Kato with the system of Hull, Jr. to obtain the invention as specified in claim 7.

Regarding ***claim 8***, Hull, Jr. and Kato disclose the microprocessor discussed above in claim 7, and Hull, Jr. further teaches that said memory controller includes an input/output interface connected to exchange coupling control signals, addresses and data with said main central processing unit [see Fig. 1], said microprocessor additionally including a second clock independent [timer 40] of said ring oscillator variable speed system clock connected to said input/output interface [whereby timer 40 is independent of clock generator 200, seen in Figs. 1 and 4].

STATEMENT OF REASONS FOR PATENTABILITY AND/OR CONFIRMATION

The following is an examiner's statement of reasons for patentability and/or confirmation of the claims found patentable in this reexamination proceeding:

Claims 9 and 10 are confirmed as patentable.

Regarding dependent ***claim 9***, the examiner does believe that the prior art of record expressly discloses the invention as claimed, particularly including the feature requiring the first push down stack has a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit. The prior art of Hull, Jr. teaches of stack elements, as seen in Fig. 2. However, Hull, Jr. fails to expressly teach of a third stack element configured as a RAM external to the single integrated circuit. Further, the reference of Muller (U.S. Patent 4,969,091), noted in the Request for Reexamination, teaches of implementing a push down stack. But, Muller fails to expressly teach the architecture that is required by the claim language, which requires a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit. Thus,

the prior art of record is not seen to expressly disclose this architecture. Therefore, in the examiner's opinion, the claim is deemed patentable.

Any comments considered necessary by PATENT OWNER regarding the above statement must be submitted promptly to avoid processing delays. Such submission by the patent owner should be labeled: "Comments on Statement of Reasons for Patentability and/or Confirmation" and will be placed in the reexamination file.

Conclusion

12. Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that *ex parte* reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extensions of time in *ex parte* reexamination proceedings are provided for in 37 CFR 1.550(c).

13. In order to ensure full consideration of any amendments, affidavits or declarations, or other documents as evidence of patentability, such documents must be submitted in response to this Office action. Submissions after the next Office action, which is intended to be a final action, will be governed by the requirements of 37 CFR 1.116, after final rejection and 37 CFR 41.33 after appeal, which will be strictly enforced.

14. The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent No. 5,530,890 throughout the course of this reexamination proceeding.

15. ALL correspondence relating to this ex parte reexamination proceeding should be directed as follows:

Please mail any communications to:

Attn: Mail Stop "Ex Parte Reexam"
Central Reexamination Unit
Commissioner for Patents
P. O. Box 1450
Alexandria VA 22313-1450

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Registered users of EFS-Web may alternatively submit such correspondence via the electronic filing system EFS-Web, at https://sportal.uspto.gov/authenticate/authenticateuserlocalepf.html. EFS-Web offers the benefit of quick submission to the particular area of the Office that needs to act on the correspondence. Also, EFS-Web submissions are "soft scanned" (i.e., electronically uploaded) directly into the official file for the reexamination proceeding, which offers parties the opportunity to review the content of their submissions after the "soft scanning" process is complete.

Any inquiry concerning this communication should be directed to Joseph R. Pokrzywa at telephone number 571-272-7410.

Signed:

Joseph R. Pokrzywa
Primary Examiner
Central Reexamination Unit 3992
(571) 272-7410

Conferees:

/r.g.f./ OPQA

EXHIBIT C

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/009,388	01/16/2009	5530890	0081-011D1X1	7136

40972 7590 04/29/2010

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EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 04/29/2010

Please find below and/or attached an Office communication concerning this application or proceeding.

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CENTRAL REEXAMINATION UNIT

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/009,388*.

PATENT NO. *5530890*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Office Action in Ex Parte Reexamination	Control No. 90/009,388	Patent Under Reexamination 5530890	
	Examiner JOSEPH R. POKRZYWA	Art Unit 3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

a☒ Responsive to the communication(s) filed on *05 January 2010* . b☒ This action is made FINAL.
c☐ A statement under 37 CFR 1.530 has not been received from the patent owner.

A shortened statutory period for response to this action is set to expire *2* month(s) from the mailing date of this letter. Failure to respond within the period for response will result in termination of the proceeding and issuance of an *ex parte* reexamination certificate in accordance with this action. 37 CFR 1.550(d). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).** If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☐ Information Disclosure Statement, PTO/SB/08.
3. ☐ Interview Summary, PTO-474.
4. ☐ _____.

Part II SUMMARY OF ACTION

1a. ☒ Claims *1-10* are subject to reexamination.
1b. ☐ Claims _____ are not subject to reexamination.
2. ☐ Claims _____ have been canceled in the present reexamination proceeding.
3. ☐ Claims *9 and 10* are patentable and/or confirmed.
4. ☐ Claims *1-8* are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ The drawings, filed on _____ are acceptable.
7. ☐ The proposed drawing correction, filed on _____ has been (7a)☐ approved (7b)☐ disapproved.
8. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
   a)☐ All b)☐ Some* c)☐ None of the certified copies have
   1☐ been received.
   2☐ not been received.
   3☐ been filed in Application No. _____ .
   4☐ been filed in reexamination Control No. _____.
   5☐ been received by the International Bureau in PCT application No. _____.
   * See the attached detailed Office action for a list of the certified copies not received.
9. ☐ Since the proceeding appears to be in condition for issuance of an *ex parte* reexamination certificate except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte* Quayle, 1935 C.D. 11, 453 O.G. 213.
10. ☐ Other: _____

cc: Requester (if third party requester)

DETAILED ACTION

Response to Request for Reconsideration

1. The Patent Owner's response was received on 1/5/2010, and has been entered and made of record. Currently, claims 1-10 of U.S. Patent Number 5,530,890 (hereafter "the '890 Patent") are pending.

2. Original claims 1-10 issued in the '890 Patent on Jun. 25, 1996. On 1/16/2009, the Third Party requested *ex parte* reexamination of claims 1-10 of the '890 Patent, whereby an order for reexamination of claims 1-10 was mailed on 4/8/2009. The Patent Owner's current response dated 1/5/2010 was received in response to the first non-final Office action dated 11/5/2009. In the Office action dated 11/5/2009, claims 1-8 of the '890 Patent were rejected, and claims 9 and 10 of the '890 Patent were indicated as being patentable, whereby the examiner notes that claim 1 is the only independent claim of the '890 Patent.

Claim Rejections - 35 USC § 102

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. **Claims 1-6** are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Number 4,989,113, issued to Hull, Jr. *et al.* (hereafter "Hull, Jr.").

Regarding ***claim 1***, Hull Jr. discloses a microprocessor [see Abstract], which comprises

a main central processing unit [CPU 12 and controller 14] and a separate direct memory access central processing unit [DMA control 22] in a single integrated circuit comprising said microprocessor [see Fig. 1],

said main central processing unit [CPU 12 and controller 14] having an arithmetic logic unit [see Fig. 2, ALU 48],

a first push down stack [data registers 50a through 50h, collectively referred to as registers 50] with a top item register [data register 50a] and a next item register [data register 50b], connected to provide inputs to said arithmetic logic unit [see Fig. 2; also see col. 8, lines 51-55],

an output of said arithmetic logic unit being connected to said top item register [see Fig. 2],

said top item register also being connected to provide inputs to an internal data bus [see col. 8, lines 51-55],

said internal data bus being bidirectionally connected to a loop counter [see col. 9, lines 54-67],

said loop counter being connected to a decrementer [see col. 9, lines 54-67, whereby "CPU 12 interprets the absence of a displacement signal as an increment or decrement the contents of register 54 used in repetitive operation."],

said internal data bus being bidirectionally connected to a stack pointer [see col. 16, lines 23-55, whereby the system utilizes a "pipelining" of the instruction codes], return stack pointer [see col. 9,lines 36-67], mode register [index registers 68a and 68b, se col. 10, lines 33-55] and instruction register [auxiliary register 54, see col. 9, lines 4-61],

said internal data bus being connected to a memory controller [controller 14, see Figs. 1 and 4],

to a Y register of a return push down stack [registers 68, see col. 10, line 33-col. 11, line 14],

an X register [register 205] and a program counter [program counter 92, see col. 16, line 22-col. 18, line 9],

said Y register, X register and program counter providing outputs to an internal address bus [see Figs. 1, 2, and 4],

said internal address bus providing inputs to said memory controller and to an incrementer [see col. 17, line 60-col. 18, line 9],

said incrementer being connected to said internal data bus [see col. 16, lines 38-55],

said direct memory access central processing unit [DMA control 22] providing inputs to said memory controller [controller 14, see Figs. 1 and 4, also see col. 18, lines 10-53],

said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory [see Fig. 1, RAMs 16 and 18].

Regarding ***claim 2***, Hull, Jr. discloses the microprocessor discussed above in claim 1, and further teaches that said memory controller includes a multiplexing means [interface ports 24 and 26] between said central processing unit and said address/data bus [see Figs. 1 and 3], said multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus [see col. 13, line 38-col. 14, line 46].

Regarding ***claim 3***, Hull, Jr. discloses the microprocessor discussed above in claim 1, and further teaches that said memory controller includes means for fetching instructions for said central processing unit on said address/data bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle [see col. 13, lines 26-37].

Regarding ***claim 4***, Hull, Jr. discloses the microprocessor discussed above in claim 3, and further teaches of means connected to said means for fetching instructions for determining if multiple instructions fetched by said means for fetching instructions require a memory access [see col. 13, lines 26-37], said means for fetching instructions fetching additional multiple instructions if the multiple instructions do not require a memory access [see col. 13, lines 26-37].

Regarding ***claim 5***, Hull, Jr. discloses the microprocessor discussed above in claim 3, and further teaches that said microprocessor and a dynamic random access memory are contained in a single integrated circuit [see Fig. 1] and said means for fetching instructions includes a column latch for receiving the multiple instructions [instruction cache 36, see Fig. 1; also see col. 5, line 41-col. 6, line 12].

Regarding ***claim 6***, Hull, Jr. discloses the microprocessor discussed above in claim 1, and further teaches that said microprocessor includes a sensing circuit and a driver circuit [interrupt logic 250], and an output enable line for connection between the random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level [see col. 18, lines 10-53], said microprocessor being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal [see col. 18, lines 10-53].

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. **Claims 1-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Number 4,758,948, issued to May *et al.* (hereafter "May'948"), which incorporates by reference the reference of U.S. Patent Number 4,680,698, issued to Edwards *et al.* (hereafter Edwards'698 Patent"), further in view of the "Transputer Reference Manual", published by Inmos Ltd., 1988 (hereafter the "Transputer Manual").

Regarding ***claim 1***, May'948 discloses a microprocessor [see Fig. 1], which comprises

a main central processing unit [CPU 12, see Figs. 1 and 2] and *a separate memory access processing unit* [external memory interface 23, seen in Fig. 1] in a single integrated circuit comprising said microprocessor [see Fig. 1],

said main central processing unit [CPU 12, see Figs. 1 and 2] having an arithmetic logic unit [see Fig. 2, ALU 30, also see col. 4, lines 52 and 53, wherein "The CPU 12 incorporates an arithmetic logic unit (ALU)..."],

a first push down stack [see Fig. 2, whereby the A, B and C registers 54, 55, and 56, respectively, within the Priority 1 register bank operate as a first push down stack] with a top item register [A register 54] and a next item register [B register 55], connected to provide inputs to said arithmetic logic unit [see col. 8, lines 47-56, wherein "The A, B, and C register stack 54, 55, and 56 are the sources and destinations for most arithmetic and logical operations. They are

organised as a stack so that the loading of a value into the A register is preceded by relocating the existing contents of the B register into the C register and from the A register into the B register. Similarly storing a value derived from the A register causes the contents of the B register to be moved into the A register and the contents of the C register into the B register."],

an output of said arithmetic logic unit being connected to said top item register [see Fig. 2, whereby the Z bus includes an output from the ALU 30 and an input to the A register 54],

said top item register also being connected to provide inputs to an internal data bus [see Fig. 2, whereby the data bus 31 is connected to the A register 54],

said internal data bus [data bus 31] being bidirectionally connected to a loop counter [being interpreted as the workspace pointer WPTR REG register 51 and the O REG register 57, seen in Fig. 3, whereby the Edwards'698 Patent states on cols. 15 and 16 within the procedure "load from workspace and increment (function code 3)", the purpose of the function includes "to facilitate the use of workspace locations as loop counters, incrementing towards zero", and includes the definition "WPTR + OREG := AREG + 1"],

said loop counter being connected to a decrementer [the Edwards'698 Patent states on cols. 15 and 16 within the procedure "load from workspace and increment (function code 3)", the purpose of the function includes "to facilitate the use of workspace locations as loop counters, incrementing towards zero", thereby effectively acting as a decrementer],

said internal data bus [data bus 31] being bidirectionally connected to a stack pointer [see Fig. 3 IPTR S 65, also see col. 9, lines 59-68, wherein "Location 65 is used

when a process is not the current process to hold a pointer (IPTR) to the next instruction to be executed by the process when it becomes the current process."], return stack pointer [see Fig. 3, LINK S 66, also see col. 9, lines 59-68, wherein "Location 66 is used to store a workspace pointer of a next process on a link list or queue of processes awaiting execution."], mode register [see Fig. 3, STATE S 67, also see col. 9, lines 59-68, wherein "Location 67 is normally used to contain an indication of the state of a process performing an alternative input operation or as a pointer for copying of a block of data."; additionally see col. 7, line 69-col. 8, line 7, wherein "PRI FLAG" is a "1 bit register or flag 47 for indicating the priority 0 or 1 of the currently executing process."] and instruction register [IB Reg 34, also see col. 7, lines 29-31, wherein "Each instruction derived from the program sequence for the process is fed to an instruction buffer 34."],

said internal data bus being connected to a memory controller [memory interface 14],

to a Y register of a return push down stack [BPTR REG 52, see Figs. 2 and 4],

an X register [FPTR REG 53, see Figs. 2 and 4] and a program counter [byte counter 111, see Fig. 12],

said Y register, X register and program counter providing outputs to an internal address bus [Z bus 81, see Figs. 2, 12, and 13],

said internal address bus providing inputs to said memory controller and to an incrementer [see col. 12, lines 35-54, wherein "the pointer register 122 incorporates an incrementor so that as each byte is received the pointer increments to the memory destination address for the next byte of the input message."; also see Fig. 13],

said incrementer being connected to said internal data bus [see Fig. 13],

s*aid memory access processing unit* [external memory interface 23, seen in Fig. 1] providing inputs to said memory controller [see Fig. 1 and 2, whereby external memory interface 23 provides inputs to the memory interface 14],

said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory [see Fig. 10, whereby memory interface 14 has an address/data bus 33 and 31, and also a plurality if control lines providing input to RAM, see Fig. 1].

However, the May'948 Patent does not expressly state if the *separate memory access processing unit* is a separate direct memory access central processing unit being in a single IC with the main central processing unit, and subsequently, if said direct memory access central processing unit provides inputs to said memory controller.

The Transputer Manual discloses a microprocessor [see Figure 1.1 on page 108], which comprises

a main central processing unit [32 bit Processor, see Figure 1.1 on page 108] and a separate direct memory access central processing unit [see page 150, wherein "DMA may also inhibit an internally running program from accessing external memory....DMA allows a bootstrap program to be loaded into external RAM ready for execution after reset."; also see pages 132-151, which shows various configurations of the EMI] in a single integrated circuit

comprising said microprocessor [see page 150, whereby the External Memory Interface allows for the programmed control of direct memory access; see Figure 1.1 on page 108],

said main central processing unit having a first push down stack [the A, B, and C registers, seen in Figs. 3.1 and 3.3; also see page 11, wherein "The A, B and C registers which form an evaluation stack."] with a top item register [Register A] and a next item register [B register], connected to provide inputs to said arithmetic logic unit [see page 111, wherein A, B, and C are sources and destinations for most arithmetic and logical operations. Loading a value into the stack pushes B into C, and A into B, before loading A."],

an internal data bus being bidirectionally connected to a loop counter [see page 115, wherein "This uses a workspace locator as a counter of the parallel construct components which have still to terminate. The counter is initialized to the number of components before the process is started. Each component ends with an end process instruction which decrements and tests the counter. For all but the last component, the counter is non-zero and the component is descheduled. For the last component, the counter is zero, and the main process continues."],

said loop counter being connected to a decrementer [see page 115],

said direct memory access central processing unit [being the External Memory Interface, seen in Fig. 1.1 on page 108] providing inputs to said memory controller [see page 108, whereby the External Memory Interface provides an input to the 32-bit Processor],

said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory [see Fig. 1.1 on page 108].

The May'948 Patent & the Transputer Manual are combinable because they are from the same field of endeavor, both being drawn to an Inmos Transputer microprocessor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the DMA teachings described in the Transputer Manual within the system described the May'948 Patent. The suggestion/motivation for doing so would have been that the system described in the May'948 Patent would be easily adapted to incorporate the direct memory access controller teachings described in the Transputer Manual, as the components and systems appear to be identical. Therefore, it would have been obvious to combine the teachings of the Transputer Manual with the system of the May'948 Patent to obtain the invention as specified in claim 1.

Regarding ***claim 2***, the May'948 Patent and the Transputer Manual disclose the microprocessor discussed above in claim 1, and the May'948 Patent further teaches that said memory controller includes a multiplexing means [condition multiplexor 36, seen in Fig. 2] between said central processing unit and said address/data bus [see Fig. 2], said multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus [see col. 7, lines 32-35]. Additionally, the Transputer Manual further teaches of including a multiplexing means [see Fig. 7.8 on page 140, Row/Column address multiplexer], with said multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus [see Fig. 7.8 on page 140, Row/Column address multiplexer].

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the multiplexer teachings described in the Transputer Manual within the system described the May'948 Patent. The suggestion/motivation for doing so would have been that the system described in the May'948 Patent would be easily adapted to incorporate the further teachings described in the Transputer Manual, as the components and systems appear to be identical. Therefore, it would have been obvious to combine the further teachings of the Transputer Manual with the system of the May'948 Patent to obtain the invention as specified in claim 2.

Regarding ***claim 3***, the May'948 Patent and the Transputer Manual disclose the microprocessor discussed above in claim 1, and the May'948 Patent further teaches that said memory controller includes means for fetching instructions for said central processing unit on said address/data bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle [see col. 6, lines 4-24; also see col. 7, lines 15-39].

Regarding ***claim 4***, the May'948 Patent and the Transputer Manual disclose the microprocessor discussed above in claim 3, and the May'948 Patent further teaches of means connected to said means for fetching instructions for determining if multiple instructions fetched by said means for fetching instructions require a memory access [see col. 6, lines 4-24; also see col. 7, lines 15-39], said means for fetching instructions fetching additional multiple instructions

if the multiple instructions do not require a memory access [see col. 6, lines 4-24; also see col. 7, lines 15-39].

7. **Claims 7 and 8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hull, Jr. in view of Kato *et al.* (U.S. Patent Number 4,766,567, hereafter "Kato").

Regarding ***claim 7***, Hull, Jr. discloses the microprocessor discussed above in claim 1, and further teaches of **a system clock** to said main central processing unit, said main central processing unit and **said system clock** being provided in a single integrated circuit [see Figs. 1 and 4, being clock generator 200, seen in Fig. 4, and read in col. 15, lines 7-27].

However, Hull, Jr. does not expressly describe the system clock as being a ring oscillator variable speed system clock connected to said main central processing unit, with the main central processing unit and the ring oscillator variable speed system clock being provided in a single integrated circuit.

Kato discloses a microprocessor having a ring oscillator variable speed system clock connected to said main central processing unit, said main central processing unit and said ring oscillator variable speed system clock being provided in a single integrated circuit [clock generator 4, see Figs. 1 and 4; also see col. 10, line 51-col. 11, line 7].

Hull, Jr. & Kato are combinable because they are from the same field of endeavor, being semiconductor systems having two distinct clock generators. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the ring oscillator teachings of Kato in the system taught by Hull, Jr. The suggestion/motivation for doing so would have been that the clock generator of Hull, Jr. would become more efficient, as using a ring oscillator would lower output frequency in proportion to the speed of the data processing circuit which is also lowered due to the drop of power supply voltage, being a characteristic of using a ring oscillator recognized by Kato on col. 11, lines 2-7. Therefore, it would have been obvious to combine the ring oscillator teachings of Kato with the system of Hull, Jr. to obtain the invention as specified in claim 7.

Regarding ***claim 8***, Hull, Jr. and Kato disclose the microprocessor discussed above in claim 7, and Hull, Jr. further teaches that said memory controller includes an input/output interface connected to exchange coupling control signals, addresses and data with said main central processing unit [see Fig. 1], said microprocessor additionally including a second clock independent [timer 40] of said ring oscillator variable speed system clock connected to said input/output interface [whereby timer 40 is independent of clock generator 200, seen in Figs. 1 and 4].

Response to Arguments

8. Patent Owner's arguments filed 1/5/2010 have been fully considered but they are not persuasive.

9. In response to the Patent Owner's argument regarding the rejection of claims 1-6 under 35 U.S.C. 102(e) as being anticipated by the Hull, Jr. reference, the Patent Owner argues on page 2 that the Hull reference fails to expressly disclose "a first push down stack...to provide inputs to said arithmetic logic unit". The examiner notes that claim 1, being the only independent claim, currently requires that "said main processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus..." Thus, independent claim 1 requires the various connections of the various components, as the claim defines a structure of the components.

10. With this, as seen in Fig. 2, Hull shows a stack of registers 50. Continuing, in col. 7, lines 55-66, Hull states "data registers 50a through 50h (collectively referred to as data registers 50)..." Further, on col. 8, lines 47-55, Hull states "The primary function of data registers 50 is an accumulator function, so that the plurality of data registers 50 in effect provides CPU 12 with multiple accumulators." Therefore, the stack of registers 50, having a top item register 50a, and a next item register 50b, can be reasonably and broadly interpreted as "a first push down stack".

11. In this regard, MPEP 2111 [R-5], states, in part:

> During patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification." >The Federal Circuit's en banc decision in *Phillips v. AWH Corp.*, 415 F.3d 1303, 75 USPQ2d 1321 (Fed. Cir. 2005) expressly recognized that the USPTO employs the "broadest reasonable interpretation" standard:
>
> > The Patent and Trademark Office ("PTO") determines the scope of claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." In re Am. Acad. of Sci. Tech. Ctr., 367 F.3d 1359, 1364[, 70 USPQ2d 1827] (Fed. Cir. 2004). Indeed, the rules of the PTO require that application claims must "conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description." 37 CFR 1.75(d)(1).

12. With this, in the reference of Hull, the stack of registers 50, seen in Fig. 2, having a top item register 50a, and a next item register 50b, as discussed on col. 7, lines 55-66, can be broadly, and reasonably interpreted as "a first push down stack", being an interpretation that is consistent with the specification of the '890 Patent, as in the specification of the '890 Patent, particularly seen in Fig. 2, a top of stack register 76 and a next item register 78, being referred to as a "push down stack", are connected to an ALU 80.

13. Further, on page 3, the Patent Owner states that "Hull provides no indication that registers 50 operate as top and next item registers (as required by Claim 1) associated with stack elements located in memory as described, for example, in US'890's Fig. 21". However, the

examiner notes that claim 1 does not require any specific "operation" of the "top item register" and "next item register", nor of the "push down stack". Particularly, the current claim language requires a structure, and does not specify any function of the "first push down stack", the "top item register", or the "next item register", whereby claim 1 requires "said main processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, ...an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus..." There is no requirement of any operation performed by the "top item register" and the "next item register". Because the structure of Hull's stack of registers appears to be equivalent, and consistent to the stack of registers in Fig. 2 of the '890 Patent, as noted above, the limitation is seen to be reasonably interpreted by Hull. Therefore, Hull is seen as teaching of "said main processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus..."

14. Continuing, on page 3, the Patent Owner argues that the Hull reference fails to teach of a "stack pointer", as the Patent Owner argues that the program counter 92 of Hull, "is not a stack pointer". Claim 1 currently states "...said internal data bus being bidirectionally connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register,..." With this, the examiner notes that the current claim language does not require any specific operations or functionality of "a stack

pointer", and only requires that an internal data bus be bidirectionally connected to a stack pointer. There is no specific requirement that a "stack pointer" is associated with the "first push down stack", or if the "stack pointer" points "to a top of a data stack", as argued by the Patent Owner. If the Patent Owner wishes that these features be considered in interpreting the current claim language, then the claim must be amended accordingly.

15. Further, Hull states on col. 18, lines 46-53, "As is well known in the art for such an operation, controller 14 will cause the prior contents of program counter 92 to be stored in a predetermined memory location (generally called a "stack"), so that the location of the instruction code which would have been fetched next will be reloaded after the interrupt has been serviced." Additionally, as read in col. 10, lines 8-32, Hull states "instruction codes...including those listed in Table 1... "add" specifies the memory location to be addressed, "Arn" specifies the contents of one of registers 54, and "disp" the value of displacement code generated by controller 14. The updated value of the contents of one of auxiliary registers 54 is denoted by "ARn'" in Table 1." Thus, with this, the instruction codes appear to point to contents in a register stack. Further, as seen in Figs. 4 and 1 of Hull, the lines leading to the internal bus 34a from the program counter 92 are seen to be bidirectional. Therefore, Hull is seen to teach of "said internal data bus being bidirectionally connected to a stack pointer", as currently required in claim 1.

16. Therefore, the rejection of claims 1-6, as cited in the Office action dated 11/5/2009, under 35 U.S.C. 102(e) as being anticipated by Hull, is maintained and repeated in this Office action.

17. Continuing, with respect to the rejection of claims 1-4 under 35 USC 103(a) as being unpatentable over May'948, which incorporates by reference Edwards '698, and further in view of the Transputer Manual, whereby on page 5, the Patent Owner argues that "none of the Transputer references, from May'948 to the Transputer Manuals, disclose a stack pointer associated with registers A, B and C, which the office action has identified as the 'first push down stack.'". Further, the Patent Owner argues that because of the internal connection of the A, B, and C register stack, the A, B, C register stack would not need a stack pointer.

18. However, the examiner notes that currently claim 1 requires "...said internal data bus being bidirectionally connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register,..." With this, there is no requirement that the "stack pointer" be associated with the push down stack, as argued by the Patent Owner, only that an internal data bus is "bidirectionally connected to a stack pointer". If the Patent Owner desires that feature that the stack pointer expressly points to the first push down stack to be considered in interpreting the current claim language, then the claim must be amended accordingly.

19. Further, the examiner notes that MPEP 2111, as noted above, requires that "During patent examination, the pending claims must be 'given their broadest reasonable interpretation consistent with the specification.'" With this, in reviewing the reference of May '948, as stated in col. 35, lines 12-32, May '948 states "The instruction pointer (IPTR) of any process in the list is stored in the IPTR location 65 of its workspace as shown in FIG. 3." Continuing, in viewing

Fig. 2, May '948 illustrates the IPTR 50 is shown as being bidirectionally connected to the stack registers A, B, and C. With this, the instruction pointer IPTR of May '948 can be seen as pointing to the stack of the A, B, and C registers. This is also described in May '948 on col. 27, lines 36-42.

20. Continuing, on page 6, the Patent Owner argues that the IPTR 65 "contains the address of an instruction, not the address of the top of a data stack." With this the examiner notes that nowhere does the current claim language expressly require that the stack pointer includes "the address of the top of a data stack". If the Patent Owner wishes that this feature be considered in interpreting the current claim language, then the claim must be amended accordingly.
With this, the May '948 reference discloses the IPTR S 65 as a pointer to a register stack, therein being considered as a "stack pointer", whereby in col. 9, lines 59-68 "Location 65 is used when a process is not the current process to fold a pointer (IPTR) to the next instruction to be executed by the process when it becomes the current process".

21. Therefore, the rejection of claims 1-4, as cited in the Office action dated 11/5/2009, under 35 U.S.C. 103(a) as being unpatentable over May '948, expressly incorporating Edwards ''698 Patent, further in view of the Transputer Manual, is maintained and repeated in this Office action.

STATEMENT OF REASONS FOR PATENTABILITY AND/OR CONFIRMATION

The following is an examiner's statement of reasons for patentability and/or confirmation of the claims found patentable in this reexamination proceeding:

Claims 9 and 10 are confirmed as patentable.

Regarding dependent ***claim 9***, the examiner does believe that the prior art of record expressly discloses the invention as claimed, particularly including the feature requiring the first push down stack has a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit. The prior art of Hull, Jr. teaches of stack elements, as seen in Fig. 2. However, Hull, Jr. fails to expressly teach of a third stack element configured as a RAM external to the single integrated circuit. Further, the reference of Muller (U.S. Patent 4,969,091), noted in the Request for Reexamination, teaches of implementing a push down stack. But, Muller fails to expressly teach the architecture that is required by the claim language, which requires a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit. Thus,

the prior art of record is not seen to expressly disclose this architecture. Therefore, in the examiner's opinion, the claim is deemed patentable.

Any comments considered necessary by PATENT OWNER regarding the above statement must be submitted promptly to avoid processing delays. Such submission by the patent owner should be labeled: "Comments on Statement of Reasons for Patentability and/or Confirmation" and will be placed in the reexamination file.

Conclusion

22. The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent No. 5,530,890 throughout the course of this reexamination proceeding.

23. **THIS ACTION IS MADE FINAL.**

A shortened statutory period for response to this action is set to expire TWO MONTHS from the mailing date of this action.

Extensions of time under 37 CFR 1.136(a) do not apply in reexamination proceedings. The provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Further, in 35 U.S.C. 305 and in 37 CFR 1.550(a), it is required that reexamination proceedings "will be conducted with special dispatch within the Office."

Extensions of time in reexamination proceedings are provided for in 37 CFR 1.550(c). A request for extension of time must be filed on or before the day on which a response to this action is due, and it must be accompanied by the petition fee set forth in 37 CFR 1.17(g). The mere filing of a request will not effect any extension of time. An extension of time will be granted only for sufficient cause, and for a reasonable time specified.

The filing of a timely first response to this final rejection will be construed as including a request to extend the shortened statutory period for an additional month, which will be granted even if previous extensions have been granted. In no event however, will the statutory period for response expire later than SIX MONTHS from the mailing date of the final action. See MPEP § 2265.

24. ALL correspondence relating to this ex parte reexamination proceeding should be directed as follows:

Please mail any communications to:

Attn: Mail Stop "Ex Parte Reexam"
Central Reexamination Unit
Commissioner for Patents
P. O. Box 1450
Alexandria VA 22313-1450

Please FAX any communications to:

(571) 273-9900
Central Reexamination Unit

Please hand-deliver any communications to:

Customer Service Window
Attn: Central Reexamination Unit
Randolph Building, Lobby Level
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

Signed:

Joseph R. Pokrzywa
Primary Examiner
Central Reexamination Unit 3992
(571) 272-7410

Conferees: /r.g.f./
ESK