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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. CV08-00877 PSG **DEFENDANTS' REPLY SUPPLEMENTAL CLAIM CONSTRUCTION BRIEF** Date: November 30, 2012 Judge: Hon. Paul S. Grewal

HTC CORPORATION and HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED, Defendants.	Case No. CV08-00882 PSG
BARCO, N.V., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED, Defendants.	Case No. CV08-05398 PSG

Table of Contents

Table of Authorities

Cases

Table of Abbreviations

'148 patent	U.S. Patent No. 6,598,148, entitled "High Performance Microprocessor Having Variable Speed System Clock," issued July 22, 2003 (attached to the Otteson Decl. as Exhibit CC)
'336 patent	U.S. Patent No. 5,809,336, entitled "High Performance Microprocessor Having Variable Speed System Clock," issued September 15, 1998 (attached to the Otteson Decl. as Exhibit DD)
'584 patent	U.S. Patent No. 5,784,584, entitled "High Performance Microprocessor Using Instructions that Operate Within Instruction Groups," issued July 21, 1998
'749 patent	U.S. Patent No. 5,440,749, entitled "High Performance, Low Cost Microprocessor Architecture," issued August 8, 1995 (attached to the Otteson Decl. as Exhibit BB)
'890 patent	U.S. Patent No. 5,530,890, entitled "High Performance, Low Cost Microprocessor," issued June 25, 1996 (attached to the Otteson Decl. as Exhibit AA)
Alliacense	Defendant Alliacense Limited; "TPL" is also used throughout this brief to refer to all three declaratory judgment defendants
Boufarah	U.S. Patent No. 5,127,091, entitled "System for Reducing Delay in Instruction Execution by Executing Branch Instructions in Separate Processor While Dispatching Subsequent Instructions to Primary Processor," issued June 30, 1992
Breit Decl.	Declaration of Michelle G. Breit in Support of Defendants' Reply Supplemental Claim Construction Brief
Chen Decl.	Declaration of Kyle D. Chen in Support of Plaintiffs' Consolidated [Supplemental] Opening Claim Construction Brief
Def. Op'n Brief	Defendants' Opening Supplemental Claim Construction Brief
Opp.	Plaintiffs' Consolidated Opening Supplemental Claim Construction Brief
Otteson Decl.	Declaration of James C. Otteson in Support of Defendants' Opening Claim Construction Brief for the "Top Ten" Terms
Patriot	Defendant Patriot Scientific Corporation; "TPL" is also used throughout this brief to refer to all three declaratory judgment defendants
Sheets	U.S. Patent No. 4,670,837, entitled "Electrical System Having Variable-Frequency Clock," issued June 2, 1987
Talbot	U.S. Patent No. 4,689,581, entitled "Integrated Circuit Phase Locked Loop Timing Apparatus," issued August 25, 1987
TPL	Defendant Technology Properties Limited; also collectively declaratory judgment defendants Technology Properties Limited, Patriot Scientific Corporation and Alliacense Limited

Introduction

Declaratory judgment defendants TPL, Patriot and Alliacense (collectively "TPL" or "Defendants") jointly submit this reply memorandum in support of Defendants' Opening Supplemental Claim Construction Brief. Judge Ware, in issuing his First Claim Construction Order on June 12, 2012, asked the parties to address two narrow issues: (1) whether or not the voltage-controlled oscillator disclosed in Talbot is or is not a ring oscillator; and (2) the meaning of a statement by the examiner in the '749 patent prosecution history related to operands. TPL thoroughly addressed these issues in its opening brief, demonstrating that (1) the Schmitt Trigger oscillator in Talbot is not a ring oscillator and (2) the '749 patent as issued includes no limitation regarding operands; instead, the examiner's comment relates to claims that issued in a divisional patent, U.S. Patent No. 5,784,584 (the "'584 patent").

Plaintiffs, in their opening brief, veer far from Judge Ware's request and devote much of their efforts to arguing that the term "ring oscillator" should be construed to exclude all voltage control oscillators by importing into the construction a limitation of "non-controllability." As set forth in detail below, Plaintiffs' argument is based on a **single word** appearing in an interview summary provided by an examiner and not adopted by the patentees. The purported disavowal has none of the indicia of an unambiguous and unmistakable disavowal by a patentee that could or should be used to drastically limit the scope of numerous patent claims. And, it is not supported by the specification or any intrinsic evidence.

Plaintiffs also rehash their arguments, rejected by Judge Ware, in an attempt gain importation of an additional limitation into the term "instruction register" that would require that operands (which are not in the claims at issue) contained within the instruction register to be "right-justified." As TPL demonstrated in its opening brief and explains further below, the examiner's reference to operands in the '749 patent prosecution history relates to claims that ultimately were filed and issued in the '584 patent. No basis exists to import that unclaimed limitation into claim 1 of the '749 patent and doing so would violate fundament rules of patent law.

Argument

I. JUDGE WARE'S INITIAL CONSTRUCTION OF "RING OSCILLATOR" IS CORRECT

A. Plaintiffs' Efforts to Limit the Claimed "Ring Oscillator" to "Non-Controllable" Are Not Supported by the Specification or Prosecution History.

Although Judge Ware requested that the parties provide supplemental briefing on the issue of "whether the voltage-controlled oscillator disclosed in Talbot is or is not a ring oscillator," Plaintiffs spend most of their brief arguing that TPL disavowed all voltage controlled oscillators due to the examiner's inclusion of the single word "non-controllable" in his interview summary in the prosecution history of the '148 patent. Plaintiffs argue that this single word in the prosecution history – provided by the examiner and not adopted by the patentee – and which appears nowhere in the claims, specification or file history save for the examiners' interview summary, should be used to drastically limit the term "ring oscillator" and thereby drastically limit the scope of claims in the '148, '336, '749 and '890 patents (parties agree that "ring counter" of '749 should be construed as "ring oscillator").

Plaintiffs' position is contrary to governing law requiring a disclaimer to be unmistakable and unambiguous. Moreover, plaintiffs' arguments rely on unabashed mischaracterizations of the prosecution file histories and specifications and cannot withstand scrutiny.

1. In accordance with controlling law, a disavowal must be "clear and unmistakable" and must be made by the patentee.

As Judge Ware observed in his claim construction Order in this case, before a submission made by a patentee during reexamination can be regarded as a disavowal, the court must find "the allegedly disavowing statement is 'so clear as to show reasonable clarity and deliberateness, and so unmistakable as to show unambiguous evidence of disclaimer.'" Order at 16, quoting *Omega Eng'g, Inc. v. Raytek Corp*., 334 F.3d 1314, 1325 (Fed. Cir. 2003) (citations omitted). Stated another way, the "disavowal" doctrine only applies where a disavowal is "clear and unmistakable." *See Cordis Corp. v. Medtronic AVE, Inc*., 511 F.3d 1157, 1177 (Fed Cir. 2008) ("alleged disavowing actions or statements made during prosecution [must] be both clear and unmistakable").

Second – and very important here – the alleged disavowal must be made by the ***patentee***, not the ***examiner***. *Salazar v. Procter & Gamble Co.*, 414 F.3d 1342, 1347 (Fed. Cir. 2005) ("unilateral statements by an examiner do not give rise to a clear disavowal of claim scope by an applicant," as "the applicant has disavowed nothing"); *Univ. of Pittsburgh of Commonwealth Sys. of Higher Educ. v. Hedrick*, 573 F.3d 1290, 1296-97 (Fed. Cir. 2009) ("a wide chasm exists between the weak inference from the [interview] summary . . . and a clear and unmistakable disavowal as required to limit a claim term"). As the Federal Circuit has recognized, "[p]rosecution history ... cannot be used to limit the scope of a claim unless the **applicant** took a position before the PTO." *3M Innovative Props. Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1373 (Fed. Cir. 2003) (emphasis added). The reason for requiring the disclaimer to come from the **applicant** rather than the **examiner** is the recognition that sometimes the examiner and applicant are talking past one another. See *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc*., 381 F.3d 1111, 1124 (Fed. Cir. 2004) (where an "examiner and applicant [are] talking past one another" and "the record finally reflects the examiner's acquiescence to the claim language chosen by the applicant, [t]his is not clear evidence of the patentee's disavowal of claim scope").

As set forth in detail below, the purported "disavowal" upon which plaintiffs seek to drastically limit the scope of claims that include a ring oscillator is not unambiguous, not unmistakable and was not adopted by the patentee.

2. Plaintiffs mischaracterize the '336 specification.

Plaintiffs incorrectly assert that the '336 specification "describes the ring oscillator frequency as non-controllable by virtue of being variable with environmental parameters." [Opp. 3:2-3] Of course, the specification makes no such disclosure. Plaintiffs point to two statements in the specification (at col 16:47:48 and col. 16:59-17:2), neither of which mentions "controllability." Instead, these statements merely refer to the fact that the invention overcomes issues in the prior art wherein the clock frequencies were fixed to worse case conditions and were not designed to vary. Clearly, these statements in the specification do not amount to the disavowal of all voltage controlled oscillators as plaintiffs assert, particularly because, by their nature, voltage control oscillators do not have a fixed frequency.

3. Plaintiffs mischaracterize the statements in the original prosecution history of the '336 patent.

Plaintiffs ask the Court to conclude that the patentees made clear in the original prosecution of the '336 patent that the claimed ring oscillator was "non-controllable" and thereby disavowed all voltage controlled oscillators. Plaintiffs, again, point to statements that, at best, fail to support their assertion, and in fact, point to the opposite conclusion. Indeed, in the statements plaintiffs cite, the patentees repeatedly point out only that the invention does not **necessitate** external circuitry to control the clock frequency; nowhere do the patentees indicate that such circuitry is prohibited in practicing the invention. Thus, in the first statement quoted by plaintiffs, the patentees told the examiner:

> the oscillator or variable speed clock varies in frequency ***but does not require*** manual or programmed inputs or external or extra components to do so.

'336 PH Amendment at 5, 0707/97 (Chen Decl., Ex. 4) (emphasis added). Similarly, in distinguishing the '336 patent invention from U.S. Patent No. 4,670,837 ("Sheets"), the patentees pointed out that by placing the clock and the CPU on the same integrated circuit, the '336 patent invention:

> ***obviates the need*** for provision of the type of frequency control information described by Sheets.

'336 PH Amendment at 8, 04/15/96 (Chen Decl., Ex. 5) (emphasis added). Later, again in distinguishing Sheets, the patentees of the '336 patent invention pointed out that:

> In Sheets, a command input is required to change the clock speed [but in] the present invention … ***[n]o command input is necessary*** to change the clock frequency.

'336 PH Amendment at 4, 01/13/97 (Chen Decl., Ex. 6) (emphasis added).

The '336 prosecution history demonstrates that the patentees distinguished their invention from the prior art by pointing out that, unlike the prior art, the oscillator or variable speed clock in their invention varies in frequency (*i.e.*, is not fixed, for example, like an external crystal) and **does not require** external frequency control. Plaintiffs' unsupported effort to expand this distinction beyond its clear meaning to impose a **prohibition** of any form of control should be rejected as unsupported and without merit.

4. Plaintiffs mischaracterize the '148 patent reexamination history related to Talbot.

Plaintiffs baldly assert that TPL "emphasized" during reexamination of the '148 patent "the non-controllability of the claimed clock circuit." [Opp. 3:27-28.] Nothing could be further from the truth. Instead, a review of the prosecution history reveals that the only reference to "non-controllability" is inclusion of the single word "non-controllable" in a summary of an interview ***prepared by the examiner***. '148 PH Interview Summary at 4 of 5, 2/12/08 (Chen Decl., Ex. 2).

Continuation of Description of the general nature of what was agreed to if an agreement was reached, or any other comments:

Discussed differences in the prior art and the claimed invention. Particularly, the patent owner argued that the references failed to teach of the limitation requiring "said memory further occupying a majority of the total area of said single substrate". The patent owner further pointed out that the reference of May, noted above, describes that the memory can be the largest and densest component on the chip, but this is different than being the "majority of the total area",

Continuing, the patent owner further argued that the reference of Talbot does not teach of a "ring oscillator". The patent owner discussed features of a ring oscillator, such as being non-controllable, and being variable based on the environment. The patent owner argued that these features distinguish over what Talbot teaches. The examiner will reconsider the current rejection based on a forthcoming response, which will include arguments similar to what was discussed.

Joseph R. Pokrzywa
Primary Examiner
Central Reexamination Unit 3992

In the short, three-sentence summary of the discussion of Talbot, the examiner provided no explanation regarding the meaning of the word. Moreover, rather than relying on "non-controllability," the examiner specifically stated he would "reconsider the current rejection [premised on Talbot] based on a forthcoming response" from the patent owner.

Within 8 days of the interview (dated February 21, 2008, though filed February 26, 2008) TPL submitted the promised written response. '148 PH Remarks/Arguments, 2/21/88 (Chen Decl., Ex. 3). This written response explained that Talbot was distinguishable because "Talbot does not teach, disclose, or suggest the ring oscillator recited in claim 4." *Id.* at 11. Nowhere – and in no way – did TPL adopt the examiner's reference to "non-controllability." TPL, in fact, made no reference to that word at all.

Importantly, TPL acknowledged that "Talbot discusses a voltage-controlled oscillator (VCO)." *Id.* After that acknowledgment, TPL did not point to that feature as distinguishing Talbot from the claimed invention. Instead, TPL wrote: "but, [Talbot] does not teach or disclose a

ring oscillator." *Id*. TPL, in other words, did not exclude or disclaim voltage controlled oscillators, as plaintiffs assert; TPL, instead, pointed out that voltage controlled oscillators *which do not employ a ring oscillator*, such as in Talbot, do not satisfy the claimed "ring oscillator" limitation of the invention.

Of further importance, in an action dated June 25, 2008, the examiner expressly accepted the arguments contained in the written response, never mentioning the interview. Specifically, the examiner stated "Patent Owner's arguments, filed 2/26/08 with respect to the rejections [based on Talbot] have been fully considered and are persuasive. Therefore, the rejection … has been withdrawn." '148 PH Re-exam, Detailed Action, at 5 (Declaration of Michelle G. Breit in Support of Defendants' Reply Supplemental Claim Construction Brief ("Breit Decl."), Exh. A. Thus, the examiner expressly relied on the patent owner's written arguments to overcome Talbot, and *not* the interview.

The law regarding disavowal is settled: Allegedly disavowing statements must be both "so clear as to show reasonable clarity and deliberateness, and so unmistakable as to show unambiguous evidence of disclaimer" for the Court to use the statement to limit the meaning of claim terms. *Omega Eng'g, Inc.*, 334 F.3d at 1325. Here, the alleged disavowing statement – "non-controllable" – remains unexplained in the file history and not adopted by the patentee. The term itself is ambiguous, and would require further construction. For example, the patent discloses that the ring oscillator frequency will vary with changes in voltage. '336 patent, 17:21-22 That disclosure indicates, therefore, that the voltage provided to the ring oscillator is not fixed and can be changed or even controlled, rendering the meaning of "non-controllable" ambiguous. Where the meaning of purported disavowal is not apparent, there can be no "clear and unambiguous" disclaimer.

As TPL set forth in its opening brief, Talbot does not disclose a ring oscillator. The patentees distinguished Talbot on that basis and the examiner then withdrew his rejection. While the claimed inventions exclude the voltage controlled oscillator disclosed in Talbot *because it does not include a ring oscillator*, nothing in the prosecution histories of '148 and '336 patents or the '336 patent specification support plaintiffs' argument that TPL disavowed all voltage controlled

oscillators. Plaintiffs' request to include the limitation of "non-controllable" in the construction of the term "ring oscillator," therefore, should be rejected.

B. Talbot Does Not Disclose a Ring Oscillator.

In their opening brief, Defendants provided a detailed explanation as to why the oscillator disclosed in Talbot is not a ring oscillator. A ring oscillator requires an odd number and at least three inverters to oscillate. The Talbot oscillator under discussion here may oscillate with only one inversion stage. In particular, Fig. 3 of Talbot discloses an oscillator that may oscillate with only one inversion stage due to the presence of a Schmitt trigger.

Although Judge Ware's preliminary claim construction of "ring oscillator" in the First Claim Construction Order adopted the term "inverter" instead of TPL's proposed term "inversion," no evidence was presented to or cited by the Court to support a distinction between the words. At deposition, both experts indicated that there could be "inversions" that are not "inverters."

If the court finds that the current proposed construction needs further clarification then Defendants would propose: "interconnected electronic components comprising multiple odd numbers of inversions arranged in a loop, where three or more inversions are required to maintain an oscillating output."

II. JUDGE WARE'S CONSTRUCTION OF "INSTRUCTION REGISTER" IS CORRECT

A. Plaintiffs' Attempt to Limit the Term "Instruction Register" to Include Unclaimed Right-Justified Operands Violates Fundamental Rules of Claim Construction.

Plaintiffs' theory appears to be there is a single "invention" disclosed in the specification of '749 patent, which specification is shared by all divisional patents that issued from the original patent application. The theory assumes that, to the extent any claim drawn from the shared specification claims an instruction register, the claim must be read also to include not only operands but operands that are right justified only.

In fact, the '749 patent specification discloses at least 10 different inventions, as demonstrated by the 10-way restriction requirement imposed by the examiner (which is discussed

in TPL's related motion for reconsideration). The '749 patent is primarily directed to multiple-instruction fetch. The '584 patent, which shares the same specification, is directed in part to instructions that employ variable-width-operands. Based on Judge Ward's claim construction, Plaintiffs improperly attempt to read into the independent claims of the '749 patent – which do not mention operands – the limitations related to instruction groups in the claims of the '584 patent. The subject of Judge Ward's claim construction concerning "instruction groups," however, was the '584 patent. See Judge Ward Memorandum Opinion and Order, at 22-24 (Otteson Decl., Exh. 3). The '584 patent, however, claims an entirely different invention that does not include the inventive features claimed in '749 patent, but instead is directed to an invention that include right-justified operands. The term "instruction register" has a well understood ordinary meaning, as Judge Ware observed. There is no basis for limiting instruction register to hold operands or even variable-width operands; nor is there a basis in the '749 patent claims to import a limitation requiring right-justified operands, particularly when the claimed invention does not relate to decoding operands, let alone variable-width operands.

1. The independent claims of the '749 Patent do not require operands.

Plaintiffs argue that the specification discloses that some instructions may employ variable-width operands, and that the means for decoding these instructions requires the operands to be right-justified in the instruction register. Even assuming the specification contains that disclosure, the independent claims of the '749 patent do not require any operands. As Defendants point out in their opening brief, issued claim 1 (filed claim 3), which was discussed in the examiner's interview under consideration here, requires fixed-width instructions due to its limitation regarding bus width. That bus width limitation was present when the discussion with the examiner occurred.

Moreover, issued claim 7 (filed claim 11), which depends from issued claim 1, further limits claim 1 by adding variable-width-operands and additional structure required to decode the instructions that utilize them. Plaintiffs' flatly ignore the doctrine of claim differentiation by seeking to read into claim 1 the narrowing limitations added in claim 7.

In addition, the prosecution history related to the *independent* claims of '749 include no discussion regarding operands. The only possible exception would be the entries related to the examiner interview; but, when one considers that issued claim 7 (filed claim 11) was also rejected over Boufarah, it becomes clear that aspect of the interview was directed at features of the *dependent* claim, as set forth in Defendants' opening brief. (Def. Op'n. Brf. at 6:5-17.) While the subsequent written amendment indicates that this subject matter was considered for incorporation into the independent claim, the applicant stated that invention would be filed as a separate divisional application – which it was seven months later. Ultimately, that application matured into the '584 patent which is directed in part to instructions that use variable-width-operands.

The record provides no grounds for concluding that the applicants ever argued that issued independent claim 1 should be construed to incorporate operands, let alone variable-width operands requiring right justification.

2. The '749 Patent Discloses Embodiments Where Operands Are Not Right Justified.

Plaintiffs devote significant effort describing embodiments in the shared patent specification that include right-justified operands. The inclusion of such embodiments, however, is not in dispute. The real issue, instead, is whether the limitations and subject matter from the '584 patent (including utilizing variable width operands) should be read into the instruction register claimed in the '749 patent claims. Fatal to plaintiffs' argument is the presence of other embodiments in the specification in which operands are present but not right-justified. For example, in one embodiment, the instruction register fetches four fixed width 8-bit instructions in a single memory cycle. See '749 Patent, 7:50-58. The specification discloses two of these fixed-width instructions with operands that are not right-justified: "Read-Local-Variable XXXX" and "Write-Local-Variable XXXX." See '749 Patent, 31:45-32:15. These fixed width instructions include a 4bit opcode and a 4bit operand represented by XXXX, which is a binary number from 0000-1111 which indicates the address of one of the 16 locations on the Return Stack. *Id.* Because these two instructions can be in any of the four 8-bit slots in the instruction register, the same is true of their fixed-width XXXX operand – meaning the operand is not right justified in the

instruction register. For example, the figure below shows how any combination of four of these instructions would contain operands that are not right justified in the 32bit instruction register as disclosed in the specifications.

1st location	2nd location	3rd location	4th location
4bit opcode & 4bit operand	4bit opcode & 4bit operand	4bit opcode & 4bit operand	4bit opcode & 4bit operand

Because the specification discloses instructions that employ various operand locations, the term "instruction register" cannot be construed to limit the location of operands to any particular operand location such as right-justified, as plaintiffs assert.

Instructions that utilize variable width operands are a separate and distinct novelty from the invention of multiple sequential instructions ('749 Patent, claim 1) which are supplied to the instruction register as claimed. They were separately claimed in a divisional application that emerged into the '584 patent. For the reasons specified here and in defendants opening supplemental claim construction brief it would be improper to adopt plaintiffs proposed claim construction which improperly imports limitations from the specifications and ignores the rules of claim differentiation.

Conclusion

For the foregoing reasons and those forth in TPL's opening brief, the Court should adopt Judge Ware's findings in his First Claim Construction and reject Plaintiffs' effort to import extraneous limitations in the patent claims.

Dated: November 9, 2012

Respectfully submitted,

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case Nos. CV08-00877 PSG **DECLARATION OF MICHELLE G. BREIT IN SUPPORT OF DEFENDANTS' REPLY SUPPLEMENTAL CLAIM CONSTRUCTION BRIEF** Date: November 30, 2012 Judge: Hon. Paul S. Grewal

HTC CORPORATION and HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED, Defendants.	Case No. CV08-00882 PSG
BARCO, N.V., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION and ALLIACENSE LIMITED, Defendants.	Case No. CV08-05398 PSG

I, Michelle G. Breit, hereby declare:

1. I am an attorney with the law firm of Agility IP Law, LLP ("Agility") which represents Technology Properties Limited and Alliacense Limited. I make this declaration of my own personal knowledge, and if called to do so, I could and would competently testify thereto.

2. I submit this Declaration in support of Defendants' Reply Supplemental Claim Construction Brief.

3. Attached hereto as Exhibit A is a true and correct copy of an excerpt of the '148 Prosecution History Re-exam: Detailed Action, June 25, 2008.

I declare under penalty of perjury that the foregoing is true and correct to the best of my knowledge and recollection.

Executed this 9th day of November 2012, at Scottsdale, Arizona.

/s/ Michelle G. Breit
Michelle G. Breit

EXHIBIT A

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/008,227	09/21/2006	6598148	0081-011D3C1X1	6167

40972 7590 06/25/2008

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EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 06/25/2008

Please find below and/or attached an Office communication concerning this application or proceeding.

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EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/008,227*.

PATENT NO. *6598148*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Office Action in Ex Parte Reexamination	Control No. 90/008,227	Patent Under Reexamination 6598148	
	Examiner JOSEPH R. POKRZYWA	Art Unit 3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

a☒ Responsive to the communication(s) filed on *26 February 2008* . b☐ This action is made FINAL.
c☐ A statement under 37 CFR 1.530 has not been received from the patent owner.

A shortened statutory period for response to this action is set to expire 2 month(s) from the mailing date of this letter. Failure to respond within the period for response will result in termination of the proceeding and issuance of an *ex parte* reexamination certificate in accordance with this action. 37 CFR 1.550(d). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).** If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☒ Information Disclosure Statement, PTO/SB/08.
3. ☐ Interview Summary, PTO-474.
4. ☐ _____.

Part II SUMMARY OF ACTION

1a. ☒ Claims *4,7,8,10 and 14-25* are subject to reexamination.
1b. ☒ Claims *1-3,5,6,9 and 11-13* are not subject to reexamination.
2. ☐ Claims _____ have been canceled in the present reexamination proceeding.
3. ☐ Claims _____ are patentable and/or confirmed.
4. ☒ Claims *4,7,8,10 and 14-25* are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ The drawings, filed on _____ are acceptable.
7. ☐ The proposed drawing correction, filed on _____ has been (7a)☐ approved (7b)☐ disapproved.
8. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
   a)☐ All b)☐ Some* c)☐ None of the certified copies have
   1☐ been received.
   2☐ not been received.
   3☐ been filed in Application No. _____ .
   4☐ been filed in reexamination Control No. _____.
   5☐ been received by the International Bureau in PCT application No. _____.
   * See the attached detailed Office action for a list of the certified copies not received.
9. ☐ Since the proceeding appears to be in condition for issuance of an *ex parte* reexamination certificate except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte* Quayle, 1935 C.D. 11, 453 O.G. 213.
10. ☐ Other: _____

cc: Requester (if third party requester)

DETAILED ACTION

Response to Amendment

1. **Claims 4, 7, 8, and 10** of U.S. Patent Number 6,598,148 (hereafter "the '148 Patent") were requested to be reexamined, and were each rejected in an Office action dated 12/21/07. Continuing, in the response dated 2/26/08, the Patent Owner argues that the references utilized in the above noted rejection do not particularly teach the claimed invention, and further adds new **claims 14-25**. Thus, currently, **claims 4, 7, 8, 10, and 14-25** are the subject of this reexamination.

Information Disclosure Statement

2. First, it is noted that the numerous Court documents submitted on 5/27/08 are acknowledged by the examiner. However, the citations of the various Court papers and documents, as listed in the Information Disclosure Statement dated 5/27/08, within the "Other Prior Art – Non Patent Literature Documents" section, have been indicated as having a line through their citations. The indicated Court documents are not considered as "Prior Art" documents, since the Court documents are each dated in the years 2007 and 2008, which is after the publication date of the '148 Patent being Jul. 22, 2003, and is not prior to the effective filing date of the '148 Patent of Aug. 3, 1989. Thus, the citations of these Court documents should not be listed in the Information Disclosure Statement.

3. Similarly, the numerous Patent Office papers of related reexamination proceedings are also listed in the Information Disclosure Statement dated 5/27/08, whereby these documents are also not considered as "Prior Art", as the dates are after the publication date of the '148 Patent being Jul. 22, 2003, and not before the effective filing date of the '148 Patent. Thus, the citations of these documents should not be listed in the Information Disclosure Statement, and have been indicated as having a line through their citations.

4. Further, the Information Disclosure Statement dated 5/27/08 includes documents that have no clear date (such as Citation Nos. CY, CZ, DC, and DF), and also documents (such as Citation No. EK-EO, being reports regarding U.S. Pat. 5,440,749) that have dates that are later than the publication dated of the '148 Patent, being July 22, 2003, and being after the effective filing date of the '148 Patent. Thus, these documents cannot be considered as prior art, since a date cannot be established so as to be considered as "prior art".

5. With this, there are numerous other references listed in the Information Disclosure Statement submitted on 5/27/08, which have been considered by the examiner (see attached PTO/SB/08).

6. However, the examiner notes that MPEP 2256, under the heading "Prior Art Patents and Printed Publications Reviewed by Examiner in Reexamination" states, in part:

> Where patents, publications, and other such items of information are submitted by a party (patent owner or requester) in compliance with the requirements of the rules, **the requisite degree of consideration to be given to such information will be normally limited by the degree to which the party filing the information citation has explained**

> **the content and relevance of the information**. The initials of the examiner placed adjacent to the citations on the form PTO/SB/08A and 08B or its equivalent, without an indication to the contrary in the record, do not signify that the information has been considered by the examiner any further than to the extent noted above. [emphasis added]

Further, MPEP 609.05(b) states:

> The information contained in information disclosure statements which comply with both the content requirements of 37 CFR 1.98 and the requirements, based on the time of filing the statement, of 37 CFR 1.97 will be considered by the examiner. Consideration by the examiner of the information submitted in an IDS means that **the examiner will consider the documents in the same manner as other documents in Office search files are considered by the examiner while conducting a search of the prior art in a proper field of search**. The initials of the examiner placed adjacent to the citations on the ** PTO/SB/08A and 08B or its equivalent mean that the information has been considered by the examiner to the extent noted above. [emphasis added]

With this, the examiner notes that with the large number of references submitted in the above noted PTO/SB/08A, the references were considered to at least the "degree to which the party filing the information citation has explained the content and relevance of the information", and in "the same manner as other documents in Office search files are considered by the examiner while conducting a search of the prior art in a proper field of search".

Response to Arguments

7. Patent Owner's arguments, filed 2/26/08, with respect to the rejection(s) of **claim(s) 4, 7, 8, and 10** under 35 U.S.C.103(a) as being unpatentable over U.S. Patent Number 4,689,581, issued to Talbot, Gerald R. (referred to as "Talbot'581") in view of European Patent Publication EP 0 113 516, issued to May, Michael D., being European Patent Application No. 83307078.2 (referred to as "May'516"), have been fully considered and are persuasive. Therefore, the rejection, as cited in the previous Office action, has been withdrawn.

8. Particularly, the references of Talbot'581 and May'516 do not particularly show that "said memory further occupying a majority of a total area of said single substrate". Patent Owner's arguments on pages 8 through 12 discuss how these references teach that the disclosed memory may be the largest component on the substrate, but this may not be a majority of the total area of the substrate. Further, the reference of Talbot'518 describes an oscillator circuit, but the specific features are unclear if the components actually make a ring oscillator.

9. However, upon further consideration, a new ground(s) of rejection is made in view of Kajigaya *et al.* (U.S. Patent Number 4,956,811), with a full discussion appearing below.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

11. **Claims 15-25** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

12. With respect to each of the newly added dependent claims, upon review of the specification of the '148 Patent, the examiner cannot find a description or indication that the oscillator/clock 316 seen in Fig. 9 is actually a ring oscillator. Further, the examiner cannot find a specific description of the memory having a specific area being just larger than twice, three times, or four times as large as the processing unit and the ring oscillator combined. Additionally, there is no description that the total area is actually just "the sum of active areas" of the substrate, nor is there a description that the total area is an area provided by an entire top surface of the single substrate.

13. Particularly, as seen in Figs. 7 and 8 of the '148 Patent, the die includes a crystal oscillator clock 282, which is noted as the Motorola 50 MegaHertz crystal oscillator clock. However, this would not be the same as a ring oscillator on the same substrate as that seen in

Fig. 9. Further, the specification of the '148 Patent describes the ring oscillator in col. 14, lines 37-60, and further states that "The clock is fabricated on the same silicon chip as the rest of the microprocessor 50." However, in Fig. 9, "clock/timing 316" is shown. The examiner cannot find in the specification of the '148 Patent where the circuit of clock/timing 316 shown in Fig. 9 is described. The specification does describe the CPU 316, in col. 10, lines 54-59, being the same component number as that of clock/timing 316, but the CPU s shown as item 314. However, the ALU, the Instruction Decode and the Clock/Timing are each seen as item 316. Is the clock 316, the ALU 316, and the instruction decode 316 each the same component?

14. But the '148 Patent specification describes a microprocessor 310, whereby in col. 6, lines 49-65, the '148 Patent states that "Fig. 9 shows another microprocessor 310 that is provided integrally with 1 megabit of DRAM 311 in a single integrated circuit 312...The microprocessor 310 is equivalent to the microprocessor 50 in Figs. 1-8." Continuing, the examiner notes that in Fig. 9, there is no microprocessor 310 labeled, as the processors of the ALU 316 and the DMA CPU 314 shown and described in col. 10, lines 43-67. With these sections, it appears that the entire drawing of Fig. 9 is referred to as microprocessor 310, which can thus replace that of microprocessor 50 seen within the layout diagram of Fig. 7, which is described as including a "clock is fabricated on the same silicon chip as the rest of the microprocessor 50".

15. However, as further described in col. 8, lines 62-67, the '148 Patent states "There are certain differences between the microprocessor 310 and the microprocessor 50 that arise from providing the microprocessor 310 on the same die 312 with the DRAM 311. Integrating the

DRAM 311 allows architectural changes in the microprocessor 310 logic to take advantage of existing on-chip DRAM 311 circuitry." Thus, while the microprocessor 310 and 50 may be equivalent, there are differences because of the "architectural changes in the microprocessor 310".

16. As discussed on pages 12 and 13 of the arguments, the Patent Owner relies on Fig. 9 as supporting each of the newly added claims. However, the examiner notes that the added claims include a range that the memory occupies an area greater than two times, greater than three times, or greater than four times the area occupied by the processing unit and the ring oscillator. First, the drawing in Fig. 9 does not teach these ranges. Referring to Fig. 9, there is no clear teaching of the area that the processing unit and the ring oscillator actually occupies. Further, there is no clear teaching of the memory occupying each of the possible ranges. For instance, there is no teaching that the memory occupies an area just over two times the area of a processing unit and oscillator combined. Continuing, there is no clear teaching that the total area only consists of active areas on the substrate. There is no discussion of active areas or inactive areas, and what would be considered an "active area". Additionally, there is no clear teaching that the total area refers to an entire top surface of the substrate.

17. Thus, the newly added claims 15-25 contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim Rejections - 35 USC § 102

18. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

19. **Claims 4, 7, 8, 10, and 14-25** are rejected under 35 U.S.C. 102(e) as being anticipated by Kajigaya *et al.* (U.S. Patent Number 4,956,811, hereafter "Kajigaya").

Regarding independent ***claim 4***, Kajigaya teaches of a microprocessor integrated circuit [see col. 3, lines 44-60, wherein "Circuit elements constituting each block shown in Fig. 32 and each of the circuit elements shown in Figs. 1-30 are, although not necessarily limitative, formed on a single semiconductor substrate such as a single crystal silicon by a known semiconductor integrated circuit manufacturing technique."] comprising:

a processing unit disposed upon an integrated circuit substrate [PC2, which includes for instance, "redundant address control circuit RAC", as read on col. 15, lines 10-23, and seen in Figs. 32 and 33; also see Figs. 23 and 24, being "circuit diagrams showing one example of a redundant address control circuit of a dynamic type RAM to which the present invention is applied", as noted in col. 3, lines 10-13],

said processing unit operating in accordance with a predefined sequence of program instructions [see col. 4, lines 18-44, whereby when the DRAM is adapted for the x 1 bit pattern, the operating modes are programmed as "a first page mode, static column mode, nybble mode, and serial mode", and when the DRAM is adapted for the x 4 bit pattern, the operating modes are programmed as "first page mode, static column mode and serial mode, and mask write mode"; also see col. 15, lines 24-51];

a memory coupled to said processing unit and capable of storing information provided by said processing unit [memory arrays MARY0-MARY3, also see Figs. 32 and 33],

said memory occupying a larger area of said integrated circuit substrate than said processing unit said memory further occupying a majority of a total area of said single substrate [see Fig. 33, whereby memory arrays MARY0-MARY3 occupy the majority of the total area of the substrate]; and

a ring oscillator having a variable output frequency [see col. 12, lines 55-58, wherein "Each of the substrate back bias voltage generating circuits includes a ring oscillator having five CMOS inverter circuits..."; also see Fig. 6, whereby the timing generating circuit TG includes a plurality of odd number of inverters, being the defining feature of a ring oscillator],

wherein the ring oscillator provides a system clock to the processing unit [see Fig. 6, being the timing generating circuit TG],

the ring oscillator disposed on said integrated circuit substrate [see col. 12, lines 55-58, wherein "Each of the substrate back bias voltage generating circuits includes a ring oscillator having five CMOS inverter circuits…", also see col. 15, lines 10-23, wherein "At one end of the semiconductor substrate SUB, ...a peripheral circuit PC1 which includes the timing generating circuit TG…is disposed between the pads TF to A9 and the memory arrays MARY0 to MARY3."].

Regarding ***claim 7***, Kajigaya discloses the microprocessor integrated circuit discussed above in claim 4, and further teaches that said memory is capable of supporting read and write operations [see col. 4, line 45-col. 5, line 10; also see col. 15, lines 24-51].

Regarding independent ***claim 8***, Kajigaya teaches of a microprocessor integrated circuit [see col. 3, lines 44-60, wherein "Circuit elements constituting each block shown in Fig. 32 and each of the circuit elements shown in Figs. 1-30 are, although not necessarily limitative, formed on a single semiconductor substrate such as a single crystal silicon by a known semiconductor integrated circuit manufacturing technique."] comprising:

a processing unit having one or more interface ports for interprocessor communication [for instance PC2, which a "redundant address control circuit RAC", as read on col. 15, lines 10-23, and seen in Figs. 32 and 33; also see Figs. 23 and 24, being "circuit diagrams showing one example of a redundant address control circuit of a dynamic type RAM to which the present

invention is applied", as noted in col. 3, lines 10-13, whereby the RAC includes various ports for interprocessor communication],

said processing unit disposed upon an integrated circuit substrate [see Figs. 32 and 33, whereby the PC2, which includes a "redundant address control circuit RAC" is disposed on the single substrate with the DRAM],

a memory disposed upon said substrate and coupled to said processing unit [memory arrays MARY0-MARY3, also see Figs. 32 and 33],

said memory occupying a greater area of said substrate than said processing unit, said memory further comprising a majority of a total area of said substrate [see Fig. 33, whereby memory arrays MARY0-MARY3 occupy the majority of the total area of the substrate]; and

a ring oscillator having a variable output frequency [see col. 12, lines 55-58, wherein "Each of the substrate back bias voltage generating circuits includes a ring oscillator having five CMOS inverter circuits..."; also see Fig. 6, whereby the timing generating circuit TG includes a plurality of odd number of inverters, being the defining feature of a ring oscillator],

wherein the ring oscillator provides a system clock to the processing unit [see Fig. 6, being the timing generating circuit TG],

the ring oscillator disposed on said substrate [see col. 12, lines 55-58, wherein "Each of the substrate back bias voltage generating circuits includes a ring oscillator having five CMOS inverter circuits...", also see col. 15, lines 10-23, wherein "At one end of the semiconductor substrate SUB, ...a peripheral circuit PC1 which includes the timing generating circuit TG...is disposed between the pads TF to A9 and the memory arrays MARY0 to MARY3."].

Regarding ***claim 10***, Kajigaya discloses the microprocessor integrated circuit discussed above in claim 8, and further teaches of including memory controller means coupled to said memory for performing direct memory access data transfer through said one or more interface ports [see col. 4, line 45-col. 5, line 10; also see col. 9, line 47-col. 10, line 18; also see col. 15, lines 24-51].

Regarding ***claims 14 and 20***, Kajigaya discloses the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and further teaches that the memory comprises a plurality of physically separate memory portions [see Figs. 32 and 33, being memory arrays MARY0, MARY1, MARY2, and MARY3].

Regarding ***claims 15 and 21***, Kajigaya discloses the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and further teaches that the memory occupies an area greater than twice as large as an area occupied by the processing unit and the ring oscillator combined [see Figs. 32 and 33].

Regarding ***claims 16 and 22***, Kajigaya discloses the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and further teaches that the memory occupies an area greater than three times as large as an area occupied by the processing unit and the ring oscillator combined [see Figs. 32 and 33].

Regarding ***claims 17 and 23***, Kajigaya discloses the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and further teaches that the memory occupies an area approximately four times as large as an area occupied by the processing unit and the ring oscillator combined [see Figs. 32 and 33].

Regarding ***claims 18 and 24***, Kajigaya discloses the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and further teaches that the total area consists of a sum of active areas of the single substrate comprising circuit elements of the integrated circuit [see Figs. 32 and 33, also see col. 14, lines 52-65, wherein "the dynamic type RAM is, although not necessarily limitative, formed on a semiconductor substrate SUB which is defined by one single crystal silicon."].

Regarding ***claims 19 and 25***, Kajigaya discloses the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and further teaches that the total area is an area provided by an entire top surface of the single substrate [see Fig. 33, also see col. 14, lines 52-65, wherein "the dynamic type RAM is, although not necessarily limitative, formed on a semiconductor substrate SUB which is defined by one single crystal silicon."].

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. **Claims 4, 7, 8, and 14-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over "A 5V Self-Adaptive Microcomputer with 16Kb of E2 Program Storage and Security", written by Mark Bagula et al., 1983 IEEE International Solid-State Circuits Conference, pages 34-35 (hereafter "Bagula") in view of Hashimoto *et al.* (U.S. Patent Number 4,882,710, hereafter "Hashimoto").

Regarding independent ***claim 4***, Bagula teaches of a microprocessor integrated circuit [see Figs. 1-4] comprising:

a processing unit disposed upon an integrated circuit substrate [see Fig. 4, "ALU and Temp Reg."],

said processing unit operating in accordance with a predefined sequence of program instructions [see page 34, col. 1, wherein "This architecture was chosen as the basis for this circuit because its microcoded instruction set and generalized building block type layout greatly facilitated the instruction set change and control circuit modifications necessary to implement EEROM memory"];

a memory coupled to said processing unit and capable of storing information provided by said processing unit [being the Microcode ROM , RAM and EEPROM Arrays, which comprise 48% of the die area],

said memory occupying a larger area of said integrated circuit substrate than said processing unit said memory further occupying a majority of a total area of said single substrate [see Figure 4; also see Table 1, wherein the memory arrays, which comprise 48% of the die area utilization, with 21.9% being "Interconnect unused area and scribe"; Thus, 48% of the active areas on the substrate comprises a majority of a total area of active areas on the single substrate. This interpretation is reasonable, especially in light of the newly added dependent claim 18, which states "wherein the total area consists of a sum of **active areas of the single substrate**"]; and

an oscillator having a variable output frequency [see "Clock Generator" in Figure 4, as well as "OSC" in Fig. 1],

wherein *the oscillator* provides a system clock to the processing unit [see Figs. 1-4 on page 35],

the oscillator disposed on said integrated circuit substrate [see "Clock Generator" in Fig. 4].

However, Bagula does not expressly disclose if the oscillator is a ring oscillator. But Bagula does state that the chip used in the design of the substrate was "developed under license from Texas Instruments" [see page 34, bottom of col. 1].

Hashimoto, having the assignee of Texas Instruments, describes a microprocessor integrated circuit comprising:

a processing unit [1A, 1B, and 4],

a memory coupled to said processing unit and capable of storing information provided by said processing unit [being the dynamic memory arrays seen in Fig. 1A]; and

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit [see Fig. 1A, and col. 2, lines 26-42].

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to utilize a ring oscillator, as described by Hashimoto, as the clock generator, described and shown by Bagula. Bagula & Hashimoto are combinable because they are from the same field of endeavor, being systems developed under the same license, having memory arrays, processing unit, and clock generators. The suggestion/motivation for doing so would have been that ring oscillators were known at the time and commonly used as system clocks, as shown by Hashimoto. Therefore, it would have been obvious to combine the teachings of Hashimoto with the system of Bagula to obtain the invention as specified in claim 4.

Regarding ***claim 7***, Bagula and Hashimoto disclose the microprocessor integrated circuit discussed above in claim 4, and Bagula further teaches that said memory is capable of supporting read and write operations [see page 34, col. 2, "Signature Read" and "Block write/clear"].

Regarding independent ***claim 8***, Bagula teaches of a microprocessor integrated circuit [see Figs. 1-4] comprising:

a processing unit having one or more interface ports for interprocessor communication [see Figs. 1 and 4 on page 35, being "ALU and Temp Reg."], said processing unit being disposed on a single substrate [see Fig. 4],

a memory disposed upon said substrate and coupled to said processing unit [being the Microcode ROM , RAM and EEPROM Arrays, which comprise 48% of the die area],

said memory occupying a greater area of said substrate than said processing unit, said memory further comprising a majority of a total area of said substrate [see Figure 4; also see Table 1, wherein the memory arrays, which comprise 48% of the die area utilization, with 21.9% being "Interconnect unused area and scribe"; Thus, 48% of the active areas on the substrate comprises a majority of a total area of active areas on the single substrate. This interpretation is reasonable, especially in light of the newly added dependent claim 18, which states "wherein the total area consists of a sum of **active areas of the single substrate**"]; and

an oscillator having a variable output frequency [see "Clock Generator" in Figure 4, as well as "OSC" in Fig. 1],

wherein *the oscillator* provides a system clock to the processing unit [see Figs. 1-4 on page 35],

the oscillator disposed on said integrated circuit substrate [see "Clock Generator" in Fig. 4].

However, Bagula does not expressly disclose if the oscillator is a ring oscillator. But Bagula does state that the chip used in the design of the substrate was "developed under license from Texas Instruments" [see page 34, bottom of col. 1].

Hashimoto, having the assignee of Texas Instruments, describes a microprocessor integrated circuit comprising:

a processing unit [1A, 1B, and 4],

a memory coupled to said processing unit [being the dynamic memory arrays seen in Fig. 1A]; and

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit [see Fig. 1A, and col. 2, lines 26-42].

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to utilize a ring oscillator, as described by Hashimoto, as the clock generator, described and shown by Bagula. Bagula & Hashimoto are combinable because they are from the same field of endeavor, being systems developed under the same license, having memory arrays, processing unit, and clock generators. The suggestion/motivation for doing so would have been that ring oscillators were known at the time and commonly used as system clocks, as shown by Hashimoto. Therefore, it would have been obvious to combine the teachings of Hashimoto with the system of Bagula to obtain the invention as specified in claim 8.

Regarding ***claims 14 and 20***, Bagula and Hashimoto disclose the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and Bagula further teaches

that the memory comprises a plurality of physically separate memory portions [see Fig. 4, being the EEROM, the RAM, and the ROM].

Regarding ***claims 15 and 21***, Bagula and Hashimoto disclose the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and Bagula further teaches that the memory occupies an area greater than twice as large as an area occupied by the processing unit and the ring oscillator combined [see Fig. 4; also see Table 1].

Regarding ***claims 16 and 22***, Bagula and Hashimoto disclose the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and Bagula further teaches that the memory occupies an area greater than three times as large as an area occupied by the processing unit and the ring oscillator combined [see Fig. 4; also see Table 1].

Regarding ***claims 17 and 23***, Bagula and Hashimoto disclose the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and Bagula further teaches that the memory occupies an area approximately four times as large as an area occupied by the processing unit and the ring oscillator combined [see Fig. 4; also see Table 1].

Regarding ***claims 18 and 24***, Bagula and Hashimoto disclose the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and Bagula further teaches that the total area consists of a sum of active areas of the single substrate comprising circuit elements of the integrated circuit [see Fig. 4; also see Table 1].

Regarding ***claims 19 and 25***, Bagula and Hashimoto disclose the microprocessor integrated circuits discussed above in claims 4 and 8, respectively, and Bagula further teaches that the total area is an area provided by an entire top surface of the single substrate [see Fig. 4; also see Table 1].

Additional Pertinent Prior Art

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Aoki *et al.* (U.S. Patent Number 4,701,884) discloses a semiconductor memory integrated circuit disposed on a single semiconductor substrate, as read in the abstract and seen in Fig. 28;

Conclusion

23. Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that *ex parte* reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extensions of time in *ex parte* reexamination proceedings are provided for in 37 CFR 1.550(c).

24. In order to ensure full consideration of any amendments, affidavits or declarations, or other documents as evidence of patentability, such documents must be submitted in response to this Office action. Submissions after the next Office action, which is intended to be a final action, will be governed by the requirements of 37 CFR 1.116, after final rejection and 37 CFR 41.33 after appeal, which will be strictly enforced.

25. The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent No. 6,598,148 throughout the course of this reexamination proceeding.

NOTICE RE PATENT OWNER'S CORRESPONDENCE ADDRESS

Effective May 16, 2007, 37 CFR 1.33(c) has been revised to provide that:

The patent owner's correspondence address for all communications in an *ex parte* reexamination or an *inter partes* reexamination is designated as the correspondence address of the patent.

> *Revisions and Technical Corrections Affecting Requirements for Ex Parte and Inter Partes Reexamination*, 72 FR 18892 (April 16, 2007)(Final Rule)

The correspondence address for any pending reexamination proceeding not having the same correspondence address as that of the patent is, by way of this revision to 37 CFR 1.33(c), automatically changed to that of the patent file as of the effective date.

This change is effective for any reexamination proceeding which is pending before the Office as of May 16, 2007, including the present reexamination proceeding, and to any reexamination proceeding which is filed after that date.

Parties are to take this change into account when filing papers, and direct communications accordingly.

In the event the patent owner's correspondence address listed in the papers (record) for the present proceeding is different from the correspondence address of the patent, it is strongly encouraged that the patent owner affirmatively file a Notification of Change of Correspondence Address in the reexamination proceeding and/or the patent (depending on which address patent owner desires), to conform the address of the proceeding with that of the patent and to clarify the record as to which address should be used for correspondence.

Telephone Numbers for reexamination inquiries:

Reexamination and Amendment Practice	(571) 272-7703
Central Reexam Unit (CRU)	(571) 272-7705
Reexamination Facsimile Transmission No.	(571) 273-9900

26. ALL correspondence relating to this ex parte reexamination proceeding should be directed as follows:

Please mail any communications to:

Attn: Mail Stop "Ex Parte Reexam"
Central Reexamination Unit
Commissioner for Patents
P. O. Box 1450
Alexandria VA 22313-1450

Please FAX any communications to:

(571) 273-9900
Central Reexamination Unit

Please hand-deliver any communications to:

Customer Service Window
Attn: Central Reexamination Unit
Randolph Building, Lobby Level
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

Signed:

Joseph R. Pokrzywa
Primary Examiner
Central Reexamination Unit 3992
(571) 272-7410

Conferees:

ROLAND G. FOSTER
PRIMARY EXAMINER

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