EXHIBIT I
To Omnibus Declaration of Irvin E. Tyan ISO Defendants' Opposition to Acer and HTC's Motions for Summary Judgment

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA, SAN JOSE DIVISION

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ACER, INC., ACER AMERICA)
CORPORATION and GATEWAY, INC.,)
Plaintiffs,)
vs.) No. 3:08-cv-00877 PSG
TECHNOLOGY PROPERTIES)
LIMITED, PATRIOT SCIENTIFIC)
CORPORATION, and ALLIACENSE)
LIMITED,)
Defendants.)
_______________________________)

HIGHLY CONFIDENTIAL

SUBJECT TO THE PROTECTIVE ORDER

VIDEOTAPED DEPOSITION OF ANDREW WOLFE, PH.D.,

VOLUME 3

Friday, July 19, 2013

Palo Alto, California

Reported by:

Hanna Kim, CLR, CSR No. 13083

Friday, July 19, 2013

9:07 a.m. - 5:43 p.m.

Videotaped deposition of ANDREW WOLFE, PH.D., taken on behalf of Defendants, Technology Properties Limited, et al., on Friday, July 19, 2013, beginning at 9:07 a.m. and ending at 5:43 p.m., at the law offices of K&L Gates at 630 Hansen Way, Palo Alto, California, California, before Hanna Kim, CLR, CSR No. 13083.

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INDEX OF EXAMINATION

WITNESS: ANDREW WOLFE, PH.D.

A. I don't recall any in the report.

MR. MARSH: Okay. We've been going for a while.

Why don't we take a little break?

THE VIDEOGRAPHER: We are off the record at 10:50 a.m.

(Short recess taken.)

THE VIDEOGRAPHER: We are back on the record at 11:05 a.m.

BY MR. MARSH:

Q. Dr. Wolfe, beginning on Page 45 of your report, there's a Section 11, anticipation of the asserted claims.

Do you see that?

A. Yes.

Q. And I'm referring to Section 11 of Exhibit 4. This is the section in which you express opinions that the Asserted Patents are anticipated by various prior art references, correct?

A. In general, I -- I express and summarize the opinions, but this section refers to, I believe, Exhibits B through F, where many of the details are.

Q. Exhibits B through F are the exhibits to Exhibit 4 of your opening report, right?

A. Yes.

Q. Now, Paragraphs 75 through 87 of Exhibit 4, those pertain to the '749 Patent no longer in this case, right?
A. In general, there are some discussions -- some general statements about the TITMS 3410 microprocessor that I think are probably duplicated in other places with respect to the '890 Patent, but -- but the opinions may overlap.
Q. Okay. Understood.
But those paragraphs, Paragraphs 75 through 87 of Exhibit 4, those are directed to the '749 Patent, aren't they?
A. That was their intent, yes.
Q. And then beginning on Paragraph 49 of Exhibit 4 in Section 11.2, you offer some anticipation patents with -- or anticipation opinions with respect to the '336 Patent, right?
A. Yes, again referring to certain exhibits. I believe, Exhibits C, D, and E are the relevant ones.
Q. And those are Exhibits C, D, and E to our deposition Exhibit 4, right?
A. Yes.
Q. You say here in Paragraph 90 of your expert report that there is inherent variation in all oscillators due to, "The real world inability to

produce a perfect fixed frequency oscillator," right?
A. Well, you left out some words I said. Well, what it actually says is, TPL alleges that the inherent de minimus variation in a fixed frequency oscillator, due to the real world inability to produce a perfect fixed frequency oscillator, is sufficient to meet certain claim requirements.
Q. But you would agree that -- that it is a fact that there's a real world inability to produce a perfect fixed frequency oscillator?
A. Yes. You cannot produce a perfect fixed frequency oscillator. There will always be some de minimus, you know -- if you measure anything carefully enough in this world, you will see that it's not perfect.
Q. So there's some inherent variation in any oscillator, is what you're saying, although you characterize it as de minimus, right?
A. Yes. In many cases, it's negligible or de minimus, but there is always, if you examine it closely enough from a scientific perspective, some de minimus variation.
An engineer would not necessarily -- in fact, generally an engineer would not concern themselves with that variation, and an engineer would ordinarily treat

something as fixed frequency, which is what I've called it, a fixed frequency oscillator. But if you were not to treat it as an engineer, but you were to measure it with perfect precision, you would always find that there's some inherent variation.

Q. Well, let me ask you this: What are some of the causes of this real world inability to produce a perfect fixed frequency oscillator that you refer to in Paragraph 90 of Exhibit 4?

A. Again, you have to look at it whether you're looking at it from a practical perspective or a theoretical perspective. From a practical perspective, you can't make a perfect measurement, so you can't even figure out whether or not anything is ever perfect.

From a more theoretical perspective, it would have to do with the fact that atoms are always moving, there's thermal noise in every electrical system that's going to cause some very small random variation.

In a particular system, there may be other things that -- that impact it. References, ground references, may change. There can be random signals that are induced by adjacent signals, radio waves, electromagnetic interference. Again, practical terms, those tend to be dominated by measurement errors, the fact that you can't even measure or respond to a signal with perfect precision.

Q. So one of the things that you mentioned that causes this real world inability to produce a perfect fixed frequency oscillator was thermal noise, right?

A. Yes.

Q. And what is thermal noise?

A. It's the fact that -- and again, I'm not a physicist, so I may not be able to give you a perfect formal answer.

But in practical engineering terms, it's the fact that, at any temperature above absolute zero, molecules are always in motion; and therefore, they interact in random and unpredictable ways, which are tiny, tiny effects and can generally be ignored in electric circuits, but sometimes can be measurable.

Q. So thermal noise, those are thermal changes or thermal fluctuations, right?

A. No. No. No. It's electrical noise caused by the fact that there is heat energy in the circuit.

Q. But you mentioned that thermal noise corresponds to the movement of the molecules, correct?

A. Yes, but it's not tied -- thermal noise is not tied to changes to temperature, merely the fact that something has a temperature above absolute zero.

Q. You also mentioned induced random signals.

Strike that.
You mentioned changes in ground references. What does that mean?
A. Whenever you look at what a circuit does, it's always a complete circuit. It's a path from a voltage source around a complete path again. And in -- in most real circuits, when you measure a voltage, you have to measure it with respect to something. And other circuits will interact with respect to a reference, and those references are never perfect. So they will have minor variations, tiny variations. Sometimes, depending on what the circuit is, sometimes large variations. And they -- the ones that we're most concerned about are the random variations caused by other circuits switching, that cause various kinds of random spikes that -- that can cause random noise in any kind of signal, including an oscillator.
Q. And so the change in ground references, that would change the effect of voltage on the device, correct?
A. It would change -- it depends what device you're talking about. If a particular circuit has a change in ground voltage, specific -- depends on the circuit, because things can be regulated. But in particular, if those changes are very rapid and random

so that they can't be compensated for, they can change the effective voltage of various signals, supply voltage or control voltages.

Q. What about the induced random signals that you mentioned or EM interference? Can those also change the effect of voltage in the circuits that receive those?

A. Well, there's always multiple effect of voltages in any interesting circuit, so -- but yes. It can change it in tiny, negligible ways, or, depending on what the circuit is, it can change it in huge ways, but again, generally random ways.

Q. Do fabrication imprecisions affect the real world inability to produce a perfect fixed frequency oscillator?

A. I'm not quite sure what you mean. If you mean that that -- again, nothing in the real world's perfect. So if you mean that, when you manufacture two chips, they're a little bit different, that doesn't have any impact on the fact that neither of them is perfect. If they were the same, they still wouldn't be perfect.

Q. But it means that the two chips would be imperfect in different ways, right?

A. Well, it's random, so it would probably be different. But as with anything that's random, it could be the same.

Q. You mention here, at the bottom of Paragraph 90, transistors that are on the same silicon die.

What's a silicon die?

A. It's a piece of silicon wafer. So when we manufacture chips in the normal way, they're manufactured on wafers. A wafer is generally round, anywhere between 100 and 300, now maybe 400 millimeters, in diameter, and it will have a whole bunch of circuits on it. And then as part of the manufacturing process, those circuits will be cut into pieces, and that piece is called a die and it consists of a number of layers that form electronic circuit elements, like transistors, wires, resistors, capacitors that can be used to perform a function.

Q. And so silicon die is what we might typically refer to as an integrated circuit, right?

A. We might. It's really part of an integrated circuit. When we play with an integrated circuit, we're typically talking about die inside of a package or mounted in some super structure. But it's the primary functional part of an integrated circuit.

Q. Would it be fair to call it the silicon substrate of the integrated circuit?

A. Substrate's usually part of the die. It's the majority of the die, and then you build things on top of the substrate to form the die.

Q. I see. So the die -- the silicon substrate, plus the circuitry on top of the substrate, right?

A. Yes.

Q. And would you agree that -- you describe the process of creating silicon die out of wafers.

Would you agree that the transistors on each silicon die are exposed to similar fabrication steps?

A. No. In general, not necessarily, especially when you use a word like "exposed."

It's often that you want to have very different kinds of transistors on the same die. So by using masks, you'll have some steps used to build some transistors and other steps that are used to build other transistors. The whole die went in the machine, but some steps were blocked from parts of a chip and allowed to build other parts of the chip; and conversely, other steps build the remaining part of the chip.

So even in terms of the way layers are built, it's not unusual to have two, three, four or more kinds of transistors on a modern die, modern being anywhere in the last 20 years. And then, of course, a transistor's characteristics are impacted by much more than just its layers. It's also impacted by its size and shape, and those routinely differ from transistor to transistor.

Q. So I guess my questions may be a little simpler. The wafer that you described, that's processed -- all the dies on the wafer are processed at the same time, right?

A. Well, they go through a sequence of steps. Today, there may be 100 of them grouped into maybe 40 or 50 processes, and -- and everything goes into every machine. But then selective masking is used to figure out which transistors are exposed to which manufacturing processes.

Q. Yeah. Understood.

So what you're saying is that at certain points certain parts of each die may be masked off and not subject to certain processes.

But in general, the whole wafer is processed together, right?

A. Well, it goes in the machine, but the whole wafer is not processed. The intent of masking it off is to prevent part of the wafer from being processed in that step.

Q. All right. I guess how are you using the word "process" in that answer? Maybe we're using the word differently.

A. That there is some chemical or mechanical change to the materials on the -- on the wafer.

Q. Okay. Let me use a different word then.

The wafer -- all the dies on the wafer are manufactured together, correct?

A. Well, it depends when. So at the early stages when a wafer's still intact, they all go through the same machines together, and then there are the masks that determine which portions of the wafer are actually exposed to a manufacturing step and which portions of the wafer skip that manufacturing step.

Q. And so when you say that the wafers all go through the machine together, they're all part of the same fabrication, aren't they?

A. I'm not sure how that's a different question. They -- you take the wafer, you put a mask on it to select which parts of the wafer are going to be impacted by the machine and which parts are going to be protected from the impact of the machine. Then you put it in the machine. The exposed parts are impacted by the manufacturing step, and the covered parts are not impacted or minimally impacted.

Q. Well, would you agree that transistors on each

die undergo similar process variations?
A. Sometimes they do. Sometimes they don't. As I said, there may be four, five, six different kinds of transistors on a die, and some of them will be similar. Some of them will be different.
Q. You would agree with me, if we look at the transistors on each die, that, as that die is heated up, they undergo similar temperature changes, right?
A. It depends how it's heated up. In operation, that's generally not true. In operation, they are often local temperature gradients. Also -- let me hear your question again. I want to make sure I understood one of the words.
Q. Yeah. My question was you would agree with me that, if you look at the transistors on each die, as the die is heated up, those transistors undergo similar temperature changes, right?
A. That depends. So if the die is heated uniformly and if the transistors are the same size, then that would be true. If the transistors are different sizes, they have different thermal mass, and they will respond differently to changes in temperature, and in almost all real circumstances, especially with operating parts, the die is not heated uniformly.

Q. So if, for example, I took -- I took a product that had a silicon die to Death Valley on a record setting heat day, the transistors on that chip would all be heated up by the environmental conditions, correct?

A. Yes, but possibly not to the same degree and possibly not proportionally.

Q. But they would all be heated up nonetheless, correct?

A. Well, it depends where you started. But if you go from a colder place to a warmer place, in general all the transistors will get warmer, but not necessarily by the same amount or in the same proportion. And of course, even if they become warmer, it won't necessarily have the same effect on them.

Q. And when those transistors are powered up, when the die is powered up, the die receives power from a single power source, correct?

A. Well, it depends what chip, but very few chips receive power from a single power source anymore.

Q. What do you mean by that?

A. Most complicated chips have multiple power sources, which are then further divided inside the chip so the individual circuits on the chip then experience even more local power conditions.

But a typical interesting chip today, something like a cell phone processor, could have as many as four or five different, completely different, power sources; and it's very common for chips that have both analog functions and digital functions to have completely separate power sources for the analog and digital functions.

Q. But ultimately, the power source for all of the transistors on that chip in the cell phone is the battery of the cell phone, right?

A. In some abstract way, but not in a practical engineering way, because those circuits are isolated from the characteristics of that battery.

That battery is used as the source of energy, but it then goes through power circuitry that generates independent voltages, independent currents that are independently filtered, independently regulated, so that the characteristics of the power seen by the circuits, or that impacts by the circuits, is independently determined by lots of different circuits or what we call power supplies.

Yeah. It depends on where you want to trace it back as to where the source of that energy was. I mean, yes, it could be the battery or it could be a wall that you plugged the battery into or it could be those variations, right?

A. With precision instruments, yes, you could measure them. But from any kind of a practical perspective, it -- I mean, when a company like Acer sells a product, they don't test it to that level of precision. Like a PC, they don't test speed of a PC to that level of precision. They don't measure it to that level of precision. There could be two sitting on a shelf that differ by that much, and neither a company nor a supplier nor a customer would ever care.

Q. So you mentioned that you could measure 1 or 2 kilohertz with precision instruments. But isn't it true that an AM radio is able to measure kilohertz?

A. Not at 300 megahertz. All right? So there's a difference. You can measure things proportionally, right? I mean, I can measure a cup of water, but I can't measure Lake Superior to within a precision of one cup of water.

So from an engineering perspective, tolerances have to be related to the magnitude of the measurement as a whole.

Q. But it is true, isn't it, that an AM radio is capable of detecting differences in frequency that's on the order of kilohertz, right?

A. Of AM frequencies, but not of -- it can't

de -- detect the difference between a 300 megahertz frequency and 300.001 megahertz frequency.
Q. And that's just because that's not what it's designed to do, right?
A. That's right.
Q. But detecting differences on the order of a kilohertz is certainly doable and possible?
A. Depends in what. You can certainly detect the difference between one kilohertz and two kilohertz signals by ear, but that's different than detecting a difference between a 300.001 megahertz signal and a 300.002 megahertz signal, just like I could look at the difference between half a cup of water and a cup of water and I can tell the difference, but I could not look at two lakes and tell whether or not they differed by half a cup of water.
Q. So in your opinion, what would constitute a de minimus variation with respect to the claims of the '336 Patent?
A. Well, in Paragraph 90 I'm talking about what has been documented by TPL as being de minimus.
In the general sense of my report, I focussed more on what is insignificant or insubstantial, and those would be things that are within the tolerances so that they don't have any substantial impact on the way

the circuits are designed, the way they're used, the way they're sold.

Q. So what would be the smallest variation that you would consider de minimus in connection with microprocessor circuits and the '336 Patent?

A. I don't tend to consider what the smallest is, but certainly anything that's within the tolerance of an oscillator, that's within its expected unpredictability, is insignificant or insubstantial.

Q. Do the claims of the '336 Patent indicate that they require some -- more than some minimum or de minimus amount of variation to be infringed?

A. Yes. By using the words in their ordinary way, they require that -- the ordinary meaning of varying is substantially variant. Every claim term has to be treated in perspective of ordinary skill in the art.

When we say in a claim that something's flat, there is some physicist with some instrument that can measure anything in the real world and prove to you that it's not flat; and yet we still use the words flat and/or planar in claims, and we understand that means that it's substantially flat for the purpose that it's intended, because that's the ordinary meaning. And these claims, all the terms that have been construed

have ordinary meanings.
Q. So could you take a look at Exhibit 2, the '336 Patent?
A. Mm-hmm.
Q. Let's look at the claims in the re-examination certificate, and if you could point me to where the claims require more than the de minimus variation, I'd like to see the language that requires that.
A. I have it in my report.
Can I refer to Exhibit 5?
Q. Absolutely. Yes.
A. So there are a number of things there. One is there are a number of terms in the claims -- and I'll go through them in a second as I finish my answer -- that indicate that a clock or an oscillator needs to vary. And the ordinary meaning of vary or variable speed is in this patent or outside this patent, to a practitioner, to a person of ordinary skill, would be that it varies in a significant or substantial way.
Q. And I'm sorry? You're referring to Exhibit 5, your rebuttal report? Where are you looking in that report?
A. I'm starting with Section 8.12 on Page 44, although there may be other sections that discuss this as well.

I also note when I read the claims that the term "variable speed system clock" is differentiated from "fixed frequency clock" in Claim 2 and throughout the patent. And, for example, in Column 17, there are two different things in -- in the patent and in ordinary usage in the field, fixed speed clock and a variable speed clock.

So my understanding, ordinary meaning, of all the claims is that there is something that has an ordinary meaning that requires it to vary more than insubstantially. And in Claims 6, 7, and 9, that's the phrase that says, "Varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation."

Q. So let's take a look at that language that you just read in Claim 6. I understand --

A. Yeah. I'm not finished with the answer. But if you want to move on, I'm happy to do that.

Q. Yeah. I understand that you have claim language here in Paragraph 80 of Exhibit 5 that you're saying requires more than a de minimus variation, right?

A. Yes, based on the ordinary meaning of those terms.

Q. And does that claim language anywhere expressly say that a certain amount of variation is required? Is there any claim language that actually says that?

A. That's the ordinary meaning of varying.

Q. So you're referring to the word "varying."

But it doesn't say varying by how much, does it?

A. No, but it needs to be substantial. All right? It needs to be -- in order to not read that word out of the claim, it has to be different than something that is invariant. And since, from a scientific, mathematical perspective, no invariant things exist in this world, I'm making the assumption that I would ordinarily make, that this is talking about the way that a person of ordinary skill would use the term "vary." And a person of ordinary skill would use the term "varying" differently than they would use the term "fixed." And if something is substantially fixed, they would call it fixed; and if it varies in a substantial way, they would call it varied.

Q. So you used the word "substantial."

What do you mean by that?

A. Something substantial in that it affects the way that the system is designed or built or used in a -- in a meaningful way. I mean, it's somewhat of a judgment call for a practitioner, but it's a judgment call that they -- that they do everyday.

When somebody -- somebody designs something to have a one-inch screw, they know that they can't get a perfect one-inch screw, but they still have a range of things that they can substantially treat as being a one-inch screw. They would probably know that a screw that changes from day to day from a quarter of an inch to three inches is not a fixed length screw. These are things that people of ordinary skill deal with in a consistent way all the time, and I applied them in that consistent way.

Q. So I asked you before about de minimus, and you couldn't tell me how much was necessary to not be a de minimus variation.

Now I want to ask you about substantial.

What would the minimum amount of variation be that would be substantial in your view?

MR. WALKER: I'm going to object to the

question to the extent it mischaracterizes the earlier testimony.

BY MR. MARSH:

Q. Let's strike that question.

Let me ask you this: What would the minimum amount of variation be that you would consider substantial in your opinion, with respect to the claims of the '336 Patent?

A. I didn't have to make that determination to -- to do -- to render my opinions. Clearly, things that were within the tolerance, within the uncertainty of the signal, that were documented as being within the range of possible random noise, that were expressly within the degree of unreliability of the part, are insubstantial in a microprocessor design. Clearly, the 100 percent variations that are described in the patent as the amount of variation one would typically see using the preferred embodiment are substantial.

I didn't have any situations where I had to evaluate anything in between.

Q. In your opinion, are the claims in the '336 Patent limited to situations in which the variation is 100 percent like the example that you mentioned?

A. No. I think they're limited to places where the variation is intentional and substantial.

Q. You mentioned, in connection with your opinions in Paragraph 90 of Exhibit 4, de minimus variation.

What is the -- what is the smallest variation that you would consider not to be de minimus in connection with the claims of the 336 patents?

A. I hadn't really formed an opinion on that. What I said was that the variation that was identified by TPL was de minimus.

Q. So you express that opinion without really deciding what is and is not de minimus then?

A. Well, I decided what is de minimus. I didn't set an explicit bound on when it stops being de minimus. We could look up the definition of de minimus, but generally de minimus is small enough that it has no practical impact. And that would have been the standard I would have applied.

Q. And how did you decide that with respect to what we say are TPL's allegations?

A. Well, we can go through the allegations, but the only thing that TPL identified, if I recall, was they identified for most of the products the simple fact that all products have thermal noise. And in these kinds of products, that would have been tiny and insignificant. There -- there were no quantitative measurements, but because the products operate, any thermal noise clearly has no impact.

And then for the two products that were based on two of the LSI chips and described in Exhibits Acer A-1 and Acer A-2, they describe the clock jitter as the source of variation. And we do have quantitative information on that. We also have testimony on that, and it's clearly de minimus on the fact that it has no impact on operation of that circuit. And if it were not there, it wouldn't make a difference. And as long as it's within the uncertainty tolerance of the clock speed, it gets disregarded by engineers and users.

Q. So you mentioned two things there that you consider de minimus, thermal noise and jitter, right?

A. In these particular products as it was identified by TPL.

Q. Okay. Is there anything else that was identified by TPL that you consider to be a de minimus variation?

A. I looked at everything identified by TPL. Those are things that I remember actually TPL actually identifying for the specific accused Acer products.

Q. Well, let's go back to Exhibit 4 on Page 51, and I want to look at your opinion about the Motorola single chip microcomputer data book that you express in

Paragraphs 92 and 93 of Exhibit 4.
Do you see that?
A. Yes.
Q. You know what? I'm sorry. Before we discuss that reference, I wanted to ask you a different question.
Turning back to Page 41 of Exhibit 4. You're aware that the varying limitations that you referred to, including the language that you quoted from Claim 6, that those have an agreed upon construction, right, shown here on Page 41 of Exhibit 4?
A. Yes.
Q. And that agreed upon construction of the varying terms, is that -- is, "increasing and decreasing proportionally," right?
A. Yes.
Q. And there's no language in that agreed upon construction about substantial variation or some level that's not de minimus of variation, is there?
A. Well, there's two things. One is I think we do need to match these up. I don't -- you cut me off on the previous answer, but I don't think this is all the terms that are identified in that Paragraph 80.
Also, it does bring up the other interesting point, that all the things that I described were random

and would not happen proportionally between two different things. So they don't meet that definition for that reason as well, as the ordinary meaning.

But again, when the construction is increasing and decreasing, I assume that the Court intends us to use those in the way that a person of ordinary skill or an ordinary juror would use those terms. There's no way that a person of ordinary skill or a juror would look at this table and say, it's increasing in height right now.

I'm sure there is some instrument that we could use to measure the height of this table that would show that it is currently increasing or decreasing; and yet, from a real world perspective, it's fixed. And that's the distinction that I'm making, is that the tiny amount that this table is increasing and decreasing as I sit here and look at it is irrelevant to any claim construction. It's irrelevant to any real world understanding of the height of the table. And I used a similar common sense standard in understanding these claim constructions.

Q. But you would agree that there's no language of quantity in this adopted claimed construction for those varying terms, right?

A. There is the ordinary meaning of increasing and decreasing, which --

Q. Okay. But the words "de minimus" don't appear in the construction, do they?

A. No. It's my understanding that any time that a word is used in a claim, it's intended to be used in an ordinary way where an insignificant or insubstantial amount is not relevant.

Q. Fair enough.

The word "substantial" or "insubstantial" also doesn't appear in the joint construction here, does it?

A. Not explicitly.

Q. Okay. So let's turn back now to Page 41, and let's talk about the Motorola single chip microcomputer data book reference. You express an opinion about this reference in Paragraphs 92 and 93, and then you have a claim chart in Exhibit C to Exhibit 4, your opening report, right?

A. Yes.

Q. And it's your opinion that that document, which I'm going to refer to as the Motorola reference, okay -- it's your opinion that that Motorola reference anticipates the claims of the '336 Patent, correct?

A. As those claims have been applied by TPL in its infringement allegations. The Motorola chip has a fixed clock. It has the same type of a fixed clock as all the Accused Products.

And if the term "variable clock" and related terms are properly understood, I don't believe that they apply to fixed clocks. But the Motorola reference has the same characteristics as the Accused Products. And if you apply the claims in the way they've been applied by TPL, then only under that situation would the Motorola reference anticipate.

Q. I see.

So if you apply the constructions in the way that you understand them, then the Motorola reference would not anticipate the claims of the '336 Patent. Is that fair?

A. If I applied them so -- the constructions so that none of the claims cover a fixed speed clock, then the Motorola reference would not anticipate. And that's, I believe, the correct way to apply the constructions.

Q. And so, if you apply the constructions in the way that you believe is correct, the Motorola reference does not anticipate the claims of the '336 Patent, right?

A. As I explained before. So if -- if you ex -- apply them in the way that I believe is correct, they would not apply to fixed speed clocks.

Q. I want to make sure you have an accurate copy here.
All right. So turning to the back, I just want to point out that this document was dated, what does it say there, April 17th, 2013, right?
A. Yes.
Q. Okay. And in your report, you said April 13th, 2013. And I just want to make sure this is actually the same report that you meant to refer to, right?
A. It appears the same. I may have reviewed a draft.
Q. Okay. I thought it was that it looked like some of the figures from this report are the ones that you've incorporated in your report now.
Okay. So you say, here in Paragraph 31 of Exhibit 5, you say, I found particular portions of that report -- you're referring to Dr. Subramanian's report that we just marked as Exhibit 9 -- to be useful with respect to this matter and to be clear and accurate. I have adopted and/or adapted these portions of his report into this report where it will be helpful for the Court, right?
A. Yes.
Q. So you agreed with

Dr. Subramanian's -- several of Dr. Subramanian's opinions that he expressed in Exhibit 9, right?

A. To the extent that I incorporated them. In general, I didn't treat anything that I incorporated as an opinion, as much as a summary of the background. But anything -- anything that I incorporated in my own report, I agreed with.

Q. And, in fact, you said that his background was clear and accurate, right?

A. The portions that I -- that I copied.

Q. And beginning on Page 14 of your report, Exhibit 5, you discuss clock signals, right?

A. In a very general sense, yes.

Q. And you show a clock signal here at the bottom of Page 14 of your rebuttal report, right?

A. Yes.

Q. And then, as we discussed on the next page, on Page 15, you say that the ordinary meaning of frequency applied to clock signals is counting the number of oscillations between a zero value and a one value during a specific time, right?

A. Yes, the number of -- of complete cycles in a given time period.

Q. Okay. Could you also say that a clock frequency could also mean counting the number of clock edges that occur during a specific time?

A. They would be related. If you have a square wave clock and you only count the edges in one direction for a specific period of time, then that would give you the frequency.

Q. So, for example, if you counted only the rising edge of the clock signal, that would give you the frequency of the clock signal, right?

A. You could calculate it from that place.

Q. And similarly, you could calculate it from counting the falling edge of the clock signal as well, right?

A. Yes, if it is a simple square wave clock like the one that's illustrated.

Q. And when you say the one that's illustrated, you're referring to the figure at the bottom of Page 14 of Exhibit 5, right?

A. Yes.

Q. And so when we're talking about the rising edge of the clock signal, we're talking about the vertical one that goes from a value of 0 to 1, correct?

A. Generally, that's true.

Q. And the falling edge is the value that goes from 1 to 0, right?

A. In a simple example like this, yes.

Q. Okay. And so the spacing of those clock edges affects the frequency of the clock signal, right?

A. In aggregate, not necessarily the spacing of an individual edge, but the average spacing over a period of time is used to determine the frequency.

Q. Okay. Fair enough.

And you also talk about -- in your report, you talk about a ring oscillator. Can you tell me just generally what is a ring oscillator in your understanding?

A. Well, do you want my general understanding distinct from the case, or do you want my -- otherwise, the way I applied it was as it's been construed for us.

Q. Okay. So you applied the Court's construction.

Let me ask you. Separate from the Court's construction, what is your understanding of what a ring oscillator is, just generally?

A. Generally, before I came to this case, a ring oscillator is the thing that the patent calls the familiar ring oscillator. It's a structure that's most commonly used in a test circuit at the edge of a chip. It consists of an odd number of inverters or inverter-like elements in a loop, in a way that its oscillating speed is unregulated, so that it runs at correct?

A. Yes.

Q. And so this is well before the Court ever construed the term "ring oscillator" in this case. This would be a common -- common sense or plain meaning type application of the term "ring oscillator," right?

A. Not that I was familiar with. But again, I was 15 in 1978, so I didn't spend a lot of time thinking about ring oscillators.

Q. Okay. But the ring oscillator shown here in Figure 1-A, it receives a control input, doesn't it?

A. Yes, it -- and again, I haven't read this patent and I don't fully understand this circuit, but it appears to be a voltage controlled oscillator of some type.

Q. So this voltage controlled oscillator is actually a ring oscillator, at least as the inventors of this patent understood it in 1978, right?

A. The '950 Patent uses that term for a portion of Figure 1-A, but, again, I haven't really read this patent. I don't know how they're using that term.

Q. Okay. But I just wanted to make sure I understood, because I think previously you told me that your understanding outside of this case is that a ring oscillator is only a non-controlled oscillator, and

that you weren't aware of a usage to describe a controlled oscillator as a ring oscillator, right?
A. That's true. I was not aware of it -- of the term being used that way commonly or at all.
Q. But this patent does use the phrase "ring oscillator" to describe that controlled oscillator shown in Figure 1-A, right?
A. It does.
Q. Okay. Turning back to Exhibit 9, Dr. Subramanian's report. In Paragraph 97, it says that, the transistors that make up the inversion stages of the ring oscillator do not turn on and off instantaneously.
Do you see that?
A. I'm sorry. I'm in the wrong place. This is Exhibit 9, Paragraph 97?
Q. Yeah.
A. Oh, it's important to know that these transistors do not turn on and off instantaneously. I do see that.
Q. And do you agree with that?
A. That MOS transistors as illustrated do not turn on and off instantaneously?
Q. Right.
A. That is true.

Q. Okay. And then he goes on to say that this delay is what allows us to control the frequency of oscillation when we put these transistors in a loop, right?
A. Yes.
Q. Do you agree with that statement?
A. It's one of the factors. I don't know that it's the only or the dominant factor.
Q. Right. What other factors?
A. There's a propagation delay caused by the resistance of the transistor in one inverter in series with the capacitance with the gate of another inverter that provides some portion of the delay in one inverter communicating its signal to another.
Q. Okay. So the propagation delay that you just mentioned is different than the delay across the transistors; is that right?
A. I'm not a device physicist, but my understanding is that, when we do the analysis, we typically treat them separately.
Q. And so the propagation delay then also contributes to the frequency of the ring oscillator, right?
MR. WALKER: Object to the form.
THE WITNESS: That depends what you mean by

propagation delay. Propagation delay is usually the aggregate of all those delay effects.

BY MR. MARSH:

Q. Okay. So is the propagation delay related to the frequency of a ring oscillator?

A. Yes, in a -- in a -- at a very general level, the frequency of a ring oscillator is determined by the average propagation delay around the loop.

Q. So you would agree with Dr. Subramanian's testimony in the ITC that the propagation delays determined the speed or frequency of the oscillation in ring oscillators, right?

A. I don't know. I didn't hear the testimony. I don't know what the context was or I didn't know what the question was.

Q. Understood. Do you agree with the statement that I just made?

A. Can you repeat it?

Q. Yes. Do you agree that the propagation delay was determined -- oops. Hold on. Let me restate it.

Do you agree that the propagation delay determines the speed or frequency of oscillation in ring oscillators?

A. If a ring oscillator -- I think that's always true. I think that basically by definition, propagation delay is the measure of the complete signal path. So it would -- I don't know that it determines the frequency, but it -- it -- I think, if we're using the terms the same way, it's tautologically related to the frequency, that the delay, the average delay between pulses, is going to be the inverse of the frequency.

Q. Do propagation delays associated with the transistors on a chip determine the speed or frequency of the CPU of that chip?

A. They contribute to it, but the calculation's extraordinarily complex.

First place, the propagation delay of each transistor is dependent on how it's connected, what wiring is connected to it, what the capacitive load is, what the size and shape of the transistor are.

And then, even if you have all the propagation delays, you have to analyze them in circuit, in paths and determine how minimum and maximum paths interact. It's an extraordinarily complex problem. And typically when one designs a CPU, they will run hours, maybe thousands of hours of analysis, to try to determine what combination of transistor delays, transistor propagation delays, impact the minimum and maximum speed of the chip; and those things get combined in very complex and nonlinear ways.

Q. In general on a chip, when an oscillator is used to clock a CPU, would you agree that the frequency of the CPU will always track the frequency of the oscillator clocking it?

A. It depends. One, when we're talking an oscillator clocking the CPU, if we're talking about it actually directly providing the clock, I would need to understand that.

So if I make that assumption, it still depends on what level you're -- you're looking at it. If you look at it at a normal engineering macroscopic level, that would be true. If you look at it at a microscopic level where you're looking at tiny deviations, then there's always things that can cause tiny timing deviations between an oscillator and a CPU.

And if you look at it at a tiny level below the tolerance levels, they may not track.

Q. Understood. So in a normal operating condition where an oscillator is used to clock a CPU on a chip, you would agree that the -- the frequency of the CPU will vary with the frequency of the oscillation that's clocking that CPU, right?

A. If the oscillation is directly clocking the CPU, then at a higher level to within some level of precision, they will track. But if you try to analyze them perfectly to infinite precision, then they will not track.

Q. Can you describe generally what a PLL is?

A. Yes.

But -- but maybe.

So the term is used in different ways in the art. It means phase-locked loop, and it's used for a variety of different kinds of circuits that lock the phase of one signal to another; and there are different kinds of circuits that use that term. I can either start to enumerate them for you or I can, if you prefer, describe the one that's common in CPU clock generating circuits.

Q. Well, why don't we focus -- you provided a figure on Page 20 from an old patent dated 1970. This is in Exhibit 5 to this deposition.

A. Yes.

Q. Now, is this kind of a typical PLL configuration?

A. Yes. This one's a little bit archaic, but it's conceptually -- it conceptually describes what a PLL does.

A more modern one probably would not have a D to A converter. It would have a charge pump instead.

MR. WALKER: If we're going off into -- before we get off it, it's been about two hours.

MR. MARSH: Sure. Why don't we go ahead and take a break?

THE VIDEOGRAPHER: We are off the record at 3:38 p.m.

(Short recess taken.)

THE VIDEOGRAPHER: We are back on the record at 3:54 p.m.

BY MR. MARSH:

Q. So before we left, we were talking about this figure on Page 20 of Exhibit 5, and this is a figure of PLL. I notice that it includes this Block Number 7, voltage controlled oscillator or VCO.

Does a PLL always include some type of oscillator?

A. In general, no. But the PLLs that are used -- well, this particular PLL architecture, or architecture similar to it, always contain a voltage controlled oscillator, but -- or a current controlled oscillator, one or the other. That's actually not true either. There are digital PLLs that have numerically controlled oscillators.

So this type of architecture always includes an oscillator, but there are other types of PLLs that only include delay elements.

Q. Okay. So digital oscillators that will be incorporated on a microprocessor, those always include some type of oscillator, right?

A. I think you asked me if oscillators always include an oscillator.

Q. Sorry. Let me ask you this. Strike that last question. Let's ask this.

Does a digital PLL that would be incorporated on a microprocessor always include some kind of oscillator?

A. No. You'd have to look at it to know what kind of a PLL it was. But this type of a PLL, the kind that has a frequency multiplier or a frequency synthesizer in it would, I think, always contain an oscillator.

Q. And what you refer to as a frequency multiplier, that's part of the reason to use this architecture in a microprocessor setting, right, is to achieve a higher clock signal than you could achieve with an off-chip crystal?

A. Not necessarily than you could achieve, but that you prefer to generate a high speed signal on-chip rather than off-chip and use the off-chip lower speed signal as a phase reference.

Q. Okay. So this type of architecture maybe with some updates is the type of architecture that's typically used in a microprocessor setting, right?

A. Yes, for microprocessor clock generation. The other type is often used in high speed memory buses and some other things. But for clock generation for the microprocessor itself, it's not uncommon to use a frequency synthesizer or frequency multiplier made from this type of a PLL, or more modern version of this type of PLL.

Q. And you mentioned both a VCO and an ICO. Those are a voltage controlled oscillator and current controlled oscillator, right?

A. Yes.

Q. And either one of those can be used in a PLL using this architecture, correct?

A. You need to make some changes, but in general, a skilled person can -- can substitute one for the other, if they make the proper required changes.

Q. And do you agree that there's no relevant distinction for this case between a VCO and an ICO, is there?

A. I think that's true, although the claims require neither. So I'm not sure how you'd make that distinction.

Q. Can a ring oscillator be a VCO?
A. Can a ring oscillator be a VCO? A ring as it's been construed in this case?
Q. Yes.
A. There may be some weird way you could do it, but not in a normal way. Normally, the idea of having a VCO, especially within a PLL, is that you make it so that it won't vary with respect to process, voltage and temperature. That's the idea of putting it into a phase-lock loop.
Q. Can a ring oscillator be an ICO?
A. Again, not as it's been construed, not in the way that it would normally be used within a PLL.
Q. Looking at the figure on Page 20 of Exhibit 5, what's the most common type of oscillator to use on this type of architecture for a PLL?
A. A VCO.
Q. You mention, beginning on Page 23, a number of alternatives that you say can be used to create a VCO that can be used in a PLL, right?
A. Yes.
Q. And on Page 24, you show at the top of the page, a differential inverter, correct?
A. I show an oscillator that includes differential inverters within it, yes.

Q. And is the oscillator shown in that figure at the top of Page 24 of Exhibit 5 a ring oscillator?
A. I don't know if I have enough information there. For one, it would depend on what it's hooked to, where those inputs are coming from. So you would need that to know that this -- and then I would generally interpret this as only having a single inversion and not multiple inversions.
Q. So it includes inverter elements, right?
A. They're called differential inverters, but because of the -- it really depends on how you hook them up as to whether or not they have an inversion function.
Q. Are you aware that Dr. Subramanian referred to this very same figure in the ITC case and indicated that it was a ring oscillator under a very similar construction?
A. I don't know what construction he was applying, and I'm not familiar with his testimony.
Q. So you don't know whether or not you agree or disagree with his characterization of the differential inverter at the top of Page 24 of Exhibit 5 as a ring oscillator?
A. That's true.
Q. A PLL is a circuit that's used to adjust the

frequency of an oscillator, right?

A. Well, again, it depends on what kind of PLL you have.

PLL is used to lock phase. If that PLL is a frequency multiplier, then it's being used to lock the phase of one portion of -- of a circuit to another.

Q. Okay. So looking at the -- the configuration shown in the figure at the top of Page 20, that PLL circuit is used to adjust the frequency of the voltage controlled oscillator shown in that figure, right?

A. Not really to adjust it, as much as to set it. The idea is to set it to a stable value that corresponds to the reference oscillator.

Q. And what component of the figure shown here at the top of Page 20 of Exhibit 5 generates the frequency of the PLL?

A. And what do you mean by the frequency of PLL? The FM output signal?

Q. Yes.

A. In this particular design, the FM output signal is generated by the voltage control oscillator, SATA.

Q. Thank you.

When you reviewed Dr. Subramanian's report, do you remember an analogy where he compared a PLL to a

cruise control of a car?
A. I do.
Q. And do you agree that a PLL is analogous to a car's cruise control?
A. At a very, very high level. There's potential for them -- for that to be misleading. There are decisions that one would make in designing a cruise control that are different than one would typically or necessarily make in designing a PLL, but they're both examples of feedback control systems.
Q. Let me have you take a look in Exhibit 9 at Page 38. I want to look at that analogy that Mr. Subramanian cited.
A. I'm sorry? What page again?
Q. Page 38, looking at Paragraph 100 of Exhibit 9.
And in that paragraph, Dr. Subramanian says, like a cruise control keeping the car at a fixed speed, the PLL will maintain a fixed frequency by telling the controlled oscillator to slow down if the oscillator starts to speed up, and by instructing the oscillator to speed up if it starts to slow down.
Do you see that?
A. Yes.
Q. Do you agree with that statement?

A. Again, it depends what scale you're looking at.

That is generally true, but it -- it -- in a well-designed PLL, like the ones that we've seen, because of the filter, there's not really any speeding up or slowing down. Or if there is, it's by a minuscule amount, by what we would call a differential amount. It's by a -- a very tiny bit, that as soon as the oscillator slows down, you know, the minimum measurable amount -- it could be one part per million or one part per billion -- that affects the rest of the circuit which compensates for it. And that filter, which we see in most of these drawings, makes those adjustments extremely gradual, much more so than in any real cruise control that you would see, and extremely fast.

So while conceptually that's true, these adjustments are so small and so fast that they may not be observable.

Q. What causes the oscillator to speed up such that the PLL has to try to adjust its frequency?

A. There can be a number of causes. It could be -- it's not that it speeds up. It's that it's too fast. And it may be that, because of the property control loops, control loops are never perfect, but they can get extremely close to perfect.

So sometimes there may just be a little oscillation where something keeps switching back and forth between being a tiny bit too fast and a tiny bit too slow. So that would be the primary situation is that it's just not possible to achieve perfection.

Q. So I guess I didn't hear there what the cause of that switching back or speeding up or however you want to characterize it as --

A. Well, the circuit's not designed to differentiate between causes, so we would have to speculate as to what the cause of any particular frequency error is, no matter how small.

It could be that -- that there's electrical noise. That could make it go a tiny bit faster or a tiny bit slower. As I said, the most common thing is that, whatever the last adjustment was, overcompensated because these compensations aren't exact. So usually when an oscillator is going too fast, it's because it was going too slow some small period of time ago, and the feedback loop overcompensated for it. Those would be the dominant factors.

But it could be some other change in the operating conditions that cause a tiny short-term change that requires compensation. But it just as likely could be an overcompensation from some previous effect.

Q. Could one of those changes be a temperature change?

A. Theoretically, although temperature changes would tend to happen so much more slowly than those other effects, that it would be unusual, maybe even impossible, to tie a single compensation change to a temperature change.

Generally, again, just like when you're steering down the highway, you're always making minuscule up and down changes to stay as close to that line as possible. And a temperature change would aggregate over millions or billions of these tiny, tiny up and down changes.

Q. Could one of those changes be a voltage change?

A. Depends what you mean by a voltage change.

A supply voltage change?

Q. Any kind of voltage change.

A. Well, the control voltage, as I said, is always adjusting. I mean, that's just the fundamental way you control the voltage controlled oscillator.

Q. How about a change in the voltage that is associated with the power supply to the chip?

A. Most of those would show up as noise. I mean, the dominant voltage changes are noise and not changes in the nominal value.

But a change in voltage -- I mean, a drifted voltage, again, would happen over such an enormous period of time that it would aggregate over billions of tiny little up and down changes. A sudden voltage change, that's part of the noise cat -- category. A sudden voltage change just is noise and could have a short-term effect of either speeding up or slowing down.

Q. Let's -- let's look back at Page 20 at the figure on that page. And I want to ask you. The PLL shown here, it only adjusts the frequency of the VCO when there's a difference between the phase of a divided down version of that -- the frequency generated by that VCO and the frequency of the reference oscillator, right?

A. I'd have to go back and read this patent to know when this particular one makes those adjustments. It depends how all past filters and the D to A have been implemented. I don't recall for this particular design.

Q. But in general, that's true, isn't it, that a PLL only adjusts when there is a phase difference, right?

A. Yes. On each reference clock edge, it will make an adjustment. But then those adjustments get low-pass filtered. So they get changed, and generally they get low-pass filtered in the analog domain, so that contribution gets spread over time, that decision gets spread over time by the low-pass filter.

Q. Understood.

So if the PLL is adjusting the frequency at any given time, that means that the signal of the VCO and the reference oscillator are out of phase, right?

A. By some amount. Again, it could be very, very small. But yes, there's some measurable phase differential.

Q. And if they're out of phase, there wouldn't be a predictable phase relationship between them then, would there?

A. It's -- well, it's predictable to within a degree of precision, right? So you can only measure anything with a certain degree of precision, and a PLL will have an adjustment unit, right?

So as I said, you can never adjust anything to be perfect, so it's going to adjust things to be accurate within a band. So it may have a phase tolerance of, out of 360 degrees of phase, of plus or minus a half a degree. So it would keep things to within -- it would keep the phase relationship to within that tolerance, but it can't keep it perfect.

Q. Now, a PLL, when they try to control the frequency of the oscillator, they can only control that frequency to within a certain range, right, much like you just described?

A. I'm not sure if we're saying the same thing. They can only control a frequency to within a certain tolerance. I mean, nothing can make a perfect frequency. You cannot create a PLL that will give you a perfect 300 megahertz frequency. It's always going to be plus or minus some value. That value can be very, very small, but there's always going to be some tolerance.

Q. And is there a name for that tolerance or that range to which a PLL can control the frequency?

A. At that broad level, I think it's just called the frequency tolerance.

Q. Have you ever heard the term "dead band"?

A. Dead band's a little bit different, but a similar situation, where dead band is -- yes. The dead band would be the -- something within the tolerance. It would be the -- something that -- that's below the adjustment range. It's below the level of precision of control.

Q. Why do they call it a dead band?

A. I think it's because there's a range of frequencies, and a range of frequencies is always called a band. And I think that within that range, the differences are so small that you can't measure them; and therefore, you can't make any adjustments. So rather than you doing live updating, the system's kind of dead and the error is so small that you can't measure it and you can't react; so that's described as being dead.

Q. So you mentioned that the system is dead.

That's a range in which the PLL is not adjusting the frequency, right?

A. It's not adjusting it because it's determined that the error is so small that it can't measure it.

Q. Have you ever heard of the term "binning" with respect to integrated circuits?

A. Yes.

Q. What is binning?

A. It -- it varies. The most common usage is for expensive digital integrated circuits, like CPU microprocessors in which there's potential to obtain a premium price for faster products.

So products can be tested, and as they're tested, they're placed into bins that describe the test results, so that if you measure that ten percent of the product's faster, you may be able to sell those for a premium price. Lots of products don't get binned. Some products get binned based on other characteristics like estimates of reliability or operating voltage ranges or other kinds of characteristics. Just depends on the market.

But most products don't get binned. A few high price products do.

Q. So products that get binned, they're grouped together with other products that have experienced similar processing, right?

A. It depends what you mean by similar processing. They've gone through the same machines, but somehow they've turned out different. Generally, that's because there's been some difference in the processing, something uncontrolled that caused them to turn out different than other things that have gone through the same machines.

Q. So, in other words, there are process variations then that relate to the different bins, right?

A. Usually, yes. Yes. Usually, the quality of process variation. So if you've controlled everything very, very carefully, you may be able to build a four gigahertz microprocessor. But if -- if, you know, the purity of your gases one day wasn't as good or if the purity of the gas wasn't as good in one corner of your chamber as in the middle, maybe some of your parts are five percent slower.

So, in very select markets, there's enough of a price premium that it's worth characterizing those parts, placing them in different bins, getting them different part numbers.

Q. And do you know whether the processors in the Accused Products shown in Exhibits 7 and 8 are subject to binning or binned?

A. I don't know for a fact. I would assume that in general they're not. And if they are, it's not based on the accused structures.

Typically, network controllers are not binned because they all sell to the same application at the same price. Typically, memory interfaces for flash memory are not binned, and when most disc drive controllers are not binned -- and when they are binned, it's based on the capability of the read channel and not on the processor clock speed.

Q. But you said you don't know for a fact. That's an assumption on your part that the processors in the Accused Products are not binned, right?

A. That's right. They've thought of product categories that are generally not binned, but I don't know for those particular part numbers.

Q. You mentioned that they might be binned based on something other than the accused structures.

What did you mean by that?

A. Sometimes for a disc controller -- and it varies from year to year depending on where the market is -- there's some value in binning them based on read channel speed so that one can build a higher density disc drive, but not based on CPU speed.

So the CPUs would all run at the same speed. There's a separate PLL that controls the speed of the read channel, and there's a separate read channel amplifier. And sometimes it makes sense to bin those products based on the read channel amplifier speed, but not based on CPU clock speed.

Again, somebody might do it, but I'm not aware of anybody in that market who's doing it.

Q. You said in that case, the CPUs would be all the same speed. But you really don't know, do you, if they're not binned based on the CPU speed, whether the CPUs are all the same speeds?

A. Well, they are, because -- I don't know if they all have the same speed capability, but they're all operating at the same speed. They all run the same firmware. They all run the same reference clock.

Again, this is from an engineering perspective. They could differ by a hundredth of a percent or something between two units, but they go through the factory and they're all set for the same fixed speed.

Q. Yeah. Understood. I guess my question's a little bit different, and that is, if they're binning based on the characterization and the way that the read channel works and that is different because of process variations, we don't know whether or not, according to your testimony, whether those process variations might also affect the transistors that make up the CPUs on the same chip, do we?

A. No. We'd have to know two things. One, as I said, generally there are different kinds of transistors on these chips, and the fact that one type of transistor is faster doesn't necessarily mean that the transistors in the CPU are faster.

And it's possible that the CPUs in some of the binned chips could potentially run at a higher clock speed. They just don't because they're connected to a fixed clock that runs at a fixed speed.

Q. Do you know whether the chips in the Accused Products in Exhibits 7 and 8, whether they have transistors that make up the CPU that are different from the transistors that make up the oscillator that clocks the CPU?

A. Not for certain. That would be common. Usually, one would use an analog transistor type for the PLL and a different digital transistor type for the CPU, but that's not universal.

Q. So you don't know one way or another with respect to the Accused Products?

A. Well, let me hear the whole question again.

Q. My question is, whether the transistors that make up the CPU on the chips in the Accused Products in Exhibits 7 and 8 are different than the transistors that make up the oscillator that clocks that CPU on the same chip?

A. I don't know whether or not they're built from the same process steps.

Given my knowledge of CPU design, it would be almost impossible for them to have the same size and shape, but I don't have any facts other than my knowledge of the fact that it would be almost impossible to design a working CPU with the characteristics that are in the data sheet, if the transistors had the same size and shape as the clock oscillator.

Q. Claim 6 of the '336 Patent refers to fabrication for operational parameters, right?

A. Yes.

Q. What's a fabrication parameter?

A. I believe it's a measurable characteristic of the materials that is due to manufacturing.

Q. And so if there are variations in a fabrication parameter, those are process variations, right?

A. They're result variations. In other words, two chips may have gone through was intended to be the same process, but you ended up with different things at some level. And these processes are so -- so far out in the extremes of manufacturing technology that you can have a 30 percent difference between two things that were manufactured on the same wafer.

Q. Let me have you look at Exhibit 9, Page 39. In Paragraph 102, Dr. Subramanian discussed the possibility of chips that might have the same design and the same architecture, but yet might be graded at different frequencies.

Do you see that?

A. Yes.

Q. That's binning, right? That's what we've been talking about?

A. Yes.

Q. And that's due to process variations, right?

A. Primarily. Primarily, it's due to -- again, we need to be clear what we're talking about by process variation. It doesn't mean they were intentionally made differently, but it means that they turned out differently in the manufacturing process.

Q. And they turned out differently because there was some difference or some variation in the process that was applied to the different chips, right?

A. Yes, at some level. Again, we're talking about super tiny things, and sometimes you're just down into quantum mechanics and how crystals line up and things like that.

But somehow there was a difference in the manufacturing process.

Q. And that process variability, that affects performance of the microprocessors, right?

A. It can affect performance in very complex ways, either up or down.

Q. Does process variation affect propagation delay?

A. It can affect propagation delay of a single transistor.

Q. Dr. Subramanian testified that temperature, voltage and process can affect transistor propagation delays.

Do you agree with that statement?

A. Depends how the transistor is being used. In the way that you would measure and test an individual transistor, that would be true. Once a transistor is placed in a circuit, it may not be true anymore.

Q. Let's take a look at Exhibit 5 on Page 44. This is your rebuttal report. And in Section 8.1.2 of your rebuttal report, you say that the accused clock or oscillator does not vary as the term is used in the '336 Patent as would be understood by a person of ordinary skill in the art, right?

A. I'm sorry. I didn't follow where you were.

Q. Sorry. I'm reading -- probably because I didn't explain it very well.

So looking at Paragraph 81, for example, you say that the oscillator in the Accused Products are different structures -- I'm sorry. Strike that.

In Paragraph 80 on Page 45, you say that the claim limitations that include the phrases, the first clock limitations of the '336 Patent, you say that they're not present in any of the Accused Products.

And so none of those products infringe, right?
A. Yes.
Q. Okay. And down below you say, in Paragraph 82, that the '336 Patent clearly indicates that its references to a variable speed clock refer to a clock that provides a frequency that varies substantially, right?
A. That's part of what it says, yes.
Q. And what is the basis for that statement?
A. The things we've talked about before, ordinary meaning of variable speed clock; the fact that the patent clearly differentiates a variable speed clock from a fixed frequency clock, a fixed speed clock. All the teachings of the patent about the variable speed clock are teaching how it's different than a traditional clock oscillator.
A traditional clock oscillator will have uncertainty. It will have jitter. Those aren't things that make something a variable speed clock from the perspective of the patent or from the perspective of a person of ordinary skill.
Q. Okay. Well, let's take a look at the patent, which is Exhibit 2. And I think we discussed previously that the word "substantially" doesn't appear in the claims, right?

A. That's true.

Q. For instance, if we look at Claim 6, the word "substantially" doesn't appear in that claim, does it?

A. That's true.

Q. And you mentioned here that the patent, the '336 Patent, refers to a variable speed clock, right?

A. In different ways. I mean, I don't think that's the exact language for most of the claims, but -- and there's various things that I list in my report that describe a variable speed clock.

Q. Okay. But Claim 6 has a clock that's just described or claimed as an entire oscillator, doesn't it?

A. Yes. But it also says requires varying the processing frequency of that oscillator.

Q. Understood. But that's separate language, right?

I mean, the oscillator itself isn't described as a variable speed clock or a ring oscillator variable speed clock.

This is a different claim, right?

A. It's not described as a ring oscillator variable speed clock, but I put the language and the reasoning into Paragraph 80. It certainly is a clock that varies. So when I use the general term "variable speed clock" to refer to what's disclosed in the patent, sometimes the claims call it a variable speed system clock and sometimes they call it a clock that varies its processing frequency or varies its clock rate.

Q. I see. So you're referring to the language here that you attribute to Claims 6, 7 and 9 in Paragraph 80 of Exhibit 5, right, the language that -- it's really the varying terms of -- the varying claim term of those claims, right?

A. In those three claims, that's right.

Q. Okay. But that's not the first clock or the oscillator claim term, is it?

A. Well, it's a required limitation of the first clock.

Q. Okay. But it's a separate limitation. I mean, the first clock is described here or claimed here as an entire oscillator, right?

A. Yes, but it doesn't change the fact that you can't practice Claims 6,7 or 9 with a fixed speed clock that doesn't vary.

Q. So you go on in your report to cite a single example in Paragraph 82, which goes over onto Page 46 of Exhibit 5.

That's a single example from the specification that you say indicates that the -- the clock varies by 100 percent over a temperature range, right?

A. That's the only quantitative example. As I mentioned in 81, it also notes that a fixed clock is different than a variable speed CPU. And that's in Column 17.

Q. Yeah. Understood.

Is this -- is there any language in the '336 Patent that you're aware of that says that the claim should be limited to that particular example that you cite in Paragraph 82 of Exhibit 5?

A. No.

Q. And are you aware of anything in prosecution history that would indicate an intention to limit the claims to that example?

A. No. I do think both the claim language and the prosecution history would limit the claims to a substantial variation. And this is one example of, given a substantial variation. But I don't think that for -- I don't think that you have to vary by 100 percent between 70 C and room temperature in order to practice the claims.

Q. Okay. So let's unpack what you said there a little bit.

You said that both the claim language and the prosecution history would limit the claims to a substantial variation. So let me ask first about which claim language of Claim 6 would limit that claim to a substantial variation?

A. The language that I cited in Paragraph 80, that the claims require varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way, as a function of parameter variation, et cetera.

Q. So I saw varying. I didn't see substantially there, right?

A. Yes.

Q. Okay.

A. Substantially is not literally there, but that's how a person of ordinary skill would understand it.

Q. Okay. Is there any other claim language that you would say limits Claim 6 to a substantial variation?

A. Nope. I think that's it.

Q. Okay. And what in the prosecution history would limit the -- would limit Claim 6 to a substantial variation?

A. I'd have to go back and review the history.

But my recollection is that the claims were distinguished from art that had fixed frequency oscillators, and those fixed frequency oscillators, like all circuits, all oscillators, would have had negligible variations.

Q. But you don't cite anything from the prosecution history here in your rebuttal report that would require the claim language or -- invent some sort of intent on the part of the applicant to limit the claim language to a substantial variation only, do you?

A. Just the things that I cited in Paragraphs 80 and 81 that are in the specification -- I'm sorry -- 81 and 82. And it's very clear from the specification itself and the claims that variable speed and fixed speed are two different things. And that, together with the ordinary meaning of vary, is what I relied on.

Q. But the specification doesn't tell us where to draw that line, does it, between fixed speed and variable speed?

A. Not quantitatively, no.

Q. And you testified earlier that you didn't decide where that threshold should be, where that line is between fixed speed and variable speed clocks, right?

A. Not precisely. I decided it clearly had to be more than the clock tolerance. And certainly, the example given in the patent is variable.

Q. In Paragraphs 89 to 93 of Exhibit 5, you discuss jitter, right?

A. Mm-hmm. Yep.

Q. And so we talked about jitter earlier. One question that I wanted to ask about this though is, does jitter affect when a clock edge arrives at a CPU?

A. It can affect when an individual clock edge arrives at a CPU.

Q. And if there's jitter, it's going to have an affect on multiple clock edges as well, right?

A. No. Well, I mean, statistically, yes, but it's a statistical property. Every clock edge is going to have some jitter, no matter how small. No clock edge is going to be perfect. But the jitter that affects one clock edge may not impact the adjacent or any other clock edge.

Q. Turning now to Page 56 of Exhibit 5. In Section 8.1.3, you express an opinion that the accused clock or oscillator does not vary either due to or as a function of or relative to PVT parameters, right?

A. Correct.

Q. And you -- you quote here some language on Page 57 of Exhibit 5 from Claims 6 and 13 and 10 and

16, right?

A. Yes.

Q. And would you agree that those claims, they only require variation due to one of the PVT parameters, right?

A. Yes, for those four claims, that's true.

And in case I wasn't clear, my opinion is that the accused oscillators don't vary as a function of any of the three.

Q. But you did testify before, didn't you, that process variations would affect any chip that's manufactured according to a process that's subject to process variability?

A. It would affect certain physical parameters, but it would not necessarily affect the frequency of a circuit.

That's why we design complex circuits, is so that they're compensated so that they can operate in the same way independently of changes.

That's the same reason why your television operates the same way when you're at 108 volts as it does at 110 volts, and it operates the same way at 72 degrees as it does at 74 degrees. It's because it's been designed with sophisticated circuits that compensate for and eliminate the impact of any of those kinds of changes.

Q. I understand where you're coming from.

Let me ask you this: Process variations are baked in during the manufacturing process, right? I mean, they're part of the chip. Once the chip is manufactured, those process variations have already affected the transistors on that chip?

A. That's actually not true for some pretty complex reasons.

Q. I'm all ears.

A. These are physical materials that change over time. They change due to a number of effects, corrosion, carrier migration, something called electromigration, where metal ions move when circuits -- when current flows through; and in some cases process variations affect the way that a chip will physically and chemically change later, rather than the way that it actually -- in addition to the way that it actually exists when it leaves the factory.

Q. Okay. I understand.

So there are some qualities that process variations will affect permanently once it is manufactured, and there are some others that may also continue to -- some post-processing variation that may continue to be affected by any variation to the

processing procedure, right?
A. That is true.
Q. So let's focus for a minute on the types of characteristics that process variations fix in an integrated circuit, okay?
MR. WALKER: Read that question back.
BY MR. MARSH:
Q. Well, it wasn't really a question. I want to focus for just a minute on, not the types of post-processing variations that process variations can later cause to arise. I want to focus instead on the permanent characteristics that are fixed because of process variations.
Does that make sense?
A. I don't know whether or not you can segregate them. I mean, what one would normally do is they would measure the material as it leaves the factory, and then you could measure it later.
So you can talk about how two chips vary at the time that they're made or at the time that they're sold. That's a logical thing to try to talk about.
Q. Okay. Let's talk about chips at the time that they're sold.
So if those chips have been subject to some process variations that caused the manufacturer to bin

them according to CPU speed, then that means that the CPU is only capable of operating at the speed that corresponds to the bin that they're put in, right?

A. No.

MR. WALKER: Objection that it's an incomplete and improper hypothetical.

Go ahead.

THE WITNESS: That's generally not true.

Binning is primarily not a manufacturing driven activity. It's primarily a market driven activity. So while it could be done in different ways, typically you simply test to see whether or not a product works at a certain speed. And then if it passes or fails, you may test at a different speed.

And depending on how that's done and where the market requirements are, it's not uncommon to have chips in a bin that could run in a much faster speed, but you don't have orders for the faster speed. So you just test them at the speed that you have orders for and figure out whether or not they should go in that bin.

BY MR. MARSH:

Q. Well, let's talk about a situation where two chips that have the same design go through manufacturing, and they come out and they're tested and

they run at different speeds?
A. Okay.
Q. And that's a common situation where one would use binning, right?
A. One could use binning. Again --
Q. Okay.
A. -- you use binning when you have customers who are willing to pay different prices at different speeds. There are thousands and thousands of products where you'll have chips that are at different speeds, but you don't use binning because customers won't pay different things for different speeds.
Q. Understood.
So let's say that those two chips that are identical in design, but because of some variations in the processes that they've both underwent, they run at different speeds.
A. Okay.
Q. And let's say that the first chip runs at a maximum of one gigahertz.
A. Okay.
Q. And the second chip runs at a maximum of two gigahertz.
Does that make sense?
A. That would be very unusual, but --

Q. That's a big process variation, sure.
A. But I can use that as a presumption.
Q. Yeah. I just want to use it as an example.
You wouldn't then try to clock the one gigahertz at two gigahertz, would you?
A. No. You would either -- for most products, you would clock them both at one gigahertz. But for some products in certain product categories, you would put two different part numbers on them and you would clock one of them at one gigahertz and one of them at two gigahertz.
Q. Sure.
So if you were then using a reference oscillator to drive the frequency or to act as a reference for a PLL on the chip -- strike that.
If you were using a crystal oscillator with each of those, you wouldn't attempt to use a crystal oscillator to cause the first chip that can only run at a maximum speed of one gigahertz to run at two gigahertz, would you?
A. I mean, you could.
MR. WALKER: Object to the form of the question.
THE WITNESS: You could. But you -- it wouldn't be commercially sensible to try to run a

clock -- a chip faster than the maximum speed you had tested it at.

BY MR. MARSH:

Q. And it likely wouldn't work, would it?

A. It likely would not work.

Q. Let's take a look on Page 58 of Exhibit 5 in Paragraph 113. You say that, it's clear to a person of ordinary skill in the art that the references to operating voltage and operating parameters in the 336 claims refer to or include the supply voltage and do not include the voltage of control signals within the oscillator, right?

A. Yes.

Q. What's the basis of that statement?

A. It's the only meaning that's consistent with the teachings of the '336 Patent. There are a number of reasons.

One, even -- any embodiment of the 336 is going to have tens of thousands, or in modern day, billions of different voltages, and clearly they're not all going to vary proportionally or in the same way.

When -- and the invention would not operate as described, if it were referring to control voltages. But perhaps the most practical issue is that the CPU would essentially never have any connection or visibility to a control voltage within an oscillator, so it couldn't vary in the same way or respond in any way to that voltage.

The only voltage that's common between the CPU and the oscillator is the supply voltage. So when the patent talks about voltage, that has to be what it's talking about.

Q. So in -- don't the inverters in a voltage controlled oscillator receive both the supply and the control voltages at the same node? Doesn't the control voltage just buy us the supply voltage on the inverters of the voltage controlled oscillator?

A. Not in any design that I'm familiar with, no.

Q. How do they work instead?

A. Well, there's lots of different kinds of voltage controlled oscillators, so we'd have to look at each one. But generally they're connected to separate circuits.

The control voltage is used to control some timing parameter, like the charge on a capacitor or the current limit along some path. And the supply voltage is used for other things, like the normal supply voltage of other amplifiers or buffers. Buffers might be inverters.

Q. So when we're talking about inverters, we're

really talking about transistors, right?
A. Inverters are made of transistors. Some simple ones are made of two transistors, but some inverters are made of many transistors.
Q. And so the control voltage is applied where on the transistor that makes up the inverter?
A. It depends what the design is. It may not be supplied to the same -- I mean, it may be supplied to a different transistor than the one that's in the inverter.
But commonly a control voltage is applied to a gate where a supply voltage is applied to a source. But that's not always true. It would depend on the particular design of the oscillator.
Q. Let's look on Page 59 in Paragraph 115 of Exhibit 5. You say that LSI's witness explained that the LSI chip in the Acer Accused Products provides a constant frequency, right?
A. Well, a particular chip. I mean, I can tell you what I actually said, is that LSI's witness explained that LSI designed the B5503A PLLs to provide a constant fixed frequency clock signal despite changes to PVT.
Q. And are you aware that LSI's witness also testified, despite attempts to provide a steady

frequency, in practice the clock source was never ideal and does change some?
A. I don't remember that exact testimony, but that wouldn't surprise me. As I said, there is no such thing as a perfect clock, and everything changes, at least in a tiny amount, all the time.
Q. Did you review the LSI's witness's deposition?
A. Yes.
MR. MARSH: Let's mark Exhibit 11, which is the deposition transcript of Joseph A. Casasanta, dated February 20th of 2013.
(Deposition Exhibit No. 11 was marked.)
BY MR. MARSH:
Q. Have you reviewed -- this is the deposition transcript that you reviewed before?
A. Yes.
Q. Why don't we take a look at Page 139 of the transcript?
And do you see in Line 16, Mr. Casasanta was asked, you said that by design, the PLL frequencies was designed not to change, but in practice it's never perfect, correct?
And in response, beginning on Line 19 of Page 139, he said, I testified that the clock source is never ideal. It will have a source of offset

characterized by jitter.

Do you see that?

A. Yes.

Q. And do you see, he was asked if jitter was affected by PVT, and he said yes, it is?

A. That's true.

Q. Do you disagree with his testimony here?

A. No. But it doesn't say there's frequency changes. It's jitter. It's the amount of error.

So what it means is that there is some uncertainty or some error that is going to be affected by PVT. So the higher temperature, the error in individual clocks may vary by plus or minus a certain amount, but it's still going to have the same statistical properties. It's still going to have the same mean frequency. So the frequency is not changed, just the amount of noise, the amount of error that's present.

Q. Are you aware that this same LSI witness, Mr. Casasanta, testified that a ring oscillator inside an on-chip PLL clocks the CPU of the chip that's in the accused Acer products?

MR. WALKER: Object to form, assumes facts not in evidence.

THE WITNESS: Can you point me to something?

BY MR. MARSH:
Q. Yeah. Why don't we take a look at Page 27 of Exhibit 11?
A. So he said there was a ring oscillator inside the PLL, but my recollection is that he also testified that he didn't know what the Court's construction of the term "ring oscillator" was. So I assume he wasn't applying the Court's claim construction.
Q. Okay. So there was a ring oscillator as understood by someone skilled in the art here though, right?
A. Separately from the way it's used in the patent, not applying the claim construction? Yes, there was something that he called a ring oscillator that is present in one of -- in the LSI B5503A.
Q. And he testified that the PLL, which would include that oscillator, was entirely on the chip, right?
A. Yes, he did testify that the PLL was entirely on the chip.
Q. And that PLL includes the ring oscillator that he said is inside the PLL, right?
A. I would presume so in the way that he's using the term "ring oscillator."
Q. And he also said that that PLL was the source

testified that the CPU and the PLL are made from the same process technology?

A. Where is that testimony?

Q. Well, let's take a look. It's on Page 133 of the transcript. If you look beginning at Line 10 through 25.

A. Okay.

Q. Okay. So the LSI witness, Mr. Casasanta, testified, didn't he, that the CPU and the PLL are made from the same process technology?

A. He did.

Q. And so, because they're made from the same process technology, they would similarly be affected by process variations, right?

A. No. For a number of reasons, that's not true.

Q. Even though they're made from the same process technology?

A. Well, first we have to make sure that his understanding of made from the same process technology is the same as ours.

Sometimes engineers will say something's made from the same process technology when they go through the same sequence in machines, not that the transistors are actually made the same way. It's ambiguous, based on his answers, as to which one he's saying.

But even if he were saying the transistors were made the same way, there are process variations at different locations on a chip, on the same chip. That's common. And the transistors may not be the same size or shape, in which case, they would not respond to the manufacturing variations in the same way.

Q. I want to take a look at Page 65 of your rebuttal report, Exhibit 5.

A. Yes.

Q. And here you quote some excerpts from a textbook that Dr. Oklobdzija cited, right?

A. Yes.

Q. And -- and these selections confirm that variation and fabrication are process parameters that impact the electrical performance of -- of microprocessors, right? It's what they call physical factors in this topmost excerpt on Page 65 of Exhibit 5.

A. Yes. It says that they are random or spatially varying. So they could be random on the chip or spatially varying between components of the chip. So it wouldn't mean that individual transistors would vary together, so it does not support the claim language. It just simply says that components can vary due to manufacturing variations, which is certainly true.

But components on the same chip wouldn't necessarily vary together, and circuits don't vary together just because individual transistors vary together, even if that were the case.

Q. This topmost selection also confirms that operational parameters, such as temperature or voltage, which are called environmental factors here, impact the electrical performance of microprocessors too, right?

A. They can have an impact, but that impact may not be predictable. And of course, if you look at this carefully, it does say that they include variations in power supply, switching activity and temperature of the chip or across the chip.

Temperature differences across the chip would mean that things don't vary in the same way, and switching activity is localized and also would mean that things don't vary in the same way.

Q. Let's turn to Page 69 of Exhibit 5. In this Section, Section 8.1.5 of your rebuttal report, you say that the Accused Products do not clock the CPU with an entire oscillator disposed upon the integrated circuit substrate, right?

A. Yes.

Q. But we just reviewed some deposition testimony from Mr. Casasanta that says that the PLL clocks the ARM CPU and that that PLL is located entirely on the chip, right?

MR. WALKER: Object that it misstates the prior testimony.

BY MR. MARSH:

Q. That's what the testimony said, isn't it?

A. Well, but if we read the entirety of Mr. Casasanta's testimony, he said that the PLL was not the entire oscillator.

The entire oscillator is the circuit that includes the crystal, the crystal oscillator, the PLL and the clock generator circuit. All those things together in sequence depend on each together to produce the clock for the CPU, and that's not entirely on the chip.

Q. But he did testify that the PLL itself was entirely on the chip, right?

A. That was his testimony. I don't know for certain exactly what he was including in that, but -- but the crystal oscillator is the part of the entire oscillator that's off-chip.

Q. And --

A. I'm sorry. The crystal, not the crystal oscillator.

THE VIDEOGRAPHER: This is the end of Volume 3 of the videotaped deposition of Mr. -- Dr. Andrew Wolfe. We are off the record at 5:43 p.m. Thank you.

(Deposition proceedings concluded at 5:43 p.m.)

JURAT

I, ANDREW WOLFE, PH.D., do hereby certify under penalty of perjury that I have read the foregoing transcript of my deposition taken on Friday, July 19, 2013, that I have made such corrections as appear noted herein in ink, initialed by me; that my testimony as contained herein, as corrected, is true and correct.

Dated this _____ day of ________________, 2013, at _____________________________________, California.

____

ANDREW WOLFE, PH.D.

CERTIFICATE OF REPORTER

I, Hanna Kim, a Certified Shorthand Reporter, do hereby certify:

That prior to being examined, the witness in the foregoing proceedings was by me duly sworn to testify to the truth, the whole truth, and nothing but the truth;

That said proceedings were taken before me at the time and place therein set forth and were taken down by me in shorthand and thereafter transcribed into typewriting under my direction and supervision;

I further certify that I am neither counsel for, nor related to, any party to said proceedings, not in anywise interested in the outcome thereof.

In witness whereof, I have hereunto subscribed my name.

Dated: ____ day of ___________, 2013

____

Hanna Kim

CLR, CSR No. 13083

ERRATA SHEET FOR THE TRANSCRIPT OF:

Case Name: Acer Inc., et al. versus TPL, et al.

Dep. Date: July 19, 2013

Deponent: Expert Deposition, Andrew Wolfe, Ph.D.

CORRECTIONS:

Pg.	Ln.	Now Reads	Should Read	Reason
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Signature of Deponent

SUBSCRIBED AND SWORN BEFORE ME

THIS____DAY OF___________, 2013.

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(Notary Public) MY COMMISSION EXPIRES:________________

EXHIBIT J
To Omnibus Declaration of Irvin E. Tyan ISO Defendants' Opposition to Acer and HTC's Motions for Summary Judgment

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION, and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00877 PSG **REBUTTAL EXPERT REPORT OF ANDREW WOLFE PH.D.** **[RELATED CASES]**
HTC CORPORATION, and HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00882 PSG

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licensed to Marvell. PIC00011863. Marvell makes dozens, perhaps hundreds, of different products. Dr. Oklobdzija has identified no evidence linking the ARM966E-S CPU to the Marvell 88i6745. Similarly, for the Realtek RTS5111, Dr. Oklobdzija cites no evidence that the identified PLL generates the clock signal received by the CPU. The CPU in this chip is an 8051 which traditionally operates at the 12MHz frequency of the crystal oscillator on the RTS5111. The PLL is most likely related to a different part of the chip. In any case, Dr. Oklobdzija has no evidence that these structures are connected as claimed. Similar deficiencies exist throughout Appendix H. Since Dr. Oklobdzija has not relied on these allegations (other than ACER-A-1 and ACER-A-2) in his current report (*See* Oklobdzija report at ¶173-176), I have not identified every deficiency in the other sections of Appendix H. I will do so if Dr. Oklobdzija provides additional opinions.

8.1.2. The accused "clock" or "oscillator" does not vary as that term is used in the ’336 patent and understood by a PHOSITA.

80. Each of the asserted ’336 claims requires a variable speed clock connected to a CPU. Claim 1 requires a “variable speed system clock … connected to said central processing unit for clocking said central processing unit.” Claims 6, 7, and 9 require “varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation.” Claim 10 requires “an entire variable speed clock disposed upon said integrated circuit substrate.” Claim 11 requires “an entire ring oscillator variable speed system clock in

said single integrated circuit and connected to said central processing unit for clocking said central processing unit." Claims 13, 14, and 15 require "varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate." Claim 16 requires "an entire variable speed clock disposed upon said integrated circuit substrate." For the reasons discussed below, the claim limitations that include these phrases are not present in any of the accused products. As such, it is my opinion that none of the accused products infringe any asserted '336 claim.

81. In each of these cases, the claims require a clock that is variable speed as opposed to a fixed-speed clock. Claim 2 claims two distinct clocks, a "variable speed system clock" and a "fixed frequency clock." These are clearly different structures from the perspective of the patent and a person of ordinary skill reading the patent would understand the references to "variable speed" and "fixed speed" to be intended to differentiate these clock types as distinct. From the perspective of this patent (and ordinary usage in the art at the time of the alleged invention), a clock cannot be both fixed-speed and variable speed. The patent is also clear that CPU 70 which is disclosed as operating at a variable speed is different from operating at a fixed speed. *See* '336 at 17:32-34.

82. The '336 patent clearly indicates that its references to a variable speed clock refer to a clock that provides a frequency that varies substantially, well in excess of any jitter or other

timing uncertainty. The only example provided in the patent varies by 100% (i.e. doubles in speed) between 70°C and room temperature.

83. “The ring oscillator frequency is determined by the parameters of temperature, voltage, and process. At room temperature, the frequency will be in the neighborhood of 100 MHZ. At 70 degrees Centigrade, the speed will be 50 MHZ. The ring oscillator 430 is useful as a system clock, with its stages 431 producing phase 0-phase 3 outputs 433 shown in FIG. 19, because its performance tracks the parameters which similarly affect all other transistors on the same silicon die. By deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast. For example, if the processing of a particular die is not good resulting in slow transistors, the latches and gates on the microprocessor 50 will operate slower than normal. Since the microprocessor 50 ring oscillator clock 430 is made from the same transistors on the same die as the latches and gates, it too will operate slower (oscillating at a lower frequency), providing compensation which allows the rest of the chip's logic to operate properly.” *See*’336 at 16:59-17:10.

84. The ’336 patent also discusses the reason for using a variable-speed clock and the problem that it solves. The patent explains that:

> “Traditional CPU designs are done so that with the worse case of the three parameters, the circuit will function at the rated clock speed. The result [sic] are designs that must be clocked a factor of two slower than their maximum theoretical performance, so they will operate properly in worse case conditions.” ’336 at 16:48-53.

85. All of the accused products are designed to operate in exactly this “traditional” manner. They operate at the same fixed clock speed at room temperature and specified typical

voltages as they do under worst-case temperature and voltage conditions. They operate at the same fixed clock speed as long as the manufacturing process is within the specified acceptance range. The clock speed is no faster on a chip that happens to be manufactured with fast transistors than a chip which happens to be manufactured with slow transistors. In general, all of the accused products are clocked “a factor of two slower than their maximum theoretical performance, so they will operate properly in worse case conditions.” The problem described in the ’336 patent is still present since the accused products all still use the prior art fixed-speed clocking technique.

86. No real-world signal in a real-world system is ever perfect. This is a fundamental physical phenomenon. Despite this reality, engineers commonly specify fixed values for signals and components and treat those values as fixed for all practical purposes. A specific model of a ruler is 12 inches long. In the real world, every one of those rulers that is produced may differ in length by a small fraction of a percent. The length of that ruler will change due to temperature and perhaps humidity due to the expansion or contraction of the wood or metal that it is made from. The ruler will flex slightly due to minute vibrations that are present everywhere and thus the length of the ruler will slightly change. The length may change slightly due to stresses within the material. Despite these imperfections, engineers who design rules and users who use them consider them to be of fixed length and rely on them as accurate enough for the purpose for which they were intended. An engineer may specify one or more tolerances to characterize the likely variation in length between units or over time. A user would obtain a ruler that is accurate enough for the suited purpose. A draftsman may need a more precise ruler than a kindergartener, but both would consider a suitable ruler to have a fixed length in the context in which it is

availability. In particular, potential customers for the accused products are not aware of the brand of hard disk or the controller chips used on the hard disk. The purported technology is, at best, a commodity-type feature. The asserted patents have no impact on buyer preferences, and certainly would not be the sole motivation for consumers to purchase the accused products.

Dated: July 2, 2013

Andrew Wolfe Ph.D.

EXHIBIT K
To Omnibus Declaration of Irvin E. Tyan ISO Defendants' Opposition to Acer and HTC's Motions for Summary Judgment

UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF CALIFORNIA
SAN JOSE DIVISION

HTC CORPORATION, et al., Plaintiffs, vs. TECHNOLOGY PROPERTIES LIMITED, et al., Defendants.	CASE NO. 5:08-CV-882 CONFIDENTIAL OUTSIDE ATTORNEYS' EYES ONLY
ACER, INC., et al., Plaintiffs, vs. TECHNOLOGY PROPERTIES LIMITED, et al., Defendants.	CASE NO. 5:08-CV-877 CONFIDENTIAL OUTSIDE ATTORNEYS' EYES ONLY

UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.

In the Matter of CERTAIN WIRELESS CONSUMER ELECTRONICS DEVICES AND COMPONENTS THEREOF	Investigation No. 337-TA-853 CONFIDENTIAL BUSINESS INFORMATION QUALCOMM OUTSIDE ATTORNEYS' EYES ONLY

CONFIDENIAL OUTSIDE ATTORNEYS'S EYES ONLY

CONFIDENTIAL BUSINESS INFORMATION
QUALCOMM OUTSIDE ATTORNEYS' EYES ONLY

VIDEOTAPED DEPOSITION OF SINA DENA
SAN DIEGO, CALIFORNIA
THURSDAY, FEBRUARY 7, 2013

UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF CALIFORNIA
SAN JOSE DIVISION

HTC CORPORATION, et al., Plaintiffs, vs. TECHNOLOGY PROPERTIES LIMITED, et al., Defendants.	CASE NO. 5:08-CV-882 CONFIDENTIAL OUTSIDE ATTORNEYS' EYES ONLY
ACER, INC., et al., Plaintiffs, vs. TECHNOLOGY PROPERTIES LIMITED, et al., Defendants.	CASE NO. 5:08-CV-877 CONFIDENTIAL OUTSIDE ATTORNEYS' EYES ONLY

UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.

In the Matter of CERTAIN WIRELESS CONSUMER ELECTRONICS DEVICES AND COMPONENTS THEREOF	Investigation No. 337-TA-853 CONFIDENTIAL BUSINESS INFORMATION QUALCOMM OUTSIDE ATTORNEYS' EYES ONLY

CONFIDENIAL OUTSIDE ATTORNEYS'S EYES ONLY

CONFIDENTIAL BUSINESS INFORMATION
QUALCOMM OUTSIDE ATTORNEYS' EYES ONLY

VIDEOTAPED DEPOSITION OF SINA DENA
SAN DIEGO, CALIFORNIA
THURSDAY, FEBRUARY 7, 2013

Videotaped deposition of SINA DENA, taken on behalf of Defendants, at 4401 Eastgate Mall, San Diego, California 92121-1909, commencing at 9:46 a.m., Thursday, February 7, 2013, before Dorien Saito, CSR 12568, CLR.

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ALSO PRESENT:

DANIEL BERMUDEZ, Videographer
ROBERT GILES, Qualcomm, Senior Legal Counsel

A. Still after reading this, I still don't know if there's a ring oscillator in here or not.

Q. Do you see the mention of ring oscillators in the third line from the top down?

MR. CHEN: The document speaks for itself.

THE WITNESS: Are we talking on the same page?

BY MR. PHAM:

Q. On page 13.

A. On page 13.

MR. DAMSTEDT: He's talking about this line.

THE WITNESS: Oh. The three-stage current control ring oscillators. Okay. I saw it.

BY MR. PHAM:

Q. Are there ring oscillators in the PLL?

MR. CHU: The same objections.

MR. MEHTA: Also scope and it calls for speculation.

THE WITNESS: This document mentions ring oscillators. This document is the data sheet. If the data sheet is corresponding correctly to the actual design, then yes.

///

BY MR. PHAM:

Q. Do you need to look at these data sheets in order to tell whether there are ring oscillators in the PLL?

MR. MEHTA: The same objections.

THE WITNESS: I would rely on talking -- if I wanted to find out something, I would rely on -- not documents, but the designer.

Unfortunately, for -- my use of these data cases are mostly with the external interfaces of this clock, not really what's inside of it, so -- so that I know how to hook up the signals to it and how to use it. What's inside, I don't really pay attention.

If the document says it's there, if the document is accurate, then it's there.

BY MR. PHAM:

Q. Who would pay attention to the inside of the PLL at Qualcomm?

A. Designers and people who have to do the characterization of the PLL when the silicone arrives because these are new designs. Every time a new design goes on the silicone, it has to be characterized, the cross-process, variation, corners, and all of that.

That is where a lot of the scrutiny goes on in all the inside elements, whether their act was temperature, voltage, process. This clock performs based on this spec that was defined.

THE VIDEOGRAPHER: Okay. Bad telephone interference.

Anybody have their phone in their pocket?

That's for you or maybe just put your phones on the table. You don't have to necessarily turn them off, but you can put them on the table. Just put it on the table, Counsel, you're going to turn it off. I mean, if you're going to turn it off in your pocket you can turn it on.

BY MR. PHAM:

Q. Have you talked to any designers?

A. Quite frequently during the course of project development, I have to talk with PLL designers.

Q. Did you discuss with them about what's inside a PLL?

MR. CHU: Objection; vague as to which PLL.

MR. DAMSTEDT: Vague and ambiguous as to which time you're talking about.

Are you talking about during his job or during preparation for the deposition?

MR. PHAM: During his job.

THE WITNESS: Yes. The type -- the type of questions we -- I ask them is not what's inside.

A lot of times the data sheets are outdated, so it's -- talk about -- is the frequency range, this is just what I'm thinking, between whatever, 300 to 1.5 speed? Is it for the speeds that I'm using? Am I using the correct settings of the PLL?

So, you know, I don't -- I don't attend design reviews or technical design reviews that they do. They have -- again, it's a separate team.

My questions usually and most -- most of the time is to call them directly and ask about the stuff I need, which is range and, you know, settings. "Well, I have a data converter. Should I use this PLL for it or the other one as a" -- you know.

So if -- to give you an idea, I'm supplying clocks across the board in the chip, which has completely different functional clocks. And some of these PLLs are high performance, some of them are low power.

So my thought is just to do due diligence to make sure I have the right selection for the particular application in the chip. That's the type of communication I do with them, and it's quite often during the course of development of the project.

BY MR. PHAM:

Q. So if you want to know what's inside a PLL, you still have to talk to the designers?

A. Yes. But I really do not have time or bandwidth to -- to get inside this. They're -- again, I'm the user. I'm not interested in what's inside that circuit.

There are a lot of analog macros that are used in the clock control, so -- I wouldn't -- I'm not an expert in or interested to know what's inside each one of them, simply because of the schedules and pressure.

Q. If designers are not available to answer questions about inside of a PLL --

A. Uh-huh.

Q. -- would you refer to these documents?

A. I refer --

MR. CHU: Objection; it calls for speculation.

THE WITNESS: I refer to documents. But I ping and ping until I find one of them.

Again, the document might not necessarily tell the whole story, and I cannot rely on -- I would rather rely on people I've worked with over time we have developed a relationship and get the data directly from -- from them.

BY MR. PHAM:

Q. Why do -- why does Qualcomm create these PLL data sheets?

A. To provide technical information about the PLLs.

Q. To who?

A. To internal and external customers. I'm an internal customer.

Q. The external customer, they don't have the access to the designers as you do, do they?

A. They do not have to do what I have to do. I have to ensure what goes on the silicone, on the integrated circuit is the correct selection.

By the time customers get the whole integrated circuit, that selection has already been made for them by someone like me. So they do not have to make a selection. All they need to do is program it.

And for the most part, we provide, you know, the specific settings of the PLL to customers. I mean, we provide it in the form of software that we deliver with the chip, at least in new era, in the past three or four years. I do not know what it was ten years ago.

Q. Does customers -- do customers rely on the PLL data sheet for anything?

MR. WALKER: Objection.

MR. CHU: Objection; vague, it calls for speculation, lack of foundation.

THE WITNESS: I can only talk about past four or five years and my experiences. So there is a clock software team which does PLL programming, clock settings, et cetera.

That software is the one that gets transferred to our customers as a platform -- as a base platform. They could modify things, but normally they would not modify clock settings.

BY MR. PHAM:

Q. If there's an error in the PLL data sheet, would Qualcomm correct those errors?

A. Absolutely. And it has -- PLLs are sensitive circuits and from time to time errors happen. Data sheets gets revved up all the time.

And, you know, we get production devices or silicone and cross corners. You know, process has corners. Not all physical chips are identical in one particular process for the same chip.

So one of the activities that we do within Qualcomm is to try to look across the process variation for the same particular chip, same particular PLLs, and ensure that on every corner this PLL hits the target that it's supposed to hit for that particular product.

So then in the course of that activity, we come across a situation, you know, that need technical modification. Sometimes even revving up the chip, changing hardware.

BY MR. PHAM:

Q. What do you mean by revving the chip?

A. Revving the chip meaning making design changes in the chip and sending it to production again.

Q. Let me refer you back to page 15 of -- page 15 of the MSM8x55 user guide --

A. Yes.

Q. -- which is Exhibit 7.

(Witness complies.)

BY MR. PHAM:

Q. Are there on chip input/output interfaces?

MR. CHU: Objection; it calls for legal conclusion, vague, and it lacks foundation.

concludes today's deposition of Sina Dena. We're off the record at 5:22 p.m.

(The deposition proceedings were concluded at 5:22 p.m.)

-0o0-

STATE OF CALIFORNIA)
) ss.
COUNTY OF LOS ANGELES)

I, SINA DENA, having appeared for my deposition on February 7, 2013, do this date state that I have read the foregoing deposition and that I have made any corrections, additions, or deletions that I was desirous of making in order to render the within transcript true and correct.

IN WITNESS WHEREOF, I have hereunto subscribed my name this ______ day of ____________________, 2013.

____
SINA DENA

DEPONENT'S CHANGES OR CORRECTIONS

Note: If you are adding to your testimony, print the exact words you want to add. If you are deleting from your testimony, print the exact words you want to delete. Specify with "add" or "delete" and sign this form.

DEPOSITION OF: SINA DENA
CASE: HTC CORPORATION, ET AL. V. TECHNOLOGY PROPERTIES LIMITED, ET AL., AND RELATED CASES
DATE OF DEPOSITION: FEBRUARY 7, 2013

PAGE LINE CHANGE/ADD/DELETE

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Deponent's Signature Date

STATE OF CALIFORNIA)
) ss.
COUNTY OF LOS ANGELES)

I, DORIEN SAITO, CSR 12568, CLR, a Certified Shorthand Reporter in and for the State of California, County of Los Angeles, do hereby certify;

That SINA DENA, the witness named in the foregoing deposition, was, before the commencement of the deposition, duly administered an oath in accordance with CCP 2094;

That said deposition was taken down in stenograph writing by me and thereafter transcribed into typewriting under my direction.

I further certify that I am neither counsel for nor related to any party to said action, nor in any way interested in the outcome thereof.

Dated this 20th day of February, 2013.

____

CERTIFIED SHORTHAND REPORTER

IN AND FOR THE COUNTY OF

LOS ANGELES, STATE OF CALIFORNIA

STATE OF CALIFORNIA)
) ss.
COUNTY OF LOS ANGELES)

I, DORIEN SAITO, CSR 12568, CLR, a Certified Shorthand Reporter, hereby certify that the attached transcript is a correct copy of the original transcript of the testimony of SINA DENA, taken before me on the 7th day of February, 2013, as thereon stated.

I declare under penalty of perjury that the foregoing is true and correct.

Executed at Los Angeles, California, this 20th day of February, 2013.

____

CERTIFIED SHORTHAND REPORTER
IN AND FOR THE COUNTY OF
LOS ANGELES, STATE OF CALIFORNIA

EXHIBIT L
To Omnibus Declaration of Irvin E. Tyan ISO Defendants' Opposition to Acer and HTC's Motions for Summary Judgment

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA, SAN JOSE DIVISION

____

HTC CORPORATION and HTC)
AMERICA, INC., et al.,)
Plaintiffs,)
vs.) No. 3:08-cv-00882PSG
TECHNOLOGY PROPERTIES LIMITED,)
PATRIOT SCIENTIFIC)
CORPORATION and ALLIACENSE)
LIMITED,)
Defendants.)
______________________________)

ATTORNEYS' EYES ONLY

QUALCOMM CONFIDENTIAL

QUALCOMM ATTORNEYS' EYES ONLY

VIDEOTAPED DEPOSITION OF THOMAS A. GAFFORD

Monday, July 8, 2013

Palo Alto, California

Reported by:

Hanna Kim, CLR, CSR No. 13083

Monday, July 8, 2013

9:37 a.m. - 6:57 p.m.

VIDEOTAPED DEPOSITION OF THOMAS A. GAFFORD, taken on behalf of Technology Properties Limited, on Monday, July 8, 2013, beginning at 9:37 a.m. and ending at 6:57 p.m. at Cooley LLP, 3175 Hanover Street, Palo Alto, California 94304, before Hanna Kim, CLR, CSR No. 13083.

APPEARANCES OF COUNSEL:

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Also Present:

SEAN GRANT, Videographer

INDEX OF EXAMINATION

WITNESS: THOMAS A. GAFFORD

crystal to vary to which it's clocked.

Q. That variation needs to be multiplied by 32 to get variation of the actual frequency output of the PLL, right?

MR. CHEN: Vague.

THE WITNESS: The -- not -- again, if you're measuring variation in parts per million, it wouldn't matter where you measure it or how you divide it. The ratio in parts per million is the same.

BY MR. PHAM:

Q. What is the degree of the variation of the M clock according to temperature?

A. As it states here, plus or minus 4.3 parts per million over the temperature range.

Q. Within the PLL, there's an oscillator, right?

A. Yes.

Q. But you could not have measured the frequency output of the oscillator itself?

A. Directly, the oscillator as oscillating at 768 megahertz? No. As I said, I don't believe that signal is supplied to any pin coming out of the -- any pin provided on the chip. I have instead measured its -- measured something that is 1/32 of that frequency -- I'm sorry. One -- yes, 1/32 to that frequency.

Q. The frequency output of the oscillator within the PLL varies with temperature, right?
A. Yes. It varies exactly in accordance with the variance of the reference frequency, as I've shown in the later figure here.
Q. You need the PLL to compare the output of the oscillator with the reference frequency in order to adjust the frequency output of the oscillator?
A. Well, part of what the phase lock loop does is it has a phase frequency detector that compares the frequency of the oscillator that -- of the controlled oscillator with the frequency of the reference oscillator.
Q. And the purpose of the comparison is to adjust the frequency of the control oscillator?
A. Actually, it's more like adjust the -- adjust the parameters of the -- of the controlled oscillator so that it doesn't vary in frequency, would be a better way to say it.
Q. Without that adjustment, the oscillator frequency will continue to depart from the reference frequency?
A. I don't know what it will do, because all I've ever looked at is working PLLs where the adjustment's always made.

Q. And the reason for the adjustment is because the frequency of the oscillator varies with temperature?

A. It is --

MR. CHEN: Vague.

THE WITNESS: It's more -- it's -- that's not quite a correct statement. The characteristics of the transistors in the oscillator vary with temperature. And in order to provide a constant frequency for clocking the processor, or at least as constant as a crystal can make it, the PLL develops a controlled voltage to prevent variation to keep it locked to the crystal.

BY MR. PHAM:

Q. If the PLL does not keep it locked, then it would vary?

A. If the PLL does not keep it locked, I don't think you have a working phone.

Q. But because the frequency oscillator -- strike that.

Because the frequency of the oscillator will vary widely, right?

A. The word "vary" -- if -- if there were no PLL, if the clock generator was -- if -- if the -- hmm.

If you didn't operate the control voltage the way it's operated in the accused devices, then you would no longer be -- you would no longer be immune to variations in temperature processor voltage.

Q. Let me direct you to Figure 10 on page 72. You see the ICL block in that figure?

A. I see a block that doesn't have that label, but it has three sine waves in it. Is that the one you mean?

Q. Yeah.

Is there a current input into that block?

A. Yes.

Q. Is the current input used to control the block in a way that the frequency output of the block will not vary too much?

A. Well, precisely so that it won't vary any more than the reference frequency varies, which isn't much. The reference frequency varies in accordance to what you'd expect from a very good crystal.

Q. You do that by adjusting the current input into the ICL block?

MR. CHEN: Vague.

THE WITNESS: Yes, that -- the current input that comes from either -- any one of these three V2I blocks goes into the ICL block to a selected one of these. I believe this is attempt -- I believe this is showing three different oscillators, and to whichever one is operating, it controls the gain and thus speed -- gain -- it controls the characteristics of the transistors in the oscillator so that the output frequency remains constant.

BY MR. PHAM:

Q. If you keep the current input into the ICL block constant, would the frequency output of the ICL block vary more with PVT?

MR. CHEN: Vague.

THE WITNESS: More than what?

BY MR. PHAM:

Q. More than in a normal case where the current input is used to control the ICL block.

A. You mean in a case of how the chips are designed and shipped by the -- by HTC?

Q. Yes.

A. Probably. How much, I don't know, but stands to reason if you stop correcting the thing that's supposed to be corrected, that there will be some variance due to PVT.

Q. During normal operation, the processing frequency of CPU varies accordingly with the output frequency of the oscillator that clocks it, right?

A. I have no idea what you're talking about. Are

you talking about the Accused Devices?
Q. Yes.
A. And what do you mean by processing frequency? I understand the phrase "current processing frequency capability," but I'm not certain I understand what you mean by processing frequency.
Q. You understand the phrase "processing frequency capability" and the phrase "actual processing frequency of a CPU"?
A. If by processing frequency -- if we're talking about claim terms now, perhaps I should have the patent in front of me. I do have the patent. Oh, good.
Why don't you point me to the claim term you're talking about. And if it's not a claim term, point me to something.
Q. Let's look at Claim 6. You see the phrase "central processing unit operating at a processing frequency"?
A. Yes. Whatever its -- whatever rate it is being driven by its clock is the processing frequency in this phrase.
Q. Does that processing frequency vary according to the frequency of the clock?
A. It is exactly the frequency of the clock. It has -- that's what processing frequency means. And the

clock in normal operation in Accused Devices doesn't vary.

Q. Is the variation in frequency output of an oscillator the same as jitter?

MR. CHEN: Vague.

THE WITNESS: Jitter and frequency variation are not the same thing. You can express the effect of jitter in the frequency domain, but jitter is an error or is a variation in, let's say, the location of a rising or falling edge in a signal, and you can have a variation in a rising or falling edge of a signal and have no variation in its period, conceivably. So you have jitter without frequency variation.

BY MR. PHAM:

Q. Does jitter decrease as temperature increases?

A. Jitter comes -- can come from a lot of sources. I think it's a very complex relationship. One source of jitter that I'm aware of is thermal noise, and thermal noise increases with temperature. So if you have a circuit whose output is jittering because of thermal noise, then that jitter might decrease with a -- with an increase in temperature, just a -- just as a theoretical circuit design matter.

Q. Is manufacturing variation permanent?

A. Permanent?

Q. Yes.
MR. CHEN: Vague.
THE WITNESS: Permanent over what? Permanent in response to what?
BY MR. PHAM:
Q. It is satisfactory by.
A. Well, you build what you build and you ship what you build. The -- I suppose in that sense, process variation stops when the process stops, is probably the simplest way to look at it.
Q. Does process variation affect processing frequency of a CPU?
MR. CHEN: Vague.
THE WITNESS: Not in the sense that we've just described it, where the processing frequency is the frequency at which the CPU is being clocked. And in the Accused Devices, that frequency doesn't vary. So the effect of processing variations will have no impact on the frequency at which the CPU is being clocked.
BY MR. PHAM:
Q. Because PLL controls the frequency?
A. Yes, because processing frequency is the frequency at which it is processing at the moment, driven by the PLL, yes.
Q. Does manufacturing variation affect the

processing frequency capability of a CPU?
A. It can.
Q. And that's why you have a binning step in manufacturing chips, right?
MR. CHEN: Vague.
THE WITNESS: To the -- I don't know exactly what you mean by binning, but I'll tell you the -- the binning that I understand. To the extent that you have a silicon component that is rated to a certain capability, and from the same process other components are rated differently, that's binning. That tells you that the maximum capability of the products of a particular manufacturing process vary, and we charge more for the good ones and less for the bad ones, or the slower ones in that case. But all that affects is -- is the fastest -- and typically, binning and things like -- well, thinking of old memory chips, for example. But binning is typically a difference in maximum performance.
BY MR. PHAM:
Q. And the differences in maximum performance is due to process variation?
A. That's what we've been talking about. It can be due to process variations.
Q. Is that the case in chips that are in the

HTC's Accused Products?
A. I don't believe so, because my understanding of the chips in all the HTC Accused Products is that for a particular product, all the phones have the same -- all the devices have the same performance specification. So whether there is any binning going on in the selecting of the system shifts for those or not doesn't matter because they're all clocked at the same rate.
So the whole point is -- of -- of this design is, you provide a clock signal -- clock frequency to the CPU that all CPUs that you will ever assemble in that unit can execute without error over the specified range of environmental conditions.
Q. Do all the chips in the HTC Accused Products have the same processing frequency capability?
A. I don't know. They are not ever clocked in use. They are never clocked as a shipped product at their -- at their capability. That would be -- at least not the way HTC ships them.
Q. So you don't know the processing frequency capability of the chips in HTC Accused Products?
A. I -- pardon me.
I know that it is sufficient to meet the specification of the product under worse-case

CERTIFICATE OF REPORTER

I, Hanna Kim, a Certified Shorthand Reporter, do hereby certify:

That prior to being examined, the witness in the foregoing proceedings was by me duly sworn to testify to the truth, the whole truth, and nothing but the truth;

That said proceedings were taken before me at the time and place therein set forth and were taken down by me in shorthand and thereafter transcribed into typewriting under my direction and supervision;

I further certify that I am neither counsel for, nor related to, any party to said proceedings, not in anywise interested in the outcome thereof.

In witness whereof, I have hereunto subscribed my name.

Dated: ____ day of ___________, 2013

____

Hanna Kim

CLR, CSR No. 13083

ERRATA SHEET FOR THE TRANSCRIPT OF:

Case Name: HTC, et al. vs. TPL, et al.

Dep. Date: July 8, 2013

Deponent: Expert Deposition, Thomas A. Gafford

CORRECTIONS:

Pg.	Ln.	Now Reads	Should Read	Reason
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Signature of Deponent

SUBSCRIBED AND SWORN BEFORE ME

THIS____DAY OF___________, 2013.

____

(Notary Public) MY COMMISSION EXPIRES:_______________

EXHIBIT R
To Omnibus Declaration of Irvin E. Tyan ISO Defendants' Opposition to Acer and HTC's Motions for Summary Judgment

In The Matter Of:

ACER, INC., et al.
v.
TECHNOLOGY PROPERTIES LTD., et al.

HTC CORPORATION, et al.
v.
TECHNOLOGY PROPERTIES LTD., et al.

VOJIN OKLOBDZIJA - Vol. 2

July 15, 2013

HIGHLY CONFIDENTIAL PURSUANT TO PROTECTIVE ORDER

MERRILL CORPORATION
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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION, and GATEWAY, INC.,

Plaintiffs,

-vs- No. 5:08-cv-00877 PSG

TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORPORATION & ALLIACENSE LIMITED,

Defendants.
/

HTC CORPORATION and HTC AMERICA, INC.,

Plaintiffs,

-vs- No. 5:08-cv-0882 PSG

TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORPORATION & ALLIACENSE LIMITED,

Defendants.
/

VIDEOTAPED DEPOSITION OF

VOJIN OKLOBDZIJA

July 15, 2013

Volume II, Pages 198 - 431

HIGHLY CONFIDENTIAL - PURSUANT TO PROTECTIVE ORDER

Reported by: WENDY E. ARLEN, CSR #4355, RMR, CRR

Job No: 2001-452355

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Deposition of VOJIN OKLOBDZIJA, taken by the plaintiffs, at AGILITY IP LAW, LLP, 149 Commonwealth Drive, Menlo Park, California, commencing at 9:06 a.m., Monday, July 15, 2013 before me, WENDY E. ARLEN, CSR, RMR, CRR.

A P P E A R A N C E S

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APPEARANCES (Cont'd)

ALSO PRESENT:

Jefree Anderson, Videographer

--oOo--

Menlo Park, California
Monday, July 15, 2013
9:06 a.m. 08:10:38

VIDEOGRAPHER: Here begins Volume II, videotape number one in the deposition of Dr. Vojin Oklobdzija in the matter of Acer, Incorporated, et al., versus Technology Properties Ltd., et al., case number 5:08-cv-00877, and HTC Corp, et al., versus Technology Properties Ltd., et al., case number 5:08-cv-00882 in United States District Court, Northern District of California, San Jose Division. 09:04:29 09:05:04 09:05:08 09:05:14 09:05:19 09:05:27 09:05:31 09:05:37

Today's date is July 15th, 2013. The time on the video monitor is 9:06 a.m. The video operator today is Jefree Anderson, a notary public contracted by Merrill Court Reporting, San Francisco, California. This video deposition is taking place at Agility IP Law in Menlo Park, California. 09:05:38 09:05:46 09:05:50 09:05:54 09:05:56 09:06:00

And I believe all the parties that were here last session are here today. Is there anyone new? 09:06:05 09:06:07

And the witness has been sworn in. So please begin. 09:06:12 09:06:18

EXAMINATION BY MR. WALKER 09:06:19

Q. Good morning, Dr. Oklobdzija. 09:06:20
A. Good morning. 09:06:22
Q. You mentioned that the -- at least some of 09:06:23

oscillator. Maybe there is some idiosynchronous like Talbot that is not which is used in computer long time ago, but as we have seen from the literature and from the analysis of all the data available, they are -- invariably they're all ring oscillator. And ring oscillator by nature would vary with the environmental operational parameters. So they contain something that is variable. 09:42:06 09:42:15 09:42:19 09:42:22 09:42:26 09:42:30 09:42:34 09:42:39

A PLL is using that variability basically to its own advantage when it is running faster than the reference, tries to slow it down. When it is running slower, tries to speed it up. So it has a variable -- variable speed clock. 09:42:45 09:42:47 09:42:51 09:42:56 09:43:00

Q. So in your infringement analysis, the variable speed clock is actually the ring oscillator within the PLL; is that correct? 09:43:01 09:43:05 09:43:09

A. Okay. In my infringement analysis, the variable speed clock is the ring oscillator within the PLL, correct. 09:43:10 09:43:15 09:43:19

Q. Is the output of the PLL variable speed frequency? 09:43:20 09:43:34

A. The output of a PLL -- we have been debating that. The output of the PLL is, depending on your magnifying glass, is -- is not fixed. The output of PLL varies. 09:43:34 09:43:42 09:43:48 09:43:52

Q. Then how do you know that there is any variation of the PLL output as a function of temperature? 10:01:02 10:01:12 10:01:18
A. Because all the PLL's are pretty much made a similar way and behave in -- in a known similar ways, and I think going from one design to another design you will find maybe differences to the degree to which varies, but they all are affected by voltage and temperature. 10:01:18 10:01:33 10:01:40 10:01:44 10:01:47 10:01:53
Q. For any of the Acer accused products, did you see a specification for a PLL that describes the PLL output as varying with temperature? 10:01:54 10:02:03 10:02:09
A. As I said, I think we had the very little specification of Acer products. I mean, what I had is basically what you can find on the Web, and they don't talk about that. 10:02:12 10:02:23 10:02:25 10:02:29
Q. Do you have any -- did you see any specification for any of the accused Acer products that describes a variation in the PLL output as a function of operating voltage? 10:02:30 10:02:37 10:02:41 10:02:46
A. I don't think they were available. So I haven't. 10:02:49 10:02:53
Q. Does your infringement analysis depend in any way on how a PLL output varies with operating voltage? 10:02:54 10:03:11 10:03:20

A. To some degree, yes. To some degree. 10:03:20
Q. Explain how, to what degree. 10:03:27
A. Well, if you look at the structure of a PLL and if the operating voltage raises, the VCO or ICO within the PLL will -- the frequency of VCO or ICO within the PLL will increase. 10:03:29 10:03:35 10:03:42 10:03:48
Now, as I think I testified before and I think I have also seen in your experts' reports that the PLL has what is called the dead band. There is a range of frequency around the center frequency where PLL is not able to -- to correct the variations. So basically it is out of luck. 10:03:50 10:03:53 10:03:58 10:04:04 10:04:09 10:04:14
So in that range if the voltage raises, the VCO would naturally increase the frequency. So my analysis based on the structure of the PLL, as I said, in the absence of any specific document describing that PLL that was used in that LSI product. 10:04:18 10:04:24 10:04:29 10:04:36 10:04:38 10:04:43
Q. Do all PLL's vary their frequency output as a function of operating voltage in exactly the same way? 10:04:46 10:04:59 10:05:04
A. Yes, they do. And basically proportional. If you increase the voltage or if you increase -- or decrease the temperature, the frequency has tendency to rise. And depending how -- how well PLL is 10:05:04 10:05:14 10:05:18 10:05:22

designed to control that -- that frequency, it may be small. You know, I can cite the example of -- of your expert Subramanian measurements, and when we look at the numbers and we magnify them, we show the clear trend to -- to go up with voltage and down with temperature. Small, but if you put it under bigger magnifying glass, you'll find it. 10:05:26 10:05:34 10:05:38 10:05:44 10:05:50 10:05:56 10:06:01

Q. Is it your view that any change in PLL output frequency is a -- due to a change in operating voltage meets the claim requirement no matter how small it is? 10:06:03 10:06:07 10:06:19 10:06:27

A. I think there are a couple of things there, you know. And we are still on claim 1. Okay. Haven't moved. But the processing does because different chips are running at a different processing capabilities. 10:06:28 10:06:33 10:06:37 10:06:52 10:06:57

Now, the claim is -- I mean, at this point I would say I would probably leave it, you know, for the legal arguments or the interpretation and I just am a technical expert. I mean, there can be an argument made over what a PLL does to VCO. 10:06:59 10:07:04 10:07:09 10:07:23 10:07:26

But as far as technical expert, I can just say, yes, it does make -- for example, even your -- your expert compares it to the cruise control, and we know that cruise control tries to keep you at the 10:07:34 10:07:38 10:07:42 10:07:47

your experts, et cetera. 18:59:49
Q. With respect to HTC products. 18:59:52
A. With respect to jitter. 18:59:54
Q. No, in the context of HTC products. 18:59:55
A. I don't know if they are talking about HTC products. 19:00:00 19:00:03
Q. No. No. Right now, I'm just asking you in the context of HTC products, did you consider jitter to be part of the variability that you're analyzing? 19:00:03 19:00:07 19:00:11
A. As I said before, I don't. You know, I consider jitter to be a temporal -- a random variable. 19:00:17 19:00:19 19:00:29
Q. I see. Okay. 19:00:29
A. So we are looking at systematic variations, not random variations. 19:00:31 19:00:34
Q. So -- so -- 19:00:36
A. And basically if you measure just as in the measures performed by Subramanian he has measured that point about a thousand times before he averages what the frequency is and then he moves to another one and gets a thousand points average and then to what the frequency is. 19:00:38 19:00:40 19:00:43 19:00:46 19:00:49 19:00:51
But when I see that those are moving away from each other, then I see systematic variability. 19:00:53 19:00:56
Q. But the jitter -- 19:00:59

A. Those may have gone like this and he has averaged them on -- on one value, which is the average value. So -- 19:01:01 19:01:04 19:01:06
Q. So jitters are not part -- 19:01:08
A. I don't consider jitter, no. 19:01:10
(Discussion off the record.) 19:01:26
Q. MR. CHEN: So in terms of variability, I'm still a little bit confused. So, like, say for example, what kind of variability in the PLL's or VCOs or ICO's in accused HTC product would be considered by you to be the kind of variability in the clock or oscillator as claimed in the '336 patent? 19:01:27 19:01:33 19:01:38 19:01:41 19:01:47 19:01:50 19:01:53
A. Well, if I have a system in which the clock is trapped inside the PLL, basically controlled by the PLL, the only freedom it has it's when PLL is basically disabled and that is that dead band. And -- and any systematic variability in that band. Because it's obviously -- let's say if we had -- and I think those Subramanian measurements were quite instructive, but when we -- when we blew them up, we saw how these numbers go basically like on the line and I think at some point they hit that band of the PLL and they go back. 19:01:53 19:02:01 19:02:07 19:02:13 19:02:19 19:02:24 19:02:27 19:02:32 19:02:36 19:02:39 19:02:42
Q. So you're saying the kind of microscopic 19:02:44

variations are the variations that you're using? 19:02:49
MR. OTTESON: Objection, mischaracterizes. 19:02:52
THE WITNESS: I would characterize them as -- I just forget now. I would characterize them as within the degree of freedom that it has. 19:02:54 19:02:58 19:03:06
Q. MR. CHEN: As defined by the phase-locked loop? 19:03:10 19:03:12
A. In the -- in the -- let's say if you're holding something, you know, but not too tight. So it has some loose movements. So within -- which is a freedom. Obviously it's constrained further than that. 19:03:12 19:03:17 19:03:21 19:03:28 19:03:31
So I would say within the -- within the range of freedom or degree of freedom that -- that it has. 19:03:32 19:03:36
Q. Okay. I just have a couple quick questions about Exhibit 4. Do you have Exhibit 4? 19:03:41 19:03:43
A. Okay. Let's make those last. 19:03:45
MR. OTTESON: You spent a lot of time talking about this yesterday. So I think you're kind of wearing out your welcome here. 19:03:59 19:04:01 19:04:03
THE WITNESS: How are we doing on tape? 19:04:05
MR. OTTESON: He started a new tape. 19:04:09
VIDEOGRAPHER: We have 16 more minutes to go. 19:04:12
Q. MR. CHEN: So could you go to column 42, line 18. Line 18. It says: "This timer mode can be used 19:04:17 19:04:24

minutes, right? 19:08:28

MR. CHEN: We'll see -- we'll see what will be required and then we can talk. 19:08:29 19:08:32

VIDEOGRAPHER: Okay, the marks the end of tape number five in the deposition of Dr. Oklobdzija. Going off the record, the time is 7:09. 19:08:34 19:08:36 19:08:40

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(Whereupon, the deposition was adjourned at deposition adjourned at 7:09 p.m.)

--o0o--

I declare under penalty of perjury that the foregoing is true and correct. Subscribed at ______________, California, this ____ day of ____________, 2013.

____

Signature of Witness

CERTIFICATE OF REPORTER

I, WENDY E. ARLEN, a Certified Shorthand Reporter, hereby certify that the witness in the foregoing deposition was by me duly sworn to tell the truth, the whole truth and nothing but the truth in the within-entitled cause;

That said deposition was taken down in shorthand by me, a disinterested person, at the time and place therein stated, and that the testimony of the said witness was thereafter reduced to typewriting, by computer, under my direction and supervision.

That before completion of the deposition, review of the transcript was not requested. If requested, any changes made by the deponent (and provided to the reporter) during the period allowed are appended hereto.

I further certify that I am not of counsel or attorney for either or any of the parties to the said deposition nor in any way interested in the event of this cause and that I am not related to any of the parties thereto.

DATED:______________________, 2013

____

WENDY E. ARLEN CSR, No. 4355