[See Signature Page for Information on Counsel for Plaintiffs]

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00877 PSG **PLAINTIFFS' CONSOLIDATED RESPONSIVE SUPPLEMENTAL CLAIM CONSTRUCTION BRIEF** **[RELATED CASES]** Date: November 30, 2012 Time: 10:00 a.m. Place: Courtroom 5, 4th Floor Judge: Paul Singh Grewal
HTC CORPORATION and HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00882 PSG
BARCO N.V., a Belgian corporation, Plaintiff, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-05398 PSG

TABLE OF CONTENTS

TABLE OF AUTHORITIES

Page(s)

CASES

STATUTES

TABLE OF ABBREVIATIONS

’148 patent or ’148	U.S. Patent No. 6,598,148, entitled “High Performance Microprocessor Having Variable Speed System Clock,” issued July 22, 2003
’336 patent or ’336	U.S. Patent No. 5,809,336, entitled “High Performance Microprocessor Having Variable Speed System Clock,” issued September 15, 1998
’749 patent or ’749	U.S. Patent No. 5,440,749, entitled “High Performance, Low Cost Microprocessor Architecture,” issued August 8, 1995
’890 patent or ’890	U.S. Patent No. 5,530,890, entitled “High Performance, Low Cost Microprocessor,” issued June 25, 1996
Plaintiffs	Declaratory judgment plaintiffs Acer, Inc., Acer America Corporation, Barco, N.V., Gateway, Inc., HTC Corporation and HTC America, Inc.
Defendants or TPL	Declaratory judgment defendants Technology Properties Limited, Patriot Scientific Corporation and Alliacense Limited
Acer Action	*Acer, Inc., Acer America Corporation and Gateway, Inc. v. Technology Properties Limited, Patriot Scientific Corporation, and Alliacense Limited*, Civil Case No. 5:08-cv-00877 PSG
Chen Decl.	Declaration of Kyle D. Chen in Support of Plaintiffs’ Opening Supplemental Claim Construction Brief (Dkt. No. 363 in *Acer* Action)
Talbot	U.S. Patent No. 4,689,581, entitled “Integrated Circuit Phase Locked Loop Timing Apparatus,” issued August 25, 1987 to Gerald R. Talbot, Attached as Exhibit 9 to Chen Declaration (Dkt. No. 363-9 in *Acer* Action)

I. INTRODUCTION

Declaratory judgment plaintiffs Acer, HTC and Barco entities, as shown on the caption page (collectively "Plaintiffs"), respectfully and jointly submit this Consolidated Responsive Supplemental Claim Construction Brief as ordered by the Court.

II. THE CLAIMED "RING OSCILLATOR" MUST BE NON-CONTROLLABLE AND VARIABLE BASED ON ENVIRONMENTAL PARAMETERS.

For the sake of convenience, the parties' competing constructions of "ring oscillator" are again set forth below:

Plaintiffs' Construction	TPL's Construction
An oscillator having a multiple, odd number of inversions arranged in a loop, **wherein the oscillator is: (1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters in the environment**	An oscillator having a multiple, odd number of inversions arranged in a loop

Defendants' Opening Supplemental Claim Construction Brief (*Acer* Action, Dkt. No. 357 ("TPL's Op. Supp. Br.")) fails to demonstrate how TPL's proposed construction of "ring oscillator" avoids reading on the voltage-controlled oscillator in Talbot Figure 3 that has been indisputably disclaimed. Instead, TPL argues without citing any authority that Judge Ware's First Claim Construction Order (*Acer* Action, Dkt. No. 336 ("Order")) is improper because, in TPL's view, whether Talbot discloses a "ring oscillator" "is not an appropriate subject for claim construction." (TPL's Op. Supp. Br. at 10.) The declaration of Dr. Oklobdzija submitted in support of TPL's supplemental briefing does not even analyze Talbot Figure 3 and does not address either party's proposed construction. (*See* "SUPPLAMENTAL [sic] DECLARATION OF DR. VOJIN OKLOBDZIJA," *Acer* Action, Dkt. 357-4 ("Supp. Oklobdzija Decl.").) Instead, Dr. Oklobdzija's declaration analyzes a hypothetical circuit that even he admits is not Talbot and is not at issue, and applies a new definition of "ring oscillator" that is not supported by any intrinsic evidence. (Oklobdzija 10/12/12 Dep. at 609:4-12, 610:1-10 and Ex. 77, 406:11–407:14 (Supplemental Declaration of Kyle D. Chen filed herewith ("Chen Supp. Decl."), Exs. 24 and 77).)

While Plaintiffs' proposed construction is supported by the intrinsic record, TPL asserts new distinctions between Talbot Figure 3 and the claimed "ring oscillator" based on a distorted

explanation of a Schmitt-trigger, distinctions that are unsupported by either the '336 specification or the prosecution history. TPL's positions are contradicted by Talbot, contradicted by a textbook written by Dr. Oklobdzija himself, and contradicted by Exhibit A to Dr. Oklobdzija's supplemental declaration.

A. Judge Ware Did Not Construe the Claimed "Ring Oscillator."

TPL misrepresents Judge Ware's Order, suggesting that Judge Ware has already construed "ring oscillator" in the patents-in-suit. To the contrary, this supplemental briefing was ordered by Judge Ware to determine the proper construction of the claimed "ring oscillator." (*See* Order at 16:14–15 ("Here, ***before*** arriving at a decision on the definition of the phrase "ring oscillator" in the context of the Talbot reference, the Court finds that it would benefit from further briefing.") (emphasis added).) Judge Ware sought supplemental declarations and briefing on "ring oscillator" because he understood the significance of Plaintiffs' proof that Talbot Figure 3 discloses three inverters arranged in a loop. The voltage-controlled oscillator in Talbot Figure 3 meets both TPL's proposed construction of "ring oscillator" as well as what Judge Ware finds one of ordinary skill would normally understand a "ring oscillator" to be without specialized meaning. (Order at 13:20–22 and 16:1–6.)

TPL's explanation of the operation of the "ring oscillator" disclosed by Figure 18 of the '336 patent applies as well to the indisputably disclaimed voltage-controlled oscillator in Talbot Figure 3 because it too has an odd number of inverters. Because Talbot has three inverters arranged in a loop, the claimed "ring oscillator" requires a specialized meaning to avoid reading on the disclaimed voltage-controlled oscillator in Talbot Figure 3.

TPL asks this Court to simply ignore the patent owner's arguments made to the Examiner during an interview, even though TPL has never challenged the accuracy of the Examiner's interview summary. TPL fails to even address similar characterizations of the claimed ring oscillator during prosecution of the '336 patent to distinguish the Magar and Sheets references, set forth in detail in Plaintiffs' Opening Supplemental Claim Construction Brief (*Acer* Action, Dkt. No. 365 ("Plaintiffs' Op. Supp. Br.")). But these disclaimers cannot be ignored. They are as

much a part of the prosecution history as the final '148 reexamination amendment that TPL characterizes as the most important.

Further, the patent owner's argument in that '148 reexamination amendment is also a disclaimer of voltage-controlled oscillators generally:

> Further, **Talbot does not teach, disclose, or suggest the ring oscillator** recited in claim 4. The examiner cited col.3, ll. 26-35, and oscillator circuit 12 shown in FIG. 1 of Talbot as teaching the recited ring oscillator. **Talbot discusses a voltage-controlled oscillator (VCO) 12, but does not teach or disclose a ring oscillator.**

('148 PH Remarks/Arguments at 11, 2/21/08 (Chen Decl., Ex. 3) (emphasis added).)

Plaintiffs' proposed construction properly holds TPL to all of its disclaimers, including the final disclaimer of voltage-controlled oscillators. TPL's proposed construction must be rejected because it fails to distinguish Talbot, is contrary to the prosecution history, and is contrary to TPL's arguments to this Court that Talbot does not disclose a "ring oscillator."

B. The Patent Owner's Arguments Recorded in Examiner's Interview Summary Constitute a Clear Disavowal of Scope for the Claimed "Ring Oscillator."

In both the prosecution history and the current briefing, TPL clearly disavows the voltage-controlled oscillator in Talbot. For that reason alone, both TPL's proposed construction and the ordinary meaning that a ring oscillator comprises nothing more than three "inversions" or "inverters" arranged in a loop must be rejected. The reason is that Talbot discloses an oscillator comprising three inverters arranged in a loop and also three inversions in a loop.

Plaintiffs' proposed construction simply includes in the "ring oscillator" the very distinction argued by TPL to the Patent Office during the '148 patent's reexamination, as evidenced by the Examiner's February 12, 2008 interview summary. ('148 PH 2/12/08 Interview Summary at 2 (Chen Decl., Ex. 2).) In arguing for patentability over Talbot, TPL failed to present any other substantive distinction between the voltage-controlled oscillator in Talbot and the claimed "ring oscillator," so it would be improper now to tell the public—including Plaintiffs—that "ring oscillator" can be narrowed in some other way to avoid Talbot. Accordingly, new distinctions based on Dr. Oklobdzija's declaration or deposition testimony must be rejected because those new distinctions were not presented to the Examiner as part of the prosecution history, which not only

deprived the public of notice of these new distinctions but also deprived the Examiner of any response to these proposed new distinctions.

TPL argues that black is white by denying that the Examiner's interview summary sets forth a clear disavowal of claim scope. The best rebuttal is to repeat again the language of the summary:

> Continuing, the patent owner further argued that the reference of Talbot does not teach of a "ring oscillator." **The patent owner discussed features of a ring oscillator, such as being non-controllable, and being variable based on the environment**. **The patent owner argued that these features distinguish over what Talbot teaches.** The examiner will reconsider the current rejection based on a forthcoming response, which will include arguments similar to what was discussed.

(*Id.* (emphasis added).)

The Examiner's interview summary is a proper basis for finding a disavowal of claim scope. It expressly reflects what TPL, the patent owner, argued. The Federal Circuit has repeatedly relied upon patent owners' arguments recorded in interview summaries to find that patent owners disavowed claim scope to distinguish prior art. *See, e.g.*, *Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319, 1322 (Fed. Cir. 2002) (disavowal found based on patent owner's arguments that the Examiner recorded in interview summary); *see also Biovail Corp. Int'l v. Andrx Pharms., Inc.*, 239 F.3d 1297, 1302–04 (Fed. Cir. 2001) (same); *Trinity Indus. v. Road Sys.*, 121 F. Supp. 2d 1028, 1044 (E.D. Tex. 2000) ("It is proper to consider the interview summary in claim construction as it is part of the prosecution history.") (citing *Athletic Alternatives, Inc. v. Prince Mfg., Inc.*, 73 F.3d 1573, 1576 (Fed. Cir. 1996) (relying upon Examiner's interview summary of patent owner's statements in claim construction)).

In its opening supplemental papers, TPL cites no legal authority in support of its argument that the Examiner's summary cannot constitute a disavowal of claim scope. In its prior claim construction papers, however, TPL argued that *Salazar v. Procter & Gamble Co.*, 414 F.3d 1342 (Fed. Cir. 2005), applies; but it does not. (*See* Defendants' Opening Claim Construction Brief at 5, *Acer* Action, Dkt. No. 310.) *Salazar* held that "unilateral statements by an examiner" in a Notice of Allowance did not give rise to a disavowal by the patent owner. The statements at issue here were not "unilateral statements" by the Examiner, but arguments made by TPL. The fact that the

Examiner recorded TPL's statements does not change the fact that it was TPL, not the Examiner, who made them.

TPL also previously misapplied *University of Pittsburgh v. Hedrick*, 573 F.3d 1290, 1297 (Fed. Cir. 2009), which refused to give weight to a "terse" and ambiguous interview summary that was unclear concerning which features of the claimed invention, if any, were being distinguished. (*See* Defendants' Opening Claim Construction Brief at 5, *Acer* Action, Dkt. No. 310.) In the present case, however, the Examiner's interview summary could not be more clear: To distinguish Talbot's voltage-controlled oscillator, the "patent owner" argued that "features" of the claimed "ring oscillator" include "being non-controllable, and being variable based on the environment." The accuracy of this record by the Examiner has never been challenged, and the disavowals clearly identify the claim language and the features on which it is distinguished.

TPL boldly asks this Court to ignore the interview summary. (TPL's Op. Supp. Br. at 9:10–12 ("[I]t is far more important to understand what occurred next."). But that would be improper because the Examiner and the public are entitled to rely on the interview summary to understand the scope of the claimed "ring oscillator." Indeed, even if the Examiner did not rely on the interview summary, the public is still entitled to rely on it. *See, e.g., Microsoft Corp. v. Multi-Tech Sys., Inc.*, 357 F.3d 1340, 1350 (Fed. Cir. 2004) ("We have stated on numerous occasions that a patentee's statements during prosecution, whether relied on by the examiner or not, are relevant to claim interpretation.") (citing cases).

If the patent owner disagreed with the Examiner's interview summary, it needed to say so explicitly in the subsequent written amendment, to properly alert both the Examiner and the public. *Hakim v. Cannon Avent Grp., PLC*, 479 F.3d 1313, 1318 (Fed. Cir. 2007) ("Although a disclaimer made during prosecution can be rescinded, permitting recapture of the disclaimed scope, the prosecution history must be sufficiently clear to inform the examiner that the previous disclaimer, and the prior art that it was made to avoid, may need to be re-visited."). Instead of "clearly informing the examiner" that the disclaimer needed to be "revisited," nine days later on February 21, 2008, the patent owner submitted its own "Interview Summary" that did not dispute

anything in the Examiner's interview summary and was entirely consistent with that interview summary. In particular, TPL again clearly disavowed any voltage-**controlled** oscillator disclosed by Talbot: "Talbot discusses a voltage-**controlled** oscillator (VCO) 12, but does not teach or disclose a ring oscillator." ('148 PH 2/21/08 Remarks/Arguments at 11, (Chen Decl., Ex. 3) (emphasis added).) Thus, TPL's summary is most appropriately interpreted as supporting its arguments recorded in the Examiner's summary.

Arguing, contrary to *Microsoft*, that it somehow matters whether the Examiner relied upon what was said at the interview, TPL fails to cite key language in the June 25, 2008 Non-Final Action that tracks the interview summary, thereby indicating that the Examiner was indeed relying on the interview. The June 25, 2008 Non-Final Action states, "Further, the reference of Talbot'518 [sic] describes an oscillator circuit, but the specific ***features*** are unclear if the components actually make a ring oscillator." ('148 PH 6/25/08 Non-Final Action at 5 (Otteson Decl., Ex. 10 at 27 of 63), *Acer* Action, Dkt. No. 357-05 (emphasis added).) The antecedent for the cited "features" is found in the Examiner's interview summary, which says "the patent owner discussed ***features*** **of a ring oscillator, such as being non-controllable, and being variable based on the environment.**" ('148 PH 2/12/08 Interview Summary at 2 (Chen Decl., Ex. 2) (emphasis added).) Thus, the Examiner has clearly relied upon the patent owner's arguments regarding the non-controllable "feature" of the claimed "ring oscillator" made during the interview and reiterated by the subsequent disclaimer of Talbot's voltage-**controlled** oscillator in allowing the claims. Thus, TPL's disclaimers must stand.

C. TPL's Arguments Regarding Whether a Hypothetical Circuit Different from Talbot Would Oscillate Is Irrelevant to What Talbot Discloses.

Judge Ware ordered supplemental expert declarations that should "fully articulate the technical basis for their opinions with respect to whether the voltage-controlled oscillator disclosed in Talbot is or is not a ring oscillator." (Order at 16:16–17.) Answering that question requires a comparison between a definition of "ring oscillator" and the disclosures of Talbot. The Supplemental Wolfe Declaration does exactly that, comparing TPL's proposed definition of "ring oscillator" to Talbot Figure 3, and doing so in enough detail to make clear that Talbot Figure 3

discloses both three inverters arranged in a loop as well as three inversions arranged in a loop.

TPL's opening papers fail to address the issue.[1] Instead, TPL relies upon Dr. Oklobdzija's declaration that analyzes a hypothetical circuit not disclosed by Talbot. Based on the assumed behavior of this hypothetical circuit (that he admits under oath is not even Talbot),[2] Dr. Oklobdzija concludes that Talbot's Figure 3 is not a "ring oscillator," all without clearly defining "ring oscillator." (Oklobdzija 10/12/12 Dep. 406:11–407:14.) Dr. Oklobdzija's conclusion is without basis or merit, and should be rejected.

Strangely, TPL cites Judge Ward's claim construction of "ring oscillator" (the very construction that TPL has proposed and that reads on Talbot Figure 3) as authority for the proposition that "a ring oscillator requires three or more inverters to oscillate." (TPL Opening Brief at 11:20–26.) But it is elementary that Judge Ward's claim construction is not binding on this Court or on any of the Plaintiffs.

In any event, Judge Ward's construction of "ring oscillator" does not support TPL's position, which appears to be that if an "inversion" by itself can make a "single inversion oscillator," such "inversion" is somehow precluded from being a component of the "ring oscillator." Nowhere does Judge Ward's construction require such preclusion. Instead, presented with evidence that an oscillator could be made with a single inversion, Judge Ward merely accepted TPL's position that the *claimed* ring oscillator must nevertheless have multiple inversions, without limiting what type of inversions that could be used. (Otteson Decl., Ex. 3 at

---

[1] Indeed, TPL argues with Judge Ware's order: "TPL believes this approach is not an appropriate subject for claim construction. The Federal Circuit has never suggested that it is the role of the district court to evaluate the *technical merits* of the applicant's arguments in construing a claim." (TPL's Opening Brief at 10:11–13 (emphasis in original).) But this supplemental briefing is doing nothing more than determining the scope of TPL's continuing disclaimer of Talbot's voltage-controlled oscillator, so that the distinction from Talbot—as articulated by the patent owner in the prosecution history—can be properly reflected in the claim construction. This is nothing more exotic than application of prosecution history estoppel.

[2] As explained in Plaintiffs' opening papers (Plaintiffs' Op. Supp. Br. at 11), Dr. Oklobdzija analyzes a different, hypothetical circuit that removes everything in Talbot Figure 3 except for the Schmitt-trigger 52 and input capacitors, and adds *a direct connection between the Schmitt-trigger 52's input and the output that is not present in Talbot*. (Supp. Oklobdzija Decl. ¶ 15 (Chen Decl., Ex. 17), *Acer* Action, Dkt. No. 363-17; *see also* Oklobdzija 10/12/12 Dep. at 609:4-12, 610:1-10, Ex. 77, (Chen Supp. Decl., Exs. 24 and 32).)

11 (*Acer* Action, Dkt. No. 357-3).)

D. Dr. Oklobdzija's New Definition of "Ring Oscillator" Cannot Be Adopted Because It Is Unsupported and Met by Talbot.

At deposition, Dr. Oklobdzija admitted that he did not apply any party's proposed definition of "ring oscillator." (Oklobdzija 10/12/12 Dep. at 406:11–407:14 (Chen Supp. Decl., Ex. 24).) Instead, he pointed to the first sentence of paragraph 7 in his declaration as his definition of "ring oscillator." (*Id.* at 406:24–407:2.) That sentence reads, "Ring oscillators are **able** to provide a continuous periodic output **because** they have an odd number of inverting components arranged in a loop or 'ring.'" (Supp. Oklobdzija Decl. at ¶ 7 (Chen Decl., Ex. 17) (emphasis added).) That "definition" is different from TPL's proposed structural definition, adding the functional limitation that ring oscillators are "**able** to provide a continuous periodic output **because** they have an odd number of "inverting components." TPL's proposed functional limitation is not in the intrinsic record and so cannot be properly read into the claim construction of "ring oscillator." Indeed, TPL offers no authoritative treatise or paper setting forth or applying such a definition for "ring oscillator," just the unsupported opinion of Dr. Oklobdzija. Such unsupported testimony is not entitled to any weight. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1318 (Fed. Cir. 2005) ("[C]onclusory, unsupported assertions by experts as to the definition of a claim term are not useful to a court.")

But beyond that, Talbot Figure 3 meets Dr. Oklobdzija's new proposed functional limitation. Talbot explains how Figure 3 works, and that explanation makes clear that the voltage-controlled oscillator in Figure 3 provides a continuous periodic output because it has an odd number (3) of inverting components arranged in a loop that perpetually change the input into the next inverting component. (Talbot at 7:56–8:21 (Chen Decl., Ex. 9) (concluding, "Thus, an oscillating output signal will be provided at the output 56 of the voltage controlled oscillator circuit and the oscillation will be sustained.").) Dr. Wolfe's declaration explains the same thing. (Supp. Wolfe Decl. at ¶¶ 9, 11, 15 and 23 (Chen Decl., Ex. 8).)

Because Dr. Oklobdzija's new definition of "ring oscillator" is unsupported and in any event met by the disclaimed voltage-controlled oscillator in Talbot, it cannot be adopted.

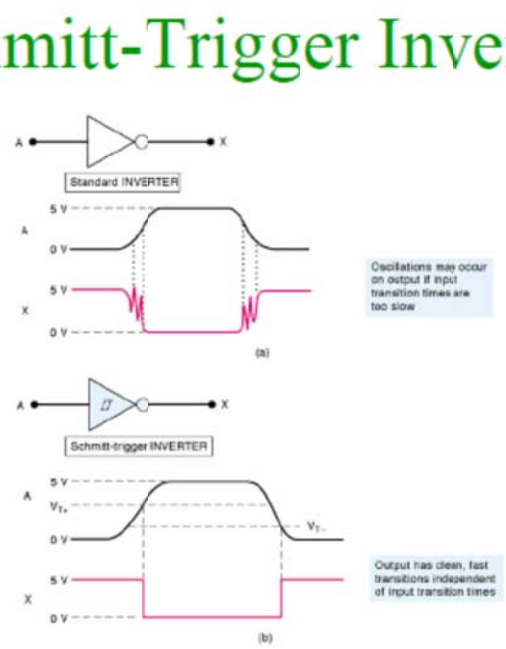
E. Talbot's Schmitt Trigger 52 Is an Inverter and Perpetuates the Oscillation in the Same Way as a Standard Inverter.

TPL argues that a Schmitt trigger is structurally and operationally different from an "inverter." To the contrary, Dr. Wolfe explains that Schmitt trigger 52 of Talbot Figure 3 is an "inverter." (*Id.* at ¶¶ 13–24.) Dr. Wolfe specifically explains, "The Schmitt trigger 52's inverting function is used to sustain the oscillation of the Talbot [voltage-controlled oscillator] in the same way that the inverters disclosed in the '336 patent sustain oscillation in the 'ring oscillator.'" (*Id.* at ¶ 23.)

Dr. Wolfe's testimony is supported by multiple independent sources (attached as exhibits to his declaration), as well as Exhibit A to Dr. Oklobdzija's Supplemental Declaration (Chen Decl., Ex. 17), which captions the very symbol used to represent Talbot Figure 3's Schmitt trigger 52 as a "Schmitt trigger inverter." Curiously, TPL failed to include with its opening papers Exhibit A of the Supplemental Oklobdzija declaration, which clearly shows a "Schmitt trigger inverter." Plaintiffs have provided it as part of Exhibit 17 to the Chen Declaration, and the relevant portion of the figure is reproduced below, together with symbol 52 from Talbot Figure 3:

(Supp. Oklobdzija Decl., Ex. A, slide 3 (Chen Decl., Ex. 17, at 14 of 50); Talbot, Figure 3 (Chen Decl., Ex. 9).) Dr. Oklobdzija admitted the above symbol is the same as that found in Talbot Figure 3. (Oklobdzija 10/12/12 Dep. at 445:6–446:2 (Chen Supp. Decl., Ex. 24).)

In its opening papers, TPL argues that the hysteresis on the input of the Schmitt trigger somehow disqualifies a Schmitt trigger inverter as a component of the claimed "ring oscillator." But hysteresis is irrelevant to how the inverting function of the Schmitt trigger 52 sustains the oscillation. (Supp. Wolfe Decl. ¶ 15 (Chen Decl., Ex. 8).) The hysteresis just protects the output from instability caused by noise on the input. (*Id.* at ¶ 16.) This point is actually illustrated by Dr. Oklobdzija's Exhibit A, as shown below:



(a) If input transition times are too long, a standard logic device-output might oscillate or change erratically; (b) a logic device with a Schmitt-trigger type of input will produce clean, fast output transitions.

(Supp. Oklobdzija Decl., Ex. A, slide 3 (Chen Decl., Ex. 17, at 14 of 50).)

The hysteresis does *not* prevent a Schmitt trigger inverter from being an inverter. As shown by Exhibit A to Dr. Oklobdzija's declaration, a Schmitt trigger inverter functions better than a standard one by providing "clean, fast output transitions" that improve upon the standard inverter's output that "might oscillate or change erratically." (*Id.*) Thus, the Schmitt trigger inverter 52 in Talbot Figure 3 is an inverter.

F. Dr. Oklobdzija's Deposition Arguments that Talbot Lacks Three Inversions/Inverters Arranged in a Loop Are Groundless and Lack Credibility.

Although his supplemental declaration does not deny that Talbot Figure 3 discloses three inverters in a loop, at deposition Dr. Oklobdzija for the first time asserted that Talbot Figure 3 does not disclose three inverters in a loop. But this deposition testimony contradicts his own textbook (which says that transistor pair 48 and 49 is an inverter) and Exhibit A to his own declaration (which captions the symbol 52 of Talbot Figure 3 as a "Schmitt-trigger inverter").

As to the Schmitt-trigger 52, Exhibit A to Dr. Oklobdzija's declaration is explained above.

Dr. Oklobdzija conceded at deposition that the symbol used in Talbot Figure 3 is an inverting type of Schmitt-trigger, but asserted it was not properly considered to be an "inverter." (Oklobdzija 10/12/12 Dep. at 443:17–444:19 (Chen Supp. Decl., Ex. 24).) This testimony is directly contradicted by Dr. Oklobdzija's testimony describing the operation of circuit 52: "Yes. I -- I agree, if you put a square wave at the input of 52, the output is going to be a square wave in the 180-degree opposite phase." (*Id.* at 572:9–11.) Dr. Oklobdzija also admitted that, when the Schmitt trigger 52 has a high input, its output would be low, and when it has a low input, its output would be high. (*Id.* at 571:3–18.) These functions—a high input resulting in a low output, and vice-versa, and a 180 degree phase shift from input to output—are exactly what an inverter does, and what it is designed to do. The fact that an inverter might have a Schmitt trigger input does not change its function at all. Similarly, the label "Schmitt trigger" is unimportant. The circuit performs an inversion, so it is an inverter. This testimony is also contradicted by Exhibit A to Dr. Oklobdzija's own declaration, which repeatedly calls the same symbol numbered 52 in Talbot Figure 3 a "Schmitt-trigger inverter." (Supp. Oklobdzija Decl., Ex. A, slide 3 (Chen Decl., Ex. 17 at 14, 15, and 19).)

As to transistor pair 48 and 49, Dr. Oklobdzija admitted that the transistor pair taken alone has the same structure as a textbook "inverter" cited by Dr. Wolfe (Oklobdzija 10/12/12 Dep. at 511:4–512:5; 515:16–517:2 (Chen Supp. Decl., Ex. 24)), and even further admitted that—given time at least—the input to transistor pair 48 and 49 has the opposite phase as the output. (*Id*. at 460:4–24.) Dr. Oklobdzija's own textbook identifies such a transistor pair as an "inverter." (Supp. Wolfe Decl. at ¶ 12, at p. 6 and Ex. L (Chen Decl., Exs. 8 and 10).) Dr. Oklobdzija even testified that one of ordinary skill in the art would interpret the symbol for "inverter 51" to represent such a transistor pair. (Oklobdzija 10/12/12 Dep. at 511:4–512:5 (Chen Supp. Decl., Ex. 24).)

Unavoidably, to distinguish Talbot over a "ring oscillator," Dr. Oklobdzija actually points to the **control** circuitry of the voltage controlled oscillator in Talbot Figure 3. Talbot identifies "input 43" as receiving the "**control** voltage." (Talbot, 7:31 (Chen Decl., Ex. 9).) According to

Dr. Oklobdzija, the frequency of oscillation of Talbot Figure 3 "really depends on the value of the **capacitors 50 and 54** and the resistance of a transistors [sic] as we spoke about, 45 and 44, which is being **controlled by the input 43**, which determines the rate of **how fast those capacitors are going to be charged or discharged**. This is what determines the principal frequency of a Talbot oscillator." (Oklobdzija 10/12/12 Dep. at 450:9–17 (Chen Supp. Decl., Ex. 24 (emphasis added).) According to Dr. Oklobdzija, transistor pair 48 and 49 is not an "inverter" because they act as "current **control** switches" (*id*. at 461:4–9 (emphasis added)) for the current that is used to charge and discharge the capacitors, (*id*. at 460:16–18). By arguing that transistor pair 48 and 49 is somehow not an inverter because they are "current **control** switches" and that the frequency is determined in part by the time to charge or discharge the capacitors on the input to Schmitt-trigger inverter 52, Dr. Oklobdzija is distinguishing Talbot based on its controllability. (*See also, e.g.*, *id.* at 488:13–23; 490:13–491:4; 638:20–639:1; 644:12–16; 647:25–648:6.) But the current **control** function performed by the transistor pair 48 and 49 does not alter its inversion function, so one of ordinary skill in the art would still consider the transistor pair to be an inverter. (*See* Wolfe Dep. at 91:12–92:13 (Chen Supp. Decl., Ex. 25).) For example, U.S. Patent No. 4,105,950 (hereinafter "Dingwall") discloses an identical control circuit as that in Talbot Figure 3 on top of a transistor pair (referred to in Dingwall as an "inverter"), also identical to Talbot's transistor pair 48 and 49. (*See id.* at 93:10–19 and Exs. 107, 109 (Chen Supp. Decl., Exs. 33, 34.); *see also* Dingwall at 1:45-46 ("Cascaded inverters I1, I2, and I3, with the output of I3 fed back to the input of I1, form a ring oscillator.")) Thus, one of ordinary skill in the art would recognize the transistor pair 48 and 49 in Talbot Figure as an inverter.

The public is entitled to consistency in the interpretation of the claimed ring oscillator. Having told the Patent Office that Talbot does not disclose a ring oscillator, the "ring oscillator" claim term must be limited to avoid reading on Talbot. The only substantive limitation in the intrinsic evidence on "ring oscillator" is the statement found in the Examiner's interview summary that the claimed ring oscillator is non-controllable and variable based on the environment. Accordingly, Plaintiffs' construction should be adopted.

G. Plaintiffs' Construction Should Be Adopted To Avoid Recapture of Abandoned Subject Matter.

Having indisputably disclaimed the voltage-controlled oscillator as part of the Phase-Locked Loop ("PLL") in Talbot Figure 3, TPL has now alleged that the claimed "ring oscillator" limitation is satisfied by a voltage- or current-controlled oscillator in a phase-locked loop—the precise structure it told the Patent Office is not covered by its claims. For example, in its infringement contentions, TPL has made the following allegation as the basis for satisfying the "ring oscillator" limitation:

> The presence of a PLL indicates the presence of a ring oscillator, either a voltage controlled oscillator ('VCO') or current controlled oscillator ('ICO'). [Underlying supplied.]

As TPL's contentions suggests, a voltage "controlled" oscillator or a current "controlled" oscillator is an oscillator that is "controlled." TPL's own expert acknowledged as much when he admitted that a voltage controlled oscillator "could be controlled by **voltage** or **current**." (*See* Oklobdzija 12/22/2010 Dep. at 354:14–19 (Chen Supp. Decl., Ex. 26) (emphasis added).)

To avoid the improper recapture of the abandoned subject matter and for all of the reasons stated above and in Plaintiffs' opening papers, Plaintiffs' construction requiring the "ring oscillator" to be "non-controllable" must be adopted.

III. OPERANDS THAT ARE PRESENT IN THE CLAIMED "INSTRUCTION REGISTER" MUST BE RIGHT JUSTIFIED.

A. An "Instruction Register" Has Always Been a Claim Limitation.

The key dispute regarding the term "instruction register" is whether statements in the prosecution history, which echo the clear and unequivocal statements in the specification, support a construction in which any operands present in the instruction register are right justified. During prosecution of the '749 patent, the examiner hand-wrote the following sentence in a summary of an October 25, 1994 interview: "Claim 1: Operand width is variable & right adjusted." TPL attempts to dismiss this statement by asserting that "whatever discussion the examiner might have had with the applicant in 1994 regarding operands is irrelevant to the construction of the term 'instruction register.'" TPL reasons that the term did not become "part of claim 1 until more than

sixteen years later," when claim 1 was amended during the '749 reexamination to expressly recite "an instruction register." (TPL Op. Supp. Br. at 6.) But TPL is wrong because, as explained below, claim 1 has always required an instruction register.

Claim 1 recites a microprocessor system that includes, among other components, a "means for fetching instructions" for the CPU. The "means for fetching" has always been recited in claim 1, and it is undisputed that the corresponding structure for this term under 35 U.S.C. § 112, ¶ 6 includes the instruction register 108 described in the specification. During the '749 reexamination, in fact, TPL specifically told the Patent Office that the corresponding structure of the "means for fetching instructions" in claim 1 includes the "instruction register." ('749 PH 1/25/2011 Amendment After Final at 18 (Chen Supp. Decl., Ex. 27) ("The patent owners have consistently contended that a proper construction of the corresponding language of claims 1 and 9 is what is now expressly recited in proposed claims 62 and 63 (with the understanding that **the "instruction register" is among the "corresponding structure" with respect to the means for fetching instructions**).") (emphasis added).) TPL's proposed construction for the "means for fetching" also includes instruction register 108. (*See* Joint Claim Construction Statement, Ex. B at 1–2 (*Acer* action, Dkt. No. 305-2).) While it is true that claim 1 was substantively narrowed in other ways during the '749 reexamination, there is no basis for TPL to argue that an "instruction register" was not a part of claim 1 until it was amended during reexamination.

B. Operands in the Instruction Register of the '749 Patent, if Present, Must Be Right Justified.

The '749 specification describes the requirement of right-justification using the type of unequivocal and absolute language that is rarely found in patent specifications. ('749, 18:34–56.) The specification describes the ability to handle variable width operands using the same opcode as "magic" and proclaims that "[t]his magic is possible because **operands must be right justified in the instruction register**. This means that the least significant bit of the operand is **always** located in the least significant bit of the instruction register." ('749, 18:43–47 (emphasis added).) Right justifying operands in the instruction register is not simply an optional design choice but a characteristic that "must be" present, to accomplish the "magic" of the alleged invention.

Plaintiffs' opening brief was accompanied by a detailed declaration from Dr. May describing the instruction register in the '749 patent and explaining in detail its disclosure of variable-width instructions with right-justified operands. Dr. May's testimony stands unrebutted, and TPL does not seriously challenge any aspect of his technical description testimony. Nor did it submit anything from its own expert regarding this term.

TPL nonetheless argues that right-justified operands should not be read as a requirement of the claimed instruction register because instructions in the '749 patent can include "simple 8-bit, fixed-width instructions," and as such, "[n]othing in this embodiment requires operands or operands in the instruction register that are right-justified." (TPL Op. Supp. Br. at 4:21:5–1.) The 8-bit (one byte) instructions to which TPL is referring, however, have no operands whatsoever.

As Dr. May explained in his declaration, an instruction in the '749 patent "may consist simply of an opcode represented in 8 bits (one byte)." (May Decl. ¶ 7 (Chen Decl., Ex. 18).) A one-byte instruction with only an opcode, however, will necessarily have no operands. (*Id.* at ¶ 7 (explaining one-byte instructions having no operands).) This possibility is in no way excluded or impacted by Plaintiffs' proposed construction: "register that receives and holds one or more instructions for supplying to circuits that interpret the instructions, in which any operands that are present must be right-justified in the register." In the case of single-byte instructions, because no operands are present, the right justified requirement would not apply.

C. Plaintiffs' Proposed Construction Would Not Vitiate Claim 7.

TPL also argues that Plaintiffs' proposed construction of "instruction register" would render claim 7 superfluous. TPL did not reproduce dependent claim 7 in its brief, and for good reason— the claim is so lengthy and includes numerous limitations not at all encompassed by Plaintiffs' proposed construction. Claim 7, following the reexamination, recites:

> 7. The microprocessor system of claim **1** wherein said instruction register for the multiple instructions and a variable width operand to be used with one of the multiple instructions is connected to
>
> said means for fetching instructions, means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for

> supplying the multiple instructions to supply the multiple instructions in succession, means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions, said counter being connected to said means for decoding to receive incrementing and reset control signals from said means for decoding, said means for decoding being configured to control said counter in response to an instruction utilizing the variable width operand stored in said instruction register, and means connected to said counter to select the variable width operand for use with the instruction utilizing the variable width operand in response to said counter.

('749 patent, *Ex Parte* Reexamination Certificate, Claim 7 (Chen Decl., Ex. 22) (text removed during reexamination omitted).)

TPL acknowledges that "[t]he doctrine of claim differentiation is at its strongest when the additional limitations proposed to be added to a parent claim appear in a dependent claim." (TPL Op. Supp. Br. at 5:6–7.) TPL cannot seriously claim that the requirement in Plaintiffs' proposed construction that "any operands that are present must be right-justified in the [instruction] register" would render superfluous or otherwise vitiate the detailed limitations of claim 7. Claim 7 recites at least the following additional limitations and structures not in claim 1:

- means connected to said instruction register for supplying the multiple instructions in succession from said instruction register;
- a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession;
- means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions.

These additional structures, which all clearly differentiate claim 7 from claim 1, are not vitiated by Plaintiffs' proposed construction by merely requiring that any operands that are present be right-justified in the instruction register.

D. The "Operand Width Is Variable and Right-Adjusted" Comment in Interview Summary Refers to Issued Claim 1 of '749 Patent.

TPL speculates that the Examiner's hand-written note in the interview summary, "Claim 1: Operand width is variable & right adjusted," was a mistake because the original claim 1 was withdrawn at that time. TPL asserts that the Examiner was likely referring to claim 11 (issued

claim 7) by the "Claim 1" reference. But TPL's theory is unsupported. The prosecution record actually reveals that the reference to "Claim 1" was directed at application claim 3 at that time, which issued as claim 1 of the '749 patent.

By the time the interview took place, claim 1 had been withdrawn and claim 2 was cancelled. ('749 PH 12/31/92 Office Action at 1 (Chen Supp. Decl., Ex. 28).) Claim 3 was therefore the first active claim under reexamination at the time of the interview. Claim 3 was also renumbered and issued as claim 1. ('749 PH 7/6/93 Amendment at 2 (Chen Supp. Decl., Ex. 29); '749 PH Amendment of 11/9/94 at 1 (Chen Supp. Decl., Ex. 30).)

TPL's speculation that the Examiner was referring to claim 11 is refuted by both parties' accounts of the interview summary. The Examiner made no reference to claim 11 as being discussed during the interview. Instead, in the "Claims discussed:" section of the Interview Summary, the Examiner referred only to claims 3, 26, and 27. ('749 PH 10/25/94 Interview Summary (Chen Supp. Decl., Ex. 31).) And the applicants, in their summary of the interview, made no reference to claim 11 as having been discussed during the interview. The applicants instead referred to claim 3. ('749 PH Amendment of 11/9/94 at 4–5 (Chen Supp. Decl., Ex. 30).) Based on the prosecution history record, it is apparent that the Examiner's comments were directed at application claim 3, which issued as claim 1.

IV. CONCLUSION

For the foregoing reasons, Plaintiffs' constructions should be adopted in their entirety.

///

///

///

///

///

///

///

///

Dated: November 9, 2012

K&L GATES LLP

By: */s/ Timothy Walker*

Timothy P. Walker, Esq.
Timothy.walker@klgates.com
Howard Chen, Esq.
Howard.chen@klgates.com
Harold H. Davis, Jr., Esq.
Harold.davis@klgates.com
Jas Dhillon, Esq.
Jas.dhillon@klgate.com
Jeffrey M. Ratinoff
Jeffrey.ratinoff@klgates.com
K&L Gates LLP
Four Embarcadero Center, Suite 1200
San Francisco, CA 94111
Phone: (415) 882-8200
Fax: (415) 882-8220

Attorneys for Acer, Inc., Acer America Corp. and Gateway, Inc.

Dated: November 9, 2012

COOLEY LLP

By: */s/ Kyle D. Chen*

Kyle D. Chen, Esq.
kyle.chen@cooley.com
Heidi L. Keefe, Esq.
hkeefe@cooley.com
Mark R. Weinstein, Esq.
mweinstein@cooley.com
Cooley LLP
3000 El Camino Real
Five Palo Alto Square, 4th Floor
Palo Alto, California 94306
Phone: (650) 843-5000
Fax: (650) 857-0663

Attorneys for HTC Corporation and HTC America, Inc.

Dated: November 9, 2012

BAKER & MCKENZIE

By: */s/ Edward Runyan*

Edward Runyan, Esq.
Edward.Runyan@bakernet.com
Baker & McKenzie
130 East Randolph Drive
Chicago, IL 60601
Phone: (312) 861-8811
Fax: (312) 698-2341

Attorneys for Barco, N.V.

ATTESTATION PER GENERAL ORDER 45

I, Edward Runyan, am the ECF User whose ID and password are being used to file Plaintiffs' Consolidated Responsive Claim Construction Brief. In compliance with General Order 45, X.B., I hereby attest that the counsel listed above have concurred with this filing.

Dated: November 9, 2012

By: */s/ Edward Runyan*
Edward Runyan

COOLEY GODWARD KRONISH LLP
HEIDI L. KEEFE (178960) (hkeefe@cooley.com)
MARK R. WEINSTEIN (193043) (mweinstein@cooley.com)
KYLE D. CHEN (239501) (kyle.chen@cooley.com)
Five Palo Alto Square
3000 El Camino Real
Palo Alto, CA 94306-2155
Telephone: (650) 843-5000
Facsimile: (650) 857-0663

Attorneys for Plaintiffs
HTC CORPORATION and
HTC AMERICA, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00877 PSG (Related to Case Nos. 5:08-cv-05398 JF and 5:08-cv-00877 JF) **SUPPLEMENTAL DECLARATION OF KYLE D. CHEN IN SUPPORT OF PLAINTIFFS' CONSOLIDATED RESPONSIVE CLAIM CONSTRUCTION BRIEF** Date: November 30, 2012 Time: 10:00 a.m. Place: Courtroom 5, 4th Floor Judge: Paul Singh Grewal
HTC CORPORATION, HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00882 PSG

BARCO N.V., a Belgian corporation, Plaintiff, v. TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORP., ALLIACENSE LTD., Defendants.	Case No. 5:08-cv-05398 PSG

I, Kyle D. Chen, declare:

1. I am an attorney at the law firm of Cooley LLP, counsel in this action for Plaintiffs HTC Corporation and HTC America, Inc. (collectively "HTC"). I make this declaration in support of Plaintiffs' Consolidated Responsive Supplemental Claim Construction Brief. I have personal knowledge of the facts contained within this declaration, and if called as a witness, could testify competently to the matters contained herein.

2. Attached to this declaration as **Exhibit 24** is a true and correct copy of excerpts from the deposition of Vojin Oklobdzija taken on October 12, 2012.

3. Attached to this declaration as **Exhibit 25** is a true and correct copy of excerpts from the deposition of Andrew Wolfe, Ph.D., taken on October 15, 2012.

4. Attached to this declaration as **Exhibit 26** is a true and correct copy of excerpts from the deposition of Vojin Oklobdzija taken on December 22, 2010.

5. Attached to this declaration as **Exhibit 27** is a true and correct copy of the Amendment in Response to Advisory Action in Ex Parte Reexamination Proceedings, dated January 25, 2011, from the file history of the reexamination of U.S. Patent No. 5,440,749 to Charles H. Moore et al.

6. Attached to this declaration as **Exhibit 28** is a true and correct copy of the Office Action, dated December 31, 1992, from the file history of U.S. Patent No. 5,440,749 to Charles H. Moore et al.

7. Attached to this declaration as **Exhibit 29** is a true and correct copy of the Amendment, dated July 6, 1993, from the file history of U.S. Patent No. 5,440,749 to Charles H. Moore et al.

8. Attached to this declaration as **Exhibit 30** is a true and correct copy of the Amendment, dated November 9, 1994, from the file history of U.S. Patent No. 5,440,749 to Charles H. Moore et al.

9. Attached to this declaration as **Exhibit 31** is a true and correct copy of the Examiner Interview Summary Record, dated October 25, 1994, from the file history of U.S. Patent No. 5,440,749 to Charles H. Moore et al.

10. Attached to this declaration as **Exhibit 32** is a true and correct copy of Exhbit 77 to the deposition of Vojin Oklobdzija taken on October 12, 2012.

11. Attached to this declaration as **Exhibit 33** is a true and correct copy of U.S. Patent No. 4,105,950 issued to Andrew Gordon Francis Dingwall, on August 8, 1978, and marked as Exhibit 107 at the deposition of Andrew Wolfe, Ph.D., taken on October 15, 2012

12. Attached to this declaration as **Exhibit 34** is a true and correct copy of excerpts from the deposition of Andrew Wolfe, Ph.D., taken on October 15, 2012 and Exhibits 108 and 109 thereto.

I declare under penalty of perjury that to the best of my knowledge the foregoing is true and correct. Executed on November 9, 2012 in Palo Alto, California.

/s/ Kyle D. Chen
Kyle D. Chen

1075599

EXHIBIT 24

UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF CALIFORNIA
--oOo--

ACER, INC., ACER AMERICA CORPORATION AND GATEWAY, INC.,
PLAINTIFFS,
vs. No. 5:08-CV-00877
TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION AND ALLIACENSE, ET AL.,

DEFENDANTS.

VIDEOTAPED DEPOSITION OF
VOJIN OKLOBDZIJA
(Volume III, Pages 395 - 653)
Friday, October 12, 2012

Reported By:
KATHLEEN WILKINS, CSR #10068, RPR, CRR, CCRR, CLR

Page 396

DEPOSITION OF VOJIN OKLOBDZIJA

BE IT REMEMBERED that on Friday, October 12, 2012, commencing at the hour of 10:42 a.m. thereof, at K&L GATES, Four Embarcadero Center, Suite 1200, San Francisco, California, before me, Kathleen A. Wilkins, RPR, CRR, CRP, a Certified Shorthand Reporter, in and for the State of California, personally appeared VOJIN OKLOBDZIJA, a witness in the above-entitled court and cause, who, being by me first duly re-sworn, was thereupon examined as a witness in said action.

Page 397

APPEARANCES OF COUNSEL

For the Plaintiffs:
K&L GATES
BY: TIMOTHY P. WALKER, ESQ.
Four Embarcadero Center, Suite 1200
San Francisco, California 94111
Telephone: (415) 882-8200
E-mail: Timothy.walker@klgates.com

For the Defendants TECHNOLOGY PROPERTIES LIMITED AND ALLIACENSE LIMITED:
AGILITY IP LAW
BY: JAMES C. OTTESON, ESQ.
149 Commonwealth Drive
Menlo Park, California 941025
Telephone: (650) 227-4800
E-mail: Jim@agiligyiplaw.com
and
OTTESON LAW GROUP, AGILITY IP LAW
BY: MICHELLE G. BREIT, ESQ.
14350 N 87th Street, Suite 190
Scottsdale, Arizona 85260
Telephone: (480) 646-3434
E-mail: Mbreit@abilityiplaw.com

Page 398

APPEARANCES OF COUNSEL (Continued)

For the Defendants HTC CORPORATION, HTC AMERICA, INC.:
COOLEY, LLP
BY: KYLE CHEN, Ph.D., Attorney at Law
3175 Hanover Street
Palo Alto, California 94304-1130
Telephone: (650) 843-5007
E-mail: Kyle.chen@cooley.com

For the Defendant BARCO N.V., a Belgian corporation:
BAKER & MCKENZIE LLP
(Appearing telephonically)
Edward K. Runyan, Attorney at Law
130 East Randolph Drive, Suite 3900
Chicago, Illinois 60601
Telephone: (312) 861-8811
E-mail: Edward.Runyan@bakermckenzie.com

ALSO PRESENT:
Philip Knolles, Videographer
–oOo–

Page 399

INDEX

INDEX OF EXAMINATIONS

INDEX OF EXHIBITS

Page 404

the same.
MR. WALKER: Just for the record, let's mark as Exhibit 66 Plaintiffs' Notice of Dr. Vojin.
(Whereupon, Deposition Exhibit 66 was marked for identification.)
MR. OTTESON: I'm sorry. Did you say 66?
MR. WALKER: Yes.
Q. All right. And, Dr. Oklobdzija, do you understand you're appearing here by agreement by the parties?
A. I'm here appearing by?
Q. Agreement of the parties.
A. Yes.
MR. WALKER: Let's mark as Exhibit 67 a pleading entitled "Supplemental Declaration of Dr. Vojin Oklobdzija." And this is just the text. I'll mark separately the -- the exhibits to it.
(Whereupon, Deposition Exhibit 67 was marked for identification.)
MR. WALKER: And we'll mark as Exhibit 68 Exhibit A to the supplemental declaration that we just marked.
(Whereupon, Deposition Exhibit 68 was

Page 405

marked for identification.)
MR. OTTESON: Thank you.
MR. WALKER: We'll mark as Exhibit 69 Exhibit B to the supplemental declaration that was previously marked.
(Whereupon, Deposition Exhibit 69 was marked for identification.)
BY MR. WALKER:
Q. So, Dr. Oklobdzija, take a look at Exhibit 67 first and tell me if you recognize that.
A. Yes, I -- I recognize it. It is my declaration which was submitted on September 14th.
Q. Is that your signature on the last page of --
A. Yes --
Q. -- the declaration?
A. -- the signature is mine.
Q. Take a look at exhibit -- what was marked as Exhibit 68 and just confirm for me that that is Exhibit A to your supplemental declaration.
A. Yes.
Q. And take a look -- take a look at what we marked as Exhibit 69 and just confirm for me

Page 406

that that is Exhibit B to your supplemental declaration.
A. Yes.
Q. Let's go back to Exhibit 67, which is your supplemental declaration. And look at page 2. There's a heading there, heading Roman numeral II, and it uses the words "ring oscillator" in quotes.
Do you see that?
A. Yes, I see.
Q. What definition of "ring oscillator" are you using in your declaration?
A. I'm using the generally accepted definition of "ring oscillator" that is being taught in courses that I teach and it's present in textbooks.
Q. Okay. Is there a paragraph of your supplemental declaration that sets forth this definition of "ring oscillator" somewhere?
A. It is at paragraph 7.
Q. Is it the entire paragraph or just a part of that paragraph?
A. Let me read through that.
You can use the first sentence as a definition, which is being amplified by the other,

Page 407

explaining the nature of -- of the oscillation and ring oscillator.
Q. So did you get that definition from a specific source?
A. I have consulted different sources. And as a matter of fact, I think I can point also to one in my declaration, which is from Fairchild Semiconductor application note, which was a figure -- Figure 1.
And over the years, what I have -- I have encountered in numerous publications in the literature. But I have not quoted any specific definition here of "ring oscillator." It is commonly understood term.
MR. WALKER: Let's mark as Exhibit 70 what's been filed in this action as a part of the joint claim construction statement of the parties. This is Exhibit B of the joint claim construction of the parties.
(Whereupon, Deposition Exhibit 70 was marked for identification.)
BY MR. WALKER:
Q. Do you recognize Exhibit 70?
A. I recognize it. I have looked at that two years ago.

Page 440

A. 52?
Q. Yes.
A. Yes.
Q. What is that a symbol for?
A. The symbol of the 52 is -- is commonly known as a Schmitt trigger.
Q. What's a Schmitt trigger?
A. Schmitt trigger is a device which output --
MR. WALKER: Go off the record.
THE VIDEOGRAPHER: Do you want to go off or ...
MR. WALKER: We'll just -- let's just go on.
THE VIDEOGRAPHER: All right.
MR. WALKER: I'll reask the question.
Q. What is a Schmitt trigger?
A. A Schmitt trigger is a device that has two different thresholds. And this is what makes it different from an inverter.
Q. So --
A. At one -- it will change the output when the signal of the input is going from zero to one, the output will change when that signal reaches particular threshold.

Page 441

When the signal is going from one to zero, the output will change not when that signal reaches the same threshold, as is the case in inverter, but when it reaches a different lower threshold, the output will change.
So this is known as a Schmitt trigger. And it is purposely made this way because that difference in the threshold levels serves as the function, like in this particular Talbot oscillator.
Q. Have you seen in engineering literature Schmitt triggers referred to as inverters?
A. The engineering literature refers to Schmitt trigger as Schmitt trigger.
Q. You've seen the phrase "Schmitt trigger inverter," correct?
A. If they want to characterize that Schmitt trigger can invert the signal, maybe. But that depends on the context, again.
I have to look at the particular context when they -- when they refer to it. But Schmitt trigger is Schmitt trigger, and it's defined as a Schmitt trigger in literature.
And we don't use it -- we don't use it in place of inverter. Actually, it's not

Page 442

interchangeable with inverter, so that if I don't have my inverter chips, I will use Schmitt triggers. No.
Q. Take a look at Exhibit A of your declaration, which is Exhibit 68. The pages aren't numbered, but if you go in about -- if we call the page that says, "Multivibrator circuits," page 1 --
A. Okay.
Q. -- go past page 2 to page 3.
A. Okay.
Q. See the title there --
A. Yes.
Q. -- on page 3, "Schmitt Trigger Inverter"?
A. Yes.
Q. Is that incorrect?
A. I would not use -- you know, if I am clear in defining academic terms, if I am presenting to this -- this to students, I would call it "Schmitt trigger operation" because that explains the operation of Schmitt trigger.
Q. What is Exhibit A to your declaration?
A. Exhibit A is a collection of lecture slides which I found on the subject, and they come

Page 443

from Villanova University in this case.
Q. How did you find them?
A. I search on the Internet, and I search for keyword "Schmitt."
Q. Did you review them before attaching them to your declaration?
A. Yes, I looked at it.
Q. Did you agree with them?
A. Not with everything. You know, with every word. But I use them because what they do is they are -- they are describing the relaxation oscillator which is based on the use of a Schmitt trigger and the charge, and this charge which is used in relaxation. And I use that to supplement my declaration of how that differs from the ring oscillator.
Q. All right. Staying with that page, that third page, titled "Schmitt Trigger Inverter," you see there's a symbol under -- underneath it, a triangle with a bubble at the output, labeled "Standard Inverter"? Do you see that?
A. The one before -- yeah, I see, it says, "Standard Inverter," yes.
Q. Do you see that?
A. Right.

Page 444

Q. If you go down --
A. Right.
Q. -- past the graphs, there's another symbol, another triangle with a bubble at the top. This one has hysteresis signal -- hysteresis symbol inside the triangle.
Do you see that?
A. Yeah.
Q. It's labeled "Schmitt Trigger Inverter."
Do you see that?
A. Yeah, I see that.
Q. Do you agree with that label, "Schmitt Trigger Inverter," for that symbol?
A. No. I think he wants to explain to students how those two, when operating by inverting the signal, are different. So -- so he's comparing the standard inverter -- inverter with the Schmitt trigger to show how the two are different.
Q. Do you agree with me that the -- I'm sorry. I don't mean to cut you off, but I'm trying to make my plane.
A. Yes, please.
Q. Do you agree with me that the symbol on page 3 of your Exhibit A to your supplemental

Page 445

declaration labeled "Schmitt Trigger Inverter" is the same symbol as used in Figure 3 of the Talbot reference labeled 52?
A. I have to look at my declaration which is in front of me.
Q. I'm sorry. I'm talking about -- I don't mean to confuse you. We're still on Exhibit A to your declaration, which is Exhibit 68, I believe.
A. Okay. No, 68 is Villanova slides.
Q. Yeah. That's what I'm talking about.
A. Okay.
Q. The third slide.
A. Yeah.
Q. Labeled "Schmitt Trigger" -- "Schmitt Inverter" at the top --
A. Right.
Q. -- right?
And now I'm directing your attention to the symbol labeled "Schmitt Trigger Inverter" on that slide.
Do you see that?
A. Yes, I see.
Q. And do you agree that that is the same symbol that is being used in Figure 3 of the Talbot reference, Feature 52?

Page 446

A. The 52 is the same symbol used on this slide.
Q. That's labeled "Schmitt Trigger Inverter" on the slide?
A. That slide is labeled "Schmitt Trigger Inverter."
Q. All right. Let's go on to Slide 5. No, I'm sorry. Let's go on to -- let's go to Slide 4 -- I'm sorry, Slide 4. Slide 4 of Exhibit 68, see the title there is "Schmitt Trigger Inverter Operation"?
A. Yes, I see it.
Q. Do you agree with that title?
A. I already answered that question. If I want to be pure, I would just call it Schmitt trigger operation because Schmitt trigger is Schmitt trigger. Because if I -- the students would confuse it with inverter, and I would not use that "inverter" in the title if I were to write those slides. But those are not my slides.
Q. Let's go to Slide 8. Up at the top it says, "Example."
A. All right.
Q. And after "Example," it says, "Show how to use a 74LS14 Schmitt trigger inverter."

Page 447

Do you see that?
A. Yes, I see that. And that shows how Schmitt trigger can oscillate with only one stage.
Q. And it's referring to that as a -- as an inverter, the Schmitt trigger, correct?
A. The outer of those slides uses that inverter with a Schmitt trigger, which, I would say, freely or in a liberal way. I don't think he's -- he's using a very precise terms.
Q. In the diagram of the solution --
A. Right.
Q. -- the symbol representing what the slide calls a Schmitt trigger inverter is the same symbol as Feature 52 of Figure 3 of Talbot, correct?
A. Yes. It is the same symbol, and that figure shows how Talbot can oscillate with only one stage. Which inverter can't. So if you had inverter in this figure, it would not oscillate. And that's, again, another distinction to show the distinction between Schmitt trigger and inverter.
Q. Let me direct your attention to Column 7 of Talbot, around line 31.
A. 31?
Q. Yeah. And actually, just to orient

Page 448

ourselves, let's take a look at line 26, which is the first sentence of that paragraph. It says:

"The voltage output from the buffer 16 is fed to an input terminal 43 of the voltage-controlled oscillator circuit."

Do you see those words?

A. Yes.

Q. All right. Down at line 31, it says, "The control voltage at input 43."

Do you see those words?

A. Yes.

Q. All right. So looking at Figure 3 of Talbot --

A. Right.

Q. -- looking at 43, that text is saying that what's coming into 43 is a control voltage?

A. Yes. That's the voltage that -- that determines the frequency of oscillation of -- of the Schmitt trigger relaxation oscillator used in Figure 3.

Q. You said earlier that VCC is the supply voltage?

A. Yes.

Page 449

Q. Does the frequency of oscillation of the voltage-controlled oscillator of Figure 3 depend on the VCC?

A. Okay. Let me qualify that and answer it in two way to make sure I'm precise.

The oscillator -- Talbot oscillator in Figure 3 is controlled by input 43. And this is the voltage that's that primarily determines the oscillation of the Talbot oscillator in Figure 3. And as I said previously, if I put 43 at zero, I can stop it.

Now, everything that is designed on the chip depends on -- in general, on the supply voltage. That is basically the nature or a physical characteristic. So if I changed VCC, anything on this die, including Talbot, would change their speed.

Q. Looking at Figure 3 of Talbot, if you were to add another inverter similar to inverter 51, would that change the frequency at which it is -- if that was the only change you made -- if that was the only change you made, and you added another inverter like 51, say, between -- between node 56 and 51, and all other operating parameters of the oscillator were the same, would that change

Page 450

the frequency of the oscillator?

A. I would have to modify the connections of 48 and 49 if I do that, and -- in order to make it operate. Because if you add another inverter in there --

Q. Let's add two inverters.

A. Okay. If you -- if you add another two inverters, in general, it will not. Okay. And the reason is because the frequency of this oscillator really depends on the value of the capacitors 50 and 54 and the resistance of a transistors as we spoke about, 45 and 44, which is being controlled by the input 43, which determines the rate of how fast those capacitors are going to be charged or discharged.

This is what determines the principal frequency of a Talbot oscillator.

Now, in general, if you vary the supply voltage, you will affect it to some extent. If you add two inverters in the loop, you may affect it to some extent. Depends on which frequency is oscillating. But in general, as it has been designed, it should not make substantial difference.

Q. But it will make some difference?

Page 451

A. Not substantial. And I could --

Q. I'm not asking if it makes substantial difference. I'm asking if it will make any difference.

MS. BREIT: Object to form.

THE WITNESS: That is -- that is, again, a very general statement. Any change here of any parameters will have some effect. And that's true for any design.

BY MR. WALKER:

Q. Okay. But there is a delay associated with propagation of the signal through inverter 51, correct?

A. Yes, but it is negligible. Let me just give you one example. If I -- if I take a ring oscillator, and -- and suppose I can make inverters infinitely fast, they have zero delay, a ring oscillator would not oscillate. Talbot will.

Q. I'm asking if inverter 51 --

A. Yes.

Q. -- has a delay associated with it.

MS. BREIT: Objection.

BY MR. WALKER:

Q. Yes or no?

MS. BREIT: Form.

Page 460

A. No. Because if -- if the voltage 43 drops to zero, Talbot stops oscillating.
Q. If Talbot is operating -- I'm sorry. If the oscillator in Figure 3 of Talbot is oscillating --
A. Right.
Q. -- because 43 is not zero --
A. Yes. Because 43 is adjusted to the frequency they desire.
Q. -- then would you agree that transistors 48 and 49 are acting as an inverter?
A. They are acting as a current controlled -- actually, as you said, Talbot described them as switches. And I think I would agree with that.
The function of 48 and 49 is to switch that capacitors either in -- I mean either charge or discharge. The fact that the signal comes out in the opposite phase is not really relevant.
Q. But the signal does come out in the opposite phase?
A. Yes. But that's not relevant. That's irrelevant to the function of Talbot. The 48 and 49 are acting as switches.
Q. Even though the output is coming out in

Page 461

opposite phase of the input, you would say that transistors 48 and 49 are not inverting the input; is that correct?
A. Transistors 48 and 49 are part of larger structure in which they operate as switches. Current control switches. To take them out of context and say, okay, because the signal comes here is zero and the output is one and say, okay, this is inverter would not be correct in my mind.
Q. Let's go to your declaration, 67. Paragraph 8 on page 3.
A. Okay.
Q. The sentence beginning on line 21:
"A Schmitt trigger is a bistable circuit such that, as the input changes, the output does not change until a certain threshold value is reached."
Do you see that?
A. Yes.
Q. I want to compare that to a regular inverter.
A. Okay.
Q. As the input changes, as the input to a normal -- what you've been speaking of as an

Page 462

inverter --
A. Okay.
Q. -- the pair of transistors acting as a transistor, as the input to that inverter changes, is it true that the output does not change until a certain threshold value is reached?
A. Let me just be -- be precise. The inverter has what is called a transfer characteristic or characteristic that shows how the output changes a function of input, and that is a curve that is followed when the input changes from zero to one or travels back from one to zero, the exact same curve is being followed.
There is a period on this curve where the inverter is in a linear region. And that switching is not instantaneous. It will change from output value one to value zero following this curve. And this is because it's not ideal.
What we would ideally want to have out of it is to make an instant change at some threshold level. But that doesn't happen.
So it will follow -- it will follow, the output will stay relatively constant. Then we'll go through the linear curve, and then it will taper the other value and also stay relatively

Page 463

constant.
So what we have when we deal with inverter, we are dealing with the ideal approximation of the inverter. So we would -- in the ideal inverter, we would have a level when we want that output to change.
Q. Is the Schmitt trigger ideal?
A. No.
Q. Does the -- I'm sorry?
A. It's not ideal, but it has two curves that it follows, so that's how it differs from -- from the inverter.
There is one part when you -- when you're moving from one to zero, the output, and there's one curve. And then when it goes back from -- from the output being zero to one, then it follows another curve, which is what -- what is known as a hysteresis of that Schmitt trigger.
Q. The inverter has a single threshold, correct?
A. Ideally, inverter would have single -- one threshold, while Schmitt trigger has two thresholds.
Q. And when the threshold of the inverter is reached, the output abruptly changes to its

Page 488

A. It doesn't have, as described '336.
Q. And in your view, the capacitance on the gates of the transistors that comprise the inverters don't count as capacitors on the inputs of those inverters; is that correct?
A. That is called intrinsic capacitance. This is called the input loading of anything that you connect to the output.
Q. So there's always some capacitance on any input is what you're saying?
A. Because you cannot produce the gate or inverter without input capacitance.
Q. And even though there's always capacitance on any input, it's your view that inserting a capacitance on an inverter input means you no longer have a ring oscillator?
MS. BREIT: Objection to form.
THE WITNESS: I haven't said that. You asked me about '336. The way it is described in '336, you have ring oscillator which doesn't have any extra capacitance on any of the nodes, and -- and that's usually how ring oscillator is implemented.
BY MR. WALKER:
Q. And you used the word "extra

Page 489

capacitance." Why did you use the word "extra capacitance"?
A. Like in Talbot, you have an extra capacitance which is added, which is essentially slowing it, and is determining the period of oscillation.
Q. And what makes the capacitance extra as opposed to intrinsic?
A. The way they did add it in Talbot, they added this transistor 50 and 54, which uses the gate to the channel capacitance. So this is how you fabricate capacitor in the integrated circuit fabrication process. So they fabricate it, two capacitors, in Figure 3 and added them to the node 53.
Q. Are you saying that the ring oscillator of the '336 patent cannot have any resistors on any of the inverter inputs?
MS. BREIT: I'm sorry. Can you repeat the question, please? I didn't hear it.
(Record read by the reporter as follows:
QUESTION: Are you saying that the ring oscillator of the '336 patent cannot have any resistors on any of the inverter inputs?)

Page 490

MS. BREIT: Objection to form.
THE WITNESS: Yeah, I haven't seen any in the '336, so there are none in the '336.
BY MR. WALKER:
Q. Even though there is some resistance between the stages?
A. That's present, you know, with every -- everything that is -- that is manufactured by the manufacturing process, because any connector has its resistance, and that's the law of physics. We don't have any material that has zero resistance, so -- or we don't know of any material yet.
Q. Are you saying that the ring oscillator of the '336 patent cannot have a capacitor resistor component in series on the inverter input?
MS. BREIT: Objection to form. And I just want to say I think you're maybe going beyond the scope of this because you're asking him to construe the '336 patent as opposed to what the Court was looking for, which is the -- whether Talbot is or is not a ring oscillator.
MR. WALKER: Within the meaning of the '336.
MS. BREIT: Well, let's see. Go ahead

Page 491

and answer.
THE WITNESS: Yeah, I don't see it in '336, and I don't see a reason why one would put that in ring oscillator.
BY MR. WALKER:
Q. And that's even though the transistors that comprise the inverters include a capacitance and the connections between the inverters include a resistance?
A. That naturally comes with them. Every transistor has its own resistance and its own capacitance. And we cannot make a transistor without -- that has no capacitance, no resistance.
So that's naturally a part of it. That's why I said that's a natural ring oscillator which consists of inverters connected to each other without anything extra being added to that or modified or -- you can certainly do -- make a lot of modification and lot of alterations, but there's no need to do that.
Q. Let's go to Figure 18. Back to Figure 18, Sheet 15 of the '336 patent.
Would you agree that Figure 18 is an incomplete --
MS. BREIT: Why don't we wait until he

Page 508

says:
"There is a commonly used symbol specifically called inverter and triangle with the bubble at the output. That symbol merely represents a circuit's inverting function. It does not specify the internal structure of the circuit" -- "does not specify the internal structure of the inverter circuitry."
Well, does not specify internal structure, but the internal structure is well understood. I mean, I think this sentence is kind of absurd, because what he's saying, this triangle represents an inverter and does not represent transistors, which are inside.
Well, I think isn't that obvious, because if we were to represent it with transistors, we would have drawn it with S transistors, not as a symbol. But we know what that symbol represents.
So I -- I'm baffled by that sentence.
According to user -- just a second.
"The use of inverter symbol is

Page 509

not required to represent circuits that perform the inverting function."
Okay. So what? I don't understand that. If you want to represent inverting function, you have to use some symbols so people understand this is inverting function. And if you are not using any symbol, then what are you representing? Okay.
"It's common to represent an inverter in drawings as combination of components that performs the inverting function."
That's another, I think, mysterious sentence because we can represent circuits at the transistor level or the logic level. And the reason we do it on the logic level, because we understood what is on the transistor level, so we don't want to repeat it. I am very puzzled by paragraph 6.
Q. Let's go back to one of the sentences that you disagreed with.
A. Okay.
Q. The sentence that begins:
"Though there is a commonly

Page 510

used symbol specifically called an inverter, a triangle with a bubble on the output, that symbol merely represents the circuit's inverting function and does not specify the internal circuitry of the inverter's circuitry."
My question is, when you see a triangle --
A. Right.
Q. -- with a bubble on it, is there only one transistor-level circuit that is represented by that symbol?
A. Yes. And this is why we -- we have established symbols, schematic symbols, and that's basically kind of a convention.
So instead of drawing transistors that make an inverter, I will make a triangle with a bubble, and everyone skilled in the art will understand how to make that with transistors.
So the sentence here, this merely represents the circuit inverting function, is puzzling to me. I don't know what is merely represent.
I think there is -- there is one-to-one

Page 511

correspondence between that and the circuit representation. If there is more than one, then we engineers would not know what we are designing.
Q. Let's skip ahead to page 5 of the supplemental Wolfe declaration, Exhibit 73.
First of all, do you recognize the figure that's captioned "Inverter circuit" from Talbot Figure 3?
A. Yes, we were discussing it, 48 and 49.
Q. Okay.
A. But I would not call it inverter circuit. Again, I said they are representing switches, and -- and, as you said also, Talbot calls them switches. And I agree with Talbot, they are switches.
Q. Let's go to the figure below that, Figure 1.4, captioned "Construction of a CMOS Inverter."
A. Yes.
Q. And you'll see that there's a -- one of the multiple figures is darker than some of the others there --
A. Yes, I see that. Right.
Q. Is that an example of a -- or is that a CMOS inverter?

Page 512

A. Yes. Figure 4 -- 4.14C represents a transistor diagram of a CMOS inverter.
Q. And that is what corresponds to a triangle with a bubble on it?
A. Yes.
Q. And is that the kind of circuitry that you were talking about as comprising the inverters of the test structure that you had experience with in 1979 through 1982?
MR. OTTESON: Objection to the form.
THE WITNESS: Okay. As I said, I want to be precise. In 79 to 82, we dealt with the NMOS technology, which had that inverter implemented different, with deletion mode, transistor replacing a P transistor. So it's a similar structure, but it was different technology. And it will be different than the one used after 85, when CMOS started to prevail.
So the transistor diagram in NMOS is different from the transistor diagram in CMOS, is different from transistor diagram in gallium arsenide.
But what we know, which technology we are talking about, there is one-to-one correspondence between the symbol and the circuit

Page 513

realization of it.
BY MR. WALKER:
Q. So the symbol that's a triangle with a bubble on it can represent different circuits depending on the technology at least; would you agree with that?
A. A symbol with a bubble --
Q. A triangle with a bubble.
A. -- triangle with a bubble is a symbol. But we have to have -- again, we have to know which technology we are talking about. It's sort of like an agreement. If I use this triangle, this is what I am representing.
So I have to specify two things: That this is a CMOS technology and CMOS technology is unambiguous, or I have to add to that this is a gallium arsenide technology, it will be, again, unambiguous, one-to-one correspondence between the transistor realization and the logic diagram.
Q. But within a particular technology, your testimony is that a triangle with a bubble on the output would correspond to a single circuit on the -- single unambiguous circuit on the transistor level?
A. In a particular technology, if we

Page 514

specify the particular technology, then there is a one-to-one correspondence between the logical symbol and the corresponding circuit realization.
And, for example, if we take that Figure 14C, we say, okay, we are in a CMOS technology, this is a symbol, and this is -- below that symbol is a circuit realization of that inverter. And we would know that.
Q. And a ring oscillator, according to the '336 patent, could be constructed of a -- a loop of inverters, connected input to output, having a structure of 1.4C on page 5 of Dr. Wolfe's supplemental declaration; is that right?
MS. BREIT: Objection to form.
THE WITNESS: The ring oscillator of '336 consists of a loop of inverters which, for example, if you look at that figure, I believe it was Figure 8, where we had that seven inverters. The symbol underneath would be that transistor structure.
And you have also asked me, you know, the output. The top one will be connected to V -- VCC, the bottom will be connected to ground. Those are the connections that you asked that were missing.

Page 515

BY MR. WALKER:
Q. In Figure 1.4. You were asking -- you're talking now about Figure 18?
A. From the -- yes. From the patent.
Q. About the power connections?
A. Right.
Q. Okay. So let's look at -- we have, up above again, we have an excerpt -- on page 5 of Dr. Wolfe's declaration, an excerpt from the Talbot Figure 3.
And so why don't we -- why don't I have you take a look at Talbot Figure 3 here just to get all of it in front of you. I just want you to compare these two figures a little bit.
A. Right.
Q. So first of all, let me ask you if -- if there's a difference -- well, first of all, let me ask you. On page 5 of Dr. Wolfe's declaration, has he correctly labeled the PMOS and NMOS transistors 48 and 49 from Talbot Figure 3?
A. Yes.
Q. All right. And in the inverter circuit from Talbot Figure 3, to the left of the transistors 48 and 49, there's a -- a dot on the lines --

Page 516

A. Right.
Q. -- do you see that?
Does the location of that dot change how the circuit works, if it was, say, relocated halfway between 48 and 49?
MR. OTTESON: Objection to form.
THE WITNESS: I want to make sure -- you're talking about a dot between 48 and 49?
BY MR. WALKER:
Q. There is a dot on the left-hand side.
A. Which is connecting gates.
Q. Connecting the gates.
A. Right.
Q. That's right.
A. Okay.
Q. And I'm trying to make sure that you'll agree with me that that -- that part of the circuit could be redrawn to look like 1.4, where the line, instead of being -- you have a horizontal input coming into a dot and then branching into the gates of the two transistors.
And that would be an equivalent circuit?
MS. BREIT: Objection to form.
THE WITNESS: Yeah, I understand what your question is. They are not drawn exactly the

Page 517

same. And your question is isn't it the same? Yes, it's the same.
BY MR. WALKER:
Q. All right. But your testimony was that Figure 3 is different because 48 and 49 are also connected to 45 and 44 in Figure 3 of Talbot?
A. Yes. And this is where, if I read that page 5 from Dr. Wolfe's testimony, that he calls that inverter circuit from Talbot Figure 3. And this is -- you know, with all due respect, is where the pulling the rabbit out of the hat comes. Because this is just a part of the Figure 3.
And to call it inverter, I think it's -- it's now a stretch of imagination. You know, the topology, they look like -- if you take this picture out and compare it to 14C, yes, they look alike. And then he jumps into conclusion, calling it inverter. Hold on. This is not an invertor. Sorry.
Q. So going to Figure 3, I just want to go to Figure 3 in Talbot --
A. Right.
Q. -- and make sure I understand a couple of things about it.
A. Right.

Page 518

Q. The -- I want to be sure that in the segment between transistor 45 and 48 --
A. Right.
Q. -- there will be a voltage there, correct?
A. Yes.
Q. And that voltage will be higher than the voltage between 49 and 44, correct?
A. You mean the voltage on the line 43?
Q. Maybe I have to be a little more careful here, how I phrase the question here.
Let's say the -- why do you say the voltage on line 43?
A. Your question was whether the VCC is higher than the voltage on 44 or something like that? So I wanted to jump ahead.
Q. Let me --
A. You meant 43?
Q. Let me restate my question.
A. All right.
Q. I want you to compare the voltage on the connection between 45 and 48.
A. Okay. Let's call it an odd X.
Q. And the connection between 49 and 44.
A. Let's call it an odd Y.

Page 519

Q. Which voltage is higher, X or Y?
A. Let me think for a moment. Can I?
Okay. This would be one of the three key questions I would ask my students to trick them and flunk them if I want. It really depends. And let me explain that.
Q. Sure.
A. For example, the 53 node is fully charged. And now I -- and the feedback flipped, switch is a switch 49. And the line 43 makes the current trickle. So Y would be pretty close to -- to the voltage on the node 53, and it will be gradually going down, okay.
Now, when it reaches the threshold, the feedback flips and triggers the transistor 48 switch, which switched to node 53. And now I have a node X, which should actually be lower than what Y was. It will start raising up and may surpass it.
So both of those nodes are bouncing up and down as -- as the feedback switches and as the Talbot relaxation oscillator oscillate. And I said the question will be tricky because I think someone jump in conclusion right away, thinking that X is higher than Y. No. No. One has to be

Page 568

MR. RUNYAN: Well, Michelle, I'm a human being. I have a brain, I have logic, and I can tell that he's -- that he's just drifting far afield, and perhaps it's because he made an incorrect assumption about what I was asking or whatever. I mean, it's not like I can't say a word until he's absolutely silent and says, "I'm done."

MS. BREIT: The irony of --

MR. RUNYAN: You know, that's ridiculous.

MS. BREIT: So the irony of this discussion was that you just cut me off right in the middle of what I was saying.

Let's go ahead and you can start questioning him again. But if you interrupt his answers, I am going to -- I'll see whether Kyle is still intending to ask his questions, but we're going to have to move on.

MR. RUNYAN: Well, I think you better be sure you're right if you're threatening to stop a deposition and direct the witness not to answer any of my questions, especially when it's for me to make a -- make a clarification. You know, it's just ridiculous.

Page 569

Q. Dr. Oklobdzija?
A. Yes, sir.
Q. You mentioned two thresholds of Schmitt trigger 52.
A. Yes, sir.
Q. Is there something that you call those thresholds? Do you have label for them, a threshold --
A. There is a -- there is a threshold low to high and there is a threshold high to low.
Q. Low to high and there's a threshold high to low. So which -- those thresholds, when you say "thresholds," they're actually -- that's actually a voltage, right, a voltage level?
A. It is actually a voltage level, exactly.
Q. Okay. So the threshold that you call low to high is a -- a voltage that -- level that is lower than the threshold that's the voltage level of high to low; is that right?
A. Yes. If I may suggest the Figure 3 from the -- the Exhibit 68 has a diagram showing the output of the Schmitt trigger as the input changes. And it has labeled the two thresholds VTL and VTH.
Q. Okay. For -- now, you said the supply

Page 570

voltage here of this circuit VCC would depend on the technology.

What is that -- what would a typical supply voltage be on the circuit, this circuit CMOS, right?

MS. BREIT: Objection to form.

THE WITNESS: This is -- sir, this is where I was getting in when we got into this whole big argument and discussion. I was just going to suggest, if you agree, if you want, let's assume that this voltage is three volts.

BY MR. RUNYAN:
Q. Okay.
A. This is the amount you mentioned before.

So if we say our assumption is this voltage is three volts, for the sake of arguing or explanation, whatever, I will accept it.
Q. Okay. So do you know what -- do you have in mind a -- what a value might be for -- a voltage value might be for the -- the lower threshold in the Schmitt trigger 52?
A. We can -- we can label this diagram, and let's say we -- we assume that the lower threshold is -- so let's say we are talking about three-volt power supply, and let's make a lower threshold to

Page 571

be one volt, and let's make the higher threshold to be two volts.
Q. Okay. All right. So my question is, if I have a voltage -- if I have a half a volt on the input of Schmitt trigger 52 and it's not changing --
A. Right.
Q. -- the output of Schmitt trigger 52 is going to be high, right?
A. Is going to be one.
Q. And when you say one, logical one, not one volt, right.
A. Yes, three volts.
Q. Okay. And when the input to Schmitt trigger 52 is above two volts and not changing, the output is going to be low, right?
A. Yes. Logical zero or close to zero volts.
Q. Right. And the -- if I put a square wave -- you know -- you know what a square wave is, right?
A. Yes.
Q. If I put a square wave into Schmitt trigger 52, what would the output look like?
A. It will be a square wave.

Page 572

Q. And it would be a square wave so the -- it will be a square wave that's actually inversion of the square wave that's on the input, right?
A. Yes.
Q. In other words, in the positive part of the -- of the input, when the -- when the square wave on the input is -- is high, the square wave on the output will be low, right?
A. Yes. I -- I agree, if you put a square wave at the input of 52, the output is going to be a square wave in the 180-degree opposite phase.
Q. Thank you, Dr. Oklobdzija.
A. Sure.
MR. RUNYAN: I have no further questions.
THE WITNESS: Thank you very much. And, again, you know, let's make peace, and I apologize for any --
MR. RUNYAN: Well, I picked up the handset so I wasn't on the speakerphone, so ...
THE WITNESS: I'm sorry. Yeah. I'm really sorry for -- for -- for -- you know, for all the commotion that came in, and -- and I apologize if I was a bit uncooperative or appeared uncooperative. I hope we are -- no bad feelings.

Page 573

MR. RUNYAN: All right. I -- I have to leave, so I'm going to sign off now. Thank you everyone.
THE WITNESS: Thank you again.
MR. RUNYAN: Bye.
THE WITNESS: Bye.
MR. CHEN: Bye, Ed.
Okay. So you want to take a break?
THE WITNESS: Let's take a break after this.
MS. BREIT: How long --
THE VIDEOGRAPHER: The time is now 4:59, and we are going off the record.
(Whereupon, a recess was taken.)
(Whereupon, Deposition Exhibit 74 was marked for identification.)
THE VIDEOGRAPHER: Correction. This marks the end of Disk 3 to the deposition of Dr. Oklobdzija. The time is now 5:06 p.m., and we are going off the record.
(Whereupon, a recess was taken.)
THE VIDEOGRAPHER: This marks the beginning of Disk 4 to the deposition of Dr. Oklobdzija. The time is now 5:12 p.m., and we are on the record.

Page 574

EXAMINATION BY MR. CHEN
BY MR. CHEN:
Q. Hello, Dr. O. So my name is Kyle Chen. I represent HTC in this matter.
Well, let's actually just do -- you know, first do some housekeeping things that, I guess, you know, earlier we didn't do.
So is there anything that's preventing you from testifying competently and truthfully today?
A. I don't think so.
Q. Okay. There was no drinking, partying before you came here?
A. No. Except the tea.
Q. Good.
All right. So, I mean, I kind of want to understand the scope you're -- the scope of your employment with the defendants.
Are you aware that the defendants have initiated an ITC action, which is International Trade Commission action, on the same patent -- one of the same patents-in-suit?
A. I don't know if I should be aware. I'm not aware.
Q. Okay.

Page 575

A. But maybe I was told.
Q. So it's not a trick question. I'm just trying to figure out --
A. Right.
Q. -- if you -- you have been retained for that matter. It sounds like, given that you are not even ...
A. I may have. I'm not even aware. You know, as you know, I was retained by Farella, Braun --
Q. Okay.
A. -- which was two years ago. We have -- we had a deposition here with you in San Jose. And it has been a long -- long period of time --
Q. Okay.
A. -- between -- has elapsed.
So my memory -- and so I was recently asked to provide my opinion on the Talbot versus ring oscillator and which is my expert testimony that I have submitted and that I'm giving.
And I have forgotten, frankly, a lot about this case, who is involved, who and what. You know, I perhaps should know, but I can't say I'm hundred percent on top of that.
Q. Okay. No problem.

Page 608

A. In this case --
Q. -- 52?
Sorry. Could you let me finish my question before you answer? I just want to make sure I understood.
So 56 is the output of the Schmitt trigger 52, correct?
MS. BREIT: Objection to form.
THE WITNESS: 56 is the output of the Schmitt trigger 52.
BY MR. CHEN:
Q. Okay. Thank you. And then please continue.
A. And the 53 is the input.
Q. Okay.
A. And they are connected together. So I am labeling them here --
Q. Okay.
A. -- on this diagram.
Q. Okay. Okay. So -- so on Exhibit 77, which is the clean copy of the picture --
A. Right.
Q. -- there is a connection between A and B, correct?
A. Yes.

Page 609

Q. And that's the connection as described in the second portion of the first sentence in 50- -- strike that.
Please refer to the connection between Point A and Point B in Exhibit 77.
A. Yes.
Q. That's the connection as described in the second portion of paragraph 15 in Exhibit 67, correct?
A. Yes.
Q. Is that connection part of Talbot?
A. No. That connection is illustration of -- in support of my statement that the oscillator in Figure 3 of Talbot is capable of oscillating with only the capacitor 50 and the Schmitt trigger when the output is connected directly back to the input of the Schmitt trigger.
In support of my declaration that states that unlike ring oscillator, which cannot oscillator with only one stage, Talbot can oscillate with one stage, which is one of the differentiating features between ring oscillator and Talbot.
Q. That's a long answer, so let me just make sure I understand it correctly.

Page 610

The connection between Point A and Point B in Exhibit 77 is not part of the Talbot patent, correct?
A. I answered that already once, and it's on the record what I said. In order to clarify, if your question is the Exhibit 77 matching anything in the Talbot patent, I said, no. And I explained that this is a construction showing how the Schmitt trigger relaxation oscillator can oscillator with one stage only.
Q. But the connection between Point A and Point B in Exhibit 77 is what you added but does not exist in the Talbot reference, correct?
A. In this case, you added -- you added it, not me, yes. And it does not exist in the Talbot record.
Q. But Exhibit 77 is an accurate depiction of the structure you described in 15 -- in paragraph 15 of your --
A. Yes --
Q. -- declaration?
A. -- of my --
Q. Okay. No problem. Yeah.
Okay. So earlier it seems that you were using the terminology -- the following

Page 611

terminologies differently, so I just want to make sure I understand.
So you seem to say an inverter is different from a Schmitt trigger?
A. Yes. In general.
Q. Okay. And you are also saying Schmitt trigger is not an inverter, correct?
A. Yes. Otherwise it will be known as an inverter. You know, would not have a specific designation and symbol as a Schmitt trigger, yes.
Q. But an inverter is not the same as an inverting stage, correct?
A. That's correct. Inverting stage is more than an inverter.
For example, if we have an NAND gate, that is an inverting structure, or a NOR gate is an inverting structure, or some block, like the block -- current control block shown in Figure 3 to the left of the Talbot, is a structure that would invert one of the inputs, because it has two inputs.
Q. What does an inverting stage do?
A. Okay.
MS. BREIT: Objection to form.
THE WITNESS: For example, if we take a

Page 636

Figure 18?
A. No. And it doesn't have to be shown because, as we went through that exercise, that symbol represents an inverter, a circuit structure which has two transistors, one P, one N, which are not visible, connected to VCC and ground. So we don't need to do it on this figure.
MR. CHEN: What's the current exhibit number?
THE REPORTER: Next one is 83.
MR. CHEN: 83.
(Whereupon, Deposition Exhibit 83 was marked for identification.)
BY MR. CHEN:
Q. Is the structure as shown in Exhibit 83 a ring oscillator?
MS. BREIT: Objection to form.
THE WITNESS: If we go by Judge definition of "ring oscillator," which says an odd number of inverters connected in a loop, then this is not.
BY MR. CHEN:
Q. Is there an inversion between the output of 51 and node 53?
A. Again, this is a cannibalized stage, and

Page 637

modified stage, which is not Talbot, does not represent Talbot. I mean, this is a Figure 3 which has been modified to such extent that it does not resemble Talbot, and it's not anything close to what was described in the Talbot patent.
So we are talking about something different here. And I will answer questions in that context.
Q. Okay. Is there an inversion between the output of 51 and node 53 as shown in Exhibit 83?
A. Yes, there is an inversion there.
Q. Is there an inversion between node 53 and 56?
A. Yes, there is an inversion.
Q. Is there an inversion between node 56 and the output of 51?
A. There is an inverter between 56 and the output of 51, which is the inverter 51.
Q. Would inverter 51 produce an inversion between node 56, which is the input of inverter 51 and the output of inverter 51?
A. Yes.
Q. How many inversions are there in the structure as depicted --
A. Again --

Page 638

Q. -- in Exhibit 83?
A. Again, let me repeat. This is a cannibalized Talbot structure to the extent -- and it's modified structure from Talbot Figure 3, that you should remove the Figure 3 below that because it has no resemblance with the Figure 3.
This is something different. This is something different. This is something that has three inversion stages in the loop, and it doesn't fit the judge -- I believe Judge -- not Judge Ward, but Judge Fogel's definition of what a ring oscillator is. Judge Weir definition.
Q. You're agreed that there are three inversions connected in a ring in the structure as depicted?
A. It's undeniable that there are three inversions in this structure. But this is a cannibalized structure that has no connection with Talbot.
We are talking about a construct -- you know, a complete construct where the essential things which make Talbot relaxation oscillator were taken away, which is -- the essential thing is the capacitance was taken away. The current control, which is used to control that oscillator,

Page 639

was taken away. And -- and it's a structure which has three inversions. You know, that's undeniable.
But it has nothing to do with the subject of this deposition, if I may say. And I think that, you know, at this point I am -- I'm getting tired, because I think all of this exhibits, 80, 79, 70, 77, that you are trying to push in front of me and are trying to make it connected somehow to Talbot have no structure with Talbot.
Because we have to be honest. If we are talking about Talbot, then we are talking about Figure 3 in Talbot. This is not Figure 3 in Talbot. And I don't know why I'm deposed here, because I'm answering questions that have nothing to do with the '336 patent case basically.
And I'm just being tortured here into a construct which have nothing to do with this case, basically. This has nothing to do with '336 case. I'm sorry. This is not -- neither resemble Talbot, neither resembles ring oscillator, and I don't know, you know, why you're taking my time.
I'm tired. I'm basically tired. And if there is a reason, and if we are related to the

Page 644

oscillator which I have described in -- in one of the previous paragraphs, Number 7.

So my paragraph 15, as I said, I have listed the differences between ring oscillator and Talbot, A, B, C, D, as the Talbot is relaxation oscillator. Ring oscillator is a ring oscillator. Ring oscillator is symmetric. Every output produces the same waveform. Talbot is not. It produces a sawtooth waveform. That the ring oscillator consists of the inverters connected in a loop. This is Judge Weir definition.

Here we have -- in case of Talbot, we have stages which are not inverter. The Schmitt trigger is not characterized as inverter. The first stage is a current control stage, which charges and discharges the capacitor.

The nature of oscillation in Talbot is based on relaxation which is charge and discharge of capacitor, while the nature of oscillation in a ring oscillator is based on the delay of the inverter employed in the loop.

And I have submitted that -- that Exhibit 82, which is clearly described in very common sources, as Webster and Wikipedia, et cetera, et cetera.

Page 645

So in my declaration, in support of my declaration, in support of my opinion, in paragraph 15, I am trying to illustrate how the two differ because the nature of oscillation of one is different from the other and, therefore, we can make relaxation oscillator, which is what Talbot is, oscillate with only one stage.

And we have actually demonstrated that to you on the exhibit which became the Exhibit Number 78. 78. Okay.

And so that is -- that is the purpose of that paragraph, to educate and explain the substantial -- and from the mental differences between the two, what makes Talbot Talbot and what makes ring ring.

MR. CHEN: Okay. I almost done. I know that the tape is out, so --

THE VIDEOGRAPHER: No.

MR. CHEN: No? You said that's --

THE VIDEOGRAPHER: No. No. I said there's 30 minutes left of depo.

MR. CHEN: Oh, yeah, yeah, but you said five minutes --

THE VIDEOGRAPHER: No, no. I was doing it on that.

Page 646

MR. CHEN: Oh, sorry. Okay. Then, in any event, let's just a take a couple minutes off, maybe three minutes. Let me just go through my notes to make sure I covered everything.

THE VIDEOGRAPHER: The time is now 7:34 p.m. We are going off the record.

(Whereupon, a recess was taken.)

THE VIDEOGRAPHER: The time is now 7:37 p.m., and we are back on the record.

BY MR. CHEN:

Q. Let's go back to Exhibit 79.

THE VIDEOGRAPHER: Correction. Audio problems. The time is now 7:37 p.m. We are back on the record.

THE WITNESS: Okay. I'm on Exhibit 79.

BY MR. CHEN:

Q. I'm sorry. Actually ...

Earlier you testified that there are three inverting stages in Figure 3 of Talbot connected in a ring, but later you changed your mind, correct?

MS. BREIT: Objection to form.

THE WITNESS: Well, when -- I think Mr. Tim Walker mentioned that Talbot characterizes that switches. I realize that is correct. And

Page 647

even though it may give appearance of inversion, the whole purpose of this stage, the more I look at it, the more I examine it, the more we probe it, the more I'm convinced it's a current control switching. This is what it is.

And to call it inverter would be wrong because inverter has only one input. This has two inputs. And it has a very different -- different function.

So calling that you can put an input in and close the inversion is really, I think, taking things out of the proper context of how the Talbot oscillator works and how it is intended to work and why the things that are in Talbot are in Talbot.

And you cannot take things out like you have been taking in those Exhibits 79, in particular, because if you take enough things out of this, Talbot -- you will eventually make it something else. And that's not the point.

So if I look at this structure, this is a current control switch. That is what intent of Talbot is to make out of that, is a current control switch.

Switches are 48 and 49, and their

Page 648

current is being controlled by the current mirror consisting of 47, 46. They are actually current mirror 44 -- 44 and 45, and the current source, which I believe -- and this one I may be wrong, is Widlar, so-called a Widlar current source, consisting of 46 and 47. So it's a Widlar -- Bob Widlar structure, the current mirror structure, that is employed at Talbot.

Again, I -- there is Widlar, there is Wilson -- it's not Wilson. I think it's Widlar, Bob Widlar's current structure that is being employed here. So it's a very different and complex structure.

So just merely reduce it and -- and call it inverter, I can't. That's why I'm -- I'm backing off from that, and it's -- it is something else.

BY MR. CHEN:

Q. You said transistor 48 and transistor 49 in Figure 3 of Talbot produce a switch, correct?

A. They are switches, yes.

Q. A switch of what?

A. A switch of the current. And that's the essence here, of the current which is supplied to them through 45 or 44. And that amount of

Page 649

current, which is essential here to Talbot, is being controlled by that current mirror on the left.

So the switch is going to switch on, but it's going to trickle only as much current as it is allowed by that left side.

So inverter can switch fully to the full potential. The transistor situation. But this is not happening here.

So those are the switches which are -- which are trickling the current into this capacitor 50, and the rate by which they supply that current to the capacitor 50 and 54 or take that current away to transistor 9 and 44 is what determines the frequency of oscillation of Talbot oscillator. That's why you call it voltage-controlled oscillator. That was his intent.

Q. Is there an inversion between the output of 51 and node 53?

MS. BREIT: I'm going to object because I think this question may have been asked maybe a dozen times in this deposition --

THE WITNESS: I think hundred times.

MS. BREIT: -- already. And it's

Page 650

getting late. He's told you he's very tired. I don't know if the goal is to hope that he gets tired enough to give you a different answer, but I think it's inappropriate at this point.

THE WITNESS: I would -- I would ask the court, the reporter, to maybe number it when I answer those, and I can just refer and say Number 5. Because I've answered many of those questions many times. So instead of answering, I just say, "Refer to Number 5" or "Refer to Number 3," which that has been already answered and explained at length.

So I think that would be my answer to that. I would say, you know, yes, would you please go back to the record and read it.

MS. BREIT: And I do want to add that I think that Counsel should have coordinated -- we're now having three counsels asking the same questions, repeating themselves and repeating from other counsel. So it's -- it's -- I think if you can't ask him something that's new, we need to end the deposition.

MR. CHEN: Okay. I have no further questions. Thank you very much.

THE WITNESS: Well, thank you very much.

Page 651

THE VIDEOGRAPHER: This marks the end of deposition. Today's date is October 12, 2012, at 7:44. We are going off the record. Thank you, Counsel.

(Whereupon, the deposition concluded at 7:44 p.m.)

--oOo--

CERTIFICATE OF DEPONENT

I hereby certify that I have read and examined the foregoing transcript, and the same is a true and accurate record of the testimony given by me. Any additions or corrections that I feel are necessary, I will attach on a separate sheet of paper to the original transcript.

_____
Signature of Deponent

I hereby certify that the individual representing himself/herself to be the above-named individual, appeared before me this _____ day of _____, 2012, and executed the above certificate in my presence.

_____
NOTARY PUBLIC IN AND FOR

_____
County Name

MY COMMISSION EXPIRES:

CERTIFICATE OF REPORTER

I, KATHLEEN A. WILKINS, RPR, CRR, CCRR, CLR, Certified Shorthand Reporter, hereby certify that the witness in the foregoing deposition was by me duly sworn to tell the truth, the whole truth and nothing but the truth in the within-entitled cause; that said deposition was taken down in shorthand by me, a disinterested person, at the time and place therein stated, and that the testimony of the said witness was thereafter reduced to typewriting, by computer, under my direction and supervision.

I further certify that I am not of counsel or attorney for either or any of the parties to the said deposition, nor in any way interested in the event of this cause, and that I am not related to any of the parties thereto.

DATED:_____, 2012

_____
KATHLEEN WILKINS, RPR, CRR, CCRR, CLR, CSR 10068

EXHIBIT 25

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs,	)	
vs.	)	No. 3:08-cv-00877 PSG
TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	)	

DEPOSITION OF ANDREW WOLFE, PH.D.

Monday, October 15, 2012

1:09 p.m.

149 Commonwealth Drive

Menlo Park, California

Reported by Hanna Kim, CLR, CSR No. 13083

MENLO PARK, CALIFORNIA
MONDAY, OCTOBER 15, 2012

DEPOSITION OF ANDREW WOLFE, PH.D., taken on behalf of the Defendants, at Agility IP Law, LLP, 149 Commonwealth Drive, Menlo Park, California, beginning at 1:09 p.m. and ending at 4:30 p.m., on Monday, October 15, 2012, before me, Hanna Kim, CLR, CSR License No. 13083.

APPEARANCES OF COUNSEL:

For Acer Inc., Acer America Corp., and Gateway Inc.:
K&L GATES LLP
BY: TIMOTHY P. WALKER, ESQ.
Four Embarcadero Center, Suite 1200
San Francisco, California 94111
415.882.8200 415.882.8220 Fax
timothy.walker@klgates.com

For HTC Corporation and HTC America, Inc.:
COOLEY LLP
BY: KYLE D. CHEN, PH.D., ESQ.
3175 Hanover Street
Palo Alto, California 94304-1130
650.843.5019 650.849.7400 Fax
kyle.chen@cooley.com

APPEARANCES OF COUNSEL:

For Technology Properties Limited and Alliacense Limited:
AGILITY IP LAW
BY: BRANDON BAUM, ESQ.
VINH PHAM, ESQ.
149 Commonwealth Drive
Menlo Park, California 99025
650.227.4800 650.318.3483 Fax
brandon@agilityiplaw.com
vpham@agilityiplaw.com

INDEX OF EXAMINATION
WITNESS: ANDREW WOLFE, PH.D.

INDEX OF EXHIBITS

INDEX OF EXHIBITS: (CONTINUED)

DEPOSITION OF ANDREW WOLFE, PH.D.
Menlo Park, California; Monday, October 15, 2012
1:09 p.m.

ANDREW WOLFE, PH.D.,
having been administered an oath, was examined and testified as follows:

(Deposition Exhibit No. 101 was marked.)

EXAMINATION

BY MR. BAUM:

Q. Good afternoon, Dr. Wolfe. I know you've been deposed in this case before, so -- but we're going to pick up with exhibits -- beginning at Exhibit No. 101 to your deposition. And I've handed you a copy of Exhibit 101.

Do you recognize that document?

A. Yes.

Q. Is that a copy of your supplemental declaration submitted in support of plaintiff's supplemental claim construction brief and signed on September 14 of 2012?

MR. WALKER: Mine has some highlight on it, I don't think was in the original. I don't know if it was intentional.

MR. BAUM: Oh, great. It's not supposed to.

At least that would not be accurate.

MR. WALKER: We have it on the record about the highlighting.

MR. BAUM: Why don't we -- do you want to go see if you can locate a clean copy?

BY MR. BAUM:

Q. May I ask for Exhibit 101 back, and we will replace it, unless you want to see my highlighting.

MR. CHEN: Oh, okay.

MR. BAUM: Thanks.

(Discussion off the record, 1:11 p.m.)

MR. BAUM: Let me mark as Exhibit 102 to the Wolfe deposition.

(Deposition Exhibit No. 102 was marked.)

BY MR. BAUM:

Q. Dr. Wolfe, I'll hand you Exhibit 102, and two copies for counsel sitting next to you.

Have you seen the first claim construction order that was issued in this case and filed on June 12, 2012?

A. Yes.

Q. And is that what is shown on Exhibit 102?

A. Yes.

Q. Can you turn to page 13 of Exhibit 102, in particular beginning on line 20.

Page 90

surrounding a portion of Figure 1A of Dingwall, is there any difference between 109 and 108?
A. There are gray squares drawn around a portion of Figure 1A of Dingwall and Figure 3 of Talbot. I guess the Talbot one is a rectangle. But other than that, I don't see any differences.
Q. Just for the record, as laying foundations, does the Figure 3 of Talbot as reproduced on Exhibit 108 an accurate reproduction of Figure 3 in Talbot?
A. It appears to be.
Q. How about the Figure 3 in Exhibit 109; other than the circle, with respect to Talbot Figure 3, is that an accurate reproduction of Figure 3 of Talbot?
A. Other than the gray rectangle, it is, yes.
Q. Please examine the circle portion of the circuitry in Exhibit 109 with respect to Dingwall U.S. Patent 4,105,950.
A. Okay.
Q. Please examine the circled portion of Figure 3 of Talbot in Exhibit 109.
A. Okay.
Q. In the circled portion of Dingwall U.S. Patent No. 4,105,950, is there a triangle surrounding certain circuitry?

Page 91

A. There's a triangle with a bubble at its tip that surrounds two transistors that are labeled P and N.
Q. I was going to ask you the bubble. That's fine.
So there is a triangle with a bubble at the end referred to as I-1 in Dingwall, U.S. Patent No. 4,105,950, correct?
A. I didn't understand the beginning of the question. What was the question?
Q. Strike that. Rephrase the question.
The triangle symbol with bubble at the end, as depicted in the circled portion of Dingwall on the Exhibit 109, what would a person skilled in the art back in 1989 would understand that symbol to mean?
A. That is a symbol to transistor CMOS inverter.
Q. How would one skilled in the art back in 1989 understand the transistor referred to as P inside I-1 of Dingwall?
A. That is a PMOS switching transistor that is part of a simple to transistor inverter.
Q. How about the transistor labeled as N inside the triangle I-1 with the bubble at the end as part of the circled portion of Dingwall?
A. That is an NMOS transistor that is part of a simple to transistor inverter.

Page 92

Q. Overall, do you see any difference whatsoever with respect to the circuitry as shown in the circled portion of Figure 1A of Dingwall U.S. Patent No. 4,105,950 and the circled portion of Figure 3 of Talbot U.S. Patent No. 4689581 as depicted in Exhibit 109?
A. Different forms of symbols are used for devices, but in terms of what those drawings would mean to a person of ordinary skill in the art, in each case, they are the identical devices connected in an identical way, only drawn using different variations of symbols for the same thing.
Q. What does VDD in Dingwall correspond to with respect to Figure 3 in Talbot?
A. VDD is a way to represent the primary supply voltage in a CMOS circuit.
Q. And how does that VDD in Dingwall correspond to the symbols or components as shown in Figure 3 of Talbot?
A. It would correspond to each place that is labeled VCC in Talbot. VCC really refers traditionally to the supply voltage in a bipolar circuit, but because engineers are familiar with it, it's often used in CMOS circuits to mean the primary supply voltage, as well.

Page 93

Q. How does P-1, as referred to in Dingwall, correspond to the components in Talbot?
A. It's the identical component representation as Transistor 47. It's drawn using a different variety of symbol, but it's the same component connected in the same way.
Q. How about P-2?
A. P-2 is the same component as Transistor 45 in Talbot, and it's connected in the same way.
Q. How about P inside the triangle I-1 with a bubble at the end?
A. Transistor P in Dingwall is the same component as Transistor 48 in Talbot, and they're connected in identical manners.
Q. How about transistor N referred to in Dingwall?
A. Transistor N in Dingwall is the same component as Transistor 49 in Talbot, and they're connected identically.
Q. How about transistor N-2 in Dingwall?
A. Transistor N-2 is the same component as Transistor 44 in Talbot, and they're connected identically.
Q. How about Transistor N-1 in Dingwall?
A. Transistor N-1 in Dingwall is the same

Page 106

the word "familiar" as used in the Moore patent?
MR. CHEN: Objection to form. Asked and answered many times.
THE WITNESS: I don't recall whether it's used in other situations, but when it's used with respect to the ring oscillator, it's talking about a particular test structure that was very well-known among microprocessor engineers as of 1989 that involved having an uncontrolled ring of inverters that would, since it was uncontrolled, track transistor manufacturing variations, temperature variations, and voltage variations.
BY MR. BAUM:
Q. I'm sorry, Dr. Wolfe, but like you, I haven't seen this patent before today, so I'm taking a little...
Have you seen the Dingwall '950 patent before today?
A. No.
MR. WALKER: Asked and answered.
MR. CHEN: Asked and answered.
BY MR. BAUM:
Q. You mentioned that you thought -- strike that.
You said that you were evaluating Dingwall based on a person having ordinary skill in the art.

Page 107

Who is a person having ordinary skill in the art, for purposes of understanding the Moore patent?
MR. CHEN: Form.
THE WITNESS: I think I explained that in my declaration.
BY MR. BAUM:
Q. Did you?
A. It may have been in my earlier declaration.
I think that was -- actually, it's not in here.
I think it would be somebody as of 1989 who was -- who had a bachelor's degree in electrical engineering or computer science or computer engineering and some working experience in microprocessor design.
Q. And is that the standard that you applied in forming the opinions that you express in Exhibit 101?
A. Yes.
MR. BAUM: That's all I have.
MR. WALKER: All I have.
MR. CHEN: Thank you.
(Proceedings concluded at 4:30 p.m.)
//
//

Page 108

JURAT

I, ANDREW WOLFE, PH.D., do hereby certify under penalty of perjury that I have read the foregoing transcript of my deposition taken on Monday, 10/15/2012; that I have made such corrections as appear noted herein in ink, initialed by me; that my testimony as contained herein, as corrected, is true and correct.

Dated this _____ day of _____, 2012, at _____, California.

_____
ANDREW WOLFE, PH.D.

Page 109

CERTIFICATE OF REPORTER

I, Hanna Kim, a Certified Shorthand Reporter, do hereby certify:
That prior to being examined, the witness in the foregoing proceedings was by me duly sworn to testify to the truth, the whole truth, and nothing but the truth;
That said proceedings were taken before me at the time and place therein set forth and were taken down by me in shorthand and thereafter transcribed into typewriting under my direction and supervision;
I further certify that I am neither counsel for, nor related to, any party to said proceedings, not in anywise interested in the outcome thereof.
In witness whereof, I have hereunto subscribed my name.

Dated: ____ day of _____, 2012

_____
Hanna Kim
CLR, CSR No. 13083

EXHIBIT 26

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

--oOo--

HTC CORPORATION and HTC AMERICA, INC.

PLAINTIFFS,

v. Case No. C-08-00882 JF

Related to Case No. C-08-00877 JF

TECHNOLOGY PROPERTIES LIMITED,

PATRIOTIC SCIENTIFIC CORPORATION

AND ALLIACENSE, LIMITED

DEFENDANTS.

VIDEOTAPED DEPOSITION OF VOJIN OKLOBDZIJA

(Volume 2, Pages 247 - 394)

Wednesday, December 22, 2010

REPORTED BY:

KATHLEEN WILKINS, CSR #10068, RPR, CRR, CCRR, CLR

DEPOSITION OF VOJIN OKLOBDZIJA

BE IT REMEMBERED that on Wednesday, December 22, 2010, commencing at the hour of 10:38 a.m. thereof, at COOLEY, LLP, 3175 Hanover Street, Palo Alto, California, before me, Kathleen A. Wilkins, RPR, CRR, CRP, a Certified Shorthand Reporter, in and for the State of California, personally appeared VOJIN OKLOBDZIJA, a witness in the above-entitled court and cause, who, being by me first duly resworn, was thereupon examined as a witness in said action.

APPEARANCES OF COUNSEL

For the Plaintiffs HTC CORPORATION, HTC AMERICA, INC.:

COOLEY, LLP
BY: KYLE CHEN, Ph.D., Attorney at Law
3175 Hanover Street
Palo Alto, California 94304-1130
Telephone: (650) 843-5007
E-mail: Kyle.chen@cooley.com

For the Defendants TECHNOLOGY PROPERTIES LIMITED AND ALLIACENSE LIMITED:

FARELLA, BRAUN & MARTEL, LLP
BY: EUGENE Y. MAR, Attorney at Law
235 Montgomery Street
San Francisco, California 94104
Telephone: (415) 954-4927
E-mail: Emar@fbm.com

APPEARANCES OF COUNSEL (Continued)

For the Defendant BARCO N.V., a Belgian corporation:

BAKER & MCKENZIE LLP
(Appearing telephonically)
Edward K. Runyan, Attorney at Law
Daniel O'Connor, Attorney at Law
130 East Randolph Drive, Suite 3900
Chicago, Illinois 60601
Telephone: (312) 861-8811
E-mail: Edward.Runyan@bakermckenzie.com

ALSO PRESENT:

Sean McGrath, Videographer

--oOo--

INDEX

INDEX OF EXAMINATIONS

INDEX OF EXHIBITS

---o0o---

Page 252

December 22, 2010 10:38 A.M.

P R O C E E D I N G S

THE VIDEOGRAPHER: Good morning. We're on the video record, ladies and gentlemen, at 10:38 a.m. I am Sean McGrath, from Alderson Court Reporting, in Washington, DC. The phone number is (202) 289-2260.

This is a matter pending before the U.S. District Court for the Northern District of California in the case captioned "HTC Corporation and HTC America, Incorporated, versus Technology Properties Limited, Patriot Scientific Corporation and Alliacense Limited," Case No. 5:08-CV-00882-JF.

This is the beginning of Disk 1, Volume II, of the deposition of Dr. Vojin Oklobdzija on December 22nd, 2010. We are located at 3175 Hanover Street, Palo Alto, California. This is taken on behalf of the defendant.

Counsel, would you please identify yourselves, starting with the questioning attorney.

MR. CHEN: Well, first of all, it's -- the deposition is for the plaintiffs, so -- that's fine.

Page 253

Kyle Chen, from Cooley, LLP, on behalf of HTC Corporation and HTC America.

MR. MAR: Eugene Mar, from Farella, Braun & Martel, for the defendants, Technology Properties, Limited, and Alliacense, Limited, and for the witness as well.

THE VIDEOGRAPHER: Will the court reporter please swear in the witness.

MR. MAR: One second.

Ed, do you want to state your --

MR. RUNYAN: Yeah. I didn't know if -- if Tim or Hal were there. This is Ed Runyan, for Barco, NV.

THE VIDEOGRAPHER: Will the court reporter please swear in the witness.

VOJIN OKLOBDZIJA,
having been duly sworn,
was examined and testified as follows:

--oOo--

THE VIDEOGRAPHER: You may proceed.

MR. MAR: Kyle, I just want to get one quick thing on the beginning of the statement.

I just want to lay on the record that TPL has agreed to produce its expert for an additional four hours of deposition time, of

Page 254

actual testimony time, to be questioned by HTC today.

MR. CHEN: All right. Thank you.

MR. MAR: Go ahead, Kyle.

EXAMINATION BY MR. CHEN

MR. CHEN: Q. Okay. Good morning, Doctor.

A. Good morning.

Q. So how are you today?

A. All right.

Q. Okay. So for the record, could you state your full name and occupation.

A. My name is Vojin Oklobdzija. I am a professor emeritus of the University of California, as well as adjunct professor at the University of Texas.

Q. Okay. Thank you.

So how long have you been a professor?

A. Okay. Let me count. About over 20 years.

Q. Over 20 years. Okay.

So could you, like, describe briefly your career as a professor for the 20 years?

A. I -- well --

Q. Like, where you started and in what

Page 255

subject area.

A. Right. I started actually in 1971, right after I -- I graduated. I got my engineering degree.

Q. Where did you graduate from?

A. University of Belgrade in Yugoslavia, in electronics and telecommunications.

Q. What was your degree? What was the degree?

A. Engineer. Diploma engineer. It's a European five-year program.

Q. Okay. Like --

A. Equivalent to master's degree here.

Q. Understood. Okay.

Okay. Please go ahead.

A. And so 1973, I was what would be kind of assistant professor title there, until 1976, when I came to U.S. to pursue a Ph.D. here. And --

Q. Where -- where was that?

A. At UCLA.

Q. UCLA.

A. Which I obtained in '82.

Q. In which department?

A. I was in computer science.

Q. Computer science. Okay?

Page 352

create, generate a voltage which is -- which is controlling the frequency of the VCO.
Q. So you control the voltage of the voltage-controlled oscillator in order to control the oscillator in a phase lock loop, correct?
A. Right.
Q. In controlling the voltage-controlled oscillator, you're locking the frequency of such voltage-controlled oscillator with the frequency of the external reference, correct?
A. Well, what phase lock loop is trying to do is -- is trying to make a voltage-controlled oscillator to run close to the frequency or multiple of the frequency or derivative of the frequency of some external reference. It's trying to steer the voltage-controlled oscillator to run idea in the lock step. That is why the "phase lock loop" term comes, to lock them in phase, ideally. But it doesn't happen.
Q. What do you mean, that it doesn't happen?
A. Because there is always a chasing around between phase lock loop signal or external reference and a VCO. They -- they never run -- they never run in a lock. All right.

Page 353

So -- and this is the base for the phase lock loop, is to generate that voltage, which is based on the error, on the difference, in order to steer the VCO toward the reference. So -- and that's the whole purpose of the phase lock loop.
Q. So the VCO receives control signals in order to be steered towards the reference clock, correct?
A. Well, the VCO is -- is controlled, but not directly, by the voltage, which is generated -- which is -- and that voltage, which is derived from the phase difference between that oscillator and some external reference derivative.
Q. So the voltage-controlled oscillator is controlled by the voltage generated by the difference between the frequency of the external reference and the frequency of the voltage-controlled oscillator, correct?
A. Let me rephrase it.
I mean, it's not directly controlled. The VCO -- the voltage that controls VCO is derived. So indirectly comes from the difference between the frequency of the VCO and derivative of some external reference.
Q. What do you mean by "indirectly"?

Page 354

A. Indirectly, I mean there is no direct control because the difference in their frequency or these phases' arrival generates the voltage, generate the pulses. It's basically -- there is a part of digital logic there.
Those pulses are filtered to generate the voltage. And that voltage is applied -- voltage or current -- it could be a current also -- that voltage may generate the current. That current controls the frequency of the VCO.
So the control of the VCO has steps. It's removed by steps further to that phase difference.
Q. Let me understand it.
So you're saying the voltage-controlled oscillator is actually controlled by current as opposed to voltage?
A. It could be, I said. You know, it could be controlled by voltage or current.
Q. If it is controlled by current, wouldn't you call it a current-controlled oscillator instead of a voltage-controlled oscillator?
A. No. This is where I said it's indirect, it's not directly. It is because that current is a consequence of the voltage. So there's a

Page 355

voltage that controls the current. The current affects the -- affects the frequency, so -- and that voltage also is a product of a filter. So -- and what comes into the filter is not the voltage. They are pulses, basically.
Q. So the current that controls the voltage-controlled oscillator will directly control the oscillator?
A. No. It -- it does affect the frequency.
Q. What directly controls the voltage-controlled oscillator?
A. The frequency of the voltage-controlled oscillator depends on many parameters, and among them, temperature and voltage.
Q. So temperature and voltage directly control the voltage-controlled oscillator?
A. I wouldn't say directly. They -- they are parameters that affect the behavior of the VCO.
Q. Are there any factors directly control the voltage-controlled oscillator in a phase lock loop?
A. I would not -- I would not single out, you know, one single factor since there are several factors. So the frequency of the VCO

and the I/O interface are clocked. They're synchronous systems. CPU is a synchronous system, and the I/O is synchronous system.

MR. CHEN: Okay. I guess I have no -- nothing further.

THE WITNESS: Thank you very much.

MR. CHEN: Thank you.

THE VIDEOGRAPHER: This marks the end of Volume II, Disk 2, and concludes the deposition of Dr. Vojin Oklobdzija. The time is 4:02 p.m. We are off the record.

(Whereupon, the deposition concluded at 4:02 p.m.)

--oOo--

CERTIFICATE OF DEPONENT

I hereby certify that I have read and examined the foregoing transcript, and the same is a true and accurate record of the testimony given by me. Any additions or corrections that I feel are necessary, I will attach on a separate sheet of paper to the original transcript.

_____
Signature of Deponent

I hereby certify that the individual representing himself/herself to be the above-named individual, appeared before me this _____ day of _____, 2010, and executed the above certificate in my presence.

_____
NOTARY PUBLIC IN AND FOR

_____
County Name

MY COMMISSION EXPIRES:

CERTIFICATE OF REPORTER

I, KATHLEEN A. WILKINS, RPR, CRR, CCRR, CLR, Certified Shorthand Reporter, hereby certify that the witness in the foregoing deposition was by me duly sworn to tell the truth, the whole truth and nothing but the truth in the within-entitled cause; that said deposition was taken down in shorthand by me, a disinterested person, at the time and place therein stated, and that the testimony of the said witness was thereafter reduced to typewriting, by computer, under my direction and supervision.

I further certify that I am not of counsel or attorney for either or any of the parties to the said deposition, nor in any way interested in the event of this cause, and that I am not related to any of the parties thereto.

DATED:_____, 2010

_____
KATHLEEN WILKINS, RPR, CRR, CCRR, CLR, CSR 10068

EXHIBIT 27

Attorney Docket No.: 0081-011X1
Merged with: 0081-011X2
Merged with: 0081-011X3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): **Moore** (et al.)
Serial No.: **90/009,034**
Filed: **March 31, 2008**

Examiner: **Pokrzywa, Joseph R.**
Attorney Docket: **0081-011X1**
Group Art Unit: **3992**

merged with

Control No.: **90/009,389**
Filed: **January 16, 2009**

Attorney Docket: **0081-011X2**

merged with

Control No.: **90/010,520**
Filed: **April 30, 2009**

Attorney Docket: **0081-011X3**

Title: **High Performance, Low Cost Microprocessor Architecture**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Customer Number: **40972**

AMENDMENT IN RESPONSE TO ADVISORY ACTION
IN EX PARTE REEXAMINATION PROCEEDINGS

In response to the Advisory Action dated **December 16, 2010**, please amend the above identified application as follows.

I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent and Trademark Office on January 25, 2011.

By: /Larry E. Henneman, Jr./

Attorney Docket No.: 0081-011X1
Merged with: 0081-011X2
Merged with: 0081-011X3

IN THE CLAIMS

Please amend the claims as follows:

1. (Curently Amended) A microprocessor system, comprising a central processing unit integrated circuit, a memory external of said central processing unit integrated circuit, a bus connecting said central processing unit integrated circuit to said memory, and means connected to said bus for fetching instructions for said central processing unit integrated circuit on said bus from said memory, said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle, said bus having a width at least equal to a number of bits in each of the instructions times a number of the instructions fetched in parallel, said central processing unit integrated circuit including an arithmetic logic unit and a first push down stack connected to said arithmetic logic unit, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input and means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input, a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack, said arithmetic logic unit having an output connected to said means for storing a top item;

wherein

the microprocessor system comprises an instruction register configured to store the multiple sequential instructions and from which instructions are accessed and decoded; and

wherein

the means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to the central processing unit integrated circuit during a single memory cycle comprises supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched.

2. (Original) The microprocessor system of claim 1 additionally comprising means connected to said means for fetching multiple instructions for determining by decoding the multiple instructions if multiple instructions fetched by said means for fetching multiple instructions require a memory access, said means for fetching multiple instructions fetching additional multiple instructions if decoding the multiple instructions shows that the multiple instructions do not require a memory access.

3. (Original) The microprocessor system of claim 2 in which the decoding determines if the multiple instructions do not require a memory access by a state of a bit of each of the multiple instructions.

4. (Original) The microprocessor system of claim 3 in which the bit is a most significant bit of the multiple instructions.

5. (Currently Amended) The microprocessor system of claim 1[additionally comprising an] wherein said instruction register for the multiple instructions is connected to said means for fetching instructions, means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession, means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions, said counter being connected to said means for decoding to receive incrementing and reset control signals from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and to supply a control signal to said means for fetching instructions in response to a SKIP instruction in the multiple instructions.

6. (Original) The microprocessor system of claim 5 additionally comprising a loop counter connected to receive a decrement control signal from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and the decrement control signal to said loop counter in response to a MICROLOOP instruction in the multiple instructions to provide a microloop within the multiple instructions in said instruction register for a number of repetitions controlled by said loop counter.

7. (Currently Amended) The microprocessor system of claim 1[additionally comprising an] wherein said instruction register for the multiple instructions and a variable width operand to be used with one of the multiple instructions is connected to said means for fetching instructions, means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession,

means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions, said counter being connected to said means for decoding to receive incrementing and reset control signals from said means for decoding, said means for decoding being configured to control said counter in response to an instruction utilizing the variable width operand stored in said instruction register, and means connected to said counter to select the variable width operand for use with the instruction utilizing the variable width operand in response to said counter.

8. (Canceled)

9. (Canceled)

10. (Currently Amended) The microprocessor system of claim [9]_62 additionally comprising a second push down stack, said means for storing a top item being connected to provide an input to said second push down stack and a control means connected between said means for storing a top item and said second push down stack for controlling provision of the input to said second push down stack.

11. (Original) The microprocessor system of claim 10 in which said second push down stack is additionally configured as a register file and said means for storing a top item and said second push down stack additionally configured as the register file are bidirectionally connected.

12. (Original) The microprocessor system of claim 11 additionally comprising means connected to said means for fetching multiple instructions for determining by decoding the multiple instructions if multiple instructions fetched by said means for fetching multiple instructions require a memory access, said means for fetching multiple instructions fetching additional multiple instructions if decoding the multiple instructions shows that the multiple instructions do not require a memory access.

13. (Currently Amended) The microprocessor system of claim 12 [additionally comprising an] wherein the instruction register for the multiple instructions is connected to said means for fetching instructions, means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession, means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions, said counter being connected to said means for decoding to receive incrementing and reset control signals from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and to supply a control signal to said means for fetching instructions in response to a SKIP instruction in the multiple instructions.

14. (Original) The microprocessor system of claim 13 additionally comprising a loop counter connected to receive a decrement control signal from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and the decrement control signal to said loop counter in response to a MICROLOOP instruction in the multiple instructions within the multiple instructions in said instruction register for a number of repetitions controlled by said loop counter.

15. (Original) The microprocessor system of claim 13 in which said means for decoding is configured to control said counter in response to one of the multiple instructions utilizing a variable width operand stored in said instruction register with the multiple instructions, said microprocessor system additionally comprising means connected to said counter to select the variable width operand for use with the instruction utilizing the variable width operand in response to a state of said counter resulting from control of said counter by said means for decoding.

16. (Original) The microprocessor system of claim 12 in which the decoding determines if the multiple instructions do not require a memory access by a state of a bit of each of the multiple instructions.

17. (Original) The microprocessor system of claim 16 in which the bit is a most significant bit of the multiple instructions.

18. (Currently Amended) The microprocessor system of claim [9] 62additionally comprising a programmable read only memory containing instructions connected to said bus, means connected to said bus for fetching instructions for said central processing unit on said bus, said means for fetching instructions including means for assembling a plurality of instructions from said programmable read only memory, storing the plurality of instructions in said dynamic random access memory and subsequently supplying the plurality of instructions from said dynamic random access memory to said central processing unit on said bus.

19. (Currently Amended) The microprocessor system of claim [9] 62additionally comprising a direct memory access processing unit having the capacity to request and execute instructions, said bus connecting said direct memory access processing unit to said dynamic random access memory, said dynamic random access memory containing instructions for said central processing unit and said direct memory access processing unit, said direct memory access processing unit being connected to means for fetching instructions for said central processing

unit on said bus and for fetching instructions for said direct memory access processing unit on said bus.

20. (Original) The microprocessor system of claim 19 additionally comprising a variable speed system clock connected to said central processing unit and a fixed speed system clock connected to control said means for fetching instructions for said central processing unit and for fetching instructions for said direct memory access processing unit.

21. (Original) The microprocessor system of claim 9 in which said microprocessor system is configured to provide different memory access timing for different storing capacity sizes of said dynamic random access memory by including a sensing circuit and a driver circuit, and an output enable line connected between said dynamic random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level after a memory read operation as a function of different capacitance on said bus as a result of the different storing capacity sizes of said dynamic random access memory, said microprocessor system being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

22. (Original) The microprocessor system of claim 21 in which the predetermined electrical level is a predetermined voltage.

23. (Original) The microprocessor system of claim 9 in which said microprocessor system is configured to operate at a variable clock speed; said microprocessor system additionally comprising a ring counter variable speed system clock connected to said central processing unit, said central processing unit and said ring counter variable speed system clock being provided in a single integrated circuit, said ring counter variable speed system clock being configured to provide different clock speed to said central processing unit as a result of transistor propagation delays, depending on at least one of temperature of said single integrated circuit, voltage and microprocessor fabrication process for said single integrated circuit.

24. (Original) The microprocessor system of claim 23 additionally comprising an input/output interface connected between said microprocessor system and an external memory bus to exchange coupling control signals, addresses and data between said central processing unit and said input/output interface, and a second clock independent of said ring counter variable speed system clock connected t said input/output interface to provide clock signals for operation of said input/output interface asynchronously from said central processing unit.

25. (Original) The microprocessor system of claim 24 in which said second clock is a fixed frequency clock.

26. (Original) The microprocessor system of claim 9 in which said first push down stack has a first plurality of stack registers having stack memory elements configured as latches, a second plurality of stack registers having stack memory elements configured as a random access memory, said first and second plurality of stack registers and said central processing unit being provided in a single integrated circuit with a top one of said second plurality of stack registers being connected to said a bottom one of said first plurality of stack registers, and a third plurality of stack registers having stack memory elements configured as a random access memory external to said single integrated circuit, with a top one of said third plurality of stack registers being connected to a bottom one of said second plurality of stack registers, said microprocessor system being configured to operate said first, second and third plurality of stack registers hierarchically as interconnected stacks.

27. (Original) The microprocessor system of claim 26 additionally comprising a first pointer connected to said first plurality of stack registers, a second pointer connected to said second plurality of stack registers, and a third pointer connected to said third plurality of stack registers, said microprocessor system being configured to operate said first, second and third plurality of stack registers hierarchically as interconnected stacks by having said central processing unit being connected to pop items from said first plurality of stack registers, said first stack pointer being connected to said second stack pointer to pop a first plurality of items from said second plurality of stack registers when said first plurality of stack registers are empty from successive pop operations by said central processing unit, said second stack pointer being connected to said third stack pointer to pop a second plurality of items from said third plurality of stack registers when said second plurality of stack registers are empty from successive pop operations by said central processing unit.

28. (Original) The microprocessor system of claim 9 additionally comprising a first register connected to supply a first input to said arithmetic logic unit, a first shifter connected between an output of said arithmetic logic unit and said first register, a second register connected to receive a starting polynomial value, an output of said second register being connected to a second shifter, a least significant bit of said second register being connected to said arithmetic logic unit, a third register connected to supply feedback terms of a polynomial to said arithmetic logic unit, a down counter, for counting down a number corresponding to digits of a polynomial to be generated, connected to said arithmetic logic unit, said arithmetic logic unit being responsive to a polynomial instruction to carry out an exclusive OR of the contents of said first register with the contents of said third register if the least significant bit of said second register is a "ONE" and to pass the contents of said first register unaltered if the least significant bit of said second register is a "ZERO" until said down counter completes a count, the polynomial to be generated resulting in said first register.

29. (Original) The microprocessor system of claim 28 in which said first register is a result register, said first shifter is a left shifting shifter, said second register is a multiplier register connected to receive a multiplier in bit reversed form, said second shifter is a right shifting shifter, said third register is connected to supply a multiplicand to said arithmetic logic unit, said down counter is configured for counting down a number corresponding to one less than the number of digits of the multiplier, said arithmetic logic unit being responsive to a multiply instruction to add the contents of said result register with the contents of said third register, if the least significant bit of said second register is a "ONE" and to pass the contents of said first register unaltered if the least significant bit of said second register is a "ZERO" until said down counter completes a count, the product resulting in said first register.

30. (Previously Presented) The microprocessor system of claim 1 wherein said central processing unit integrated circuit includes a prefetch circuit configured to request a fetch of a next set of multiple sequential instructions when no unexecuted instruction in the instruction register requires a memory access.

31-33. (Canceled)

34. (Currently Amended) The microprocessor system of claim 1 wherein said central processing unit integrated circuit is configured to access an operand located in a first instruction location of the instruction register in response to an instruction of the multiple sequential instructions in a second instruction location of the instruction register distinct from the first instruction location.

35. (Previously Presented) The microprocessor system of claim 34 wherein said central processing unit integrated circuit is configured to access the operand in response to an op-code of the instruction in the second instruction location.

36. (Currently Amended) The microprocessor system of claim 1 wherein the instruction register is configured to store the multiple sequential instructions in corresponding instruction locations including a particular location for storing an instruction to be executed, the central processing unit integrated circuit being configured to respond to content of an instruction of the multiple sequential instructions by accessing the particular location of the instruction register.

37. (Previously Presented) The microprocessor system of claim 36 wherein the central processing unit integrated circuit is configured to respond to content of the instruction of the multiple sequential instructions by accessing the particular location of the instruction register after the means for fetching fetches next multiple sequential instructions.

38. (Previously Presented) The microprocessor system of claim 36 wherein the central processing unit integrated circuit is configured to respond to content of the instruction of the multiple sequential instructions by accessing the first-execution location of the instruction register without the fetching means fetching next multiple sequential instructions.

39. (Previously Presented) The microprocessor system of claim 36 wherein the content is an op-code.

40. (Previously Presented) The microprocessor system of claim 1 wherein the multiple sequential instructions comprise a first plurality of sequential instructions arranged from beginning to ending positions of the first plurality of sequential instructions, the central processing unit integrated circuit being configured to respond to content of a first instruction of the first plurality of sequential instructions stored in said instruction register by accessing a second instruction in a second plurality of sequential instructions arranged from beginning to ending positions of the second plurality of sequential instructions, the second instruction being in the beginning position of the second plurality of sequential instructions.

41. (Previously Presented) The microprocessor system of claim 40 wherein the second plurality of sequential instructions is distinct from the first plurality of sequential instructions.

42. (Previously Presented) The microprocessor system of claim 40 wherein the second plurality of sequential instructions is the first plurality of sequential instructions and the first instruction is disposed in a position other than the beginning position of the first plurality of instructions.

43. (Previously Presented) The microprocessor system of claim 40 wherein the content is an op-code.

44. (Currently Amended) The microprocessor system of claim 1 wherein the instruction register has a plurality of instruction locations for storing the multiple sequential instructions according to an order, the plurality of instruction locations including a first location to be accessed before any other of the plurality of instruction locations, the central processing unit integrated circuit further including means for accessing a next instruction out of the order, the next instruction being located at the first location.

45. (Currently Amended) The microprocessor system of claim 1 wherein the instruction register hasa plurality of instruction locations for storing the multiple sequential instructions, the plurality of instruction locations including a first location to be accessed before any other of the plurality of instruction locations, the central processing unit integrated circuit further including means, responsive to content of an instruction of the multiple sequential instructions in a location other than the first location, for accessing a next instruction at the first location.

46. (Previously Presented) The microprocessor system of claim 1wherein said central processing unit integrated circuit includes a program counter comprising address bits, said fetching means configured to locate the multiple sequential instructions using the address bits from the program counter.

47. (Previously Presented)The microprocessor system of claim 46 wherein the address bits are a most significant bit portion from the program counter.

48. (Previously Presented) The microprocessor system of claim 47 wherein the central processing unit integrated circuit is configured to increment the address bits of the program counter after said means for fetching multiple sequential instructions fetches the multiple sequential instructions.

49. (Currently Amended) The microprocessor system of claim 47 wherein the most significant bit portion is 30 of 32 bits of the program counter.

50. (Currently Amended) The microprocessor system of claim 47 wherein the instruction register has a plurality of instruction locations for storing the multiple sequential instructions, and multiplexer means connected to said instruction register for selectively supplying multiple instructions from said instruction register.

51. (Previously Presented) The microprocessor system of claim 47 wherein the multiple sequential instructions comprise a first plurality of sequential instructions, the central processing unit integrated circuit being configured to respond to content of a first instruction of the first plurality of sequential instructions by accessing a second plurality of sequential instructions using an address specified by the address bits.

52. (Previously Presented) The microprocessor system of claim 51 wherein the second plurality of sequential instructions is distinct from the first plurality of sequential instructions.

53. (Previously Presented) The microprocessor system of claim 51 wherein the content is an op-code.

54. (Currently Amended) The microprocessor system of claim 47 wherein the instruction register has a plurality of instruction locations ordered from a beginning instruction location to an ending instruction location, wherein the central processing unit integrated circuit is configured to respond to content in an instruction location other than the beginning instruction location by accessing the beginning instruction location.

55. (Previously Presented) The microprocessor system of claim 1 in which said microprocessor system is configured to provide different memory access timing for different storing capacity sizes of said external memory by including a sensing circuit and a driver circuit, and an output enable line connected between said external access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level after a memory read operation as a function of different capacitance on said bus as a result of the different storing capacity sizes of said external memory, said microprocessor system being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

56. (Previously Presented) The microprocessor system of claim 55 in which the predetermined electrical level is a predetermined voltage.

57. (Previously Presented) The microprocessor system of claim 1 in which said microprocessor system is configured to operate at a variable clock speed; said microprocessor system additionally comprising a ring counter variable speed system clock connected to said central processing unit integrated circuit, said central processing unit integrated circuit and said ring counter variable speed system clock being provided in a single integrated circuit, said ring counter variable speed system clock being configured to provide different clock speed to said central processing unit integrated circuit as a result of transistor propagation delays, depending on at least one of temperature of said single integrated circuit, voltage and microprocessor fabrication process for said single integrated circuit.

58. (Previously Presented) The microprocessor system of claim 57 additionally comprising an input/output interface connected between said microprocessor system and an external memory bus to exchange coupling control signals, addresses and data between said central processing unit integrated circuit and said input/output interface, and a second clock independent of said ring counter variable speed system clock connected to said input/output interface to provide clock signals for operation of said input/output interface asynchronously from said central processing unit.

59. (Previously Presented) The microprocessor system of claim 58 in which said second clock is a fixed frequency clock.

60. (Previously Presented) The microprocessor system of claim 1 in which said first push down stack has a first plurality of stack registers having stack memory elements configured as latches, a second plurality of stack registers having stack memory elements configured as a random access memory, said first and second plurality of stack registers and said central processing unit integrated circuit being provided in a single integrated circuit with a top one of said second plurality of stack registers being connected to said a bottom one of said first plurality of stack registers, and a third plurality of stack registers having stack memory elements configured as a random access memory external to said single integrated circuit, with a top one of said third plurality of stack registers being connected to a bottom one of said second plurality of stack registers, said microprocessor system being configured to operate said first, second and third plurality of stack registers hierarchically as interconnected stacks.

61. (Previously Presented) The microprocessor system of claim 60 additionally comprising a first pointer connected to said first plurality of stack registers, a second pointer connected to said second plurality of stack registers, and a third pointer connected to said third plurality of stack registers, said microprocessor system being configured to operate said first, second and third plurality of stack registers hierarchically as interconnected stacks by having said central processing unit integrated circuit being connected to pop items from said first plurality of stack registers, said first stack pointer being connected to said second stack pointer to pop a first plurality of items from said second plurality of stack registers when said first plurality of stack registers are empty from successive pop operations by said central processing unit, said second stack pointer being connected to said third stack pointer to pop a second plurality of items from said third plurality of stack registers when said second plurality of stack registers are empty from successive pop operations by said central processing unit.

62. (New) The microprocessor system of claim 9 wherein

the microprocessor system comprises an instruction register configured to store the multiple sequential instructions and from which instructions are accessed and decoded; and wherein

the means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to the central processing unit during a single memory cycle comprises supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched.

I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent and Trademark Office on January 25, 2011.

By: /Larry E. Henneman, Jr./

REMARKS

These remarks are in response to the Advisory Action dated December 16, 2010, which has a shortened statutory period for response set to expire January 28, 2010. No extension of time is required.

Claims 1-61 are pending in the above-identified reexamination proceeding. Claims 1-27 and 30-61 are subject to reexamination. Original claims 28-29 are not subject to reexamination. Claims 5-7, 13-15, 21-27, 34-39, 44, 45, and 54-61 were confirmed patentable. Claims 1-4, 8-12, 16-20, 30, 40-43, and 46-53 stand finally rejected. Proposed claims 62, depending from claim 1, and claim 63, depending from claim 9, are indicated to contain patentable subject matter. Claim 1 has been amended to incorporate the limitations of proposed claim 62. (Claim 1 had previously been amended to add "integrated circuit" after the second occurrence of "central processing unit" to correct an antecedent basis problem.) Proposed claim 63 is added as new claim 62. Claims 8, 9 and 31-33 are canceled.

The Advisory Action indicates that new claims 62 and 63 contain patentable subject matter and would be allowable if submitted with an appropriate amendment canceling the non-allowed claims. This amendment incorporates the limitations of indicated allowable claim 62 into claim 1. Indicated allowable claim 63 is renumbered as new claim 62. Independent claims 8 and 9 are cancelled. Claims 31-33 are also cancelled. Therefore, only claims including indicated allowable subject matter remain.

In his reasons for indicating the allowability of claims 62 and 63 the examiner stated:

> Regarding ***claims 62 and 63***, in the examiner's opinion, it would not have been obvious to one of ordinary skill in the art to have the system as claimed, further include the features of "supplying the multiple sequential instructions in parallel to said

> instruction register during the same memory cycle the multiple instructions fetched". **This limitation is seen to clarify the function of the current invention**, …" (emphasis added)

Patent owners' appreciate the examiner's remarks in this regard. The patent owners have consistently contended that a proper construction of the corresponding language of claims 1 and 9 is what is now expressly recited in proposed claims 62 and 63 (with the understanding that the "instruction register" is among the "corresponding structure" with respect to the means for fetching instructions). The examiner has consistently pointed out that he is obligated to construe the claims using the "broadest reasonable interpretation" standard and that using such a standard the claims could be construed so as to not be limited to this construction. Whether an amendment clarifies claim construction or modifies the scope of the claim is important in determining whether amended reexamined claims have retroactive effect under 35 USC §252. As amended, the scope of the claims under the Office's "broadest reasonable interpretation" standard now corresponds to the scope of the original issued claims as they would be properly construed outside of the Office after prosecution has been closed. Patent owners' appreciate the examiner's stated opinion that the amendment is clarifying in nature.

The amendment of claim 1 to include the indicated patentable subject matter renders all claims depending from claim 1 patentable for at least the same reasons as claim 1. Similarly, patent owners have amended all finally rejected claims that previously depended from claim 9 to depend from new claim 62 (previously claim 63), which is also indicated to be patentable. Those claims are now patentable for at least the same reasons as claim 62. Therefore, all claims subject to reexamination should be confirmable or deemed patentable.

In further detail:

Finally rejected claims 2-4, 30, 40-43 and 46-54 depend, either directly or indirectly, from claim 1. Claim 1 has been amended to include the allowable subject matter of proposed claim 62. Claims 2-4, 30, 40-43 and 46-54 are, therefore, now allowable.

Finally rejected claims 10-12, 16-18 and 19 were dependent upon canceled claim 9. These claims are currently amended to depend from indicated allowable claim 62 (previously claim 63). Claims 10-12, 16-18 and 19 are, therefore, now allowable.

Claims 5, 7, 34, 36, 44, 45, 50 and 54 depend from claim 1. They are currently amended to reflect the addition of the instruction register to claim 1.

Claim 13 now depends from claim 62. It is similarly amended to reflect the introduction of the instruction register in new claim 62.

Claim 49 is amended to recite "microprocessor system" to be consistent with the other claims.

Claims 2-4, 6, 11,12, 14-17, 20-29, 35, 37-43, 46-48, 51-53, and 55-61 are not presently amended.

All claims 1-62, save for the canceled claims 8, 9 and 31-33, are either confirmed, deemed patentable, depend from a claim that was confirmed or deemed patentable, or are not subject to re-examination.

For the foregoing reasons, Patent Owners believe all non cancelled claims subject to reexamination should be confirmed as patentable. Should the Examiner undertake any action other than confirmation of all pending claims, or if the Examiner has any questions or suggestions for expediting the prosecution of this reexamination proceeding, the Examiner is requested to contact Patent Owners' attorney at (269) 279-8820.

I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent and Trademark Office on January 25, 2011.

By: /Larry E. Henneman, Jr./

Attorney Docket No.: 0081-011X1
Merged with: 0081-011X2
Merged with: 0081-011X3

Respectfully submitted,

January 25, 2011 /Larry E. Henneman, Jr./

Date: _____ _____

Larry E. Henneman, Jr., Reg. No. 41,063
Attorney for Patent Owners(s)
Henneman & Associates, PLC
70 N. Main St.
Three Rivers, MI 49093

CERTIFICATE OF MAILING (37 CFR 1.8(A))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

January 25, 2011 /Larry E. Henneman, Jr./

Date: _____ _____

Larry E. Henneman, Jr.

EXHIBIT 28

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address : COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
07/389,334	08/03/89	MOORE	C	A50412WEH

EXAMINER
ENG, D

FLEHR, HOHBACH, TEST,
ALBRITTON & HERBERT
SUITE 3400
FOUR EMBARCADERO CENTER
SAN FRANCISCO, CA 94111

ART UNIT	PAPER NUMBER
2315	8

DATE MAILED: 12/31/92

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☒ Responsive to communication filed on 10/6/92 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire — 3 — month(s), ——— days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, Form PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 1, 3, 6-13, 16-30 and 32-70 are pending in the application.
   Of the above, claims 1, 12-13, 16-25, and 48-70 are withdrawn from consideration.
2. ☒ Claims 2, 4, 5, 14, 15 and 31 have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 3, 6-11, 26-30, 32-47 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable. ☐ not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed on _____, has been ☐ approved. ☐ disapproved (see explanation).
12. ☐ Acknowledgment is made of the claim for priority under U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____ ; filed on _____
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

15. In the communication filed on October 2, 1992, applicants elect Group II with traverse. The claims are properly restricted for the reasons set forth in the last office action.

16. In the communication, applicants stated that claim 26 serves as a linking claim and that a complete examination of claim 26 will require consideration of the art for both groups. The examiner disagrees. In considering restriction, the claims are assumed to be patentable (MPEP 806.05 (a)). The art for Group I and II is separately claimed in claim 1 and 3. In other words, each of the Group I and II does not rely on the other for patentability. In examining claim 26, it does not require to consider the detail claimed in claim 2 which is in Group I. In examining claim 13, it does not require to consider all the details claimed in claim 36. In examining claim 16, it does not require to consider all the details claimed in claim 39. In examining claim 41, it does not require to consider all the details claimed in 21. In examining claim 2, it does not require to consider all the detail claimed in claim 6. In examining claim 24, it does not require to consider all the details claimed in claim 46. In examining claim 3, it does not require to consider the detail in claim 59-62.

17. In conclusion, the independent claims which respectively and solely claim the subject matter in a group is evidence that they do not rely on the detail claimed in the combination claims (one

of the dependent claims in the set of independent claim 26) for patentability. The restriction therefore is proper.

18. The remark in line 11-13 of page 2 of the October 2 communication is not understood. Claim 22 is neither in Group II nor Group X.

19. Claim 12 is inadvertently omitted in the last office action. The error is regretted. Claim 12 should be in Group II.

20. Claims 6, 10, 11, 26-30 and 31-37 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

21. With respect to claim 6, the components (means for storing a top item, means for storing a next item and the at least one stack register) of the first push down stack as recited do not appear to render the push down stack to operate as a stack. Note that a stack is such that an inputted item propagates from one end of the stack to another via the stages in the stack. The stack as recited in the claim does not do that. Further, the claim fails to recite how the components of the stack are interconnected so as to form a stack having stages between the input and the output of the stack. The second push down stack has similar defects. Register file is not a stack.

22. Claim 6 further fails to recite how each of the means as recited functionally coacts with each other so as to achieve any

meaningful function or improvement. Although each of the means are recited to be interconnected, no meaningful coact is seen. For example, the means for storing top item of the first stack which is for providing a top item to ALU is recited for providing the same to another stack. The second stack as recited has nothing to do with arithmetic operation. It is not seen why it should receive a top item as the ALU. More example, the second stack is recited to be connected to the means for storing top item bidirectionally. However, the means for storing top item has not been recited for receiving anything from the second stack. It appears to the examiner that they should not be bidirectionally connected and controlled because the means for storing top item is part of another stack and it should receive items from the next stage of its own stack and not from another stack (the second stack).

23. Other claims (claims 27-29 and 37-38, for example) which recite stack have similar defects as claim 6.

24. In claims 10 and 33, it is not clear what is meant by "to provide a microloop in said instruction register". Note that an IR is commonly for storing instruction. Further, it is not seen how the supplying of control/reset signals to counters would provide a microloop in an instruction register.

25. Function of the counter as recited in claims 11 and 34 is not clear. It is not seen how the counter which is recited for

controlling supply of instructions can select variable width operand. Further, claims 11 fails to recite where the variables width operand is stored.

26. In claim 26, function of the multiplexing means is not clear. A multiplexer which is commonly for multiplexing is recited to provide different types of data on a bus. Where do the row addresses, column addresses and data come from and go to?

27. In claim 35, function of the means for fetching is not clear. A fetching means which is commonly for fetching is erroneously recited for assembly and storing instructions.

28. In claim 39, it is not clear what is meant by "different memory access timing for different sizes of DRAM". Is it referring to different storing capacity sizes, to different amount of instructions accessed at a time or to different physical sizes? Further with respect to claim 39, it is not seen how the sensing circuit and the driver circuit as recited can render the microprocessor to provide different sizes of DRAM.

29. Claim 41 is not understood. It is not clear what is meant by "ring counter -- to provide different clock speed -- depending on at least one of temperature, voltage and microprocessor fabrication process --". How does the clock response to the temperature, voltage and microprocessor fabrication process?

30. In claim 42, what is meant by "I/O interface -- to exchange -- signals -- with said I/O interface --"? What is

connected to the I/O interface and exchange with who? Claim 42 further fails to recite how the clock and the I/O interface functionally coact with each other so as to perform any meaningful operation.

31. Claims 44 and 45 fail to recite function of each of the elements recited therein and how they are functionally coact with each other such that desired result can be achieved.

32. Claims 37-38 are rejected under 35 USC 112 and objected to under 37 CFR 1.75 (b) as unduly multiplied.

33. Claims 37-38 are almost identical to parent claim 27-29.

34. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

35. Claims 3, 6-10, 26-30 and 32-33 are rejected under 35 U.S.C. § 103 as being unpatentable over Takahira.

36. See at least Figure 2 and the corresponding description in

the specification of Takahira. The drawing shows a data processing system having a CPU, memory, EEPROM, RAM, ROM, clock circuit, register file, status register, index register X and Y, program counter H and L for fetching instructions, ALU, accumulator, stacks and stack pointer, instruction register, instruction decoder and a bus. With respect to claim 3, Takahira does not specify how many instructions can be fetched per memory cycle.

One of ordinary skill in the art should readily recognize that, for the same machine, more instructions can be fetched if the memory cycle is extended longer. How long a memory cycle should be is merely a matter of design choice because it is dependent on the speed of the elements used and on the engineering design.

37. With respect to claim 7, one of ordinary skill in the art should readily recognize that for the same given amount of time more instructions can be fetched if the previous instruction is not a memory instruction because it is well known that a memory instruction takes longer time to executed.

38. With respect to claim 10, looping is well known in programming art. One of ordinary skill in the art should readily recognize that the processing system of Takahira as shown in Figure 2 is capable of looping because it also has program counters.

39. Claims 11 and 34 are rejected under 35 U.S.C. § 103 as being unpatentable over Takahira in view of Heath.

40. Takahira discloses claim combination set forth above. Takahira does not state whether his operand is of variable length. Heath shows such in lines 31 et seq. of column 5. It would have been obvious to make Takahira's operand variable length because it would be more flexible.

41. Claim 35 ~~is~~ and 12 are rejected under 35 U.S.C. § 103 as being unpatentable over Takahira and Heath in view of Bruinhorst.

42. Takahira and Heath disclose claim combination set forth above. Takahira does not state whether his program in PROM is transferred to RAM. Such is well known in the art as shown by Bruinhorst in lines 43 et seq. of column 15. It would have been obvious to load from PROM to RAM in Takahira as taught by Bruinhorst because it is more flexible in programming.

43. Claims 36, 37 and 38 are rejected under 35 U.S.C. § 103 as being unpatentable over Takahira, Heath, Bruinhorst further in view of Derchak.

44. Takahira, Heath and Bruinhorst disclose claim combination set forth above. Takahira does not show a DMA. DMA is well known in the art. Derchak shows such. It would have been obvious to a person of ordinary skill in the art to incorporate a DMA as taught by Derchak in Takahira because that would render Takahira's system more efficient.

45. Claims 39 and 40 are rejected under 35 U.S.C. § 103 as being unpatentable over Takahira, Heath, Bruinhorst, Derchak further in view of Kimoto.

46. Takahira does not state whether his microprocessor is capable of accessing the memory at a desired variable access time. Such is well known in the art as shown by Kimoto. It would have been obvious to a person of ordinary skill in the art to access the memory of Takahira as taught by Kimoto because the system of Takahira would run more efficiently.

47. Claims 41-45 are rejected under 35 U.S.C. § 103 as being unpatentable over Takahira, Heath, Bruinhorst, Derchak, Kimoto further in view of ~~Kimoto~~ Martin.

48. Takahira does not state whether his clock is of variable clock rate. Variable rate clock is well known in the art. ~~Kimoto~~ Martin shows such. (Fajcon) It would have been obvious to a person of ordinary skill in the art to incorporate a variable speed clock in Takahira's system if the circuits require.

49. With respect to claims 42-43, Takahira shows an I/O interface 13 in Figure 2.

50. Claims 46 and 47 are allowable if the 35 USC 112, second paragraph rejection is overcome.

51. Applicant's arguments with respect to claims 3, 6-11 and 26-30 and 32-45 have been considered but are deemed to be moot in view of the new grounds of rejection.

52. The prior art cited on July 10, 1992 has not been considered because the class and subclass information is missing.

Any inquiry concerning this communication should be directed to David Eng at telephone number (703) 308-1635.

DAVID Y. ENG
PRIMARY EXAMINER
ART UNIT 232

DE/kw
December 29, 1992

EXHIBIT 29

10/B

PATENT

7/28/93 mc

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: David Y. Eng
CHARLES H. MOORE ET AL.	Group Art Unit: 2302
Serial No. 07/389,334	San Francisco, CA
Filed: August 3, 1989	
For: HIGH PERFORMANCE, LOW COST MICROPROCESSOR	

11/28/93 mc

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, DC 20231 on June 30, 1993.

Signed: _____

AMENDMENT

Commissioner of Patents
and Trademarks
Washington, D.C. 20231

Sir:

In response to the Office Action dated December 31, 1992, please amend the above application as follows:

In the Claims:

Rewrite claims 3, 6, 7, 10, 11, 26, 27, 29, 30, 33, 34, 35, 36, 39, 41, 42, 44 and 45 as follows:

Sub C1

3(Twice Amended). A microprocessor system, comprising a central processing unit, a memory, a bus connecting said central processing unit to said memory, and means connected to said bus for fetching instructions for said central processing unit on said bus from said memory, said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit during a single memory cycle.

6(Twice Amended). The microprocessor system of Claim 3 in which said central processing unit includes an arithmetic logic unit and a first push down stack connected to said arithmetic logic unit, said first push down stack further including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input, means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input, [and at least one stack register connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack,] said arithmetic logic unit having an output connected to said means for storing a top item, a second push down stack, said means for storing a top item being connected to provide an input to said second push down stack and a control means connected between said means for storing a top item and said second push down stack for controlling provision of the input to said second push down stack, said second push down stack [comprises] additionally being configured as a register file and said means for storing a top item and said second push down stack additionally configured as the register file are bidirectionally connected.

21(Amended). The microprocessor system of Claim 1 additionally comprising means connected to said means for fetching multiple instructions for determining by decoding the multiple instructions if multiple instructions fetched by said means for fetching multiple instructions require a memory access, said means for fetching multiple instructions fetching additional multiple instructions if decoding the multiple instructions shows that the multiple instructions do not require a memory access.

~~10~~(Twice Amended). The microprocessor system of Claim ~~9~~ additionally comprising a loop counter connected to receive a decrement control signal from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and the decrement control signal to said loop counter in response to a MICROLOOP instruction in the multiple instructions to provide a microloop within the multiple instructions in said instruction register for a number of repetitions controlled by said loop counter.

~~11~~(Amended). The microprocessor system of Claim ~~3~~ additionally comprising an instruction register for the multiple instructions and a variable width operand to be used with one of the multiple instructions connected to said means for fetching instructions, means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession,

means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions, said counter being connected to said means for decoding to receive incrementing and reset control signals from said means for decoding, said means for decoding being configured to control said counter in response to an instruction utilizing [a] the variable width operand stored in said instruction register, and means connected to said counter to select the variable width operand for use with the instruction utilizing the variable width operand in response to said counter.

26(~~Twice Amended~~). ~~A microprocessor system, comprising a central~~ processing unit, a dynamic random access memory, a bus connecting said central processing unit to said dynamic random access memory, and multiplexing means on said bus between said central processing unit and said dynamic random access memory, said multiplexing means being connected and configured to provide multiplexed row addresses, column addresses and data on said bus from said central

processing unit to said dynamic random access memory and to provide data from said dynamic random access memory to said central processing unit, and

means connected to said bus for fetching instructions for said central processing unit on said bus from said dynamic random access memory, said means for fetching instructions being configured to fetch multiple sequential instructions from said dynamic random access memory in parallel and supply the multiple instructions to said central processing unit during a single memory cycle.

10
~~27~~(Twice Amended). The microprocessor system of Claim ~~26~~ in which said central processing unit includes an arithmetic logic unit and a first push down stack connected to said arithmetic logic unit, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input, and means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input, [and at least one] a remainder of said first push down stack [register] being connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack, said arithmetic logic unit having an output connected to said means for storing a top item.

11 ~~12~~ ~~29~~(Amended). The microprocessor system of Claim ~~28~~ 10 in which said second push down stack [comprises] is additionally configured as a register file and said means for storing a top item and said second push down stack additionally configured as the register file are bidirectionally connected.

12 ~~13~~ ~~30~~(Amended). The microprocessor system of Claim ~~29~~ 11 additionally comprising means connected to said means for fetching multiple instructions for determining by decoding the multiple instructions if multiple instructions fetched by said means for fetching multiple instructions require a memory access, said means for fetching multiple instructions fetching additional multiple instructions if decoding the multiple instructions shows that the multiple instructions do not require a memory access.

14 ~~15~~ ~~14~~ 13

~~33~~(Amended). The microprocessor system of Claim ~~32~~ additionally comprising a loop counter connected to receive a decrement control signal from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and the decrement control signal to said loop counter in response to a MICROLOOP instruction in the multiple instructions within the multiple instructions in said instruction register for a number of repetitions controlled by said loop counter.

34(Twice Amended). The microprocessor system of Claim 33 in which said means for decoding is configured to control said counter in response to [an instruction] one of the multiple instructions utilizing a variable width operand stored in said instruction register with the multiple instructions, said microprocessor system additionally comprising means connected to said counter to select the variable width operand for use with the instruction utilizing the variable width operand in response to a state of said counter resulting from control of said counter by said means for decoding.

35(Amended). The microprocessor system of Claim 34 additionally comprising a programmable read only memory containing instructions connected to said bus, means connected to said bus for fetching instructions for said central processing unit on said bus, said means for fetching instructions including means for assembling a plurality of instructions from said programmable read only memory, [and] storing the plurality of instructions in said dynamic random access memory and subsequently supplying the plurality of instructions from said dynamic random access memory to said central processing unit on said bus.

36(Amended). The microprocessor system of Claim 35 additionally comprising a direct memory access processing unit having the capacity to fetch and execute instructions, said bus connecting said direct memory access processing unit to said dynamic random access memory, said dynamic random access memory containing instructions for said central processing unit and said direct memory access processing unit, said direct memory access processing unit including means

for fetching instructions for said central processing unit on said bus and for fetching instructions for said direct memory access processing unit on said bus.

39(Twice Amended). The microprocessor system of Claim [38] 36 in which said microprocessor system is configured to provide different memory access timing for different storing capacity sizes of said dynamic random access memory by including a sensing circuit and a driver circuit, and an output enable line connected between said dynamic random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level after a memory read operation as a function of different capacitance on said bus as a result of the different storing capacity sizes of said dynamic random access memory, said microprocessor system being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

41(Twice Amended). The microprocessor system of Claim 40 in which said microprocessor system is configured to operate at a variable clock speed, said microprocessor system additionally comprising a ring counter variable speed system clock connected to said central processing unit, said central processing unit and said ring counter variable speed system clock being provided in a single integrated circuit, said ring counter variable speed system clock being configured to provide different clock speed to said central processing unit as a result of transistor propagation delays, depending on at least one of temperature of said single integrated circuit, voltage and microprocessor fabrication process for said single integrated circuit.

~~42~~(Amended). The microprocessor system of Claim ~~41~~ additionally comprising an input/output interface connected between said microprocessor system and an external memory bus to exchange coupling control signals, addresses and data [with] between said central processing unit and said input/output interface, and a second clock independent of said ring counter variable speed system clock

connected to said input/output interface to provide clock signals for operation of said input/output interface asynchronously from said central processing unit.

44(Twice Amended). The microprocessor system of Claim 43 in which said first push down stack has a first plurality of stack registers having stack memory elements configured as latches, a second plurality of stack registers having stack memory elements configured as a random access memory, said first and second plurality of stack registers and said central processing unit being provided in a single integrated circuit with a top one of said second plurality of stack registers being connected to said a bottom one of said first plurality of stack registers, and a third plurality of stack registers having stack memory elements configured as a random access memory external to said single integrated circuit, with a top one of said third plurality of stack registers being connected to a bottom one of said second plurality of stack registers, said microprocessor system being configured to operate said first, second and third plurality of stack registers hierarchically as interconnected stacks.

~~45~~(Twice Amended). The microprocessor system of Claim ~~44~~ additionally comprising a first pointer connected to said first plurality of stack registers, a second pointer connected to said second plurality of stack registers, and a third pointer connected to said third plurality of stack registers, said microprocessor system being configured to operate said first, second and third plurality of stack registers hierarchically as interconnected stacks by having said central processing unit being connected to pop items from said first plurality of stack registers, said first stack pointer being connected to said second stack pointer to pop a first plurality of items from said second plurality of stack registers when said first plurality of stack registers are empty from successive pop operations by said central processing unit, said second stack pointer being connected to said third stack pointer to pop a second plurality of items from said third plurality of stack registers when said second plurality of stack registers are empty from successive pop operations by said central processing unit.

Cancel claims 37-38.

Add the following new claims:

3-~~71~~. The microprocessor system of Claim ~~7~~ 2 in which the decoding determines if the multiple instructions do not require a memory access by a state of a bit of each of the multiple instructions.

~~72~~ 4. The microprocessor system of Claim ~~71~~ 3 in which the bit is a most significant bit of the multiple instructions.

~~73~~ 16 ~~17~~. The microprocessor system of Claim ~~30~~ 12 ~~13~~ in which the decoding determines if the multiple instructions do not require a memory access by a state of a bit of each of the multiple instructions.

~~74~~ 17 ~~18~~. The microprocessor system of Claim ~~73~~ 16 ~~17~~ in which the bit is a most significant bit of the multiple instructions.

~~75~~ 20 ~~21~~. The microprocessor system of Claim ~~36~~ 19 ~~20~~ additionally comprising a variable speed system clock connected to said central processing unit and a fixed speed system clock connected to control said means for fetching instructions for said central processing unit and for fetching instructions for said direct memory access processing unit.--.

B13

REMARKS

Claims 3, 6-11, 26-30 and 32-47 are presently under examination in the application. The allowability of claims 46 and 47, if amended to overcome the rejection under 35 U.S.C. § 112, is noted. Claims 37-38 have been canceled to advance the prosecution of the application.

Claims 6, 10, 11, 26-30 and 31-37 were rejected under 35 U.S.C. § 112 as indefinite. In response, claims 6, 10, 11, 26, 27, 29, 34, 35, 39, 41, 42, 44 and 45 have been rewritten to define the invention with more particularity.

In claim 6, the first push down stack is now recited as further including the means for storing a top item connected to a first input of the arithmetic logic unit to provide the top item to the first input and the means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input. Thus, as the Examiner correctly notes, these items do not render the first push down stack to operate as a stack. These items are in addition to the conventional construction of the first push down stack which allow it to operate as a stack. Similarly, the second push down stack is now recited as additionally being configured as a register file. In both cases, the recited language is in addition to conventional organization of the stacks which allow them to operate as stacks.

The Examiner is correct that a register file is not a stack. However, a stack which posses an organization which emulates registers is still a stack. Such an organization conveys the benefits of both stacks and registers while avoiding the limitations of either. Since the elements of both stacks that allow them to operate as stacks are conventional, they have not been recited beyond specifying these elements as being push down stacks.

The recited structure of claim 6 permits use of the technique of placing local variables on the stack, which allows automatic nesting of procedures and their local variables, simply by pushing new variables on the stack to allocate new space.

The two stacks as now claimed serve distinct functions. The first push down stack is exemplified by the stack 74 in Figures 2 and 13. The stack 74 in fact allows arithmetic operations to be carried out on operands supplied from it to the ALU and receives ALU results as a result of the recited connections.

The second push down stack is exemplified by the stack 134 in Figures 2 and 13. The RSTACK 134 stores return addresses for subroutine nesting as well as local storage for subroutines.

The defined relationship between the two stacks is that they are linked to a bidirectional buffer, which allows the stacks to exchange individual contents. Two instructions, POP-STACK-PUSH-RSTACK and POP-RSTACK-PUSH-STACK,

move the top items of one stack to the top item of the other. WRITE-LOCAL-VARIABLE and READ-LOCAL-VARIABLE write or read the top arithmetic stack item to the local variables stored on the RSTACK 134.

The underlying rationale for using two stacks is to remove the processing bottleneck found in single stack machines. This much is taught, for example, by the Moore et al prior art U.S. Patent 5,070,451, discussed in the Information Disclosure Statement of record. Those familiar with languages like FORTH which make extensive use of the dual stack concept are comfortable with the dual stack arrangement. The addition of a register array embedded in the second stack as claimed eliminates the stack machine problem of either storing local variables on the stack or in off-chip memory. Storing local variables on either stack becomes very clumsy with prior art dual stacks once the number of variables exceeds three. Off-chip variables access far slower than on-chip registers.

Similarly, claims 27-29 have been rewritten to specify that the first push down stack functions both to supply operands to and receive results from the ALU, as well as being a conventional push down stack. The second push down stack is also now specified as operating both as a register file and as a conventional push down stack.

Claims 10 and 33 have been rewritten to require that the MICROLOOP instruction in the multiple instructions provide a microloop within the multiple instructions in the instruction register and that the loop counter controls the number of repetitions of the microloop. It is believed that the provision of the microloop and the function of the loop counter are now clear.

Claims 11 and 34 have been rewritten to specify that the variable width operand is stored in the instruction register and that the variable width operand is selected for use with the instruction utilizing the variable width operand in response to the counter. As is explained at page 33 of the specification with reference to Figure 20, the instruction decoder tests the counter to determine the position of a JUMP op-code in the four instruction group and assumes that the remaining bits in the instruction group are the JUMP operand. Since the JUMP instruction's position in the four instruction group determines the length of the operand, a single JUMP op-

code may have three different length operands. With these amendments, the function of the counter in these claims is now believed to be clear.

Claim 26 has been rewritten to specify that the multiplexer provides multiplexed row addresses, column addresses and data on the bus from the central processing unit to the dynamic random access memory and data from the dynamic random access memory to the central processing unit. The instructions are now specified as being from the dynamic random access memory. The function of the multiplexer is now believed to be clear, and the locations from which the row addresses, column addresses, data and instructions come are now specified.

Claim 35 has been rewritten to specify that the means for fetching instructions includes means for assembling a plurality of instructions from the programmable read only memory, storing the plurality of instructions in the dynamic random access memory and subsequently supplying the plurality of instructions from the dynamic random access memory to the central processing unit on said bus. Thus, it is now clear that the means for fetching instructions is capable of fetching a plurality of instructions because it also includes a means for assembling the plurality of instructions from the programmable read only memory and storing the plurality of instructions in the random access memory, from which they are supplied to the central processing unit. The function of the means for fetching is now believed to be clear.

Claim 39 now specifies different storing capacity sizes of the dynamic random access memory and that the ready signal is provided when the output enable line reaches a predetermined electrical level after a memory read operation as a function of different capacitance on the bus as a result of the different storing capacity sizes of the dynamic random access memory. The different sizes of DRAM and the ability of the system to provide different memory timing for the different sizes of DRAM is now believed to be clear.

Claim 41 now specifies that the ring counter variable speed system clock is configured to provide different clock speed to the central processing unit as a result of transistor propagation delays, depending on at least one of temperature, voltage and microprocessor fabrication process for the single integrated circuit. The clock thus indirectly responds to temperature, voltage and microprocessor fabrication

process by responding to transistor propagation delays, which are determined by those parameters. Claim 41 is therefore believed to be clarified.

Claim 42 now recites an input/output interface connected between the microprocessor system and an external memory bus to exchange coupling control signals, addresses and data between the central processing unit and the input/output interface. The claim now further calls for a second clock independent of the ring counter variable speed system clock connected to the input/output interface to provide clock signals for operation of the input/output interface asynchronously from the central processing unit. It is therefore believed that the function of the input/output interface is now clear and the function of the second clock to allow asynchronous operation of the input/output interface with respect to the central processing unit has been clarified.

Claims 44 and 45 have been rewritten to specify the interconnections among the first, second and third plurality of stack registers and to specify that the microprocessor system is configured to operate the first, second and third plurality of stack registers hierarchically as interconnected stacks. It is believed that these claims now recite the function of the elements and how they functionally coact with one another to achieve a desired result.

Based on the above changes to the claims and remarks, it is believed that all of the claims are now definite in form. The rejection of claims 6, 10, 11, 26-30 and 31-37 under 35 U.S.C. § 112 is believed to be overcome.

Claims 3, 6-10, 26-30 and 32-33 were rejected under 35 U.S.C. § 103 as unpatentable over Takahira et al., U.S. Patent 5,036,460. In response, in addition to the above-discussed changes to the claims, claims 3, 7, 26 and 30 have been rewritten to define the invention better over the prior art, and new claims 71-74 have been added to provide more complete protection for the invention. This rejection is believed to be overcome by the above changes to the claims and the following remarks.

Claim 3 has been rewritten to specify that the means for fetching is configured and connected to fetch multiple sequential instructions from the memory in parallel and to supply the multiple sequential instructions to the central processing unit during a single memory cycle. A system including such a means for fetching is

not taught or suggested by Takahira et al. Takahira et al. disclose only the parallel movement of data within a memory, solely for the purpose of writing to an EEPROM. The system of claim 3 is a low-cost technique which allows balancing a very fast CPU with a very slow memory to produce a fast computing system.

In the rejection, the Examiner argues that it would be obvious to extend the memory cycle in Takahira et al. to allow multiple instruction fetching. This argument misunderstands the subject matter of the claim. As claimed, the multiple instructions are fetched in parallel during a single memory cycle. Because they are fetched in parallel, no substantial extension of the memory cycle is required to fetch the multiple instructions. Even if the Examiner is correct that it would be obvious to extend a memory cycle to allow multiple instruction fetching, doing so as posited by the Examiner would not give the claimed subject matter.

The rejection contains no separate discussion of the subject matter of claim 6. The above clarifying changes made to that claim and remarks with respect to the § 112 rejection also make it clear that the subject matter of claim 6 is not suggested by Takahira et al. That reference contains no teaching or suggestion of dual stacks which are operable as both stacks and registers.

Claims 7 and 30 have been rewritten to require determining by decoding the multiple instructions if multiple instructions fetched by the means for fetching multiple instructions require a memory access. Making the determination in this manner means that it can be done in 2.5 nanoseconds in the described embodiment, as pointed out at page 38, line 19 of the specification. No such determination, whether or not done by decoding, is taught or suggested by Takahira et al. New claims 71-74 provide further details on how the decoding is carried out, and are also not taught or suggested by Takahira et al.

Claim 9 adds structure to the microprocessor system of claim 3 to handle SKIP instructions. Claim 32 adds the same structure to the microprocessor system of claim 30. Takahira et al. contains no teaching of how SKIP instructions are handled in the system there disclosed.

Claim 10 adds to the microprocessor system of claim 9 a loop counter for controlling the number of repetitions of a microloop within the multiple instructions. In the rejection of this claim, the Examiner equates the loop counter to the program

counter in Takahira et al, used for controlling software looping. In fact, claim 10 is directed to a hardware accelerator for microloop repetition and is not suggested by a conventional program counter to control software looping.

Claim 26 includes the fetching of multiple sequential instructions from the memory in parallel and supplying the multiple sequential instructions to the central processing unit during a single memory cycle as in claim 3 and the provision of a multiplexed bus connected between the memory and the central processing unit for supplying addresses and data between the central processing unit and the memory. No such combination is shown or suggested by Takahira. The above comments with respect to the rejection of claim 6 are equally applicable to the subject matter added to the microprocessor system by claim 29. The above comments with respect to the rejection of claim 10 are equally applicable to the subject matter added to the microprocessor system by claim 33.

Based on the above changes to the claims and remarks, the rejection of claims 3, 6-10, 26-30 and 32-33 under 35 U.S.C. § 103 as unpatentable over Takahira et al. is believed to be overcome.

Claims 11 and 34 were rejected under 35 U.S.C. § 103 as unpatentable over Takahira et al. in view of Heath, U.S. Patent 3,603,934. The above remarks with respect to the rejection of claim 3 are equally applicable to the rejection of claim 11. The above amendments to these claims clarify the function of the counter in these claims to control selection of the variable width operand by determining the position of the instruction utilizing the variable width operand. The bare mention of variable width operands in Heath fails to teach or suggest the subject matter added to the microprocessor system by claims 11 and 34. This rejection is believed to be overcome.

Claims 12 and 35 were rejected under 35 U.S.C. § 103 as unpatentable over Takahira et al. and Heath in view of Bruinshorst, U.S. Patent 4,376,977. The loading of instructions from a PROM to RAM as disclosed by Bruinshorst fails to teach or suggest the use of a bus in unmultiplexed form for reading instructions from a PROM and the dynamic reconfiguration of the same bus to multiplexed form for row addresses, column addresses and data during the transmission of the instructions to the RAM, as recited in claim 12. The above remarks with respect to

the rejections of claims 34, 33, 32, 30, 29, 28, 27 and 26 are equally applicable to the rejection of claim 35. The rejection of claims 12 and 35 is therefore believed to be overcome.

Claims 36, 37 and 38 were rejected under 35 U.S.C. § 103 as unpatentable over Takahira et al., Heath, Bruinshorst, further in view of Derchak, U.S. Patent 4,067,059. In response, claim 36 has been rewritten to distinguish the invention better over the prior art. Claims 37-38 have been canceled to advance the prosecution of the application. New claim 75 has been added to provide more complete protection for the invention. The above comments with respect to the rejections of claims 35, 34, 33, 32, 30, 29, 28, 27 and 26 are equally applicable to this rejection.

As described at page 15, lines 8-11, claim 36 has been rewritten to specify that the direct memory access processing unit is capable of fetching and executing instructions. Like the central processing unit, it is therefore also a stored program processing unit. In making the rejection, the Examiner has equated the subject matter added to the system by claim 36 to direct memory access, as shown by Derchak. However, as pointed out by Derchak at column 1, lines 29-39, conventional direct memory access controllers do not have the capability to fetch their own instructions, as required by rewritten claim 36. Instead, instructions and data necessary for the direct memory access controller are supplied to the direct memory access controller by the central processing unit. The Derchak patent deals with the sharing of a direct memory access controller among multiple peripherals, and there is no indication that the direct memory access controllers in Derchak have the capability to fetch their own instructions, as claimed.

New claim 75 further distinguishes from these references by specifying a variable speed system clock for the central processing unit and a fixed speed system clock connected to control the means for fetching instructions for said central processing unit and for fetching instructions for said direct memory access processing unit, as shown in Figure 17.

The system of claim 75 allows a division of computing work between that which is real-time (I/O) and that which is not (everything else). Real-time

computing work is driven either by time or external events. The crystal clock in Figure 17 is the time base for the I/O interface 432.

Everything else, such as calculating, sorting and performing logical operations, is by nature asyncronous with the real world. The optimal implementation for such computing work is whatever produces results faster. The variable speed clock for the CPU 70 in Figure 17 clocks execution as fast as possible, given the voltage, temperature and process parameters of the CPU, without having to be concerned with slowing down for I/O considerations.

The invention of claim 75 achieves efficiencies by dividing the real-time component of the direct memory access processing unit from the non-real time component of the central processing unit. In this system, two processors with independent instruction streams, independent program counters and even independent instruction sets coexist in a loosely coupled fashion, synchronizing only when necessary to exchange information.

If the CPU clock were the same as the direct memory access clock, CPU instructions would have to be slowed down to less than their fastest speed, because, while the operation of a crystal is near constant over voltage and temperature, the operation of transistors is not. If the direct memory access clock were the same as the variable speed CPU clock, no time precise direct memory access could be performed because no time standard would exist.

For these reasons, an independent basis for patentability of new claim 75 over this prior art is present. Based on the above changes to claim 36 and remarks, its rejection under 35 U.S.C. § 103 is believed to be overcome.

Claims 39 and 40 were rejected under 35 U.S.C. § 103 as unpatentable over Takahira et al., Heath, Bruinshorst, Derchak, further in view of Kimoto et al., U.S. Patent 4,870,562. The above comments with respect to the rejection of claim 36 are equally applicable to this rejection. Claim 39 has been rewritten to make it clear that the different memory access timing is provided for different storing capacity sizes of the dynamic random access memory as a function of different capacitance on the bus as a result of the different storing capacity sizes of the dynamic random access memory. No such operation is suggested by Kimoto et al. Kimoto et al. involves executing instructions at faster speeds when fetched from on-

board memory and slower speeds when fetched from external memory. This is essentially an instruction cache patent and has nothing to do with sensing memory expansion by measuring capacitance attached to a memory bus, as claimed. The rejection of claims 39 and 40 is believed to be overcome.

Claims 41-45 were rejected under 35 U.S.C. § 103 as unpatentable over Takahira et al., Heath, Bruinshorst, Derchak, Kimoto et al., further in view of Martin. The above remarks with respect to the rejection of claims 39 and 40 are equally applicable to this rejection. Additionally, claim 41 has been rewritten to require that the ring counter variable speed system clock provide a different clock speed to the central processing unit as a result of transistor propagation delays depending on temperature of the integrated circuit containing the microprocessor system.

The Martin patent is directed to a similar problem as claims 41-45, but an external temperature sensor measures ambient temperature, which is at best only an indirect approximation of the integrated circuit temperature. In claim 41, the ring counter in the integrated circuit serves as a direct measure of propagation delays, which are a function of the integrated circuit temperature. No such direct measurement of integrated circuit temperature is contemplated by Martin, nor is varying clock speed on the basis of voltage or integrated circuit fabrication process, the other two factors recited in claim 41. The above comments with respect to the rejection of claim 36 and the subject matter of new claim 75 are applicable to the rejection of claims 42-43. None of these references teach or suggest the hierarchically interconnected stack registers of claims 44-45. The rejection of claims 41-45 is believed to be overcome.

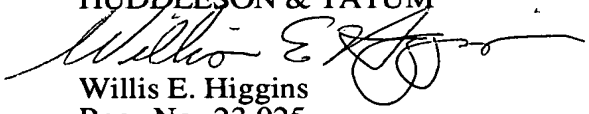
In the Office Action, the Examiner indicates that the references cited in the Information Disclosure Statement have not been considered because the class and subclass information for the references was not supplied. In response, PTO Form 1449 is being resubmitted to include this information. Applicants note that copies of the references were included with the Information Disclosure Statement, and it is therefore not clear why the class and subclass information was necessary to consider these references.

A three-month extension of time to reply to the Office Action is requested. A check for $420.00 to cover the fee for this extension is enclosed. Please charge any additional extension of time fee or credit any overpayment to Deposit Account No. 03-3117(Order No. NANO-001US). A copy of this page is enclosed for charging purposes.

All of the claims in the application are believed to be patentable over the prior art. This application is believed to be in condition for allowance, and allowance is solicited.

Respectfully submitted,

COOLEY GODWARD CASTRO
HUDDLESON & TATUM



Willis E. Higgins
Reg. No. 23,025

Five Palo Alto Square
Fourth Floor
Palo Alto, California 94306-2155
Telephone: (415) 843-5145

EXHIBIT 30

20/1D

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
CHARLES H. MOORE ET AL.
Serial No. 07/389,334
Filed: August 3, 1989
For: HIGH PERFORMANCE, LOW COST MICROPROCESSOR

Examiner: David Y. Eng
Group Art Unit: 2302
Palo Alto, CA

NOV 10 1994

AMENDMENT

Commissioner of Patents
and Trademarks
Box AF
Washington, D.C. 20231

OFFICIAL

Sir:

In response to the Office Action dated June 9, 1994, please amend the above application as follows:

In the Claims:

Rewrite claim 3 as follows:

3(Four Times Amended). A microprocessor system, comprising a central processing unit integrated circuit, a memory external of said central processing unit integrated circuit, a bus connecting said central processing unit integrated circuit to said memory, and means connected to said bus for fetching instructions for said central processing unit integrated circuit on said bus from said memory, said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle, said bus having a width at least equal to a number of bits in each of the instructions times a number of the instructions fetched in parallel, said central

NANO-001US
Resp. to 5th. O.A.

84

processing unit including an arithmetic logic unit and a first push down stack connected to said arithmetic logic unit, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input, and means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input, a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack, said arithmetic logic unit having an output connected to said means for storing a top item.

D1

13 ~~14~~ 15 ~~16~~ ~~34~~(Three Times Amended). The microprocessor system of Claim [33] ~~32~~ in which said means for decoding is configured to control said counter in response to one of the multiple instructions utilizing a variable width operand stored in said instruction register with the multiple instructions, said microprocessor system additionally comprising means connected to said counter to select the variable width operand for use with the instruction utilizing the variable width operand in response to a state of said counter resulting from control of said counter by said means for decoding.

D2

~~18~~ 4 ~~19~~ ~~35~~(Twice Amended). The microprocessor system of Claim [34] ~~27~~ additionally comprising a programmable read only memory containing instructions connected to said bus, means connected to said bus for fetching instructions for said central processing unit on said bus, said means for fetching instructions including means for assembling a plurality of instructions from said programmable read only memory, storing the plurality of instructions in said dynamic random access memory and subsequently supplying the plurality of instructions from said dynamic random access memory to said central processing unit on said bus.

D3

19 ~~20~~ 9 ~~10~~ ~~36~~(Twice Amended). The microprocessor system of Claim [35] ~~27~~ additionally comprising a direct memory access processing unit having the capacity to [fetch] request and execute instructions, said bus connecting said direct memory access processing unit to said dynamic random access memory, said dynamic

D3

random access memory containing instructions for said central processing unit and said direct memory access processing unit, said direct memory access processing unit [including] being connected to means for fetching instructions for said central processing unit on said bus and for fetching instructions for said direct memory access processing unit on said bus.

D4

21 ~~22~~ ~~39~~(Three Times Amended). The microprocessor system of Claim [36] ~~27~~ 10 9 in which said microprocessor system is configured to provide different memory access timing for different storing capacity sizes of said dynamic random access memory by including a sensing circuit and a driver circuit, and an output enable line connected between said dynamic random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level after a memory read operation as a function of different capacitance on said bus as a result of the different storing capacity sizes of said dynamic random access memory, said microprocessor system being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

D5

23 ~~25~~ ~~41~~(Three Times Amended). The microprocessor system of Claim [40] ~~27~~ 10 9 in which said microprocessor system is configured to operate at a variable clock speed, said microprocessor system additionally comprising a ring counter variable speed system clock connected to said central processing unit, said central processing unit and said ring counter variable speed system clock being provided in a single integrated circuit, said ring counter variable speed system clock being configured to provide different clock speed to said central processing unit as a result of transistor propagation delays, depending on at least one of temperature of said single integrated circuit, voltage and microprocessor fabrication process for said single integrated circuit.

D6

26 ~~27~~ ~~44~~(Three Times Amended). The microprocessor system of Claim [43] ~~27~~ 10 9 in which said first push down stack has a first plurality of stack registers having stack memory elements configured as latches, a second plurality of stack registers

NANO-001US
Resp. to 5th. O.A.

fc.

having stack memory elements configured as a random access memory, said first and second plurality of stack registers and said central processing unit being provided in a single integrated circuit with a top one of said second plurality of stack registers being connected to said a bottom one of said first plurality of stack registers, and a third plurality of stack registers having stack memory elements configured as a random access memory external to said single integrated circuit, with a top one of said third plurality of stack registers being connected to a bottom one of said second plurality of stack registers, said microprocessor system being configured to operate said first, second and third plurality of stack registers hierarchically as interconnected stacks.

~~46~~(Amended). The microprocessor system of Claim [45] ~~27~~ additionally comprising a first register connected to supply a first input to said arithmetic logic unit, a first shifter connected between an output of said arithmetic logic unit and said first register, a second register connected to receive a starting polynomial value, an output of said second register being connected to a second shifter, a least significant bit of said second register being connected to said arithmetic logic unit, a third register connected to supply feedback terms of a polynomial to said arithmetic logic unit, a down counter, for counting down a number corresponding to digits of a polynomial to be generated, connected to said arithmetic logic unit, said arithmetic logic unit being responsive to a polynomial instruction to carry out an exclusive OR of the contents of said first register with the contents of said third register if the least significant bit of said second register is a "ONE" and to pass the contents of said first register unaltered if the least significant bit of said second register is a "ZERO", until said down counter completes a count, the polynomial to be generated resulting in said first register.

Cancel claims 1, 12-13, 16-26, 48-70 and 76-77.

REMARKS

Appreciation is expressed for the courteous and helpful interview granted by the Examiner in this application on October 25, 1994. The above changes to

NANO-001US
Resp. to 5th. O.A.

claim 3 were discussed at the interview. Other proposed changes to claim 26 and an alternative amendment to claim 3 were also discussed, but those changes will be made in a successor application, because the Examiner stated that they would raise new issues after the final rejection. The Examiner reserved judgment on whether the above changes to claim 3 would raise a new issue after the final rejection. Claims 1, 12-13, 16-25 and 48-70 have been canceled as drawn to non-elected inventions, subject to inclusion in a successor application. Claims 76-77 have been canceled to advance the prosecution of the application, subject to inclusion in a successor application.

The above changes to claim 3 add the limitations of the last clause of allowed claim 27 to claim 3. Claim 27 was allowed as a claim dependent on rejected claim 26 in the Office Action dated November 3, 1993. Claim 27 was rewritten as an independent claim by reciting the subject matter of rejected claim 26 in the amendment filed March 24, 1994. Claim 3 therefore does not raise new issues after final because the same language accorded patentable significance in claim 27 by the Examiner has been added to rejected claim 3.

Claims 3, 7-11, 26, 71-72 and 76-77 were rejected under 35 U.S.C. § 103 as unpatentable over Boufarah et al., U.S. Patent 5,127,091. The rejection of claims 3, 7-11 and 71-72 on this basis is believed to be overcome by the above changes to claim 3 and the following remarks. The language of the last clause of allowed claim 27 defines a stack architecture and was accorded patentable significance as pointed out above by the allowance of that claim when it was a dependent claim reciting just that clause. This same language accorded patentable significance has now been added to claim 3. Claim 3 thus now recites the combination of multiple instruction fetch in a single memory cycle and a stack architecture. No such combination is taught or suggested by either the Boufarah et al. patent or the Intel 80386 Programmer's Reference Manual given to the Examiner in the interview. While the Intel Manual discloses a multiple instruction fetch in a single memory cycle, the Intel 80386 microprocessor does not employ a stack architecture.

Because the Examiner has already concluded that the multiple instruction fetch in a single memory cycle alone as claimed in claim 3 is not of patentable

significance, the existence of the Intel 80386 teaching of that feature does not affect the patentability of the allowed claims. The above changes to claims 34, 35, 36, 39, 41, 44 and 46 change the dependencies of those claims but do not affect their patentability, because all of these claims remain dependent on an allowed claim.

All of the claims in the application are believed to be patentable over the prior art. This application is believed to be in condition for allowance, and allowance is solicited.

Respectfully submitted,

COOLEY GODWARD CASTRO HUDDLESON & TATUM

Willis E. Higgins
Reg. No. 23,025

Five Palo Alto Square
Fourth Floor
Palo Alto, California 94306-2155
Telephone: (415) 843-5145

OFFICIAL

NOV 1 0 1994

EXHIBIT 31

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
07/389,334	8/3/89	Moore	

EXAMINER	
ENG	
ART UNIT	PAPER NUMBER
2315	17

DATE MAILED:

EXAMINER INTERVIEW SUMMARY RECORD

All participants (applicant, applicant's representative, PTO personnel):

(1) D. ENG (3) _____

(2) W. HIGGINS (4) _____

Date of interview 10/25/94

Type: ☐ Telephonic ☒ Personal (copy is given to ☐ applicant ☐ applicant's representative).

Exhibit shown or demonstration conducted: ☐ Yes ☒ No. If yes, brief description: _____

Agreement ☐ was reached with respect to some or all of the claims in question. ☒ was not reached.

Claims discussed: 3, 26 & 27

Identification of prior art discussed: Bonfanah

Description of the general nature of what was agreed to if an agreement was reached, or any other comments: Claim 1: Operand width is variable & right adjusted. Claim 26: Figure 9 shows that DAAM & CPU are on the same chip. Ref. Intel 80386 (provided by applicant) shows a CPU chip with internal memory and multiply units width fetch

(A fuller description, if necessary, and a copy of the amendments, if available, which the examiner agreed would render the claims allowable must be attached. Also, where no copy of the amendments which would render the claims allowable is available, a summary thereof must be attached.)

Unless the paragraphs below have been checked to indicate to the contrary, A FORMAL WRITTEN RESPONSE TO THE LAST OFFICE ACTION IS NOT WAIVED AND MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW (e.g., items 1–7 on the reverse side of this form). If a response to the last Office action has already been filed, then applicant is given one month from this interview date to provide a statement of the substance of the interview.

☐ It is not necessary for applicant to provide a separate record of the substance of the interview.

☐ Since the examiner's interview summary above (including any attachments) reflects a complete response to each of the objections, rejections and requirements that may be present in the last Office action, and since the claims are now allowable, this completed form is considered to fulfill the response requirements of the last Office action.

Examiner's Signature

PTOL-413 (REV. 1-84)

ORIGINAL FOR INSERTION IN RIGHT HAND FLAP OF FILE WRAPPER

EXHIBIT 32

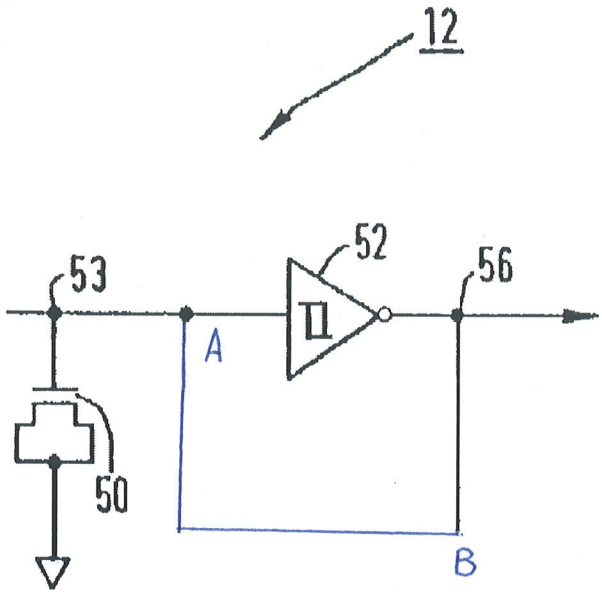


FIG. 3

77

EXHIBIT 33

United States Patent [19]

Dingwall

[11] **4,105,950**

[45] **Aug. 8, 1978**

[54] **VOLTAGE CONTROLLED OSCILLATOR (VCO) EMPLOYING NESTED OSCILLATING LOOPS**

[75] Inventor: **Andrew Gordon Francis Dingwall,** Bridgewater, N.J.

[73] Assignee: **RCA Corporation,** New York, N.Y.

[21] Appl. No.: **832,285**

[22] Filed: **Sep. 12, 1977**

[30] **Foreign Application Priority Data**

Sep. 13, 1976 [GB] United Kingdom 37853/76

[51] **Int. Cl.**[2] **H03B 3/04;** H03B 5/24; H03K 3/282

[52] **U.S. Cl.** ..... **331/57;** 331/108 D; 331/111; 331/135; 331/143; 331/177 R

[58] **Field of Search** ..... 331/57, 108 B, 108 C, 331/108 D, 111, 113 R, 135, 143, 177 R

[56] **References Cited**

U.S. PATENT DOCUMENTS

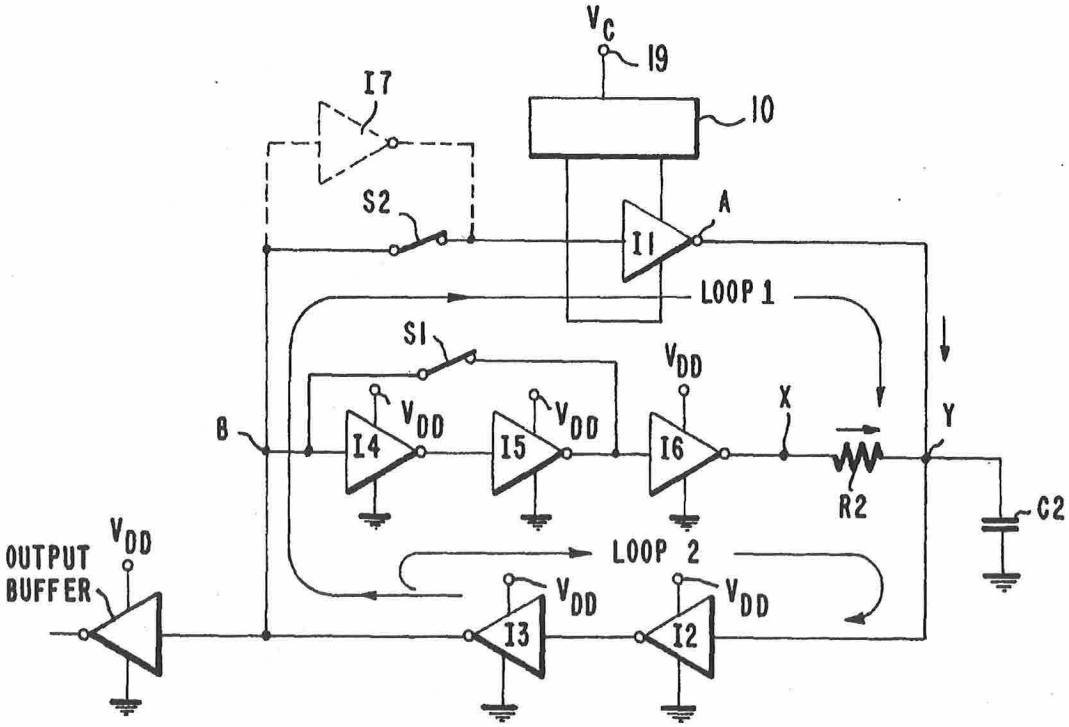
3,676,801	7/1972	Musa	331/116 R
3,863,179	1/1975	Goo	331/108 D
3,878,482	4/1975	Schowe, Jr.	331/108 D
3,904,988	9/1975	Hsiao	331/111
3,931,588	1/1976	Gehweiler	331/57

Primary Examiner—Siegfried H. Grimm
Attorney, Agent, or Firm—H. Christoffersen; Henry I. Schanzer

[57] **ABSTRACT**

The VCO is comprised of first and second "nested" oscillating loops. The first loop includes M cascaded inverters interconnected to normally oscillate at a given fixed frequency. The second loop includes N cascaded inverters where the input of the first of the N inverters is connected to the output of one of the M inverters and where the output of the Nth inverter is coupled to the output of a different one of the M inverters, whereby at least one of the M inverters is common to the two loops, and where M and N are integers. A control voltage is coupled to at least one of the N inverters to vary its conductivity and cause the frequency of oscillation of the two loops to change.

6 Claims, 5 Drawing Figures



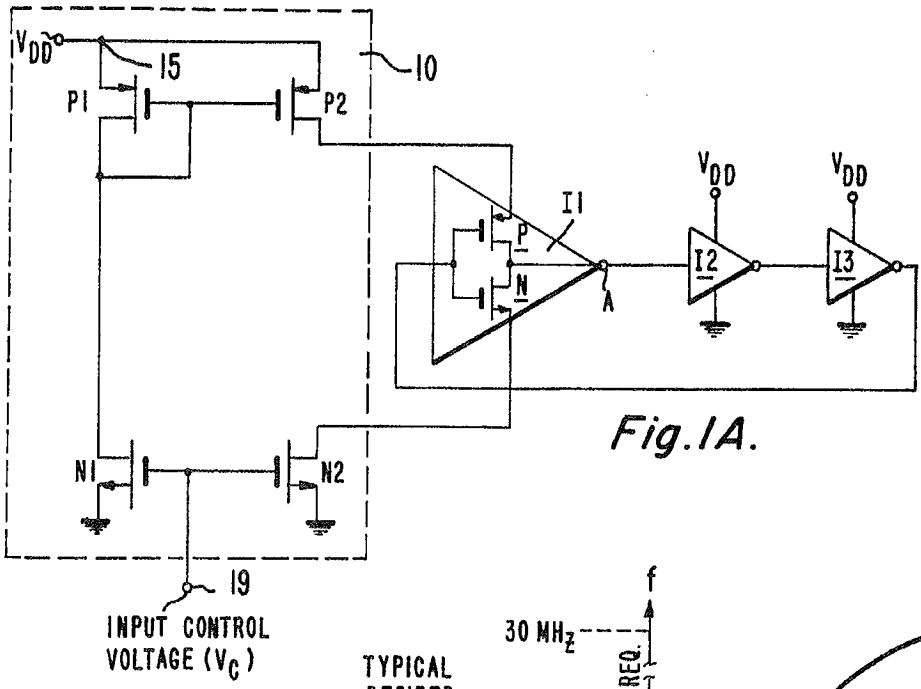


Fig. 1A.

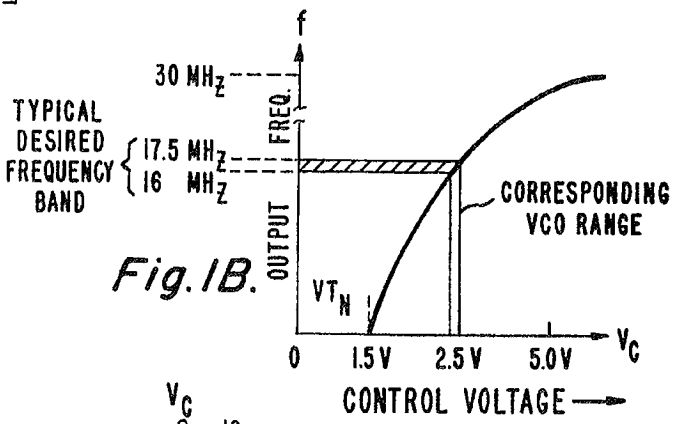


Fig. 1B.

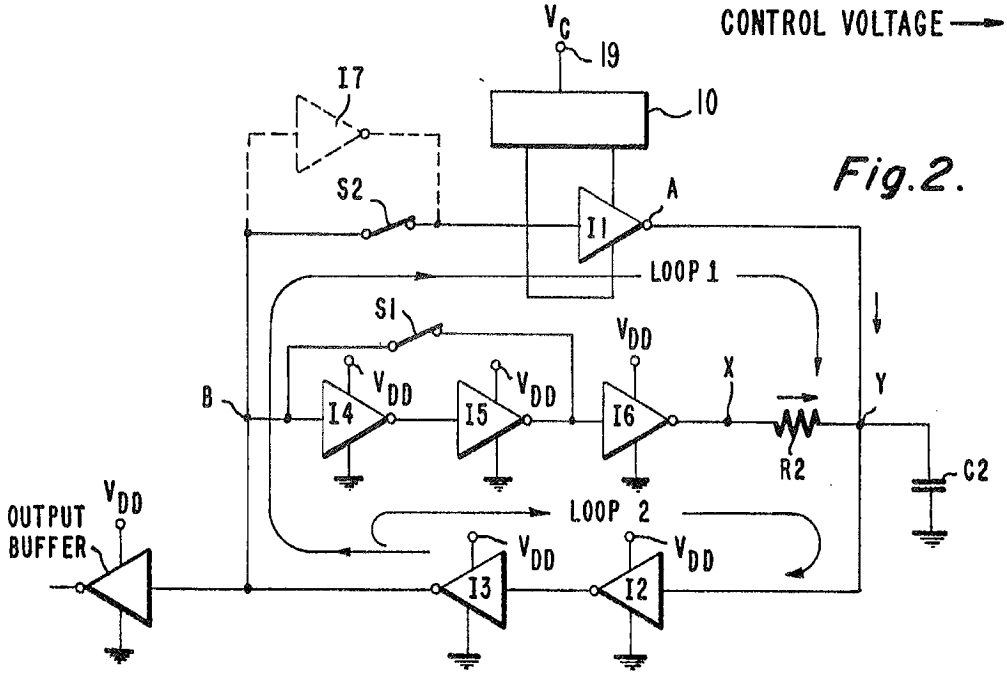


Fig. 2.

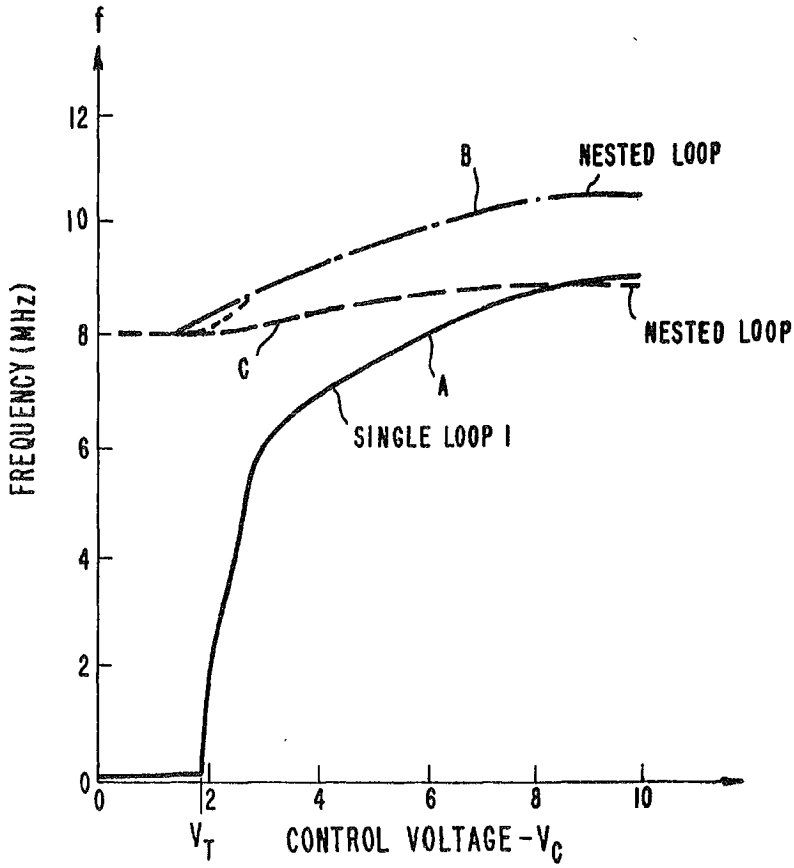

f
12
10
8
6
4
2
0
FREQUENCY (MHz)
B
NESTED LOOP
C
NESTED LOOP
A
SINGLE LOOP I
0
2
4
6
8
10
V_T
CONTROL VOLTAGE - V_C

Fig. 3.

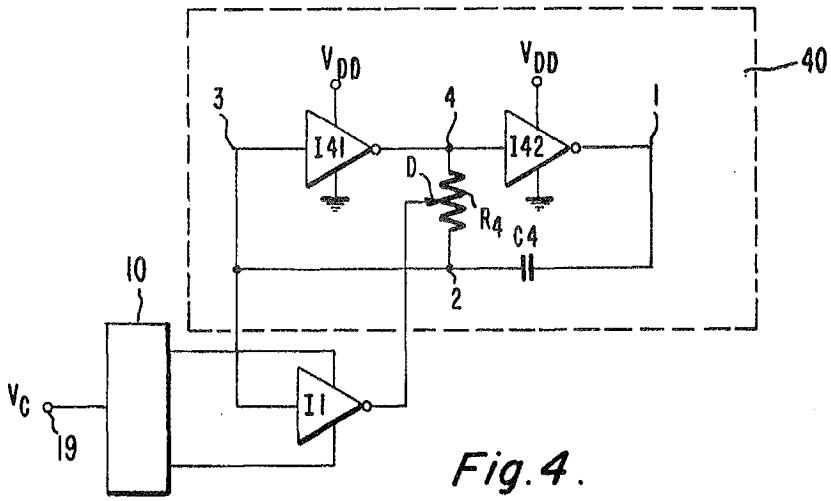

V_{DD}
V_{DD}
40
3
4
I
I41
I42
D
R_4
C_4
2
10
V_C
19
I1

Fig. 4.

VOLTAGE CONTROLLED OSCILLATOR (VCO) EMPLOYING NESTED OSCILLATING LOOPS

This invention relates to voltage controlled oscillators (VCOs) having a fixed frequency output in the absence of an input control voltage (V_C) and a well-controlled frequency response as a function of V_C.

FIG. 1A is a schematic diagram of a known VCO;

FIG. 1B is a diagram showing the change in frequency as a function of control voltage (V_C) for the circuit of FIG. 1A;

FIG. 2 is a schematic diagram of a VCO employing nested oscillator loops in accordance with the invention;

FIG. 3 is a diagram of the frequency response versus V_C of the circuit of FIG. 2 for different conditions of the nested loops; and

FIG. 4 is a schematic diagram of another VCO embodying the invention.

Voltage Controlled Oscillators are used in numerous applications. One of these is in frequency synthesizers for CB radios to generate various ones of the channel frequencies. Typically, the output of the VCO is divided down by a counter and then fed into a phase comparator to which is also applied the output of a reference oscillator. The output of the phase comparator is then used to generate a control voltage (V_C) which controls the potential applied to the VCO and hence its frequency of oscillation.

Numerous VCO circuits are known and are commercially available. However, these circuits suffer from one or more of the following disadvantages:

a. deadband—for values of V_C below a certain level there is no oscillation of the circuit;
b. the frequency variations of the oscillator are too rapid for small variations in V_C; and
c. a tank circuit may be required to load down one of the nodes of the circuit.

These disadvantages are illustrated by reference to FIG. 1A which shows a "single loop" VCO of the type described in my pending U.S. application Ser. No. 783,657, titled VOLTAGE CONTROLLED OSCILLATOR, and assigned to RCA Corporation.

Cascaded inverters I1, I2, and I3, with the output of I3 fed back to the input of I1, form a ring oscillator. A fixed operating voltage (V_{DD} and GND) is applied to inverters I2 and I3 while the voltage and current supplied to inverter I1 are varied by means of a current mirror arrangement 10, responsive to a control voltage, V_C, applied to terminal 19. The current mirror 10 includes insulated-gate field-effect transistors (IGFETs) P1, P2, N1 and N2. Transistors P1 and N1 whose conduction paths are serially connected between V_{DD} and ground pass the same current. The current through transistors P1 and N1 is mirrored through transistors P2 and N2 whose gate to source regions are connected in parallel with those of P1 and N1, respectively. When the value of V_C applied to the gates of transistors N1 and N2 exceeds their threshold voltage (V_T), currents flow through P2 and N2 and oscillation begins. The frequency of oscillation of the ring oscillator depends on the current passed via controlled current source transistor P2 and controlled current sink transistor N2 to the output A of inverter I1. As shown in FIG. 1B, which depicts the frequency response of the circuit as a function of V_C, the frequency of oscillation rises rapidly from zero Hz to about 50 MHz for a change in V_C of 2

or 3 volts (above V_T volts). Where, as shown in FIG. 1B, the desired frequency band is narrow (e.g., 16.5 to 17.5 MHz), the corresponding range of V_C is very small, and voltage perturbations of even a vew millivolts (due to noise or switching) on the control line result in excessive frequency shifts.

The problem of excessive frequency shift may be resolved by using a resonant tank circuit connected to one of the nodes (e.g., A) of the oscillator circuit. But, as the oscillator is operated away from the resonant frequency of the tank circuit, there is considerable power dissipation due to the decreased impedance of the tank. Secondly, and perhaps most importantly, tank circuits require inductance(s) and capacitance(s). The inductance cannot be manufactured readily as part of an integrated circuit (IC) and it is impractical to manufacture large values of capacitance on an IC. Thus, the circuit of FIG. 1A has a deadband, excessive frequency shift (for some applications), and may require a tank circuit to contain the frequency of oscillation within a given range.

Applicant has found that the disadvantages discussed above may be avoided by "nesting" one oscillating loop within another oscillating loop; where "nesting" as used herein refers to the sharing by the two loops of at least one common element causing the two loops to oscillate at the same frequency. One loop is designed to, normally, oscillate at a given frequency when a control voltage coupled to the other loop is below a given level. The other loop includes means responsive to the control voltage which, when the control voltage exceeds the given level, varies the frequency of oscillation of the two loops. The one loop ensures a fixed oscillator frequency during the deadband (when V_C is less than V_T) and functions as a tuned tank circuit. As a result, increased linearity of response is achieved with lower power dissipation than with known tank circuits. These and other advantages of the invention may best be explained with reference to the remaining drawings.

The VCO circuit of FIG. 2 includes two loops. The first loop, 1, which is essentially the same as the circuit shown in FIG. 1A, includes a voltage controlled ring oscillator loop comprised of inverters I1, I2 and I3. The input of inverter I1 is connected via switch S2 to node B and its output, A, is connected to node Y. Inverters I2 and I3 are connected in cascade between nodes Y and B in a direction to produce an output at node B in response to an input at node Y. The operating potential applied across I1 and hence the current supplied to, and by, inverter I1 is controlled by a current mirror network 10 responsive to an input control voltage (V_C) applied to terminal 19, as described for FIG. 1A.

The operation of loop 1 has been discussed above, a similar circuit is discussed in detail in my application cited above, and therefore, the operation of loop 1 will not be discussed in great detail at this point. Suffice it to say, that for V_C below V_T, inverter I1 does not conduct, it supplies no output current and the loop does not oscillate. For V_C increasing above V_T, the output current (being supplied and sinked) at node A of inverter I1 increases and loop 1 oscillates at higher rates corresponding to the higher currents produced by I1.

The second loop 2, includes an odd number of inverters (I2, I3, I4, I5 and I6), two of which (I2, I3) are common to loop 1. Inverters I4, I5 and I6 are connected in cascade, with the input of inverter I4 connected to node B and with the output of inverter I6 connected to terminal X. A resistor R2 is connected between terminal

X and node Y, and a capacitor C2 is connected between node Y and ground.

Where the inverters are interconnected by direct current (d.c.) connections (wires or resistors), an odd number of inverters have to be connected in a series (cascaded) loop to provide an unstable configuration assuring oscillation of the loop. Loop 2 is shown with five inverters (I2, I3, I4, I5 and I6); in a breadboarded circuit it was found that the output of the oscillator contained less harmonics when five, rather than three, inverters were connected in the loop. However, for ease of the description to follow, it is assumed that inverters I4 and I5 are short circuited by means of normally closed switch S1 connected between the input of inverter I4 and the output of inverter I5.

In the circuit of FIG. 2 all the inverters except for inverter I1 have V_{DD} volts and ground applied to their appropriate power terminals.

With its inverters powered and with I1 non-conducting, loop 2 oscillates at a rate determined by the capacitance at the input and output of each inverter, the potential across the inverters (V_{DD} and ground), the current flowing through the inverting stages (since the stage current determines the rate at which nodal capacitances can be charged or discharged), the open loop gain, and the frequency response of the transistors forming the inverters. Ring oscillators comprising three cascaded complementary inverters were built (with R2 shorted and without the addition of capacitance C2) and, when operated at V_{DD} equal to 10 volts, oscillated in a free running mode at about 100 MHz.

To have loop 2 generate a reproducible predetermined frequency of oscillation, and to reduce the effect of variations in inverter response in each circuit, and from circuit to circuit, a passive reactive network (R2, C2) is included in the loop.

By making R2 greater than the equivalent output resistance (R_0) of I6 and by making C2 significantly greater than the stray or distributed capacitance at any of the other nodes of the circuit, R2 and C2 dominate the other circuit parameters and, therefore, control and set the frequency of oscillation of loop 2. For this condition, the frequency of oscillation of loop 2 (with I1 non-conducting) is determined by the rate at which inverter I6 can charge or discharge capacitor C2, and may be calculated, to a first approximation, as follows:

$$f_{Osc} = 1/(2\pi \cdot RC)$$

where R is equal to R2 plus R_O of I6 (when inverter I1 is non-conducting) and C = C2.

The circuit of FIG. 2 was breadboarded using inverters of the complementary conductivity type shown in FIG. 1A, with R2 set to 500 ohms, C2 set to 30 picofarads and with a V_{DD} of 10 volts applied across all the inverters except I1. The measured frequency of oscillation of loop 2 (for $V_C = 0$) was just above 8MHz, which corresponds to R_0 of inverter I6 being approximately 150 ohms. To better explain the operation of the circuit reference is made to FIG. 3 which graphs results obtained from the breadboarded circuit under different operating conditions.

To better demonstrate the effect of "nesting" the two loops, the breadboarded circuit was operated with the branch comprising inverters I4, I5, I6 and resistor R2 opened and thus not in the circuit, but with a capacitor C2 of 30 picofarads (30×10^{-12}F) connected between node Y and ground. The response of the "single-loop" (i.e., loop 1) operation is shown in waveform A of FIG. 3. Note that there is a deadband (F = 0Hz) for values of V_C below about 2 volts, followed by a sharp increase in frequency for V_C between 2 and 4 volts and a somewhat slower rise in frequency as V_C increases above 4 volts. The slower rise in frequency for V_C above 4 volts is due, in part, to C2.

The breadboarded circuit was then operated with inverters I1 and I6 connected in parallel between node B and terminal X, with a resistor R2 of 500 ohms and a C2 of 30pf. As noted above and as shown in waveform B of FIG. 3, for values of V_C less than V_T (with I1 non-conducting) the circuit (i.e., loop 2) oscillated at approximately 8 MHz. Inverter I6 produces an alternating current which alternately charges and discharges node Y producing a signal fed back to node B via inverters I2 and I3. For sustained oscillation the Barkhausen criteria must be met; i.e., the loop phase shift must be 360° or an integer multiple thereof and with a gain of at least one. Hence, the phase shift across each inverter at the frequency of oscillation is greater than 180° such that together with the shift due to the RC network a phase shift of $n \times 360°$ is obtained around the loop.

With V_C above V_T volts, I1 is rendered conducting. With the inputs of I1 and I6 directly connected to node B (switches S1 and S2 closed) the same signal is applied to their inputs. These two inverters being of similar construction produce output currents which will, therefore, be in-phase. Hence the output current of inverter I1 flows into node Y where it is summed algebraically with the output current produced by inverter I6. For the in-phase condition, more current flows into node Y, charging and discharging it faster and thus increasing the frequency of oscillation. As before, the signal produced at node Y is fed back to node B via inverters I2 and I3. The signal at node B is applied to the paralleled inverters I1 and I6. These two inverters are then locked in on the same signal and respond in phase. As shown in waveform B of FIG. 3 the oscillator frequency is higher when both I1 and I6 are conducting in-phase. Summing the currents from the two loops does not result in the sharp change in frequency for a given change in V_C experienced for single loop operation. Rather, a higher frequency of oscillation is obtained with greater linearity. Loops 1 and 2 operate at the same frequency since they share the same elements (inverters I2, I3) and the combination of the two loops functions as a single oscillator. There is no modulation of one frequency signal by another frequency signal as would occur if the two loops were operated independently and their outputs subsequently mixed.

One effect of "nesting" loops 1 and 2 is that the resulting frequency response versus V_C is similar to the response obtained by connecting a tank circuit to node Y. But, in sharp contrast thereto, there is no need for an inductance and there is less power dissipation than with a tank circuit.

In the circuit of FIG. 2 the output A of inverter I1 may be connected to terminal X instead of to node Y. The effect of this connection is to further decrease the rate at which the frequency of oscillation changes versus V_C as shown in waveform C of FIG. 3. For the connection of output A to terminal X the output resistances of inverters I1 and I6 are effectively connected in parallel with each other and then connected in series with R2. This connection further reduces the effect of I1 and thus lowers the maximum frequency obtainable.

An important aspect of the circuit of FIG. 2 is the recognition that the output currents of inverters I1 and I6 are algebraically summed. Where the signals applied to the inputs of the two inverters are in-phase (when their two inputs are direct current connected to the same node) the frequency of oscillation increases as I1 is made more conductive.

By applying out-of-phase signals to the inputs of inverters I1 and I6, the frequency of oscillation may be made to decrease with increasing V_C. This may be achieved, for example, by opening switch S2 and connecting an inverter I7, shown with dashed lines in FIG. 2, between node B and the input of inverter I1.

Since an even number of inverters is then connected in series in loop 1, it does not oscillate unconditionally. But, with V_C less than V_T, loop 2 still oscillates at its set frequency. As V_C increases above V_T, the output current of I1 increases. But, with inverter I7 in series with inverter I1, the signal applied to the input of inverter I1 is out-of-phase with the signal applied to inverter I6. The output current supplied by inverter I1 into node Y then subtracts from the output current supplied by I6. Consequently, for out-of-phase operation, the frequency of oscillation decreases for and increasing V_C. Thus, the output characteristic of the VCO may be shaped to increase or decrease depending on whether an in-phase or an out-of-phase mode of operation is selected.

In the description and in the testing of the circuits, complementary inverters of the type shown for inverter I1 in FIG. 1A were used, but it should be understood that any other suitable inverter could be used instead.

Also, only one controlled inverter (i.e., I1) was shown, but other controlled inverters could have been added to loop 1 or in branches parallel to the branch including inverter I1 between nodes B and Y.

In the circuit of FIG. 4 the frequency of oscillation of an astable multivibrator 40 is varied and controlled by means of inverter I1. The circuit 40 includes two cascaded inverters I41, I42 with resistor R4 connected between the input and output of I41 and capacitor C4 connected between the output of I42 and the input of I41. Inverter I1, whose conductivity is controlled by V_C applied to the current mirror arrangement 10, is connected at its input to node 3 to which is connected the input of I41, and is connected at its output to a point D along R4 between nodes 2 and 4. The operation of the astable circuit 40 will not be detailed since it is well known and described, among others, in Application Note ICAN 6466, published May 1976 by RCA Corporation. When inverter I1 is non-conductive, during one portion of the cycle, terminal 1 of capacitor C4 is positively charged towards V_{DD} by the output of I42 and terminal 2 of capacitor C4 is discharged via resistor R4 and the output of inverter I41 towards ground. During another portion of the cycle, terminal 2 of capacitor C4 is positively charged towards V_{DD} by the output of I41 via resistor R4, and terminal 1 of C4 is returned to ground via the output of I42.

When I1 is rendered conductive by V_C exceeding V_T it supplies a current into node D which is in-phase with the output current produced by I41. This additional current charges and discharges C4 faster and hence the frequency of oscillation of this nested arrangement is varied as a function of V_C. The circuit of FIG. 4 thus illustrates that the invention may be practiced with oscillating loops (e.g., astable multivibrator) other than ring oscillators.

Note that the loop which includes cascaded inverters I41, I42 is closed by means of capacitor C4 which provides alternating current (AC) feedback between the output of I42 and the input of I41. In contrast to the resistively coupled ring oscillator loop 2 of FIG. 2 which requires an odd number of inverters to oscillate, the AC coupled loop sustains oscillation with an even number of inverters in the loop.

What is claimed is:

1. A voltage controlled oscillator comprising:

first and second terminals;

an input terminal adapted to receive a control voltage;

R, S and F cascaded inverters, where R, S and F are integers;

means connecting said R inverters and said S inverters in parallel between said first and second terminals; said R and S inverters being connected in a direction to produce an output at said second terminal in response to an input at said first terminal;

means connecting said F inverters between said second and said first terminals in a direction to produce an output at said first terminal in response to an input at said second terminal; said R and F inverters forming a loop when said control voltage is below a given level, which normally oscillates at a given frequency; and

means receptive to said control voltage being coupled to at least one of said S inverters for varying its conductivity and output current in response to said control voltage being above said given level and, in turn, varying the frequency of oscillation of said loop and said oscillator.

2. The combination as claimed in claim 1 wherein said means connecting said R inverters includes a resistor connected between the output of the Rth of said R inverters and said second terminal; and wherein a capacitance greater in value than any stray capacitance associated with said R, S and F inverters is connected between said second terminal and a point of fixed operating potential.

3. The combination as claimed in claim 2 wherein R and S are each equal to 1 and F is equal to 2.

4. The combination as claimed in claim 1 wherein R, S and F are each equal to 1; wherein said means connecting said F inverters between said second and first terminals includes a capacitor connected between the output of said F inverter and said first terminal; and

wherein said means connecting said R and S inverters in parallel includes means direct current connecting the inputs of said R and S inverters via negligible impedance means to said first terminal and resistive means connecting the output of one of said R and S inverters to said second terminal.

5. A voltage controlled oscillator comprising:

M inverters connected in cascade, and N inverters connected in cascade; where M and N are integers;

means connecting the output of the Mth of said M inverters to the input of the first one of said M inverters for forming a loop normally oscillating at a predetermined frequency;

means connecting the input of the first of said N inverters to the output of one of said M inverters, and means connecting the output of the Nth of said N inverters to the output of a different one of said M inverters for forming a second loop; and

means responsive to an input control voltage connected to at least one of said N inverters for alter-

ing its conductivity in response to said control voltage and thereby altering said predetermined frequency of oscillation.

6. In combination with a first, voltage controlled oscillator, loop comprised of N cascaded inverters; were N is an odd number equal to or greater than 1, and where the output of the Nth inverter is fed back to the input of the first inverter and where a control input voltage controls the voltage and current applied to at least one of the inverters of the first loop for controlling its frequency of oscillation, the improvement comprising:

R cascaded inverters;

means connecting the input of the first of said R inverters to the output of one of said N inverters; and

means including a reactive network connected between the output of the Rth of said R inverters and the output of a different one of said N inverters for forming a second oscillating loop and said reactive network being selected to cause said second loop to normally oscillate at a predetermined frequency when said control input voltage is below a given value.

* * * * *

EXHIBIT 34

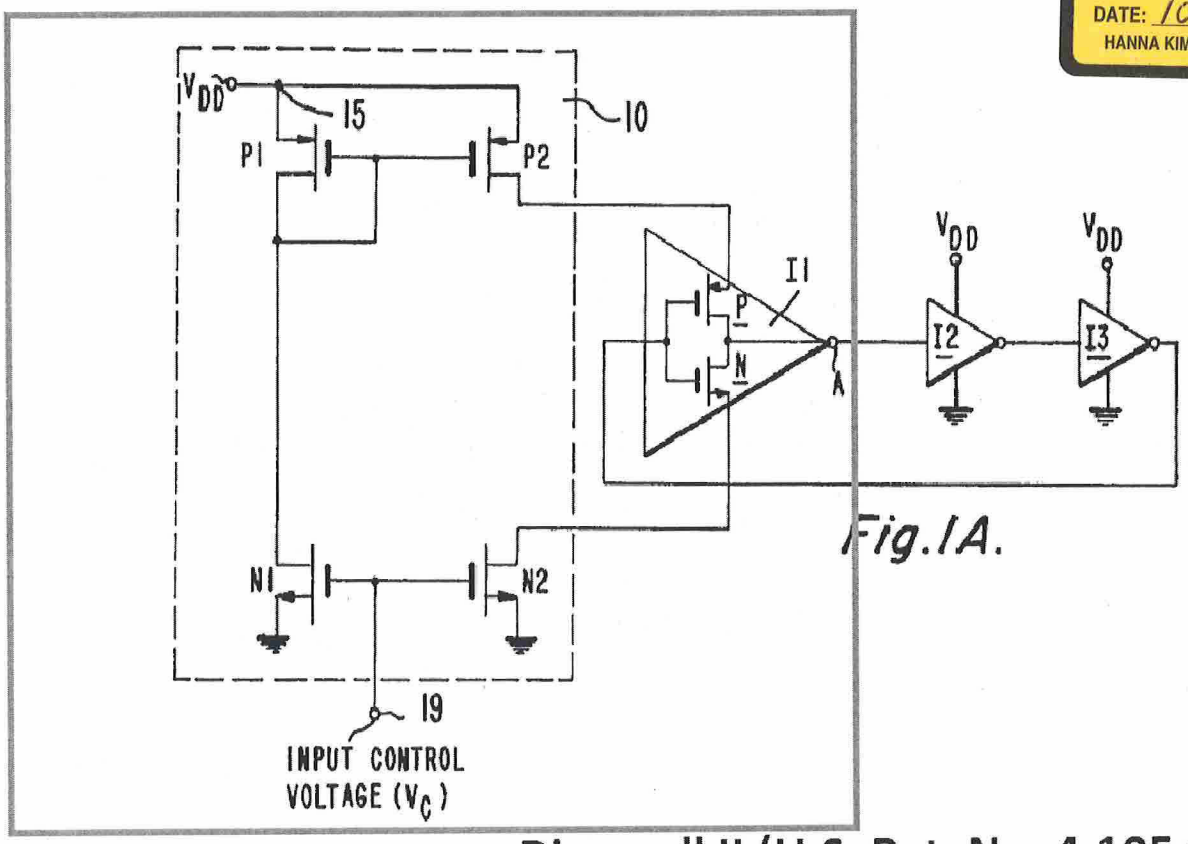


Fig.1A.

Dingwall II (U.S. Pat. No. 4,105,950)

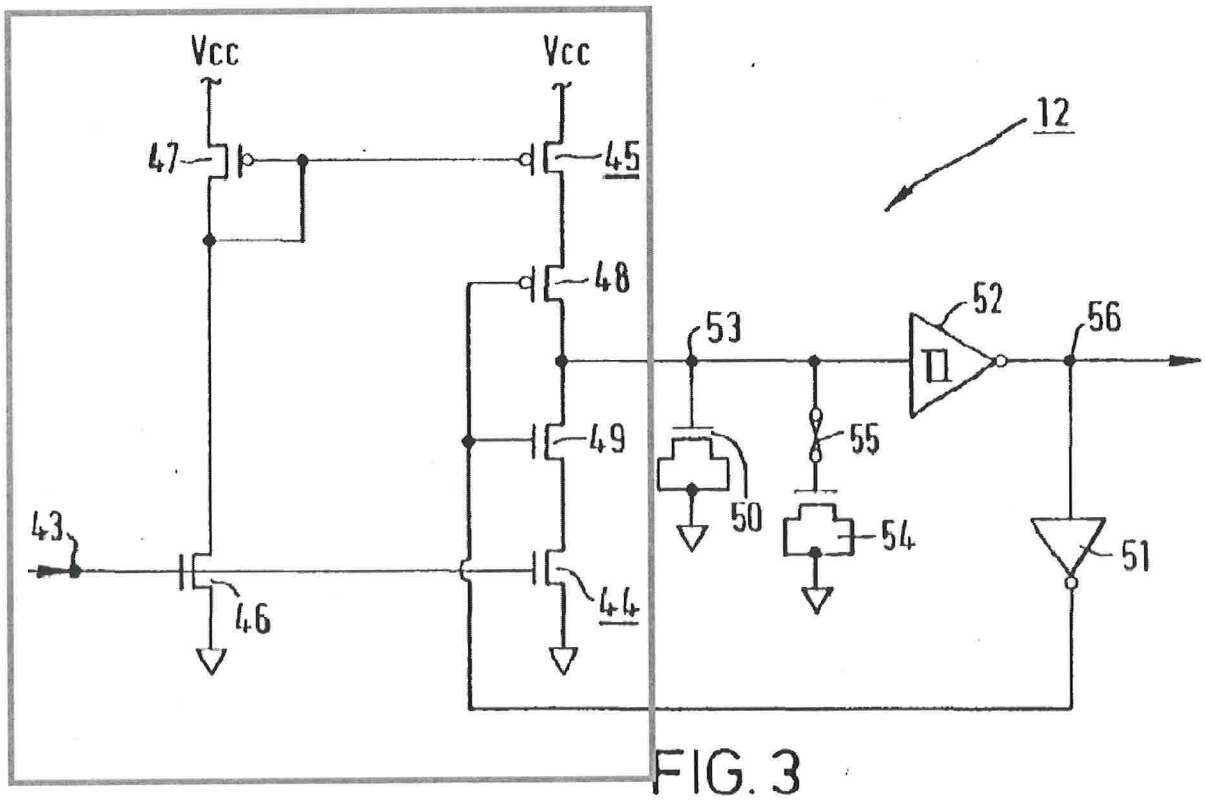


FIG. 3

Talbot (U.S. Pat. No. 4,689,581)