[See Signature Page for Information on Counsel for Plaintiffs]

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00877 PSG **PLAINTIFFS' SUR-REPLY IN SUPPORT OF THEIR OPPOSITION TO DEFENDANTS' MOTION FOR RECONSIDERATION OF CERTAIN ASPECTS OF FIRST CLAIM CONSTRUCTION ORDER** **[RELATED CASES]** Date: November 30, 2012 Time: 10:00 a.m. Place: Courtroom 5, 4th Floor Judge: Paul Singh Grewal
HTC CORPORATION, HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00882 PSG
BARCO N.V., a Belgian corporation, Plaintiff, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-05398 PSG

I. INTRODUCTION

Defendants Technology Properties Ltd., Patriot Scientific Corp. and Alliacense Ltd. (hereinafter "Defendants" or "TPL") filed their motion for reconsideration of Judge Ware's construction of "separate direct memory access central processing unit" ("separate DMA CPU") presenting only two arguments: (1) that a restriction requirement in the parent application of the '890 patent allegedly supported a broader construction; and (2) that statements in the reexamination file history allegedly confirm that DMA CPU could include a conventional DMA controller. (Dkt. No. 349-1 in No. 08-cv-00877-PSG ("*Acer* Action"), at 3-6.)

TPL's reply brief, however, goes far beyond the two arguments presented in its opening brief and attempts to relitigate the entire construction of DMA CPU. It includes five pages of new arguments about the "intrinsic record as a whole" that TPL admits go beyond the two arguments presented in its opening brief. (Dkt. No. 369 in *Acer* action, at 10:20-21 ("**Beyond** just the restriction requirement and the reexamination proceeding, the entire intrinsic record supports Defendants' proposed construction of DMA CPU ….") (emphasis added).) The new arguments presented on pages 10 through 14 of TPL's reply brief should not be considered because they exceed the scope of the leave granted to TPL to seek reconsideration, and are improper for a reply brief. But if the Court is inclined to consider those arguments, Plaintiffs respectfully request that the Court consider the responsive arguments below so it will have a full discussion of the intrinsic record – a record that refutes TPL's overbroad construction and its misplaced arguments.

II. ARGUMENT

The basic argument presented on pages 10 through 14 of TPL's reply brief is that the '890 specification discloses an alternative embodiment in which the DMA CPU is replaced with a conventional DMA controller. TPL contends that Judge Ware erred by focusing on the first embodiment (DMA CPU **72**) and adopting a construction that excluded the conventional prior art DMA controller used in the alternative embodiment. (Reply at 10-14.)

A. TPL Has Not Overcome The Express Claim Language.

TPL's argument ignores the plain language of the claim and is based on an incorrect legal

premise. Claim 11 of the '890 patent, the only independent claim following the reexamination,[1] recites "[a] microprocessor, which comprises a main central processing unit and **a separate direct memory access central processing unit** in a single integrated circuit . . . ." ('890, Reexam. Cert., Claim 11.) The claim does not recite a DMA controller, and as explained in more detail below, the specification repeatedly differentiates the claimed DMA CPU from the DMA controller of the prior art. ('890, *e.g.*, 1:55-58, 12:62-65.)

TPL's argument assumes that "DMA CPU" must be construed broadly enough to cover every DMA-related embodiment in the specification, but this is not the law. As the Federal Circuit has observed, "[o]ur precedent is replete with examples of subject matter that is included in the specification, but is not claimed." *TIP Sys., LLC v. Phillips & Brooks/Gladwin, Inc.*, 529 F.3d 1364, 1373 (Fed. Cir. 2008). That the specification discloses an embodiment in which a DMA controller is employed does not mean that "DMA CPU" must be construed to cover that embodiment. "Therefore, the mere fact that there is an alternative embodiment disclosed in the ['890] patent that is not encompassed by district court's claim construction does not outweigh the language of the claim, especially when the court's construction is supported by the intrinsic evidence." *Id.* And such a construction would clash with the intrinsic record as explained below.

B. TPL's Latest Attempt To Read "CPU" Out of "DMA CPU" Fails.

The term "direct memory access" or "DMA" is a well-known technology for improving the performance of computer systems. DMA allows certain subsystems or components within a computer (such as a disk drive or other devices) to transfer data to memory without the main CPU having to perform the actual data transfer, allowing the CPU to perform other tasks. The '890 specification identifies two distinct structures that involve DMA operations – the unclaimed "DMA controller" of the prior art, and the DMA CPU recited in claim 11.

The '890 patent acknowledges that DMA controllers are not only the prior art, but the prior art over which the applicants sought to make an improvement. The specification states that "DMA controllers can provide routine handling of DMA requests and responses, but some processing by

[1] Claim 1 was canceled in the reexamination and new claim 11 was added.

the main central processing unit (CPU) of the microprocessor is required." ('890, 1:55-58.) The specification identifies, as an object of the alleged invention, a processor "in which DMA does not require use of the main CPU during DMA requests and responses and which provides very rapid DMA response with predictable response times." ('890, 2:2-5.) The '890 patent purports to provide such a processor by claiming a "separate direct memory access **central processing unit**," which is recited in the independent claim 11 of the '890 patent. As explained in the specification: "The DMA CPU **72** controls itself and has the ability to fetch and execute instructions. It operates as a co-processor to the main CPU **70** (FIG. 2) for time specific processing." ('890, 8:22-24.)

One of the key disputes during the claim construction proceedings before Judge Ware was whether a DMA CPU had the ability to "fetch and execute" instructions for performing DMA operations. Judge Ware found that "a person of ordinary skill in the art would understand 'CPU' to mean a unit of a computing system that fetches, decodes, and executes programmed instructions," and that "the inventors use the term CPU consistently with its plain and ordinary meaning." (First Claim Construction Order at 12:6–9 ("Order"), Dkt. No. 336 in *Acer* Action.) Judge Ware further observed that the "written description criticizes '[c]onventional microprocessors' that use 'DMA controllers' because 'some processing by the main central processing unit (CPU) of the microprocessor is required.'" (*Id.* at 12:10-13 (quoting '890, 1:52-58).) The Court accordingly construed "separate DMA CPU" to mean "a central processing unit that accesses memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit." (*Id.* at 13:3-4 (emphasis added).)

TPL's reply brief does not explain how its construction could be adopted without reading "CPU" out of the claim term "DMA CPU." TPL does not dispute that Judge Ware accurately described how one of ordinary skill in the art would understand "CPU." In fact, TPL conceded in its earlier briefing that "DMA controllers" are different from the claimed "DMA CPU" because: "This 'more traditional DMA controller' is one that functions more as a **traditional** state machine, **without the ability to fetch its own instructions that characterizes a CPU**." (*See* Dkt. No. 310 in *Acer* action, TPL's Opening Br. for "Top Ten" Terms, at 9:24-26 (emphasis added).) But the ability to fetch and then execute its own instructions – a feature that undisputedly "characterizes a

CPU" – is conspicuously missing from the construction TPL advances before this Court. TPL's renewed attempt to rewrite the claim to remove "CPU" from "DMA CPU" should be rejected. *See K-2 Corp. v. Salomon S.A.*, 191 F.3d 1356, 1364 (Fed. Cir. 1999) ("Courts do not rewrite claims; instead, we give effect to the terms chosen by the patentee").

C. The "DMA Controller" Embodiment Supports Judge Ware's Construction.

TPL's reply brief argues that the '890 specification treats the DMA CPU and DMA controller as interchangeable. TPL bases this argument entirely on the disclosure of an embodiment in which the DMA CPU is "replaced" with a traditional prior art DMA controller. But as shown below, this embodiment does not suggest that a "DMA CPU" and a "DMA controller" are the same thing; it actually confirms that the two are different.

The '890 specification discloses three embodiments that include structures for handling DMA operations. The first is the microprocessor **50** shown in Figure 2, which includes "DMA CPU **72**," which is further described in the specification at Column 8, lines 1-24. ('890, 8:1-24, Fig. 5 (showing further details of DMA CPU **72**).) As noted above, that description states that DMA CPU **72** "controls itself and has the ability to fetch and execute instructions" and "operates as a co-processor to the main CPU **70** (FIG. 2) for time specific processing." ('890, 8:22-24.)

Figure 9 of the '890 patent shows "a layout diagram of a second embodiment of a microprocessor" **310** that is depicted as including "DMA CPU **314**" and "CPU **316**." ('890, 4:61-63, 10:41, 10:52 and Fig. 9 (middle of figure).) This second embodiment is described as having a larger amount of on-chip memory but is otherwise no different from the microprocessor **50** in Figure 2. ('890, 9:5-6 ("The microprocessor **310** [of Fig. 9] is equivalent to the microprocessor **50** in FIGS. 1-8.").) Each of microprocessors **50** and **310** has the "dual processors" of a main CPU and a separate DMA CPU. *See* '890, 9:6-10 ("The microprocessors **50** and **310** are … requiring fewer than 50,000 transistors for ***dual processors 70 and 72*** (FIG. 2) or ***314 and 316*** ….") (emphasis added).

A separate passage appearing columns later in the '890 specification describes a third embodiment: "The microprocessor **310** CPU **316** resides on an already crowded DRAM die **312**. To keep chip size as small as possible, the DMA processor **72** of the microprocessor **50** has been

replaced with a more traditional DMA controller **314**." ('890, 12:61-65 (emphasis added).) There are no figures associated with this third embodiment. TPL relies on this embodiment, but it actually reinforces Judge Ware's construction. By disclosing an alternative system in which DMA CPU **72** has been "***replaced*** with a more traditional DMA controller **314**" ('890, 12:62-13:4 (emphasis added)), it confirms that the two are different. If a DMA CPU was the same thing as a DMA controller, as TPL contends, there would be no need to disclose an embodiment in which the DMA CPU is "replaced" with "a more traditional DMA controller." The specification further explains that this replacement was motivated by the need "[t]o keep chip size as small as possible" ('890, 12:62-63), an objective accomplished by replacing the larger and more complex DMA CPU with the smaller and simpler DMA controller of the prior art.

Everything in the intrinsic record confirms that when the specification refers to the DMA CPU and the DMA controller, it is talking about two very different structures. But only one of those structures – the DMA CPU – was actually claimed. The specification describes the more complex DMA CPU as an improvement over the conventional DMA controller, so it makes sense that "DMA CPU" as recited in the claims of the '890 patent would not cover the prior art DMA controller. And as explained above, the fact that the DMA controller is unclaimed is irrelevant. *See TIP Sys.*529 F.3d at 1373 ("Our precedent is replete with examples of subject matter that is included in the specification, but is not claimed.").

III. CONCLUSION

TPL's improper reconsideration arguments have been previously presented to and properly rejected by Judge Ware in his previous ruling. If the Court is inclined to consider them on the merits, it should reject them again. Because TPL's construction improperly seeks to lay claim over the DMA controller that the specification distinguishes from the claimed DMA CPU, it should be rejected. For the foregoing reasons, and the reasons stated in Plaintiffs' opposition brief, TPL's motion for reconsideration should be denied in its entirety.

Dated: December 5, 2012

Respectfully submitted,

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FILER'S ATTESTATOIN PURSUANT TO L.R. 5-1(i)(3)

I, Kyle D. Chen, attest that concurrence in the filing of PLAINTIFFS' SUR-REPLY IN SUPPORT OF THEIR OPPOSITION TO DEFENDANTS' MOTION FOR RECONSIDERATION OF CERTAIN ASPECTS OF FIRST CLAIM CONSTRUCTION ORDER has been obtained from each of the other Signatories hereto.

Executed this 5th day of December, 2012, at Palo Alto, California

By: */s/ Kyle D. Chen*
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