[See Signature Page for Information on Counsel for Plaintiffs]

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00877 PSG **REPLY BRIEF IN SUPPORT OF PLAINTIFFS' MOTION FOR RECONSIDERATION OF CERTAIN ASPECTS OF FIRST CLAIM CONSTRUCTION ORDER** **[RELATED CASES]** **DATE: NOVEMBER 30, 2012** **TIME: 10:00 A.M.** **PLACE: COURTROOM 5, 4TH FLOOR** **JUDGE: PAUL SINGH GREWAL**
HTC CORPORATION, HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00882 PSG
BARCO N.V., a Belgian corporation, Plaintiff, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-05398 PSG

I. INTRODUCTION

TPL's opposition papers (Dkt. 367 *Acer* Action, hereinafter "Opposition") employ the familiar refrain of accusing Plaintiffs of attempting to import extraneous limitations into the claims. ("TPL" includes Defendants Technology Properties Ltd., Patriot Scientific Corp. and Alliacense Ltd.) TPL's arguments are without merit, and Plaintiffs' proposed constructions should be adopted.

With respect to the phrase "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle" from U.S. Patent No. 5,440,749 (the "'749 patent" or "'749"), TPL attempts to obfuscate the issue by accusing Plaintiffs of seeking to exclude any system that happens to include a prefetch buffer or a one-instruction-wide instruction buffer. But this is not and has never been Plaintiffs' position. TPL made clear and unmistakable disclaimers during the '749 reexamination in which it told the Patent Office that this phrase excludes systems that supply instructions to the CPU one at a time. Plaintiffs merely seek to hold TPL to its representations to the Patent Office, which were neither rescinded during the reexamination nor affected by subsequent amendments to other claim elements.

With respect to the phrase "clocking said central processing unit" in U.S. Patent No. 5,809,336 (the "'336 patent" or "'336"), the Court should adopt Plaintiffs' construction because clocking the CPU to always achieve its maximum speed was described, in both the specification and file history, as a feature of the invention and a distinction over the prior art. TPL suggests that the intrinsic record merely describes the ability of the CPU to sometimes operate at the fastest possible speed, but this is inconsistent with the intrinsic record and would recapture the prior art systems that were criticized and distinguished throughout the intrinsic record.

II. ARGUMENT

A. "SUPPLY THE MULTIPLE SEQUENTIAL INSTRUCTIONS . . . "

TPL's argument on this phrase begins with the misleading heading "Judge Ware Correctly Construed the 'Supply Multiple Sequential instructions . . . ' Phrase." (Defs.' Response Brief in Opposition to Plaintiffs' Motion for Reconsideration at 3:4–5 ("Opposition"), Dkt. 367, *Acer Inc. et al. v. Technology Properties Ltd. et al.*, 08-cv-877-PSG ("*Acer* Action") (capitalization

altered).) But Judge Ware did not construe this phrase at all. He specifically declined to construe it based on his erroneous belief that the sole issue tendered for decision was "whether the phrase should be defined as requiring a 'prefetch buffer.'" (First Claim Construction Order at 8, *Acer* Action, Dkt. No. 336 ("Order").) TPL implicitly acknowledges as much by advancing its own construction of this phrase, which is the same construction it pursued in its arguments before Judge Ware. The proper construction of this phrase is therefore properly before this Court.

1. TPL Misstates the Underlying Dispute.

TPL devotes a large portion of its argument on this phrase to refuting a supposed position of Plaintiffs that they have not actually taken—that this phrase excludes any system that has either a prefetch buffer or a one-instruction-wide instruction buffer. (Opposition at 4.) This is not and has not been Plaintiffs' position. Plaintiffs have instead argued for a construction of this phrase that excludes "a prefetch buffer or a one-instruction-wide instruction buffer that ***supplies one instruction at a time***." (*See id.* at 3 (Plaintiffs' Proposed Construction).) The key issue in this phrase is whether it excludes instructions being supplied to the CPU one at a time, regardless of the physical structure used to supply the instructions.

Plaintiffs' proposed construction refers to a "prefetch buffer" and a "one-instruction-wide instruction buffer" only because TPL expressly distinguished those structures in the prior art which were used to supply instructions one at a time to the CPU. For example, TPL made the following disclaimer in distinguishing Edwards:

> Edwards describes the way the Transputer decodes and executes instructions. As described in Edwards, see, e.g., Fig. 8, below, instructions are supplied to a **one-instruction-wide instruction buffer**, one at a time, and are there decoded. Fetching multiple instructions into a **prefetch buffer** and then supplying them one at a time is not sufficient to meet the claim limitation – the supplying of "multiple sequential instructions to a CPU during a single memory cycle."

(Amendment, 1/19/2010, at 26 of 58, Chen Decl. Ex. 2, *Acer* Action, Dkt. No. 358-3 (emphasis added).)

TPL has no legitimate basis to object to the reference to a "prefetch buffer" or a "one instruction-wide buffer" in the proposed construction of this phrase. Plaintiffs' proposed construction would not exclude a system simply because it happens to include a prefetch buffer or

a one-instruction-wide instruction buffer. But it would exclude a system that uses one of those structures to supply instructions one at a time to the CPU.

TPL appears to concede, in fact, that it did disclaim a system that supplies instructions one at a time to the CPU. In characterizing its own arguments to the Patent Office during the '749 reexamination, TPL states that each of its statements:

> expressly distinguishes the prior art reference on the same basis: (1) the instructions are supplied to the CPU one at a time, (b) although two instructions might be fetched at the same time, one instruction is supplied to the CPU at a time, and (c) the 'during a single memory cycle' limitation is not satisfied by supplying only one instruction to the CPU at a time.

(Opposition at 5:26–6:2.)

But TPL's proposed construction of this phrase does not incorporate an express prohibition against supplying instructions one at a time to the CPU. Its construction, "provide the multiple sequential instructions in parallel to said central processing unit integrated circuit during a single memory cycle," merely parrots other language of the claim. Because TPL concedes that the claimed systems do not supply instructions to the CPU one at a time, Plaintiffs' construction should be adopted:

> provide the multiple sequential instructions in parallel **(as opposed to one-by-one)** to said central processing unit integrated circuit during a single memory cycle **without using a prefetch buffer or a one-instruction-wide instruction buffer that supplies one instruction at a time**

(Plaintiffs' Motion for Reconsideration at 2, *Acer* Action, Dkt. No. 358 (emphasis added).)

2. The Amendments to Claim 1 Did Not Rescind Earlier Disclaimers.

TPL relies on amended language at the end of claim 1, which recites that supplying the multiple sequential instructions to the CPU "comprises supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched." ('749 *Ex Parte* Reexamination Certificate, 1:65–2:2, Chen Decl. Ex. 1, *Acer* Action, Dkt. No. 358-2).) TPL suggests that this amendment to claim 1 should be viewed as actually defining the disputed phrase, effectively erasing TPL's earlier disclaimers. (Opposition at 6.) This argument is without merit for at least two reasons.

First, TPL does not explain how any of its earlier disclaimers were rescinded or otherwise rendered ineffective. Although a disclaimer made during prosecution can be rescinded, "the prosecution history must be sufficiently clear to inform the examiner that the previous disclaimer, and the prior art that it was made to avoid, may need to be re-visited." *Hakim v. Cannon Avent Group, PLC*, 479 F.3d 1313, 1318 (Fed. Cir. 2007). This never happened during the '749 reexamination. TPL never informed the Examiner that its previous disclaimers made in distinguishing Edwards, May, and/or MacGregor needed to be revisited. And TPL never rescinded its earlier disclaimers.

Second and more fundamentally, the amendment to claim 1 does not even address the question of whether the phrase at issue here, "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle," excludes systems that supply instructions one-at-a-time to the CPU. The amended language merely recites a ***sub-step*** to the process of supplying multiple sequential instructions to the CPU. This is apparent from the amended claim language, which states that supplying the multiple sequential instructions to the CPU "*comprises* supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle." ('749 *Ex Parte* Reexamination Certificate, 1:65–2:2, Chen Decl. Ex. 1, *Acer* Action, Dkt. No. 358-2 (emphasis added).) This language, using the open-ended "comprising" transitional phrase, does not ***define*** the claimed step of supplying the multiple sequential instructions to the CPU—it merely specifies a particular sub-step that the claim step must include.

The fact that the amendment represents merely a sub-step is evident from a critical difference between the language of the term being construed and the amendment to claim 1 that TPL has overlooked. The amended language of claim 1 recites "supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle," while the phrase being construed is "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle." As explained below, because TPL's amendment involves the "instruction register," not the separately claimed "central processing unit

integrated circuit" (CPU), it has no bearing on reexamination disclaimers directed specifically at the phrase at issue here.

The "instruction register" and the CPU ("central processing unit integrated circuit") are separate and distinctly recited components of the claimed microprocessor system. Claim 1, in particular, recites a "microprocessor system" that comprises a "central processing unit integrated circuit" (CPU) which, in turn, "include[es] an arithmetic logic unit and a first push down stack." (*Id.* at 1:43.) The claim does not list the "instruction register" as a component of the CPU. The claim instead recites "an instruction register" four elements later in the claim, as an element of the broader microprocessor system ("wherein the ***microprocessor system*** comprises an instruction register") (*id.* at 1:55–57 (emphasis added)), not as part of the earlier-recited CPU. It is well-settled Federal Circuit law that "[w]here a claim lists elements separately, 'the clear implication of the claim language' is that those elements are 'distinct component[s]' of the patented invention." *Becton, Dickinson & Co. v. Tyco Healthcare Group, LP*, 616 F.3d 1249, 1254 (Fed. Cir. 2010) (quoting *Gaus v. Conair Corp.*, 363 F.3d 1284, 1288 (Fed. Cir. 2004)). Had the patentee intended for the "instruction register" to have been a part of the claimed CPU, it would have added that component to the CPU element rather than separately claiming it as part of the overall "microprocessor system."

Because supplying multiple sequential instructions to the "instruction register" as recited in the amendment does not by itself complete the step of supplying those instructions to the CPU, the amendment merely recites a sub-step in the process of supplying those instructions to the CPU. This is entirely consistent with the specification, which explains that the instructions must be supplied <u>from</u> the instruction register <u>to</u> the CPU. (*See* '749, 2:40–45 ("In still another aspect of the invention, the microprocessor system additionally includes an instruction register for the multiple instructions connected to the means for fetching instructions. A means is connected to the instruction register ***for supplying the multiple instructions in succession <u>from</u> the instruction register***.") (emphasis added).)[1]

[1] To use a real-world analogy, a claim could recite that "a means for delivering documents to Judge Grewal's courtroom on the fourth floor comprises clearing security on the first floor of the

The "instruction register" amendments to claim 1 therefore have no relevance to TPL's disclaimers regarding the phrase at issue here, "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle." TPL's disclaimers in the reexamination all related to supplying the instructions to the CPU, not to the instruction register. Those disclaimers did not even use the term "instruction register," let alone distinguish the prior art based on supplying the instructions to the instruction register.

3. Plaintiffs' Construction Will Prevent TPL's Improper Attempt To Recapture Disclaimed Subject Matter.

The importance of holding TPL to its statements to the Patent Office is highlighted by its Infringement Contentions as to the '749 patent seeking to accuse systems that behave in precisely the same way as the prior art distinguished during the reexamination. TPL's infringement contentions rely on a mode of operation in the accused systems ("Thumb mode") in which instructions are fed to the CPU one at a time. (Product Reports at 6 and 14 of 24, Chen Decl. Ex. 4, *Acer* Action, Dkt. No. 358-5 (emphasis added) (quoting ARM Ltd., An Introduction to Thumb).) TPL does not dispute that the accused products operate in this way, but contends that this is permissible because multiple instructions are received in parallel "by the instruction register." (Opposition at 8.) This argument relies on the assumption that the "instruction register" is part of the CPU, which is incorrect as explained above. Plaintiffs' proposed construction, which expressly excludes systems in which instructions are supplied to the CPU one at a time, must be adopted to prevent TPL's improper attempt to recapture the systems that it disclaimed to overcome prior art during the '749 reexamination.

B. "CLOCKING SAID CENTRAL PROCESSING UNIT"

The interpretation of the phrase "clocking said central processing unit" turns on whether TPL's emphatic statements in the specification and prosecution history describing the clocking of the invention should be given weight in claim construction. TPL attempts to characterize these statements as merely "describing one advantage of a preferred embodiment" (Opposition at 11),

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building at 280 South First Street." Clearing security on the first floor would certainly be a required sub-step in the delivery of the documents, but the delivery could not be complete until the documents were subsequently carried to Judge Grewal's courtroom on the fourth floor.

but this is inaccurate. The '336 specification and prosecution history describe the feature of always clocking the CPU at its maximum speed as a feature of the invention, and criticize prior art systems lacking this feature. This feature is properly incorporated into the construction of this term. *See, e.g.*, *Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1329–30 (Fed. Cir. 2009) ("Where the specification makes clear that the invention does not include a particular feature, that feature is deemed to be outside the reach of the claims of the patent, even though the language of the claims, read without reference to the specification, might be considered broad enough to encompass the feature in question.") (quoting *SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1341 (Fed. Cir. 2001)).[2]

TPL repeats the same misleading argument it made to Judge Ware, that "[t]he specification of the patents-in-suit discloses multiple embodiments of the various inventions; so many that the PTO required the applicants to divide the original application into 10 separate applications." (Opposition at 11:13–15.) But those supposed "multiple embodiments" did not relate to the clocking mechanism claimed in the '336 patent. As explained in connection with TPL's own motion for reconsideration, the examiner issued a restriction requirement during the prosecution of the '749 patent directing the applicants to file separate divisional applications because the applicants' proposed claims covered distinct inventions (Group I through Group X). Only one of those so-called "multiple embodiments" (Group V) was directed to the clocking features of the disclosed microprocessor system. (08/31/1992 Restriction Requirement, at ¶ 19 (Group V), Chen Decl. Ex. 6, *Acer* Action, Dkt. No. 368-7.)[3]

The applicants were forced to file separate divisional applications because their claims were directed at "independent and distinct inventions," 35 U.S.C. § 121, not because they covered multiple embodiments of a single invention, as TPL now suggests. With respect to the clocking features of the disclosed microprocessor system, their entire detailed description is contained in a

[2] TPL misleadingly suggests that Judge Ward construed this phrase in the previous Texas litigation involving the '336 patent, but he did not. Judge Ward construed a narrower and different phrase directed to what an "oscillator" was, not how the CPU was clocked. (See Ward Order at 13, Otteson Decl. Ex. 3, *Acer* Action, Dkt. No. 357-3.)

few passages between columns 16 and 17 of the specification. ('336, 16:44–17:37, *Acer* Action, Dkt. No. 358-6). The "ring oscillator" described in those passages is the only disclosed embodiment for clocking the CPU.

1. TPL's Attempt To Recapture the Prior Art Should Be Rejected.

TPL argues that nothing in the specification or the prosecution history "requires the clock operate at the fastest possible speed; rather, the embodiment discussed merely allows the clock to operate at a fastest possible speed." (Opposition at 12:10-11 (emphasis in original).) This argument cannot be reconciled with the plain language of the specification, which states that "[b]y deriving system timing from the ring oscillator 430, CPU 70 will ***always*** execute at the maximum frequency possible, but never too fast." ('336, 16:63–17:2, Chen Decl. Ex. 5, *Acer* Action, Dkt. No. 358-6; *see also id.*, 17:19–21 ("The CPU 70 executes at the fastest speed possible using the adaptive ring counter[ ] clock 430.").)

But more fundamentally, a system that merely allows the CPU clock to operate at the fastest possible speed would recapture the prior art systems that TPL distinguished in the '336 specification and during prosecution. The specification explains that prior art CPUs were clocked at a "rated clock speed" to achieve best performance under worst case conditions. (*Id.*, 16:47–53.) Those prior art systems, therefore, ***will*** operate at the fastest possible speed ***under those worst case conditions***. (*See* Amendment, 1/13/97, at 3–4, Chen Decl. Ex. 8, *Acer* Action, Dkt. No. 358-9 ("In contrast, prior art microprocessor systems are given a rated speed based on possible worst case operation conditions . . . . Under other than worst case operating conditions, the prior art microprocessors are actually capable of operating at a faster clock speed than their rated speed.").) Construing this phrase to merely allow the CPU to sometimes operate at its maximum frequency, therefore, would recapture indisputably disclaimed prior art systems.

The purported advantage of the alleged invention's use of an on-chip oscillator clock is that the clock "always" adjusts to maintain the same relationship with the CPU's maximum speed. If voltage, temperature, or other conditions cause the CPU's maximum speed to drop, these conditions "always" cause a corresponding change to the on-chip oscillator clock's frequency as well. ('336, 16:63–17:2, Chen Decl. Ex. 5, *Acer* Action, Dkt. No. 358-6.) The construction of

"clocking said CPU" must therefore not merely allow, but require, that the CPU always execute at the maximum frequency possible.

2. Plaintiffs' Proposed Construction Is Not Vague or Ambiguous.

TPL asserts that Plaintiffs' construction that the CPU "will always execute at the maximum frequency possible, but never too fast" is vague and ambiguous. (Opposition at 13.) TPL further asserts that the construction specifies no criteria to enable a jury to determine the "maximum frequency possible" or whether the CPU is going "too fast." TPL's own statements, however, debunk such an assertion. TPL had no trouble at all understanding the "fastest speed possible" (*i.e.*, "maximum frequency possible") of the CPU to mean "the upper end of the range of speeds at which the CPU can operate." (*See* Pls.' Claim Construction Brief at 24, *Technology Properties Ltd. et al. v. Fujitsu et al.*, 05-cv-00494-TJW, Dkt. No. 220 (Supplemental Decl. of Kyle Chen in Support of Motion for Reconsideration, Ex. 10).) Citing its own expert declaration, TPL further explained that the fastest speed possible is "the maximum frequency a CPU can operate at and still provide a valid output." (*Id.*) TPL even explained that, when "the frequency of a CPU exceeds its maximum theoretical performance," *i.e.*, when the frequency is "too fast," "errors are likely to result." (*Id.*) TPL thus has no basis to argue that a construction based on the applicants' own statements in the specification and prosecution history is either vague or ambiguous.

III. CONCLUSION

For the foregoing reasons, Plaintiffs' motion for reconsideration should be granted in its entirety.

Dated: November 9, 2012

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ATTESTATION PER GENERAL ORDER 45

I, Edward Runyan, am the ECF User whose ID and password are being used to file Corrected Plaintiffs' Consolidated Opening Supplemental Claim Construction Brief. In compliance with General Order 45, X.B., I hereby attest that the counsel listed above have concurred with this filing.

Dated: November 9, 2012

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00877 PSG (Related to Case Nos. 5:08-cv-05398 JF and 5:08-cv-00877 JF) **SUPPLEMENTAL DECLARATION OF KYLE D. CHEN IN SUPPORT OF MOTION FOR RECONSIDERATION OF CERTAIN ASPECTS OF FIRST CLAIM CONSTRUCTION ORDER** Date: November 30, 2012 Time: 10:00 a.m. Place: Courtroom 5, 4th Floor Judge: Paul Singh Grewal
HTC CORPORATION, HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED, Defendants.	Case No. 5:08-cv-00882 PSG

BARCO N.V., a Belgian corporation, Plaintiff, v. TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORP., ALLIACENSE LTD., Defendants.	Case No. 5:08-cv-05398 PSG

I, Kyle D. Chen, declare:

1. I am an attorney at the law firm of Cooley LLP, counsel in this action for Plaintiffs HTC Corporation and HTC America, Inc. (collectively "HTC"). I make this declaration in support of Plaintiffs' Motion for Reconsideration of Certain Aspects of First Claim Construction Order. I have personal knowledge of the facts contained within this declaration, and if called as a witness, could testify competently to the matters contained herein.

2. Attached to this declaration as **Exhibit 10** is a true and correct copy of Plaintiffs Technology Property Limited's and Patriot Scientific Corporation's Claim Construction Brief, filed on March 19, 2007 (Dkt. No. 217) in *Technology Properties Limited, Inc. v. Fujitsu et al.*, Case No. 05-cv-00494 in the United States District Court for the Eastern District of Texas.

I declare under penalty of perjury that to the best of my knowledge the foregoing is true and correct. Executed on November 9, 2012 in Palo Alto, California.

/s/ Kyle D. Chen
Kyle D. Chen

EXHIBIT 10

UNITED STATES DISTRICT COURT

EASTERN DISTRICT OF TEXAS

MARSHALL DIVISION

Technology Properties Limited, Inc. and Patriot Scientific Corporation, Plaintiffs, v. Matsushita Electrical Industrial Co., Ltd., Panasonic Corporation of North America, JVC Americas Corporation, NEC Corporation, NEC Electronics America, Inc., NEC Corporation of America, NEC Display Solutions of America, Inc., NEC Unified Solutions, Inc., Toshiba Corporation, Toshiba America, Inc., Toshiba America Electronic Components, Inc., Toshiba America Information Systems, Inc. and Toshiba America Consumer Products, LLC, Defendants.	§	Case No. 2:05-CV-00494 (TJW) **JURY TRIAL DEMANDED**

PLAINTIFFS TECHNOLOGY PROPERTY LIMITED'S AND PATRIOT SCIENTIFIC CORPORATION'S CLAIM CONSTRUCTION BRIEF

TABLE OF CONTENTS

TABLE OF CONTENTS(con't)

TABLE OF CONTENTS(con't)

TABLE OF CONTENTS(con't)

TABLE OF AUTHORITIES

Page

Cases

TABLE OF AUTHORITIES (con't)

Page

Other Authorities

Treatises

I. INTRODUCTION

Charles Moore ("Moore") and Russell Fish ("Fish") are co-inventors named in the patents-in-suit. Between late 1988 and 1989, Moore[1], with Fish's help, designed a 32-bit Forth-based microprocessor, which Moore and Fish named "ShBoom." On August 3, 1989, Moore and Fish filed a comprehensive microprocessor patent application. The patent examiner issued a restriction requirement finding that the original application contained ten separate inventions and seven patents, including the patents-in-suit, ultimately issued.

Moore subsequently assigned his rights and interest in the seven patents, including the patents-in-suit, to TPL, in return for a royalty interest, and currently serves as the Chief Technology Officer of TPL and its affiliates. TPL and its affiliated companies specialize in the development, commercialization and management of intellectual property assets, including the patents-in-suit. On the product development side, utilizing licensing proceeds, TPL and Moore are developing specialized microprocessors that utilize the inventions claimed in the patents-in-suit for use in hearing aid and listening devices.

Patriot is the assignee of Fish's rights in and to the patents-in-suit. Historically, Patriot developed hybrid RISC-stack technology, which resulted in smaller, lower power, less expensive system-on-chip designs. Today Patriot is an intellectual property licensing company that develops, markets and enables innovative proprietary technologies.

TPL and Patriot have together licensed the patents-in-suit to more than a dozen companies, including Intel, Hewlett Packard, Fujitsu, NEC Corp., and Sony.

II. LEGAL STANDARD GOVERNING CLAIM CONSTRUCTION

A. The Role of Claim Construction in a Patent Infringement Suit

Patent infringement analysis entails two steps. First determine the meaning and scope of

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[1] Moore created the powerful Forth computer language in the mid-1970s for programming of one of the world's first radio telescope installations at Kitt Peak, and, in the early 1980s, designed unique microprocessors and architectures optimized for the Forth language. These microprocessors were remarkably powerful and very popular with NASA and related aerospace projects. Harris Corporation took one of Moore's designs to market as one of the world's first commercially successful Reduced Instruction Set Computing ("RISC") microprocessors.

the patent claims asserted to be infringed, and second compare the properly construed claims to the accused infringing device. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 976 (Fed. Cir. 1995) (*en banc*), *aff'd,* 517 U.S. 370 (1996). Claim construction is determined as a matter of law. *Markman*, 517 U.S. 370, 372 (1996).

B. Claim Construction Methodology

The Federal Circuit decided *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005), *en banc* to resolve the raging controversy over proper claim construction methodology.[2] In *Phillips*, the court criticized the *Texas Digital* approach to claim construction, with its heavy reliance on general dictionary definitions, which the court concluded was inconsistent with years of claim construction precedent,[3] and restored the proper methodology for claim construction -- placing primary emphasis on the intrinsic record, including the claims, the specification, and the prosecution history, and relegating extrinsic evidence, including dictionary definitions, to secondary status.

1. Claim Terms Are Given Their Ordinary and Customary Meaning To One of Ordinary Skill in the Art At the Time of Invention

Claim construction begins by inquiring into how a person of ordinary skill in the art would understand the claim term at the time of the effective filing date of the patent application. *Phillips*, 415 F.3d at 1313. This inquiry is "based on the well-settled understanding that inventors are typically persons skilled in the field of the invention and that patents are addressed to and intended to be read by others of skill in the pertinent art." *Id.*, citing *Multiform Desiccants, Inc. v. Medzam, Inc.*, 133 F.3d 1473, 1477 (Fed. Cir. 1998).

Claim construction requires analysis of terms that have a particular meaning in a field of

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[2] Prior to *Phillip*s, two conflicting approaches to claim construction had developed, a contextual approach based on *Markman*, and a dictionary definition approach best exemplified by *Texas Digital Systems, Inc. v. Telegenix, Inc.*, 308 F.3d 1193 (Fed. Cir. 2002).

[3] The Court found that "the *Texas Digital* approach limits the role of the specification in claim construction to serving as a check on the dictionary meaning of a claim term" and that "assigning such a limited role to the specification was inconsistent with precedent that the specification is the 'single best guide to the meaning of a disputed term.'" *Phillips*, 415 F.3d at 1320-21, *quoting Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996).

art. Because the meaning of a claim term as understood by persons of skill in the art is often not immediately apparent to a layperson (or the Court), "the court must examine the claims, the specification, the prosecution history, and extrinsic evidence concerning the background of the technology, the meaning of technical terms and the state of the art to determine what a person of skill in the art would have understood the term to mean." *Phillips*, 415 F.3d at 1314.

2. The Claims Are of Primary Importance in Claim Construction

Claims are of primary importance in claim construction. *Phillips*, 415 F.3d at 1314, *citing Vitronics*, 90 F.3d at 1582. ("The claims themselves provide substantial guidance as to the meaning of particular claim terms.") Courts should look at the context in which a claim term is used in the claim to determine its proper meaning. *Id.*; *see also ACTV, Inc. v. Walt Disney Co.*, 346 F.3d 1082, 1088 (Fed. Cir. 2003) ("the context of the surrounding words of the claim also must be considered in determining the ordinary and customary meaning of those terms"). Other claims of the patent, both asserted and unasserted, also can shed light on the meaning of a claim term. *Phillips*, 415 F.3d at 1314, *citing Vitronics*, 90 F.3d at 1582 ("Because claim terms usually are used consistently throughout a patent, the usage of a term in one claim can often illuminate the meaning of the same term in other claims."). Where a particular limitation is added in a dependent claim, there is a presumption that the limitation is not present in the independent claim. *Id.* at 1315, *citing Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 910 (Fed. Cir. 2004).

3. The Specification Is the Single Best Guide to Claim Construction

The specification is of paramount importance in claim construction. For purposes of claim construction, the claims "do not stand alone," but rather are part of "'a fully integrated written instrument.'" *Phillips*, 415 F.3d at 1315, *quoting Markman*, 52 F.3d at 978-79. The claims "must be read in view of the specification, of which they are a part." *Id.* The specification "is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term." *Phillips*, 415 F.3d at 1315, *quoting Vitronics*, 90 F.3d at 1582.

A patentee's lexicography, either explicit or implicit, controls the meaning of the claim

term. *Phillips,* 415 F.3d at 1316 ("The specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such cases, the inventor's lexicography governs."). Where the specification reveals an intentional disclaimer, or disavowal of claim scope by the inventor, that intention is dispositive. *Phillips*, 415 F.3d at 1316, *citing SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc.*, 242 F.3d 1337, 1343-44 (Fed. Cir. 2001).

4. Importation of Limitations From the Specification Is Improper

Importing limitations from the specification into the claims is improper. Although "the distinction between using the specification to interpret the meaning of a claim and importing limitations from the specification into the claim can be a difficult one to apply in practice," the line should be reasonably clear if the district court remains focused on how a person of ordinary skill in the art would understand the claim terms. *Phillips*, 415 F.3d at 1323. Reading the specification in context will usually inform the court whether the patentee is setting out specific examples of the invention or whether the patentee instead intends for the claims to cover only the described embodiments in the specification. *Id.*; *see also SciMed Life Sys.*, 242 F.3d at 1341. Where the specification describes specific embodiments, the claims should not be confined to those embodiments. *Phillips, 415 F.3d at 1323; see also Nazomi Communications, Inc. v. ARM Holdings, PLC*, 403 F.3d 1364, 1369 (Fed. Cir. 2005) (claims may embrace "different subject matter than is illustrated in the specific embodiments in the specification").

5. The Prosecution History Can Inform the Meaning of Claim Terms

The prosecution history is part of the intrinsic record and can be helpful in claim construction. The prosecution history can "inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be. *Phillips,* 415 F.3d at 1317, *citing Vitronics*, 90 F.3d at 1582-83. However, the prosecution history may be less useful than the specification because it represents an ongoing negotiation between the PTO and the applicant, and often lacks the clarity of the specification. *Phillips*, 415 F.3d at 1317.

6. Extrinsic Evidence Must Be Considered in the Context of Intrinsic Evidence

Extrinsic evidence is all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises. *Phillips*, 415 F.3d at 1317, *quoting Markman*, 52 F.3d at 980. Although extrinsic evidence "can shed useful light on the relevant art," it is "less significant than the intrinsic record in determining 'the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317, *quoting C.R. Bard, Inc. v. U.S. Surgical Corp*., 388 F.3d 858, 862 (Fed. Cir. 2004), *Vanderlande Indus. Nederland BV v. Int'l Trade Comm'n*, 366 F.3d 1311, 1318 (Fed. Cir. 2004). Moreover, extrinsic evidence must be considered in the context of the intrinsic evidence. *Phillips*, 415 F.3d at 1319. Technical dictionaries and treatises may assist the Court in understanding the underlying technology and the way in which one of skill in the art might use the claim terms. *Aquatex Indus., Inc. v. Techniche Solutions*, 419 F.3d 1374, 1380 (Fed. Cir. 2005).

7. The Court Must Attach Appropriate Weight to Dictionary Definitions

Although *Phillips* criticized the *Texas Digital* approach of relying primarily on dictionary definitions to define claim terms, it did not preclude the appropriate use of dictionaries. *Phillips*, 415 F.3d at 1322. Courts are authorized to rely on extrinsic evidence, including dictionaries, as one of many claim construction tools, as long as they attach appropriate weight to dictionary definitions in the context of the intrinsic evidence. *Terlep v. The Brinkmann Corp.*, 418 F.3d 1379, 1382 (Fed. Cir. 2005), *citing Phillips*, 415 F.3d at 1324. Even a non-technical word describing patent technology should take "its definition from the context in which it was used by the inventor." *Tap Pharm. Products, Inc. v. Owl Pharm.*, 419 F.3d 1346, 1354 (Fed. Cir. 2005).

"[H]eavy reliance on the dictionary divorced from the intrinsic evidence risks transforming the meaning of the claim term to the artisan into the meaning of the term in the abstract, out of its particular context, which is the specification." *Phillips*, 415 F.3d at 1321. It is better to focus "at the outset on how the patentee used the claim term in the claims, specification and prosecution history, rather than starting with a broad definition and whittling it down." *Id.*

III. THE '336 PATENT

A. Background of the Technology of the '336 Patent

Dr. Alvin Despain is Emeritus Professor of Electrical Engineering at the University of Southern California, and has been a professor of electrical engineering and/or computer science for over 40 years. He is the author of over 150 technical papers, the founder of four computer technology companies, and an inventor on seven issued U.S. patents.

As Dr. Despain explains in his accompanying Declaration in support of Plaintiffs' Claim Construction Brief, modern microprocessors are amazingly complex machines, with millions of individual parts (transistors), whose operation must be coordinated with the others to avoid collisions. Dr. Despain analogizes the issue of coordinating complex, overlapping operations to a symphony conductor, whose waving of a baton results in the intricate melodies of a symphony. For microprocessors, clock signals are the "baton" that determines the beat. There are many different sources of clock signals, such as quartz crystals and ring oscillators. Despain ¶ 21.[4]

Multiple microprocessor operations must be clocked, such as input/output interfaces and central system operations. Prior to the '336 patent inventions, the system clock generally needed to run synchronously with the slower input/output clock rate, which slowed all microprocessor operations. But the '336 patent teaches a technique to "decouple" the input/output clock and the system clock, allowing them to run independently and therefore allowing the system clock to run faster. Also, the '336 teaches a variable-speed clock circuit that is on the same chip as the microprocessor, and which is subject to the same variations in operating conditions (such as temperature and voltage) as the microprocessor, causing the speed of the clock circuit and the range of operable speeds of the microprocessor to vary together, ensuring that the output of the microprocessor remains valid, even at high speeds. Despain ¶¶ 22-23.

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[4] All references to "Despain" herein refer to the Declaration of Alvin M. Despain in Support of Plaintiffs' Claim Construction Brief.

B. Claim Construction Analysis of the '336 Patent[5]

1. "central processing unit"

This phrase (claims 1-2, 6-10) should be construed to mean "an electronic circuit that controls the interpretation and execution of programmed instructions." Defendants propose construing this phrase as "the central electronic circuit in a computer that controls the interpretation and execution of programmed instructions." Thus, the difference between the parties' proposed constructions is that Defendants' construction requires that the CPU be ***the central*** electronic circuit in a ***computer***. Neither the '336 patent specification nor the understanding of a person of ordinary supports the inclusion of these extraneous limitations. In fact, the '336 patent teaches against limiting the meaning of this phrase as Defendants propose.

The '336 patent specifically teaches that the integrated circuit 312 disclosed in the '336 patent, of which CPU 316 is a part, can be used in applications other than a computer:

> Dramatic changes in price/performance always reshape existing applications and almost always create new ones. The introduction of microprocessors in the mid 1970s created video games, personal computers, automotive computers, electrically controlled appliances, and low cost computer peripherals.
>
> The integrated circuit 312 will find applications in all of the above areas, plus create some new ones. … Interesting product possibilities using the integrated circuit 312 include high speed reading machines, real-time speech recognition, spoken language translation, real-time robot vision, a product to identify people by their faces, and an automotive or aviation collision avoidance system.
>
> A real time processor for enhancing high density television (HDTV) images, or compressing the HDTV information into a smaller bandwidth, would be very feasible.

'336, 9:62-10:12.[6] Thus, Defendants' proposed construction that the CPU must be used in a computer is flatly contradicted by the patent specification.

Also, the '336 teaches an embodiment in which the microprocessor 310, of which CPU

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[5] Plaintiffs have provided a side-by-side comparison chart of Plaintiffs' and Defendants' claim constructions for all three patents-in-suit for the Court's convenience, created from the Joint Claim Construction Statement filed on Feb. 16, 2007, attached hereto as Exhibit 25 of the accompanying Declaration of Roger L. Cook in Support of Plaintiffs Technology Property Limited's and Patriot Scientific Corporation's Claim Construction Brief ("Cook ").

[6] The '336 patent is attached as Cook Exhibit 1.

316 is a part, is used in a ***multiprocessor system***. '336, 9:28-61, 11:64-13:27. According to the specification, "up to 64 CPU 310/RAM 311 processors should be able to intercommunicate" in a multiprocessor system using the microprocessor architecture disclosed in the '336 patent. '336, 9:28-61. In such a system, with an array of 64 microprocessors, each of which contains a CPU, it would be impossible to identify any one of those 64 CPUs as ***the central electronic circuit*** in the system. Therefore, Defendants' proposed limitation is inconsistent with the specification and must be rejected.

2. "microprocessor"

This term (claims 1-10) should be construed to mean "an electronic circuit that executes programmed instructions and is capable of interfacing with input/output circuitry and/or memory circuitry." Defendants propose that this term be construed as "an electronic circuit that uses a central processing unit to interpret and execute programmed instructions." Thus, the parties' proposed constructions differ in that the Defendants omit the requirement that the microprocessor be capable of interfacing with input/output circuitry and/or memory circuitry; and include the extraneous requirement that a microprocessor use a control processing unit.

a) The microprocessor should interface with I/O and/or memory

The '336 specification states that "microprocessor 50 is a very high performance (50 MHz) RISC influenced 32-bit CPU designed to work closely with dynamic RAM;" and that "microprocessor 50 accesses memory via an external 32-bit bus [and most] of the memory 311 for the microprocessor 310 is on the same die 312. External access to more memory is made using an 8-bit bus." '336, 8:56-58, 11:49-54. Thus, the '336 patent specifically teaches that the microprocessor communicates with memory circuitry over either a 32-bit bus or an 8-bit bus, depending upon the amount of DRAM in the microprocessor.

The 32-bit bus used by the microprocessor to access external memory is shown at the bottom of Figure 2 as address/data 151, connected to memory controller 118. This 32-bit data bus is connected to the memory controller 118 of the microprocessor.

While the '336 teaches that this external 32-bit bus can be used to communicate with external memory, it need not communicate with only memory in all instances. If it

communicates with some other device, such as a hard drive, keyboard or monitor, that other device would necessarily have its own input/output circuitry. Despain ¶ 43. In fact, if the microprocessor could not communicate with the input/output circuitry of other devices, then it would not perform any useful function. *Id*. Thus, a person of ordinary skill in the art, reading the '336 patent, would realize that the microprocessor must be able to interface with either the input/output circuitry of another device or memory circuitry (or both).

b) The microprocessor need not use a CPU

The '336 specification does not require the microprocessor to use a central processing unit. Furthermore, the claim language itself shows that a microprocessor may, but does not have to, include a CPU. Independent claims 10 recites "[i]n a microprocessor system including a central processing unit, a method for clocking said central processing unit …." Independent claim 3, on the other hand, recites "[i]n a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit …." Thus, claim 3 refers to clocking the microprocessor, whereas claim 10 refers to clocking the CPU. In fact, whereas every other independent claim recites a central processing unit, claim 3 does not. If differences in the language of the '336 patent claims are to be given effect, then Defendants' extraneous limitation requiring that a microprocessor include a CPU must be rejected.

3. "oscillator"

This term (claims 6-9, also as part of "ring oscillator" in claims 1-5, 10) should be construed to mean "a circuit that is capable of maintaining an alternating output using feedback."

The parties agreed upon the meaning of this commonly understood term until the day the joint claim construction statement was filed, when Defendants submitted a revised definition, ***nearly identical to Plaintiff's definition, except for omitting*** the "using feedback" limitation. Thus, the dispute is whether "oscillator" requires feedback.

Generally speaking, feedback refers to some part of an output of a system that is looped back to the input of that system to control the system from within itself. In this context, feedback is necessary to ***maintain*** oscillation. For example, in a ring oscillator (a type of oscillator

discussed below), feedback means that the output of the last inverter[7] is fed back into the first inverter, forming a ring or loop. This ensures that the alternating signal can continue to propagate around the oscillator circuit once it reaches the end, when it is returned to the beginning. Without feedback, oscillation would be "damped" and quickly die away. This type of transient oscillator could not be used as a system clock for generating signal(s) used for timing the operation of the CPU. Thus, in the context of the claims of the '336 patent, and indeed for almost every ***intentional*** oscillator, the oscillator ***must*** use feedback to be capable of maintaining oscillation.

The literature supports this fact. For example, the textbook *Introduction to Electronic Circuit Design*, in the section on "Positive Feedback and Oscillators," notes that "[o]scillators depend on ***positive feedback*** to keep the oscillation going." Richard R. Spencer and Mohammed S. Ghausi, *Introduction to Electronic Circuit Design* 743 (2001) (emphasis added), Ex. 19.[8] And, for crystal-controlled oscillators, the book *Precision Frequency Control* states that "[n]early all crystal-controlled oscillator circuits may be considered to consist of two essential parts: an amplifier, or gain circuit, and a ***feedback network*** that provides positive feedback at the frequency of oscillation." 2 *Precision Frequency Control: Oscillators and Standards* 47 (1985) (emphasis added), Ex. 20. Because feedback is necessary for an oscillator to maintain oscillation, the Court should adopt Plaintiffs' definition for this term.

4. "ring oscillator"

This term (claims 1-5, 9) should be construed to mean "an oscillator having a multiple, odd number of inversions arranged in a loop."

Defendants' slightly different definition is "an oscillator having an odd number of inverting logic stages connected in a loop." The key differences are Plaintiffs' "inversions"

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[7] As is more fully explained below, an inverter, as its name suggests, "inverts" the output from the input, *i.e.*, if the input is low, the output is high and *vice versa*. If the inverters are arranged in a true ring, there may not be a distinguishable "first" and "last" inverter.

[8] All referenced exhibits are attached to the accompanying Cook Declaration (see footnote 5, *supra*), and will be referenced herein as "Ex. __."

versus Defendants' "inverting logic stages," and Plaintiffs' requirement for a "multiple, odd" number of such inversions, whereas Defendants imply, but do not explicitly require, more than one inverting logic stage.

In a ring oscillator, a signal propagates through an odd number of inversions, arranged in a loop, such that the input signal will invert an odd number of times, and then return to its starting point inverted. At the starting point, this inverted signal will again pass around the loop and again undergo an odd number of inversions, returning to the starting point a second time, now in its original non-inverted state, whereupon the whole process begins anew. The odd number of inversions provide instability that keeps the signal continuously propagating around the loop, alternating each time, so that the ring oscillator can maintain an alternating output.

Plaintiffs' reference to "inversions" arranged in a loop, rather than "inverting logic states," reflects the numerous ways that ring oscillators are implemented. The actual circuitry that implements the "inversions" can vary, as does its description in the literature. Fig. 18 of the '336 shows a series of seven inverters, and the written description does not limit those circuit elements to any specific design. The textbook *Design of Analog CMOS Integrated Circuits* defines a ring oscillator as "a number of gain stages in a loop," and both a five-stage single-ended ring oscillator and a four-stage differential ring oscillator (with three inversions − the fourth stages is non-inverting) are shown at Fig. 14.15. Behzad Razavi, *Design of Analog CMOS Integrated Circuits* 484, 491 (2001), Ex. 21. The article *A 300-MHz CMOS Voltage-Controlled Ring Oscillator* describes a ring oscillator as "an odd-numbered ring of inverting gain stages connected back on itself." S. K. Enam & Asad A. Abidi, *A 300-MHz CMOS Voltage-Controlled Ring Oscillator*, 25 IEEE J. of Solid-State Circuits 312 (1990), Ex. 22. The inverter circuitry in these examples can be digital, analog, or even a hybrid of the two. Plaintiffs' definition properly focuses on the functional nature of the inversions, versus any specific circuitry to implement that functionality. Defendants' definition, in contrast, limits the claim term to digital logic circuitry, which is not required by the claims or taught in the specification. Moreover, even if the inverters shown in Fig. 18 of the '336 patent were a specific type, it would be improper to import such aspects of a preferred embodiment into the claims.

Plaintiffs' requirement of a "multiple," odd number of inversions reflects the reality that a single inverter would not be a feasible implementation of a ring oscillator generally, let alone for use as a system clock. In a one-stage ring oscillator, the inverter's output would be tied to its input, which means that as soon as the output of the inverter switched, the same value would appear at its input, and it would quickly go to a stable and unvarying state, *i.e.*, it would not be capable of maintaining an oscillating output. Stated another way in *Design of Analog CMOS Integrated Circuits*, a single-stage (*i.e.*, single inverter) ring oscillator does not oscillate because the maximum phase shift that can be achieved is 270 degrees, whereas 360 degrees is required: "The loop therefore fails to sustain oscillation growth." Razavi, *supra*, at 485, Example 14.1, Ex. 21. The '336 and the literature are in accord. In '336 Fig. 18, a ***seven-stage*** ring oscillator is shown. The Razavi textbook shows a ***five-stage*** single-ended ring oscillator and a ***four-stage (three inversion)*** differential ring oscillator at Fig. 14.15. Razavi, *supra*, at 491, Ex. 21. The article *A 300-MHz CMOS Voltage-Controlled Ring Oscillator* shows ***three-stage*** ring oscillators. Enam, *supra*, at 313 (*e.g.*, Figs. 1-2), Ex. 22. It is commonly known that ring oscillators are implemented as a "multiple," odd number of inversions. Defendants' definition implicitly acknowledges this fact in that it uses the term "stages," the plural of "stage," but leaves ambiguity that should be avoided.

Plaintiffs' definition, which is more technically consistent with the operation of a ring oscillator from the perspective of one of ordinary skill and is not ambiguous, should be adopted.

5. "an entire ring oscillator variable speed system clock in said single integrated circuit"

This phrase (claims 1-2) should be construed to mean "a ring oscillator that generates the signal(s) used for timing the operation of the CPU, capable of operating at speeds that can change, where the ring oscillator is located entirely on the same semiconductor substrate as the CPU." This, together with the phrases in §§ 6-8, are addressed in §8.

6. "an entire ring oscillator system clock constructed of electronic devices within the integrated circuit"

This phrase (claims 3-5) should be construed to mean "a ring oscillator that generates the signal(s) used for timing the operation of the CPU, where the ring oscillator is located entirely on

the same semiconductor substrate as the microprocessor."

7. "an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking"

This phrase (claims 6-9) should be construed to mean "an oscillator that generates the signal(s) used for timing the operation of the CPU, where the oscillator is located entirely on the same semiconductor substrate as the CPU and is electrically coupled to the CPU."

8. "an entire variable speed clock disposed upon said integrated circuit substrate"

This phrase (claim 10) should be construed to mean "a circuit that generates the signal(s) used for timing the operation of the CPU, capable of operating at speeds that can change, where the circuit is located entirely on the same semiconductor substrate as the CPU."

The parties have substantially disparate definitions for these phrases. While Plaintiffs generally prefer to construe shorter, discrete components of larger phrases ("sub-terms"), Defendants want longer phrases construed. In reality, however, Defendants appear to incorporate their definitions of all sub-terms, and instead focus on the meaning of "entire" in each of these longer phrases. Thus, Defendants' definitions only identify elements that, if present, would purportedly preclude the presence of an "entire" ring oscillator, oscillator, or variable speed clock (i.e., "… does not rely on a control signal or an external crystal/clock generator"). Thus, Defendants' proposed constructions are less like a definition useful to one of ordinary skill in the art, and more like non-infringement arguments in the guise of claim construction.[9]

The phrases in subsections 5 through 8 can be addressed as a group because they are all related, mainly differing in what functional circuit (*i.e.*, ring oscillator for claims 1-5, oscillator for claims 6-9, and variable speed clock for claim 10) is ***entirely*** on the same substrate as the

[9] Defendants' awkward, negatively-phrased definitions are unhelpful to one of ordinary skill in the art attempting to determine the (positive) scope of the claims. Dr. Despain opines that one of ordinary skill in the art would not rely on this type of multi-exception negative limitation to describe a device or its functionality, because its scope would not be clear. Despain ¶ 48. Defendants' approach is a transparent attempt to narrow claim scope that would otherwise cover Defendants' products.

CPU. The other differences are whether the phrases include the "variable speed" and "system clock" limitations, and the specific descriptions for the functional circuit on the same substrate as the CPU. In the larger context, these differences are less significant because each functional circuit is "variable speed," is a "system clock," and is on the same substrate as the CPU.

a) The Specification and File History Support Plaintiffs' Definitions

As Dr. Despain opines, and as discussed above in the context of the shorter sub-terms, Plaintiffs' definitions[10] are supported by the '336 specification and file history. Despain ¶¶ 45-47. For example, the specification describes the operation of the ring oscillator[11] "system clock": "The microprocessor 50 uses the technique shown in Figs. 17-19 ***to generate the system clock*** and its required phases." '336, 17:54-55 (emphasis added). Because Figs. 17-19 illustrate the ring oscillator and its operation, this teaches that the ring oscillator system clock "generates the signal(s) used for timing the operation of the CPU," as provided in Plaintiffs' definition. Also, the specification provides an example of the "variable speed" ring oscillator: "The ring oscillator frequency is determined by the parameters of temperature, voltage, and process. At room temperature, the frequency will be in the neighborhood of 100 MHz. At 70 degrees Centigrade, the speed will be 50 MHz." '336, 16:59-63. In this example, the ring oscillator changes speed with variations in temperature, demonstrating that the variable speed ring oscillator is "capable of operating at speeds that can change," as provided in Plaintiffs' definition.

The specification also teaches that the "entire" ring oscillator is located on the same substrate as the CPU: "Clock circuit 430 is the familiar 'ring oscillator' used to test process performance. The clock is fabricated on the same silicon chip as the rest of the microprocessor 50." '336, 16:56-58. This confirms that the "entire" ring oscillator is "located entirely on the same semiconductor substrate as the microprocessor," as provided in Plaintiffs' definition. Dr. Despain cites additional support from the specification and prosecution history. Despain ¶¶ 45-

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[10] Dr. Despain considers the four phrases under discussion as functionally equivalent for claim construction purposes. *See* Despain, ¶¶ 59-64.

[11] While a ring oscillator (claims 1-5) is discussed in this and other examples, the same reasoning applies equally to an oscillator (claims 6-9) and a variable speed clock (claim 10).

47. As shown, Plaintiffs' definitions conform to the teachings of the '336 and its intrinsic record.

b) Defendants' Definitions Rely Entirely on Questionable Portions of the File History

Defendants' definitions improperly import limitations having no support in the specification or claims, solely relying on the file history.[12] This reliance is dubious at best. In some cases, Defendants appear to misread the file history, in other cases they appear to take statements out of context, and in others cases there appears to be no support at all. These problems reflect the difficulty in relying on the prosecution history for claim construction, as noted by the Federal Circuit in *Phillips*: "[B]ecause the prosecution history represents an ongoing negotiation between the PTO and the applicant, rather than the final product of that negotiation, it often lacks the clarity of the specification and thus is less useful for claim construction purposes." *Phillips*, 415 F.3d at 1317. The incongruities between Defendants' proposed definitions and the statement in the file history are discussed further below.

c) Defendants Seek Three Separate Disclaimers Based on an Erroneous Reading of the File History, but Cannot Meet the Stringent Federal Circuit Requirements for Disclaimer.

Defendants appear poised to argue that Plaintiffs have "disclaimed" reliance on "a control signal" or "an external crystal/clock generator." However, "for prosecution disclaimer to attach, [Federal Circuit] precedent requires that the alleged disavowing actions or statements made during prosecution be both ***clear*** and ***unmistakable***." *Omega Engineering, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1325-26 (Fed. Cir. 2003) (emphasis added). "[T]he prosecution history may not be used to infer the intentional narrowing of a claim absent the applicant's ***clear disavowal*** of claim coverage, such as an amendment to overcome a rejection." *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1327 (Fed. Cir. 2003) (emphasis added). Here, the patent applicants made no clear and unmistakable disavowal of claim coverage.

Defendants' definitions depend on three alleged "entire ring oscillator" *et al.* limitations: the circuit cannt rely on a "control signal," an "external crystal," or an "external clock generator."

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[12] This is based on the fact that the definitions bear some resemblance to statements made in the prosecution history, but have no apparent connection to the claims or specification.

(1) Control Signal

For "control signal," the Defendants apparently look to prosecution history remarks distinguishing the Sheets reference. Sheets teaches a voltage-controlled oscillator ("VCO") whose frequency can be programmed by the CPU.[13] Despain ¶ 54. To distinguish Sheets, applicants noted that the invention of the '336 patent did not require a "command input" to change speeds, but rather changed automatically in conjunction with variations in operating parameters (*e.g.*, voltage and temperature). *Id*. The discussion in the prosecution history centered on the nature of the variable-speed operation of the VCO − whether programmed from a command input as in Sheets, or automatic due to variations in voltage and temperature as in the '336 − not on which classes of VCOs qualified as "entire ring oscillators" or "entire oscillators" based on their control mechanisms. *Id.*

Yet, Defendants rely on these statements to exclude all uses of a "control signal" in conjunction with a ring oscillator / oscillator / variable speed clock, even though the file history discussion concerned the more narrow "command input." The broader term "control signal" advanced by Defendants arguably includes any signal used to control a circuit, regardless of purpose. Despain ¶ 53. Applicants plainly did not disclaim all oscillators and ring oscillators using any type of control signal, such as ***voltage-controlled*** oscillators and ***current-controlled*** oscillators, which use voltage and current respectively to control oscillator operation.[14] *Id.* This is a misreading and distortion of the prosecution history, which becomes a double error when Defendants read that distorted interpretation into the claims as a limitation, as the Federal Circuit cautions against. *See Storage Technology Corp. v. Cisco Systems, Inc.*, 329 F.3d 823, 831 (Fed. Cir. 2003) (noting there is a "fine line between reading a claim in light of the written description

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[13] The precise location of the VCO, whether on-chip or off-chip, was the subject of dispute between the applicants' attorney and the examiner, and never resolved. *See, e.g.*, Off. Action 7/08/96 at 4, Ex. 5; Amd. 1/08/97 at 4, Ex. 6. Instead, the examiner dropped his rejection based on Sheets and asserted a new prior art reference, Magar, in a subsequent office action. *See* Off. Action 4/03/97, Ex. 7.

[14] This fact alone renders Defendants' definition nonsensical, as under this definition the Sheets' VCO would be excluded as an "entire ring oscillator," yet the teachings of Sheets are the basis for the alleged disclaimer of any reliance on a "control signal."

and relevant prosecution history, and reading a new limitation into the claims," which is "improper").

(2) External Crystal

For the "external crystal" limitation, Defendants apparently rely on prosecution history remarks distinguishing the Magar reference. Magar teaches a traditional crystal oscillator in conjunction with a clock generator to provide internal timing signals. Despain ¶ 49. Magar utilizes an external (off-chip) crystal to oscillate, *i.e.*, to maintain an alternating output, which is in turn connected to the on-chip clock generator circuit. The on-chip clock generator modifies the output of the oscillator to provide timing signals for the CPU, but it is the external crystal that determines the frequency or rate of those timing signals in accordance with the fixed frequency of the crystal. *Id.*; Amd. 7/03/97 at 4, Ex. 8. Because the external crystal is not on the same semiconductor substrate as the CPU, it is not subject to the same variations in operating conditions (such as temperature or voltage) or manufacturing variations as the CPU, and will not vary accordingly. *Id*.

In contrast to the conventional crystal oscillator of Magar, the oscillator of the '336 invention is variable speed, and does change in frequency with respect to variations in voltage, temperature, and process parameters on the substrate. Despain ¶ 50. Also, changes in frequency of the oscillator vary together with changes in frequency of the CPU. These benefits are achieved because the '336 invention utilizes an "entire" oscillator on the same semiconductor substrate as the CPU. *Id*. Applicants explain these facts in detail in the file history. *See* Ex. 8; Amd. 2/06/98, Ex. 9. However, Defendants appear poised to use these statements made to distinguish over the traditional crystal oscillator of Magar, by taking them out of context, and then arguing that they are a sweeping, universal disclaimer of all types and uses of external crystals. But given that only one use of an external crystal − a traditional crystal oscillator − was being considered, there is no "clear and unmistakable" intent to disclaim all uses of external crystals. Despain ¶ 52.

As Dr. Despain explains, there are other uses of an external crystal in conjunction with a system clock that were not considered in the prosecution history. For example, a delay-locked

loop (DLL) uses an external crystal not to directly generate the system clock signal like a crystal oscillator, but rather to function as a reference signal against which the internal distribution of that reference can be adjusted ("phase-locked") to account for delay across certain circuit elements. *See* Despain at ¶ 51. To read the applicants' statements as a complete disclaimer of all external crystals that could work in any manner with the '336 invention, such as a DLL, would be inconsistent with patentees' right to seek broad patent coverage. ("To balance the importance of public notice and the right of patentees to seek broad patent coverage, we have thus consistently rejected prosecution statements too vague or ambiguous to qualify as a disavowal of claim scope." *Omega*, 314 F.3d at 1325.)

(3) External Clock Generator

Defendants' third proposed exclusion, "external … clock generator," appears equally unsupported, although it is not entirely clear what Defendants are proposing. While the full proposed exclusion is actually "external crystal/clock generator," a crystal and a clock generator are two different things. Despain ¶¶ 55, 57. A crystal (like in Magar) is often used as an oscillator, whereas a clock generator modifies the output of an oscillator, so there is no equivalence between the two − Defendants' slash ("/") notwithstanding. *Id.* ¶ 57. Also, the only clock generator even discussed in the file history was the ***on-chip*** clock generator in Magar, so it is unclear where Defendants derive support, if any, for an ***external*** clock generator. Despain ¶ 55. Nor was the presence or absence of an on-chip clock generator a basis for distinguishing the '336 invention over Magar, with the focus instead on the "entire" oscillator on the same semiconductor substrate as the CPU, as discussed above. The clock generator of Magar was significant only to the extent that it alone was not an "entire" oscillator as required by the claims of the '336 patent. *Id.* ¶ 55.

Several statements in the prosecution history, at first glance, look similar to Defendants' proposed exclusion of "external clock generator," but in reality are fundamentally different. There are at least three sentences in the file history that reference "a crystal or ***external generator***" (2x), and "an external crystal or ***external frequency generator***" (1x). It is possible that Defendants were considering these statements when they proposed the "external

crystal/clock generator" exclusion. However, an external generator or external frequency generator has nothing to do with an external ***clock*** generator. An external frequency generator is simply an off-chip oscillator, an example of which is a crystal oscillator. Despain ¶ 57. Hence, a crystal and an external frequency generator are often equivalent, as reflected in the prosecution history by, *e.g.,* the reference to "a crystal (or external generator)." Ex. 9. It would appear that Defendants' proposed exclusion may be a misreading of the file history, mistakenly equating or confusing an external frequency generator with an external clock generator, rather than recognizing that these are two different things. As such, this exclusion is inconsistent with how one of ordinary skill would view the scope of the '336 claims. Despain ¶ 57.

Because Plaintiffs' §§5-8 definitions conform to the specification and prosecution history, whereas Defendants' definitions would add unsupported, improper, and unduly restrictive limitations/exclusions, Plaintiffs' definitions should be adopted.

9. "variable speed"

This term (claims 1-5, 10) should be construed to mean "capable of operating at speeds that can change." This term is also discussed in the context of the longer phrases in which it appears, such as "an entire ring oscillator variable speed system clock" (claims 1-2), above.

Plaintiffs' construction is supported by the claims and specification, while Defendants' definition ("a speed (frequency) that is not tightly controlled and varies more than minimally") is unduly restrictive and not supported. The '336 specification describes changes in frequency (*i.e.*, "speed") for the ring oscillator (claims 1-5), oscillator[15] (claims 6-9), and variable speed clock (claim 10) in response to variations in operating conditions, such as temperature and voltage, and due to manufacturing variations. The specification describes the effects of temperature on the speed of the ring oscillator: "The ring oscillator frequency is determined by the parameters of temperature, voltage, and process. At room temperature, the frequency will be in the neighborhood of 100 MHz. At 70 degrees Centigrade, the speed will be 50 MHz." '336, 16:59-

[15] While the "oscillator" element in claims 6-9 is not explicitly referred to as "variable speed," it is clear from the context of these claims that this feature also applies to the oscillator.

63. Thus, the specification discloses a ring oscillator capable of operating at speeds that can change.

In contrast to Plaintiffs' straightforward, supportable definition, Defendants rely on a prosecution history statement characterizing a structure unrelated to the present invention (*i.e.*, the fixed-frequency external crystal of the prior-art Magar reference, *see* Ex. 8), created the inverse of that statement, and attempt to apply this inverse statement as a fundamental limitation of the '336 invention. But this proposal is based on the following logical fallacy: Since applicants were distinguishing over Magar, and because the Magar clock includes a crystal, which has the attributes of being fixed-frequency, having a tightly-controlled speed, and varying minimally, applicants therefore [allegedly] disclaimed all devices that have these attributes. However, in characterizing the external crystal of Magar's traditional crystal oscillator, applicants were not defining the ***scope*** of the claimed invention, but rather describing the teachings of a single reference. Once again, Defendants attempt to take statements made in the prosecution history, remove their context, and apply them as broad, wide-ranging disclaimers. This is contrary to the Federal Circuit restrictions on applying prosecution history disclaimer, see *Omega,* 334 F.3d at 1325-26, and is inconsistent with how one of ordinary skill would interpret the file history.

10. "system clock" and "variable speed clock"

These terms ("system clock" in claims 1-5, "variable speed clock" in claim 10) should be construed to mean "a circuit that generates the signal(s) used for timing the operation of the CPU." Defendants would narrow this definition by adding that the system clock circuit "is itself responsible for determining the frequency of" the timing signal(s).

Plaintiffs' construction is consistent with the intrinsic evidence. For example, the '336 specification describes generation of signals used for timing the CPU, stating that "[t]he microprocessor 50 uses the technique shown in Figs. 17-19 to generate the ***system clock*** and its required phases." '336, 16:54-55 (emphasis added). As shown in these figures, a "ring oscillator 430 is useful as a ***system clock***, with its stages 431 producing phase 0-phase 3 outputs as shown in Fig. 19." '336, 16:63-65 (emphasis added). The specification also refers to "***deriving*** system timing from the ring oscillator 430. '336, 16:67 (emphasis added). From these passages, it

follows that ring oscillator 430 is an example of a system clock because it generates signals used for timing operation of the CPU. Despain §§ 45-46.

Defendants' proposed construction finds no support in the intrinsic evidence and adds ambiguity to the term. What would this exclude? Such a construction would ***itself*** need construction. Defendants' proposed construction should be rejected.

11. "oscillator clocking"

Plaintiffs do not believe that this term (claims 6-9) needs to be construed by the Court, since it is part of the larger phrase "an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking" discussed above. Addressing this particular sub-term in the abstract as a stand-alone term does not make sense in the larger context of the claims. However, if the Court determines to construe this phrase, it should mean "the oscillator generates the signal(s) used for timing the operation of the CPU."

Defendants' separate construction of this sub-term narrows the claim to try to avoid infringement. *See* Plaintiffs' discussion regarding the Defendants' definitions for "system clock" and "variable speed clock," subsection 10, for which Defendants' definitions are nearly identical to their definition for this term. If it decides to separately construe this phrase, the Court should adopt Plaintiffs' definition for the same reasons expressed regarding "system clock" and "variable speed clock."

12. "processing frequency capability"

This phrase is addressed in section 13.

13. "processing frequency"

"Processing frequency capability" should be construed as "the range of speeds at which the CPU can operate," and "processing frequency" should be construed as "the speed at which the CPU operates." Defendants would construe "processing frequency capability" as the "fastest safe operating speed (frequency) at which the CPU can operate" and "processing frequency" as the "fastest safe operating speed (frequency) at which the CPU operates." The main difference between the parties is Defendants' improper inclusion of the "fastest safe operating speed (frequency)" in both constructions.

The '336 specification describes one embodiment where the microprocessor has a ring oscillator serving as a system clock. '336, 16:43-17:37. The specification never mentions "fastest safe operating speed" or any similar language. In its description of this embodiment, however, the '336 states that "[by] deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast." '336, 16:67-17:2. Thus, the '336 introduces the concept of the CPU operating at its maximum possible frequency with regard to one embodiment. This is the closest the specification comes to describing a "fastest safe operating speed." The language "maximum possible frequency" is not, however, included in the claim language. Rather, the claims use the phrases "variable [processing] frequency" and "varying the processing frequency."

The patentees mentioned a "fastest safe operating speed" only in responding to an office action rejecting the pending claims over U.S. Patent No. 4,670,837 (the "Sheets Patent"):

> In the interview [with the examiner], the fact that operating characteristics of electronic devices in an integrated circuit will track one another depending on variations in the manufacturing process used to make the integrated circuit was discussed …. This fact is utilized in the present invention to provide a ***variable speed clock*** for the microprocessor, with the clock speed varying in the same way as variations in the operating characteristics of the electronic devices making up the microprocessor. This ***allows*** the microprocessor to operate at its ***fastest safe operating speed***, given its manufacturing process or changes in its operating temperature or voltage.

Ex. 6 (emphasis added). According to this, the invention uses a variable speed clock. While this means that the microprocessor is ***capable*** of operating at its fastest safe operating speed, it does not mean that the microprocessor ***must*** operate at its fastest safe operating speed in all instances. The only potentially limiting characterization made by the patentees was that the "present invention" includes a variable speed clock; however, the claim is in fact limited to ***variable speed*** (as noted above),whereas ***variable speed*** is not limited to the ***fastest safe operating speed***.

Defendants' proposed constructions attempt to impermissibly read limitations from the specification into the claims. *NCube Corp. v. Seachange, Int'l, Inc.*, 2006 U.S. App. LEXIS 631 (Fed. Cir. Jan. 9, 2006) (improper to read a limitation "into a claim from the specification wholly apart from any need to interpret what the patent meant by particular words or phrases in the claim."). Therefore, Defendants' proposed constructions should be rejected.

Plaintiffs' proposed constructions of "processing frequency capability" and "processing frequency" differ in that the former is defined as a range of speeds, whereas the latter is defined as a single speed. These differences take into account the plain meaning of the common English word "capability." In combination with the phrase "processing frequency," "capability" means the processing frequencies at which the processor ***can*** operate (as opposed to the processing frequency at which the processor ***actually*** operates). Persons of ordinary skill in the art would understand that a processor can operate over a range of frequencies, not just at one frequency.

14. "varying together" and "vary together" and "varying . . . in the same way" and "varying in the same way"

These terms ("varying together" in claims 1-2, "vary together" in claims 3-5, "varying … in the same way" in claims 6-9, and "varying in the same way" in claim 10) should be construed to mean "both increase or both decrease." Defendants' narrower definition requires that the increasing or decreasing be "by the same amount," *i.e.*, in a 1-to-1 ratio.

While these terms are slightly different, they can benefit from a common definition because they refer to the same general concept. In context, the specific items that vary together change somewhat, but the functional nature of how those items vary together remains constant. Defendants apparently agree because they similarly offer a single definition for all of these terms. For purposes of discussion, the speed of the ring oscillator will be considered in the context of "varying together" with the processing frequency capability (*i.e.*, the range of speeds at which the CPU can operate), as specified in claim 1-2, but it should be understood that the rationale is equally applicable to the varying together of the other parameters in the other claims.

Plaintiffs' definition conforms to the '336 specification and prosecution history. The '336 refers to the "propagation delays" of transistors, which is the amount of time it takes before the output of a transistor becomes valid after being provided with an input, also known as the "switching speed" of the transistor. Despain ¶ 66. This is loosely analogous to the time required to turn on a lightbulb, *i.e.*, from the step of turning on the light until the bulb actually illuminates, during which time the switch must be flipped and electricity must travel from the now-connected power circuit to the bulb. Transistor propagation delays are affected by things like operating parameters, such as voltage, temperature, and variations in manufacturing processes. *Id.*

Dr. Despain describes how the changes in the propagation delays of the individual transistors affect the components of the '336 invention. *Id.* First, the speed of the ring oscillator (as an example) will change based on variations in the operating conditions like temperature and voltage. For example, as a chip gets warmer, the transistors on that chip slow down, and hence its system clock (ring oscillator) will slow down. The specification describes the ring oscillator frequency in one example as 100 MHz at room temperature (*e.g.*, 20 degrees Centigrade), which changes to 50 MHz at 70 degrees Centigrade. '336, 16:59-63. The present speed of the ring oscillator will also affect the present speed of the CPU, since the CPU is clocked by the signals generated by the ring oscillator. Despain ¶ 66.

A second effect of the changes in transistor propagation delays is on the ***range*** of speeds at which the CPU can operate (*i.e.*, the processing frequency capability), which correspondingly changes in accordance with variations in temperature, voltage, and process parameters. *Id.* at ¶ 67. As the specification notes, in one embodiment, the CPU executes at the fastest speed possible (*i.e.*, at the upper end of the range of speeds at which the CPU can operate), while "[s]peed may vary by a factor of four depending upon temperature, voltage, and process." '336, 17:19-22. Dr. Despain notes that the fastest speed possible is the maximum frequency a CPU can operate at and still provide a valid output. Despain ¶ 67. The specification also refers to this as the "maximum theoretical performance." '336, 16:50-53. If the frequency of a CPU exceeds its maximum theoretical performance, this generally means that the switching speeds of the transistors have been exceeded, and errors are likely to result.

Collectively, the change in speed of the ring oscillator, and the change in the processing frequency capability of the CPU, vary together. The specification discusses how the speed of the ring oscillator and the processing frequency capability of the CPU vary together, because the ring oscillator and the CPU are made of transistors located on the same semiconductor substrate. As such, they are subject to the same changes in transistor propagation delays resulting from variations in voltage, temperature, etc. Despain ¶¶ 66-68. Thus, a reduction in the switching speed of the transistors results in a decrease in the range of speeds over which the CPU can operate, but this is offset by a reduction in the switching speed of the transistors of the ring

oscillator and the resulting decrease in the operational speed of the ring oscillator. In other words, ***both*** the speed of the ring oscillator and the processing frequency capability of the CPU ***decrease***. This ensures the output of the CPU remains valid. *Id*. at ¶¶ 68, 70. As Dr. Despain notes, the file history refers to the varying together as occurring "similarly" and "automatically." *Id*. at ¶ 69.

Defendants would narrow this term by requiring that the increasing or decreasing be in an exact 1-to-1 ratio ("… by the same amount"). In other words, the amount of the change of the transistor propagation delays and/or speed of the ring oscillator, and the amount of the change of the transistor propagation delays and/or speed of the CPU, must ***exactly match***. There is no such requirement in the specification or the prosecution history. Despain at ¶¶ 70-71.

In addition, there are at least two reasons why one of ordinary skill in the art would not find such a limitation reasonable or even feasible. First, the variations in voltage, temperature, and process parameters would not be 100% identical across a substrate, as micro-variations would likely occur, and hence changes in transistor propagation delays would not exactly match across the chip. Despain ¶ 71. Second, for the output of the CPU to remain valid, it is not necessary that the speed of the ring oscillator and the processing frequency capability of the CPU remain identical, but rather just that the speed of the ring oscillator not ***exceed*** the processing frequency capability of the CPU. Thus, it is perfectly acceptable that if the processing frequency capability of the CPU slows down due to an increase in operating temperature, the speed of the ring oscillator slows down even more, as this will not lead to errors. *Id*. at ¶ 72. Thus, there is no technical reason that a 1-to-1 correspondence must be met to practice the '336 inventions, and a person of ordinary skill would not expect this to occur. *Id*. at ¶ 73.

15. "second clock"

This term (claims 1-5) should be construed to mean "a clock not derived from the first clock," where the term "first clock" is used as a convenience to refer to the output signal of the "ring oscillator variable speed system clock" in claims 1-2 or the "ring oscillator system clock" in claims 3-5. Defendants propose simply "another clock," which could include clock signals derived from the first clock.

Plaintiffs' construction, which excludes signals derived from the first clock, is consistent with the intrinsic and extrinsic evidence. Claims 1 and 3 each state that the second clock is "independent of" the circuit that generates the first clock. While the meaning of "independent of" is discussed further below, it is clear that a second clock that is derived from the first clock, such as a delayed or buffered version of the first clock, would not be independent of the first clock as the claims require. Despain ¶ 80. Defendants' construction would not exclude such clocks.

The specification also supports Plaintiffs' construction. A microprocessor with a second clock signal is described at '336, 17:11-37 and shown in Fig. 17. The CPU 70 is clocked at a variable speed by the "adaptive ring counter clock 430." '336, 17:20-21. While the I/O interface 432 is clocked by "a conventional crystal clock 434." '336, 17:25-27. Here, the adaptive ring counter clock 430 provides a first clock signal while the crystal clock 434 provides a second clock signal. The crystal clock circuit 434 includes its own oscillator, and the clock signal produced by the crystal clock circuit 434 is derived from that oscillator, not from the ring oscillator that is the source of the first clock signal. Thus, in the only embodiment, the second clock signal is not derived from the first clock signal. Despain ¶ 77. The specification also states that the purpose of using two clocks is "decoupling the variable speed of the CPU 70 from the fixed speed of the I/O interface 432." '336, 17:32-33. Such decoupling can be achieved only if the second clock is not derived from the first clock. Despain ¶ 78.

The file history is also consistent. Applicants distinguished claims with limitations related to the "second clock" from a prior art patent that "provides no indication that bus interface 10 is clocked by ***a signal from a clock different from*** that used to clock the host microprocessor." Amd. 4/11/96 at 9, Ex. 4. In other words, Applicants meant the "second clock" to refer to a signal from a different circuit than the system clock; such a signal would not be derived from the system clock. Despain ¶ 79. For these reasons, the Court should construe "second clock" to mean "a clock not derived from the first clock."

16. "external clock"

This term (claims 6-10) should be construed to mean "a clock not derived from the first

clock, and which is not originated on the same semiconductor substrate upon which the entire oscillator (claims 6-9) or the entire variable speed clock (claim 10) is located." Similarly to "second clock," the term "first clock" is used here to mean the output of the "oscillator" in claims 6-9 or the "variable speed clock" in claim 10. Defendants propose "a clock not on the integrated circuit substrate" or no construction at all.

Plaintiffs' construction is consistent with the intrinsic and extrinsic evidence. As with the "second clock" of claims 1 and 3, claims 6 and 10 state that the "external clock" (or the frequency thereof) is independent of the circuit that generates the first clock (or its frequency), and this language requires that the external clock not be derived from the first clock. Despain ¶ 85. Further, the support in the specification for an "external clock" is the same as the support for "second clock" discussed above. Thus, like "second clock," "external clock" should be understood as referring to a clock that is not derived from the first clock.

"External clock" differs from "second clock" by the addition of the qualifier "external." It is apparent from the claims themselves that at some point, the external clock signal must be brought onto the integrated circuit substrate so that it can be used to clock the I/O interface as claims 6 and 10 require. *Id*. at ¶ 91. Thus, it is helpful to articulate, as Plaintiffs' construction does, that what is "external" to the integrated circuit substrate is the ***origin*** of the external clock signal. Defendants' proposed construction, which simply states that the external clock is "not on the integrated circuit substrate," is inconsistent with bringing the clock signal onto the substrate as the claims require.

17. "second clock independent of said ring oscillator … system clock" and "second clock independent of the ring oscillator system clock"

These phrases (claims 1-5) should be construed to mean "a change in the frequency of the ring oscillator does not affect the frequency of the second clock," as addressed in the next section.

18. "external clock is operative at a frequency independent of a clock frequency of said oscillator" and "independent of said oscillator"

These phrases (claims 6-10) should be construed to mean "a change in the frequency of the oscillator (claims 6-9) or the variable speed clock (claim 10) does not affect the frequency of

the external clock."

Claims 1, 3, 6 and 10 each include a phrase that describes one clock (or clock frequency) as being "independent of" another clock (or clock frequency). Specifically, in claims 1 and 3, the "second clock" that clocks the input/output ("I/O") interface is said to be "independent of" the "ring oscillator variable speed system clock" (claim 1) or "ring oscillator system clock" (claim 3). In claim 6, the "external clock" is said to be "independent of" the "oscillator." In claim 10, the operative frequency of the "external clock" is said to be "independent of" the "clock frequency of said variable speed clock."[16] Each of these phrases can be understood as stating that an "I/O Clock" that clocks the I/O interface is "independent of" a "CPU Clock" that clocks the CPU (claims 1-2 and 6-10) or microprocessor (claims 3-5).

The phrase "[the I/O Clock] independent of [the CPU Clock]" in each claim should be construed to mean that "a change in the frequency of [the CPU Clock] does not affect the frequency of [the I/O Clock]." Defendants would construe this to mean that "a change in the frequency of either [the I/O Clock] or [the CPU Clock] does not affect the frequency of the other." Thus, the only issue is whether the phrase "independent of" refers to "one-way" independence, as Plaintiffs' propose, or "mutual" independence.

Plaintiffs' construction conforms to the specification. An embodiment with two independent clocks is shown in Fig. 17 and described at col. 17, lines 11-37, of the '336 patent. The rationale for two clocks is described as "decoupling the ***variable*** speed of the CPU 70 from the ***fixed*** speed of the I/O interface 432" so that "optimum performance can be achieved by each." '336, 17:32-33 (emphasis added). Thus, what is described is one-way independence: the frequency of the CPU Clock can change without affecting the (fixed) frequency of the I/O Clock, as Plaintiffs' proposed construction states.

One-way independence is also consistent with the general usage of "independent of,"

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[16] As printed, claim 10 actually reads "clock frequency of said oscillator." This is due to an inadvertent error when claims were amended during prosecution. A petition for Certificate of Correction is pending in the U.S. Patent and Trademark Office.

which is often used to describe one-way independence. The dictionary defines independent as "not dependent: as **a** (1): not subject to control by others" or "**b** (1) not requiring or relying on something else." Webster's Ninth New Collegiate Dictionary 612 (1988), Ex. 23. For example, the temperature outdoors is independent of an outdoor thermometer since the outdoor temperature is not subject to control by the thermometer, even though the thermometer reading is dependent on the outside temperature. To unambiguously convey mutual independence, it is preferred to say that two things are "independent of each other." Applicants opted for the one-way formulation.

There is no basis for requiring two-way independence, as Defendants' propose. In the disclosed embodiment, the frequency of the I/O clock is said to be "fixed" ('336, 17:33), and there is no discussion as to whether varying the frequency of the I/O clock would affect the CPU clock. This indicates the important feature is the one-way independence that Plaintiffs' construction captures, not mutual independence as Defendants would require.

19. "fixed frequency"

Plaintiffs do not believe that this term (claims 2, 4, 8) needs to be construed by the Court. If the Court decides otherwise, this term should be construed to mean "a non-variable frequency." Defendants would construe this phrase as "having a speed (frequency) that varies minimally and is tightly controlled." Defendants' proposed construction would require that the frequency ***vary minimally*** and be ***tightly controlled***.

Defendants derive these requirements from an amendment made during prosecution of the '336 patent in response to an office action rejection of the pending claims over U.S. Patent No. 4,503,500 (the "Magar Patent"), the patentees stated:

> Crystals are by design fixed-frequency devices whose oscillation speed is designed to be ***tightly controlled and to vary minimally*** due to variations in manufacturing, operating voltage and temperature.

Ex. 8. Note with regard to this statement that the defendants are not defining the term "fixed frequency," but rather are describing a characteristic of crystals. Thus, the patentees state that crystals are fixed-frequency devices, and that the oscillation speed of crystals is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage

and temperature. This does not mean that the oscillation speed of all fixed frequency devices is designed to be tightly controlled and to vary minimally, or *vice versa*.

Also, Defendants' use of this phrase is highly misleading. In this statement, the patentees were merely commenting on a characteristic of crystals. In the amendment the applicants provided further explanation of crystals:

> All these systems operate at a frequency determined by the external crystal. The single, fixed, oscillation frequency of the crystal is determined by how the device is manufactured, i.e., how the crystal is cut and trimmed, and other factors. Crystals are used precisely for this purpose; they oscillate at a given frequency within a tolerance determined by their manufacture.

Ex. 8 at 4. Thus, when the patentees stated that the oscillation speed of crystals is designed to be "tightly controlled," all they were saying was that crystals oscillate at a given frequency within a tolerance determined by their manufacture, which in turn depends upon how they are cut and trimmed (among other factors). Similarly, when they said that the oscillation speed of crystals is designed to "vary minimally due to variations in manufacturing, operating voltage and temperature," they were saying that crystals vary due to something other than these things, namely how they are cut and trimmed. In other words, the patentees were simply describing some fundamental differences between crystals and variable frequency clocks – they were not defining the term "fixed frequency." To use the patentees' statements to assign a definition to the term "fixed frequency" would be taking those statement completely out of context in a manner never intended by the patentees.

IV. THE '148 PATENT

A. Background of the Technology of the '148 Patent

The '148 Patent generally relates to a microprocessor that includes both a processing unit and memory on the same substrate. In the '148, the memory occupies a majority of the active area of the substrate. There are many different types of memory, such as dynamic random access memory ("DRAM"), registers, cache, and latches. All of these different types of memory are contemplated by the '148. The '148 also teaches using the microprocessor in a multiprocessor environment. The microprocessors communicate with each other over interface ports that the '148 describes as a serial input/output interface. While these ports can be used for

communicating with other microprocessors, they can also be used for communication with other devices that are external to the microprocessor. Also, the '148, like the '336, teaches using a ring-oscillator to provide a system clock that is on the same chip as the microprocessor.

B. Claim Construction Analysis of the '148 Patent

1. "processing unit"

The phrase "processing unit" (claims 4, 7, 8, 10) should be construed as "an electronic circuit that controls the interpretation and execution of programmed instructions." Defendants do not propose a construction for this phrase. One of ordinary skill in the art would understand "processing unit" to have the same meaning as the phrase "central processing unit." Despain ¶ 94. Therefore, plaintiffs' proposed construction of "processing unit" should be adopted for the same reasons as "central processing unit" in the discussion of the '336.

2. "memory"

The term is addressed in section 3.

3. "a memory"

"Memory" and "a memory" (claims 4, 7, 8, 10) should be construed as "all of the storage elements on the substrate and the control circuitry configured to access the storage elements." This construction is consistent with the teachings of the '148 as well as the understanding of a person of ordinary skill in the art. Defendants would construe "memory" and "a memory" as "an information storing array that does not include registers, cache or column latches," thereby excluding circuitry that one of ordinary skill in the art would consider to fall within the meaning of "memory." Since the patentee did nothing to narrow the scope of "memory," or otherwise alter its meaning, plaintiffs' proposed construction should be adopted.

The '148 specification describes an embodiment in which a CPU is integrated directly onto a memory chip. '148, 6:49-11:16 [17] In this embodiment, the memory is described as being DRAM. *Id*. at 6:51-53. Furthermore, the specification states that the DRAM can be an

[17] The '148 patent is attached as Exhibit 2.

"intelligent DRAM" that is "optimized for high-speed operation with the integrated circuit 312 by having ***three on-chip address registers: Program Counter, X Register and Y Register.***" *Id.* at 8:48-61 (emphasis added). The specification also states that:

> Integrating the DRAM 311 allows architectural changes in the microprocessor 310 logic to take advantage of existing on-chip DRAM 311 circuitry. Row and column design is inherent in memory architecture. The DRAMs 311 access random bits in a memory array by first selecting a row of 1024 bits, storing them into a ***column latch***, and then selecting one of the bits as the data to be read or written.

Id. at 8:65-9:4 (emphasis added). Additionally, the specification states that "[s]ince the DRAM 311 maintains a ***1024-bit latch for the column bits***, the microprocessor 310 treats the ***column latch*** as a ***cache for 128 8-bit instructions***." *Id.* at 9:16-18 (emphasis added). Thus, the '148 specification makes clear that the registers and column latches within the DRAM are included within the scope of the term "memory." Also, the specification states that the column latches within the DRAM are used as cache by the microprocessor, making clear that cache is part of memory, and that registers, column latches and cache are all included within "memory." This use of the term "memory" is consistent with the understanding of a person of ordinary skill in the art. Despain ¶¶ 95-100. Therefore, defendants' proposed construction, which excludes registers, cache and column latches, is inconsistent with the teachings of the '148 patent specification.

4. "total area of said single substrate"

This and the terms of §§ 5 -7 are addressed in § 7.

This term (claims 4, 7) should be construed to mean "the total surface of the supporting material upon or within which is formed an interconnected array of circuit elements."

5. "total area of said substrate"

This term (claims 8, 10) should be construed to mean "the total surface of the supporting material upon or within which is formed an interconnected array of circuit elements."

6. "area of said single substrate"

This term (claims 4, 7) should be construed to mean "the surface of the supporting material upon or within which is formed an interconnected array of circuit elements."

7. "area of said integrated circuit substrate"

This term (claims 4, 7) should be construed to mean "the surface of the supporting material upon or within which is formed an interconnected array of circuit elements."

Plaintiffs' proposed constructions of the terms of §§ 4-7 are supported by the specification and are consistent with the understanding of a person of ordinary skill in the art. Defendants would construe these terms as the "area enclosed by the outermost edges of the substrate," enlarging the area used to determine whether or not the "memory" occupies a majority of the area of the substrates.

As explained with regard to "memory" and "a memory," the '148 specification discloses an embodiment in which a CPU is integrated directly onto a memory chip. '148, 6:49-11:16. This is illustrated in '148 Figure 9, which shows blocks of "32K Bytes" memory 311, along with "DMA CPU" 314 and processor 316 (which includes "Instruction Decode" logic, "ALU" and "Clock/Timing" circuitry). *Id*. at Fig. 9. The memory in Fig. 9 clearly occupies a majority of the total area of the substrate under plaintiffs' constructions because they properly define the substrate area as being the area where there is active circuitry.

A semiconductor substrate has six sides, like a cube. Despain ¶ 102. A person of ordinary skill would understand that "surface" refers to the surface of the substrate where there is active circuitry. *Id*. at ¶¶ 102-104. So understood, the memory in the microprocessor depicted in Figure 9 occupies a majority of the area of the substrate because only the portion of the substrate having active circuitry is counted. If the other portions of the substrate which do not contain active circuitry -- for example, the bottom surface of the substrate -- were counted, Figure 9 would not depict a memory occupying a majority of the area of the substrate. In fact, if portions of the substrate not containing active circuitry were included within the substrate area, the only way to practice the '148 patent claims would be to include memory on the bottom and/or sides of the substrate. Clearly such a construction was not contemplated by the patentee.

Defendants' proposed construction includes within the substrate area portions of the substrate that do not have active circuitry, thereby potentially covering the bottoms and sides of substrates. Clearly, this is not what the patentee meant.

8. "integrated circuit substrate"

Plaintiffs do not believe that the term "integrated circuit substrate" (claims 4, 7, 8, 10) needs to be construed by the Court. If the Court decides otherwise, this term should mean "the supporting material upon or within which is formed an interconnected array of circuit elements." This construction is consistent with the patent specification and the understanding of a person of ordinary skill in the art. Despain ¶¶ 105-107.

9. "variable"

This term (claims 4, 7, 8, 10) should be construed to mean "capable of changing." "Variable" is a non-technical term that should be construed in accordance with its dictionary definition. Plaintiffs' proposed construction is from a standard English dictionary that was published around the same time as the filing date of the '148 patent. *Webster's*, *supra*, at 1304, Ex. 23. Defendants, on the other hand, propose that this term be construed as "not tightly controlled and varying more than minimally." Defendants' construction improperly limits the claim to the preferred embodiment of the patent, and should be rejected.

10. "system clock"

This term (claims 4, 7, 8, 10) should be construed as "a circuit that generates the signal(s) used for timing the operation of the CPU" -- the same as in the '336. As a general rule, when the same term is used in different patents in the same family, that term is given the same meaning absent specific reason to do otherwise. *NTP, Inc. v. Research In Motion, Ltd.*, 418 F.3d 1282, 1293 (Fed. Cir. 2005) ("Because NTP's patents all derive from the same parent application and share many common terms, we must interpret the claims consistently across all asserted patents. . . . [w]e thus draw distinctions between the various patents only where necessary."). As shown on their cover pages, the '148 and '336 are divisionals of a common parent application and therefore have substantially identical specifications. Since their file histories contain nothing to suggest "system clock" mean different things in the '148 and '336 claims, the Court should construe "system clock" the same in each patent.

11. "ring oscillator"

This term (claims 4, 7, 8, 10) should be construed to mean "an oscillator having a

multiple, odd number of inversions arranged in a loop," which is the same construction proposed by Plaintiffs in the '336 patent, for the same legal principle and reasoning discussed in the immediately preceding section 10.

12. "a ring oscillator having a variable output frequency"

"A ring oscillator having a variable output frequency" (claims 4, 7, 8, 10) should be construed as "a circuit having a multiple, odd number of inversions arranged in a loop that generates an output having a frequency that can change." This construction essentially combines Plaintiffs' proposed constructions for the phrases "ring oscillator" and "variable speed," both of which appear in the '336. For all of the reasons provided with regard to those phrases in the '336, plaintiffs' proposed construction for this phrase should be adopted.

13. "the ring oscillator disposed on said integrated circuit substrate" and "the ring oscillator disposed on said substrate"

Plaintiffs do not believe that "the ring oscillator disposed on said integrated circuit substrate" (claims 4, 7) or "the ring oscillator disposed on said substrate" (claims 8, 10) need to be construed by the Court. If the Court decides otherwise, these terms should mean "a circuit having a multiple, odd number of inversions arranged in a loop, where the circuit is located on the integrated circuit substrate (claims 4, 7) or the single substrate (claims 8, 10)." This essentially combines the proposed constructions for "ring oscillator" and "integrated circuit substrate" or "substrate." For the reasons provided with regard to those phrases, this proposed construction should be adopted.

14. "interface ports for interprocessor communication"

Plaintiffs do not believe that the phrase "interface ports for interprocessor communication" (claims 8, 10) needs to be construed by the Court. If the Court decides otherwise, this phrase should mean "channels through which data can be transferred between two separate processing units." Defendants would construe this term to mean "channels though which data is transferred between two separate processing units." Thus, the only meaningful distinction between the parties' proposed constructions is that defendants' proposed construction requires that the interface ports ***must*** be used for interprocessor communication, whereas

plaintiffs' proposed construction requires only that the interface ports be ***capable of*** being used for interprocessor communication. One of ordinary skill would understand that the interface ports described and claimed in the '148 specification are versatile and can be used for various input/output functions, one of which can be interprocessor communication. Despain ¶¶ 108-110. Therefore, one of ordinary skill would understand that while the interface port could be used for interprocessor communication, it does not have to be used that way. *Id.*

The '148 patent specification discloses an embodiment in which shift registers configured for video output can also be configured as interprocessor communication links. '148, 9:59-61. These interprocessor communication links take advantage of the column latch architecture described in the '148 patent. *Id*. at 9:61-64. The interprocessor communication links use serial input/output over the following six lines: DATA IN, CLOCK IN, READY FOR DATA, DATA OUT, DATA READY? AND CLOCK OUT. *Id*. at 9:64-10:7. At startup, a special start up sequence is used to initialize the DRAM in each of the processors. *Id*. at 10:8-9. This architecture allows a microprocessor to deliver information directly to the internal registers or cache of neighboring microprocessors. *Id*. at 10:10-12. These six lines, however, do not have to be used for interprocessor communication – rather, they can be used for other functions such as video output, depending upon the start up sequence run to initialize the chip. *Id*. at 9:59-6:9. Thus, the patent makes clear that the disclosed interface ports (i.e. the six lines listed above) are configurable, and can be used for purposes other that interprocessor communication (such as video output). Indeed, Dr. Despain explains in his declaration that the flexibility and versatility of the disclosed microprocessor, including the interface ports, is one of key aspects that make the invention claimed in the '148 patent valuable. Despain ¶ 110. Plaintiffs' proposed construction should be adopted.

V. THE '584 PATENT

A. Background of the Technology of the '584 Patent

The '584 patent discloses a number of improvements in the fetching and decoding of instructions. Despain ¶¶ 36-39. These improvements, used separately or together, can reduce the size of instructions and thereby increase the average number of instructions that can be

fetched in parallel. A fixed-size group of instructions (i.e., an "instruction group") is fetched into an instruction register. '584 19:17-21, 5:24-27.[18] The instructions are allowed to vary in size, so that different groups might contain different numbers of instructions. '584, 20:41-42, 22:42-43. For at least some of the instructions, the microprocessor uses the position of the instruction within its instruction group to determine some aspect of how the instruction is processed. The '584 patent provides numerous examples of instructions having this property. '584, 14:4-39, 41-64, 20:41-22:39, 23:3-25:19, 26:66-27:14, 28:62-29:24; Amd. 2/05/98 at 7-9, Ex. 17. In one example, the target of a BRANCH instruction is ***always the first instruction*** in one of the instruction groups. '584, 20:35-36, 21:43-45; Ex. 17 at 8 Other examples include a SKIP instruction that causes execution to skip ahead to ***the first instruction in the next group*** ('584, 14:4-39); an IMMEDIATE instruction that causes all bits ***from the end of the instruction opcode[19] to the end of the current group*** to be loaded onto the processor's parameter stack ('584, 16:7-26); and a LOAD-SHORT-LITERAL instruction that causes the ***last eight bits of the current group*** to be loaded onto the processor's parameter stack ('584, 29:21-24).

B. Claim Construction Analysis of the '584 Patent

Plaintiffs assert that Defendants infringe claim 29 of the '584. The parties seek the Court's construction for nine terms and phrases used in claim 29. In accordance with *Phillips*, these terms and phrases must be construed as they would have been understood by a person having ordinary skill in the art of microprocessor design as of 1989, the effective filing date of the application for the '584 patent. *See Phillips*, 415 F.3d at 1303. As discussed below, Plaintiffs' proposed construction of each of these nine terms is supported by the intrinsic evidence, including the specification and claims, as well as by extrinsic evidence including expert opinion and pertinent technical treatises. Consequently, the Court should adopt Plaintiffs' proposed constructions.

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[18] The '584 patent is attached as Exhibit 3.

[19] An "opcode" is the portion of each instruction that specifies the operation to be performed.

1. "microprocessor"

The construction given to this term in the '336 should be applied to the '584 because, when the same term is used in different patents in the same family, that term is given the same meaning absent specific reason to do otherwise. *NTP*, 418 F.3d at 1293 ("Because NTP's patents all derive from the same parent application and share many common terms, we must interpret the claims consistently across all asserted patents. . . . [w]e thus draw distinctions between the various patents only where necessary."). The '584 and '336 are divisionals of a common parent application and have substantially identical specifications. The file history contains nothing that would suggest "microprocessor" was intended to mean something different in the '584 and '336 patents.

2. "central processing unit"

The construction given to this term in the '336 patent should be applied to the '584 patent, for the same reasons discussed in §1 above.

3. "instruction register"

This term should be construed to mean "the register that temporarily stores the instruction group whose instructions are currently being decoded by the control unit of the computer." The construction of "instruction groups" is discussed in §4 below.

Plaintiffs' construction is consistent with the intrinsic and extrinsic evidence. For example, one embodiment of the '584 patent includes an instruction register 108 that receives four instruction bytes. '584, 5:63-65, Fig. 4. A multiplexer 170 delivers bytes from the instruction register 108 to decoder 184. '584, 5:65-6:4. Elsewhere, the '584 patent states that the instruction register "[h]olds 4-byte instruction groups ***while they are being decoded and executed***." '584, 19:56-59 (Table) (emphasis added). Plaintiffs' definition is consistent with this description of the role of the instruction register.

Plaintiffs' construction is also consistent with the extrinsic evidence. A 1987 textbook, *From Chips to Systems*, describes a "standard microprocessor" as including an instruction register ("IR") that is "a special register of the control unit." Rodnay Zaks & Alexander Wolfe, *From Chips to Systems* 65 (1987), Ex. 24. The text states that "[o]nce in the IR, [an instruction]

is ***decoded*** by a decoder." *Id.* (emphasis in original). Consistent with the '584 specification, this textbook illustrates how the term "instruction register" is used in the art to identify where an instruction is held during decoding.

Plaintiffs' construction also incorporates the important feature of the '584 patent that the instruction register holds an "instruction group" rather than the traditional single instruction. This construction is based on the language of claim 29 itself, which recites "providing ***instruction groups*** to said instruction register," implying that the IR receives and holds a group, rather than a single instruction as is conventional.

4. "instruction groups"

This term should be construed to mean "sets of from 1 to a maximum number of sequential instructions, each set being provided to the instruction register as a unit and having a boundary." Defendants would also require that "any operand that is present must be right justified" and that an instruction group "cannot encompass a single 32-bit RISC instruction." These arbitrary requirements have no basis in the intrinsic or extrinsic evidence.

Plaintiffs' construction is consistent with the intrinsic and extrinsic evidence. The '584 specification describes a microprocessor that "fetches instructions in 4-byte instruction groups" and states that "[a]n instruction group may contain from one to four instructions." '584, 19:17-18. The parties agree that an instruction group may include one or more sequential instructions.

The parties also agree that the fixed boundaries of the instruction groups are important, although they articulate the point differently. Plaintiffs refer to "having a boundary," while Defendants state that "execution of the instructions depends on each set being provided to the instruction register as a unit." Defendants' formulation, which implies that the boundaries of ***every*** group matter, is too strong. The '584 patent does disclose ***some*** instructions that rely on the fixed group boundaries for execution. For instance, BRANCH or CALL instructions redirect execution to targets that are always located at 32-bit word boundaries ('584, 21:43-44), which "correspond to instruction group boundaries." Ex. 17 at 7. Other instructions, however, ***do not*** rely on group boundaries at all. For example, execution of logic and math instructions ('584, 29:25-30:19) is not affected by group boundaries. Simply requiring that each group has a

boundary, rather than requiring that the boundary ***always*** be relied on, is consistent with the scope of the invention.

Defendants also propose to add two further limitations that would arbitrarily narrow the claim. While "right justified" operands are a feature of the preferred embodiment, a person skilled in the art would recognize that they are not necessary, and other techniques could be used. Despain ¶ 116. The exclusion of "a single 32-bit RISC instruction" is even more problematic. The '584 patent specifically includes some 32-bit instructions. '584, 20:41-42. Using the qualifier "RISC" to identify the excluded instructions only creates confusion because, as Dr. Despain notes, "it is not possible for one skilled in the art to determine with certainty whether a single instruction is or is not a 'RISC instruction.'" Despain ¶ 118. Adding to the confusion, the '584 patent describes a preferred embodiment as "a simplified reduced-instruction set computer (RISC) microprocessor" ('584, 1:12-13), a "RISC-influenced 32-bit CPU" (*id.* at 7:13-14), and "like any RISC type architecture" (*id*. at 25:66). Thus, there is simply no basis for distinguishing "RISC instructions" from the instructions of the '584 patent.

5. "operand"

This should be construed to mean "an input to an operation specified by an instruction that is encoded as part of the instruction." Defendants' additional restriction to operands of variable width inappropriately narrows the scope of the claim. Plaintiffs' construction is consistent with the intrinsic and extrinsic evidence. During prosecution of the '584, the applicants explained that "in general, operands can be of many types," but "[i]n the instant case, the only type of operands referred to are 'immediate operands,' that is, operands that are encoded as part of the instruction." Amd. 11/21/97 at 8, Ex. 16. Thus, an "operand" is "an input to an operation that is encoded as part of the instruction."

Further narrowing the term to include only variable-width operands, as Defendants propose, is improper because a construction that excludes a preferred embodiment "is rarely, if ever, correct and would require highly persuasive evidentiary support." *Vitronics*, 90 F.3d at 1583. Defendants may argue that during prosecution, Applicants made reference to variable-width operands. Amd. 4/08/96 at 11, Ex. 13; Amd. 6/12/97 at 12, Ex. 14. However, the final

paper Applicants filed during prosecution included a list of "examples in the specification that support the claims as amended." Ex. 17 at 6-8. This paper prompted the Examiner to allow the claims. Notice of Allowability 2/13/1998, Ex. 18. The examples included at least two instructions that use fixed-length operands: LOAD-SHORT-LITERAL and FETCH-VIA-PC. Ex. 17 at 7-8. In the case of LOAD-SHORT-LITERAL, the immediate operand is ***always 8 bits*** ('584, 29:62-65; Despain ¶ 125); for FETCH-VIA-PC, the immediate operand is ***always 32 bits.*** ('584, 26:66-27:7; Despain ¶ 124. These examples show that the allowed claims cover instructions that cause access to fixed-length immediate operands.

6. "said instruction groups include at least one instruction that, when executed, causes an access to an operand or instruction or both"

This phrase should be construed to mean "the instruction being executed causes the CPU to use an immediate operand or execute a second instruction which is not the next sequential instruction." The phrase "at least one instruction" means that this limitation is applicable to one or more, though not necessarily all, instructions executed by the processor. Despain ¶ 127.

Defendants would equate "an access to an operand" with using data. But this is inconsistent with the construction of "operand" discussed in §5 above, since processors also use many types of data other than immediate operands. Limiting the phrase to immediate operands is consistent with the applicants' statement that [i]n the instant case, the only type of operands referred to are 'immediate operands,' that is, operands that are encoded as part of the instruction." Ex. 16 at 8.

Defendants would omit the phrase "other than the next sequential instruction." But excluding the next sequential instruction is proper, given the way microprocessors operate. Programs normally flow from one instruction to the next sequential instruction, and those skilled in the art do not regard this normal program flow as "causing an access to an instruction." Despain ¶¶ 131-136.

7. "said operand or instruction being located at a predetermined position from a boundary of said instruction groups"

This phrase should be construed to mean "the immediate operand or the instruction that is accessed has a position, relative to the beginning or end of the instruction group that includes the

operand or instruction being accessed, that is determined based on a portion of an accessing instruction that identifies an operation to be performed and without reference to operand or address bits in the accessing instruction." As discussed here and in §§ 8 and 9 below, only this construction is consistent with the intrinsic and extrinsic evidence.

This construction precisely defines "a predetermined position from a boundary of said instruction groups." The specification does not use the phrase "predetermined position from a boundary" in describing instruction execution. Instead, this language was developed in the course of protracted negotiations between the patent examiner and the applicants. S*ee generally* Amd. 4/08/96; Amd. 6/12/97; Amd. 11/21/97; Amd. 2/05/98, Exs. 13-14, 16-17. When the applicants introduced the "predetermined position" language, they also provided a list of "examples in the specification that support the claims as amended." Ex.17 at 6-7. This list included seven instructions: SKIP, MICROLOOP, IMMEDIATE, BRANCH and CALL, FETCH-VIA-PC, and LOAD-SHORT-LITERAL. *Id*. at 7-8. For each instruction, the applicants identified the specific boundary relative to which the predetermined position of the accessed operand or instruction (also referred to herein as "the target") is located. *Id.*

These examples show that the applicants consistently used "a predetermined position from a boundary of said instruction groups" to refer to the beginning or end of the instruction group that contains the operand or instruction being accessed (also referred to herein as "the target group"). This group can be, but is not necessarily, the instruction group that contains the instruction that causes the access. For example, in the case of SKIP, the applicants state that "[t]he result of resetting the counter is to begin executing at the beginning boundary of the ***next*** instruction group" (Ex. 17 at 7 (emphasis added)), not the current instruction group. In the case of BRANCH and CALL, the applicants note that these instructions "also reference instructions that are located at a predetermined position from a boundary of an instruction group," specifically the 32-bit word boundary ***to which the branch or call is made***. Ex. 17 at 7; Despain ¶¶ 143-144 . In the case of FETCH-VIA-PC, the applicants stated that "the operand, the 32-bit memory content fetched, is located at a predetermined position from a boundary of an instruction group, that is, the ***next*** instruction group." Ex. 17 at 7-8 (emphasis added). Clearly, the

applicants intended "a predetermined position from a boundary of said instruction groups" to refer to the instruction group that contains the operand or instruction that is accessed.

These examples also further clarify the applicants' statement that "[o]ne of the unique characteristics of the claimed processor and processing method is the locating of operands or instructions by their position within the current group of instructions." Ex. 17 at 6. As the foregoing discussion demonstrates, the applicants' phrase "current group of instructions" in this statement logically refers to the instruction group that contains the accessed operand or instruction. This group is loaded into the instruction register, and thus becomes "current," as part of the access operation. In a case where the accessing instruction and the target are in the same group (e.g., MICROLOOP), the accessing group and the instruction group that contains the accessing instruction happen to be the same group. But in cases where the two instructions are in different groups (*e.g.,* SKIP and BRANCH), the "predetermined position from a boundary of said instruction groups" can only refer to the instruction group that contains the operand or instruction that is accessed. *See also* Despain ¶ 146.

Plaintiffs' construction also correctly identifies the significance of the word "predetermined" by describing the position relative to the boundary as being "determined based on a portion of an accessing instruction that identifies an operation to be performed and without reference to operand or address bits in the accessing instruction." This interpretation is consistent with the instructions cited by Applicants as supporting the claims. Ex. 17 at 6-8. In each case, the position is described as "always" being at a particular place for instructions of that type. For instance, the SKIP and MICROLOOP instructions automatically reset the microinstruction counter to zero, so that execution of the target group (the next group in the case of SKIP or the current group in the case of MICROLOOP) ***always*** begins at the beginning boundary of the group. Ex.17 at 7; '584, 14:24-27, 14:54-57; Despain ¶ 151. Similarly, branches and calls are ***always*** "made to 32-bit word boundaries," *i.e.*, to the beginning boundary of the target group. Ex. 17 at 7; '584, 20:35-36, 21:43-45; Despain ¶¶ 143, 152. The target address specified by the instruction has no effect on the decision to begin execution at the beginning boundary of the target group.

8. "decoding said at least one instruction to determine said predetermined position"

This phrase should be construed to mean "interpreting an instruction, in particular the portion thereof that signifies the operation to be performed, in order to identify a position relative to the beginning or end of the instruction group that includes the operand or instruction being accessed, without reference to operand or address bits in the instruction being interpreted." Defendants' proposal differs only in that the position is identified "relative to the beginning or end of the current instruction group." Thus, the dispute between the parties again relates to the construction of "predetermined position."

As discussed in §7 above, the "predetermined position" is properly understood as being a position "relative to the beginning or end of the instruction group that includes the operand or instruction being accessed." In cases where the accessed operand or instruction and the accessing instruction are in different groups, e.g., MICROLOOP, BRANCH, or FETCH-VIA-PC, the "current group" at the time of decoding would be the group that contains the accessing instruction. But this is not the group relative to which the "predetermined position" is defined. *See* §7, *supra*.

Further, as in §7 above, the "predetermined position" is "predetermined" in the sense that it is "determined based on a portion of an accessing instruction that identifies an operation to be performed." It follows that "decoding said at least one instruction to determine said predetermined position" refers to interpreting the portion of the instruction that identifies the operation to be performed, for determining where the target (i.e., the operand or instruction to be accessed) is located within the instruction group that contains the target.

9. "locating said predetermined position"

This phrase should be construed to mean "establishing operand or instruction supply within the instruction group that includes the operand or instruction being accessed at the predetermined position." Defendants' proposal refers to ascertaining the address of the accessed operand or instruction "by referencing the current group address" and "without adding or subtracting an operand with the current Program Counter," both of which are inaccurate.

In claim 29, the "locating …" step follows the "decoding …" step discussed in §8 above and precedes a step of "supplying … said operand or instruction or both to said central processing unit," which the parties have agreed means "using the result of the locating step in the step of transferring the bits forming the accessed operand or instruction to the CPU." Ex. B to Joint Claim Constr. Stmt. As in §7 above, the "predetermined position" refers to the position of the accessed operand or operand relative to the boundaries of the group that contains the accessed operand or instruction. Thus, "locating said predetermined position" refers to establishing the point of operand or instruction supply at this position so that the accessed operand or instruction can be supplied.

The parties again disagree as to which instruction group is the reference for the "predetermined position." The reasons for adopting Plaintiffs' construction, which specifies that the predetermined position is located relative to "the instruction group that includes the operand or instruction being accessed," as set forth in §7 above, apply here as well.

Defendants also propose that the predetermined position be located "without adding or subtracting an operand with the current Program Counter." This limitation is improper because it would exclude a disclosed embodiment. The '584 patent describes an embodiment with "four instructions to redirect execution" that can take operands of three different lengths. '584, 11:6-11. Regardless of operand length, the processor "treats the three operands similarly ***by adding or subtracting them to the current program counter***." *Id.* at 11:13-15 (emphasis added). Thus, adding or subtracting an operand with a program counter to locate a target instruction is clearly within the scope of the invention. While the '584 patent also discloses an embodiment that avoids adding or subtracting an operand with the program counter (*id.* at 20:41-53), there is no basis for inferring that the claims were intended to be limited only to the latter embodiment.

VI. CONCLUSION

For the reasons given, the Court should adopt Plaintiffs' proposed constructions.

DATED: March 19, 2007 Respectfully submitted,

By: /s/ Roger L. Cook

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CERTIFICATE OF SERVICE

I hereby certify that counsel of record who are deemed to have consented to electronic service are being served this 19th day of March, 2007, with a copy of this document via the Court's CM/ECF system per Local Rule CV-5(a)(3). Any other counsel of record will be served by electronic mail, facsimile transmission and/or first class mail on this same date.

/s/ Roger L. Cook
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