[See Signature Page for Information on Counsel for Plaintiffs]

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

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| ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC.,<br>Plaintiffs,<br>v.<br>TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED,<br>Defendants. | Case No. 3:08-cv-00877 JW<br>**PLAINTIFFS' CONSOLIDATED RESPONSIVE CLAIM CONSTRUCTION BRIEF**<br>**[RELATED CASES]**<br>**JURY TRIAL DEMANDED**<br>Date: January 27, 2012<br>Time: 9:00 a.m.<br>Place: Courtroom 9, 9th Floor<br>Judge: Hon. James Ware |
| HTC CORPORATION, HTC AMERICA, INC.,<br>Plaintiffs,<br>v.<br>TECHNOLOGY PROPERTIES LIMITED, PATRIOT SCIENTIFIC CORPORATION, and ALLIACENSE LIMITED,<br>Defendants. | Case No. 3:08-cv-00882 JW |
| BARCO N.V., a Belgian corporation,<br>Plaintiff,<br>v.<br>TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORP., ALLIACENSE LTD.,<br>Defendants. | Case No. 3:08-cv-05398 JW |

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## STATUTES

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| ’148 patent or ’148 | U.S. Patent No. 6,598,148, entitled “High Performance Microprocessor Having Variable Speed System Clock,” issued July 22, 2003 |
| ’336 patent or ’336 | U.S. Patent No. 5,809,336, entitled “High Performance Microprocessor Having Variable Speed System Clock,” issued September 15, 1998 |
| ’749 patent or ’749 | U.S. Patent No. 5,440,749, entitled “High Performance, Low Cost Microprocessor Architecture,” issued August 8, 1995 |
| ’890 patent or ’890 | U.S. Patent No. 5,530,890, entitled “High Performance, Low Cost Microprocessor,” issued June 25, 1996 |
| Plaintiffs | Declaratory judgment plaintiffs Acer, Inc., Acer America Corporation, Barco, N.V., Gateway, Inc., HTC Corporation and HTC America, Inc. |
| Defendants or TPL | Declaratory judgment defendants Technology Properties Limited, Patriot Scientific Corporation and Alliacense Limited |
| *HTC* action | *HTC Corporation, HTC America, Inc. v. Technology Properties Limited, Patriot Scientific Corporation, and Alliacense Limited*, Civil Case No. 5:08-cv-00882 JW |
| *Acer* action | *Acer, Inc., Acer America Corporation and Gateway, Inc. v. Technology Properties Limited, Patriot Scientific Corporation, and Alliacense Limited*, Civil Case No. 5:08-cv-00877 JW |
| Opening Br. | Defendants’ Opening Claim Construction Brief for the “Top Ten” Terms, filed December 23, 2012 (HTC action Dkt. No. 339) |
| Chen Decl. | Declaration of Kyle D. Chen in Support of Plaintiffs’ Consolidated Responsive Claim Construction Brief |
| Ward Order | Memorandum Opinion and Order by Judge T. John Ward, filed June 15, 2007 (Docket No. 259) in *Technology Properties Ltd., et al. v. Matsushita Electric Industrial Co., et al.*, Civil Action No. 2:05-CV-494 (TJW), in the U.S. District Court for the Eastern District of Texas, Marshall Division (“*TPL v. Matsushita*”). |
| Talbot | U.S. Patent No. 4,689,581, entitled “Integrated Circuit Phase Locked Loop Timing Apparatus,” issued August 25, 1987 to Gerald R. Talbot |
| Edwards | U.S. Patent No. 4,680,698, entitled “High Density ROM in Separate Isolation Well on Single with Chip,” issued July 14, 1987 to Jonathan Edwards, et al. |

Declaratory relief plaintiffs Acer, HTC and Barco entities as shown on the caption page (collectively "Plaintiffs") submit this joint brief in support of their claim construction positions.

## I. INTRODUCTION

The four patents-in-suit (the '336, '148, '749 and '890 patents) share the same specification and concern features of a commercially failed microprocessor called "Sh-Boom." Plaintiffs' proposed constructions are all based on the intrinsic record provided by the specification and prosecution history. The patent owner's own words, through the specification and file histories of those patents, provide a clear picture of the true, narrow scope of the claims. When the patents were challenged in reexamination, TPL was forced to characterize and amend their claims even more narrowly to avoid prior art. TPL cannot now avoid its disclaimers, disavowals and characterizations of the alleged invention by simply ignoring them or by trying to run away from its own specification and file histories.

Rather than address the intrinsic record, TPL focuses on hearsay rhetoric regarding its Sh-Boom microprocessor. However, even the article that TPL relies upon describes Sh-Boom as "a bizarre processor" that was "never a commercial success."[1] Contrary to TPL's rhetoric, the intrinsic record shows that the patents-in-suit do not cover all microprocessors, but rather, only the "bizarre" features of Sh-Boom that were not implemented by the Plaintiffs.

## II. DISPUTED TERMS

### A. CPU Clock-Related Terms from the '336, '148, '749 and '890 Patents

Five of the "top ten" disputed terms relate to mechanisms for timing or "clocking" a central processing unit ("CPU"): (1) "ring oscillator," (2) "providing an entire variable speed clock disposed upon said integrated circuit substrate," (3) "clocking said central processing unit," (4) "operates asynchronously to," and (5) "as a function of parameter variation." These closely-related terms will be discussed together in this brief. Although these terms appear most prevalently in the '336 and '148 patents, the term "ring oscillator" also appears in asserted claims of the '749 and '890 patents. Because the clock-related terms are related and potentially

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[1] http://spectrum.ieee.org/semiconductors/processors/25-microchips-that-shook-the-world/5

dispositive of claims in all four patents-in-suit, this brief will address them first.

#### *i. The "variable speed" clock of the patents-in-suit*

The CPU in a commercial microprocessor consists of millions of transistors that work together to interpret and execute instructions. To ensure that those millions of transistors work in harmony instead of chaos, a CPU typically relies on a series of timing signals known as "clock signals" to drive its operations. The clock signals, which are generated by a clocking device, are akin to "heartbeats" that drive blood through a human body. The clock signals control (and in fact equal) the speed at which the CPU operates.

To operate properly, a CPU's transistors must have enough time between clock signals to complete their operations before the next clock signal arrives. Accordingly, a CPU has a maximum speed that depends on how fast its transistors can operate. To ensure proper operation, the clocking device should never send clock signals "too fast" such that they exceed the CPU's maximum speed. *See* '336, 16:67-17:2 ("CPU **70** will always execute at the maximum frequency possible, but never too fast.").[2]

Because the transistors in the CPU depend on electrical signals to operate, their maximum speed for proper operation is constrained by how fast the electrical signals can transmit through them, known as "transistor propagation delays." According to the patents-in-suit, these delays depend on varying environmental conditions such as temperature, voltage and manufacturing process, which thus "determine" the CPU's maximum speed. '336, 16:47-50 and 59-60. For example, if the temperature in the environment rises, the CPU's maximum speed for proper operation decreases. '336, 16:59-67.

The patents-in-suit explain that, to avoid clocking the CPU at a rate faster than its maximum speed, prior art systems constrain the clock speed to a fixed rate slow enough to "operate properly in worse [sic] case conditions." '336, 16:48-53. The patents criticize this approach by claiming that this constraint results in a CPU that operates at less than half of its theoretical maximum

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[2] All citations to "xx:yy-zz" refer to columns and lines in the referenced patent. As noted in the text, the patents-in-suit share a common specification. For purposes of consistency, this brief will cite to columns and lines in the '336 patent (Chen Decl., Ex. 1) when discussing the five clock-related terms.

performance. ’336, 16:50-53.

The ’336 and ’148 patents are both entitled “High Performance Microprocessor Having Variable Speed System Clock” and disclose a ***variable speed clock*** comprised of transistors on the ***same integrated circuit*** as the CPU to provide higher performance when environmental conditions permit. By placing a variable speed clock on the same integrated circuit as the CPU, according to the patents-in-suit, the speed of the variable speed clock and the CPU’s maximum speed will “vary together” in the same way according to changing environmental conditions. The result of this allegedly improved approach is that “CPU **70** will always execute at the maximum frequency possible, but never too fast.” ’336, 16:67-17:2.

The only variable speed clock disclosed in the patents-in-suit is a clock generating circuit called a “ring oscillator” that is made of the same transistors on the same integrated circuit as those in the CPU itself. ’336, 16:54-57. According to the patents-in-suit, because the ring oscillator and the CPU are on the same integrated circuit, they are subject to the same environmental conditions (temperature, voltage and process), resulting in the CPU “always” being clocked at its “maximum frequency possible, but never too fast” under any environmental conditions. ’336, 16:54-17:10.

### ***ii. Construction of “ring oscillator” (’336, ’148, ’749, ’890)***

In the prior Texas action, Judge Ward construed “ring oscillator” as “an oscillator having a multiple, odd number of inversions arranged in a loop.” Chen Decl., Ex. 2 at 11. The parties’ dispute turns primarily on whether the construction should incorporate statements made by TPL in subsequent reexamination concerning the claimed “ring oscillator”:

| Plaintiffs’ Construction | TPL’s Construction |
|---|---|
| An oscillator having a multiple, odd number of inversions arranged in a loop, **wherein the oscillator is: (1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters in the environment.** | An oscillator having a multiple, odd number of inversions arranged in a loop |

Plaintiffs’ construction includes a “wherein” clause that incorporates explicit arguments and disavowals that TPL made during reexamination after Judge Ward’s claim construction order and after the dismissal of the Texas action. Specifically, in order to overcome a rejection of its claims based on U.S. Patent No. 4,689,581 to Talbot (Chen Decl., Ex. 3), TPL argued that the voltage-controlled oscillator ("VCO") of Talbot did not teach the "ring oscillator" of the patents-in-suit. The examiner summarized TPL's arguments, which were made in an in-person interview, as follows:

> Continuing, the patent owner further argued that the reference of Talbot does not teach of [sic] a "ring oscillator." The patent owner discussed features of a ring oscillator, such as being **non-controllable**, and being **variable based on the environment**. The **patent owner** argued that **these features distinguish over what Talbot teaches**.

Interview Summary, 2/12/08, Control No. 90/008,227 (emphasis added) (Chen Decl., Ex. 4).

In light of TPL's disavowing arguments made to the PTO after Judge Ward's ruling, the construction must be adapted to require that the claimed "ring oscillator" be (1) "non-controllable," and (2) "variable based on the environment."[3] Federal Circuit law is clear that "[a]rguments made during the prosecution of a patent application are given the same weight as claim amendments." *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 979 (Fed. Cir. 1999). It is also black letter law that a court "cannot construe the claims to cover subject matter broader than that which the patentee itself regarded as comprising its invention and represented to the PTO." *Microsoft Corp. v. Multi-Tech. Sys., Inc.*, 357 F.3d 1340, 1349 (Fed. Cir. 2004). "The purpose of consulting the prosecution history in construing a claim is to 'exclude any interpretation that was disclaimed during prosecution.'" *Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) (citation omitted). "Accordingly, 'where the patentee has unequivocally disavowed a certain meaning to obtain his patent, the doctrine of prosecution disclaimer attaches and narrows the ordinary meaning of the claim congruent with the scope of the surrender.'" *Id.* (citation omitted); *see also, e.g., Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319, 1325 (Fed. Cir. 2002) ("Explicit arguments made during prosecution to overcome prior art can lead to narrow claim interpretations because 'the public has a right to rely on such definitive statements made during prosecution.'")

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[3] Plaintiffs' construction requires that the oscillator be "(1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters in the environment." Part (2) of this construction is based on TPL's explanation of the term "environment" in its previous claim construction briefing. *See* Doc. No. 221 in *Acer* action (02/11/2011 TPL Claim Construction Brief), at 17:17-19 ("According to the '336 specification, 'the ring oscillator frequency is determined by the parameters of temperature, voltage and process.' This is the only 'environment' that is disclosed in the specification.") (citation omitted).

(citation omitted).

The examiner's interview summary is a proper basis for finding a disavowal of claim scope. It expressly reflects what TPL, the patent owner, argued. The Federal Circuit has repeatedly relied upon patent owners' arguments recorded in interview summaries to find that patent owners disavowed claim scope to distinguish prior art. *See, e.g.*, *Rheox, Inc. v. Entact, Inc.*, 276 F.3d 1319, 1322 (Fed. Cir. 2002) (disavowal found based on patent owner's arguments that the examiner recorded in interview summary); *see also Biovail Corp. Int'l v. Andrx Pharms., Inc.*, 239 F.3d 1297, 1302-04 (Fed. Cir. 2001) (same); *Trinity Indus. v. Road Sys.*, 121 F. Supp. 2d 1028, 1044 (E.D. Tex. 2000) ("It is proper to consider the interview summary in claim construction as it is part of the prosecution history.") (citing *Athletic Alternatives, Inc. v. Prince Mfg., Inc.*, 73 F.3d 1573, 1576 (Fed. Cir. 1996) (relying upon examiner's interview summary of patent owner's statements in claim construction)).

The examiner had no motive to misstate TPL's position, and TPL does not dispute the accuracy of any aspect of the examiner's summary of TPL's argument. In its opening brief, TPL cites its own self-serving amendment, written and filed after the examiner's summary, but tellingly that amendment did not dispute the examiner's summary of TPL's "ring oscillator" argument.

TPL's speculation that the examiner did not rely upon TPL's interview argument regarding the claimed "ring oscillator" is unsupported and immaterial. The Federal Circuit has held "on numerous occasions that patentee's statements during prosecution, whether relied on by the examiner or not, are relevant to claim interpretation." *Microsoft Corp.*, 357 F.3d at 1350.

TPL argues that *Salazar v. Procter & Gamble Co.*, 414 F.3d 1342 (Fed. Cir. 2005), applies, but it does not. *Salazar* held that "unilateral statements by an examiner" in a Notice of Allowance did not give rise to a disavowal by the patent owner. The statements at issue here were not "unilateral statements" by the examiner, but arguments made by TPL. The fact that the examiner recorded TPL's statements does not change the fact that it was TPL, not the examiner, who made them.

TPL also misapplies *University of Pittsburgh v. Hedrick*, 573 F.3d 1290 (Fed. Cir. 2009), which refused to give weight to a "terse" and ambiguous interview summary that was unclear concerning which features of the claimed invention, if any, were being distinguished. *Id.* at 1297. In the present case, however, TPL clearly argued that the claimed ring oscillator "distinguish[es] over what Talbot teaches" because it has "features" such as "being non-controllable, and being variable based on the environment." Interview Summary, 2/12/08, Control No. 90/008,227 (Chen Decl., Ex. 4). These disavowals clearly identify the claim language and the features on which it is distinguished.

Finally, there is no merit to TPL's suggestion that its disavowal is ineffective because it occurred in the reexamination of the '148 patent. The '148 patent shares the same specification and is directly related to the other three patents-in-suit, all of which claim a "ring oscillator." The Federal Circuit has made clear that "[a]ny statement of the patentee in the prosecution of a related application as to the scope of the invention would be relevant to claim construction." *Microsoft Corp.*, 357 F.3d at 1350. Accordingly, TPL's arguments in the '148 reexamination are relevant to how common claim language should be interpreted in closely-related patents. TPL has not argued that "ring oscillator" should be construed differently in the '148 patent, nor would there be any basis for TPL to do so. In light of TPL's disavowing statements made to the PTO after Judge Ward's ruling, Plaintiffs' proposal should be adopted.

#### *iii. "Non-controllable" and "variable based on the environment" is consistent with TPL's description of the ring oscillator during the original prosecution.*

TPL's reexamination disavowal as to the ring oscillator being "non-controllable" and "variable based on the environment" was essentially a shorthand summary of the numerous arguments the applicants made during the original prosecution of the '336 patent to overcome multiple prior art references. The original prosecution history underscores that the variable speed clock is non-controllable because its frequency variation is based on environmental parameters.

TPL distorts the specification to argue the claimed ring oscillator is "controllable via these [environmental] parameters" because "temperature, voltage and process are all controllable to one degree or another." Opening Br. at 18 (quoting '336, 16:59-60). TPL is wrong. Nowhere does the patent or prosecution history suggest using the environmental parameters to somehow control the ring oscillator. Instead, as described by the patent and prosecution history, the claimed ring oscillator ***naturally*** clocks the CPU at its maximum speed because they are comprised of the same transistors on the same integrated circuit and respond to ***uncontrollable*** variations in temperature, voltage and manufacturing process in the same way. *See, e.g.*, '336 PH 04/15/1996 Amend. at 8 (emphasis added) (Chen Decl., Ex. 5 at HTCMSJ000025) ("the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (*e.g.*, temperature) affecting circuit performance"). No control of the ring oscillator is needed or permitted. Indeed, any control of the ring oscillator would defeat the purpose of the alleged invention by slowing the CPU from its maximum speed, as done in the prior art.

In the '336 prosecution history, TPL repeatedly drew the distinction between (a) deliberate "control" of the oscillator's frequency through an input signal, crystal or other component of the system and (b) the ability of the oscillator's frequency to vary based on the "environmental parameters" of temperature, voltage and process. For example, in response to rejections of claims reciting a "variable speed clock," a "ring oscillator variable speed system clock" and an "oscillator," TPL made the following argument:

> **A <u>ring oscillator</u> will oscillate at a frequency determined by its fabrication and design and the operating environment**. Thus in this example, the user designs the ring oscillator (clock) to oscillate at a frequency appropriate for the driven device when both the oscillator and the device are under specified fabrication and environmental parameters. **Crucial to the present invention is that** since both the oscillator or variable speed clock and driven device are on the same substrate, **when the fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together. This differs from all cited references in** that the oscillator or variable speed clock and the driven device are on the same substrate, and **that the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so**.

'336 PH Amend. 07/07/1997 at 5 (Chen Decl., Ex. 5 at HTCMSJ000014) (emphasis added).

The patent owner continued to draw this "crucial" distinction between the prior art's concept of "control" (*e.g.*, based on manual or programmed inputs or external components) and the environmental factors discussed in the patent. For example, the patent owner contrasted the "frequency controlled" clock in U.S. Patent No. 4,503,500 ("Magar") with the claimed "variable speed clock," "ring oscillator variable speed system clock" and "oscillator" as follows:

> [O]ne of ordinary skill in the art should readily recognize that **the speed of the cpu and**

> **the clock *do not* vary together due to manufacturing variation, operating voltage and temperature** of the IC in the Magar microprocessor . . . This is simply because the **Magar microprocessor clock is frequency controlled by a crystal** which is also external to the microprocessor. Crystals are by design fixed-frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. **The Magar microprocessor in no way contemplates a variable speed clock as claimed**.

*See id.* at 3-4 (Chen Decl., Ex. 5 at HTCMSJ000012-13) (italics in original; boldface and underlining added). The patent owner further argued:

> **[C]rystals are by design fixed-frequency devices whose oscillation frequency is designed to be tightly controlled** and to vary minimally due to variations in manufacturing, operating voltage and temperature. **The oscillation frequency of a crystal on the same substrate with the microprocessor would inherently not vary due to variations in manufacturing, operating voltage and temperature** in the same way as the frequency capability of the microprocessor on the same underlying substrate, as claimed.

*See id.* at 4 (Chen Decl., Ex. 5 at HTCMSJ000013) (emphasis added).

In another example, the patent owner distinguished the "frequency control information" and "clock control signals" in U.S. Patent No. 4,670,837 ("Sheets") from the claimed variable speed clocking mechanisms:

> **The present invention does not similarly rely upon provision of frequency control information to an external clock**, but instead contemplates providing a ring oscillator clock and the microprocessor within the same integrated circuit. The placement of these elements within the same integrated circuit obviates the need for provision of the type of **frequency control information** described by Sheets, since **the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance**. Sheets' system for providing **clock control signals** to an external clock is thus seen to be unrelated to the integral microprocessor/clock system of the present invention.

'336 PH 04/15/1996 Amend. at 8 (Chen Decl., Ex. 5 at HTCMSJ000025) (emphasis added).

Specifically, the patent owner pointed out that the claimed oscillator will "naturally tend to vary commensurately in speed as a function of **various parameters (e.g., temperature)** affecting circuit performance." *Id.* (emphasis added). Later, the patentee went even further to distinguish Sheets' clock "in the same integrated circuit" controlled by a "command input" as follows:

> Even if the Examiner is correct that the variable clock in Sheets is in the same integrated circuit as the microprocessor of system 100, that still does not give the claimed subject matter. In Sheets, a command input is required to change the clock speed. **In the present invention, the clock speed varies correspondingly to variations in operating**

> **parameters of the electronic devices of the microprocessor because both the variable speed clock and the microprocessor are fabricated together in the same integrated circuit. No command input is necessary to change the clock frequency**.

’336 PH 01/03/1997 Amend. at 4 ( Chen Decl., Ex. 5 at HTCMSJ000016) (emphasis added).

As the preceding discussion shows, the patent owners consistently characterized the claimed “variable speed clock,” “ring oscillator variable system clock” and “oscillator” as environmentally dependent, and expressly distinguished prior art clocks that were “controlled,” whether through “clock control signals,” “frequency control information,” or “command inputs.” It should therefore come as no surprise that, during reexamination, TPL again emphasized the “features of a ring oscillator, such as being non-controllable, and being variable based on the environment” as distinguishing the claims over the prior art. Interview Summary, 2/12/08, Control No. 90/008,227 (Chen Decl., Ex. 4).

#### iv. *Plaintiffs’ construction of the other clock-related terms should be adopted.*

The term “providing an entire variable speed clock disposed upon said integrated circuit substrate” should be construed together with the other two “ring oscillator” related terms: “an entire ring oscillator variable speed system clock in said single integrated circuit” and “an entire oscillator disposed upon said integrated circuit substrate.” Although the ’336 patent language uses three different terms to claim the variable speed clock in the claims (i.e., “variable speed clock,” “ring oscillator variable speed system clock” and “oscillator,”) each side has proposed parallel constructions for each term with common limitations, as shown below:

| Term | Plaintiffs’ Construction | TPL’s Construction |
|---|---|---|
| providing an entire variable speed clock disposed upon said integrated circuit substrate | Providing a variable speed clock<br>that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an external crystal/clock generator to generate a clock signal,<br>wherein the variable speed clock is: (1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters in the environment | Providing a variable speed **system** clock<br>that is located entirely on the same semiconductor substrate as the CPU and does not **directly** rely on a **command input** control signal or an external crystal/clock generator to generate a clock signal |

| Term | Plaintiffs' Construction | TPL's Construction |
|---|---|---|
| an entire ring oscillator variable speed system clock in said single integrated circuit | A ring oscillator variable speed system clock<br>that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an external crystal/clock generator to generate a clock signal,<br>wherein the ring oscillator variable speed system clock is: (1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters in the environment | A ring oscillator variable speed system clock<br>that is located entirely on the same semiconductor substrate as the CPU and does not **directly** rely on a **command input** control signal or an external crystal/clock generator to generate a clock signal |
| an entire oscillator disposed upon said integrated circuit substrate | An oscillator<br>that is located entirely on the same semiconductor substrate as the CPU and does not rely on a control signal or an external crystal/clock generator to generate a clock signal,<br>wherein the oscillator is: (1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters in the environment | An oscillator<br>that is located entirely on the same semiconductor substrate as the CPU and does not **directly** rely on a **command input** control signal or an external crystal/clock generator to generate a clock signal |

The parties appear to agree that these three terms present common issues notwithstanding differences in terminology. Both sides have treated the three terms in parallel fashion, reflecting that they are supported by the same "ring oscillator" disclosure in the specification. *See Nystrom v. Trex Co.*, 424 F.3d 1136, 1143 (Fed. Cir. 2005) ("Different terms or phrases in separate claims may be construed to cover the same subject matter where the written description and prosecution history indicate that such a reading of the terms or phrases is proper.").

The disputes regarding these terms fall into two categories. First, for the reasons explained above, these terms should incorporate the requirement that the clock be "(1) non-controllable; and (2) variable based on the temperature, voltage, and process parameters in the environment," based on the patent owner's explicit arguments during prosecution and reexamination.

The remaining dispute turns on whether the claimed variable speed clock "does not rely on a control signal" (Plaintiffs' proposal) or whether the signal must be a specific "command input control signal" that is "directly" relied upon, as TPL proposes. Plaintiffs' construction incorporates TPL's arguments that the variable speed clock must be "non-controllable." Logically, a "non-controllable" clock cannot rely in any way – directly, indirectly, or otherwise – on any "control signal," whether it is based upon "clock control signals," "frequency control information," or "command inputs," which was disclaimed during the '336 prosecution. Indeed, the specification discloses no "control signal" for the claimed clocking mechanisms, and inclusion of the word "directly" has no support in the intrinsic record. Plaintiffs' proposed language, which does not include "directly" or "command input," should therefore be adopted.

TPL's proposal also improperly attempts to recapture subject matter it surrendered when it distinguished the Talbot reference. TPL now contends that a clocking circuit known as a "phase locked loop" ("PLL") infringes the "non-controllable" clocking mechanisms, despite the fact that TPL previously argued that its claims do not cover such an arrangement in order to overcome the Talbot reference. *See generally* HTC's Motion for Summary Judgment of Non-Infringement (Doc. No. 293 in *HTC* action). Talbot discloses a phase-locked loop (PLL), as confirmed by its title: "Integrated Circuit Phase Locked Looped Timing Apparatus." The PLL that TPL attempted to distinguish is shown in Figure 1 of Talbot reproduced below (the PLL is numbered as **4**):

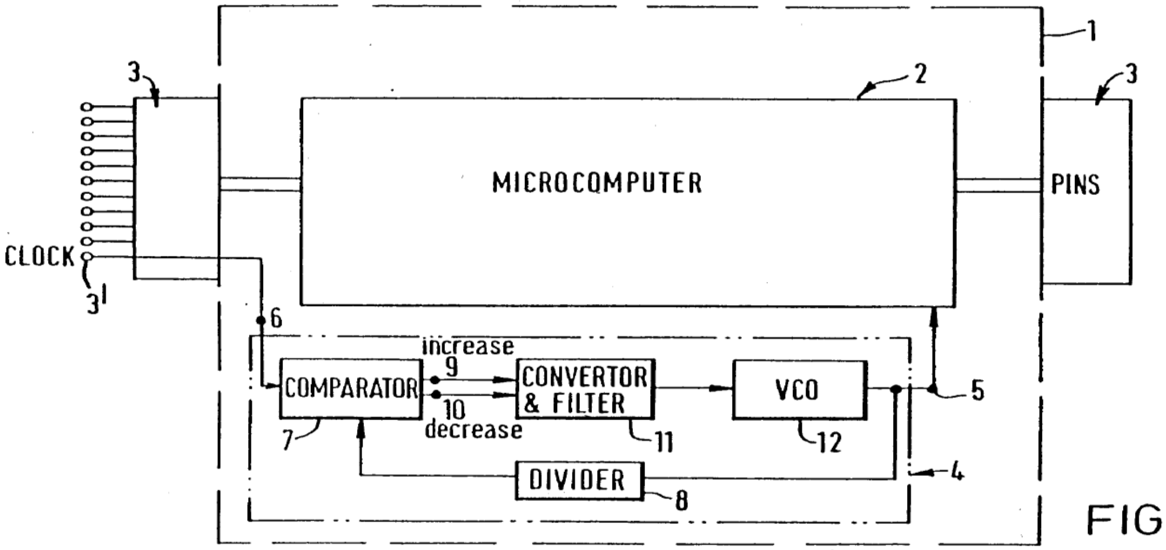

FIG.1

A phase-locked loop provides a clock whose output frequency is *controlled* by locking the phase of the output clock signal to the phase of the input clock signal provided by an external crystal clock. For example, if the frequency of the crystal clock relied upon by a phase-locked loop is 10

MHz (10 million cycles per second), the phase-locked loop can multiply the crystal frequency by 2 or 3 to provide clock signal frequencies at 20 MHz or 30 MHz, respectively.

As noted above, TPL argued that the claimed ring oscillator was "non-controllable" and "variable based on the environment," and was distinguishable from Talbot. The particular oscillator in Talbot was a "voltage-controlled oscillator," shown as "**VCO**" in Figure 1 above (item 12). *See* Amendment, 2/26/08 at 11 (Chen Decl., Ex. 6) and Interview Summary, 2/12/08, Control No. 90/008,227 (Chen Decl., Ex. 4). The frequency of Talbot's voltage-controlled oscillator **12** is "controlled" by a "control signal" based upon the external clock signal (item 3). *See* Talbot at 2:58-63, 3:7-16, 3:26-36 (Chen Decl., Ex. 3) ("[A] convertor and filter circuit **11** . . . is arranged to convert the output pulses from the comparator **7** into **a voltage signal for controlling the frequency of oscillation of a voltage controlled oscillator circuit 12**.") (emphasis added). Talbot's voltage-controlled oscillator, therefore, relies on a control signal and an external crystal/clock generator to generate its clock signal. *See id.*

TPL's clear disclaimer of Talbot's voltage-controlled oscillator confirms that the claimed clocking mechanisms do not include a clock that relies on a control signal (voltage, current or otherwise) or external crystal clock generator. In fact, absent its reliance on the control signal and external clock, Talbot's voltage-controlled oscillator **12** is structurally no different than an "oscillator having a multiple, odd number of inversions arranged in a loop," which is how TPL proposes to construe the term "ring oscillator." *See* Wolfe Decl. in support of Plaintiffs' Sur-Reply (Doc. No. 266 in *Acer* action).[4]

As noted, TPL now seeks to accuse the same type of voltage-controlled clocks it had to disclaim during prosecution and reexamination. *See* Chen Ex. 7. It would be improper to permit this. *See Desper Prods., Inc. v. QSound Labs, Inc.*, 157 F.3d 1325, 1340 (Fed. Cir. 1998) ("Post-hoc, litigation-inspired argument cannot be used to reclaim subject matter that the public record in the PTO clearly shows has been abandoned."). Because the claimed clocking mechanisms are non-controllable and cannot rely on any signal, directly or otherwise, the words "directly" and

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[4] Judge Fogel permitted the filing of the Wolfe Declaration during the prior briefing to rebut TPL's incorrect factual assertion that Talbot did not disclose an odd number of inversions in a loop.

"command input" should be removed from Judge Ward's construction, and Plaintiffs' proposals should be adopted in their entirety.

### *v. Construction of "clocking said CPU" ('336 patent)*

The disputed phrase, "clocking said CPU," is in all asserted claims of the '336 patent. The dispute is whether the claimed variable speed clock will time the operation of the CPU at its maximum frequency as disclosed by the specification:

| **Plaintiffs' Construction** [JCCS 20] | **TPL's Construction** |
|---|---|
| Timing the operation of the CPU **such that it will always execute at the maximum frequency possible, but never too fast** | Timing the operation of the CPU |

Plaintiffs' construction of "clocking said CPU" states that the CPU "will always execute at the maximum frequency possible, but never too fast," that is based directly on the clear statements in the specification and prosecution history. As noted above, the specification criticizes prior art approaches resulting in a CPU that operates at less than half of its theoretical maximum performance. '336, 16:50-53. The specification instead asserts that the alleged invention, "[b]y deriving system timing from the ring oscillator 430, CPU 70 will **always execute at the maximum frequency possible, but never too fast**." '336, 16:59-17:2 (emphasis added).

TPL argues that Plaintiffs' construction attempts to import limitations from the specification. TPL is wrong. This patent is not entitled to claims broader than the sole embodiment in the specification. When the embodiment "is described in the specification as the invention itself, the claims are not necessarily entitled to a scope broader than that embodiment." *Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1330 (Fed. Cir. 2009) (citation omitted). Moreover, "[w]here the specification makes clear that the invention does not include a particular feature, that feature is deemed to be outside the reach of the claims of the patent, even though the language of the claims, read without reference to the specification, might be considered broad enough to encompass the feature in question." *Id.* at 1329 (citation omitted). And finally, when the specification "describes a feature of the invention ... and criticizes other products ... that lack that same feature, this operates as a clear disavowal of these other products...." *Id.* at 1333.

All of these principles apply here because the specification emphatically declares that the

CPU of the alleged invention "always" executes at the maximum frequency and criticizes products that lack that feature. The patent owner also relied on this feature to distinguish the Sheets reference during prosecution of the '336 patent, arguing that "CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430." Amendment, 4/15/96 at 8-9 (Chen Decl., Ex. 8). The term "clocking said CPU" should therefore be construed to require "timing the operation of the CPU such that it will always execute at its maximum frequency possible, but never too fast."

### *vi. Construction of "operates asynchronously to" ('336)*

The phrase "operates asynchronously to" appears at the end of claims 11, 13 and 16 and is part of the longer phrase: "wherein said central processing unit **operates asynchronously to** said input/output interface." The dispute is whether operating "asynchronously" excludes synchronous operation using independent clocks:

| **Plaintiffs' Construction** [JCCS 29] | **TPL's Construction** |
|---|---|
| operates without a timing relationship to/with | timed by independent clock signals |

As discussed above, the patent discloses a variable speed ring oscillator that clocks the CPU at its maximum frequency possible while varying its frequency based on the environmental conditions. However, for the CPU to communicate with outside components, "[t]he external world must be synchronized to the microprocessor **50** for operations such as video display updating and disc drive reading and writing." '336, 17:23-25. To synchronize the microprocessor with the external world, a second, fixed speed clock for timing the I/O interface is provided. "This synchronization is performed by the I/O interface **432**, speed of which is controlled by a conventional crystal clock **434**." '336, 17:25-27. The specification explains that this "dual clock scheme" has the additional advantage of not dragging down the CPU's speed with the typically slower I/O interface. '336, 17:12-21.

To allow the CPU to always execute at the maximum frequency possible and not be dragged down by the speed of the I/O interface, the CPU must operate "asynchronously," *i.e.*, without a timing relationship with, the I/O interface. Indeed, it is logically impossible for the CPU's environmentally dependent "***variable*** speed clock" to have any timing relationship with the I/O interface's ***fixed*** frequency clock.

TPL's proposed construction, "timed by independent clock signals," is contrary to the plain meaning of "asynchronous" because "independent" clock signals can nevertheless have a timing relationship with one other – in other words, be "synchronized." Anything that is synchronized, by definition, is not "**<u>a</u>**synchronous." A simple example of "independent" yet synchronized clocks comes from old war movies in which soldiers synchronize their "independent" wrist watches. During reexamination, TPL actually dedicated an entire section entitled "Synchronism Does Not Preclude Independence" to distinguish the Kato prior art by arguing that "independent" clocks may nonetheless be synchronous. *See* Amendment, 9/8/08, pp. 21-22 of 28 (Chen Decl., Ex. 9). TPL's argument that two "independent" clocks can nonetheless operate "synchronously" fatally undermines its current litigation position on the meaning of "asynchronously." TPL's proposed construction, as admitted by TPL, improperly includes both asynchronous <u>and</u> synchronous operations, contrary to the plain claim language.

TPL's definition is derived entirely from an excerpt of an extrinsic reference, *Computation Structures*, that TPL submitted to the PTO in the reexamination. *See* Opening Br. at 12. TPL's reliance on this textbook is problematic. Because the excerpt was submitted to the PTO during this litigation, perhaps in anticipation of claim construction, it should be given little weight. *See Moleculon Research Corp. v. CBS, Inc.*, 793 F.2d 1261, 1270 (Fed. Cir. 1986) (observing that documents submitted to PTO during litigation "might very well contain merely self-serving statements which likely would be accorded no more weight than testimony of an interested witness or argument of counsel."). TPL's reliance on its own submission also improperly attempts to use the prosecution history to broaden the scope of its claims. *See, e.g., Dow Chem. Co. v. NOVA Chems. Corp. (Can.)*, 629 F. Supp. 2d 397, 415 (D. Del. 2009) ("[Plaintiff] does not cite any authority, and the Court is not aware of any, suggesting that the prosecution history can be used to broaden the scope of claims beyond that which is supported by the specification.").

A more relevant portion of that textbook, which TPL failed to submit to the PTO or this Court, shows that by "independent clocks," the textbook actually describes separate clocks with no timing relationship. In a section entitled "Multiple-Clock Systems," the book describes a situation involving "multiple asynchronous clocks, each clock a **free-running** oscillator generating [clock signals] independently of the others." Chen Decl., Ex. 10 at 175 (emphasis added). The book goes on to explain: "This relationship is common among large, independently designed subsystems; as an extreme example, the interconnection of two separate computers (each of which may run synchronously with its single clock) constitutes a system with at least two unsynchronized clocks." *Id.* Two separate computers, which might have been powered on at different times and may be separated by great distances, present a clear example of two things that operate without a timing relationship with each other, or in other words, asynchronously. This passage clarifies that when *Computation Structures* uses the term "independent" in the context of asynchronous operations, it is referring to the lack of a timing relationship.

### *vii. Construction of "as a function of parameter variation" ('336/'148)*

The '336 and '148 patents require that the CPU's maximum speed for proper operations and the "oscillator" vary in the same way "as a function of parameter variation" in fabrication or operational parameters. The two sides' competing proposals are below:

| Plaintiffs' Construction | TPL's Construction |
|---|---|
| **in a determined functional relationship with** parameter variation | **based on** parameter variation |

The specification explains that the temperature, voltage and process parameters in the environment "determine" the CPU's and the oscillator's frequencies in a "functional relationship:"

> The ring oscillator['s] frequency is **determined by** the parameters of temperature, voltage, and process. At room temperature, the frequency will be in the neighborhood of 100 MHZ. At 70 degrees Centigrade, the speed will be 50 MHZ. The ring oscillator **430** is useful as a system clock, . . . because its performance tracks the parameters which similarly affect all other transistors on the same silicon die.

'336, 16:59-67 (emphasis added). By disclosing that the ring oscillator's frequency is "determined by" the environmental parameters and claiming that the CPU's processing frequency is a "function" of the parameters' variation, the claims require that the frequency of the CPU and the on-chip oscillator have a specific and unique value for any given combination of temperature, voltage and process. Put another way, for a given combination of temperature, voltage and process parameters, the CPU's and the on-chip oscillator's frequencies should be reproducible. The numerical example provided by the specification in fact suggests such a determined functional relationship. ’336, 16:60-63 (“At room temperature, the frequency will be in the neighborhood of 100 MHZ. At 70 degrees Centigrade, the speed will be 50 MHZ.”). Plaintiffs’ proposed construction captures this requirement of a “determined” value. Plaintiffs’ construction is also consistent with and interpretive of the example in the specification discussed above.

TPL’s proposed construction is too vague and claims, as environmental parameters vary, non-reproducible, even random (*i.e.*, undetermined) CPU and oscillator frequencies for a given combination of temperature, voltage and process. Thus, TPL’s proposal should be rejected.

### B. Microprocessor Architecture Related Terms from the ’890 and ’749 Patents

The ’890 and ’749 patents, both entitled “High Performance, Low Cost Microprocessor Architecture,” disclose different aspects of a specialized microprocessor system. The following five related terms from the ’890 and ’749 patents will be discussed together: “separate direct memory access central processing unit,” “(first) push down stack connected to said arithmetic logic unit,” “supplying the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle,” “instruction register” and “multiple sequential instructions.”

#### *i. Construction of “separate direct memory access central processing unit” (’890)*

The ’890 patent purports to describe aspects of the specialized microprocessor architecture intended to allow faster access to certain memory locations. Claim 11, the only independent claim of the ’890 patent following the reexamination,[5] recites “[a] microprocessor, which comprises a main central processing unit and **a separate direct memory access central processing unit** in a single integrated circuit….” ’890, Reexam. Cert., Claim 11 (Chen Decl., Ex. 11) (emphasis added).

The term “direct memory access” or “DMA” is a well-known technology for improving the performance of computer systems. DMA allows certain subsystems or components within a computer (such as a disk drive or other device) to transfer data to memory without the main CPU having to perform the actual data transfer, allowing the CPU to perform other tasks. The ’890 patent acknowledges that conventional “DMA controllers can provide routine handling of DMA

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[5] Claim 1 was canceled in the reexamination and new claim 11 was added.

requests and responses, but some processing by the main central processing unit (CPU) of the microprocessor is required." '890, 1:55-58. The '890 patent purports to address this problem by claiming a "separate direct memory access **central processing unit**" ("separate DMA CPU"), for which the parties have proposed the following constructions:

| Plaintiffs' Construction | TPL's Construction |
|---|---|
| a separate central processing unit that fetches and executes instructions for performing direct memory access without using the main central processing unit | electrical circuit for reading and writing to memory that is separate from a main CPU |

Plaintiffs' proposed construction is the only one that comports with the specification and claim language of the '890 patent. The claim language itself recites "a **separate** direct memory access central processing unit," which is "separate" in the sense that it is physically and functionally distinct from the main CPU. As explained in the specification: "The DMA CPU **72** controls itself and has the ability to fetch and execute instructions. It operates as a co-processor to the main CPU **70** (FIG. 2) for time specific processing." '890, 8:22-24. The specification criticizes "conventional microprocessors" that use "DMA controllers" because "some processing by the main central processing unit (CPU) of the microprocessor is required." '890, 1:52-58. The specification identifies as an object of the invention a processor "in which DMA does not require use of the main CPU during DMA requests and responses and which provides very rapid DMA response with predictable response times." '890, 2:2-5. The specification confirms, therefore, that a separate DMA CPU is a separate CPU that fetches and executes instructions for performing DMA without using the main CPU, as Plaintiffs have proposed.

TPL's proposal should be rejected because it ignores the "CPU" in the claim term "DMA CPU." TPL relies on the disclosure of a "DMA controller" embodiment that, as a matter of plain claim language, is unclaimed. The DMA CPU, unlike a conventional DMA controller, has the ability to fetch and execute instructions. TPL concedes in its opening brief that "DMA controllers" are different from the claimed "DMA CPU" because: "This 'more traditional DMA controller' is one that functions more as a **traditional** state machine, **without the ability to fetch its own instructions that characterizes a CPU**." Opening Br. at 9:24-26 (emphasis added). But the ability to fetch instructions – a feature that even TPL concedes "characterizes a CPU" – is conspicuously missing from its construction of DMA CPU. TPL's construction attempts to rewrite the claim to remove "CPU" from the claim term "DMA CPU." This would be improper. *See K-2 Corp. v. Salomon S.A.*, 191 F.3d 1356, 1364 (Fed. Cir. 1999) ("Courts do not rewrite claims; instead, we give effect to the terms chosen by the patentee").

TPL attempts to equate the DMA CPU 314 of Figure 9 with a DMA controller, but TPL is wrong. Figure 9 shows "a layout diagram of a second embodiment of a microprocessor" that has a "DMA CPU 314." '890, 4:61-63 and Fig. 9. A separate passage appearing eight columns later in the specification describes a different and unclaimed embodiment in which "the DMA processor **72** of the microprocessor **50** has been replaced with a more traditional DMA controller **314**." '890, 12:62-13:4. That passage makes no reference to Figure 9 or the DMA CPU described earlier in the specification, and in fact, actually supports Plaintiffs' position. By disclosing an alternative system in which a DMA CPU has been "**replaced** with a more traditional DMA controller 314" ('890, 12:62-13:4 (emphasis added)), the specification actually confirms that a DMA CPU is **different** from a DMA controller.

TPL's assertion that Plaintiffs' construction would exclude a preferred embodiment is similarly without merit. The Federal Circuit has repeatedly recognized that a specification can disclose subject matter not covered by the claims. *See TIP Sys., LLC v. Phillips & Brooks/Gladwin, Inc.*, 529 F.3d 1364, 1373 (Fed. Cir. 2008) ("Our precedent is replete with examples of subject matter that is included in the specification, but is not claimed."). "Therefore, the mere fact that there is an alternative embodiment disclosed in the [patent-in-suit] that is not encompassed by [a proposed] claim construction does not outweigh the language of the claim, especially when [that] construction is supported by the intrinsic evidence." *Id.* Because the specification describes the DMA CPU as an improvement and replacement over the conventional DMA controller, it makes sense that the claims exclude the DMA controller. Because TPL's construction improperly seeks to lay claim over the DMA controller that the specification distinguishes from the claimed DMA CPU, it should be rejected.

Finally, TPL asserts that Acer's claim construction expert, Dr. Wolfe, acknowledged that the main CPU can initiate memory transfers. Opening Br. at 10:3-8.[6] This argument misses the point completely: the issue is what a DMA CPU can do without the main CPU, not what the main CPU can do (with or without a DMA CPU). Although a main CPU can *initiate* a memory transfer request, the specification makes clear that the DMA memory transfer is actually *performed* by the DMA CPU – not the main CPU. '890, 2:2-5. Plaintiffs' proposed language, "*performing* direct memory access without using the main [CPU]," is therefore accurate and should be adopted.

#### ii. Construction of "push down stack" in "(first) push down stack connected to said arithmetic logic unit" ('749)

The '749 patent claims a specialized microprocessor architecture with a "first push down stack." (Chen Decl., Ex. 13.) The operation of a push down stack is often explained by analogy to a spring-loaded stack of plates at a cafeteria in which the most recently stored plate is pushed onto the top of the plate stack. The top item in the stack, the one that was most recently added, is also the first to be removed. A push down stack, therefore, operates in a "last-in-first-out" manner. When a new item is placed on the top of the stack, it "pushes" the other items down by one storage space, causing the other items to move towards the bottom of the stack by one space. This everyday analogy is consistent with how the term "push down stack" is used in the '749 patent, and is captured by Plaintiff's proposed construction:

| Plaintiffs' Construction | TPL's Construction |
|---|---|
| data storage elements organized **from top to bottom** to provide last-in first-out access to **stored** items, **wherein any previously stored items propagate towards the bottom by one data storage element when a new item is stored in the top data storage element** | data storage elements organized to provide last-in first-out access to items |

The term "push down stack" is a component of the larger phrase, "first push down stack connected to said arithmetic logic unit," which is among the top ten terms and addressed separately below.[7] Plaintiffs' construction of "push down stack" should be adopted because it is consistent with the intrinsic record and, unlike TPL's construction, explains for the jury what "last-in-first-out" means.

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[6] TPL mischaracterizes the testimony of Dr. Wolfe on this point. When asked if the main CPU can perform any DMA-related operations, he testified: "Any? I don't think so." Wolfe Depo. at 167:11-13 (Chen Decl., Ex. 12). Dr. Wolfe did testify that the main CPU can request a single element of data from memory, but made clear that such a request is not a "DMA-related" function. *Id.* at 167:19-168:10.

[7] Because "push down stack" is a component of "push down stack connected to said arithmetic logic unit," the parties are in agreement that these terms count as a single term.

During prosecution of the ’749 patent, the examiner described a push down stack as follows: “Note that a stack is such that inputted items propagate from one end of the stack to another via the stages in the stack.” ’749, Office Action 12/31/92 at 3 (Chen Decl., Ex. 14). “Statements about a claim term made by an examiner during prosecution of an application may be evidence of how one of skill in the art understood the term at the time the application was filed.” *Salazar*, 414 F.3d at 1347. Plaintiffs’ proposed construction accordingly incorporates the examiner’s concept that the inputted items “propagate” from the top of the stack towards the bottom, which accurately describes how a “push down stack” in the ’749 patent operates.

Construction of “(first) push down stack connected to said arithmetic logic unit”

The ’749 patent recites a “first push down stack connected to said arithmetic logic unit.” The parties’ proposed constructions are set forth below:

| Plaintiffs’ Construction | TPL’s Construction |
|---|---|
| (first) push down stack **comprising a top item register and a next item register, both directly coupled to** the ALU **such that source and destination addresses are not used** | data storage elements organized to provide last-in first-out access to items **connected to convey signals to** a digital circuit that performs both arithmetic and logical operations |

Plaintiffs have separately addressed the meaning of “push down stack” in the preceding section of this brief, and the parties have stipulated that an “arithmetic logic unit” (“ALU”) is a digital circuit that performs both arithmetic and logical operations. The remaining disputes with respect to this term relate to the structure of the first push down stack and the manner in which it is connected to the ALU. The specification and file history make clear that the “first push down stack” includes a top item and next item register directly coupled to the ALU such that source and destination addresses are not used.

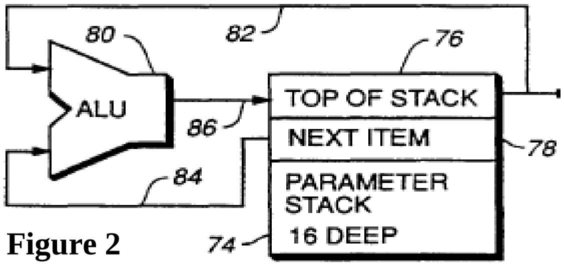

Figure 2

The “first push down stack” is depicted in Figure 2 of the ’749 patent, which shows how the first push down stack (74) is structurally connected to the ALU. TPL acknowledges in its opening brief that “Figure 2 discloses a push down stack (74) connected to separate top and next item registers (76 and 78).” Opening Br. at 21:13-14; *id.* at

21:2-3 ("Figure 2 illustrates dedicated registers that provide inputs to the ALU."). The specification explains: "The microprocessor **50** architecture has the ALU **80** (FIG. **2**) **directly coupled to the top two stack locations 76** and **78**." '749, 19:6-8 (emphasis added). This direct coupling is not merely a design choice of the disclosed embodiment, but an essential aspect of the claimed invention.

The '749 patent explains that prior art microprocessors rely on instructions that have to specify (a) the logical or arithmetic operation to be performed by the ALU ***and*** (b) the locations (i.e., addresses) of the two "sources" of the data to be used and one "destination" where the result of the operation will be held. *See* '749, 26:68-27:3. To take a simplified example, suppose an instruction specifies a computation in which a first number (X) is added to a second number (Y) to yield a third number (Z) (i.e., X+Y=Z). Such an instruction might require: (a) 8 bits to specify the "add" arithmetic operation to be performed, (b) 8 bits to specify the address of the first number (X), (c) 8 bits to specify the address of the second number (Y) and (d) 8 bits to specify the address where the computed value (Z) will be stored. '749, 26:68-27:3 ("Many 32-bit architectures use 8-bits to specify the operation to perform but use an additional 24-bits to specify two sources and a destination [because each requires 8-bits for addressing].").

The need to specify the source and destination addresses (b, c, and d above) is eliminated by the fact that the ALU is "directly coupled" to the top and next item registers (76) and (78). In particular, the top item and next item registers (76) and (78) hold the two sources for the operation. After the arithmetic or logic operation is completed, the top item register (76) serves as the destination holding the result of the operation. '749, 15:30-32 ("A math or logic operation always uses the top two stack items as source and the top of stack as destination."). Because the top item and next item registers are "directly coupled" to the ALU, the ALU can exchange data with them without the need for explicit addresses. '749, 7:19-22 ("The push down stack allows the use of implied addresses, rather than the prior art technique of explicit addresses for two sources and a destination."). Using the push down stack of the '749 patent, therefore, saves 24 bits.

The advantages of using an 8-bit instruction instead of a 32-bit instruction by eliminating the 24-bits used to specify the two sources and one destination were repeatedly emphasized throughout the specification:

> “For math and logic operations, the microprocessor **50** exploits the **inherent advantage** of a stack by **designating the source operand(s) as the top stack item and the next stack item**. The math or logic operation is performed, the operands are popped from the stack, and the result is pushed back on the stack. **The result is a very efficient utilization of instruction bits as well as registers**.” ’749, 26:4-11 (emphasis added).
>
> “Most microprocessors use on-chip registers for temporary storage of variables . . . A few microprocessors use an on-chip push down stack for temporary storage. A stack has the advantage of **faster operation compared to on-chip registers by avoiding the necessity to select source and destination registers.**” ’749, 15:24-30 (emphasis added).
>
> “The availability of 8-bit instructions also allows another architectural innovation, the fetching of four instructions in a single 32-bit memory cycle.” ’749, 26:16-18.

By touting the use of implicit addressing and criticizing the prior art’s use of explicit addressing, the patent owner told the public that **not** using explicit addressing for the top and next item locations of the first push down stack was essential to the invention. *See Edwards Lifesciences LLC*, 582 F.3d at 1334 (when the patent owner “describes a feature of the invention . . . and criticizes other products . . . that lack that same feature,” a clear disavowal of those other products results); *see also Microsoft Corp.*, 357 F.3d at 1347 (construing “connected to” as requiring direct connection based on description of invention in specification); *Inpro II Licensing, S.A.R.L. v. T-Mobile USA, Inc.*, 450 F.3d 1350, 1354-56 (Fed. Cir. 2006) (construing claim to require a “direct connection” between components based on statements in specification touting performance advantages of such a direct connection).

This point was reiterated during prosecution where the patent owner told the PTO that the connection between the ALU and the top and next item locations of the first push down stack are “in addition to the conventional construction of the first push down stack . . . .” ’749 File History, 7/6/93 Amendment at 9 (Chen Decl., Ex. 15). The importance of the recited “additional” connections was clear: “The [first push down] stack 74 in fact allows arithmetic operations to be carried out on operands supplied from it to the ALU and receives ALU results **as a result of the**

**recited connections**." *Id.* (emphasis added).

TPL's assertion that Plaintiffs' proposed construction improperly imports limitations from the specification also ignores the use of narrow "means-plus-function" language in the claim itself defining the "first push down stack." Claim 1 recites, in relevant part:

> **first push down stack connected to said arithmetic logic unit**,
> said **first push down stack** including
> **means** for storing a **top item** connected to a first input of said arithmetic logic unit to provide the top item to the first input and
> **means** for storing a **next item** connected to a second input of said arithmetic logic unit to provide the next item to the second input, . . . ,
> said arithmetic logic unit having an output connected to said **means** for storing a top item; […]

As shown above, the claim language expressly ***defines*** the "first push down stack" as including the "**means** for storing a top item" and the "**means** for storing a next item," and specifies the precise connections between them and the ALU. All parties agree that these top item and next item elements are written in means-plus-function format under 35 U.S.C. § 112 ¶ 6. Joint Claim Construction Statement, Ex. B at 3 (Doc. No. 305-2 in *Acer* action). Federal Circuit law is clear that a court ***must*** look to the specification to identify the corresponding structure for a means-plus-function element. *See Cardiac Pacemakers, Inc. v. St. Jude Med., Inc.*, 296 F.3d 1106, 1113 (Fed. Cir. 2002). Critically, "[a] structure disclosed in the specification qualifies as 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *Default Proof Credit Card Sys., Inc. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1298 (Fed. Cir. 2005). The top item and next item registers that are directly coupled to the ALU in Figure 2 precisely match the function recited in the claim language. The use of means-plus-function claim language defining the "first push down stack" and its connection to the ALU reinforces the critical importance of the specification in construing this term.

TPL ignores the disclosures in the specification and the claim language discussed above. TPL instead points to unrelated details in the specification that have nothing to do with the first push down stack or how it is connected to the ALU. TPL first contends that Figure 13 shows an alternative embodiment that does not disclose the dedicated registers of Figure 2. But TPL ignores that Figure 13 shows exactly the same arrangement as Figure 2, with precisely the same "direct coupling" between the top and next item registers and the ALU, as shown in the figures.

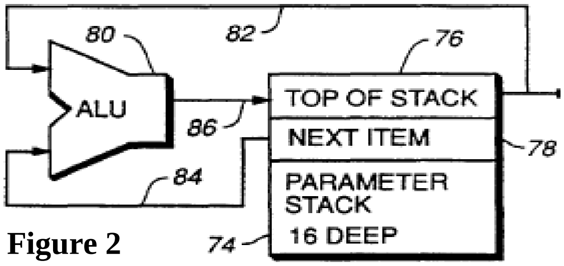

**Figure 2**

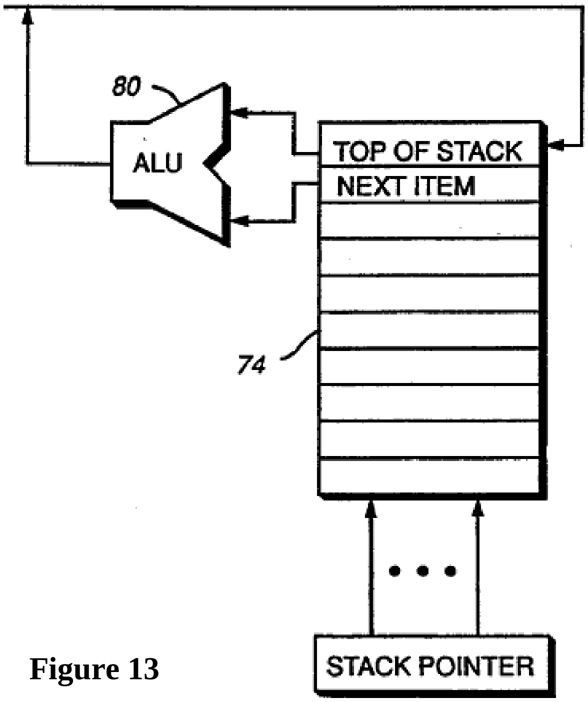

**Figure 13**

TPL's assertion that the "STACK POINTER" in Figure 13 is connected to the first push down stack is similarly baseless. *See* Opening Br. at 21:4-5. The stack pointer shown in Figure 13 is not used to communicate to the ALU at all. It is instead pointing to the *bottom* of the first push down stack. *See* '749, Fig. 13. Finally, TPL's argument based on the stack architecture in Figure 21 is similarly inapposite. Nothing in Figure 21 shows an ALU, let alone any connection between any push-down stack with top and next item registers and the ALU. Instead, the stack pointer is used only to manage inter-stack operations of the "triple cache stack architecture" illustrated in Figure 21. '336, 18:23-27.

The primary flaw in TPL's arguments regarding Figure 13 and 21 is that it ignores the specific term at issue here, the "**first** push down stack **connected to said arithmetic logic unit**." The portions of the figures cited by TPL relate to other stacks in the specification that are not the first push down stack. One such example is the "second push down stack" that is separately recited in claim 10. But the claim language itself confirms that the "**first** push down stack" is the one depicted in Figures 2 and 13 as item 74, because it is the only push down stack in the specification that is "connected to said arithmetic logic unit" ***and*** has a "top item" register and a "next item" register connected to inputs of the ALU, as expressly recited in the claim language. TPL's attempt to point to details of other stacks that are not the "first push down stack" is unavailing.

### *iii. Construction of "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle"*

The microprocessor described in the '749 patent operates by fetching "instructions" (which specify CPU operations) from memory into an instruction register, which supplies them to the CPU for execution. The '749 patent explains, however, that "[t]he slowest procedure the microprocessor **50** performs is to access memory. Memory is accessed when data is read or written. Memory is also read when instructions are fetched." '749, 22:14-17. "The bottleneck in most computer systems is the memory bus. The bus is used to fetch instructions and fetch and store data." '749, 5:54-56. The '749 patent purports to address this issue by fetching multiple instructions from memory and then supplying them to the CPU during "a single memory cycle."

According to the '749 patent, because the CPU can execute instructions much faster than they can be fetched from memory, multiple instructions can be executed during a single memory cycle. The alleged invention allows fetching and execution of instructions to be overlapped, resulting in performance improvements. *See* '749, 22:17-40. The specification repeatedly touts the advantages of this feature, including:

> "The microprocessor **50** fetches 4 instructions per memory cycle . . . System speed is therefore 4 times the memory bus bandwidth. This ability enables the microprocessor to break the Von Neumann bottleneck of the speed of getting the next instruction." '749, 7:12-15.
>
> "The bottleneck in most computer systems is the memory bus. The bus is used to fetch instructions and fetch and store data. The ability to fetch four instructions in a single memory bus cycle significantly increases the bus availability to handle data." '749, 5:54-58.
>
> "The microprocessor **50** fetches up to four instructions in a single memory cycle and can perform much useful work before requiring another memory access." '749, 18:10-12.

Claim 1 captures this requirement by reciting the following limitation (boldface type showing the disputed term): "said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and **supply the multiple sequential instructions to said central processing unit during a single memory cycle**." '749, claim 1. The parties have proposed the following constructions:

| Plaintiffs' Construction | TPL's Construction |
|---|---|
| provide the multiple sequential instructions in parallel **(as opposed to one-by-one)** to said central processing unit integrated circuit during a single memory cycle **without using a prefetch buffer or a one-instruction-wide instruction buffer, that supplies one instruction at a time** | provide the multiple sequential instructions in parallel to said central processing unit integrated circuit during a single memory cycle |

The additional language in Plaintiffs' proposed construction comes directly from TPL's express disclaimer made during reexamination of the '749 patent. In particular, in attempting to distinguish U.S. Patent No. 4,680,698 to Edwards ("Edwards"), TPL argued:

> Edwards describes the way the Transputer decodes and executes instructions. **As described in Edwards,** see, e.g., Fig. 8, below, **instructions are supplied to a one-instruction-wide instruction buffer, one at a time**, and are there decoded. **Fetching multiple instructions into a prefetch buffer and then supplying them one at a time is not sufficient to meet the claim limitation** – the supplying of 'multiple sequential instructions to a CPU during a single memory cycle.'

Amendment, 1/19/10 at 26 of 58 (Chen Decl., Ex. 16) (emphasis added).[8] TPL further made a similar disavowal in attempting to distinguish an article entitled *The Motorola MC68020* by Doug MacGregor et al. ("MacGregor"):

> However, [MacGregor] does not disclose fetching "multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle". MacGregor might imply that it fetches two instructions from memory at a time, **but the instructions are supplied to the CPU one at a time**. **Such non-parallel supplying of instructions to the CPU is not supplying them to the CPU during a single memory cycle as required by the claim**.

*Id.* at 45 (emphasis added). Then, following an interview with the Examiner, TPL filed a written response summarizing the substance of the interview and further disclaimed systems that supply instructions to the CPU one at a time:

> Next the MacGregor reference was discussed [during the interview]. Mr. Henneman [TPL's counsel] explained that **although two instructions might be fetched at the same time, only one instruction is supplied to the CPU at a time**. The second instruction is stored in a temporary register. Because MacGregor only discloses providing instructions to the CPU one-at-a-time, Examiner Pokrzwya indicated that he would reconsider this rejection.

11/29/2010 Interview Summary at 19-20 of 35 (Chen Decl., Ex. 18) (emphasis added).

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[8] Citing no evidentiary support, TPL asserts that "the instructions [in Edwards] were not supplied to the instruction register until a second memory cycle." Opening Br. at 14. Nothing in Edwards supports TPL's assertion. *See* Chen Decl., Ex. 17.

Emphasizing how important this feature is, TPL made this point yet again:

> As discussed in the interview and elaborated on above with respect to the May/Edwards rejections, **the "during a single memory cycle" limitation is not satisfied by supplying only one instruction to a CPU at a time**. Rather, the "multiple sequential instructions" must be supplied "during a single memory cycle."

11/29/2010 Remarks at 13 of 35 (Chen Decl. 18) (emphasis added).

As such, this term must be construed consistently with the multiple clear and unmistakable disavowals and disclaimers that TPL made to the PTO. *See Rheox*, 276 F.3d at 1325. This phrase should be construed as providing the multiple sequential instructions "in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during a single memory cycle without using a prefetch buffer or a one-instruction-wide buffer, that supplies one instruction at a time." Doc. No. 243 in *HTC* action, at 25:11-14.

#### *iv. Construction of "instruction register"*

Computer instructions generally include two components, known as "opcodes" and "operands." An "opcode" is generally used to specify a specific logical or arithmetic operation to perform, while "operands" specify the data that will be subject to the operation. In a theoretical instruction in which two numbers are added together, *i.e.*, A+B, the opcode is "+" and the two operands identify A and B. This theoretical instruction could then be provided to an "instruction register," which supplies the instruction to circuits that interpret and execute the instruction (in this case, by adding the two numbers). The dispute here turns on how the operands in the "instruction register" are arranged. The parties' proposed constructions are set forth below:

| Plaintiffs' Construction | TPL's Construction |
|---|---|
| register that receives and holds one or more instructions for supplying to circuits that interpret the instructions**, in which any operands that are present must be right-justified in the register** | register that receives and holds one or more instructions for supplying to circuits that interpret the instruction |

Plaintiffs' proposed construction of "instruction register" should be adopted because it alone comports with the undisputed intrinsic evidence. The '749 patent describes a specialized instruction register that, according to the specification, provides significant advantages over prior art systems. The specification explains that, unlike prior art microprocessors, the processor in the

’749 patent can handle operands of variable sizes using the same opcode. ’749, 18:35-37. The specification describes this accomplishment as “magic,” and explains that: “This magic is possible because **operands must be right justified in the instruction register**. This means that the least significant bit of the operand is always located in the least significant [i.e., right-most] bit of the instruction register.” ’749, 18:43-47 (emphasis added). The specification makes clear, therefore, that right justified operands in the instruction register are not an optional design choice of one embodiment, but a required feature – something that “must” be present in order to accomplish the “magic” of the alleged invention.

TPL further emphasized this “magic” during the original prosecution of the ’749 patent in an attempt to distinguish U.S. Patent No. 5,127,091 to Boufarah. In a summary of an in-person interview with the examiner on October 25, 1994, the examiner noted with respect to claim 1: “operand width is **variable** and **right adjusted**.” 10/25/1994 Interview Summary at 1 (Chen Decl., Ex. 19) (emphasis added).) The interview summary, which was never disputed, is consistent with the specification’s description of the alleged invention.

Judge Ward and the Federal Circuit have also addressed this issue in connection with the prior Texas litigation that involved U.S. Patent No. 5,784,584 (“’584 patent”), a division of the ’749 patent. The key issue involving the ’584 patent was whether any “operands” in the “instruction register” must be “right justified.” The claim language of the ’584 patent did not expressly recite that instruction operands had to be right justified, so TPL argued -- as it does here – that “right justified operands are a feature of the preferred embodiment.” Ward Order at 22 (Chen Decl., Ex. 2). Judge Ward rejected TPL’s argument and noted that “[t]he specification and prosecution history refer to the fact that operands in the instruction register must be right justified.” *Id.* at 23.[9] Because it was clear that the accused processors in that case did not have right justified

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[9] Judge Ward also construed the term “operand” as “an input to a single operation specified by an instruction that is encoded as part of the instruction where the size of the input can vary.” *Id.* at 24. Judge Ward also noted that TPL “appear[ed] to agree” that the size of the operand in the specification was variable. *Id.* TPL’s previous claim construction briefing in this case, however, argued that the specification discloses “fixed length” operands that need not be right justified, but TPL appears to have abandoned that position – and for good reason. This issue was specifically litigated in the Federal Circuit appeal that TPL lost. *See* ARM Appeal Brief at 23-24 (Chen Decl., Ex. 20) (“**The Specification Confirms The Right Justified Operands Are the <u>Only</u>**

operands, TPL stipulated to a judgment of non-infringement and appealed to the Federal Circuit. *See* TPL Appeal Brief at 23 (Chen Decl., Ex. 21). The Federal Circuit rejected TPL's arguments and summarily affirmed Judge Ward's decision. *See* Fed. Cir. Ruling (Chen Decl., Ex. 22). Following the Federal Circuit's ruling, TPL granted a covenant-not-to-sue to the Plaintiffs herein and the '584 patent was dismissed from this litigation. The issue of whether the operands in the instruction register must be right justified has been correctly settled, and those rulings should not be disturbed.

### *v. Construction of "multiple sequential instructions"*

As explained above, the specification and file history of the '749 patent, as well as rulings from Judge Ward and the Federal Circuit, confirm that the instruction operands must be right justified in the instruction register. This same requirement should also apply to the term "multiple sequential instructions" from the '749 patent:

| Plaintiffs' Construction | TPL's Construction |
|---|---|
| Two or more instructions in sequence, **in which any operands that are present must be right-justified in the instruction register** | Two or more instructions in a program sequence |

Judge Ward's prior construction of the '584 patent construed a closely-related phrase, "instruction groups," as "sets of from 1 to a maximum number of **sequential instructions**, each set being provided to the **instruction register** as a unit and having a boundary, and in which **any operand that is present must be right justified**." Ward Order at 22-23 (Chen Decl., Ex. 2) (emphasis added). An "instruction group" is synonymous with "multiple sequential instructions," as recognized by Judge Ward's construction. For all of the reasons explained above, the requirement that operands be right justified in the instruction register should be incorporated into the construction of this term.

## III. CONCLUSION

For the foregoing reasons, Plaintiffs' constructions should be adopted in their entirety.

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**Embodiment Described.**") (boldface and underlining in original). TPL cannot cite a single instance of any operand in the specification that is not right justified.

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|---|---|
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## ATTESTATION PER GENERAL ORDER 45

I, Kyle D. Chen, am the ECF User whose ID and password are being used to file Plaintiffs' Consolidated Responsive Claim Construction Brief. In compliance with General Order 45, X.B., I hereby attest that the counsel listed above have concurred with this filing.

Dated: January 6, 2012

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