Harold Davis, Jr. (CA Bar No. 235552)
K&L Gates LLP
4 Embarcadero Center, 12th Floor
San Francisco, CA 94111
Telephone: 415-882-8200
Harold.Davis@klgates.com

Attorney for *STMicroelectronics, Inc.*

UNITED STATES BANKRUPTCY COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

In re: TECHNOLOGY PROPERTIES LIMITED LLC, a California corporation, Debtor.	Case No. 13-51589-SLJ-11 Chapter 11 Date: October 2, 2014 Time: 3:00 p.m. Place: United States Bankruptcy Court 280 S. First Street, Room 3099 San Jose, CA 95113 Judge: Honorable Stephen L. Johnson

OBJECTION OF STMICROELECTRONICS, INC. TO DISCLOSURE STATEMENT RE: MOORE MONETIZATION PLAN OF REORGANIZATION DATED AUGUST 28, 2014

STMicroelectronics, Inc. ("STMicro"), a defendant in certain litigation commenced by Technology Properties Limited LLC (the "Debtor") in the United States District Court for the District of Delaware (the "Delaware Fast Logic Litigation"), hereby submits this objection to the Disclosure Statement Re: Moore Monetization Plan of Reorganization Dated August 28, 2014 (the "Moore Disclosure Statement") (Dkt. No. 520.) As set forth below, STMicro believes that the Moore Disclosure Statement fails to provide creditors with "adequate information" as defined in 11 U.S.C. §1125 as it relates to the Delaware Fast Logic Litigation because it fails to adequately warn creditors and interested parties of the potential, significant fee shifting that may occur if the Delaware Fast Logic Litigation is pursued and not dismissed.

I. RELEVANT BACKGROUND

1. On August 28, 2014, counsel for Charles Moore filed a "Monetization Plan of Reorganization" (the "Moore Plan") (Dkt. No. 519) and the Moore Disclosure Statement (Dkt. No. 520.)

2. The Moore Disclosure Statement contains vague references to the existence of litigation in the United States District Court for the District of Delaware concerning the Fast Logic Portfolio of the Debtor but fails to provide any concrete details on the status of the Delaware Fast Logic Litigation, potential recoveries and potential risks of pursuit of such litigation.

3. In the Delaware Fast Logic Litigation, the Debtor continues to assert infringement claims against defendants, Micron Technology Inc., Sandisk Corporation, STMicroelectronics, Inc., STMicroelectronics N.V., Toshiba Corporation, Toshiba America Inc., and Toshiba America Electronic Components Inc. (Case No. 11-cv-770, pending in the U.S.D.C., District of Delaware (the "Delaware Court") alleging patent infringement of select patents in Debtor's Fast Logic Portfolio, which is comprised entirely of now-expired patents. The Debtor continues to claim that STMicro infringed U.S. Patent 5,030,853 (the "853 Patent"). The defendants have vigorously defended the patent infringement claims, and certain defendants also filed counterclaims for non-infringement and invalidity of all asserted patents.

4. On June 17, 2014, the Delaware Court issued its "Markman" ruling which considered and expressly rejected the Debtor's proposed construction of multiple critical claim terms, including the "predetermined factor" term, which is contained within every asserted claim of the 853 patent, attached as Exh. A. The Delaware Court ruled that "predetermined factor" must be defined by "Equation 37, and only that equation." (Exh. A, Markman Op. at 5). Further, the Court ruled that "while the patent discusses the design process, the claims are drawn to the finished product." Id. The Court commented that because Equation 37 includes variables such as "desired rise time" that are not discernible from finished products, "proving infringement using Equation 37 thus appears to present difficult issues." Id.

5. Notably, after the Markman ruling, STMicro provided notice to the Debtor and counsel for Mr. Moore that they will seek to have their legal fees borne by the Debtor in accordance with 35 U.S.C. §285 if the Debtor persists in its pursuit of the Delaware Fast Logic Litigation. Pursuant to 35 U.S.C. §285, a prevailing party in patent litigation may recover its reasonable legal fees from the opposing party in "exceptional cases" such as the present case where a plaintiff persists in pursuing infringement litigation where no reasonable litigant could realistically expect success in its infringement case in light of the Markman ruling.

6. While there has been no final decision in the Delaware Fast Logic Litigation and no award of fees yet, in light of the Markman decision in the case, such an award is a distinct possibility and certainly cannot be ruled out as a risk of litigation.

7. The defendants in the Delaware Fast Logic Litigation have incurred millions of dollars in legal fees and costs to date, and this amount will continue to grow significantly if the Debtor or a trustee acting on its behalf proceeds with the Delaware Fast Logic Litigation.

8. Counsel for STMicro has also advised counsel for Mr. Moore and counsel for the Debtor that it may seek administrative expense treatment for any fees awarded to it as a result of the postpetition damages that the pursuit of the frivolous Delaware Fast Logic Litigation against STMicro causes, including the reasonable legal fees that STMicro is forced to incur. Other defendants in this same litigation are aware of STMicro's strategy and may make similar claims. Certainly, in light of the statutory authorization and the results of the Markman hearing, the fee shifting permitted under 35 U.S.C. §285 is a risk factor that should be disclosed to all creditors voting on any plan that contemplates the pursuit of litigation that will result in not only substantial attorneys' fees for the Debtor's estate as plaintiff but also the possibility of an award of substantial legal fees to separate counsel for multiple defendants.

II. LEGAL STANDARD

9. The purpose of a disclosure statement is to provide "adequate information" for those voting on a plan.

10. As defined in Section 1125 of the Bankruptcy Code, "adequate information" includes "information of a kind, and in sufficient detail, as far as is reasonably practicable in light of the nature and history of the debtor."

11. "[I]n determining whether a disclosure statement provides adequate information, the court shall consider the complexity of the case, the benefit of additional information to creditors and other parties in interest, and the cost of providing additional information ..." 11 U.S.C. § 1125(a)(1). The information in the disclosure statement must enable impaired classes and interest holders to make an informed judgment about the proposed plan and determine whether to vote in favor of or against that plan." Id., *see also In re Phoenix Petroleum Co.*, 278 B.R. 385, 393 (Bankr. E.D. Pa. 2001).

12. Courts determine what constitutes "adequate information" on a case-by-case basis and should take a practical approach as to what is necessary under the unique circumstances of each case. *In re Brotby*, 303 B.R. 177, 193 (B.A.P. 9th Cir. 2003).

13. In assessing the adequacy of information contained within a disclosure statement courts will look generally for the following types of information:

a. the circumstances surrounding the filing of the bankruptcy petition
b. a complete description of the available assets and their value;
c. the debtor's projected future;
d. the source of the information contained within the disclosure statement;
e. a disclaimer;
f. the condition and performance of the debtor while in the process of reorganization;
g. information regarding claims against the estate;
h. a liquidation analysis setting forth the estimated return creditors would receive under Chapter 7;
i. the accounting and valuation methods used to produce financial information in the disclosure statement;

j. information regarding the future management of the debtor, including the amount of compensation to be paid to any insiders, directors and/or officers of the debtor;

k. a summary of the plan;

l. *an estimate of all administrative expenses, including attorneys' fees and accountants' fees*;

m. the collectability of any accounts receivable;

n. *any financial information, valuations or pro forma projections that would be relevant to creditors' determinations of whether to accept or reject the plan*;

o. *information relevant to the risks being taken by the creditors and interest holders*;

p. the actual or projected value that can be obtained from avoidable transfers;

q. *the existence, likelihood and possible success of non-bankruptcy litigation*;

r. the tax consequences of the plan; and

s. the relationship of the debtor with its affiliates.

E.g., *In re Metrocraft Pub. Services. Inc.*, 39 B.R. 567, 568 (Bankr. N.D.Ga. 1984)(emphasis added); *In re Reilly*, 71 B.R. 132, 134 (Bankr. D.Mont. 1987); *see also In re Paific Shores Dev., Inc.*, 2011 WL 778205, 4-6 (Bankr. S.D.Cal. 2011)(citing *Metrocraft* and *Reilly* with approval); *In re Phoenix Petroleum Co.*, 278 B.R. 385, 393 n. 6 (Bankr. E.D.Pa. 2001); *In re Scioto Valley Mortgage Co.*, 88 B.R. 168, 170-71 (Bankr. S.D.Ohio 1988).

III. OBJECTIONS

14. As indicated in the *Metrocraft* and *Pacific Shores* decisions, financial information and projections concerning those assets and potential litigation risks and recoveries are critical information that should be provided to creditors in a disclosure statement to assist creditors and other interested parties in evaluating any proposed plan and its potential impact on that creditor or interested party.

15. The Moore Disclosure Statement fails to provide any details concerning the: (i) status of the Delaware Fast Logic Litigation; (ii) the occurrence and effect of the Markman ruling; (iii) the potential or projected recoveries from the Delaware Fast Logic Litigation; (iv) the projected costs of the Delaware Fast Logic Litigation; and (v) the risk of potential fee shifting in the Delaware Fast Logic Litigation and the classification and impact that the award of fees could have on the Moore Plan.

16. As such, the Moore Disclosure Statement fails to provide creditors and parties in interest with enough information about the Delaware Fast Logic Litigation to make an informed decision about the potential impact of that litigation on the Moore Plan and the potential recoveries and substantial claims that may arise from such litigation.

IV. CONCLUSION

For all of the foregoing reasons, the Moore Disclosure Statement fails to provide adequate information, within the meaning 11 U.S.C. §1125(a)(1) and should not be approved without further disclosure about the Markman decision, projections on the costs and expected recoveries and claims/risk of substantial fee shifting concerning the Delaware Fast Logic Litigation.

DATED this 25th day of September, 2014.

K&L GATES LLP

By: /s/ *Harold H. Davis, Jr.*

Harold H. Davis, Jr.
Counsel for STMicroelectronics, Inc.

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

HSM Portfolio LLC and **Technology Properties Limited LLC,** Plaintiffs, v. **Fujitsu Limited, et al.,** Defendants.	Civil Action No. 11-770-RGA

MEMORANDUM OPINION

Brian E. Farnan, Esq., Farnan LLP, Wilmington, DE; Michael J. Farnan, Esq., Farnan LLP, Wilmington, DE; Jeffrey R. Bragalone, Esq. (argued), Bragalone Conroy PC, Dallas, TX; Daniel F. Olejko, Esq. (argued), Bragalone Conroy PC, Dallas, TX; Monte M. Bond, Esq., Bragalone Conroy PC, Dallas, TX, attorneys for Plaintiffs.

Frederick L. Cottrell, III, Esq., Richards, Layton & Finger, PA, Wilmington, DE; Jared Bobrow, Esq. (argued), Weil, Gotshal & Manges LLP, Silicon Valley, CA; Jason Lang, Esq. (argued), Weil, Gotshal & Manges LLP, Silicon Valley, CA, attorneys for Defendant Micron Technology Inc.

David Ellis Moore, Esq., Potter Anderson & Corroon, LLP, Wilmington, DE; Michael Hawes, Esq. (argued), Baker Botts, Houston, TX; Scott F. Partridge, Esq., Baker Botts, Houston, TX, attorneys for Defendant Toshiba Corporation.

David Ellis Moore, Esq., Potter Anderson & Corroon, LLP, Wilmington, DE; Jim Brogan, Esq. (argued), Cooley LLP, Palo Alto, CA; Drew Koning, Esq., Cooley LLP, San Diego, CA, attorneys for Defendant Qualcomm Incorporated.

Jeffrey L. Moyer, Esq., Richards, Layton & Finger, PA, Wilmington, DE; Kevin R. Casey, Esq., Stradley Ronon Stevens & Young, LLP, Malvern, PA; Keith R. Dutill, Esq., Stradley Ronon Stevens & Young, LLP, Malvern, PA, attorneys for Defendants STMicroelectronics Inc. and STMicroelectronics, N.V.

Michael J. Flynn, Esq., Morris, Nichols, Arsht & Tunnell LLP, Wilmington, DE; Gregory L. Lippetz, Esq., Jones Day, Silicon Valley, CA; Kyle T. Barrett, Esq., Jones Day, Silicon Valley, CA, attorneys for Defendant Sandisk Corporation.

EXHIBIT A

Mary B. Graham, Esq., Morris, Nichols, Arsht & Tunnell LLP, Wilmington, DE; Karl J. Kramer, Esq., Morrison & Foerster LLP, Palo Alto, CA, attorneys for Defendants Fujitsu Limited, Fujitsu America Inc., and Fujitsu Semiconductor America Inc.

Mary B. Graham, Esq., Morris, Nichols, Arsht & Tunnell LLP, Wilmington, DE, attorney for Defendant Zoran Corporation.

June 17, 2014

EXHIBIT A

ANDREWS, U.S. District Judge:

Pending before this Court is the issue of claim construction of eleven disputed terms found in U.S. Patent No. 5,030,853, U.S. Patent No. 5,391,949, U.S. Patent No. 5,247,212, and U.S. Patent No. 5,001,367.

I. BACKGROUND

On September 1, 2011, Plaintiffs HSM Portfolio LLC and Technology Properties Limited LLC filed a patent infringement action against eighteen Defendant Groups, eight of which remain in the case. The Court has considered the Parties' Joint Claim Construction Brief (D.I. 677) and heard oral argument on June 5, 2014. (D.I. 698).

II. LEGAL STANDARD

"It is a bedrock principle of patent law that the claims of a patent define the invention to which the patentee is entitled the right to exclude." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal quotation marks omitted). "'[T]here is no magic formula or catechism for conducting claim construction.' Instead, the court is free to attach the appropriate weight to appropriate sources 'in light of the statutes and policies that inform patent law.'" *SoftView LLC v. Apple Inc.*, 2013 WL 4758195, at *1 (D. Del. Sept. 4, 2013) (quoting *Phillips*, 415 F.3d at 1324). When construing patent claims, a matter of law, a court considers the literal language of the claim, the patent specification, and the prosecution history. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 977-80 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996). Of these sources, "the specification is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term." *Phillips*, 415 F.3d at 1315 (internal quotations and citations omitted).

Furthermore, "the words of a claim are generally given their ordinary and customary

meaning . . . [which is] the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e. as of the effective filing date of the patent application." *Phillips*, 415 F.3d at 1312-13 (internal citations and quotation marks omitted). "[T]he ordinary meaning of a claim term is its meaning to [an] ordinary artisan after reading the entire patent." *Id.* at 1321 (internal quotation marks omitted). "In some cases, the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words." *Id.* at 1314 (internal citations omitted).

A court may consider extrinsic evidence, which "consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises," in order to assist the court in understanding the underlying technology, the meaning of terms to one skilled in the art and how the invention works. *Id.* at 1317-19 (internal quotation marks and citations omitted). However, extrinsic evidence is less reliable and less useful in claim construction than the patent and its prosecution history. *Id.*

Finally, "[a] claim construction is persuasive, not because it follows a certain rule, but because it defines terms in the context of the whole patent." *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998). It follows that "a claim interpretation that would exclude the inventor's device is rarely the correct interpretation." *Osram GmbH v. Int'l Trade Comm'n*, 505 F.3d 1351, 1358 (Fed. Cir. 2007) (internal quotation marks and citation omitted).

III. CONSTRUCTION OF DISPUTED TERMS

A. Terms from Claims 1 and 3 of the '853 Patent

1. "the N-channel field effect transistor in each inverter stage having a channel width which is less than a [predetermined factor] times the width of the N-channel of the immediately preceding inverter stage"

   a. *Plaintiffs' proposed construction*: "the N-channel field effect transistor in each inverter stage after the first inverter stage having a channel width that is greater than the channel width of the immediately preceding inverter stage but less than K times the channel width of the N-channel field effect transistor of the immediately preceding inverter stage," where K is "a defined value that governs the maximum increase in channel width of the N-channel transistors in succeeding inverter stages such that the capacitive load can be driven with a specific signal rise time"

   b. *Defendants' proposed construction*: [predetermined factor] "a value calculated in advance of selecting the widths and lengths of the complementary FETs in each inverter stage, the value calculated using Equation (37) in the specification"

   c. *Court's Construction*: "the N-channel field effect transistor in each inverter stage after the first inverter stage having a channel width that is greater than the channel width of the immediately preceding inverter stage but less than K times the channel width of the N-channel field effect transistor of the immediately preceding inverter stage, where K is calculated using Equation (37) in the specification"

2. "wherein the N-channel field effect transistor in the first inverter stage has a channel width which is less than said [predetermined factor] times the width of the at least one N-channel field effect transistor in the logic gate"

   a. *Plaintiffs' proposed construction*: "wherein the N-channel field effect transistor in the first inverter stage has a channel width which is greater than the channel width of the at least one N-channel field effect transistor in the logic gate but less than K times the channel width of the at least one N-channel field effect transistor in the logic gate," where K is "a defined value that governs the maximum increase in channel width of the N-channel transistors in succeeding inverter stages such that the capacitive load can be driven with a specific signal rise time"

   b. *Defendants' proposed construction*: [predetermined factor] "a value calculated in advance of selecting the widths and lengths of the complementary FETs in each inverter stage, the value calculated using Equation (37) in the specification"

   c. *Court's Construction*: "wherein the N-channel field effect transistor in the first inverter stage has a channel width which is greater than the channel width of the at least one N-channel field effect transistor in the logic gate but less

EXHIBIT A

> than K times the channel width of the at least one N-channel field effect transistor in the logic gate, where K is calculated using Equation (37) in the specification"

The parties agree that these two terms rise and fall together. The parties also agree that "predetermined factor" refers to K, as described in the specification. The main dispute is whether K must be calculated according to Equation 37 or whether there are other ways to calculate K. Defendants point out that Equation 37 is the only equation which is solved for K, and the specification describes using Equation 37, and only that equation, to determine K. Additionally, during prosecution the Examiner stated that it was his belief that the "predetermined factor" referred to K, as calculated using Equation 37.

Plaintiffs argue that K should not be limited to just using Equation 37, because it would violate the doctrine of claim differentiation. Dependent claim 12 defines "predetermined value" as K, calculated according to Equation 37. Therefore, if the Court were to import Equation 37 into the construction of "predetermined value," Plaintiffs argue that the doctrine of claim differentiation would be violated, making claim 12 meaningless. Plaintiffs also point out that K is used in multiple equations in the specification, and that the construction should allow for using any of those equations. Yet at oral argument, Plaintiffs stated that no matter which formula was used to calculate K, the result would always be the same. (D.I. 698 at 15:16-20). This begs the question of why it matters which formula one uses in the claim construction if the result is always the same.

The answer, as it became clear at oral argument, is that Equation 37 uses a variable, T_{rise}, which is the desired rise time of the circuit. Actual circuits do not have a desired rise time; they have an actual rise time. Proving infringement using Equation 37 thus appears to present difficult issues. Would one substitute the actual rise time for the desired rise time, or would one need

some evidence of the desired rise time? It seems farfetched to rely on a designer's intent to prove infringement. There is no such thing as attempted patent infringement; one either infringes or does not.

How easy it would be to determine infringement using Equation 37 is irrelevant at this stage. There is no canon of claim construction that prefers an "easy to prove infringement" construction. The presence of T_{rise} in Equation 37 supports one of Plaintiffs' arguments against using only Equation 37, and with Defendants' proposed construction in general. Defendants' proposed construction attempts to incorporate temporal process limitations into an apparatus claim, which Plaintiffs argue is improper. The Court agrees. While the patent itself discusses the design process, the claims are drawn to the finished product. The patentee did not claim a process of making a chip, but the chip itself. The fact that the specification describes one method of ending up at the final product does not limit the claims to using only that method.

The intrinsic evidence is that the patentee intended Equation 37, and only that equation, to define "predetermined factor." ('853 patent at 3:22-30) ("In particular, the factor, referred to as "K" [] is defined by: [Equation 37]"). The specification makes clear that when designing a chip according to the invention, the "predetermined factor" is calculated after determining the width of the N-channel in the last stage and before determining the maximum width of the N-channel in the first stage. ('853 patent at 19:30-40). However, a statement of how to design the chip does not limit the claims to that design process. To prevent any further incorporation of process limitations into this claim term, the Court adopts the language "after the first inverter stage" from Plaintiffs' proposed construction to make clear that the first inverter stage does not have a preceding inverter stage.

3. "[the P-channel field effect transistor in each inverter stage having a channel

which is wider than the channel of the corresponding N-channel field effect transistor of each inverter stage by η], the ratio of electron mobility in the N-channel field effect transistors to hole mobility in the P-channel field effect transistors"

a. *Plaintiffs' proposed construction*: "the corresponding P-channel and N-channel field effect transistors in each inverter stage are sized such that the inverter transfer function of each inverter stage is symmetrical"

b. *Defendants' proposed construction*: [bracketed portion]"The P-channel field effect transistor in each inverter stage having a channel width that is equal to the corresponding N-channel field effect transistor width multiplied by η, that provides a symmetrical voltage transfer function for each stage"

c. *Court's Construction*: "the P-channel field effect transistor in each inverter stage having a channel which is wider than the channel of the corresponding N-channel field effect transistor of each inverter stage by a factor of η, the ratio of electron mobility in the N-channel field effect transistors to hole mobility in the P-channel field effect transistors, such that the voltage transfer function of each inverter stage is symmetrical"

Both parties agree that the P-channel width must by approximately equal to the N-channel width times η, and that this results in a symmetrical voltage transfer function. Plaintiffs oppose Defendants' proposed construction because it inserts the term "equal to," which Plaintiffs contend is too limiting. Plaintiffs contend that by using "equal to," the P-channel must be exactly equal to the N-channel width multiplied by η, but that the person of ordinary skill would understand that there is some margin of error which would still be within the claims. What that margin of error is, Plaintiffs could not say, but posit that their expert, and therefore a person of ordinary skill, would understand what falls within the claim. The Court's construction attempts to clarify that the N-channel width is multiplied by η, rather than added to it,[1] while staying as true to the claim language as possible. Additionally, as neither side disputes the symmetrical voltage transfer function, that language has been added to the construction.

[1] The parties at oral argument agreed that η played this role.

B. Terms from Claims 1-2 and 8-11 of the '949 Patent

4. "[A Field Effect Transistor (FET) Differential Latching Inverter (DLI) circuit] for sensing signals on first and second bit lines of a memory"

   a. *Plaintiffs' proposed construction*: No construction necessary as the preamble does not limit the body of the claim.

   b. *Defendants' proposed construction*: Limiting preamble. "Memory" should be accorded its plain and ordinary meaning. "First and second bit lines" should be accorded meaning as discussed in next claim term.

   c. *Court's Construction*: The preamble is not limiting.

5. "first and second bit lines of a memory" (Preamble) "first bit line" / "second bit line" (Body)

   a. *Plaintiffs' proposed construction*: No construction necessary as the preamble does not limit the body of the claim. "Bit line" should be accorded its plain and ordinary meaning. Alternatively, "bit line" should be construed as "signal lines for transmitting binary values."

   b. *Defendants' proposed construction*: "a pair of different conductive lines in a memory cell array that are connected to memory cells for transferring the stored value of a selected memory cell out of the memory cell array"

   c. *Court's Construction*: The term "first bit line" and "second bit line" in the body of the claim are construed as "a pair of different conductive lines in a memory cell array that are connected to memory cells for transferring the stored value of a selected memory cell out of the memory cell array."

There are two intertwined disputes in these terms. The first is whether the preamble limits the claims. The second is the construction of "bit lines." The preamble of claim 1 states that the circuit is "for sensing signals on first and second bit lines of a memory." ('949 patent claim 1). On its own, this is intended use language that would not limit the claims. *See Marrin v. Griffin*, 599 F.3d 1290, 1294 (Fed. Cir. 2010). Based on the preamble alone, the claims do not require that the circuit be used for sensing memory signals. However, the term "bit lines" are used in the body of the claim and would ordinarily be understood there to be limitations.

Plaintiffs argue that even though the term "bit line" is used in the body of the claim, it is

not a limitation because it is merely a reference point for the placement of the circuit. (D.I. 677 at p. 42). The claim is drawn to a DLI circuit, and not the surrounding circuitry. Therefore Plaintiffs assert that since the bit lines are connected to the circuit, the bit lines are part of the surrounding circuitry and not part of the claimed DLI circuit. In support of this assertion, Plaintiffs cite to *C.R. Bard, Inc. v. M3 Sys., Inc.*, 157 F.3d 1340, 1350 (Fed. Cir. 1998), and *Vaupel Textilmaschinen KG v. Meccanica Euro Italia SPA*, 944 F.2d 870, 880 (Fed. Cir. 1991), where the Federal Circuit held that language in the body of the claim, which referred to a non-limiting preamble, was not a limitation because it merely provided a physical reference point.

I agree that in this instance the preamble does not limit the claims. The preamble is not necessary to give meaning to the claims. It merely states a preferred use. During prosecution, the Examiner stated that the invention could be used as a Schmitt Trigger or a threshold detector. (D.I. 676-13 at 3). While this statement in and of itself is not intrinsic evidence, it is extrinsic evidence that one of ordinary skill in the art would recognize that the claimed invention had utility outside of a memory circuit. Therefore I do not find that the preamble is limiting.

However, I disagree that the term "bit line" in the body of the claim is not a limitation. In *C.R. Bard* the claim at issue was drawn to a biopsy needle. 157 F.3d at 1348-49. The preamble stated that it was "for use with a tissue sampling device having a housing with a forward end, a first slide mounted for longitudinal motion within said housing, and a second slide mounted for longitudinal motion within said housing." *Id.* The body of the claim included four limitations: a hollow needle, a second needle, a first head, and a second head. *Id.* at 1349. Within the first head and second head limitations, the claim included the following language: "for coupling said hollow first needle to said first slide for longitudinal motion both toward and away from said forward end of said housing." *Id.* The Court held that the claim did not require a housing because

EXHIBIT A

the preamble was not limiting, as it merely "provide[d] reference points in the gun that aid in defining the needles as set forth in the body of the claim." *Id.*

Similarly, in *Vaupel*, the claim was drawn to an improvement in a weaving machine having a "breast plate." 944 F.2d at 872-73. Even though the body of the claim contained the language "ahead of the breast plate," and "to said breast plate," those references were not limitations because "they indicate[d] a reference point to fix the direction of movement of the woven fabric from the loom." *Id.* at 880. This case is unlike *C.R. Bard* and *Vaupel*. The claim does not use "bit lines" as a reference point. The claim requires that the bit lines are present and connected to the circuit. '949 patent, claim 1 ("the first bit line being connected to the first input of said first inverter and the second bit line being connected to the first input of said second inverter"). In fact, the structure of the claim presents the first and second bit lines as a distinct limitation, not as reference points. Therefore I find that "first bit line" and "second bit line" are limitations.

Having found that the term "bit line" in the body of the claim is a limitation, it must be construed. Plaintiffs argue that "bit line" has a plain and ordinary meaning, or, alternatively, that it refers to "signal lines for transmitting binary values." Defendants argue that Plaintiffs' proposed construction of "bit line" is too broad. The specification refers both to "word lines" and "bit lines." ('949 patent at 1:25-40). Defendants argue that Plaintiffs' proposed construction would cover both "word lines" and "bit lines," and would render the distinction meaningless. I agree. The specification makes multiple references to "bit lines," always in the context of memory. (*See, e.g.*, '949 patent at 5:25-33). Because Plaintiffs' proposed construction is too broad, I adopt Defendants' proposed construction.

6. "an inverter transfer function… which is identical when said first and second

inverters turn on and turn off"

a. *Plaintiffs' proposed construction*: Plain and ordinary meaning. Alternatively, "each inverter has a transfer function which is the same when turning on and when turning off."

b. *Defendants' proposed construction*: "identical when the input voltage to the respective inverter moves from the second reference voltage to the first reference voltage and when the input voltage moves from the first reference voltage to the second reference voltage"

c. *Court's Construction*: "each inverter has a transfer function which is identical when the inverter turns on (i.e. moves from 5 volts to 0 volts input voltage) and when the inverter turns off (i.e. moves from 0 volts to 5 volts input voltage)"

The parties agree that this term means "free of hysteresis," but that such a construction would not be helpful to the jury. Plaintiffs' main criticism of Defendants' proposed construction is that it reads a functional limitation into an apparatus claim by requiring that the device be used. (D.I. 677 at p. 48). I do not agree that Defendants' proposed construction requires that the device be used. However, neither proposed construction is particularly helpful to the jury. Interestingly, both parties cite to the very same prosecution history for support of their respective constructions. There, the applicant stated that, "Support for this recitation may be found in Figure 2 of the specification, which shows an inverter transfer function for skewed inverts 11, 11' which is identical when the inverter turns on (i.e. moves from 5 volts to 0 volts input voltage) and when the inverter turns off (i.e. moves from 0 volts to 5 volts input voltage)." (D.I. 676-8 at 4). I therefore construe the term as closely to this description as possible.

7. "the outputs of said first and second complementary FET inverters producing output signals for said DLI circuit"

a. *Plaintiffs' proposed construction*: "each of the first and second complementary FET inverters is capable of producing an output signal for said DLI circuit"

b. *Defendants' proposed construction*: "each of the first and second

complementary FET inverters produces a separate signal for output from the DLI circuit"

c. *Court's Construction*: "each of the first and second complementary FET inverters is capable of producing a separate signal for output from the DLI circuit"

There are two disputes regarding this term. The first is whether this limitation requires that the circuit actually produces the claimed output signals or whether the circuit only need be capable of producing the output signals. The claim at issue is inelegantly written. It appears to require the production of signals, which cannot be the case for an apparatus. As Plaintiffs argue, an apparatus claim covers what the apparatus is, not what it does. I agree that this term does not require the actual production of output signals. Therefore, I will construe it only to require the capability to produce output signals.

The second dispute is whether the output signals are "for" the circuit or whether they are "from" the circuit. It is clear that "outputs" refers to a signal that emanates "from" a source. Using the word "from" does not rewrite the term "for," as Plaintiffs argue. It construes the term. Furthermore, whether there is circuitry downstream from the output does not transform the outputs into something else. The Court will thus clarify what is meant by the disputed claim language.

C. Terms from Claims 22 and 23 of the '212 Patent

8. "for receiving [a logic input signal/a clock input signal]"

a. *Plaintiffs' proposed construction*: Plain and ordinary meaning. Alternatively, "capable of receiving a voltage comprising a binary value" / "capable of receiving a voltage comprising a periodic timing signal."

b. *Defendants' proposed construction*: [a logic input signal] "a signal input to the logic cell" / [a clock input signal] "a periodic signal with a constant frequency used for synchronization"

c. *Court's Construction*: [a logic input signal] "a signal input to the logic cell" /

EXHIBIT A

> [a clock input signal] "a periodic signal with a constant frequency used for synchronization"

While the parties briefly dispute the "logic input signal" language, the main dispute is in regard to the definition of "clock input signal."[2] Plaintiffs argue that a "clock input signal" refers to periodic signals sent by a clock circuit. Defendants agree. However, the parties dispute if periodic signals must have a constant frequency. Plaintiffs argue that there need not be a constant frequency, and cite to the IEEE Standard Dictionary of Electrical and Electronics Terms (4th ed. 1988), which defines a "clock" as "device that generates periodic signals used for synchronization." (D.I. 677-5 at 155-56). Additionally, Plaintiffs cite to the '853 patent as extrinsic evidence that clock signals can be asynchronous. ('853 patent at 27:29-41).

Defendants argue that a clock signal must have a constant frequency. They cite to the ACADEMIC PRESS DICTIONARY OF SCIENCE AND TECHNOLOGY 447 (1992), which defines "clock pulses" as "a train of signals in which the separation between pulses is constant and which serves to synchronize information transfer among computer components." (D.I. 677-14). Additionally, Defendants point to THE PENGUIN DICTIONARY OF ELECTRONICS 74 (2nd ed. 1988), which contains the following explanation for the term "clock":

> An electronic device that generates periodic signals that are used to synchronize operations in a *computer or to monitor and measure properties of the circuits involved. The master frequency generated by a clock is the *clock frequency*. The regular pulses applied to the elements of a *logic circuit to effect logical operations are called *clock pulses*. The use of clock pulses in order to drive any particular electronic circuit, device, or apparatus is knows as *clocking* and the driven circuit, etc., is described as *clocked* or *synchronous*.

(D.I. 677-15).

The extrinsic evidence cited by both parties is complementary. Nothing in the ACADEMIC

[2] For an explanation of the construction of "logic input signals," see term 11, *infra*.

PRESS DICTIONARY OF SCIENCE AND TECHNOLOGY 447 (1992) or THE PENGUIN DICTIONARY OF ELECTRONICS 74 (2nd ed. 1988) is inconsistent with the definition of clock from the IEEE Standard Dictionary of Electrical and Electronics Terms (4th ed. 1988). The only evidence which arguably supports Plaintiffs' non-constant frequency theorem is the '853 patent. A section of the '853 patent is labeled "Asynchronous Clock Pulse Generation." ('853 patent at 27:29). The patent states that the invention "may also be used to construct an asynchronous clock pulse generator." ('853 patent at 27:30-34). However, there is no discussion of how an asynchronous clock pulse generator relates to the term "clock signal." Because the evidence makes clear that clock signals must have a constant frequency, I adopt Defendants' construction.

D. Terms from Claim 1 of the '367 Patent

9. "A field effect transistor (FET) logic circuit comprising"

   a. *Plaintiffs' proposed construction*: No construction necessary, as this preamble language is defined by the body of the claim.

   b. *Defendants' proposed construction*: Limiting preamble. "Logic circuit" means "an electronic circuit that operates on digital signals in accordance with a logic function."

   c. *Court's Construction*: "an electronic circuit that is capable of operating on digital signals in accordance with a logic function"

Plaintiffs argue that Defendants' construction adds a functional limitation to an apparatus claim, and is therefore improper. Whether the apparatus infringed would depend on what function it was performing. Plaintiffs argue that by limiting the circuit to a logic circuit, the circuit would have to be used to perform a logic operation in order to infringe. Defendants dispute this assertion, stating that, "[a]n AND logic circuit exists regardless of use because an AND circuit is structured to execute the AND function." (D.I. 677 at p. 9). Furthermore, Defendants point out that because the dependent claims limit the logic circuit to a particular type,

i.e., an AND or OR circuit, it would be nonsensical for the independent claim to be anything but a logic circuit, especially when that language is in the claim.

I agree with Defendants that the claim must be limited to a logic circuit. I do not agree that, in order to infringe, the circuit must be used to perform a logic operation. It must be capable of performing a logic operation. Defendants imply that there is no difference. (D.I. 677 at p. 9). If that is so, it does not matter whether the construction is that the circuit is used in accordance with a logic function, or that it is capable of being used in accordance with a logic function. Thus, I do not understand Defendants to object to the "capable of" language.

10. "the product of the carrier mobility and the ratio of channel width to length of the inverter FET of said first conductivity type being [substantially greater than] the product of the carrier mobility and the ratio of channel width to length of the inverter FET of said second conductivity type"

    a. *Plaintiffs' proposed construction*: "the complementary FET inverter having a skewed transfer function toward the first potential level"

    b. *Defendants' proposed construction*: [substantially greater than] "sufficiently greater (i.e., at least about four times) to create an inverter transfer function that is dramatically skewed"

    c. *Court's Construction*: "the product of the carrier mobility and the ratio of channel width to length of the inverter FET of said first conductivity type being substantially greater than the product of the carrier mobility and the ratio of channel width to length of the inverter FET of said second conductivity type, resulting in an inverter transfer function that is skewed"

The parties agree that the inverter function must be skewed. They disagree as to how skewed. Defendants cherry pick a preferred embodiment, *i.e.*, at least about four times, which would completely negate claim 6, a dependent claim. Plaintiffs' proposed construction entirely reads out the term "substantially greater than." The Court's construction stays true to the claim language while making clear that the inverter function must be skewed. The term "substantially" does not need construction as it is a commonly used term with which all jurors are familiar.

EXHIBIT A

11. "for receiving [logic input signals]"

a. *Plaintiffs' proposed construction*: "capable of receiving a voltage comprising a binary value"

b. *Defendants' proposed construction*: [logic input signals] "signal inputs to the logic circuit"

c. *Court's Construction*: [logic input signals] "signal inputs to the logic circuit"

Defendants' proposed construction seeks to clarify that the "logic input signals" are signals input to a logic circuit. Plaintiffs argue that "logic input signals" means signals sent by the logic circuit. In support of this, Plaintiffs cite to the abstract of the patent, which describes that the "FET logic circuit includes a driving stage having a plurality of parallel FETs of a first conductivity type for receiving logic input signals." ('367 patent at Abstract). It is entirely unclear how a signal which is received by a logic circuit could refer to a signal sent by the very same logic circuit. I therefore adopt Defendants' proposed construction.

IV. CONCLUSION

Within five days the parties should submit a proposed order, consistent with this opinion, suitable for submission to the jury.

EXHIBIT A