Reexam

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(Also referred to as FORM PTO-1465)

71338 U.S. PTO

REQUEST FOR *EX PARTE* REEXAMINATION TRANSMITTAL FORM

71338 U.S. PTO 90008237

09/21/06

Address to:
Mail Stop *Ex Parte* Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

09/21/06

Attorney Docket No.: 069974-0160

Date: September 21, 2006

1. [X] This is a request for *ex parte* reexamination pursuant to 37 CFR 1.510 of patent number 5,809,336 issued September 15, 1998. The request is made by:

   [ ] patent owner. [X] third party requester.

2. [X] The name and address of the person requesting reexamination is:

   Matthew A. Smith, on behalf of NEC Electronics America, Inc.
   Foley & Lardner LLP
   3000 K Street, NW, Suite 500, Washington, DC 20007

3. [ ] a. A check in the amount of $_____ is enclosed to cover the reexamination fee, 37 CFR 1.20(c)(1);

   [ ] b. The Director is hereby authorized to charge the fee as set forth in 37 CFR 1.20(c)(1) to Deposit Account No. _____ (submit duplicative copy for fee processing); or

   [X] c. Payment by credit card. Form PTO-2038 is attached.

4. [ ] Any refund should be made by [ ] check or [ ] credit to Deposit Account No._____. 37 CFR 1.26(c). If payment is made by credit card, refund must be to credit card account.

5. [X] A copy of the patent to be reexamined having a double column format on one side of a separate paper is enclosed. 37 CFR 1.510(b)(4)

6. [ ] CD-ROM or CD-R in duplicate, Computer Program (Appendix) or large table
   [ ] Landscape Table on CD

7. [ ] Nucleotide and/or Amino Acid Sequence Submission
   If applicable, items a. – c. are required.

   a. [ ] Computer Readable Form (CRF)
   b. Specification Sequence Listing on:

      i. [ ] CD-ROM (2 copies) or CD-R (2 copies); **or**
      ii. [ ] paper

   c. [ ] Statements verifying identity of above copies

8. [ ] A copy of any disclaimer, certificate of correction or reexamination certificate issued in the patent is included.

9. [X] Reexamination of claim(s) 1 - 10 is requested.

10. [X] A copy of every patent or printed publication relied upon is submitted herewith including a listing thereof on Form PTO/SB/08, PTO-1449, or equivalent.

09/26/2006 INGDUGA 00000003 90008237
01 FC:1812 2520.00 OP

11. [ ] An English language translation of all necessary and pertinent non-English language patents and/or printed publications is included.

12. [X] The attached detailed request includes at least the following items:

a. A statement identifying each substantial new question of patentability based on prior patents and printed publications. 37 CFR 1.510(b)(1)
b. An identification of every claim for which reexamination is requested, and a detailed explanation of the pertinency and manner of applying the cited art to every claim for which reexamination is requested. 37 CFR 1.510(b)(2)

13. [ ] A proposed amendment is included (only where the patent owner is the requester). 37 CFR 1.510(e)

14. [X] a. It is certified that a copy of this request (if filed by other than the patent owner) has been served in its entirety on the patent owner as provided in 37 CFR 1.33(c).
The name and address of the party served and the date of service are:

Mr. Drew S. Hamilton

Knobbe, Martens, Olson & Bear, LLP

550 W C St. Suite 120, San Diego, CA 92101

Date of Service: September 21, 2006; or

[ ] b. A duplicate copy is enclosed since service on patent owner was not possible.

15. Correspondence Address: Direct all communication about the reexamination to:

[X] The address associated with Customer Number: 22428

OR

[ ] Firm or Individual Name

Address

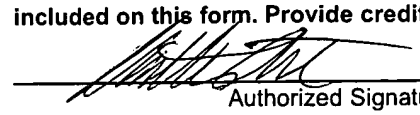
City	State	Zip
Country		
Telephone	Email	

16. [X] The patent is currently the subject of the following concurrent proceeding(s):

[ ] a. Copending reissue Application No. _____.
[ ] b. Copending reexamination Control No. _____.
[ ] c. Copending Interference No. _____.
[X] d. Copending litigation styled:

Technology Properties Limited, Inc. v. Fujitsu Limited et al., Case No. 2:05-cv-00494-TJW, Federal District Court for the Eastern District of Texas, Marshall Division

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.



Authorized Signature

Sept. 21, 2006
Date

Matthew A. Smith
Typed/Printed Name

49,003
Registration No.

[ ] For Patent Owner Requester
[X] For Third Party Requester

ATTORNEY DOCKET NO. 069974-0160

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Caption: In re Reexamination of Charles MOORE, *et al.*

Title: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

Pat. No.: 5,809,336

Issue Date: Sept. 15, 1998

Examiner: unassigned

Art Unit: unassigned

REQUEST FOR *EX PARTE* REEXAMINATION UNDER 37 C.F.R. §1.510

Mail Stop Ex Parte Reexamination
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Enclosed please find a request for *ex parte* reexamination of U.S. Pat. No. 5,809,336 ("the '336 patent") under 35 U.S.C. § 302 and 37 C.F.R. § 1.510, together with the fee required under 37 C.F.R. § 1.20(c)(1). The request is filed on behalf of NEC Electronics America, Inc. A detailed presentation of the prior art in light of the claims is attached as Appendix A.

I. STATEMENT POINTING OUT EACH SUBSTANTIAL NEW QUESTION OF PATENTABILITY

The following Substantial New Questions of Patentability are presented and summarized briefly below. These questions are presented in more detail in Appendix A.

A. **Are claims 1, 3, and 5-10 of U.S. Pat. No. 5,809,336 anticipated under 35 U.S.C. § 102(b) by or Obvious under 35 U.S.C. § 103(a) Over Ledzius, *et al.*, U.S. Pat. No. 4,691,124?**

U.S. Pat. No. 4,691,124 to Ledzius, *et al.* (Exhibit 2) is prior art under 35 U.S.C. §102 (b), and was not cited during the original prosecution of the of the '336 patent. The disclosure of Ledzius, *et al.* describes all elements of claims 1, 3 and 5-10 as described below. In particular, the Ledzius, *et al.* reference discloses a feature considered by the Applicants to be "crucial" to the patentability of the claims: a free-running ring oscillator on an integrated circuit substrate. *See* Exhibit 10, p. 5. No other prior art reference of record in the original prosecution describes this feature. The Requester thus believes that there is a substantial likelihood that a reasonable Examiner would have considered the teachings of the Ledzius, *et al.* reference to be important in deciding whether the claims of the '336 patent were patentable.

B. **Are claims 1-10 of U.S. Pat. No. 5,809,336 obvious under 35 U.S.C. § 103(a) over the Mead & Conway textbook in view of in view of IEEE Std 796-1983?**

Like the Ledzius, *et al.* reference, the 1980 Mead & Conway textbook "Introduction to VLSI Systems" (Exhibit 18) describes the use of free-running ring oscillators to clock microprocessors. Mead & Conway further describe the use of a microprocessor with a system bus and system bus interface. The IEEE Std. 796-1983 provides a standard system bus and system bus interface that were designed for use with multiple devices of different types, and which disclose the input / output elements of claims 1-10. Both references were published more than one year prior to the earliest possible benefit date of the '336 patent and are prior art under 35 U.S.C. § 102(b). Neither reference was cited to the office during original prosecution. Since no reference before the Examiner during original prosecution taught the use of a free-running ring oscillator as a system clock or the use of a system bus interface, Requester respectfully submits that there is a substantial likelihood that a reasonable Examiner would have considered

the teachings of the Mead & Conway textbook and the IEEE Std. 796-1983 reference to be important in deciding whether the claims of the '336 patent were patentable.

C. **Are claims 1-10 of U.S. Pat. No. 5,809,336 obvious under 35 U.S.C. § 103(a) over Kato, U.S. Pat. No. 4,766,567 in view of Crosby, *et al.*, U.S. Pat. No. 4,750,111?**

Like the Ledzius, *et al.* reference, U.S. Pat. No. 4,766,567 to Kato (Exhibit 4) describes a microprocessor circuit with a free-running on-chip ring oscillator. U.S. Patent No. 4,750,111 to Crosby, *et al.* describes a processor bus and externally clocked interface meeting all the input / output interface limitations of claims 1-10. The interface can be used with a wide variety of processors running at different speeds and external memory. Kato is prior art at least under 35 U.S.C. § 102(e), Crosby *et al.* is prior art under 35 U.S.C. § 102(b). Since no reference before the Examiner during original prosecution disclosed a free-running on-chip ring oscillator or a synchronous processor bus with external memory, Requester believes that there is a substantial likelihood that a reasonable Examiner would have considered the teachings of the Kato and Crosby, *et al.* references to be important in deciding whether the claims of the '336 patent were patentable.

II. AN IDENTIFICATION OF EVERY CLAIM FOR WHICH REEXAMINATION IS REQUESTED.

Reexamination is requested for all claims 1-10.

III. MANNER OF APPLYING THE CITED PRIOR ART TO EVERY CLAIM FOR WHICH REEXAMINATION IS REQUESTED.

Please see attached Appendix A, below, "Manner of Applying the Cited Prior Art to Every Claim for Which Reexamination is Requested."

IV. A COPY OF EVERY PATENT OR PRINTED PUBLICATION RELIED UPON OR REFERRED TO.

Every patent or printed publication relied upon or referred to is attached as follows and is also cited on the attached modified Form PTO/SB/42:

EXHIBIT NO.	REFERENCE
EXHIBIT 1	Moore, *et al.*, U.S. Pat. No. 5,809,336.
EXHIBIT 2	Ledzius, *et. al* , U.S. Pat. No. 4,691,124.
EXHIBIT 3	Crosby, *et al.*, U.S. Pat. No. 4,750,111.
EXHIBIT 4	Kato, U.S. Pat. No. 4,766,567.
EXHIBIT 5	TPL Web Site.
EXHIBIT 6	Kronlage, U.S. Patent No. 4,079,338.
EXHIBIT 7	Hotta, *et al.* U.S. Pat. No. 5,133,064.
EXHIBIT 8	File History of the '336 Patent: Amendment of April 15, 1996.
EXHIBIT 9	File History of the '336 Patent: Amendment of January 8, 1997.
EXHIBIT 10	File History of the '336 Patent: Amendment of July 3, 1997.
EXHIBIT 11	Magar, U.S. Pat. No. 4,503,500.
EXHIBIT 12	Schaire, U.S. Pat. No. 4,453,229.
EXHIBIT 13	Claim Chart Provided by Alleged Patent Owner in part Technology Properties, Ltd. Pursuant to Local Rules of the Federal District Court of the Eastern District of Texas.
EXHIBIT 14	IEEE Std. 796-1983.
EXHIBIT 15	Antonaccio, *et al.,* U.S. Pat. No. 4,223,880.
EXHIBIT 16	Brenig, U.S. Pat. No. 4,718,081.
EXHIBIT 17	Y. Parker, Multi-Microprocessor Systems (1983), Chapter 1.
EXHIBIT 18	Mead & Conway, *Introduction to VLSI Systems* (1980).

V. A COPY OF THE REEXAMINATION PATENT IN DOUBLE-COLUMN FORMAT

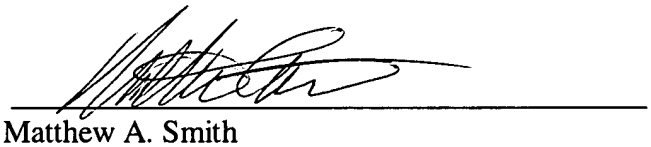
A copy of the reexamination patent in double column format is attached as Exhibit 1.

VI. **CERTIFICATION THAT A COPY OF THE REQUEST FILED BY A PERSON OTHER THAN THE PATENT OWNER HAS BEEN SERVED IN ITS ENTIRETY ON THE PATENT OWNER AT THE ADDRESS AS PROVIDED FOR IN § 1.33(C).**

I hereby certify that on September 21, 2006, I caused a complete copy of this request for *ex parte* reexamination together with all exhibits and attachments to be served upon the following party by First Class Mail as provided in 37 C.F.R. §1.248(a)(4):

Mr. Drew S. Hamilton
Knobbe, Martens, Olson & Bear, LLP
550 W C St Ste 1200
San Diego, CA 92101

Date Sept. 21, 2006



Matthew A. Smith
Registration No. 49,003

VII. **NOTICE OF PENDING LITIGATION**

Requester is aware that U.S. Pat. No. 5,809,336 is being asserted by Technology Properties Limited, Inc. before the Federal District Court for the Eastern District of Texas in the case styled:

> *Technology Properties Limited, Inc., v. Fujitsu Limited et al.*, Case No. 2:05-cv-00494-TJW, Federal District Court for the Eastern District of Texas, Marshall Division.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this request under 37 C.F.R., or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check or credit card payment form being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741.

Respectfully submitted,

Date Sept. 21, 2006 By _____

FOLEY & LARDNER LLP
Customer Number: 22428
PATENT TRADEMARK OFFICE
Telephone: (202) 295-4618
Facsimile: (202) 672-5399

Matthew A. Smith
Registration No. 49,003

APPENDIX A:

MANNER OF APPLYING THE CITED PRIOR ART TO EVERY CLAIM FOR WHICH REEXAMINATION IS REQUESTED

TABLE OF CONTENTS

I. INTRODUCTION

Technology Properties Limited, Inc. ("TPL"), a self-styled "purpose-built boutique that specializes in the development, commercialization and management of IP assets," (Exhibit 5), has sued several major suppliers of microprocessors for infringement of U.S. Pat. No. 5,809,336 ("the '336 patent") before the Federal District Court for the Eastern District of Texas. TPL appears to believe that any computer sold today requires a license under the '336 patent. On its Web site, for example, TPL states "[u]se of US '336 is prevalent across most microprocessors from low speed microcontrollers to sophisticated systems on chips....Virtually every product manufactured today utilizing microprocessors or embedded processors will require an MMP Portfolio license."

The dense thicket of highly relevant, unexamined prior art that predates the '336 patent, however, belies TPL's views. As the Requester will show, at the time of the earliest possible benefit date of the '336 patent (1989), every technique claimed by the '336 patent, although ultimately not commercially successful, had already become part of the prior art. For these reasons, Requester respectfully submits that all claims of the '336 patent should be reexamined and found unpatentable in light of the newly cited prior art.

II. TECHNOLOGY AT ISSUE AND FIELD OF THE INVENTION

The '336 patent deals, broadly speaking, with methods for clocking microprocessors. In many commercially available microprocessors, a clock is required to help control the operation of the microprocessor and to help synchronize events between different components of the microprocessor system. Using a clock, the components of the microprocessor

system can be synchronized, so that communications between components can take place efficiently.

Claim 1 of the '336 patent is reproduced here for the Examiner's reference:

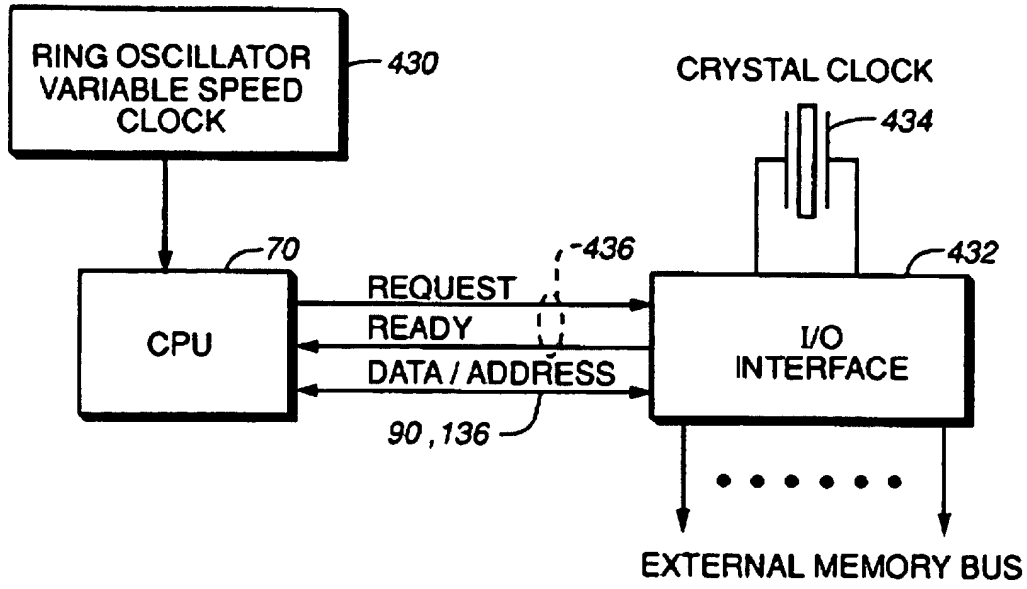
1. A microprocessor system, comprising a single integrated circuit including

a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,

said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;

an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.

The first body limitation claims "an entire ring oscillator variable speed system clock...for clocking said central processing unit". The figure on the face of the '336 patent shows a relevant configuration:



A ring oscillator as recited in claim 1 (and shown in the Figure above as reference symbol 430) can be defined as an odd number of inverting elements connected in a loop. Each inverter operates after a small delay to produce an output that is the inverse of its input. Figure 18 of the '336 patent shows a typical ring oscillator, which has seven inverters connected serially in a ring form:

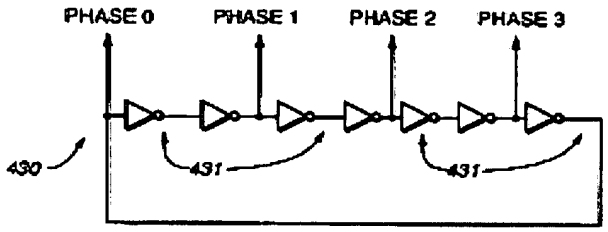


FIG._18

Since the number of inverting elements is odd, the system is unstable, and the output of any one inverter will change roughly as fast as the series of the remaining inverters can switch. For example, if the first node (phase 0) in Fig. 18 is at low voltage (LO), the output of the first inverter will be high voltage (HI). The output of the following inverters, working from left to right will be

Inverter 2 output (phase 1)	LO
Inverter 3 output	HI
Inverter 4 output (phase 2)	LO
Inverter 5 output	HI
Inverter 6 output (phase 3)	LO
Inverter 7 output (phase 0)	HI

The output of the seventh inverter is connected to the input of the first inverter (phase 0), which began at LO. Since the output of the seventh inverter is HI, this changes all of the values in the above table to their opposites. In this manner, the input voltage to the first

inverter (and indeed all of the inverters) changes as fast as the other inverters in the ring can switch. Using these principles, a number of ring oscillator configurations can be produced, some of which are shown in the 1980 Mead & Conway undergraduate textbook entitled "*Introduction to VLSI Systems*" (Exhibit 18, p. 234-35).

According to the '336 patent, since a ring oscillator is constructed from semiconductor elements, its frequency may vary over a wide range with ambient and manufacturing conditions. This is in contrast to crystal-based oscillators and conventional frequency-controlled ring oscillators, which vary their oscillation frequencies within a more limited range. The '336 patent microprocessor design calls for allowing the ring oscillator to run freely, in the hope that it will vary in the same way as the speed of other semiconductor components in the microprocessor with changes temperature and other conditions.

The purported advantage of this may be considered as follows: suppose the CPU changes the speed at which it can carry out operations like addition and multiplication with changes in temperature and other conditions. If the maximum (error-free) CPU speed becomes lower, but the clock speed remains the same, there is some risk that the maximum CPU speed will dip below the clock speed. To take this into account, designers can use a "safe" clock speed—one significantly lower than the maximum CPU speed under normal conditions. The '336 patent, however, claims to solve the problem in a different way: by placing the clock resonator on the same integrated circuit as the CPU, and allowing the resonator to run freely, without constraint. According to the '336 patent, this allows the clock to be designed to run faster, because it will automatically scale back its speed if the CPU slows down:

> The ring oscillator 430 is useful as a system clock, with its stages 431 producing phase 0-phase 3 outputs 433 shown in FIG. 19,

> because its performance tracks the parameters which similarly affect all other transistors on the same silicon die. By deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast. [Col. 16, l. 63 – col. 17, l. 2] (emphasis added).

The '336 patent describes that the ring oscillator varies over a wide range of frequencies:

> The CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process. [Col. 17, ll. 19-22]

The Applicants considered this feature central to their invention, and represented this to the Office several times during original prosecution. For example, in their Amendment of April 15, 1996, the Applicants stated:

> Applicants note that the present invention is directed to a microprocessor system including a central processing unit and a ring oscillator variable speed system clock connected thereto. In accordance with the claimed invention, the central processing unit and the ring oscillator variable speed system clock are provided in a single integrated circuit. This allows for example the central processing unit to track variations in the speed of the ring oscillator variable speed system clock, since the elements of each are disposed in the same integrated circuit. [Exhibit 8, p. 6] (emphasis added).

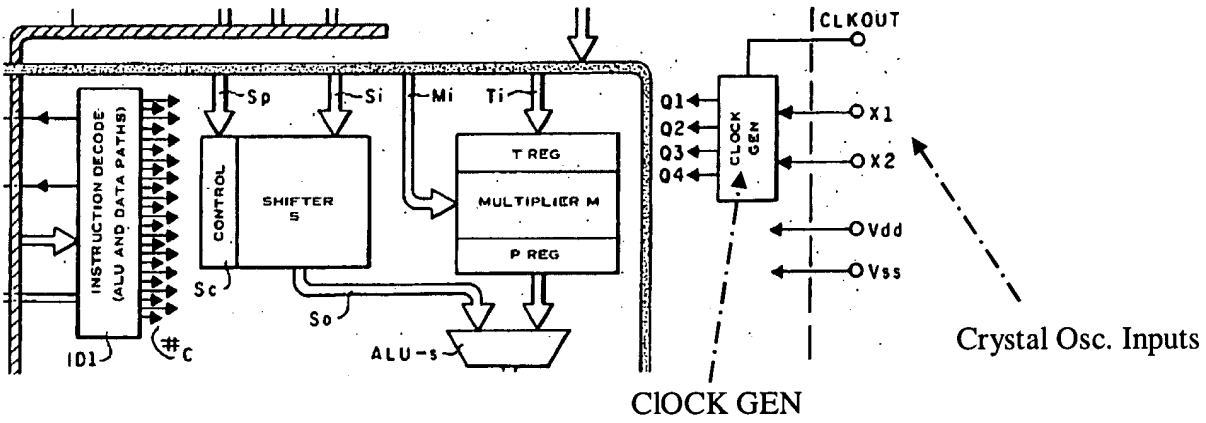
In their Amendment of January 8, 1997, Applicants stated:

> In the interview, the fact that operating characteristics of electronic devices in an integrated circuit will track one another depending on variations in the manufacturing process used to make the integrated circuit was discussed. This allows the microprocessor to operate at its fastest safe operating speed, given its manufacturing process or changes in its operating temperature or voltage. In contrast, prior art microprocessor systems are given a rated speed based on possible worst case operating conditions and an external clock is used to drive them no faster than the rated speed. [Exhibit 9, pp. 3-4] (emphasis added).

In their Amendment of July 3, 1997, the Applicants assured the Examiner:

> Crucial to the present invention is that since both the oscillator or variable speed clock and driven device are on the same substrate, when the fabrication and environmental parameters vary, the oscillation or clock frequency and the frequency capability of the driven device will automatically vary together. This differs from all cited references in that the oscillator or variable speed clock and the driven device are on the same substrate.... [Exhibit 10, p. 5] (emphasis added).

The Office was not able to rebut such statements during original prosecution, which were true only in the limited vacuum of the "cited prior art". The reference before the Examiner that most closely approximated the "on-chip ring oscillator" or "variable speed system clock" was the Magar patent, (U.S. Pat. No. 4,503,500, Exhibit 11). The Magar patent described an off-chip crystal oscillator, with on-chip clock generation circuitry. The pertinent portions of Fig. 2A from the Magar patent are shown below, with dashed arrows added by the Requester to indicate particular features:



Magar shows "CLOCK GEN" circuitry on the right-hand side of Fig. 2A that is on a single substrate with the CPU. The CLOCK GEN circuitry, however, has crystal oscillator inputs X1 and X2. This leads to the supposition that CLOCK GEN is not a resonator itself, but rather circuitry that amplifies, filters or otherwise prepares the crystal resonator output for use as

a CPU clock. Since the crystal resonator of Magar was off-chip, the Applicants were able to assert:

> one of ordinary skill in the art should readily recognize the speed of the CPU and the clock *do not* vary together due to manufacturing variation, operating voltage and temperature of the IC in the Magar microprocessor, as taught in the above quotation from the reference. This is simply because the Magar microprocessor clock is frequency-controlled by a crystal which is also external to the microprocessor. Crystals are by design fixed-frequency devices whose oscillation speed is designed to be tightly controlled and to vary minimally due to variations in manufacturing, operating voltage and temperature. The Magar microprocessor in no way contemplates the variable speed clock as claimed. (emphasis in original) [Amendment of July 3, 1997, Exhibit 10, p. 3-4]

If the Office had had access to the best prior art, it could have quickly met this argument with a better rejection. In fact, by 1980, the use of on-chip ring oscillators to clock integrated circuits was *undergraduate textbook knowledge*, appearing in Mead & Conway (Exhibit 18). In Chapter 7, the Mead & Conway textbook discusses integrated circuit clocks, stating that they are most easily constructed using on-chip ring oscillators, and that the frequency of the ring oscillators will vary with ambient conditions and process technology:

> Process variation in integrated circuit fabrication does not allow accurate resonant networks to be fabricated by usual means, but it is perfectly feasible, indeed essential for self-contained VLSI systems, to generate clock signals on the chip....[T]he role of the clock in a synchronous system is to connect sequence and time....A *model* of the temporal behavior of the systems being clocked is built into the clock generator or in the choice of times for the various timers. The easiest way to build these timers is as chains of inverters. The propagation delay time of such a chain will of course vary with τ, according to the way in which the fabrication process, aging, temperature and power voltage affect τ. However, these variations only make the inverter chain a better model of the system being clocked than a fixed timer would be....Clocks that employ these delays as timers are all elaborations

> of the *ring oscillator*. [Exibit 25, p. 233-35](italics in original, underlining added).

Numerous other examples are found in the art prior to 1989. One example of the use of a frequency-controlled ring oscillator is provided in U.S. Pat. No. 4,079,338 to Kronlage (Exhibit 6). The Kronlage patent issued in 1978, more than ten years before the earliest possible filing date of the applications leading to the '336 patent. Kronlage describes the use of an on-chip ring oscillator. For example, the Abstract provides:

> [a] novel ring oscillator circuit includes means by which the repetition rate is adjustable...The ring oscillator may be fabricated on a single substrate along with other I^2L circuitry and be utilized as the clock source therefore. [Abstract]

As a third example, *Ledzius, et al.*, U.S. Pat. No. 4,691,124, shows a ring oscillator used to drive a processor at its maximum possible speed (Exhibit 2; Figs. 1-2; RN 18, 58). The description states:

> [s]ince both clock generator 18 and functional circuit 16 are constructed on substrate 14, clock generator 18 compensates for temperature and process caused variations in the true maximum speed of functional circuit 16. The frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances. Accordingly, process caused variations are compensated because clock generator 18 is always physically made from the same batch and section of a semiconductor wafer as functional circuit 16. Slowest signal path 38 of functional circuit 16 controls the true maximum speed. Accordingly, process variations which affect slowest signal path 38 also affect clock generator 18. [Exhibit 2; col. 4, lines 5-14] (emphasis added).

Yet another example may be found in *Kato*, U.S. Pat. No. 4,766,567, which deals with a single chip microprocessor, states "first clock generating section 141 may be replaced by a ring oscillator of the known type or a CR clock oscillator similar which is completely built on semiconductor substrate 10. When a ring oscillator is used, its output frequency lowers in

proportion to the speed of the data processing circuit which is lowered due to the drop of power supply voltage. Therefore, the above-mentioned advantages will be more prominent." [Exhibit 4; Fig. 4, RN 141, Col. 10, l. 67 – Col. 11, l. 7] (emphasis added).

Since the Office had not been provided with the art describing a "crucial" limitation of the claims, its later discovery is respectfully submitted to raise a substantial new question of patentability.

The '336 patent also mentions, although not in sufficient detail to satisfy the requirements of 35 U.S.C. § 112, a communications interface for the processor. For example, claim 19 (patent claim 1) was amended to recite:

> an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock, independent of said first ring oscillator variable speed system clock connected to said input/output interface.

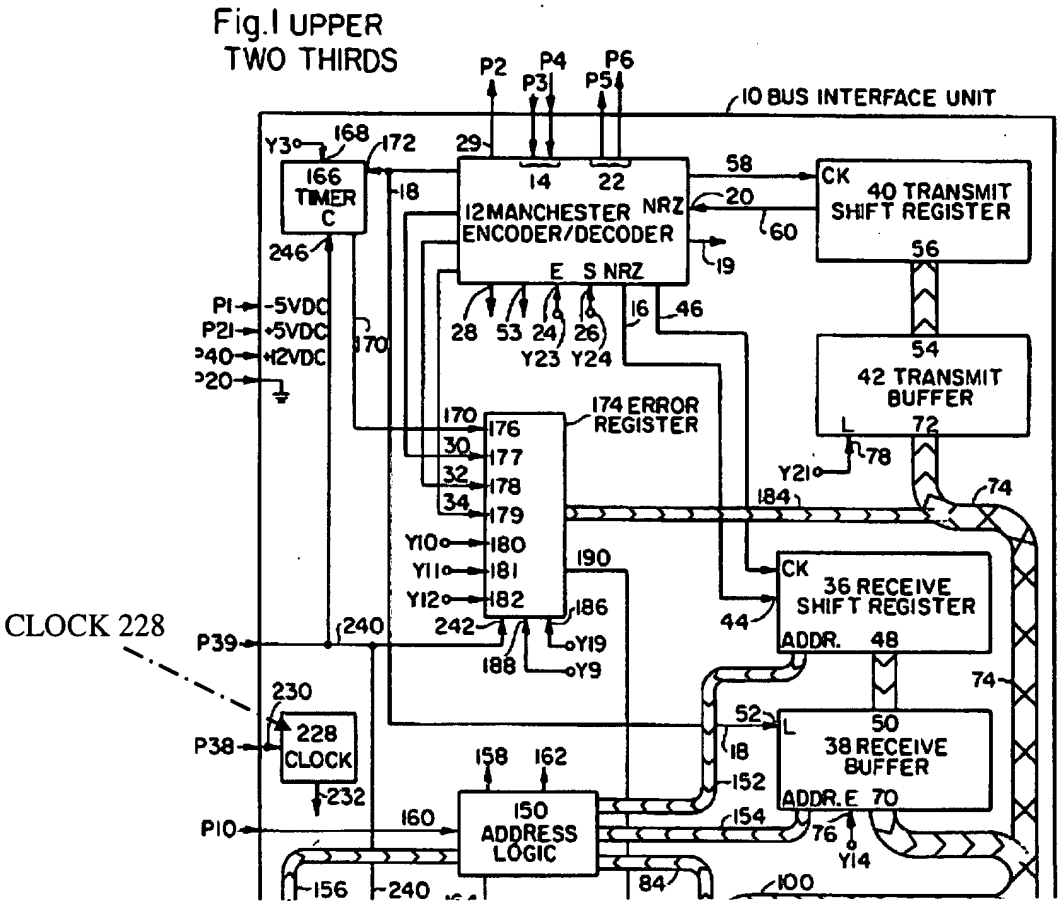
Since the ring oscillator varies its output over a wide range of frequencies, the question arises as to how the processor can communicate with other devices off of the integrated circuit, which have no information about the ring oscillator's speed. Does the processor force the outside world to run at the speed of the ring oscillator? If one credits the specification of the '336 patent, this solution would be of limited practical use, since other devices would not vary in their processing frequency capabilities in the same way as the ring oscillator would vary its speed.

More likely, the processor employs an "asynchronous" interface that allows the processor, which has a wide range of speeds due to the ring oscillator, to interact with other

devices that may have more fixed operation frequencies. The '336 patent tangentially states this idea as follows:

> The CPU 70 executes at the fastest speed possible using the adaptive ring counter clock 430. Speed may vary by a factor of four depending upon temperature, voltage, and process. The external world must be synchronized to the microprocessor 50 for operations such as video display updating and disc drive reading and writing. This synchronization is performed by the I/O interface 432, speed of which is controlled by a conventional crystal clock 434. [Exhibit 1, Col. 17, ll. 19-27]

During original prosecution, the Examiner apparently considered the most relevant art regarding these final limitations to be the Schaire reference, U.S. Pat. No. 4,453,229 (Exhibit 12). As noted by Examiner Eng in the Office Action of December 12, 1995, Schaire shows an input/output interface with a clock 228. Figure 1 from Schaire is partially reproduced here, with a dashed arrow added to point out the clock 228:



In response to the Examiner's rejections of claim 20 over Schaire in combination with Sheets, Applicants stated that "Schaire provides no indication that bus interface unit 10 is clocked by a signal from a clock different from that used to clock the host microprocessor."

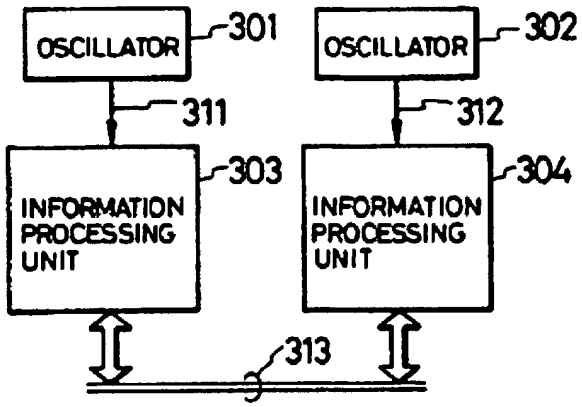
Again, however, the best art was not before the Examiner. In fact asynchronous interfacing between systems with different clock speeds had been known for years in the art. The 1980 undergraduate text Mead & Conway, for example, described the principle nearly ten years before the filing of the first Moore, *et al.* application as follows:

> A system such as a microprocessor may be entirely synchronous internally but cannot extend this synchrony indefinitely to encompass all of the external world with which it may interact. If asynchronous signals of external origin are allowed to enter a synchronous system as ordinary inputs, the timing constraints

> required to assure correct operation cannot be satisfied, since there is no known relationship between the timing of the asynchronous inputs and the clock....So, a slightly smarter thing to do is to ensure that only one clocked storage element is affected by a given asynchronous input. A clocked storage element that is used this way is called a synchronizer, since it is intended to produce an output signal that is in synchrony with the clock. [Exhibit 18, pp. 237-38.

Hotta, *et al.*, U.S. Pat. No. 5,133,064 (Exhibit 7, filed April 28, 1988), is also indicative of the state of the art with regard to asynchronous interfaces in the relevant time period. For example, in the *Background of the Invention* section of Hotta *et al.*, prior art work on asynchronous interfaces is described. Figure 3 of the Hotta, *et al.* reference is shown below:

FIG. 3 PRIOR ART



Each processor operates with a separate, independent oscillator. *See* Hotta, *et al.*, col. 2, ll. 1-3. As noted in Hotta, *et al.*, this necessitates the use of well-known asynchronous interfaces available in the art prior to 1989:

> The arrangement of the second prior art approach [Fig. 3] is <u>often found in microprocessor systems</u> or the like. Each information processing unit corresponds to an LSI chip. The first problem of this prior art approach is that, since the two information processing

> units are controlled by two different clock signals, the information processing units must be interfaced asynchronously. [Col. 2, ll. 3-15].

Numerous other asynchronous interfaces and synchronous interfaces with dual clock schemes had been known for years prior to the filing of the application leading to the '336 patent. For example, Ledzius, *et al.*, U.S. Pat. No. 4,691,124, shows an on-chip ring oscillator used to drive the microprocessor at its maximum theoretical processing speed, coupled to an on-chip input/output interface connected to a processor bus driven by an external clock. *See* Exhibit 2, col. 3, l. 67 – col. 4, l. 2.

Another example is provided by U.S. Pat. No. 4,750,111 to Crosby, *et al.* (Exhibit 3), which describes a multi-processor BOSS bus. The BOSS bus is a synchronous bus for use with multiple processors having different clock speeds. *See* col. 8, l. 59 – col. 9, l. 1; col. 5, ll. 45-52; col. 5, l. 64 – col. 6, l. 7. The processor bus has an interface (Fig. 5, col. 4, ll. 19-21) to each processor on the system for exchanging data, address and control signals. *See* claim 1, element (e); col. 2, ll. 52-58; col. 10, ll. 10-42. The processor bus runs at a clock rate independent of each processor that is fed to each processor bus interface. *See* col. 13, ll. 22-27; col. 9, ll. 19-26; col. 7, ll. 37-49; col. 10, ll. 26-42; Fig. 5 (inputs PBCLK and PBSYNC); col. 9, ll. 3-6.

Similarly, IEEE Std. 796-1983 (Exhibit 14) describes a standardized processor/memory bus based on the Intel Microbus® that is designed to "[allow] modules of different speeds to be interfaced by way of the bus." *See* p. 9. The bus can be operated in multimaster mode. *See id.* Each master has a CPU which sends "command signals, address signals, and memory or I/O addresses" through the "bus exchange logic" to the system bus. *See* p.11, §2.1.1. The 796 Bus Specification calls for two clock lines. The first clock line BCLK* is used to synchronize bus contention logic and can be generated by only one master at a time,

meaning that the bus contention logic, part of the bus interface on other masters on the system are necessarily operating with an external clock. *See* p.12, §2.1.3.1.1. There is also a CCLK*, which is a fixed frequency clock generated by one of the master systems and supplied to all other masters. *See* p.12, §2.1.3.1.1.

As a further example, U.S. Pat. No. 4,223,880 to Antonaccio, *et al.* (Exhibit 15), describes a multiprocessor system bus. Each processor has an interface unit which exchanges "data, address and control information" with a CPU by way of an intraprocessor bus. *See* col. 2, ll. 5-15; Fig. 2. The bus operates according to a bus sync clock signal that is a derivative of the master system clock signal and which is fed into each bus interface module. *See* col. 5, ll. 17-40.

Requester thus makes this request based on the simple belief that a reasonable Examiner, presented with the most relevant prior art describing the features claimed to be patentable by the applicants, would not have allowed the claims in their present form. A detailed application of the prior art cited in the request, not before the Office during original prosecution, is described below.

III. PATENT OWNER'S CLAIM INTERPRETATIONS

The purported patent owner (in part) TPL has taken the position that the claims of '336 patent cover all microprocessors, including those that do not use variable speed clocks. The Requester, of course, opposes the claim interpretations proposed by TPL. Requester further recognizes that the Examiner is required to examine the claims under their broadest reasonable construction, whereas the construction given by a court may be considerably narrower. *See In re Yamamoto,* 740 F.2d. 1569, 1571 (Fed. Cir. 1984). TPL's constructions will be presented where

pertinent in this request, however, as an aide to the Examiner in understanding the how the claims are being understood and asserted by the patent owner.

IV. CLAIMS 1-10 ARE INVALID UNDER 35 U.S.C. § 102(B) OR 35 U.S.C. § 103(A) OVER LEDZIUS, *ET AL.*

U.S. Pat. No. 4,691,124 to Ledzius *et al.* ('124 patent) is entitled "[s]elf-compensating, maximum speed integrated circuit". The circuit employs an on-chip ring oscillator with input/output ports clocked by a second clock. The '124 patent discloses each element of all claims expressly or inherently, except as noted below. The Ledzius, *et al.* patent issued on September 1, 1987 and is prior art under 35 U.S.C. § 102(b).

1. Claim 1

(a) A microprocessor system, comprising a single integrated circuit including a central processing unit

The '124 patent discloses a microprocessor system comprising an integrated circuit. For example, the specification refers to an integrated circuit (IC) attached to a processor bus:

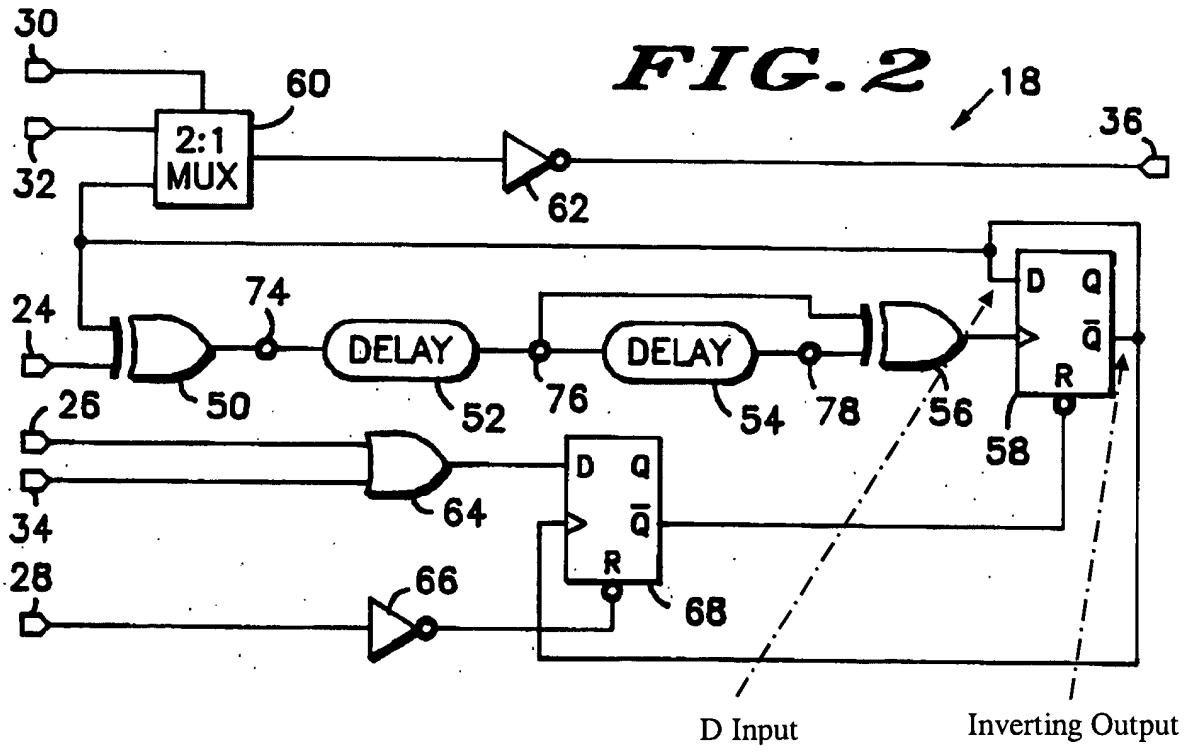
> Referring to FIG. 1, an integrated circuit (IC) 10 couples to a processor bus 12. Processor bus 12 includes conventional address, data, and control lines as may be required for a processor (not shown) to successfully communicate with IC 10. A functional circuit 16, a clock generator 18, and interface devices, such as latches 20, 21, 22, and 23 reside on a substrate 14 within IC 10." [Col. 2, ll. 24-32.]

The IC 10 is disclosed as having, among other things, a digital signal processing function. *See* col. 2, lines 43-45. One skilled in the art would immediately recognize that a circuitry for performing a digital signal processing function would include a CPU. As of 1989, a digital signal processor was conventionally implemented as a programmable microprocessor with a central processing unit. *See, e.g.,* Exhibit 16, U.S. Pat. No. 4,718,081, issued January 5,

1988, at col. 5, ll. 64-67 ("[c]ell site controller 26 may be any conventional digital signal processor, and preferably includes a central processing unit.").

(b) and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,

The '124 patent further discloses an entire ring oscillator variable speed system clock in said single integrated circuit. For example, Fig. 2 shows clock generator 18, which is part of the integrated circuit as shown in Fig. 1. Clock generator 18 has a D-Flip Flop connected in ring form, as indicated by the dashed arrows below, which have been added to Fig. 2:



The non-clock input to the D flip flop is connected to the inverting output. This arrangement is nothing more than an odd number (one) of inverting elements connected in a ring, *i.e.* a ring oscillator. Ring oscillators with similar delay schemes are shown in the 1980 Mead & Conway textbook. *See* Exhibit 18, page 235. The elements 50, 52, 54 and 56 are delays and

exclusive-OR gates used to generate a pulse of width corresponding to delay 54 to activate the D flip-flop every time the inverting output Q' signal changes. This results in a clock signal which is routed to clock output 36, and used to clock the central processing unit:

> Clock generator 18 contains a clock output node 36 which couples to clock input node 37 of functional circuit 16 and a process complete input node 34 which couples to process complete output node 35 of functional circuit 16. Additionally, clock generator 18 contains an external clock node 32 that couples to processor bus 12." [col. 3, l. 64-col. 4, l. 2].

(c) *said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;*

The '124 patent discloses that the ring oscillator and CPU are manufactured with the same process technology, and thus vary together in speed:

> Since both clock generator 18 and functional circuit 16 are constructed on substrate 14, clock generator 18 compensates for temperature and process caused variations in the true maximum speed of functional circuit 16. The frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances. Accordingly, process caused variations are compensated because clock generator 18 is always physically made from the same batch and section of a semiconductor wafer as functional circuit 16. Slowest signal path 38 of functional circuit 16 controls the true maximum speed. Accordingly, process variations which affect slowest signal path 38 also affect clock generator 18. [Col. 4, lines 5-14.]

> Furthermore, as disclosed in the summary of the invention:

> Accordingly, it is an object of the present invention to provide an improved integrated circuit (IC) which successfully operates at its true maximum speed. Another object of the present invention concerns providing an improved IC that is self-compensated so

that IC speed changes with temperature and process variations to insure operation at the IC's true maximum speed. [Col. 1, ll. 45-52].

(d) an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;

Fig. 1 of the '124 patent, shown below, indicates that the CPU and processor bus are connected by an on-chip[1] input/output interface comprising a number of latches 20-23 and control registers that exchange coupling control signals, addresses and data:

> Latches 20-22 represent conventional devices which pass data between functional circuit 16 and processor bus 12. As shown in FIG. 1, latches 20 and 21 represent input ports in which the processor writes data for use by functional circuit 16. Latch 22 represents an output port in which functional circuit 16 stores data so that the processor may read the data. No limit is placed on the number of data latches utilized by the present invention. Rather, the particular requirements of functional circuit 16 for each application control the number of data input and output latches." col. 3, lines 32-42.

[1] *See* Col. 2, ll. 29-32: "A functional circuit 16, a clock generator 18, and interface devices, such as latches 20, 21, 22, and 23 reside on a substrate 14 within IC 10."

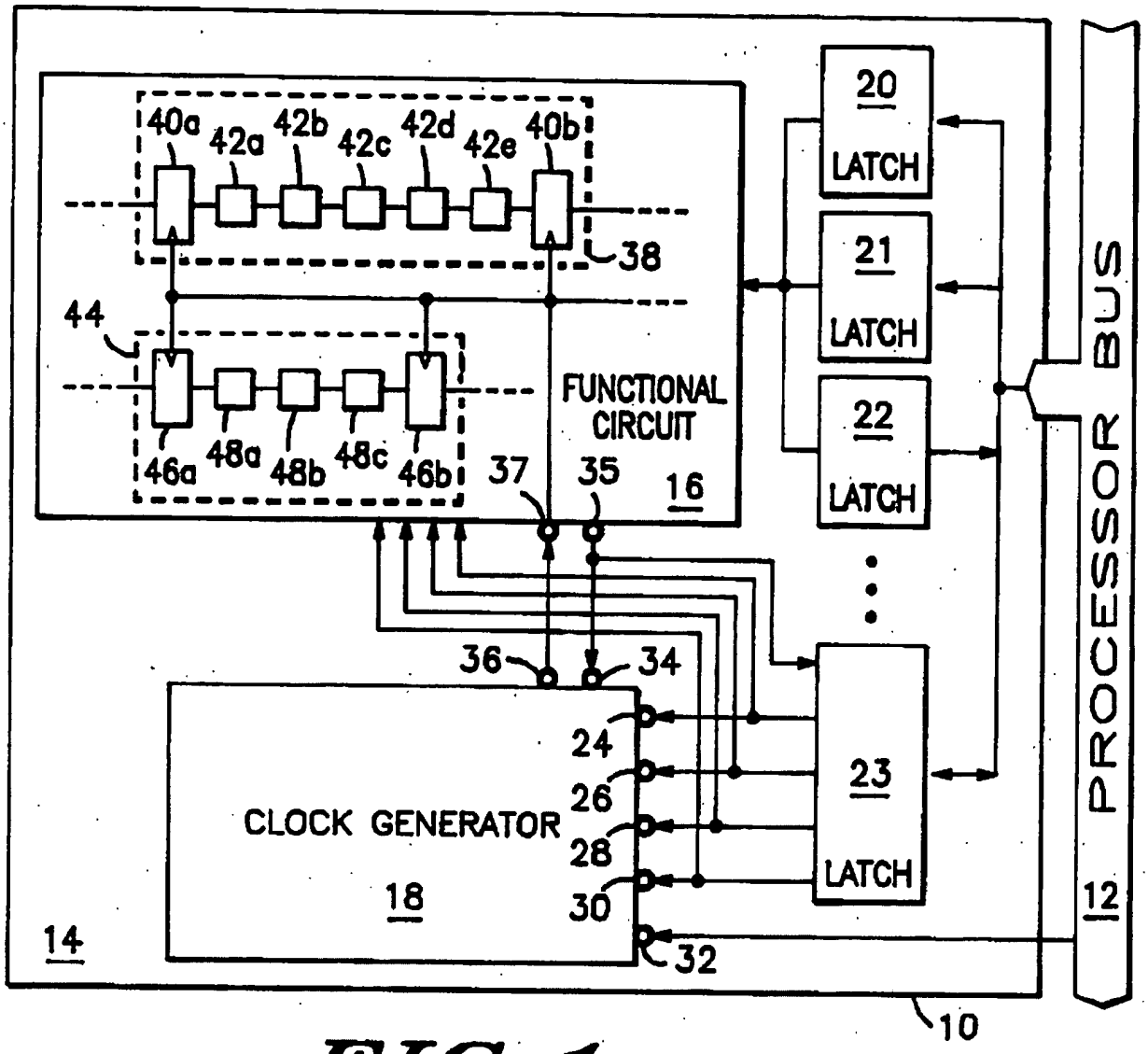


FIG. 1

The '124 patent, much like the '336 patent, deals with the problems of interprocessor communications. The typical communication arrangement described in the '124 patent involves processor 16 communicating over an input/output interface comprised of latches 20-23 with another processor on the processor bus 12. The input/output interface is required for processor 16, which operates asynchronously (at a different clock speed) to the processor bus, to communicate with another processor on the bus 12. *See, e.g.*, Abstract, ll. 3-5 ("The integrated

circuit operates asynchronously from a processor bus and contains circuitry for interfacing with the processor bus"); col. 1, ll. 57-59 ("another object of the present invention concerns providing an improved IC which operates asynchronously with other devices.").

Coupling with the processor bus 12 requires the exchange of addresses, data and control signals between the processor 16 and the input/output interface. *See, e.g.,* col. 2, ll. 26-29 ("Processor bus 12 includes conventional address, data and control lines as may be required for a processor (not shown) to successfully communicate with IC 10."). A person of ordinary skill in the art in 1989 would have immediately recognized that the processor 16 exchanges coupling control signals, data and addresses with the input/output interface, comprising at least input/output latches 20-23.

As one specific example of control signals, the '124 patent discloses that latch 23 that exchanges control signals that allow a processor on the processor bus to control the clock generator 18 and obtain information about when data from a particular process is available:

> Latch 23 represents a status/control interface between clock generator 18 and functional circuit 16 on one side and processor bus 12 on the other. Accordingly, outputs from latch 23 connect to a run node 24, a stop node 26, reset node 28, and a clock select node 30 of clock generator 18 as well as to inputs of functional circuit 16. Corresponding inputs of latch 23 couple to processor bus 12. Additionally, the process complete node 35 of functional circuit 16 connects to an input node of latch 23 with a corresponding output node coupled to processor bus 12. The processor writes bits of data to latch 23 to control operation of clock generator 18 and functional circuit 16. The processor reads bits of data from latch 23 to monitor the status of operations within functional circuit 16. Latch 23 is not limited to the particular number and description of signals described above but may accommodate any number of signals required by a particular application. For example, other signals may couple to processor bus 12 through latch 23 to communicate information about error conditions. [Col. 3, ll. 43-63].

One of the coupling control signals exchanged between the processor 16 and the input/output interface is the "process complete" signal 35. *See, e.g.,* col. 3, ll. 25-30. This signal informs other processors on the processor bus 12 that data is available to be read from the input/output interface, and is thus a form of handshaking signal.

(e) and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.

The '124 patent discloses that a second clock (shown in Fig. 1 as signal trace 32) is found on the processor bus and connected to the input/output interface comprising latches 20-23. *See, e.g.,* col. 3, l. 67 – col. 4, l. 2 ("Additionally, clock generator 18 contains an external clock node 32 that couples to processor bus 12.").

As shown in Fig. 1, the external clock is both on processor bus 12 and applied to an input of clock generator 18. The processor bus 12 is connected to the input/output interface latches 20-23. The processor bus clock is also used to clock input / output latches 20-23 when the clock generator 18 is disabled in favor of the external clock, since it is then the only available clock. *See* Col. 6, ll. 11-16.

2. Claim 2

The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.

The '124 patent describes that the clock 32 may be a "synchronous clock". See col. 6, ll. 14-16. In the prior art, a synchronous bus clock is almost always a fixed-frequency clock driven by a frequency-stable resonator. For example, Crosby, *et al.*, U.S. Pat. No. 4,750,111, describe the use of a synchronous processor bus having an asynchronous interface. The processor bus is clocked with a signal operating at a constant speed of 10 MHz (col. 19, ll. 44-45). This signal is used to clock each processor device interface. *See* '111 patent, col. 13, ll.

22-27; col. 9, ll. 19-26; col. 7, ll. 37-49; col. 10, ll. 26-42; Fig. 5 (inputs PBCLK and PBSYNC); col. 9, ll. 3-6. Thus, it would have been obvious to choose a fixed-frequency clock source based on the teaching of a processor bus with a synchronous clock in Ledzius *et al.*

3. Claim 3

(a) In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:

The '124 patent describes an integrated circuit microprocessor. Please see analysis and evidence under claim element 1(a), above. A method for clocking the microprocessor is also taught as described below.

(b) providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;

The '124 patent describes providing an entire ring oscillator within the integrated circuit which varies its operating characteristics with the operating characteristics of electronic devices within the microprocessor. Please see analysis and evidence under claim elements 1(b) and 1(c), above.

(c) using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;

The ring oscillator of the '124 patent is used to clock the microprocessor at a variable frequency. Please see analysis and evidence under claim elements 1(b) and 1(c), above.

(d) providing an on chip input/output interface for the microprocessor integrated circuit; and

The '124 patent teaches providing an on chip input/output interface. Please see analysis and evidence under claim elements 1(d) above.

(e) clocking the input/output interface with a second clock independent of the ring oscillator system clock.

The '124 patent teaches that the input/output interface is clocked with a second clock independent of the ring oscillator system clock. Please see analysis and evidence under claim elements 1(e) above. The processor bus clock 12 is used to clock the input / output interfaces when data is written to the latches by the bus or read from the latches by the bus.

4. Claim 4

The method of claim 3 in which the second clock is a fixed frequency clock.

Please see analysis and evidence under claim 2, above.

5. Claim 5

The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.

This claim appears to be indefinite or at least not described or enabled under 35 U.S.C. § 112. The literal wording seems to require that information be transferred to the *microprocessor* (*i.e* to the chip from an off-chip component) only on clock edges that coincide with clock edges of the ring oscillator.

The purported patent owner (in part) TPL, however, has indicated its intent to assert this claim on any system that can effect an information transfer over an interface. For example, Exhibit 13 is an infringement claim chart provided by TPL to Requester. The chart at page 19 indicates that TPL considers a UART in communication with a microprocessor as

meeting the claim language. TPL states "[t]he UART interface transfers information to and from the microprocessor in synchrony with the system clock." Since a UART (Universal Asynchronous Receive/Transmit) inherently involves an asynchronous timing relationship, TPL's interpretation of the claims would appear to have the claim language read on any transfer, irrespective of the timing relationships. Under this interpretation, which Requester opposes, the claimed limitation will always be met by prior art that shows the capability of effecting a transfer of information to the CPU, such as Ledzius, *et al.*

6. Claim 6

(a) A microprocessor system comprising:

The '124 patent describes an integrated circuit microprocessor. Please see analysis and evidence under claim element 1(a), above.

(b) a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

The '124 patent specifies that an integrated circuit made from a specific process will have a maximum speed (or processing frequency) depending on the process, operating conditions and the layout of the circuit:

> Most ICs which require a clock signal specify a maximum speed at which the IC operates. This specification typically takes the form of a maximum frequency or minimum time period that the clock signal must observe. The maximum speed specification typically accounts for temperature and process variations. In effect, each IC may be guaranteed to operate at least at the specified maximum speed regardless of a particular operating temperature within an acceptable temperature range or a particular wafer or batch in which the IC is processed. Accordingly, the specified maximum speed is slower than a true maximum speed at which most ICs will operate. [Col. 1, ll. 13-25]

(c) *an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;*

The '124 patent describes providing an entire ring oscillator within the integrated circuit which varies its operating characteristics with the operating characteristics of electronic devices within the processor. Please see analysis and evidence under claim elements 1(b) and 1(c), above.

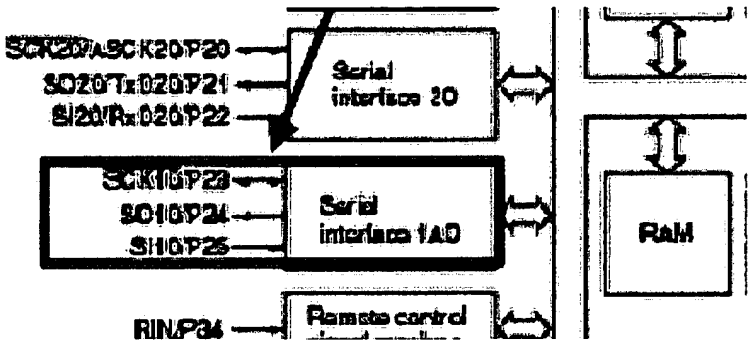
(d) *an on-chip input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and*

The '124 patent describes the processor 16 as connected via an input/output interface to a processor bus 12. The processor bus carries data and address signals. Although memory is not expressly described as being connected to the bus, it would have been immediately apparent to a person of skill in the art as of 1989 that the term "processor bus" means a bus that connects a microprocessor to external memory.

For example, the reference Y. Parker describes in his 1983 book "Multi-Processor Systems" (Exhibit 17) that the "[p]rocessor bus is the medium for all memory and input-output connections." (p. 11) and that the "[p]rocessor bus is the medium used for connection to memory and other input-output devices." (p. 17). These statements are made in the context of the Z8000, 8086 and MC68000 microprocessors, all leading microprocessors in their time. In addition, Crosby, *et al.*, U.S. Pat No. 4,750,111, (Exhibit 3) also describe the processor bus as a

bus connecting a number of processor devices and memory. *See* Crosby, *et al.*, Fig. 1; col. 6, ll. 3-7.

Furthermore, TPL has indicated in its claim charts provided to Requester that the presence of a serial interface on-chip is sufficient to meet the limitation of "an external memory interface".[2] For example, on page 24 of Exhibit 13, TPL points to the following structure as meeting this claim limitation:



Thus, according to TPL, the disclosure in Ledzius, *et al.* of interface latches should be sufficient to meet this claim limitation.

(e) an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

The '124 patent describes the processor bus as having an external clock 32 that is included in the bus. Figure 1 shows that the clock is connected to the input/output interface over processor bus 12. Please see analysis and evidence under claim element 1(e), above.

[2] Requester opposes this interpretation of the claims.

7. Claim 7

The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

Please see the analysis under claim elements 1(b) and 1(c), above.

8. Claim 8

The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.

This claim appears to be indefinite, not described and not enabled under 35 U.S.C. § 112. The claim seems to literally require that a fixed frequency clock signal that has clock edges that coincide with clock edges of a clock signal produced by the oscillator of claim 6. According to claim 6, however, the external clock is operative at a frequency independent of a clock frequency of the oscillator, and at a variable frequency.

TPL attempts to make sense of this claim in much the same way it makes sense of claim 5. That is, TPL asserts that if a transfer takes place, it must have been done "in synchrony" with the system clock.[3] For example, on page 29 of Exhibit 13, TPL points to a serial interface as meeting the claim limitation, with the notation: "[i]n order for the microprocessor to read uncorrupted data, the external clock domain must pass the data to the system clock domain in synchrony."

Thus, according to TPL, the mere fact that a data transfer takes place means that the external and internal clocks are "in synchrony". Since Ledzius, *et al.* show the transfer of data, this limitation is disclosed.

[3] Requester opposes this interpretation of the claim.

9. Claim 9

The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.

The '124 patent describes a ring oscillator. Please see the analysis and evidence under claim element 1(b), above.

10. Claim 10

(a) In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

The '124 patent describes a method of clocking the CPU in a microprocessor. Please see the analysis and evidence under claim elements 3(b)-(c), above.

(b) providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

Please see the analysis and evidence under claim element 6(b), above.

(c) providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

Please see the analysis and evidence under claim element 1(b), above.

(d) clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

Please see the analysis and evidence under claim elements 1(b)-(c), above.

(e) connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses

and data between said input/output interface and said central processing unit; and

The '124 patent describes that the input/output interface is connected to a processor bus, which is an external memory bus. Please see 6(d), above. The CPU and the input/output interface exchange address, data and coupling control signals, as demonstrated by the analysis and evidence cited under claim element 1(e), above.

(f) clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

Please see the analysis and evidence under claim element 3(e), above.

V. CLAIMS 1-10 ARE INVALID UNDER 35 U.S.C. § 103(A) OVER MEAD & CONWAY IN VIEW OF IEEE STD 796-1983.

The Mead & Conway text "Introduction to VLSI Systems" (Exhibit 18) is one of the better-known microprocessor design textbooks in history. It describes many aspects of design, including clocking using ring oscillators and asynchronously interfacing between synchronous systems. IEEE Standard. 796-1983 "Microcomputer System Bus" (Exhibit 14) provides a standard asynchronous system bus architecture and system bus interface for use with multiprocessor and multi-device systems.

There is express and implied motivation to combine the Mead & Conway and IEEE 796-1983 references. Mead & Conway disclose a microcomputer in Chapters 5 and 6 of their textbook. The disclosure of the microcomputer includes its incorporation into a system having a system bus and a system bus interface, as shown on page 147 in Figure 5.1, here with dashed arrows added:

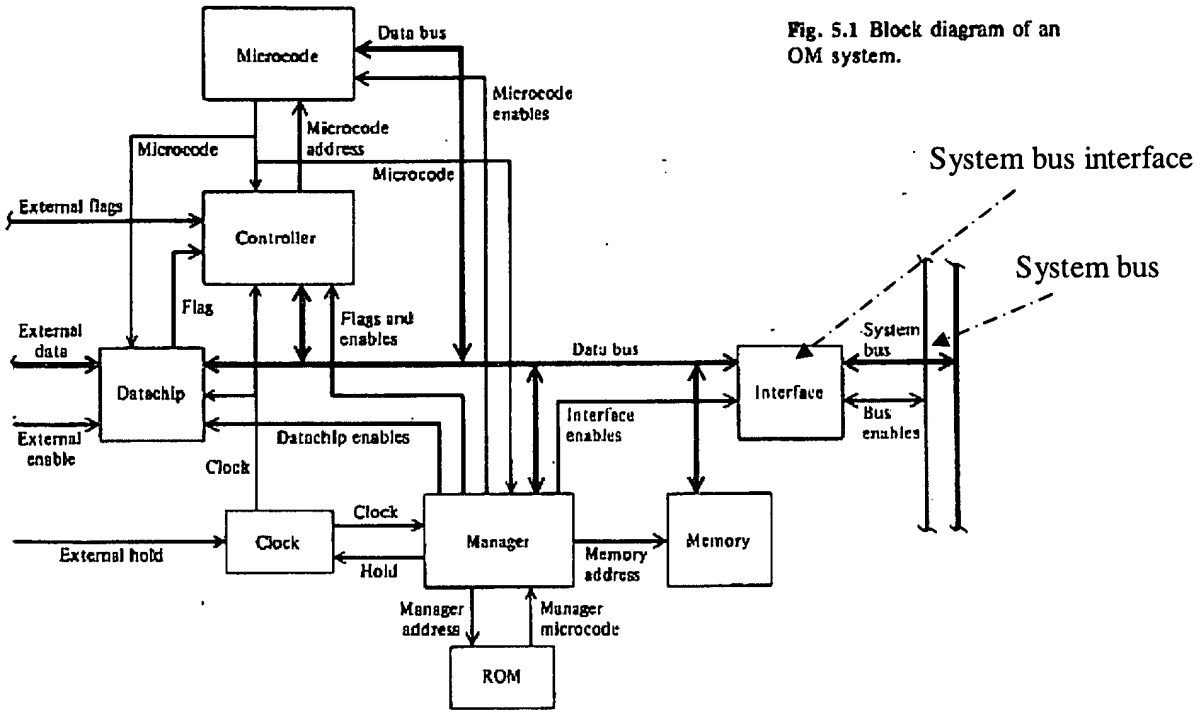


Fig. 5.1 Block diagram of an OM system.

Such a system bus and system bus interface are shown in IEEE Standard 796-1983. Stated purposes of the standard are to "[d]efine a general purpose microcomputer system bus", "[s]pecify device-independent electrical and functional interface requirements that a module shall meet in order to interconnect unambiguously by way of the system.", "[e]nable the interconnection of independently manufactured devices into a single functional system", "[p]ermit products with a wide range of capabilities to be introduced to the system simultaneously" and to "[d]efine a system with a minimum of restrictions on the performance characteristics of devices connected to the system." [Exhibit 14, p. 9].

Thus, Mead & Conway suggested in 1980 the incorporation of their device into a standard system bus, and IEEE Std. 796-1983 provided in 1983 a industry-standard way to do so. The skilled artisan working in 1989 would have had little difficulty in combining these two teachings.

1. Claim 1

(a) A microprocessor system, comprising a single integrated circuit including a central processing unit.

Mead & Conway describe a microprocessor system with a central processing unit in Chapters 5 and 6 of their textbook. *See* Exhibit 18, p. 147. Figure 5.1 of Mead & Conway describes an overall computer system with datachip and controller elements. The datachip comprises registers and ALUs, while the controller chip comprises the stack and program counter. *See* p. 190. The Mead & Conway textbook does not disclose that the components of its computer system are on a single integrated circuit. This would have been obvious, however, given the numerous statements in Mead & Conway relating to the desirability of integration onto Silicon and the trend toward higher levels of integration. For example,:

> Many LSI chips, such as microprocessors, now consist of multiple complex subsystems, and thus are really integrated systems rather than integrated circuits. What we have seen so far is only the beginning. Achievable circuit density now doubles with each passing year or two. Physical principles indicate that transistors can be scaled down to less than $1/100^{th}$ of their present area and still function as the sort of switching elements with which we can build digital systems. By the late 1980s it will be become possible to fabricate chips containing millions of transistors. [Preface].
>
> As λ is scaled down toward its minimum value, ultimately limited by the physics of semiconductors to about 0.1 μm, it will become feasible to implement single chip, maximum density VLSI systems of enormous functional power. [p. 137]
>
> As we look into the future and anticipate the dimensional scaling of technology, we must recognize that it will ultimately be possible to place large numbers of simple machines on a single chip. [p. 189]

It is further noted that the '336 patent for which reexamination is requested does not provide any teachings regarding integration techniques. That is, there is no breakthrough enabling disclosure in the '336 patent that would suddenly have allowed the art to combine on

one chip all elements that were previously on separate chips. If that enablement is not provided by the rest of the art, then the claims of the '336 patent are invalid under 35 U.S.C. § 112 ¶1.

(b) and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,

Mead & Conway describe the use of a ring oscillator as the system clock for an integrated circuit:

> [T]he role of the clock in a synchronous system is to connect sequence and time....A *model* of the temporal behavior of the systems being clocked is built into the clock generator or in the choice of times for the various timers. The easiest way to build these timers is as chains of inverters....Clocks that employ these delays as timers are all elaborations of the *ring oscillator*. [Exhibit 19, p. 233-35](italics in original, underling added).

The microprocessor disclosed in Chapter 5 has a "clock chip" which comprises an oscillator. Mead & Conway, as quoted above, state that the ring oscillator is the easiest and preferred method to clock the microprocessor.

(c) said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;

Mead & Conway disclose that the on-chip ring oscillator will vary with process variations, age, temperature and voltage. Mead & Conway further state that the on-chip ring oscillator will provide a "better model" than an off-chip oscillator for the VLSI system being clocked:

> Process variation in integrated circuit fabrication does not allow accurate resonant networks to be fabricated by usual means, but it

> is perfectly feasible, indeed essential for self-contained VLSI systems, to generate clock signals on the chip....The propagation delay time of such a chain will of course vary with τ, according to the way in which the fabrication process, aging, temperature and power voltage affect τ. However, these variations only make the inverter chain a better model of the system being clocked than a fixed timer would be.... [Exhibit 19, p. 233-35](italics in original, underling added).

(d) an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;

IEEE Std. 796-1983 describes a standardized processor/memory bus based on the Intel Microbus® that is designed to "[allow] modules of different speeds to be interfaced by way of the bus." Exhibit 15, p. 9. The IEEE Std. 796-1983 discloses a bus interface (see p. 11, Fig. 1 (bus exchange); p. 25; p. 12, Fig. 2; p. 26, Fig. 15) which would have been obvious to integrate on-chip given the requisite level of integration available in the art. Please see above under limitation 1(a).

Each master has a CPU which sends "command signals, address signals, and memory or I/O addresses" through the "bus exchange logic" to the system bus. *See* p.11, §2.1.1.

(e) and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.

The IEEE Std. 796-1983 calls for two clock lines. The first clock line, BCLK*, is used to synchronize bus contention logic and can be generated by one system master and is received by all other system masters. *See* chart at page 32..All signals used by each device's bus interface to control master acquisition of the bus are synchronized using the BCLK* signal, and BCLK* is thus furthermore used to clock the interface. *See* p. 25 ("All bus exchange signals are synchronized using BCLK*"). Each master bus interface has access to the BCLK* signals, since these signals are used by the master to request control of the bus. *See* p. 24; see also chart at p.

32. For example, as shown on page 32, the BCLK* signal is generated in "1 place" and received by all bus masters. The BREQ* signal, which is clocked by BCLK* (p. 25), is generated by "each master" and received by the "central priority module". Thus, when used in a multi-master system as described (*see* p. 9), the IEEE Std. 796-1983 teaches the use of a second, independent and external clock connected to the input / output interface and used to clock the interface.

The second clock line is designated CCLK*, which is a fixed frequency clock generated by one of the master systems and supplied to all other masters. *See* p.12, §2.1.3.1.1. This clock is part of the bus and thus connected to the bus interface. *See* p. 14, Fig. 2 (note that the diagram in Fig. 2 does not show the BCLK* signal because "[i]t is assumed in this discussion that there is only one master on the bus, and therefore no bus contention exists." p. 14.). When generated by another master, CCLK* is independent and external to the system clock.

Claim 2

The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.

The CCLK* is disclosed as being a "periodic signal of constant frequency". *See* p. 12. The BCLK* signal is disclosed as having a range of possible periods and hence frequencies (*see e.g.* chart at p. 30, row entry 4). The IEEE Std. 796-1983 also discloses that the BCLK* may be slowed or stopped. *See* p. 25. However, these must be understood as design possibilities, not as a disclosure that BCLK* is a always clock with variable frequency. That is, the designer may choose a fixed frequency, and once the designer chooses the operating frequency, it is stable with an narrow range, such as the clock provided by a crystal resonator. This is disclosed at page 25, where it is stated "[t]here is no requirement for synchronization between BCLK* and CCLK*, but they may be derived from the same source." Since CCLK* is a fixed-frequency clock, BCLK* will also be fixed-frequency if it is derived from the same

source, although through clock skew it may not be in-phase (synchronized) with CCLK*. *See also* p. 27 ("[i]f the maximum BCLK* of 10 MHz is used, then the number of masters in a serial chain is limited to three.").

2. *Claim 3*

(a) *In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:*

Please see analysis and evidence under claim element 1(a), above. A method for clocking the microprocessor is also taught.

(b) *providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;*

Please see analysis and evidence under claim elements 1(b) and 1(c), above.

(c) *using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;*

Please see analysis and evidence under claim elements 1(b) and 1(c), above.

(d) *providing an on chip input/output interface for the microprocessor integrated circuit; and*

Please see analysis and evidence under claim elements 1(d) above.

(e) *clocking the input/output interface with a second clock independent of the ring oscillator system clock.*

Please see analysis and evidence under claim elements 1(e) above.

3. Claim 4

The method of claim 3 in which the second clock is a fixed frequency clock.

Please see analysis and evidence under claim 2, above.

4. Claim 5

The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.

This claim appears to be indefinite or at least not described or enabled under 35 U.S.C. § 112. The literal wording seems to require that information be transferred to the *microprocessor* (*i.e.* to the chip from an off-chip component) only on clock edges that coincide with clock edges of the ring oscillator.

The purported patent owner (in part) TPL, however, has indicated its intent to assert this claim on any system that can effect an information transfer over an interface. For example, Exhibit 13 is an infringement claim chart provided by TPL to Requester. The chart at page 19 indicates that TPL considers a UART in communication with a microprocessor as meeting the claim language. TPL states "[t]he UART interface transfers information to and from the microprocessor in synchrony with the system clock." Since a UART (Universal Asynchronous Receive/Transmit) inherently involves an asynchronous timing relationship, TPL's interpretation of the claims would appear to have the claim language read on any transfer, irrespective of the timing relationships. Under this interpretation, which Requester opposes, the claimed limitation will always be met by prior art that shows the capability of effecting a transfer of information to the CPU, such as the combination of Mead & Coway with IEEE Std. 796-1983.

5. Claim 6

(a) A microprocessor system comprising:

Please see analysis and evidence under claim element 1(a), above.

(b) a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

Please see analysis and evidence under claim element 1(a), above.

(c) an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;

Please see analysis and evidence under claim elements 1(b) and 1(c), above.

(d) an on-chip input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

Please see analysis and evidence under claim element 1(d), above. The IEEE Std. 796-1983 bus is an external memory bus. *See* p. 11, Fig. 1; p. 14, Fig. 2.

(e) an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

Please see analysis and evidence under claim element 1(e), above.

6. Claim 7

The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

Please see the analysis and evidence cited under claim elements 1(b) and 1(c), above. The Mead & Conway text explicitly discloses that the ring oscillator varies with the operating voltage of the system.

7. Claim 8

The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.

This claim appears to be indefinite, not described and not enabled under 35 U.S.C. § 112. The claim seems to literally require that a fixed frequency clock signal that has clock edges that coincide with clock edges of a clock signal produced by the oscillator of claim 6. According to claim 6, however, the external clock is operative at a frequency independent of a clock frequency of the oscillator, and at a variable frequency.

TPL attempts to make sense of this claim in much the same way it makes sense of claim 5. That is, TPL asserts that if a transfer takes place, it must have been done "in synchrony" with the system clock.[4] For example, on page 29 of Exhibit 13, TPL points to a serial interface as meeting the claim limitation, with the notation: "[i]n order for the microprocessor to read uncorrupted data, the external clock domain must pass the data to the system clock domain in synchrony."

[4] Requester opposes this interpretation of the claim.

Thus, according to TPL, the mere fact that a data transfer takes place means that the external and internal clocks are "in synchrony". Since IEEE Std. 796-1983 shows the transfer of data, this limitation is disclosed.

8. Claim 9

The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.

The Mead & Conway expressly discloses the use of a ring oscillator. *See* Exhibit 18, page 233-35.

9. Claim 10

(a) In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

Please see the analysis and evidence under claim elements 3(b)-(c), above.

(b) providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

Please see the analysis and evidence under claim element 1(b) and 1(c), above.

(c) providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

Please see the analysis and evidence under claim element 1(b), above.

(d) clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

Please see the analysis and evidence under claim element 1(b) and 1(c), above.

(e) *connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and*

The CPU and the input/output interface exchange address, data and coupling control signals, as demonstrated by the analysis and evidence cited under claim elements 6(d) and 1(d), above.

VI. CLAIMS 1-10 OF U.S. PAT. NO. 5,809,336 ARE INVALID UNDER 35 U.S.C. § 103(A) OVER KATO, U.S. PAT. NO. 4,766,567 IN VIEW OF CROSBY, *ET AL.*, U.S. PAT. NO. 4,750,111.

U.S. Pat. No. 4,766,567 to Kato ('567 patent) describes a system on a chip as predicted by Mead & Conway (Exhibit 18, at Preface). Kato describes a chip including a CPU, a ring oscillator system clock that varies its processing speed with the operating conditions of the CPU, and on-chip input / output interfaces.

U.S. Pat. No. 4,750,111 to Crosby, *et al.* ('111 patent) describes a multi-processor BOSS bus. The BOSS bus is a synchronous bus for use with multiple processors having different clock speeds.

Express and implied motivation to combine can be found from both references. Both references are in the field of microprocessor and microcomputer system design. *See* '567 patent, col. 1, ll. 5-10; '111 patent, col. 6, ll. 7-12. The '567 patent presents a microprocessor that is designed for communication with external components. *See* '567 patent, col. 3, ll. 10-13. The '111 specifically provides that a "standard internal architecture" that can be used in "many different applications." '111 patent, col. 1, ll. 20-21. The '111 patent furthermore states that it is "optimized for multi-master, high-speed data transfer and satisfies the requirement that the equipment accommodate a highly diverse mix of processor devices and support efficient

intermodule data transfers." Col. 2, ll. 46-50. The '111 goes so far as to show how microprocessors can be used with its bus, and places no restriction on the type of microprocessor that can be used. For example, Fig. 2 of the '111 patent shows how microprocessors can be used with the '111 patent bus. The '111 patent describes the required standard bus interface and how it should be connected. *See* '111 patent, col. 9, ll. 19-32; col. 15, l. 12 – col. 17, l. 14; Figs. 5-9. A person of skill in the art would thus have had no difficulty in attaching a microprocessor to a bus designed to be a standard interface between microprocessors. It would therefore have been obvious to combine the microprocessor of Kato with the BOSS bus interface of Crosby, *et al.*, particularly given the advancing state of the art in integration technology as demonstrated in Mead & Conway. *See* Exhibit 18, at preface, p. 137, p. 189.

1. Claim 1

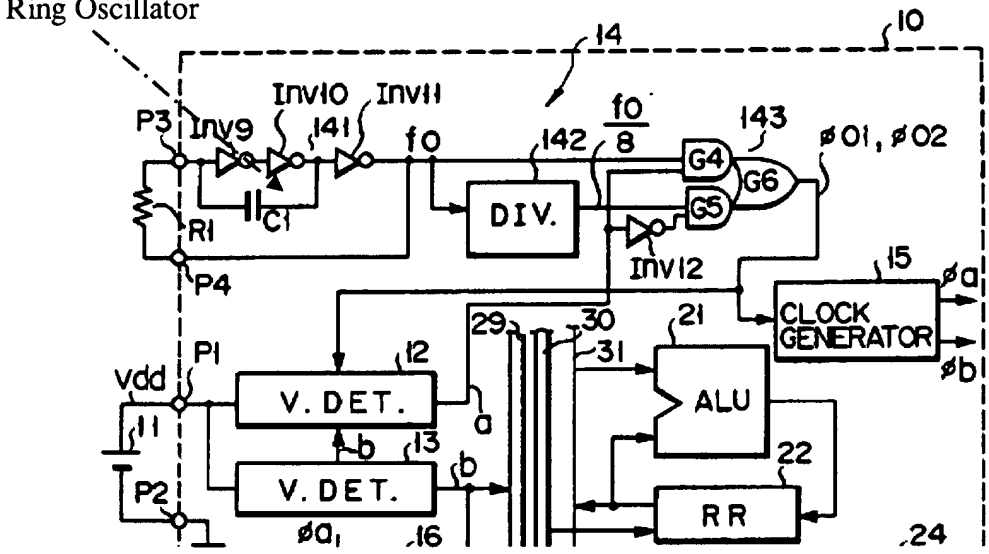
(a) A microprocessor system, comprising a single integrated circuit including a central processing unit.

The '567 patent describes a single integrated circuit microprocessor having a central processing unit. *See* col. 1, ll. 6-10; col. 4, ll. 63-68.

(b) and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,

The '567 patent describes on-chip ring oscillator with regard to the embodiment of Fig. 4. Pertinent parts of Fig. 4 are reproduced below, with a dashed arrow added to show the ring oscillator.

F I G. 4



The oscillator 141 comprises inverters Inv9, Inv10, and Inv11, and capacitor C1 on semiconductor substrate 10, as well as external resistor R1. This oscillator is a free running clock generation circuit that produces outputs Φ01 and Φ02 that are used to clock the CPU. *See* Fig. 4, col. 9, l. 67 – col. 10, l. 1.

Kato discloses that oscillator 141 can be replaced by a ring oscillator of a known type which is "completely built on the semiconductor substrate 10." Col. 10, l. 67 – col 11, l. 2 (emphasis added).

(c) *said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;*

The '567 patent discloses that the ring oscillator circuit is constructed on the same integrated circuit substrate (and hence from the same process technology) as the CPU. The '567

patent furthermore discloses that the ring oscillator need not be frequency-stable and varies its speed with the processing conditions of the CPU:

> The one-chip semiconductor device shown in FIG. 4 has the same advantages as the first embodiment (FIGS. 1 and 2). Since first clock signal Φ01 from which second clock signal Φ02 is produced, need not have a very accurate frequency, first clock generating section 141 may be replaced by a ring oscillator of the known type or a CR clock oscillator similar which is completely built on semiconductor substrate 10. When a ring oscillator is used, its output frequency lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of power supply voltage. Therefore, the above-mentioned advantages will be more prominent. [Col. 10, l. 63 – col. 11, l. 7].

(d) an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;

The '567 patent discloses on-chip input / output interfaces. *See* Fig. 1, RN 26-28. The '111 patent discloses a bus interface device to connect to the BOSS bus. *See* Fig. 5, col. 4, ll. 19-21; col. 9, ll. 19-32; col. 12, ll. 64-66. This interface exchanges data, addresses and coupling control signals with the associated CPU. *See* Fig. 5; col. 15, ll. 22-26 (describing Fig. 5); col. 16, ll. 17 – 23; claim 1, element (e); col. 2, ll. 52-58; col. 10, ll. 10-42. For example, the specification states that the processor bus interface acts as a conduit for data and addresses that come from the CPU going to the bus or vice versa:

> [t]he portion of a processor device interface that feeds data into and out of the device RAM, MCU, Computer, etc., such as 56 in FIG. 5, from or to another processor device or convertor module on the Converter Bus is the data interface circuit shown in FIG. 8. It feeds data and addresses to and from the Processor Bus where the device is in either the master or slave mode. [Col. 16, ll. 17 – 23].

Examples of control signals may be found in Table 3 ("Processor Device Interface Internal Signals", cols. 11-12), which lists the control signals which facilitate coupling between

the CPU ("device") and the processor bus interface, such as INADEN (indicated the presence of an address on buffered address lines), INT (indicating the type of transfer to be performed), INTEN (indicating the presence of an interrupt address), PBEN (indicating that a transfer will be made), WRT (indicating whether a read or write is to be performed), and DAWRT indicating that data to be written can be latched.

(e) and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.

The BOSS bus described in the '111 patent is a synchronous bus for use with multiple processors having different clock speeds:

> Furthermore, all processor devices have a standard bus interface that coordinates data transfers without involving complex bus swapping schemes or designating bus masters. This results in a relatively simple system that can handle relatively complex transfers between many processor devices operating at different speeds and between processor devices and the relatively very slow input/output converter modules. [Col. 9, ll. 19-27].

See also col. 8, l. 59 – col. 9, l. 1; col. 5, ll. 45-52; col. 5, l. 64 – col. 6, l. 7. The processor bus runs at a constant clock rate (10 MHz, col. 19, ll. 44-45) independent of and external to each processor. As combined with Kato, which uses a ring-oscillator that varies widely in speed, the fixed-frequency processor bus would furthermore have to operate independent of the processor bus clock. The processor bus clock signals are fed into each processor bus interface on each device and used to clock the interface. *See* col. 13, ll. 22-27; col. 9, ll. 19-26; col. 7, ll. 37-49; col. 10, ll. 26-42; Fig. 5 (inputs PBCLK and PBSYNC); col. 9, ll. 3-6.

2. Claim 2

The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.

The '111 patent discloses that the processor bus runs at a constant clock rate (10 MHz) independent of each processor. *See* col. 19, ll. 44-45.

3. Claim 3

(a) In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:

Please see analysis and evidence under claim element 1(a), above. A method for clocking the microprocessor is also thereby taught.

(b) providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;

Please see analysis and evidence under claim elements 1(b) and 1(c), above.

(c) using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;

Please see analysis and evidence under claim elements 1(b) and 1(c), above.

(d) providing an on chip input/output interface for the microprocessor integrated circuit; and

Please see analysis and evidence under claim elements 1(d) above.

(e) clocking the input/output interface with a second clock independent of the ring oscillator system clock.

Please see analysis and evidence under claim elements 1(e) above.

4. Claim 4

The method of claim 3 in which the second clock is a fixed frequency clock.

Please see analysis and evidence under claim 2, above.

(f) clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.

Please see the analysis and evidence under claim element 1(e), above.

5. Claim 5

The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.

This claim appears to be indefinite or at least not described or enabled under 35 U.S.C. § 112. The literal wording seems to require that information be transferred to the *microprocessor* (*i.e.* to the chip from an off-chip component) only on clock edges that coincide with clock edges of the ring oscillator.

The purported patent owner (in part) TPL, however, has indicated its intent to assert this claim on any system that can effect an information transfer over an interface. For example, Exhibit 13 is an infringement claim chart provided by TPL to Requester. The chart at page 19 indicates that TPL considers a UART in communication with a microprocessor as meeting the claim language. TPL states "[t]he UART interface transfers information to and from the microprocessor in synchrony with the system clock." Since a UART (Universal Asynchronous Receive/Transmit) inherently involves an asynchronous timing relationship, TPL's interpretation of the claims would appear to have the claim language read on any transfer, irrespective of the timing relationships. Under this interpretation, which Requester opposes, the

claimed limitation will always be met by prior art that shows the capability of effecting a transfer of information to the CPU, such as the combination of Kato with Crosby, *et al.*

6. Claim 6

(a) A microprocessor system comprising:

Please see analysis and evidence under claim element 1(a), above.

(b) a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

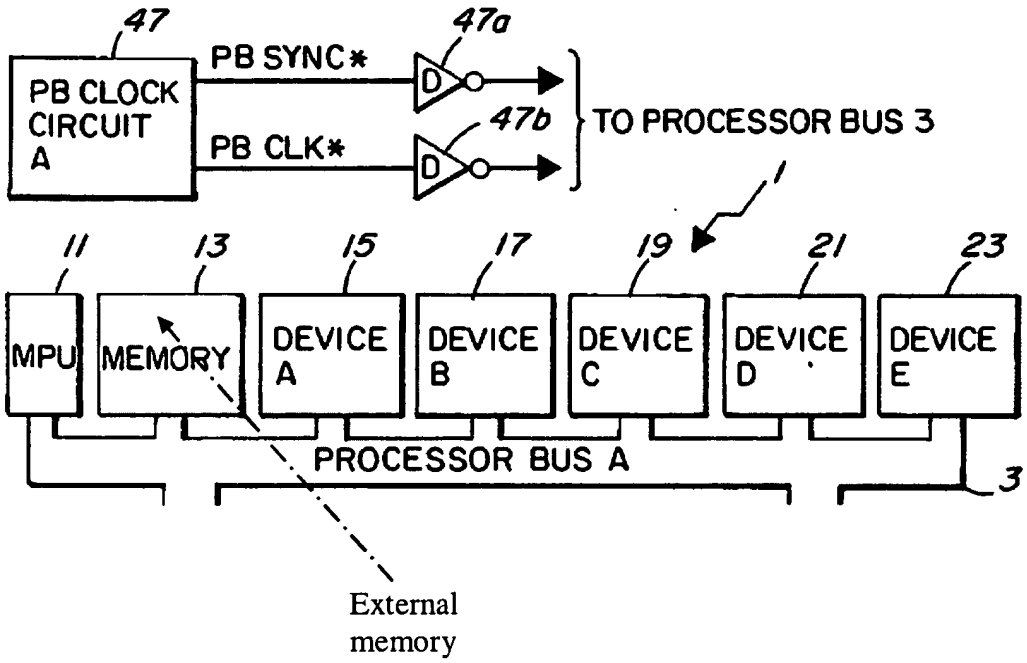
Please see analysis and evidence under claim element 1(a), above.

(c) an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;

Please see analysis and evidence under claim elements 1(b) and 1(c), above.

(d) an on-chip input/output interface, connected between said said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

Please see analysis and evidence under claim elements 1(d) above. It is clear that the BOSS processor bus is a memory bus, as shown in Fig. 1 of the '111 patent, the pertinent portions of which are shown below with a dashed arrow added to indicate the external memory:



(e) *an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.*

Please see analysis and evidence under claim element 1(e), above.

7. Claim 7

The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

Please see the analysis and evidence cited under claim elements 1(b) and 1(c), above. The '567 patent expressly discloses that the ring oscillator varies with the operating voltage of the system. *See* col. 11, ll. 2-7.

8. Claim 8

The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.

This claim appears to be indefinite, not described and not enabled under 35 U.S.C. § 112. The claim seems to literally require that a fixed frequency clock signal that has

clock edges that coincide with clock edges of a clock signal produced by the oscillator of claim 6. According to claim 6, however, the external clock is operative at a frequency independent of a clock frequency of the oscillator, and at a variable frequency.

TPL attempts to make sense of this claim in much the same way it makes sense of claim 5. That is, TPL asserts that if a transfer takes place, it must have been done "in synchrony" with the system clock.[5] For example, on page 29 of Exhibit 13, TPL points to a serial interface as meeting the claim limitation, with the notation: "[i]n order for the microprocessor to read uncorrupted data, the external clock domain must pass the data to the system clock domain in synchrony."

Thus, according to TPL, the mere fact that a data transfer takes place means that the external and internal clocks are "in synchrony". Since Crosby *et al.* show the transfer of data, this limitation is disclosed.

9. Claim 9

The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.

The '567 patent expressly discloses the use of a ring oscillator. *See* Fig. 4; col. 11, ll. 2-7.

10. Claim 10

(a) In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

Please see the analysis and evidence under claim elements 3(b)-(c), above.

[5] Requester opposes this interpretation of the claim.

(b) *providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;*

Please see the analysis and evidence under claim element 1(b) and 1(c), above.

(c) *providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;*

Please see the analysis and evidence under claim element 1(b), above.

(d) *clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;*

Please see the analysis and evidence under claim element 1(b) and 1(c), above.

(e) *connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and*

The CPU and the input/output interface exchange address, data and coupling control signals, as demonstrated by the analysis and evidence cited under claim elements 6(d) and 1(d), above.

(f) *clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.*

Please see the analysis and evidence under claim element 1(e), above.

VII. CONCLUSIONS

In summary, the ideas underlying the claims of the '336 patent had been described in the prior art and even taught to undergraduate students in the late 1970s and early 1980s, years before Mr. Moore and Mr. Fish filed their first application for patent. The most pertinent art was never cited to the Examiner, however. Requester believes that with a full view of the published art, a reasonable Examiner would find there to be a substantial new question of patentability regarding claims of the '336 patent. Requester thus urges that the '336 patent be reexamined.