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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/008,474	01/30/2007	5809336		2845

40972 7590 04/05/2007

HENNEMAN & ASSOCIATES, PLC
714 W. MICHIGAN AVENUE
THREE RIVERS, MI 49093

EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 04/05/2007

Please find below and/or attached an Office communication concerning this application or proceeding.

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(THIRD PARTY REQUESTER'S CORRESPONDENCE ADDRESS)

Daniel B. Ravicher
Public Patent Foundation
1375 Broadway, Suite 600
New York, NY 10018

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. 90/008,474.

PATENT NO. 5809336.

ART UNIT 3992.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Order Granting / D nying R qu st F r Ex Parte R examination	Control No.	Pat nt Under Reexamination	
	90/008,474	5809336	
	Examiner	Art Unit	
	Joseph R. Pokrzywa	3992	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

The request for *ex parte* reexamination filed 30 January 2007 has been considered and a determination has been made. An identification of the claims, the references relied upon, and the rationale supporting the determination are attached.

Attachments: a)☐ PTO-892, b)☒ PTO/SB/08, c)☐ Other: _____

1. ☒ The request for *ex parte* reexamination is GRANTED.

RESPONSE TIMES ARE SET AS FOLLOWS:

For Patent Owner's Statement (Optional): TWO MONTHS from the mailing date of this communication (37 CFR 1.530 (b)). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).**

For Requester's Reply (optional): TWO MONTHS from the **date of service** of any timely filed Patent Owner's Statement (37 CFR 1.535). **NO EXTENSION OF THIS TIME PERIOD IS PERMITTED.** If Patent Owner does not file a timely statement under 37 CFR 1.530(b), then no reply by requester is permitted.

2. ☐ The request for *ex parte* reexamination is DENIED.

This decision is not appealable (35 U.S.C. 303(c)). Requester may seek review by petition to the Commissioner under 37 CFR 1.181 within ONE MONTH from the mailing date of this communication (37 CFR 1.515(c)). **EXTENSION OF TIME TO FILE SUCH A PETITION UNDER 37 CFR 1.181 ARE AVAILABLE ONLY BY PETITION TO SUSPEND OR WAIVE THE REGULATIONS UNDER 37 CFR 1.183.**

In due course, a refund under 37 CFR 1.26 (c) will be made to requester:

a) ☐ by Treasury check or,

b) ☐ by credit to Deposit Account No. _____, or

c) ☐ by credit to a credit card account, unless otherwise notified (35 U.S.C. 303(c)).

Joseph R Pokrzywa

Joseph R. Pokrzywa
Primary Examiner
Art Unit: 3992

cc:Requester (if third party requester)

DETAILED ACTION

Response to Request for *ex parte* Reexamination

1. Reexamination has been requested for claims 1-10 of U.S. Patent Number 5,809,336 ('336 Patent).

2. A substantial new question of patentability affecting claims 1-10 of United States Patent Number 5,809,336 is raised by the request for *ex parte* reexamination.

3. A prior art patent or printed publication raises a substantial new question of patentability where there is:

(A) a substantial likelihood that a reasonable Examiner would consider the prior art patent or printed publication important in deciding whether or not the claim is patentable, MPEP §2242 (I) and,

(B) the same question of patentability as to the claim has not been decided in a previous or pending proceeding or in a final holding of invalidity by a federal court. See MPEP §2242 (III).

4. The '336 Patent is currently assigned to:

Patriot Scientific Corporation

10989 Via Frontera

San Diego, California 92127

5. The '336 Patent application issued on Sep. 15, 1998, with a filing date of Jun. 7, 1995, being a division of U.S. Appl. No. 07/389,334, filed on Aug. 3, 1989, now U.S. Patent No. 5,440,749.

6. The '336 Patent is the subject of the litigation *Technology Properties Limited, Inc. v. Fujitsu Limited et al.*, No. 2:05-CV-00494-TJW, Federal District Court for the Eastern District of Texas, Marshall Division.

Discussion of References

7. In the request for reexamination, the third party requester alleges that the '336 Patent **claims 1-10** are anticipated and/or rendered obvious in light of the following references:

a. U.S. Patent No. 4,691,124, issued to Ledzius *et al.* (hereafter Ledzius)

b. U.S. Patent No. 4,718,081, issued to Brenig (hereafter "Brenig")

c. Mostek Corp., Mostek 1981 3870/F8 Microcomputer Data Book, Feb. 1981, pp. III-76 through III-77, III-100 through III-129 and VI-1 through VI-11 (hereafter "Mostek")

d. Mostek Corp., EDN, Nov. 20, 1976, Advertising (hereafter "EDN")

e. United Technical Publications, IC Master, 1980, pp. 1and 2016-2040 (hereafter "IC Master")

f. U.S. Patent No. 4,710,648, issued to Hanamura *et al.* (hereafter "Hanamura")

g. Guttag, K.M., "The TMS34010: An Embedded Microprocessor", IEEE Micro, Vol. 8, No. 3, pp. 39-52 (1988), published as the May/June 1988 volume (hereafter "Guttag")

h. U.S. Patent No. 4,660,155, issued to Thaden *et al.* (hereafter "Thaden")

i. Hitachi America LTD., 8-bit Single Chip Microcomputer Data Book, July 1985, Table of Contents, pp. 251-279 (hereafter "Hitachi")

j. U.S. Patent No. 4,334,268, issued to Boney et al. (hereafter "Boney")

8. The aforementioned newly cited references are not of record in the file of the '336 Patent and are not cumulative to the art of record in the original file.

9. The prior art reference of Ledzius was previously deemed to raise a substantial new question of patentability in a copending reexamination (90/008,306). Thus, the discussion of the teachings of Ledzius, and the corresponding proposed rejections using Ledzius, which are noted as Ledzius in view of Mostek, Ledzius in view of Guttag, and Ledzius in view of Thaden, would not be considered as raising a substantial *new* question for this request. The references of Guttag and Thaden alone, both teach portions of the limitations, as noted by the Third Party Requester.

However, Guttag and Thaden, alone do not raise a SNQ of patentability to the claims of the '336 Patent.

10. Contrarily, it is agreed that the reference of Mostek would have been considered important by a reasonable examiner in deciding whether or not at least independent **claim 6** was patentable, for the reasons discussed *infra*.

11. Particularly, Mostek teaches of a microprocessor and clock being constructed on the same IC using the same process technology [see pages III-77 and III-105], and that the on-chip oscillator frequency varies due to changes in manufacturing process, supply voltage, and temperature [see page III-118]. With this, Mostek is seen as teaching of a central processing unit disposed upon an integrated circuit substrate, and varying the processing frequency of a first plurality of electronic devices and the clock rate of a second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate. Further Mostek can be interpreted as teaching of an on-chip input/output interface [see page III-105], and an external clock, independent of said oscillator, connected to the input/output interface [see pages III-114 and III-115].

12. Further, it is also agreed that the combination of references of Hitachi and Boney would have been considered important by a reasonable examiner in deciding whether or not at least independent **claim 1** was patentable, for the reasons discussed *infra.*

13. Specifically, Hitachi teaches of an integrated circuit that includes an oscillator entirely on-chip, therein being constructed of the same processing technology, having corresponding manufacturing variations [see pages 251 and 262]. Further Hitachi teaches that the HD6805 chip includes an input/output interface [see page 259] and an external timer, being independent of the ring oscillator variable speed clock [seen as Timer 2 on page 259]. The reference of Boney teaches of utilizing an entire ring oscillator variable speed system clock in a single integrated circuit [see Figs. 1 and 7F, and col. 7, lines 14-23].

14. Thus, the references of Mostek, Hitachi, and Boney, introduced by the Third Party requester, would likely have been important to a reasonable examiner in deciding whether or not the claims were patentable. The above discussed teachings were not present during the prosecution of the application which became the '336 Patent. Thereby, the references raise a substantial new question regarding at least independent claim 1 and/or independent claim 6 of the instant '336 Patent.

Conclusion

15. **Claims 1-10** for U.S. Patent Number 5,809,336 are subject to reexamination.

16. Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that *ex parte* reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extensions of time in *ex parte* reexamination proceedings are provided for in 37 CFR 1.550(c).

17. The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent No. 5,809,336 throughout the course of this reexamination proceeding. The third party requester is also reminded of the ability to similarly apprise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP §§ 2207, 2282 and 2286.

18. ALL correspondence relating to this ex parte reexamination proceeding should be directed as follows:

Please mail any communications to:

Attn: Mail Stop "Ex Parte Reexam"
Central Reexamination Unit
Commissioner for Patents
P. O. Box 1450
Alexandria VA 22313-1450

Please FAX any communications to:

(571) 273-9900
Central Reexamination Unit

Please hand-deliver any communications to:

Customer Service Window
Attn: Central Reexamination Unit
Randolph Building, Lobby Level
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

Signed:

JOSEPH R. POKRZYWA
PRIMARY EXAMINER

Joseph R. Pokrzywa
Central Reexamination Unit 3992
(571) 272-7410

Conferees :

ROLAND G. FOSTER
CRU EXAMINER-AU 3992

RQAS

PTO/SB/57 (04-05)
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also referred to as FORM PTO-1465)

REQUEST FOR *EX PARTE* REEXAMINATION TRANSMITTAL FORM

Address to:
Mail Stop *Ex Parte* Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attorney Docket No.:

Date: January 30, 2007

1. [X] This is a request for *ex parte* reexamination pursuant to 37 CFR 1.510 of patent number 5,809,336 issued September 15, 1998. The request is made by:

[ ] patent owner. [X] third party requester.

64660 U.S. PTO
90008474
01/30/07

2. [X] The name and address of the person requesting reexamination is:

Public Patent Foundation
1375 Broadway, Suite 600
New York, New York 10018

3. [X] a. A check in the amount of $ 2,520.00 is enclosed to cover the reexamination fee, 37 CFR 1.20(c)(1);

[ ] b. The Director is hereby authorized to charge the fee as set forth in 37 CFR 1.20(c)(1) to Deposit Account No. ______ (submit duplicative copy for fee processing); or

[ ] c. Payment by credit card. Form PTO-2038 is attached.

4. [X] Any refund should be made by [X] check or [ ] credit to Deposit Account No.______. 37 CFR 1.26(c). If payment is made by credit card, refund must be to credit card account.

5. [X] A copy of the patent to be reexamined having a double column format on one side of a separate paper is enclosed. 37 CFR 1.510(b)(4)

6. [ ] CD-ROM or CD-R in duplicate, Computer Program (Appendix) or large table
[ ] Landscape Table on CD

7. [ ] Nucleotide and/or Amino Acid Sequence Submission
If applicable, items a. – c. are required.

a. [ ] Computer Readable Form (CRF)
b. Specification Sequence Listing on:

i. [ ] CD-ROM (2 copies) or CD-R (2 copies); or
ii. [ ] paper

c. [ ] Statements verifying identity of above copies

8. [X] A copy of any disclaimer, certificate of correction or reexamination certificate issued in the patent is included.

9. [X] Reexamination of claim(s) 1 - 10 is requested.

10. [X] A copy of every patent or printed publication relied upon is submitted herewith including a listing thereof on Form PTO/SB/08, PTO-1449, or equivalent.

11. [ ] An English language translation of all necessary and pertinent non-English language patents and/or printed publications is included.

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12. [X] The attached detailed request includes at least the following items:

a. A statement identifying each substantial new question of patentability based on prior patents and printed publications. 37 CFR 1.510(b)(1)
b. An identification of every claim for which reexamination is requested, and a detailed explanation of the pertinency and manner of applying the cited art to every claim for which reexamination is requested. 37 CFR 1.510(b)(2)

13. [ ] A proposed amendment is included (only where the patent owner is the requester). 37 CFR 1.510(e)

14. [X] a. It is certified that a copy of this request (if filed by other than the patent owner) has been served in its entirety on the patent owner as provided in 37 CFR 1.33(c).
The name and address of the party served and the date of service are:

Daniel E. Leckrone, Technology Properties Limited
20400 Stevens Creek Blvd., 5th Floor
Cupertino, CA 95014

Drew S. Hamilton,
Knobbe, Martens, Olson & Bear LLP,
550 W.C. St., STE 1200, San Diego, CA 92101

Date of Service: ______________________; or

[ ] b. A duplicate copy is enclosed since service on patent owner was not possible.

15. Correspondence Address: Direct all communication about the reexamination to:

[ ] The address associated with Customer Number: [ ]

OR

[X] Firm or Individual Name	Public Patent Foundation		
Address	1375 Broadway, Suite 600		
City	New York	State New York	Zip 10018
Country	U.S.A.		
Telephone	(212) 796-0570	Email info@pubpat.org	

16. [X] The patent is currently the subject of the following concurrent proceeding(s):
[ ] a. Copending reissue Application No. ______
[X] b. Copending reexamination Control No. 90/008,237 and 90/008,306
[ ] c. Copending Interference No. ______
[X] d. Copending litigation styled:
Technology Properties Limited, Inc. v. Fujitsu Limited, et al.
Case No. 2:05-CV-00494-TJW, U.S. District Court for the Eastern District of Texas, Marshall Division

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Authorized Signature

January 30, 2007
Date

Daniel B. Ravicher
Typed/Printed Name

47,015
Registration No.

[ ] For Patent Owner Requester
[X] For Third Party Requester

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent No: 5,809,336

Patentee: Moore et al.

Serial No.: 08/484,918

Filing Date: June 7, 1995

Issue Date: September 15, 1998

For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

REQUEST FOR *EX PARTE* REEXAMINATION;
REQUESTER'S DETAILED STATEMENT PURSUANT TO 37 C.F.R. §1.510

MS *Ex Parte* Reexamination
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Public Patent Foundation (hereinafter "Requester") is a not-for-profit public service organization that aims to protect the public from the harms caused by undeserved patents and unsound patent policy. Requester, under provisions of 35 U.S.C. 302-307 and 37 C.F.R. § 1.510 *et seq*., requests *ex parte* reexamination of claims 1-10 of United States Patent No. 5,809,336 for

"High Performance Microprocessor Having Variable Speed System Clock," issued September 15, 1998 to Charles H. Moore et al. ("the '336 patent") and presently assigned to Technology Properties Limited, Inc. ("TPL"), in view of substantial new questions of patentability raised against the '336 patent by the prior art submitted with this request.

Pursuant to 35 U.S.C. § 303, Requester respectfully submits that the prior art cited herewith raises substantial new questions of patentability with respect to each of claims 1-10 of the '336 patent. This request for reexamination is based on printed publications that were not presented to nor considered by the Patent Office during examination of the '336 patent. Pursuant to 37 C.F.R. § 1.510(b)(1), Requester provides a statement pointing out each substantial new question of patentability for each claim for which it has requested reexamination. Requester also includes a detailed explanation of the pertinence and manner of applying the cited patents and publications to each identified claim pursuant to 37 C.F.R. § 1.510(b)(2). Under 37 C.F.R. § 1.510(b)(3) and (b)(4), Requester includes copies of the pertinent patents and publications relied upon, and a copy of the entire '336 Patent including the front face, drawings, and specification/claims. Requester also includes the fee for requesting reexamination provided under 37 C.F.R. § 1.20(c)(1).

TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

I. STATEMENT UNDER 37 C.F.R. §1.510(B)(1) POINTING OUT SUBSTANTIAL NEW QUESTIONS OF PATENTABILITY

A. Introduction

Requester respectfully submits that the prior art cited herewith raises substantial new questions of patentability with respect to each of claims 1-10 of the '336 Patent and believes that the '336 Patent warrants reexamination. These questions are summarized in this section I below and discussed in more detail in section II.

B. Summary of the Law Governing Reexamination

1. *Claim interpretation*

In determining whether a "substantial new question of patentability" warrants reexamination, "the PTO must apply the broadest reasonable meaning to the claim language, taking into account any definitions presented in the specification." *In re Bass*, 314 F.3d 575, 577 (Fed. Cir. 2002). Thus, in the analysis and discussion that follows, the identified claims are given their broadest reasonable interpretation consistent with the '336 Patent specification, even though a narrower interpretation may be appropriate in an infringement suit.

Also, during reexamination, no claim is entitled to a presumption of validity; only a preponderance of the evidence is required in order to invalidate a claim during reexamination.[1]

2. *Evidence that may be used in a reexamination*

In addition to patents and printed publications, admissions by a patentee also may be used as evidence to establish a substantial new question of patentability in combination with a patent

[1] *See Xerox Corp. v. 3Com Corp.*, 69 F. Supp. 2d 404, 407 (W.D.N.Y. 1999) ("[I]n a reexamination proceeding before the PTO, there is no presumption of validity and there must only be a preponderance of the evidence to show unpatentability before the PTO may reject the patent claim(s).").

or a printed publication. MPEP §2217. An admission by a patentee may reside in a record created during litigation. *Id.* Such patentee admissions may be relied upon for any matter affecting patentability. 37 C.F.R. §1.104(c)(3). Many such admissions have been made in the specification.

C. Subject Matter Background of the '336 Patent

U.S. Patent No. 5,809,336 to Moore, et. al. ("the '336 Patent") (attached hereto as Appendix I) is titled "High Performance Microprocessor Having Variable Speed System Clock." The parent application leading to the patent was filed on August 3, 1989, and the patent was issued on September 15, 1998. The '336 Patent is directed to methods for clocking microcomputers in order to control operation of the microprocessor and other microcomputer components, and to synchronize communications between the microcomputer and external components.

The patent describes a system in which a single integrated chip includes a microprocessor, an oscillator and an input/output (I/O) interface. The microprocessor is clocked by a clock signal derived from the oscillator, and the input/output (I/O) interface is clocked, at least in part, from a different clock source. Some claims require that the oscillator is a ring oscillator. The oscillator is constructed on the same integrated chip and realized with the same type of processing and layout as is used for the processor. Because of this, as the patentee disclosed in the '336 Patent specification and argued during the previous examination, the process variations which affect the processor's speed capability will be matched by variations in the frequency of the clock signal derived from the ring oscillator. For example, when the process characteristics provide a processor capable of operating at a higher than average frequency, the clock frequency produced by the ring oscillator will also be higher.

During the previous examination of the '336 Patent, the patentee argued that when the microprocessor and oscillator are constructed on the same integrated circuit of the same process technology, their frequencies inherently vary together with changes in various parameters:

> The placement of [the clock and the microprocessor] within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, since <u>the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters</u> (e.g., temperature) affecting performance. ('336 Patent Prosecution History, Paper 6, Exhibit 1, p. 8, ¶ 2, *emphasis added*) ("*Paper 6*").

The patentee argued that the oscillator and processor frequencies "<u>automatically varying together</u>", which occurs "since <u>both the oscillator...and driven device are on the same substrate</u>", is "crucial to the present invention," and "<u>differs from all cited references</u>." ('336 Patent Prosecution History, Paper 12, Exhibit 2, p. 5, ¶ 1, *emphasis added*) ("*Paper 12*"). The patentee distinguished references, such as the *Magar* reference, that have the oscillator frequency determined by external components because the oscillator and processor frequencies "would inherently not vary due to variations in [parameters] in the same way...as claimed." (*Id.* at p. 4, ¶ 2).

D. Notice of Pending Litigation Involving the '336 Patent

Requester is aware that U.S. Pat. No. 5,809,336 is being asserted by Technology Properties Limited, Inc. and Patriot Scientific Corp. before the U.S. District Court for the Eastern District of Texas in the case styled:

Technology Properties Limited, Inc. v. Fujitsu Limited, et al., Case No. 2:05-cv-00494-TJW, U.S. District Court for the Eastern District of Texas;, Marshall Division.

E. A substantial new question of patentability as to claims 1-10 is raised by *Ledzius* in light of *Mostek*, as further evidenced by prior prosecution correspondences, *Paper 6* and *Paper 12*.[2]

U.S. Patent No. 4,691,124 to Ledzius, et al. ("*Ledzius*"), entitled "Self-Compensating, Maximum Speed Integrated Circuit," was filed on May 16, 1986, and issued on September 1, 1987. The *Mostek 1981 3870/F8 Microcomputer Data Book* ("*Mostek*") describes the 3870 Single Chip family of microcomputers manufactured by Mostek Corp., including the MK3873 chip. The data book was published in February 1981. Neither *Ledzius* nor *Mostek* was cited during the previous examination, and both references are prior art under 35 U.S.C. 102(b) and 103(a).

Ledzius in light of *Mostek* discloses all elements of claims 1-10. In general, both *Ledzius* and *Mostek* disclose an integrated circuit that contains a processor clocked by an on-chip ring oscillator and input/output interfaces that can be clocked by an external clock for interfacing asynchronously with external components, such as external memory.

In particular, both references disclose features not disclosed by any reference considered during the previous examination. As discussed in section C above, during prosecution of the '336 patent, the applicant argued that because the claimed oscillator and processor are on the same integrated circuit, their frequencies will inherently vary together due to changes in various parameters, and that this is "crucial to the present invention" and "differs from all cited references." (*Paper 6*; *Paper 12*, emphasis added). *Ledzius* discloses a ring oscillator,

[2] In accord with MPEP § 2131.01, prior prosecution correspondences, *Paper 6* and *Paper 12* are provided to show that it is inherent that the discussed frequenies would vary together and that one skilled in the art in 1989 would know of the inherency.

microprocessor and input/output interface on the same IC, where the oscillator and processor frequencies vary together with changes in various parameters. *Mostek* too discloses an oscillator, microprocessor and input/output interface on the same IC with the interface clocked by an external clock. Requester believes that a reasonable examiner would consider these teachings important, perhaps "crucial", in determining whether claims 1-10 of the '336 patent are patentable. Therefore, the teachings raise a substantial new question of patentability with respect to claims 1-10.

F. A substantial new question of patentability as to claims 1-10 is raised by *Mostek*.

As discussed in section E above, *Mostek* is prior art under 35 U.S.C. 102(b) and 103(a), and discloses, either expressly or inherently, or renders obvious all elements of the claims, including features not disclosed by any reference considered during the previous examination, such as a ring oscillator, microprocessor and input/output interface on the same IC, where the oscillator and processor frequencies vary together with changes in various parameters and the interface is clocked by an external clock. Requester believes that a reasonable examiner would consider these teachings important in determining whether claims 1-10 of the'336 patent are patentable, and they raise a substantial new question of patentability with respect to claims 1-10.

G. A substantial new question of patentability as to claims 1-10 is raised by *Ledzius* in light of *Guttag*.

A technical article by Guttag, et al., entitled "The TMS34010: An Embedded Microprocessor" ("*Guttag*"), was published in the May/June 1988 volume of the IEEE Micro journal. *Guttag* describes the structure and operation of the TMS34010 microprocessor chip, which can be used as an input/output interface between a host microprocessor and memory that is local to the interface. The reference was not cited during the previous examination and is prior art under 35 U.S.C. 102(b) and 103(a).

Ledzius, with *Guttag*, discloses all elements of the claims, including features not disclosed by any reference considered during the previous examination, such as an oscillator, microprocessor and input/output interface on the same IC with the interface clocked in part by the processor's clock and in part by an external clock. Requester believes that a reasonable examiner would consider these teachings important in determining whether claims 1-10 of the '336 patent are patentable, and they raise a substantial new question of patentability with respect to claims 1-10.

H. A substantial new question of patentability as to claims 1-10 is raised by *Ledzius* in light of *Thaden*.

U.S. Patent No. 4,660,155 to Thaden, et al. ("*Thaden*"), entitled "Single Chip Video System With Separate Clocks For Memory Controller, CRT Controller," was filed on July 23, 1984 and issued on April 21, 1987. *Thaden* describes an interface between a microprocessor and video circuitry, including memory. The reference was not cited during the previous examination and is prior art under 35 U.S.C. 102(b) and 103(a).

Ledzius, with *Thaden*, discloses all elements of the claims, including features not disclosed by any reference considered during the previous examination, such as an oscillator, microprocessor and input/output interface on the same IC with the interface clocked in part by the processor's clock and in part by an external clock. Requester believes that a reasonable examiner would consider these teachings important in determining whether claims 1-10 of the '336 patent are patentable, and they raise a substantial new question of patentability with respect to claims 1-10.

I. A substantial new question of patentability as to claims 1-5 is raised by *Hitachi* in light of *Boney*.

The *8-Bit Single-Chip Microcomputer Data Book* ("*Hitachi*") was published in July 1985 by Hitachi Corp. U.S. Patent No. 4,334,268 to Boney, et al. ("*Boney*"), entitled "Microcomputer With Branch On Bit Set/Clear Instructions," was filed on May 1, 1979 and issued on June 8, 1982. *Hitachi* describes the HD6800 family of microcomputer chips, including the HD6805W1 integrated circuit chip. *Boney* also describes a single-chip microcomputer. Neither reference was cited during the previous examination, and both references are prior art under 35 U.S.C. 102(b) and 103(a).

Hitachi, with *Boney*, discloses all elements of the claims, including features not disclosed by any reference considered during the previous examination, such as a ring oscillator, microprocessor and input/output interface on the same IC with the interface clocked in part by the processor's clock and in part by an external clock. Requester believes that a reasonable examiner would consider these teachings important in determining whether claims 1-5 of the '336 patent are patentable, and they raise a substantial new question of patentability with respect to claims 1-5.

II. DETAILED EXPLANATION UNDER 37 C.F.R. §1.510(B)(2) OF THE PERTINENCY AND MANNER OF APPLYING THE CITED PRIOR ART TO EVERY CLAIM FOR WHICH REEXAMINATION IS REQUESTED

A. Cited References

A copy of every patent or publication relied upon or referred to is attached as listed below and is cited in the attached modified Form PTO/SB/42.

Exhibit 1 Moore, et al., Prosecution History for U.S. Patent No. 5,809,336, Paper 6, Apr. 11, 1996 Amendment, pp. 1-10, ("*Paper 6*");

Exhibit 2 Moore, et al., Prosecution History for U.S. Patent No. 5,809,336, Paper 12, July 3, 1997 Amendment, pp. 1-5, ("*Paper 12*");

Exhibit 3 Ledzius, et al., U.S. Patent No. 4,691,124, "Self-Compensating, Maximum Speed Integrated Circuit," filed on May 16, 1986 and issued on September 1, 1987, ("*Ledzius*");

Exhibit 4 Brenig, U.S. Patent No. 4,718,081, " Method and apparatus for reducing handoff errors in a cellular radio telephone communications system," filed on November 13, 1986 and issued on January 5, 1988, ("*Brenig*");

Exhibit 5 Mostek Corp., Mostek 1981 3870/F8 Microcomputer Data Book, Feb. 1981, pp. III-76 through III-77, III-100 through III-129 and VI-1 through VI-11("*Mostek*");

Exhibit 6 Mostek Corp., *EDN*, Nov. 20, 1976, Advertising, ("*EDN*");

Exhibit 7 United Technical Publications, *IC Master*, 1980, pp. 1 and 2016-2040, ("*IC Master*");

Exhibit 8 Hanamura, et al., U.S. Patent No. 4,710,648, " Semiconductor Including Signal Processor And Transient Detector For Low Temperature Operation," filed May 6, 1985, issued December 1, 1987, ("*Hanamura*");

Exhibit 9 Guttag, K. M., "The TMS34010: An Embedded Microprocessor," IEEE Micro, Vol. 8, No. 3, pp. 39-52 (1988), published as the May/June 1988 volume, ("*Guttag*");

Exhibit 10 Thaden, et al., U.S. Patent No. 4,660,155, "Single Chip Video System With Separate Clocks For Memory Controller, CRT Controller," filed July 23, 1984, issued April 21, 1987, ("*Thaden*");

Exhibit 11 Hitachi America Ltd., 8-Bit Single-Chip Microcomputer Data Book, July 1985, Table of Contents, pp. 251-279, ("*Hitachi*"); and

Exhibit 12 Boney, et al., U.S. Patent No. 4,334,268, "Microcomputer With Branch On Bit Set/Clear Instructions," filed May 1, 1979, issued June 8, 1982, ("*Boney*").

Additionally, Appendix I is a copy of the patent to be reexamined, U.S. Patent No. 5,809,336 to Moore, et al., in double column format.

B. Claims 1-10 are obvious over *Ledzius* in light of *Mostek*, as further evidenced by *Brenig* and prior prosecution correspondences, *Paper 6* and *Paper 12*.[3]

Ledzius, alone, arguably discloses all elements of claims 1-10 and therefore anticipates the claims. However, in any event, all elements of claims 1-10 would at least have been obvious to one of ordinary skill in 1989 over *Ledzius* in light of *Mostek* and the knowledge of one skilled in the art in 1989 as shown in *Brenig* (U.S. Patent No. 4,718,081, filed on November 13, 1986 and issued on January 5, 1988).

1. *Claim 1*

(a) *A microprocessor system, comprising a single integrated circuit including a central processing unit*

Ledzius discloses an integrated circuit (IC) 10 that includes a microprocessor system that has a central processing unit, "functional circuit 16." (Exhibit 3, Fig. 1 (shown in section B(1)(b), below); 2:28-31; 4:5-7). Functional circuit 16 is a processor that performs "a relatively large quantity of arithmetic operations on initial data" for "any of a wide variety of diverse tasks," including digital signal processing or cryptographic algorithms. (2:32-38; 2:43-54). It would have been obvious to one of ordinary skill in 1989 that the disclosed digital signal processor was commonly implemented as a programmable microprocessor. (*See*, e.g., *Brenig* (Exhibit 4) at 5:64-67 ("[c]ell site controller 26 may be any conventional digital signal processor, and preferably includes a central processing unit.")). As discussed in section C below, *Mostek* also discloses a single integrated circuit with a CPU.

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3 In accord with MPEP § 2131.01, prior prosecution correspondences, *Paper 6* and *Paper 12* are provided to show that it is inherent that the discussed frequenies would vary together and that one skilled in the art in 1989 would know of the inherency. Similarly, the Brenig reference is provided to show that a digital signal processor is commonly implemented as a microprocessor.

(b) ***and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,***

Ledzius discloses an "integrated circuit 10" that includes an entire ring oscillator, "clock generator 18", and a central processing unit, "functional circuit 16." (Fig. 1; 1:65-68; *also* 2:28-31; 4:5-7; Abstract) The oscillator is complete and operates "without communication or interference from other ICs or devices." (2:33-40; *also* 4:22-23; 5:53-58; 6:63-65) The oscillator has a variable speed: "[t]he frequency of the clock signal produced by clock generator 18 varies...." (4:5-21).

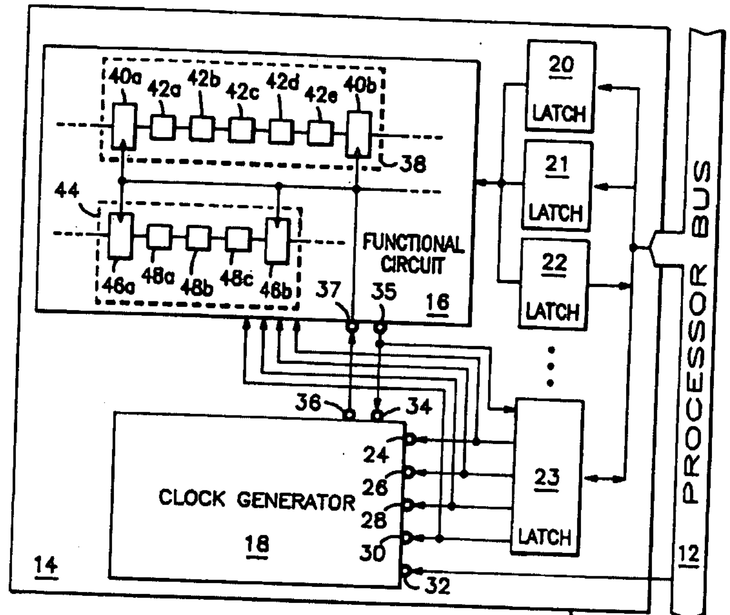


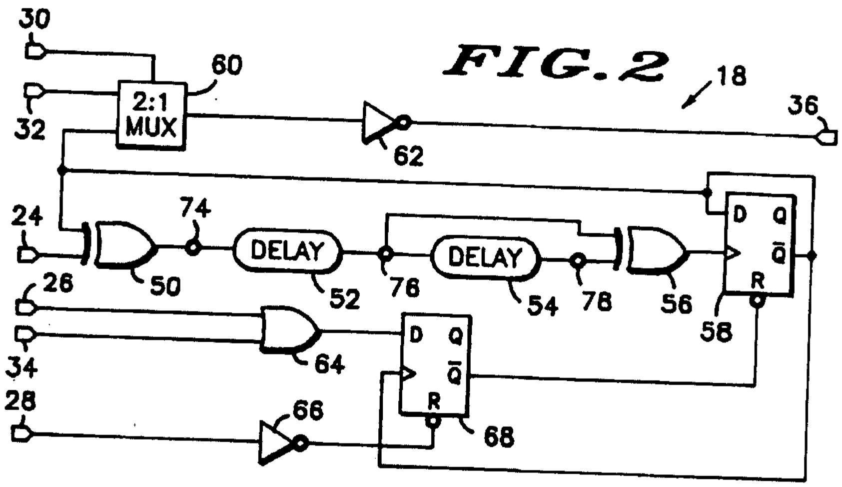
FIG. 1

Ledzius teaches that the on-chip oscillator clocks the processor: "signal 58' [becoming signal 36 in Figs. 1 and 2] represents the clock which drives functional circuit 16 (see FIG. 1)." (5:56-58; *also* 1:53-56; 1:65-68; 2:58-60; 4:22-23; and Figs. 1-2). Additionally, as discussed in section C below, *Mostek*, Exhibit 5, discloses that the single IC, with a CPU, also has an entire on-chip oscillator connected to drive the CPU with a varying frequency.

Ledzius discloses that the on-chip clock includes a ring oscillator. Although a common configuration, the meaning of "ring oscillator" should not be limited to having only inverters connected in a loop. It should be reasonably construed to include any cascade of delay elements connected in a circular circuit path that provides unstable feedback (signals that cause the elements to switch from their previous state) to generate a clock signal. *Ledzius* discloses a

"Clock generator 18" that includes three logic components, 50, 56 and 58, and two additional delays, 52 and 54, connected in a circular circuit path to provide an unstable feedback that generates clock signal 58'. (Figs. 2-3; 4:50-5:60)

FIG. 2



The circuit of Figure 2 also contains additional controls that allow the microprocessor to start or stop the oscillation. When a "run" signal is applied to pin 24, gate 50 acts as an inverter. (4:65-5:9) When a "reset" signal is removed from pin 28 and signal 56' rises, flip-flop 58 inverts its output. (Figs. 2-3; 4:65-5:49). The signal circulation "continues indefinitely until an external event [such as a "reset" signal or a "run" signal] happens to stop signal 58' from changing states in the prescribed manner." (5:53-54). Alternatively, the ring oscillator can be allowed to "free-run," without start or stop control. (6:63-65).

(c) ***said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;***

Ledzius discloses that the clock and processor each include electronic devices constructed of the same process technology and having the same manufacturing variations. They vary together in frequency due to manufacturing and temperature variations:

> <u>Since</u> both clock generator 18 and functional circuit 16 are constructed on substrate 14, <u>clock generator 18 compensates for temperature and process caused variations in the true maximum speed of the functional circuit 16</u>. The frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances. Accordingly, process caused variations are compensated because clock generator 18 is always physically made from the same batch and section of a semiconductor wafer as functional circuit 16. <u>Slowest signal path 38 of functional circuit 16 controls the true maximum speed. Accordingly, process variations which affect slowest path 38 also affect clock generator 18</u>. (4:5-21, *emphasis added*).

It is inherent, and would have been obvious to one of ordinary skill in 1989, that the processor and clock frequencies, which are designed to vary together as described above, will also vary together due to variation in the common supply voltage.

Also, as discussed in section I(C) above, during prosecution of the '336 Patent, the patentee argued that they inherently vary together with changes in various parameters:

> The placement of [the clock and the microprocessor] within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, since <u>the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters</u> (e.g., temperature) <u>affecting performance</u>. ('336 Patent Prosecution History, *Paper 6*, p. 8, ¶ 2; see also *Paper 12*, p. 5, ¶ 1).

It would have been obvious to one of ordinary skill in the art in 1989 that one of the "parameters affecting [circuit] performance" would be the supply voltage. Additionally, as discussed in section C below, *Mostek* also teaches that for the microcomputers of the 3870 family, the microprocessor and clock are constructed on the same IC using the same process technology and that the on-chip oscillator frequency varies due to changes in manufacturing process, supply voltage and temperature. Therefore, in accord with the discussion above, it is inherent that the clock and microprocessor frequencies vary together due to these changes.

(d) ***an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;***

Ledzius discloses an on-chip input/output interface (latches 20-22) that passes data, addresses and coupling control signals between the processor and an external bus. (Fig. 1; 3:31-53 ("...Latch 22 represents an output port in which functional circuit 16 stores data..."; "Latch 23 represents a status/control interface between clock generator 18 and functional circuit 16 on one side and processor bus 12 on the other"); 3:54-63 ("...signals may couple to processor bus 12 through latch 23 to communicate information about error conditions."); 2:29-32; 2:26-29 ("Processor bus 12 includes conventional address, data and control lines as may be required for a processor (not shown) to successfully communicate with IC 10.").

Also, *Ledzius* <u>explicitly suggests</u> using a different input/output interface in place of latches 20-23. "Those skilled in the art can...use alternate methods for interfacing between processor bus 12 and an asynchronously operating functional circuit 16." (6:63-67). *Mostek* discloses an on-chip input/output interface as part of <u>a solution for the same problem</u> that *Ledzius* is directed to, which is providing asynchronous operation of a processor and external devices, such as external memory. (*Ledzius* at 1:57-59 (Summary of the Invention); *Mostek*,

Exhibit 5 at p. III-102, col. 1,¶ 1). Therefore, given the similarity of feature and function, it would have been obvious to one skilled in the art of 1989 to combine the teachings of *Mostek* and *Ledzius* to apply *Mostek's* input/output interface in place of the interface of *Ledzius*.

Specifically, *Mostek* discloses an on-chip input/output interface connected between the central processing unit and an external memory bus: "The Serial Input/Output Port....provide[s] the MK3873 with a half duplex asynchronous or a full duplex synchronous, variable bit length serial port." (p. III-105, Serial I/O Operation). "The serial port...could be used...as an interface to external serial logic or serial memory devices." (p. III-102, col. 1,¶ 1).

The Serial Port interface is connected to exchange control, address and data information: Control information is received and placed in the "Serial Port Control Register." (p. III-107, "Port D Serial Port Control Register" section; p. III-111, col. 2, ¶ 2). ("Note that if <u>a new control word is written to port D</u>...the bit count will be reset"). "Data is shifted into or out of the shift register at a rate determined by the internal baud rate generator or external clock." (p. III-105, "Serial I/O Operation" section). Also, it is inherent that the serial port interface exchanges address information because *Mostek* discloses that "[t]he serial port...could be used...as an interface to external...<u>memory</u> devices," which would require <u>address</u> information. (p. III-102, col. 1,¶1).

(e) ***and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.***

Mostek discloses that the on-chip input/output interface is connected to and clocked by a second, external clock: "Data is shifted into or out of the [Serial Port's] shift register at a rate determined by the internal baud rate generator or <u>external clock</u>." (p. III-102, col. 1,¶1; p. III-105, Serial I/O Operation section). "If all zeros are loaded into this [Baud Rate Control] port, the

External Clock mode is selected....Any TTL compatible square wave input can be used to generate the clock for the serial port." (p. III-110, ¶ 2 and Fig. 8, "External Clock Mode"). "Sync data transmission carries the clock with the data. [For example,] modems normally manage the clocking...." (p. VI-4, "MK3873 Application Note", col. 1, SYNC, ¶ 1).

The second clock frequency disclosed in *Mostek* is inherently independent of the on-chip clock frequency because "...[in] the External Clock mode....Any TTL compatible square wave input can be used to generate the clock for the serial port" and the second (serial port) clock has no connection to the on-chip clock. (p. III-110, ¶ 2, emphasis added). Furthermore, it would have been obvious to one of ordinary skill in 1989 that the two frequencies would be independent because, while the on-chip clock has a variable frequency, the serial port interface, which exchanges data with external devices, requires standardized (fixed) baud rates.

Because the combination of *Ledzius* and *Mostek* renders all elements of claim 1 obvious to one of ordinary skill in 1989 and it would have been obvious to combine their teachings, claim 1 is unpatentable. The claim elements and cited references discussed above are summarized in the table below.

'336 Patent Claim 1	**Cited References**
A microprocessor system, comprising a single integrated circuit including a central processing unit and	*Ledzius*: Fig. 1; 2:28-38; 2:43-54; 4:5-7. *Brenig*: 5:64-67.
an entire ring oscillator variable speed system clock in said single integrated circuit and	*Ledzius*: Fig. 1; 1:65-68; *also* 2:28-40; 4:5-7; Abstract; *also* 4:22-23; 5:53-58; 6:63-65 (entire on-chip oscillator). *Ledzius*: 4:5-21 (variable speed clock).

	Ledzius: Figs. 2-3; 4:50-5:60; 6:63-65 (ring oscillator)
Connected to said central processing unit for clocking said central processing unit,	*Ledzius*: 5:56-58; and Figs. 1-2; *also* 1:53-56; 1:65-68; 2:58-60; 4:22-23.
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	*Ledzius*: 4:5-21 (the same process technology and corresponding manufacturing variations)
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	*Ledzius*: 4:5-21. *Paper 6*, p. 8, ¶.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and	*Ledzius*: Fig. 1; 3:31-53; 3:54-63; 2:29-32; 2:26-29 (interface exchanging control, address and data signals with the processor). *Ledzius*: 6:63-67; 1:57-59 (combining references). *Mostek*: p. III-105, Serial I/O Operation section; p. III-102, col. 1,¶ 1; p. III-107, "Port D Serial Port Control Register" section; p. III-111, col. 2, ¶ 2 (interface exchanging control and data signals with the processor). *Mostek*: p. III-102, col. 1,¶1 (interface exchanging addresses with the processor).
a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	*Mostek*: p. III-102, col. 1,¶1; p. III-105, Serial I/O Operation section; p. III-110, ¶ 2 and Fig. 8, "External Clock Mode"; p. VI-4, "MK3873 Application Note", col. 1, SYNC, ¶ 1 (second clock connected to the interface). *Mostek*: p. III-110, ¶ 2 (second clock independent).

2. *Claim 2*

The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.

The claimed "fixed-frequency clock" should be reasonably construed to mean an external clock that has a frequency fixed by its source and not share the frequency variations of the on-chip clock. It is inherent that all clock sources vary in frequency to some extent. The '336 Patent Specification does not discuss the meaning of "fixed frequency." The Specification only contrasts "fixed frequency" with the variable frequency of the on-chip clock. (17:32-34).

It is inherent that the second clock disclosed by *Mostek*, which has no connection to the on-chip clock, has its frequency fixed by its source and does not share the frequency variations of the on-chip clock.

Therefore, considering also the discussion of claim 1 above, the combination of *Ledzius* and *Mostek* renders all elements of claim 2 obvious to one of ordinary skill in 1989, and claim 2 should be rejected.

3. *Claim 3*

(a) ***In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:***

Ledzius discloses an integrated circuit (IC)10 that includes a microprocessor and a method for clocking the microprocessor, as discussed in sections B(1)(a) and (b) above.

(b) ***providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;***

Ledzius discloses that IC 10 includes an entire ring oscillator and that the on-chip oscillator and microprocessor vary together in frequency because they include electronic devices with operating characteristics that vary together with variations in manufacturing and operating characteristics, as discussed in sections B(1)(b) and (c) above.

(c) ***using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;***

Ledzius discloses using the ring oscillator for clocking the microprocessor at a variable frequency, as discussed in section B(1)(b) above.

(d) ***providing an on chip input/output interface for the microprocessor integrated circuit; and***

As discussed in section B(1)(d) above, *Ledzius* discloses an on-chip input/output interface (latches 20-22) that passes data, addresses and coupling control signals between the processor and an external bus. Also, it would have been obvious to one skilled in the art in 1989 to combine the teachings of *Mostek* and *Ledzius* to apply *Mostek's* input/output interface as the interface of *Ledzius.*

(e) ***clocking the input/output interface with a second clock independent of the ring oscillator system clock.***

Mostek discloses that the on-chip input/output interface is connected to and clocked by a second, external clock, and that the external clock can be independent of the on-chip system clock, as discussed in section B(1)(e) above.

Because the combination of *Ledzius* and *Mostek* renders every element of claim 3 obvious to one of ordinary skill in 1989 and it would have been obvious to combine their teachings, claim 3 is unpatentable.

4. *Claim 4*

The method of claim 3 in which the second clock is a fixed frequency clock.

Mostek discloses that the second clock has a fixed frequency, as discussed in section B(2) above. Therefore, considering also the discussion of claim 3 above, the combination of *Ledzius* and *Mostek* renders all elements of claim 4 obvious to one of ordinary skill in 1989, and claim 4 should be rejected.

5. *Claim 5*

The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock

Mostek discloses that information can be transferred between the microprocessor and the input/output interface in synchrony with the on-chip clock. The '336 Patent Specification does not define "in synchrony with said ring oscillator." (*E.g.*, 17:12-27). However, the patentee's remarks during prosecution of the '336 Patent indicate that the I/O interface transfers data to and from the CPU with a timing set by the on-chip clock. "...information is <u>transferred to and from the microprocessor in synchrony with the ring oscillator clock</u>, and that this information is [then] buffered to facilitate transfer to and from system memory...." ('336 Patent Prosecution, *Paper 6*, Apr. 11, 1996 at 9-10, *emphasis added*).

Mostek discloses the above described configuration, in which the I/O interface is buffered by a FIFO buffer that "is often used to connect two asynchronous processes....The [external] sender transmits at its own rate, which may be quite sporadic....The [CPU's] protocol handler takes characters out the other end of the FIFO buffer at its own rate...." (p. VI-8, "MK3873 Application Note," col. 2, "FIFO Buffering", ¶ 3 (*emphasis added*); *see also* p. III-105, col. 2, ¶ 3 and p. III-107, Fig. 5A (further discussion of the double-buffered ports E and F for exchanging information with the CPU)).

Thus, considering also the discussion of claim 3 above, claim 5 should be rejected as being obvious over *Ledzius* in light of *Mostek.*

6. ***Claim 6***

(a) ***A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;***

Ledzius discloses an integrated circuit (IC) 10 that includes a microprocessor system, with a central processing unit, that operates at a frequency and is constructed of electronic devices, as discussed in sections B(1)(a) and (c) above.

(b) ***an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,***

Ledzius discloses that IC 10 also includes an entire oscillator, that the oscillator is constructed of electronic devices, and that it is used for clocking the microprocessor, as discussed in section B(1)(b) above.

(c) ***thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;***

Ledzius discloses using the ring oscillator for clocking the microprocessor at a variable frequency, as discussed in section B(1)(b) above. *Ledzius* discloses that the on-chip oscillator and microprocessor vary together in frequency because they include electronic devices with operating characteristics that vary together with variations in manufacturing and operating characteristics, as discussed in section B(1)(c) above.

(d) ***an on-chip input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and***

As discussed in section B(1)(d) above, *Ledzius* discloses an on-chip input/output interface, latches 20-22, that is connected to pass data, addresses and coupling control signals between the functional circuit and an external bus. *Ledzius* also suggests using a different input/output interface in place of latches 20-22, and *Mostek* discloses an on-chip input/output interface connected between the central processing unit and an external memory bus to exchange coupling control signals, addresses and data with the CPU.

(e) ***an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.***

Mostek discloses that the on-chip input/output interface is connected to and clocked by a second, external clock, and it is inherent that the external clock is independent of the on-chip system clock, as discussed in section B(1)(e) above.

Because the combination of *Ledzius* and *Mostek* renders all elements of claim 6 obvious to one of ordinary skill in 1989 and it would have been obvious to combine their teachings, claim 6 is unpatentable.

7. *Claim 7*

The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

Ledzius discloses that the on-chip oscillator and microprocessor vary together in frequency due to variations in temperature, as discussed in section B(1)(c) above. Therefore, considering also the discussion of claim 6 above, the combination of *Ledzius* and *Mostek* renders all elements of claim 7 obvious to one of ordinary skill in 1989, and claim 7 should be rejected.

8. *Claim 8*

The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.

As discussed in section B(2) above, the second clock disclosed by *Mostek* has its frequency fixed by its source and does not share the frequency variations of the on-chip clock.

As discussed below, claim 8 may be indefinite, but the most nearly reasonable construction of claim 8 would be anticipated by *Mostek*, which discloses that the external clock may operate synchronously with external devices.

Claim 8 may be invalid under 35 U.S.C. § 112, ¶ 2, as being indefinite because the claim limitation, "operates synchronously relative to said [on-chip] oscillator," is mutually exclusive of requirements of parent-claim 6 or is not understandable in light of those requirements.[4]

Alternatively, the limitation might be construed to mean operating in synchrony with external components, rather than being in synchrony with the on-chip oscillator. The '336 Patent Specification does not explicitly define what is meant by "synchronously relative to said oscillator."

However, the Specification teaches that "[t]he microprocessor 50 provides a dual-clock scheme...with the CPU 70 operating [asynchronously] to I/O interface 432...and the I/O interface 432 operating synchronously with the external world of memory and I/O devices." (17:14-19). During prosecution of the '336 Patent, the patentee explained that "information is transferred to and from the microprocessor in synchrony with the ring oscillator clock, and that this information is buffered to facilitate transfer to and from [external] system memory synchronously...." ('336 Patent Prosecution, *Paper 6*, Apr. 11, 1996 at 9-10).

4 Claim 6 recites a variable-rate on-chip oscillator and also an external clock. The external clock is "independent of said oscillator [and]...operative at a frequency independent of a clock frequency of said oscillator." Dependent claim 8 adds that the external clock is a "fixed frequency clock."

However, claim 8 also recites that the "external clock...operates synchronously relative to said [on-chip] oscillator" (emphasis added). It is inherent, and would have been obvious to one of ordinary skill in 1989, that two oscillators used in microprocessor systems cannot be both independent of each other, with independent frequencies, one frequency varying and the other fixed, and still operate synchronously to each other.

As discussed in section B(1)(e) above, *Mostek* discloses that the serial input/output interface can transfer data out of the chip clocked by an external clock. As discussed in section B(5) above, *Mostek* also discloses that the external clock can be asynchronous with the on-chip clock and in synchrony with external components. As an alternative, *Mostek* discloses that the external clock could be in synchrony with the on-chip oscillator because when the serial port is in the "External Clock mode", "Any TTL compatible square wave input can be used to generate the clock for the serial port." (p. III-110, col. 1, ¶ 2 and Fig. 8, "External Clock Mode").

Therefore, considering also the discussion of claim 6 above, the combination of *Ledzius* and *Mostek* renders all elements of claim 8 obvious to one of ordinary skill in 1989, and claim 8 should be rejected.

9. *Claim 9*

The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.

Ledzius discloses that the on-chip oscillator is a ring oscillator, as discussed in section B(1)(b) above. Thus, considering also the discussion of claim 6 above, claim 8 should be rejected as being obvious over *Ledzius* in light of *Mostek*.

10. *Claim 10*

(a) ***In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of: providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;***

Ledzius discloses an integrated circuit (IC) 10 that includes a microprocessor system, with a central processing unit that operates at a frequency and is constructed of electronic devices, as discussed in sections B(1)(a) and (c) above. It is inherent, and would have been obvious to one of ordinary skill in 1989, that a CPU constructed on an IC would be constructed of transistors. *Ledzius* also discloses a method for clocking the central processing unit as discussed in section B(1)(b) above.

(b) ***providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;***

Ledzius discloses that IC 10 also includes an entire variable speed clock, as discussed in section B(1)(b) above. *Ledzius* discloses that the on-chip clock is constructed of electronic devices, as discussed in section B(1)(c) above. It is inherent, and would have been obvious to one of ordinary skill in 1989, that the on-chip clock would be constructed of transistors.

(c) ***clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;***

Ledzius discloses using the ring oscillator for clocking the microprocessor at a variable frequency, as discussed in section B(1)(b) above. *Ledzius* also discloses that the on-chip oscillator and microprocessor, constructed on the same IC, vary together in frequency with IC fabrication or operating parameters, as discussed in section B(1)(c) above.

(d) ***connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and***

As discussed in section B(1)(d) above, *Ledzius* discloses an on-chip input/output interface, latches 20-22, that is connected to pass data and coupling control signals between the functional circuit and an external bus. *Ledzius* also suggests using a different input/output interface in place of latches 20-22. *Mostek* discloses an on-chip input/output interface connected between the central processing unit and an external memory bus to exchange coupling control signals, addresses and data with the CPU.

(e) ***clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.***

Mostek discloses that the on-chip input/output interface is connected to and clocked by a second, external clock, and that the external clock can be independent of the on-chip system clock, as discussed in section B(1)(e) above.

Because the combination of *Ledzius* and *Mostek* renders all elements of claim 10 obvious to one of ordinary skill in 1989 and it would have been obvious to combine their teachings, claim 10 is unpatentable.

C. Claims 1-10 are obvious over *Mostek*, and claims 6-8 and 10 are anticipated by *Mostek*, as further evidenced by *EDN*, *IC Master* and *Hanamura* and prior prosecution correspondences, *Paper 6* and *Paper 12*.[5]

All elements of claims 1-10 would have been obvious to one of ordinary skill in the art in 1989 in light of *Mostek*. Also, all elements of claims 6-8 and 10 are disclosed either expressly or inherently in *Mostek*.

1. *Claim 1*

(a) *A microprocessor system, comprising a single integrated circuit including a central processing unit*

Mostek discloses an integrated circuit (IC) that includes a microprocessor system, with a central processing unit. (p. III-102, col. 1, ¶ 1; p. III-103, Fig. 1).

(b) *and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,*

Mostek teaches that the integrated circuit includes an entire on-chip oscillator that clocks the central processing unit: "The 3873 contains an on-chip oscillator circuit which provides an internal clock." (p. III-114, col. 2, "3873 TIME BASE OPTIONS"; *see also* p. III-102, col. 2, ¶ 6; p. III-103, Fig. 1; p. III-115, cols. 1-2).

In the section entitled, 3873 TIME BASE OPTIONS, cited above, *Mostek* explicitly discusses only clock modes that require external components. However, as discussed below, it is inherent, and also would have been obvious to one of ordinary skill in the art in 1989, that the MK3870 may be used with only its internal oscillator and without external components. *Mostek*

[5] In accord with MPEP § 2131.01, the *EDN* and *IC Master* references are provided to show that the oscillator, discussed in section (b) ¶ 2 below, which is entirely on-chip, is inherent in the MK3870 family of microcomputers, including the MK3873. The *EDN* and *IC Master* references also show that one skilled in the art in 1989 would know of the inherency. Similarly, the Hanamura reference is provided to show that it was well known in 1989 to use a ring oscillator as an oscillator on an integrated circuit.

shows this by disclosing that "the architecture of the MK3873 is identical to that of the rest of the devices in the 3870 family, with the exception [that the MK3873 also has a] serial port logic." (p. III-102, col. 2, "MK3873 Architecture"). The 3870 family architecture includes an "Internal time base" clock option that uses "no external components," as discussed in, for example, advertisement of the MK3870 microprocessor chips. (*EDN*, Exhibit 6, p. 2, MK 3870-F8/1 Features). As another example, the IC Master book ("*IC Master*") discusses operation of the on-chip clocks in the 3870 chips without external components.

> The time base for the 3870 may originate from one of five sources. There are four external and one internal mode. If both XTL1 and XTL2 are grounded, the 3870 will activate its internal oscillator.

(*IC Master*, Exhibit 7, p. 2024, "F3870 Clocks"; p. 2029, Fig. 4, "Internal Mode").

It would have been obvious to one of ordinary skill in the art in 1989, that the on-chip oscillator could operate using a ring oscillator because a ring oscillator is one of the most basic and commonly used oscillator designs. For example, the *Hanamura* patent, which issued in 1987, shows a ring oscillator on an integrated circuit that is used to clock an on-chip signal processor. (*Hanamura*, Figs. 10, 12; 6:25-40; 7:9-20).

Mostek discloses that the on-chip oscillator has a variable speed: it has "[f]requency variation from unit to unit due to switching speed [process variations] and level at constant temperature and Vcc....[also] due to Vcc with all other parameters constant....[or] due to temperature [with] all other parameters constant...." (p. III-118, col. 1, RC MODE CONFIGURATION).

(c) ***said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;***

Mostek discloses that for the microcomputers of the 3870 family, the microprocessor and clock are both constructed of electronic devices on the same IC, using the same process technology: "The MK3870 is a complete 8-bit microcomputer on a single MOS integrated circuit." (p. III-77, "General Description"). The MK3873 is one of "the 3870 microcomputer family." (p. III-102, "General Description", and p. III-101, Title).

It is inherent, and would have been obvious to one of ordinary skill in 1989, that the microprocessor and system clock in the same integrated circuit would have corresponding manufacturing variations and, therefore, would vary together in frequency due to manufacturing and temperature variations. During prosecution of the '336 Patent, the patentee argued such inherency to distinguish prior art.

> The placement of [the clock and the microprocessor] within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, since <u>the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters</u> (e.g., temperature) affecting performance. ('336 Patent Prosecution History, *Paper 6*, p. 8, ¶ 2).

Therefore, it is inherent that the clock and microprocessor on the MK3873 chip vary together in frequency due to manufacturing and temperature variations.

(d) ***an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;***

As discussed in section B(1)(d) above, *Mostek* discloses an on-chip input/output interface connected between the central processing unit and an external memory bus, to exchange coupling control signals, addresses and data with the CPU.

(e) ***and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.***

As discussed in section B(1)(e) above, the on-chip input/output interface is connected to and clocked by a second, external clock, and it is inherent that the external clock is independent of the on-chip system clock.

Because every element of claim 1 is disclosed expressly or inherently in *Mostek*, or would have been obvious to one of ordinary skill in the art in 1989, claim 1 is unpatentable. The claim elements and cited references discussed above are summarized in the table below.

'336 Patent Claim 1	**Cited References**
A microprocessor system, comprising a single integrated circuit including a central processing unit and	*Mostek*: p. III-102, col. 1, ¶ 1; p. III-103, Fig. 1.
an entire ring oscillator variable speed system clock in said single integrated circuit and	*Mostek*: p. III-114, col. 2, "3873 TIME BASE OPTIONS"; *see also* p. III-102, col. 2, ¶ 6; p. III-103, Fig. 1; p. III-115, cols. 1-2 (on-chip oscillator). *Mostek*: p. III-102, col. 2, "MK3873 Architecture" (the time base modes of the MK3870 are inherent in the MK3873). *EDN*: p. 2, MK 3870-F8/1 Features (MK3870

	with internal-only clock mode). *IC Master*: p. 2024, "F3870 Clocks"; p. 2029, Fig. 4, "Internal Mode". *Mostek*: p. III-118, col. 1, RC MODE CONFIGURATION (variable speed clock). *Hanamura*, Figs. 10, 12; 6:25-40; 7:9-20.
connected to said central processing unit for clocking said central processing unit,	*Mostek*: p. III-114, col. 2, "3873 TIME BASE OPTIONS"; *see also* p. III-102, col. 2, ¶ 6; p. III-103, Fig. 1; p. III-115, cols. 1-2 (connected to clock the CPU).
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	*Mostek*: p. III-102, "General Description", and p. III-101, Title (MK3873 is one of the MK3870 family). *Mostek*: p. III-77, "General Description" (the MK3870 family has the CPU and clock on the same IC, constructed of the same process technology).
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	*Paper 6*, p. 8, ¶ 2.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and	*Mostek*: p. III-105, Serial I/O Operation section; p. III-102, col. 1,¶ 1; p. III-107, "Port D Serial Port Control Register" section; p. III-111, col. 2, ¶ 2 (interface exchanging control and data signals with the processor). *Mostek*: p. III-102, col. 1,¶1 (interface exchanging addresses with the processor).
a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	*Mostek*: p. III-102, col. 1,¶1; p. III-105, Serial I/O Operation section; p. III-110, ¶ 2 and Fig. 8, "External Clock Mode"; p. VI-4, "MK3873 Application Note", col. 1, SYNC, ¶ 1 (second clock connected to the interface). *Mostek*: p. III-110, ¶ 2 (second clock

	independent).

2. *Claim 2*

The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.

As discussed in section B(2) above, it is inherent that the second clock disclosed by *Mostek* is a fixed frequency clock. Thus, considering the discussion of claim 1 above, every element of claim 2 is disclosed in *Mostek* or would have been obvious to a Skilled Artisan in 1989, and claim 2 should be rejected.

3. *Claim 3*

(a) ***In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:***

As discussed in section C(1)(a) above, *Mostek* discloses an integrated circuit (IC) that includes a microprocessor system, with a microprocessor.

(b) ***providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;***

As discussed in sections C(1)(b) and (c) above, *Mostek* makes obvious the integrated circuit including an entire ring oscillator that is constructed of electronic devices with operating characteristics that vary together with those of the microprocessor.

(c) *using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;*

As discussed in sections C(1)(b) and (c) above, *Mostek* teaches that the ring oscillator clocks the central processing unit to operate at a variable clock rate.

(d) *providing an on chip input/output interface for the microprocessor integrated circuit; and*

As discussed in section B(1)(d) above, *Mostek* discloses an on-chip input/output interface for the microprocessor.

(e) *clocking the input/output interface with a second clock independent of the ring oscillator system clock.*

As discussed in section B(1)(e) above, *Mostek* discloses that the on-chip input/output interface is connected to and clocked by a second, external clock, and it is inherent that the external clock is independent of the on-chip system clock.

Because every element of claim 3 is disclosed expressly or inherently in *Mostek* or would have been obvious to one of ordinary skill in the art in 1989, claim 3 is unpatentable.

4. *Claim 4*

The method of claim 3 in which the second clock is a fixed frequency clock.

As discussed in section C(2) above, *Mostek* discloses that the second clock has a fixed frequency. Considering also the discussion of claim 3 above, every element of claim 4 is disclosed by *Mostek* or would have been obvious to one of ordinary skill in 1989. Therefore, claim 4 should be rejected.

5. *Claim 5*

The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock

As discussed in section B(5) above, *Mostek* discloses that information can be transferred between the microprocessor and the input/output interface in synchrony with the on-chip clock. Thus, considering also the discussion of claim 3 above, claim 5 should be rejected as being obvious over *Ledzius* in light of *Mostek.*

6. *Claim 6*

(a) ***A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;***

As discussed in section C(1)(a) above, *Mostek* discloses an integrated circuit (IC) that includes a microprocessor system, with a central processing unit.

(b) ***an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,***

As discussed in sections C(1)(b) and (c) above, *Mostek* teaches that the integrated circuit includes an entire on-chip oscillator, constructed of electronic devices, that clocks the central processing unit at a clock rate.

(c) *thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;*

As discussed in sections C(1)(b) and (c) above, *Mostek* discloses that the on-chip oscillator and processor frequencies vary in the same way due to variation in fabrication or operational parameters so that the processing frequency tracks the clock rate.

(d) ***an on-chip input/output interface, connected between [said] central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and***

As discussed in section B(1)(d) above, *Mostek* discloses an on-chip input/output interface connected between the central processing unit and an external memory bus, to exchange coupling control signals, addresses and data with the CPU.

(e) ***an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.***

As discussed in section B(1)(e) above, *Mostek* discloses that the on-chip input/output interface is connected to and clocked by a second, external clock, and it is inherent that the external clock is independent of the on-chip system clock.

Because every element of claim 6 is disclosed expressly or inherently in *Mostek* or would have been obvious to one of ordinary skill in the art in 1989, claim 6 is unpatentable.

7. *Claim 7*

The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

As discussed in section C(1)(c) above, *Mostek* discloses that the on-chip oscillator varies in frequency due to variation in operating voltage and temperature. It is inherent, and would have been obvious to one of ordinary skill in 1989, that the microprocessor and system clock in the same integrated circuit would vary together in frequency due to manufacturing and temperature variations. Therefore, considering also the discussion of claim 6 above, every element of claim 7 is disclosed in *Mostek* or would have been obvious to one of ordinary skill in 1989, and claim 7 should be rejected.

8. *Claim 8*

The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.

As discussed in section B(8) above, claim 8 may be invalid under 35 U.S.C. § 112, ¶ 2, as being indefinite. Alternately, the claim limitation, "operates synchronously relative to said [on-chip] oscillator", might be construed to mean that the external clock operates in synchrony with external components, rather than in synchrony with the on-chip oscillator.

Mostek discloses that the serial input/output interface may transfer data out of the chip using a fixed frequency, external clock, and the external clock may operate in synchrony with external components. Therefore, considering also the discussion of claim 6 above, claim 8 should be rejected as being anticipated by *Mostek*.

9. *Claim 9*

The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.

As discussed in section C(1)(b) above, it would have been obvious to one of ordinary skill in the art in 1989, that the on-chip oscillator could be a ring oscillator. Therefore, considering also the discussion of claim 6 above, claim 9 should be rejected as being invalid over *Mostek*.

10. *Claim 10*

(a) ***In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of: providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;***

As discussed in section C(1)(a) above, *Mostek* discloses an integrated circuit that includes a microprocessor system, with a central processing unit. (p. III-102, col. 1, ¶ 1; p. III-103, Fig. 1).

(b) ***providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;***

As discussed in sections C(1)(b) and (c) above, *Mostek* teaches that the integrated circuit includes an entire variable speed oscillator. It is inherent that an integrated circuit clock is constructed of transistors.

(c) *clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;*

As discussed in sections C(1)(b) and (c) above, *Mostek* teaches that the on-chip oscillator clocks the central processing unit at a frequency that varies with process, supply voltage and temperature. It is inherent that the microprocessor and system clock in the same integrated circuit would vary in frequency in the same way due to manufacturing and temperature variations.

(d) *connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and*

As discussed in section B(1)(d) above, *Mostek* discloses an on-chip input/output interface connected between the central processing unit and an external memory bus, to exchange coupling control signals, addresses and data with the CPU.

(e) *clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.*

Mostek discloses that the on-chip input/output interface is connected to and clocked by a second, external clock, and it is inherent that the external clock is independent of the on-chip system clock, as discussed in section B(1)(e) above.

Because every element of claim 10 is disclosed expressly or inherently in *Mostek* or would have been obvious to one of ordinary skill in the art in 1989, claim 10 is unpatentable.

D. Claims 1-10 are obvious over *Ledzius* in light of *Guttag, as further evidenced by prior prosecution correspondence, Paper 6.*[6]

Every element of claims 1-10 is expressly or inherently disclosed in the combination of *Ledzius* and *Guttag* or would have been obvious to one of ordinary skill in 1989.

1. *Claim 1*

(a) ***A microprocessor system, comprising a single integrated circuit including a central processing unit***

As discussed in section B(1)(a) above, *Ledzius* discloses microprocessor system on an integrated circuit (IC)10 that includes a central processing unit.

(b) ***and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,***

As discussed in section B(1)(b) above, *Ledzius* discloses an entire on-chip ring oscillator and system clock that has variable speed and is connected to clock the central processing unit.

(c) ***said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;***

As discussed in section B(1)(c) above, *Ledzius* discloses that the clock and processor each include electronic devices constructed of the same process technology and having the same manufacturing variations. They vary together in frequency due to manufacturing and

6 *Paper 6* is provided as discussed in section II(B) above.

temperature variations, and it is inherent, and would have been obvious to one of ordinary skill in 1989, that they also vary together due to variation in supply voltage.

(d) ***an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;***

As discussed in section B(1)(d) above, *Ledzius* discloses an on-chip input/output interface (latches 20-22) that passes data, addresses and coupling control signals between the processor and an external bus. Also, *Ledzius* explicitly suggests using a different input/output interface in place of latches 20-23.

Guttag discloses a solution for the same problem discussed in *Ledzius*, which is providing asynchronous operation of a processor and external devices, such as external memory. (*Ledzius* at 1:57-59, "Summary of the Invention"; *Guttag*, Exhibit 9, at p. 44, ¶ 2, "Host Interface"). Therefore, given the similarity of feature and function, it would have been obvious to one skilled in the art of 1989 to combine the teachings of *Guttag* and *Ledzius* to apply the input/output interface of *Guttag* as the interface of *Ledzius*.

Specifically, *Guttag* discloses that the TMS34010 chip (which includes a microprocessor) may be used as an input/output "Host Interface" for a different, host processor. (p. 44, ¶ 2). The Host Interface may be connected between a host processor and an external memory bus and memory: "...[T]he 34010 has a dedicated interface port to allow another processor to gain access to [the interface's] memory." (p. 44, ¶ 2, "Host interface"; Figs.6 and 8). The TMS34010 chip may exchange data, addresses and control signals with the host processor. (p.41, Fig.2; p. 44, ¶ 2-p. 45, col.1, ¶ 2, "Host Interface"; p. 45, col. 2, ¶ 2; p.48, Fig.6; p.51, Fig.8).

(e) ***and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.***

Guttag discloses that the TMS34010 chip Host Interface is connected to its own external clock: "The [TMS34010 Host Interface] processor uses a high-frequency (40MHz to 60 MHz) input clock so that it can precisely place the large number of timing edges required by a DRAM." (p. 48, col. 2, ¶ 3; Fig. 6 with 50 MHz oscillator). (The interface has and uses "internal timing clock [signals]", but they are generated from the external input clock frequency. (p. 46, col. 1, "Internal Clocks."). It is inherent that *Guttag*'s external clock (e.g., 50 MHz oscillator in Fig. 6), which has no connection to the Host Processor's on-chip clock, would be <u>independent</u> of the on-chip clock.

Because the combination of *Ledzius* and *Guttag* renders all elements of claim 1 obvious to one of ordinary skill in 1989 and it would have been obvious to combine their teachings, claim 1 is unpatentable. The claim elements and cited references discussed above are summarized in the table below.

<u>**'336 Patent Claim 1**</u>	<u>**Cited References**</u>
A microprocessor system, comprising a single integrated circuit including a central processing unit and	*Ledzius*: Fig. 1; 2:28-38; 2:43-54; 4:5-7. *Brenig*: 5:64-67.
an entire ring oscillator variable speed system clock in said single integrated circuit and	*Ledzius*: Fig. 1; 1:65-68; *also* 2:28-40; 4:5-7; Abstract; *also* 4:22-23; 5:53-58; 6:63-65 (entirely on-chip oscillator). *Ledzius*: 4:5-21 (variable speed clock). *Ledzius*: Figs. 2-3; 4:50-5:60; 6:63-65 (ring oscillator)
connected to said central processing unit for	*Ledzius*: 5:56-58; and Figs. 1-2; *also* 1:53-56;

clocking said central processing unit,	1:65-68; 2:58-60; 4:22-23.
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	*Ledzius*: 4:5-21 (the same process technology and corresponding manufacturing variations)
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	*Ledzius*: 4:5-21. *Paper 6*, p. 8, ¶.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and	*Ledzius*: Fig. 1; 3:31-53; 3:54-63; 2:29-32; 2:26-29 (interface exchanging control, address and data signals with the processor). *Ledzius*: 6:63-67; 1:57-59 (combining references). *Guttag*: Figs.2, 6 and 8; p. 44, ¶ 2-p. 45, col.1, ¶ 2, "Host Interface"; p. 45, col. 2, ¶ 2 (interface exchanging data, addresses and control signals with a host processor).
a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	*Guttag*: p. 48, col. 2, ¶ 3; Fig. 6 (Host Interface connected to external 50 MHz oscillator)

2. ***Claim 2***

The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.

Guttag discloses that the host interface is connected to an external clock with a fixed frequency. (Fig. 6,"50 MHz" oscillator). Therefore, considering also the discussion of claim 1 above, the combination of *Ledzius* and *Guttag* renders all elements of claim 2 obvious to one of ordinary skill in 1989, and claim 2 should be rejected.

3. *Claim 3*

(a) ***In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:***

Ledzius discloses an integrated circuit (IC)10 that includes a microprocessor and a method for clocking the microprocessor, as discussed in sections B(1)(a) and (b) above.

(b) ***providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;***

Ledzius discloses that IC 10 includes an entire ring oscillator and that the on-chip oscillator and microprocessor vary together in frequency because they include electronic devices with operating characteristics that vary together with variations in manufacturing and operating characteristics, as discussed in sections B(1)(b) and (c) above.

(c) ***using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;***

Ledzius discloses using the ring oscillator for clocking the microprocessor at a variable frequency, as discussed in section B(1)(b) above.

(d) ***providing an on chip input/output interface for the microprocessor integrated circuit; and***

As discussed in section B(1)(d) above, *Ledzius* discloses an on-chip input/output interface (latches 20-22) that passes data, addresses and coupling control signals between the processor and an external bus. *Ledzius* also explicitly suggests using a different input/output interface in place of latches 20-22. As discussed in section D(1)(d) above, *Guttag* discloses an on-chip input/output Host Interface for a microprocessor. It would have been obvious to one skilled in the art of 1989 to combine the teachings of *Guttag* and *Ledzius* to apply the input/output interface of *Guttag* as the interface of *Ledzius*.

(e) ***clocking the input/output interface with a second clock independent of the ring oscillator system clock.***

As discussed in section D(1)(e) above, *Guttag* discloses that the Host Interface is connected to an external clock with a frequency fixed at 50 MHz, independent of the host processor clock.

Because the combination of *Ledzius* and *Guttag* renders every element of claim 3 obvious to one of ordinary skill in 1989 and it would have been obvious to combine their teachings, claim 3 is unpatentable.

4. ***Claim 4***

The method of claim 3 in which the second clock is a fixed frequency clock.

As discussed in section D(2) above, *Guttag* discloses that the TMS34010 Host Interface is connected to an external clock with a fixed frequency. (Fig. 6 with 50 MHz oscillator). Therefore, considering also the discussion of claim 3 above, the combination of *Ledzius* and

Guttag renders all elements of claim 4 obvious to one of ordinary skill in 1989, and claim 4 should be rejected.

5. *Claim 5*

The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock

Guttag discloses that the TMS34010 Host Interface exchanges information with the Host Processor in synchrony with the host processor's clock. The host processor exchanges information with the interface through the interface's "four internal memory-mapped [data, address and control] registers [that] are <u>dedicated to the host</u>. These registers are loaded from the 8/16-bit host bus under the control of two function select pins." (p. 44, last paragraph, emphasis added). It is inherent that the host processor's oscillator would control timing of access to the dedicated registers in the TMS34010 interface.

Thus, considering also the discussion of claim 3 above, claim 5 should be rejected as being obvious over *Ledzius* in light of *Guttag*.

6. *Claim 6*

(a) ***A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;***

Ledzius discloses an integrated circuit (IC) 10 that includes a microprocessor system, with a central processing unit, that operates at a frequency and is constructed of electronic devices, as discussed in sections B(1)(a) and (c) above.

(b) ***an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,***

Ledzius discloses that IC 10 also includes an entire oscillator, that the oscillator is constructed of electronic devices, and that it is used for clocking the microprocessor, as discussed in section B(1)(b) above.

(c) ***thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;***

Ledzius discloses using the ring oscillator for clocking the microprocessor at a variable frequency, as discussed in section B(1)(b) above. *Ledzius* discloses that the on-chip oscillator and microprocessor vary together in frequency because they include electronic devices with operating characteristics that vary together with variations in manufacturing and operating characteristics, as discussed in section B(1)(c) above.

(d) ***an on-chip input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and***

As discussed in section B(1)(d) above, *Ledzius* discloses an on-chip input/output interface but also explicitly suggests using a different input/output interface in its place. As discussed in section D(1)(d) above, *Guttag* discloses an input/output "Host Interface" connected between a host processor and an external memory bus to exchange data, addresses and control signals with the host processor. It would have been obvious to one skilled in the art of 1989 to combine the teachings of *Guttag* and *Ledzius* to apply the input/output interface of *Guttag* as the interface of *Ledzius*.

(e) ***an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.***

As discussed in section D(1)(d) above, *Guttag* discloses that the Host Interface is connected to its own external clock that is independent of the host processor's on-chip clock.

Because the combination of *Ledzius* and *Guttag* renders all elements of claim 6 obvious to one of ordinary skill in 1989 and it would have been obvious to combine their teachings, claim 6 is unpatentable.

7. *Claim 7*

The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

Ledzius discloses that the on-chip oscillator and microprocessor vary together in frequency due to variations in temperature, as discussed in section B(1)(c) above. Therefore, considering also the discussion of claim 6 above, the combination of *Ledzius* and *Guttag* renders all elements of claim 7 obvious to one of ordinary skill in 1989, and claim 7 should be rejected.

8. *Claim 8*

The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.

As discussed in section B(8) above, claim 8 may be invalid under 35 U.S.C. § 112, ¶ 2, as being indefinite. Alternately, the claim limitation, "operates synchronously relative to said [on-chip] oscillator", might be construed to mean that the external clock operates in synchrony with external components, rather than in synchrony with the on-chip oscillator.

Guttag discloses that the TMS34010 host interface's external clock operates in synchrony with the interface's external components. Specifically, the same clock that is input to the interface is used to generate "the local bus clock signals used by external devices [e.g., local memory] to operate synchronously with the [TMS34010 interface's] local bus." (p. 46, col. 1, ¶ 4, "Internal Clocks"). Therefore, considering also the discussion of claim 6 above, the combination of *Ledzius* and *Guttag* renders all elements of claim 8 obvious to one of ordinary skill in 1989, and claim 8 should be rejected.

9. *Claim 9*

The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.

Ledzius discloses that the on-chip oscillator is a ring oscillator, as discussed in section B(1)(b) above. Thus, considering also the discussion of claim 6 above, claim 8 should be rejected as being obvious over *Ledzius* in light of *Guttag*.

10. *Claim 10*

(a) ***In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of: providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;***

Ledzius discloses an integrated circuit (IC) 10 that includes a microprocessor system, with a central processing unit that operates at a frequency and is constructed of electronic devices, as discussed in sections B(1)(a) and (c) above. It is inherent, and would have been obvious to one of ordinary skill in 1989, that a CPU constructed on an IC would be constructed of transistors. *Ledzius* also discloses a method for clocking the central processing unit as discussed in section B(1)(b) above.

(b) ***providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;***

Ledzius discloses that IC 10 also includes an entire variable speed clock, as discussed in section B(1)(b) above. *Ledzius* discloses that the on-chip clock is constructed of electronic devices, as discussed in section B(1)(c) above. It is inherent, and would have been obvious to one of ordinary skill in 1989, that the on-chip clock would be constructed of transistors.

(c) ***clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;***

Ledzius discloses using the ring oscillator for clocking the microprocessor at a variable frequency, as discussed in section B(1)(b) above. *Ledzius* also discloses that the on-chip oscillator and microprocessor, constructed on the same IC, vary together in frequency with IC fabrication or operating parameters, as discussed in section B(1)(c) above.

(d) ***connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and***

As discussed in section B(1)(d) above, *Ledzius* discloses an on-chip input/output interface, latches 20-22, that is connected to pass data and coupling control signals between the functional circuit and an external bus. *Ledzius* also <u>explicitly suggests</u> using a different input/output interface in place of latches 20-22. As discussed in section D(1)(d) above, *Guttag* discloses an on-chip input/output Host Interface connected between the central processing unit and an external memory bus to exchange coupling control signals, addresses and data with the CPU. It would have been obvious to one skilled in the art of 1989 to combine the teachings of *Guttag* and *Ledzius* to apply the input/output interface of *Guttag* as the interface of *Ledzius*.

(e) ***clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.***

As discussed in section D(1)(e) above, *Guttag* discloses that the Host Interface is connected to an external clock with a frequency fixed at 50 MHz, independent of the host processor clock.

Because the combination of *Ledzius* and *Guttag* renders all elements of claim 10 obvious to one of ordinary skill in 1989 and it would have been obvious to combine their teachings, claim 10 is unpatentable.

E. Claims 1-10 are obvious over *Ledzius* in light of *Thaden*, as further evidenced by prior prosecution correspondence, *Paper 6*.[7]

Every element of claims 1-10 is either expressly or inherently disclosed in the combination of *Ledzius* and *Thaden* or would have been obvious to one of ordinary skill in 1989.

1. *Claim 1*

(a) ***A microprocessor system, comprising a single integrated circuit including a central processing unit***

As discussed in section B(1)(a) above, *Ledzius* discloses a microprocessor system on an integrated circuit (IC)10 that includes a central processing unit.

(b) ***and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,***

As discussed in section B(1)(b) above, *Ledzius* discloses an entire on-chip ring oscillator and system clock that has variable speed and is connected to clock the central processing unit.

(c) ***said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;***

As discussed in section B(1)(c) above, *Ledzius* discloses that the clock and processor each include electronic devices constructed of the same process technology and having the same manufacturing variations. They vary together in frequency due to manufacturing and

[7] *Paper 6* is provided as discussed in section II(B) above.

temperature variations, and it is inherent, and would have been obvious to one of ordinary skill in 1989, that they also vary together due to variation in supply voltage.

(d) ***an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;***

As discussed in section B(1)(d) above, *Ledzius* discloses an on-chip input/output interface (latches 20-22) that passes data, addresses and coupling control signals between the processor and an external bus. Also, *Ledzius* explicitly suggests using a different input/output interface in place of latches 20-23.

Thaden discloses an input/output interface as a solution for the same problem discussed in *Ledzius*, which is providing asynchronous operation of a functional circuit and external devices, such as a microprocessor and external memory. (*Ledzius* at 1:57-59, "Summary of the Invention"; *Thaden*, Exhibit 10, at 3:31-40, "Summary of the Invention"). Therefore, given the similarity of feature and function, it would have been obvious to one skilled in the art of 1989 to combine the teachings of *Thaden* and *Ledzius* to apply the input/output interface of *Thaden* as the interface of *Ledzius*.

Specifically, *Thaden* discloses an input/output interface, "video system controller (VSC) 3", that provides communication between a microprocessor and an external display and its memory. (Fig. 1; 3:30-40). The VSC interface is connected between the microprocessor and two memory busses, memory address bus 25 and control bus 27, which connect to display memory 5. (Figs. 1-2; 5:66-6:1; 6:7-21; 6:28-31; 6:34-37; and 6:65-7:4). Therefore, the VSC interface facilitates the exchange of control and address signals with the microprocessor 1. (*Id*)..

The VSC interface is not physically connected between the microprocessor and the data bus, but it is connected to facilitate exchange of data because it is connected to enable data transfer over data bus 17 between microprocessor 1 and system memory 19 (and display memory 5). (*Id.*; 6:28-31).

(e) ***and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.***

Thaden discloses that the VSC interface is connected to a first clock source that "provides timing for the processor which is in synch with the timing of the processor" and is also connected to a second clock source that "provides timing for the CRT interface and is in synch with the timing of the CRT monitor." (3:33-40; Fig. 2, with SYSCLK entering on the left and VIDCLK on the right side of the circuit). (Note that in *Thaden*, the names "first clock source" and "second clock source" are the reverse of those in the '336 patent; the names have been modified in the discussion above to be consistent with the terminology of the '336 Patent). "VIDCLK [the '336 Patent's second clock]...may be different from the microprocessor 1 clock, SYSCLK [the '336 Patent's first clock]." (30:44-46).

Thaden discloses that the VSC interface is connected to an external clock that is independent of the computer system clock: *Thaden's* Claim 1 recites, "...a system clock means for generating a system clock signal; a video clock means for generating a video clock signal which is independent of and asynchronous with said system clock signal...a video system controller means...connected to...said video clock means."

Because the combination of *Ledzius* and *Thaden* renders all elements of claim 1 obvious to one of ordinary skill in 1989 and it would have been obvious to combine their teachings, claim 1 is unpatentable. The claim elements and cited references discussed above are summarized in the table below.

'336 Patent Claim 1	Cited References
A microprocessor system, comprising a single integrated circuit including a central processing unit and	*Ledzius*: Fig. 1; 2:28-38; 2:43-54; 4:5-7. *Brenig*: 5:64-67.
an entire ring oscillator variable speed system clock in said single integrated circuit and	*Ledzius*: Fig. 1; 1:65-68; *also* 2:28-40; 4:5-7; Abstract; *also* 4:22-23; 5:53-58; 6:63-65 (entirely on-chip oscillator). *Ledzius*: 4:5-21 (variable speed clock). *Ledzius*: Figs. 2-3; 4:50-5:60; 6:63-65 (ring oscillator)
connected to said central processing unit for clocking said central processing unit,	*Ledzius*: 5:56-58; and Figs. 1-2; *also* 1:53-56; 1:65-68; 2:58-60; 4:22-23.
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	*Ledzius*: 4:5-21 (the same process technology and corresponding manufacturing variations)
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	*Ledzius*: 4:5-21. *Paper 6*, p. 8, ¶.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and	*Ledzius*: Fig. 1; 3:31-53; 3:54-63; 2:29-32; 2:26-29 (interface exchanging control, address and data signals with the processor). *Ledzius*: 6:63-67; 1:57-59 (combining references). *Thaden*: Figs. 1-2; 3:30-40; 5:66-6:1; 6:7-21; 6:28-31; 6:34-37; and 6:65-7:4 (video system controller exchanging data, addresses and control signals with the processor).

a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	*Thaden*: Fig. 2 (SYSCLK entering on the left and VIDCLK on the right side of the circuit); 3:33-46; (video system controller connected to external VIDCLK). *Thaden*: Claim 1 (the external clock VIDCLK is <u>independent</u> of the computer system clock SYSCLK).

2. *Claim 2*

The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.

Thaden discloses that the VSC interface's external clock frequency is fixed to be "in synch with the timing of the CRT monitor." (3:36-37, the *Thaden* specification calling the <u>external</u> clock the "<u>first</u> clock source"). Therefore, considering also the discussion of claim 1 above, the combination of *Ledzius* and *Thaden* renders all elements of claim 2 obvious to one of ordinary skill in 1989, and claim 2 should be rejected.

3. *Claim 3*

(a) ***In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:***

As discussed in sections B(1)(a) and (b) above, *Ledzius* discloses an integrated circuit (IC) 10 that includes a microprocessor and a method for clocking the microprocessor.

(b) ***providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;***

Ledzius discloses that IC 10 includes an entire ring oscillator and that the on-chip oscillator and microprocessor vary together in frequency because they include electronic devices with operating characteristics that vary together with variations in manufacturing and operating characteristics, as discussed in sections B(1)(b) and (c) above.

(c) ***using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;***

Ledzius discloses using the ring oscillator for clocking the microprocessor at a variable frequency, as discussed in section B(1)(b) above.

(d) ***providing an on chip input/output interface for the microprocessor integrated circuit; and***

As discussed in section B(1)(d) above, *Ledzius* discloses an on-chip input/output interface (latches 20-22) that passes data, addresses and coupling control signals between the processor and an external bus. *Ledzius* also <u>explicitly suggests</u> using a different input/output interface in place of latches 20-22. As discussed in section E(1)(d) above, *Thaden* discloses an on-chip input/output interface, "video system controller," for a microprocessor. It would have been obvious to one skilled in the art of 1989 to combine the teachings of *Thaden* and *Ledzius* to apply the input/output interface of *Thaden* as the interface of *Ledzius*.

(e) ***clocking the input/output interface with a second clock independent of the ring oscillator system clock.***

As discussed in section E(1)(e) above, *Thaden* discloses that the VSC interface is connected to an external clock that is independent of the computer system clock.

Because the combination of *Ledzius* and *Thaden* renders every element of claim 3 obvious to one of ordinary skill in 1989 and it would have been obvious to combine their teachings, claim 3 is unpatentable.

4. *Claim 4*

The method of claim 3 in which the second clock is a fixed frequency clock.

As discussed in section E(2) above, *Thaden* discloses that the VSC interface is connected to a second, external, clock with a frequency that is fixed to be "in synch with the timing of the CRT monitor." Therefore, considering also the discussion of claim 3 above, the combination of *Ledzius* and *Thaden* renders all elements of claim 4 obvious to one of ordinary skill in 1989, and claim 4 should be rejected.

5. *Claim 5*

The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock

Thaden discloses that the VSC interface transfers information from the microprocessor with timing controlled by the system clock: *Thaden's* claim 1 recites, "...said video system controller means include[es] a data processor address latch connected to said system clock means[,] thereby having timing controlled by said system clock signal, and [connected] to said first address bus for storing an address received from said data processor means."

Thaden also discloses that microprocessor interface signals input to the VSC interface are clocked by the system clock. "SYSCLK is the system input clock, which is used to generate the timing of signals output to the memory, and the timing of the INT- and RDY/HOLD- signals output to the microprocessor. Additionally, all microprocessor 1 interface signals input to the Video System Controller 3 must be synchronous to SYSCLK." (13, Table 1, describing SYSCLK). Thus, considering also the discussion of claim 3 above, claim 5 should be rejected as being obvious over *Ledzius* in light of *Thaden.*

6. *Claim 6*

(a) ***A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;***

Ledzius discloses an integrated circuit (IC) 10 that includes a microprocessor system, with a central processing unit, that operates at a frequency and is constructed of electronic devices, as discussed in sections B(1)(a) and (c) above.

(b) ***an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,***

Ledzius discloses that IC 10 also includes an entire oscillator, that the oscillator is constructed of electronic devices, and that it is used for clocking the microprocessor, as discussed in section B(1)(b) above.

(c) *thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;*

Ledzius discloses using the ring oscillator for clocking the microprocessor at a variable frequency, as discussed in section B(1)(b) above. *Ledzius* discloses that the on-chip oscillator and microprocessor vary together in frequency because they include electronic devices with operating characteristics that vary together with variations in manufacturing and operating characteristics, as discussed in section B(1)(c) above.

(d) *an on-chip input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and*

As discussed in section B(1)(d) above, *Ledzius* discloses an on-chip input/output interface but also explicitly suggests using a different input/output interface in its place. As discussed in section E(1)(d) above, *Thaden* discloses an on-chip input/output interface, "video system controller," connected between a central processing unit and an external memory bus to exchange data, addresses and control signals with the central processing unit. It would have been obvious to one skilled in the art of 1989 to combine the teachings of *Thaden* and *Ledzius* to apply the input/output interface of *Thaden* as the input/output interface of *Ledzius*.

As discussed in section E(1)(d) above, the VSC interface is connected between the microprocessor and two memory busses, memory address bus 25 and control bus 27 to facilitate the exchange of control and address signals with the microprocessor 1. The VSC interface is not physically connected between the microprocessor and the data bus, but claim 6 recites only connection with "an [at least one] external memory bus", which is disclosed in the connections to the memory address bus and control bus discussed above. Nonetheless, the VSC interface is functionally connected between the microprocessor and the data bus because it is connected to enable data transfer over data bus 17 between microprocessor 1 and system memory 19 (and display memory 5). (6:28-31).

(e) ***an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.***

As discussed in section E(1)(e) above, *Thaden* discloses that the VSC interface is connected to an external clock that is independent of the computer system clock. *Thaden* also discloses that the VSC interface operates at a frequency independent of the system clock: *Thaden's* claim 1 recites, "[S]aid video system controller means including...a video memory cycle generator means...having timing controlled by said video clock signal."

Because the combination of *Ledzius* and *Thaden* renders all elements of claim 6 obvious to one of ordinary skill in 1989 and it would have been obvious to combine their teachings, claim 6 is unpatentable.

7. *Claim 7*

The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

Ledzius discloses that the on-chip oscillator and microprocessor vary together in frequency due to variations in temperature, as discussed in section B(1)(c) above. Therefore, considering also the discussion of claim 6 above, the combination of *Ledzius* and *Thaden* renders all elements of claim 7 obvious to one of ordinary skill in 1989, and claim 7 should be rejected.

8. *Claim 8*

The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.

As discussed in Section B(8) above, claim 8 may be invalid under 35 U.S.C. § 112 as being indefinite. Alternately, the claim may be construed to require operating in synchrony with external components.

Thaden discloses that the external clock (video input clock or VIDCLK) can operate synchronously to external components. "The video input clock drives the portion of the logic within the Video System Controller 3 chip that is responsible for generating the timing for the synch and blanking signals....Typically, VIDCLK is harmonically related to the dot (or pixel) clock used to stream video data from the external shift registers in the memory system to the CRT monitor." (17, Table 1, describing "VIDCLK"). Therefore, considering also the discussion of claim 6 above, the combination of *Ledzius* and *Thaden* renders all elements of claim 8 obvious to one of ordinary skill in 1989, and claim 8 should be rejected.

9. *Claim 9*

The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.

Ledzius discloses that the on-chip oscillator is a ring oscillator, as discussed in section B(1)(b) above. Thus, considering also the discussion of claim 6 above, claim 8 should be rejected as being obvious over *Ledzius* in light of *Thaden*.

10. *Claim 10*

(a) ***In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of: providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;***

Ledzius discloses an integrated circuit (IC) 10 that includes a microprocessor system, with a central processing unit that operates at a frequency and is constructed of electronic devices, as discussed in sections B(1)(a) and (c) above. It is inherent, and would have been obvious to one of ordinary skill in 1989, that a CPU constructed on an IC would be constructed of transistors. *Ledzius* also discloses a method for clocking the central processing unit as discussed in section B(1)(b) above.

(b) ***providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;***

Ledzius discloses that IC 10 also includes an entire variable speed clock, as discussed in section B(1)(b) above. *Ledzius* discloses that the on-chip clock is constructed of electronic devices, as discussed in section B(1)(c) above. It is inherent, and would have been obvious to one of ordinary skill in 1989, that the on-chip clock would be constructed of transistors.

(c) *clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;*

Ledzius discloses using the ring oscillator for clocking the microprocessor at a variable frequency, as discussed in section B(1)(b) above. *Ledzius* also discloses that the on-chip oscillator and microprocessor, constructed on the same IC, vary together in frequency with IC fabrication or operating parameters, as discussed in section B(1)(c) above.

(d) ***connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and***

As discussed in section B(1)(d) above, *Ledzius* discloses an on-chip input/output interface, latches 20-22, that is connected to pass data and coupling control signals between the functional circuit and an external bus. *Ledzius* also explicitly suggests using a different input/output interface in place of latches 20-22. As discussed in section E(6)(d) above, *Thaden* discloses an on-chip input/output interface, "video system controller," connected between a central processing unit and an external memory bus to exchange data, addresses and control signals with the central processing unit. It would have been obvious to one skilled in the art of 1989 to combine the teachings of *Ledzius* and *Thaden* to apply the input/output interface of *Thaden* in place of the input/output interface of *Ledzius*.

(e) ***clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.***

As discussed in section E(1)(e) above, *Thaden* discloses that the VSC interface is connected to an external clock that is independent of the computer system clock. *Thaden* also discloses that the VSC interface operates at <u>a frequency independent</u> of the system clock: *Thaden's* claim 1 recites, "[S]aid video system controller means including...a video memory cycle generator means...having timing controlled by said video clock signal."

Because the combination of *Ledzius* and *Thaden* renders all elements of claim 10 obvious to one of ordinary skill in 1989 and it would have been obvious to combine their teachings, claim 10 is unpatentable.

F. Claims 1-5 are obvious over *Hitachi* in light of *Boney*, as further evidenced by prior prosecution correspondence, *Paper 6* .[8]

Every element of claims 1-5 is expressly or inherently disclosed in the combination of *Hitachi* and *Boney* or would have been obvious to one of ordinary skill in 1989.

1. *Claim 1*

(a) ***A microprocessor system, comprising a single integrated circuit including a central processing unit***

Hitachi discloses that the HD6805W1 integrated circuit chip "is an 8-bit microcomputer unit (MCU) which contains a CPU." (Exhibit 11, p. 251, ¶ 1 and figure showing DP-40). (Also, *Boney* discloses a "single-chip [single integrated circuit] microcomputer" that "comprises a central processor unit (CPU) 100." (4:54-62; Fig. 1).

8 *Paper 6* is provided as discussed in section II(B) above.

(b) ***and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,***

Hitachi discloses that the integrated circuit includes an oscillator that is entirely on-chip and can operate with no external components, only an external jumper. (p. 251, ¶ 1; p. 262, Internal Oscillator Options; Fig. 11). The oscillator speed is variable because the speed has "Approximately 25% Accuracy." (p. 262, Fig. 11). The on-chip oscillator is connected to and clocks the CPU. (p. 252, Block Diagram).

Hitachi discloses that the HD6805W1 is a member of the 6805 family of microcomputers. (Table of contents; p. 251, ¶ 1). *Boney* discloses a microcomputer and references further microcomputer features from the 6805 microcomputer family. "With reference to FIG. 1 a block diagram of the single-chip microcomputer embodying the present invention is shown....The microcomputer shown in FIG. 1 represents the Motorola MC6805 microcomputer." (Exhibit 12 at 4:54-60). Therefore, given the similarity of feature and function, it would have been obvious to one skilled in the art of 1989 to combine the teachings of *Boney* and *Hitachi* to apply the on-chip clock of *Boney* for the on-chip clock of *Hitachi*.

As shown in Figures 1 and 7F, together, *Boney* discloses that the on-chip system clock has a ring oscillator that provides the clock for the microprocessor: "The XTL and EXTL pins are provided for clocking the microcomputer." (Figs. 1 and 7F; 7:14-15). (The clock circuit in *Boney* may also accept input from an external resistor, but, as shown below, the ring oscillator is entirely on-chip). Figure 7F shows details of the circuit indicated at pins XTL and EXTL in Figure 1. The clock signal is generated through a circuit path shown in Figure 7F that circles through three inverters.

The path follows from the output (at point A, indicated at the bottom of Fig. 7F below) of a first inverter (the NMOS transistor to the right of A), to the input of a second inverter (the NMOS transistor at B), from the output of the second inverter to the input of a third inverter (at C), from the output of the third inverter to the input of the first inverter (at D). The circuit described above is a ring oscillator.

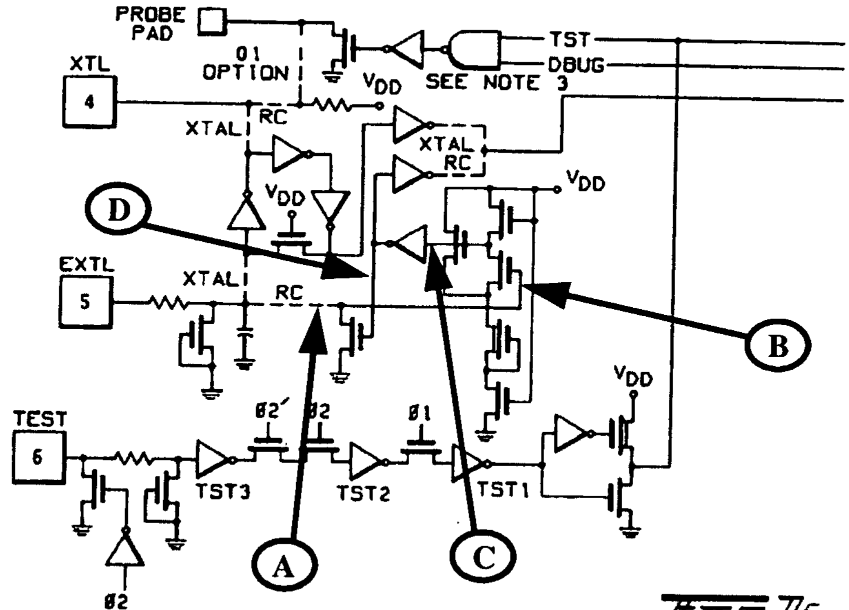


Fig. 7F

(c) ***said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;***

Hitachi discloses that the clock and CPU are constructed in the same integrated circuit and of the same technology: "The HD6805W1 is an 8-bit microcomputer unit (MCU) which contains...[an] on-chip clock...." (p. 251, ¶ 1; Table of Contents at HD6805W1, "Microcomputer Unit (NMOS)"). It is inherent that the clock and CPU, constructed in the same integrated circuit, of the same processing technology, would have corresponding manufacturing variations.

It is inherent and would have been obvious to one of ordinary skill in 1989 that the CPU and clock, constructed on the same IC, would vary together in frequency due to variation in the common manufacturing variations, temperature and supply voltage. (*Id.*). During prosecution of the '336 Patent, the patentee argued that the CPU and the clock inherently vary together in frequency with changes in various parameters:

> The placement of [the clock and the microprocessor] within the same integrated circuit obviates the need for provision of the type of frequency control information described by Sheets, since <u>the microprocessor and clock will naturally tend to vary commensurately in speed as a function of various parameters</u> (e.g., temperature) affecting performance. '336 Patent Prosecution History, *Paper 6*, p. 8, ¶ 2.

(d) ***an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;***

Hitachi discloses that the HD6805W1 chip includes an input/output interface, an "8-bit programmable timer (Timer 2)" which is connected to the CPU. (p. 259, ¶ 1, "Timer 2"). Timer 2 includes a Prescaler Control Register 2 ("PCR2"), Output Compare Register ("OCR"), and Input Capture Register ("ICR"), that are all connected to and read by and/or written to by the CPU. (p. 259, Fig. 7; ¶¶ 3-5, Output Compare Register and Input Capture Register).

Hitachi discloses that the CPU exchanges data with Timer 2. (p. 259, Fig. 7; ¶¶ 3-5, Output Compare Register and Input Capture Register (the OCR and ICR undergoing "Read/Write" and "Read" operations)). The CPU also exchanges addresses with Timer 2 when it sends data to Timer 2's OCR and ICR registers, addressed "01D" and "01E" respectively. (*Id.*). Timer 2 receives control signals from the CPU through the Prescaler Control Register, and Timer 2 sends control signals to the CPU as the Internal Interrupts Request Signals. (p. 259, Fig. 7).

(e) ***and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.***

Hitachi discloses that "Timer 2...[can be] driven by...the [external] TIMER input...." (p. 259, Fig. 7; ¶ 2). It is inherent that the external TIMER disclosed by *Hitachi* with no connection to the on-chip clock would be independent of the on-chip clock.

Because the combination of *Hitachi* and *Boney* renders all elements of claim 1 obvious to one of ordinary skill in 1989 and it would have been obvious to combine their teachings, claim 1 is unpatentable. The claim elements and cited references discussed above are summarized in the table below.

'336 Patent Claim 1	**Cited References**
A microprocessor system, comprising a single integrated circuit including a central processing unit and	*Hitachi*: p. 251, ¶ 1 and figure showing DP-40. *Boney*: 4:54-62; Fig. 1.
an entire ring oscillator variable speed system clock in said single integrated circuit and	*Hitachi*: p. 251, ¶ 1; p. 262, Internal Oscillator Options; Fig. 11 (entirely on-chip oscillator). *Hitachi*: p. 262, Fig. 11 (variable speed clock with "Approximately 25% Accuracy"). *Hitachi*: Table of contents; p. 251, ¶ 1 (the disclosed HD6805W1 IC is a member of the MC6805 family of microcomputers). *Boney*: 4:54-60 (the reference describes the MC6805 microcomputer; combining references). *Boney*: Figs. 1 and 7F; 7:14-15 (ring oscillator).
connected to said central processing unit for clocking said central processing unit,	*Hitachi*: p. 252, Block Diagram.
said central processing unit and said ring	*Hitachi*: p. 251, ¶ 1; Table of Contents at

oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	HD6805W1 (on the same IC and constructed of the same process technology, "Microcomputer Unit (NMOS)").
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	*Paper 6*, p. 8, ¶.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and	*Hitachi*: p. 259, ¶ 1, "Timer 2"; p. 259, ¶¶ 3-5; Fig. 7 (interface, Timer 2, exchanging control, address and data signals with the processor).
a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	*Hitachi*: p. 259, Fig. 7; ¶ 2 (interface, Timer 2, is driven by an external TIMER input).

2. *Claim 2*

The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.

As discussed in section B(2) above, the claimed "fixed-frequency clock" should be reasonably construed to mean an external clock that has a frequency fixed by its source and not share the frequency variations of the on-chip clock.

It is inherent that *Hitachi*'s second clock, which has no connection to the on-chip clock, would have its frequency fixed by its source, and not by the frequency variations of the on-chip clock. Therefore, considering also the discussion of claim 1 above, the combination of *Hitachi* and *Boney* renders all elements of claim 2 obvious to one of ordinary skill in 1989, and claim 2 should be rejected.

3. *Claim 3*

(a) ***In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:***

As discussed in sections F(1)(a) and (b) above, *Hitachi* discloses that the HD6805W1 integrated circuit chip includes a microprocessor and also discloses a method for clocking the microprocessor.

(b) ***providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;***

As discussed in sections F(1)(b) and (c) above, *Hitachi* discloses that the integrated circuit includes both the microprocessor and a system clock that is entirely on-chip, and *Boney* discloses that the on-chip clock has a ring oscillator. Given the similarity of feature and function, it would have been obvious to one skilled in the art of 1989 to combine the teachings of *Boney* and *Hitachi* to use the on-chip clock of *Boney* as the on-chip clock of *Hitachi*. As the applicant argued during prosecution of the '336 patent, it is inherent that the clock and microprocessor, constructed in the same integrated circuit, by the same processing technology, would have operating characteristics that vary together.

(c) ***using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;***

As discussed in sections F(1)(b) and (c) above, *Hitachi* discloses that the on-chip clock is variable in speed and clocks the microprocessor. Therefore, it is inherent that the microprocessor operates at a variable frequency dependent on the speed of the clock.

(d) ***providing an on chip input/output interface for the microprocessor integrated circuit; and***

As discussed in section F(1)(d) above, *Hitachi* discloses that the HD6805W1 chip includes an input/output interface, Timer 2, which is connected to the microprocessor.

(e) ***clocking the input/output interface with a second clock independent of the ring oscillator system clock.***

As discussed in section F(1)(e) above, *Hitachi* discloses that Timer 2 may be driven by either an internal, on-chip clock or an external "TIMER." It is inherent that the external TIMER, which has no connection to the on-chip clock, would be independent of the on-chip clock.

Because the combination of *Hitachi* and *Boney* renders every element of claim 3 obvious to one of ordinary skill in 1989 and it would have been obvious to combine their teachings, claim 3 is unpatentable.

4. *Claim 4*

The method of claim 3 in which the second clock is a fixed frequency clock.

It is inherent that *Hitachi*'s second clock, which has no connection to the on-chip clock, would have its frequency fixed by its source and not by the frequency variations of the on-chip clock. Therefore, considering also the discussion of claim 3 above, the combination of *Hitachi* and *Boney* renders all elements of claim 4 obvious to one of ordinary skill in 1989, and claim 4 should be rejected.

5. *Claim 5*

The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.

Hitachi discloses that the on-chip oscillator is connected to and clocks the microprocessor. (p. 252, Block Diagram). The microprocessor exchanges data with the input/output interface's OCR and ICR registers ("Read/Write" and "Read" operations, respectively), and the external TIMER is not connected to the OCR or ICR. (p. 259, Fig. 7; ¶¶ 3-5, Output Compare Register and Input Capture Register). Therefore, it is inherent that the exchange of data between the CPU, which is driven by the on-chip ring oscillator, and the OCR and ICR registers of Timer 2, which have no connection with the external TIMER, would be in synchrony with the ring oscillator.

Thus, considering also the discussion of claim 3 above, claim 5 should be rejected as being obvious over *Hitachi* in light of *Boney*.

III. CONCLUSION

For the reasons stated herein, Requester respectfully submits that the cited references raise substantial new questions of patentability as to claims of the '336 Patent and *ex parte* reexamination should be commenced. Furthermore, Requester submits that claims 1-10 of the '336 Patent are unpatentable over the prior art cited in this Petition and should be canceled by the Office.

Please find the attached modified Form PTO/SB/08 listing the patents and cited prior art, herein relied upon or referred to as well as Appendix I, and a copy of the patent of which reexamination is requested.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that relief is required for proper consideration of this request, Requester petitions for any required relief necessary to initiate the reexamination requested herein.

January 30, 2007

Date

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IV. CERTIFICATION OF SERVICE

The undersigned certifies that a copy of this Request for *Ex Parte* Reexamination in its entirety, including all accompanying documents, is being deposited with the U.S. Postal Service as Express Mail on the date of the signature below in an envelope addressed to the attorney of record for the assignee of U.S. Patent No. 5,809,336 as provided for in 37 C.F.R. § 1.33(c):

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APPENDIX I