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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 11/14/2009

Please find below and/or attached an Office communication concerning this application or proceeding.

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EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/009,457*.

PATENT NO. *5809336*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Order Granting / Denying Request For Ex Parte Reexamination	Control No.	Patent Under Reexamination	
	90/009,457	5809336	
	Examiner	Art Unit	
	B. James Peikari	3992	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

The request for *ex parte* reexamination filed *24 August 2009* has been considered and a determination has been made. An identification of the claims, the references relied upon, and the rationale supporting the determination are attached.

Attachments: a)☐ PTO-892, b)☒ PTO/SB/08, c)☐ Other: _____

1. ☒ The request for *ex parte* reexamination is GRANTED.

RESPONSE TIMES ARE SET AS FOLLOWS:

For Patent Owner's Statement (Optional): TWO MONTHS from the mailing date of this communication (37 CFR 1.530 (b)). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).**

For Requester's Reply (optional): TWO MONTHS from the **date of service** of any timely filed Patent Owner's Statement (37 CFR 1.535). **NO EXTENSION OF THIS TIME PERIOD IS PERMITTED.** If Patent Owner does not file a timely statement under 37 CFR 1.530(b), then no reply by requester is permitted.

2. ☐ The request for *ex parte* reexamination is DENIED.

This decision is not appealable (35 U.S.C. 303(c)). Requester may seek review by petition to the Commissioner under 37 CFR 1.181 within ONE MONTH from the mailing date of this communication (37 CFR 1.515(c)). **EXTENSION OF TIME TO FILE SUCH A PETITION UNDER 37 CFR 1.181 ARE AVAILABLE ONLY BY PETITION TO SUSPEND OR WAIVE THE REGULATIONS UNDER 37 CFR 1.183.**

In due course, a refund under 37 CFR 1.26 (c) will be made to requester:

a) ☐ by Treasury check or,

b) ☐ by credit to Deposit Account No. _____, or

c) ☐ by credit to a credit card account, unless otherwise notified (35 U.S.C. 303(c)).

cc:Requester (if third party requester)

RESPONSE TO REQUEST FOR *EX PARTE* REEXAMINATION

1. The Request filed August 24, 2009 alleges that there is a substantial new question of patentability (SNQ) affecting claims 1-10 of U.S. Patent Number 5,809,336 (the '336 patent) based on the following prior art references:

(1) U.S. Patent No. 4,853,841 to Richter ("Richter").

(2) U.S. Patent No. 4,348,743 to Dozier ("Dozier").

(3) Mostek Corporation, Mostek 1981: 3870 Microcomputer Data Book. Carrollton, TX: Mostek, Feb. 1981; pp. III-101 to III-129 & VI-1 to VI-11 ("Mostek").

(4) U.S. Patent No. 4,931,748 to McDermott et al ("McDermott").

(5) U.S. Patent No. 4,766,567 to Kato ("Kato").

(6) U.S. Patent No. 4,691,124 to Ledzius et al ("Ledzius").

(7) Howell, Dave, ed., IC Master 1980. Garden City, NY: United Technical Publications, 1980; pp. 2016-2040 ("IC Master").

Information Disclosure Statement

2. Regarding the information disclosure statement filed April 24, 2009:

(1) References 17 and 18 have been considered by the examiner. However, these citations have been lined through on the Form PTO/SB/08 (or PTO-1449) so as not to be published on the reexamination certificate because they fail to constitute patents or printed publications in accordance with 37 CFR 1.97, 1.98 and MPEP § 609.

Documents that are not patents or printed publications that are the basis of reexamination as described in 37 CFR 1.501(a), 37 CFR 1.510(a) and (b)(3), and MPEP 2256 (for ex parte reexamination) or 37 CFR 1.913, 37 CFR 1.915(b)(2) and MPEP 2656 (for inter partes reexamination). Although MPEP 609.06 provides for printing on the patent face of citations listed on a Forms PTO/SB/08, it applies to information available for reference purposes, as opposed to information as to concurrent proceedings (Office actions, litigation papers, etc.) which are addressed by MPEP 2282 and MPEP 2686, and as opposed to declarations/affidavits which are addressed by MPEP 2258 and 2658.

(2) References 19 and 20 have been considered by the examiner. However, these citations have been lined through on the Form PTO/SB/08 (or PTO-1449) because they have not been made in accordance with 37 CFR § 1.98(b)(5), which states "Each publication listed in an information disclosure statement must be identified by publisher, author (if any), title, relevant pages of the publication, date, and place of publication".

Proper citations of references 19 and 20 appear in section 1 of this Office action. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

(3) A cover page from "EDN" magazine, dated November 20, 1976, appears to have been attached to the Mostek reference. This page has not been listed on the IDS or mentioned in the Request. It has not been considered.

Brief Overview of the Patent

3. The '336 patent is directed to a microprocessor system (*see Figure 17 below*) having a central processing unit (*70*) and a ring oscillator (*430*) providing a variable speed system clock for the microprocessor. The central processing unit and ring oscillator variable speed system clock each include a plurality of electronic devices of like type, which allows the central processing unit to operate at a variable processing frequency dependent upon a variable speed of the ring oscillator variable speed system clock. The microprocessor system may also include an input/output interface (*432*) that is independently clocked by a second clock (*434*).

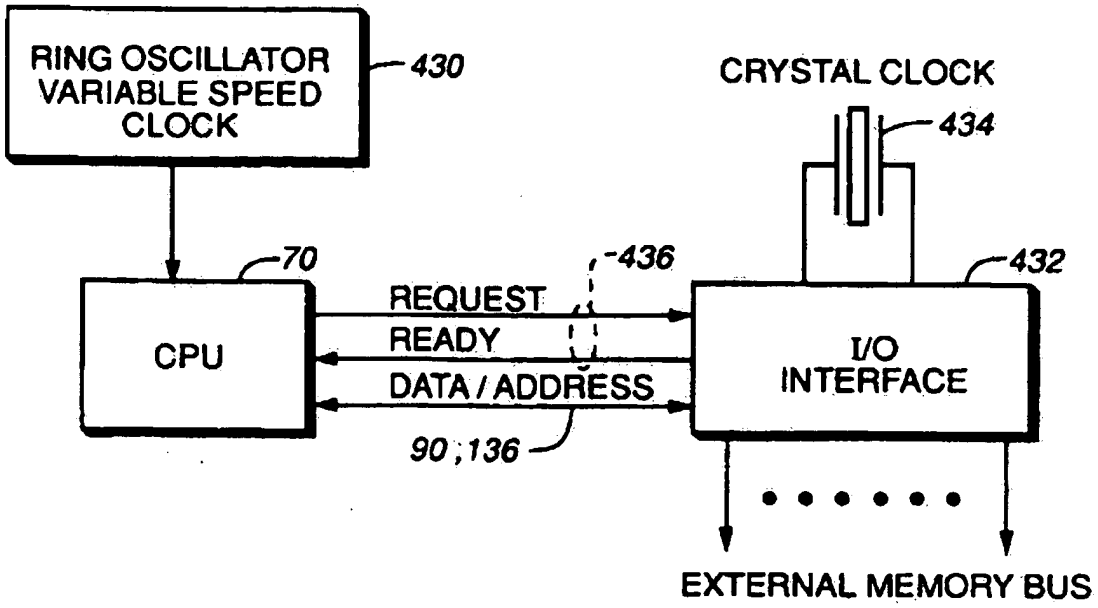

FIG._17

Prosecution History

4. The '336 patent matured from U.S. Patent Application No. 08/484,918, whose relevant prosecution history may be summarized as follows:

- The application was filed on June 7, 1995 with claims 1-70, as a divisional of U.S. Patent Application No. 07/389,334, filed on August 3, 1989.
- A non-final office action was mailed by the USPTO December 12, 1995. Claims 1-18, 22- 64 and 68-70 are indicated as being cancelled. Claims 19-21 and 65-67 were rejected under 35 USC 112, second paragraph. Claims 19 and 65 were rejected under 35 USC 103 as being unpatentable in view of Sheets (U.S. Patent 4,670,837). Claims 20-21 and 66-67 were rejected under 35 USC 103 as being unpatentable in view of Sheets (U.S. Patent 4,670,837) and Schaire (U.S. Patent 4,453,229).
- Applicant submitted a reply on April 15, 1996. Claims 19-20 and 65-66 were amended. Claims 71-79 were added.
- A final office action was mailed by the USPTO on July 8. 1996. Claims 19-21, 65-67 and 71-79 were rejected under 35 USC 112, second paragraph. Claims 65-67, 72 and 78-79 were rejected under 35 USC 101. Claims 65-67 and 72-79 were rejected under 35 USC 112, first paragraph. Claims 19, 65, 73-74 and 77-78 were rejected under 35 USC 103 as being unpatentable in view of Sheets (U.S. Patent 4,670,837). Claims 20-21, 71-72, 66-67, 75-76 and 79 were rejected under 35 USC 103 as being unpatentable in view of Sheets (U.S. Patent 4,670,837) and Schaire (U.S. Patent 4,453,229).

- Applicant submitted a reply on January 13, 1997 including amendments to claims 65, 66, 72 and 73.
- A non-final office action was mailed by the USPTO on April 3, 1997. Claims 19-21, 65-67 and 72-79 were rejected under 35 USC 103 as being unpatentable in view of Magar (U.S. Patent 4,503,500) and Pelgrom et al (U.S. Patent 4,627,082).
- Applicant submitted a reply on July 7, 1997, including an amendment to claim 73.
- A non-final office action was mailed by the USPTO on October 16, 1997. Claims 19-21, 65-67 and 72-79 were rejected under 35 USC 103 as being unpatentable in view of Magar (U.S. Patent 4,503,500).
- Applicant submitted a reply on February 10, 1998 including amendments to claims 65, 73 and 78.
- An interview was held with the primary patent examiner on April 23, 2008 in which an agreement was reached with respect to claims 19, 20, 65, 66, 73 75, 78 and 79.
- Applicant submitted a reply on April 24, 1998 amending claim 78 and cancelling claims 20, 66, 75 and 79.
- A notice of allowance was mailed by the USPTO on May 13, 1998. Examiner's amendments were presented to claims 20, 65, 66 and 75. Claims 19, 21, 65, 67, 72-74 and 76-78 were indicated as allowed. The allowed claim set was re-numbered as being claims 1-10 in the paper file jacket.
- On September 15, 1998, the application issued as U.S. Patent No. 5,809,336.

SNQs Raised in the Request

5. The Requester identified the following SNQs (see Request, pages i-ii):

- **Issue 1:** A SNQ as to claims 1-7, 9 and 10 is raised by Mostek in view of IC Master.
- **Issue 2:** A SNQ as to claims 6, 7 and 10 is raised by Mostek in view of IC Master and further in view of Ledzius.
- **Issue 3:** A SNQ as to claims 1-5, 8 and 9 is raised by Mostek in view of Kato, further in view of IC Master, and further in view of Ledzius.
- **Issue 4:** A SNQ as to claims 1-10 is raised by Dozier.
- **Issue 5:** A SNQ as to claims 1-10 is raised by Dozier in view of Mostek and further in view of IC Master, and further in view of Kato, and further in view of Ledzius.
- **Issue 6:** A SNQ as to claims 1-10 is raised by Richter.
- **Issue 7:** A SNQ as to claims 6, 7 and 10 is raised by Richter in view of Ledzius.
- **Issue 8:** A SNQ as to claims 8 and 9 is raised by Richter in view of Ledzius and further in view of Kato.
- **Issue 9:** A SNQ as to claims 1-5 is raised by Richter in view of Ledzius and further in view of Kato, and further in view of McDermott.

6. The Requester also discussed the patentability of claims proposed in a copending reexamination proceeding.

Discussion of SNQs

7. A prior art patent or printed publication raises a substantial new question of patentability where there is:

> (A) a substantial likelihood that a reasonable Examiner would consider the prior art patent or printed publication important in deciding whether or not the claim is patentable, MPEP §2242 (I) and,
>
> (B) the same question of patentability as to the claim has not been decided in a previous or pending proceeding or in a final holding of invalidity by a federal court. See MPEP §2242 (III).

For any reexamination ordered on or after November 2, 2002, reliance on previously cited/considered art, i.e., "old art," does not necessarily preclude the existence of a substantial new question of patentability that is based exclusively on that old art. Rather, determinations on whether a substantial new question of patentability exists in such an instance shall be based upon a fact-specific inquiry done on a case-by-case basis. See MPEP 2242.

Issue 1

A SNQ as to claims 1-7, 9 and 10 is raised by Mostek in view of IC Master.

8. Mostek is directed to a system (*note the MK3873*) having a single semiconductor chip containing a main control logic that is clocked by a variable internal oscillator (*see Mostek, Figure 1, page III-103*). The chip also includes a serial I/O port that can be clocked by a fixed frequency and an external clock that is independent of the internal oscillator.

IC Master is directed to a number of microprocessor systems. Of relevance is the F3870. In the description of the F3870 there is shown a variable internal oscillator (*see IC Master, pages*

2019). Furthermore, IC Master discloses variable frequencies of the on-chip oscillator and temperature and V_{cc} variations on the same pages (*see IC Master, pages 2024-2026*), suggesting that the frequency of the on-chip oscillator may vary in response to "stresses" such as temperature and voltage variations.

Mostek and IC Master appear compatible with each other, since each was directed to a microprocessor system that utilized a variable internal oscillator. When combined, these references would teach a system a system having a single semiconductor chip containing a main control logic that is clocked by a variable internal oscillator, wherein the frequency of the on-chip oscillator may vary in response to temperature and variations and wherein a serial I/O port can be clocked by a fixed frequency and an external clock that is independent of the internal oscillator, which it appears the examiner considered to be allowable features of claims 1-10.

The Request has neither shown any explicit teaching nor provided any discussion of obviousness and/or motivation to utilize a ring oscillator as the variable internal oscillator in the Mostek or the IC Master systems. Instead, the request relies on an allegation of an admission by the patent owner, but provides no evidence of such an admission. Further, the Request has not demonstrated how such an admission would establish the obviousness of such a feature to one having ordinary skill in the art at the time the invention was made. Therefore the question of the obviousness of utilizing a ring oscillator in the combination of Mostek and IC Master has yet to be addressed.

9. There is a substantial likelihood that a reasonable examiner would consider the combination of Mostek and IC Master important in deciding the patentability of the claims of the '336 patent. Mostek and IC Master are not of record in the file of the '336 patent and are not cumulative to the art of record in the original file. The teachings of Mostek and IC Master were not subject to a final holding of invalidity by a federal court.

Accordingly, it is **agreed** that the combination of Mostek and IC Master raises a substantial new question of patentability as to claims 1-10.

Issue 2

A SNQ as to claims 6, 7 and 10 is raised by Mostek in view of IC Master and further in view of Ledzius.

10. In addition to the teachings of Mostek and IC Master described above, Ledzius teaches a clock generator (*18*) for providing clock signals to various components of an integrated circuit. The clock generator (*18*) varies to reflect process variations throughout the circuit and temperature variances. Ledzius teaches that the integrated circuit includes one or more data ports. Ledzius further teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in process variations throughout the circuit (*see column 4, lines 12-22*). Ledzius further teaches that the "frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances" (*see column 4, lines 9-22*).

Ledzius appears compatible with Mostek and IC Master, since each was directed to clock generation in a microprocessor system. When combined, these references would teach a system

a system having a single semiconductor chip containing a main control logic that is clocked by a variable internal oscillator, wherein the frequency of the on-chip oscillator may vary in response to temperature and variations and wherein a serial I/O port can be clocked by a fixed frequency and an external clock that is independent of the internal oscillator and manufacturing such circuits from the same batch and section of semiconductor wafer, which it appears the examiner considered to be allowable features of claims 6, 7 and 10.

11. There is a substantial likelihood that a reasonable examiner would consider the combination of Mostek, IC Master and Ledzius important in deciding the patentability of the claims of the '336 patent. Ledzius is not of record in the file of the '336 patent and is not cumulative to the art of record in the original file. The teachings of Ledzius were not subject to a final holding of invalidity by a federal court.

Accordingly, it is **agreed** that the combination of Mostek, IC Master and Ledzius raises a substantial new question of patentability as to claims 6, 7 and 10.

Issue 3

A SNQ as to claims 1-5, 8 and 9 is raised by Mostek in view of Kato, further in view of IC Master, and further in view of Ledzius.

12. In addition to the teachings of Mostek, IC Master and Ledzius described above, Kato is directed to an integrated circuit having a first clock generator (*see Figure 4, element 141*) which can be a ring oscillator (*see column 10, lines 67-68*).

Kato appears compatible with Mostek, IC Master and Ledzius, since each was directed to clock generation in an integrated circuit system. When combined, these references would teach a system a system having a single semiconductor chip containing a main control logic that is clocked by a variable internal ring oscillator, wherein the frequency of the on-chip oscillator may vary in response to temperature and variations and wherein a serial I/O port can be clocked by a fixed frequency and an external clock that is independent of the internal oscillator and manufacturing such circuits from the same batch and section of semiconductor wafer, which it appears the examiner considered to be allowable features of claims 1-5, 8 and 9.

13. There is a substantial likelihood that a reasonable examiner would consider the combination of Mostek, Kato, IC Master and Ledzius important in deciding the patentability of the claims of the '336 patent. Kato is not of record in the file of the '336 patent and is not cumulative to the art of record in the original file. The teachings of Kato were not subject to a final holding of invalidity by a federal court.

Accordingly, it is **agreed** that the combination of Mostek, Kato, IC Master and Ledzius raises a substantial new question of patentability as to claims 1-5, 8 and 9.

Issue 4

A SNQ as to claims 1-10 is raised by Dozier.

14. Dozier is directed to a system having a microprocessor that is implemented on a single semiconductor chip, contains a main control logic that is clocked by an internal oscillator, and

has input/output ports. Specifically, the Dozier discloses a "microprogrammed computer 10 which may be implemented by MOS/LSI techniques and which may be fabricated on a single semiconductor chip" (*see column 2, lines 60-63*). Dozier further teaches that the clock generator 38 of the microprogrammed computer includes "an internal oscillator which is activated when both the XTL 1 and XTL 2 pins are grounded." This internal oscillator provides clocking signals for the Main Control Logic. The main cycle clock signal generated by the clock generator 38 "is the cycle clock for the computer system 10" (*see column 5, lines 9-14 and 5, lines 27-28*).

Dozier additionally teaches a test mode for the microprogrammed computer 10, whereby information on one of the ports is immediately fed into the data bus at a rate not synchronized with the clock generator. Specifically, in the test mode "port 5 will take the information existing on its pins and drive it into the internal data bus [which] permits port 5 to be a dedicated input to the internal data bus" (*see column 3, lines 62-66*). Likewise, the I/O port 4 logic block will take the data from the data bus and supply it directly to its output pins. This operation is not synchronized with the main cycle clock signal (*see column 3, lines 54-57*).

Thus, Dozier appears to teach a system a system having a single semiconductor chip containing a main control logic that is clocked by a variable internal oscillator, wherein the frequency of the on-chip oscillator may vary and wherein a serial I/O port can be clocked by a fixed frequency and an external clock that is independent of the internal oscillator, which it appears the examiner considered to be allowable features of claims 1-10.

The Request has neither shown any explicit teaching nor provided any discussion of obviousness and/or motivation to utilize a ring oscillator as the variable internal oscillator in the Dozier system. Instead, the request relies on an allegation of an admission by the patent owner,

but provides no evidence of such an admission. Further, the Request has not demonstrated how such an admission would establish the obviousness of such a feature to one having ordinary skill in the art at the time the invention was made. Therefore the question of the obviousness of utilizing a ring oscillator in the Dozier system has yet to be addressed.

15. There is a substantial likelihood that a reasonable examiner would consider Dozier important in deciding the patentability of the claims of the '336 patent. Dozier is not of record in the file of the '336 patent and is not cumulative to the art of record in the original file. The teachings of Dozier were not subject to a final holding of invalidity by a federal court.

Accordingly, it is **agreed** that Dozier raises a substantial new question of patentability as to claims 1-10.

Issue 5

A SNQ as to claims 1-10 is raised by Dozier in view of Mostek and further in view of IC Master, and further in view of Kato, and further in view of Ledzius.

16. The systems of Dozier, Mostek, IC Master, Kato and Ledzius. have been described above.

Dozier, Mostek, IC Master, Kato and Ledzius appear compatible with each other, since each was directed to clock generation in an integrated circuit system. When combined, these references would teach a system a system having a single semiconductor chip containing a main control logic that is clocked by a variable internal ring oscillator, wherein the frequency of the

on-chip oscillator may vary in response to temperature and variations and wherein a serial I/O port can be clocked by a fixed frequency and an external clock that is independent of the internal oscillator and manufacturing such circuits from the same batch and section of semiconductor wafer, which it appears the examiner considered to be allowable features of claims 1-10.

17. There is a substantial likelihood that a reasonable examiner would consider the combination of Dozier, Mostek, IC Master, Kato and Ledzius important in deciding the patentability of the claims of the '336 patent.

Accordingly, it is **agreed** that the combination of Dozier, Mostek, IC Master, Kato and Ledzius raises a substantial new question of patentability as to claims 1-10.

Issue 6

A SNQ as to claims 1-10 is raised by Richter.

18. Richter is directed to a microprocessor system having a "voltage-controlled oscillator" for generating "a clock pulse 'ftakt' that acts upon the microprocessor system." (*see column 3, lines 18-20*). In some embodiments the 'ftakt' signal is used as both the system clock and a clock for the I/O port. (*see column 4, lines 34-43*). In other embodiments Richter teaches that the microprocessor is clocked by a "separate system clock generator for the microprocessor 2." (*see column. 4, lines 34-38*). Richter further teaches an embodiment in which the microprocessor system 2 is provided "in a one-chip system" with a microprocessor, RAM and ROM memory chips, a serial interface, and "other chips required for their operation."

Thus, Richter appears to teach a system a system having a single semiconductor chip containing a main control logic that is clocked by a variable internal oscillator, wherein the frequency of the on-chip oscillator may vary and wherein a serial I/O port can be clocked by a fixed frequency and an external clock that is independent of the internal oscillator, which it appears the examiner considered to be allowable features of claims 1-10.

The Request has neither shown any explicit teaching nor provided any discussion of obviousness and/or motivation to utilize a ring oscillator as the variable internal oscillator in the Richter system. Instead, the request relies on an allegation of an admission by the patent owner, but provides no evidence of such an admission. Further, the Request has not demonstrated how such an admission would establish the obviousness of such a feature to one having ordinary skill in the art at the time the invention was made. Therefore the question of the obviousness of utilizing a ring oscillator in the Richter system has yet to be addressed.

19. There is a substantial likelihood that a reasonable examiner would consider Richter important in deciding the patentability of the claims of the '336 patent. Richter is not of record in the file of the '336 patent and is not cumulative to the art of record in the original file. The teachings of Richter were not subject to a final holding of invalidity by a federal court.

Accordingly, it is **agreed** that Richter raises a substantial new question of patentability as to claims 1-10.

Issue 7

A SNQ as to claims 6, 7 and 10 is raised by Richter in view of Ledzius.

20. The systems of Richter and Ledzius have been described above.

Richter and Ledzius appear compatible, since both were directed to clock generation in a microprocessor system. When combined, these references would teach a system a system having a single semiconductor chip containing a main control logic that is clocked by a variable internal oscillator, wherein the frequency of the on-chip oscillator may vary in response to temperature and variations and wherein a serial I/O port can be clocked by a fixed frequency and an external clock that is independent of the internal oscillator and manufacturing such circuits from the same batch and section of semiconductor wafer, which it appears the examiner considered to be allowable features of claims 6, 7 and 10.

21. There is a substantial likelihood that a reasonable examiner would consider the combination of Richter and Ledzius important in deciding the patentability of the claims of the '336 patent.

Accordingly, it is **agreed** that the combination of Richter and Ledzius raises a substantial new question of patentability as to claims 6, 7 and 10.

Issue 8

A SNQ as to claims 8 and 9 is raised by Richter in view of Ledzius and further in view of Kato.

22. The systems of Richter, Ledzius and Kato have been described above.

Richter, Ledzius and Kato appear compatible with each other, since each was directed to clock generation in an integrated circuit system. When combined, these references would teach a system a system having a single semiconductor chip containing a main control logic that is clocked by a variable internal ring oscillator, wherein the frequency of the on-chip oscillator may vary in response to temperature and variations and wherein a serial I/O port can be clocked by a fixed frequency and an external clock that is independent of the internal oscillator and manufacturing such circuits from the same batch and section of semiconductor wafer, which it appears the examiner considered to be allowable features of claims 8 and 9.

23. There is a substantial likelihood that a reasonable examiner would consider the combination of Richter, Ledzius and Kato important in deciding the patentability of the claims of the '336 patent.

Accordingly, it is **agreed** that the combination of Richter, Ledzius and Kato raises a substantial new question of patentability as to claims 8 and 9.

Issue 9

A SNQ as to claims 1-5 is raised by Richter in view of Ledzius and further in view of Kato, and further in view of McDermott.

24. In addition to the teachings of Richter, Ledzius and Kato described above, McDermott is directed to a "voltage controlled oscillator" that resides on a single integrated circuit and clocks the entire microcomputer (*see column 3, lines 17-21 and 57-63, and column 4, lines 24-29*).

McDermott appears compatible with Richter, Ledzius and Kato, since each was directed to clock generation in an integrated circuit system. When combined, these references would teach a system a system having a single semiconductor chip containing a main control logic that is clocked by a variable internal ring oscillator, wherein the frequency of the on-chip oscillator may vary in response to temperature and variations and wherein a serial I/O port can be clocked by a fixed frequency and an external clock that is independent of the internal oscillator and manufacturing such circuits from the same batch and section of semiconductor wafer, which it appears the examiner considered to be allowable features of claims 1-5.

25. There is a substantial likelihood that a reasonable examiner would consider the combination of Richter, Ledzius, Kato and McDermott important in deciding the patentability of the claims of the '336 patent. McDermott is not of record in the file of the '336 patent and is not cumulative to the art of record in the original file. The teachings of McDermott were not subject to a final holding of invalidity by a federal court.

Accordingly, it is **agreed** that the combination of Richter, Ledzius, Kato and McDermott raises a substantial new question of patentability as to claims 1-5.

Claims Proposed in a Copending Reexamination Proceeding

26. Regarding the discussion of claims 11-20, proposed by and amendment in a copending reexamination proceeding, these claims do not exist in the original patent and have not been placed in effect within the Moore et al patent by the issuance of a reexamination certificate.

A pending proposed amendment in a pending reexamination proceeding is not in effect within a patent, since it not part of the original patent text nor added to the patent through the issuance of a reexamination certificate. MPEP 2242 states:

"However, in order for the second or subsequent request for reexamination to be granted, the second or subsequent requester must independently provide a substantial new question of patentability which is different from that raised in the pending reexamination for the claims in effect at the time of the determination *The decision on the second or subsequent request is thus based on the claims in effect at the time of the determination (37 CFR 1.515(a)).* *If a 'different' substantial new question of patentability is not provided by the second or subsequent request for the claims in effect at the time of the determination, the second or subsequent request for reexamination must be denied since the Office is only authorized by statute to grant a reexamination proceeding based on a substantial new question of patentability 'affecting any claim of the patent.' See 35 U.S.C. 303. Accordingly, there must be at least one substantial new question of patentability established for the existing claims in the patent in order to grant reexamination."* (emphasis added)

Consequently, **no substantial new question of patentability is raised in this reexamination proceeding with respect to claims 11-20, since these claims are not in effect in the patent at the time this determination is made.**

Conclusion

27. Claims 1-10 are subject to reexamination.

Waiver of Right to File Patent Owner Statement

28. In a reexamination proceeding, Patent Owner may waive the right under 37 C.F.R. 1.530 to file a Patent Owner Statement. The document needs to contain a statement that Patent Owner waives the right under 37 C.F.R. 1.530 to file a Patent Owner Statement and proof of service in the manner provided by 37 C.F.R. 1.248, if the request for reexamination was made by a third party requester, see 37 C.F.R 1.550(f).

Service of Papers

29. After filing of a request for ex parte reexamination by a third party requester, any document filed by either the patent owner or the third party requester must be served on the other party (or parties where two or more third party requester proceedings are merged) in the reexamination proceeding in the manner provided in 37 CFR 1.248. The document must reflect service or the document may be refused consideration by the Office. See 37 CFR 1.550(f).

Extensions of Time

30. Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that *ex parte* reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extensions of time in *ex parte* reexamination proceedings are provided for in 37 CFR 1.550(c).

Litigation Reminder

31. The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving the patent throughout the course of this reexamination proceeding. The third party requester is also reminded of the ability to similarly apprise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP §§ 2207, 2282 and 2286.

All correspondence relating to this *ex parte* reexamination proceeding should be directed:

By Mail to: Mail Stop *Ex Parte* Reexam
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand to: Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Registered users of EFS-Web may alternatively submit such correspondence via the electronic filing system EFS-Web, at https://sportal.uspto.gov/authenticate/authenticateuserlocalepf.html. EFS-Web offers the benefit of quick submission to the particular area of the Office that needs to act on the correspondence. Also, EFS-Web submissions are "soft scanned" (i.e., electronically uploaded) directly into the official file for the reexamination proceeding, which offers parties the opportunity to review the content of their submissions after the "soft scanning" process is complete.

Any inquiry concerning this communication should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

B. James Peikari
Primary Examiner
Central Reexamination Unit 3992

EBK

04/24/09

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Sheet 1 of 1

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 24567-0002RX1	Application No.
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		~~Applicant~~ Inventors: Moore et al.	
		Filing Date 8/24/09	Group Art Unit 3992

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	1	5,809,336	09/1998	Moore et al			
	2	4,853,841	08/1989	Richter			
	3	4,348,743	09/1982	Dozier			
	4	4,931,748	06/1990	McDermott et al.			
	5	4,766,567	08/1988	Kato			
	6	4,691,124	09/1987	Ledzius et al.			
	7						
	8						
	9						
	10						
	11						

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	12							
	13							
	14							
	15							
	16							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	~~17~~	~~Relevant portions of the '336 patent file history~~
	~~18~~	~~Relevant portions of the merged '336 reexamination (Control No. 90/008,474)~~
	~~19~~	~~Mostek, 3870 Microcomputer Data Book (Feb. 1981)~~
	~~20~~	~~IC Master 1980 (United Technical Publications) (1980)~~

Examiner Signature	Date Considered
/B. James Peikari/	11/11/2009

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form (PTO-1449)

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /BJP/

Search Notes	Application/Control No.	Applicant(s)/Patent under Reexamination
	90/009,457	5809336
	Examiner	Art Unit
	B. James Peikari	3992

SEARCHED			
Class	Subclass	Date	Examiner

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
Review of the prosecution history of U.S. Patent No. 5,809,336.	11/11/2009	BJP