I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent and Trademark Office on October 29, 2009.

/Larry E. Henneman, Jr./
By: Larry E. Henneman, Jr., Reg. No. 41,063

PATENT
Attorney Docket No.: 0081-011D3C1X1
Merged with: 0081-011D3C1X2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Ex Parte Reexamination:

Control No.: 90/008,227
Filed: September 21, 2006

merged with

Control No.: 90/010,562
Filed: May 29, 2009

For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

U.S. Patent No. 6,598,148

Examiner: Pokrzywa, Joseph R.

Technology Center/Art Unit: 3992

TRANSMITTAL FOR:

AMENDMENT CONFORMING MERGED EX PARTE REEXAMINATION PROCEEDINGS

Mail Stop ***Ex Parte Reexamination***
Central Reexamination Unit
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith for filing in the above-referenced merged reexamination proceedings are the following documents:

1. Amendment Conforming Merged Ex Parte Reexamination Proceedings (6 pages); and
2. Certification of Service (2 pages).

October 29, 2009

Respectfully submitted,

/Larry E. Henneman, Jr./

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Mail Stop ***Ex Parte Reexamination***
Central Reexamination Unit
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated October 2, 2009, please enter the following amendments and remarks:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 5 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Original) A microprocessor integrated circuit comprising:

a program-controlled processing unit operative in accordance with a sequence of program instructions;

a memory coupled to said processing unit and capable of storing information provided by said processing unit;

a plurality of column latches coupled to the processing unit and the memory, wherein, during a read operation, a row of bits are read from the memory and stored in the column latch; and

a variable speed system clock having an output coupled to said processing unit;

said processing unit, said variable speed system clock, said plurality of column latches, and said memory fabricated on a single substrate, said memory using a greater area of said single substrate than said processing unit, said memory further using a majority of a total area of said single substrate.

2. (Original) The microprocessor integrated circuit of claim 1 wherein said memory is dynamic random-access memory.

3. (Original) The microprocessor integrated circuit of claim 1 wherein said memory is static random-access memory.

4. (Original) A microprocessor integrated circuit comprising:

a processing unit disposed upon an integrated circuit substrate, said processing unit operating in accordance with a predefined sequence of program instructions;

a memory coupled to said processing unit and capable of storing information provided by said processing unit, said memory occupying a larger area of said integrated circuit substrate than said processing unit said memory further occupying a majority of a total area of said single substrate; and

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said integrated circuit substrate.

5. (Original) The microprocessor integrated circuit of claim 4 wherein said memory is dynamic random-access memory.

6. (Original) The microprocessor integrated circuit of claim 4 wherein said memory is static random-access memory.

7. (Original) The microprocessor integrated circuit of claim 4 wherein said memory is capable of supporting read and write operations.

8. (Cancelled).

9. (Amended) [The microprocessor integrated circuit of claim 8] A microprocessor integrated circuit comprising:

a processing unit having one or more interface ports for interprocessor communication, said processing unit being disposed on a single substrate;

a memory disposed upon said substrate and coupled to said processing unit, said memory occupying a greater area of said substrate than said processing unit, said memory further comprising a majority of a total area of said substrate; and

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said substrate;

wherein a first of said interface ports includes a column latch, said column latch facilitating serial communication through said first of said interface ports.

10. (Cancelled).

11. (Original) A microprocessor computational system comprising:

a first processing unit disposed upon a first substrate;

a first memory disposed upon said first substrate and coupled to said first processing unit, said first memory occupying a greater area of said first substrate than said first processing unit, said memory further occupying a majority of a total area of said substrate;

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said first substrate; and

a second processing unit coupled to said first processing unit and configured for interprocessor communication with said first processing unit.

12. (Original) The microprocessor computational system of claim 11 wherein said second processing unit and a second memory are disposed upon a second substrate, said second memory occupying a greater area of said second substrate than said second processing unit said second memory further occupying a majority of a total area of said substrate.

13. (Original) The multiprocessor computational system of claim 11 wherein said first processing unit includes an interface port for establishing said interprocessor communication between an internal register of said first processing unit and second processing unit.

14. (New) The microprocessor integrated circuit of claim 4 wherein the memory comprises a plurality of physically separate memory portions.

15. (New) The microprocessor integrated circuit of claim 4 wherein the total area is an area provided by an entire top surface of the single substrate.

REMARKS

This "housekeeping amendment" is filed in response to the Decision *Sua Sponte* Merging Reexamination Proceedings dated October 2, 2009, whereby reexamination control number 90/008,227 ("the '227 proceeding") and reexamination control number 90/010,562 ("the '562 proceeding") were merged. The purpose of this amendment is solely to conform the specification and claims of the merged reexamination proceedings.

The amendments made herein are made with respect to the originally issued Claims 1-13 of U.S. Patent No. 6,598,148. Claim 9 is amended, and Claims 8 and 10 are cancelled. Claims 1-7 and 11-13 remain as originally issued. New Claims 14 and 15 are added.

The prosecution history of the '227 proceeding is different than the prosecution history of the '562 proceeding. For example, new claims have been added to the '227 proceeding, and some, but not all, of those claims have been subsequently canceled. In particular, new Claims 14-25 were added by the amendment of February 21, 2008. Subsequently, by the amendment of August 25, 2008 Claims 15-18 and 21-24 were canceled, and by the amendment of March 27, 2009 Claims 8, 10, 20 and 25 were canceled. As a result, Claims 1-7, 9, 11-14, and 19 remained in the '227 proceeding. In contrast, there have been no amendments filed in the '562 proceeding, so that original Claims 1-13 remained in the '562 proceeding.

In order to file duplicate original amendments in each of the merged reexamination proceedings that conform the claims of the '227 proceeding and the '562 proceeding, Patent Owners hereby withdraw all previously filed amendments in the '227 proceeding, and the amendments made herein are made with respect to the original issued claims of U.S. Patent No. 6,598,148. This appears to Patent Owners to be the only way to conform the claims of the '227 proceeding with the claims of the '562 proceeding, including conforming the claim numbering of the newly added claims.

No amendments to the specification have been made in either the '227 proceeding nor the '562 proceeding, and none are made herein.

CONCLUSION

If the Examiner has any questions regarding this amendment, he is invited to telephone the undersigned at 269-279-8820.

Respectfully submitted,

October 29, 2009

/Larry E. Henneman, Jr./

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reexamination of: U.S. Patent No.: 6,598,148 Reexamination Control No.:: 90/008,227 Filed: September 21, 2006 merged with: Reexamination Control No.:: 90/010,562 Filed: May 29, 2006 Titled: HIGH PERFORMANCE MICRO-PROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK	Customer No.: 40972 Examiner: Joseph R. Pokrzywa Art Unit: 3992 CERTIFICATION OF SERVICE UNDER 37 C.F.R. §1.510(b)(5) and MPEP §2220

CERTIFICATION OF SERVICE

The undersigned hereby certifies pursuant to 37 C.F.R. §1.550(f) and MPEP §2266.03 that a complete copy of the attached papers (Amendment Conforming Merged Ex Parte Reexamination Proceedings) is being served via first class mail, simultaneously with the filing of this paper, upon the attorneys of record for the third party reexamination requestors in a manner provided by 37 C.F.R. §1.248:

Martin J. Cosenza
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Date: October 29, 2009

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CERTIFICATE OF MAILING (37 CFR 1.8(A))

I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent and Trademark Office on October 16, 2009

Date: October 29, 2009 /Larry E. Henneman, Jr./
Larry E. Henneman, Jr.

Electronic Acknowledgement Receipt

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Application Number:	90008227
International Application Number:	
Confirmation Number:	6167
Title of Invention:	HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK
First Named Inventor/Applicant Name:	6598148
Customer Number:	40972
Filer:	Larry E. Henneman
Filer Authorized By:	
Attorney Docket Number:	0081-011D3C1X1
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1	Trans Letter filing of a response in a reexam	Transmittal.pdf	80567 da5915052db7c4a69aeff06c12053bc9ee795589	no	1

Warnings:	
Information:	

2	Response after non-final action-owner timely	MergerAmendment.pdf	104557 eeda7e02733b1c49dfe3bd40133c2485fb27689f	no	6
Warnings:					
Information:					
3	Reexam Certificate of Service	ServiceCert.pdf	66537 a835fa9a6232ed5526556193248b72805000593a	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	251661	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.