INTERVIEW SUMMARY

An in person interview was held at the U.S. Patent and Trademark Office on March 3, 2009 to discuss the outstanding Office Action dated January 26, 2009. The participants in the interview included Examiner Joseph Pokrzywa, Examiner Sue Lao, Examiner Roland Foster, and Applicant's attorney Larry Henneman. Applicants appreciate the opportunity to have the interview and especially the constructive and cooperative spirit of all three of the examiners that participated in the interview.

First, the rejections under 35 U.S.C. §103 over USPN 4,956,811 (Kajigaya) in view of USPN 4,660,180 (Tanimura et al.) were discussed. Mr. Henneman pointed out that Kajigaya and Tanimura et al. were both directed to dynamic random access memories (DRAMs) and that neither reference disclosed a ring oscillator clocking a processing unit. Examiner Pokrzywa confirmed that the column address decoder (C-DCR), the row address decoder (R-DCR), and the multiplexer (MPX) of Tanimura et al. (FIG. 1) were collectively considered to be the claimed processing unit. Mr. Henneman objected to the characterization of these combinational logic devices as a processing unit. Examiner Pokrzywa indicated that the broadest reasonable interpretation of "processing unit" did not exclude the cited elements of Tanimura et al. Mr. Henneman pointed out that there was no evidence that one skilled in the electronic arts would consider the elements of the cited reference a "processing unit." It was agreed that Applicants would clarify in the record that a processing unit is a device that executes program instructions. Examiner Foster suggested providing multiple examples from Applicants' patent to demonstrate that the term "processing unit" was used consistently to describe a device that processes program instructions. Examiner Lao suggested providing a dictionary definition of "processing unit" to establish that processing units necessarily process program instructions. It was agreed that the instruction processing aspect of the term "processing unit" could be clarified on the record without amending the claims.

Mr. Henneman further pointed out that neither Kajigaya nor Tanimura et al. disclose a "processing unit operating in accordance with a predefined sequence of program instructions," as recited in Claim 4. Examiner Pokrzywa disagreed, citing the control signals SC, NE, SR, and MS of Kajigaya as "a predefined sequence of program instructions." Mr.

Henneman disagreed and pointed out that the "control signals" of Kajigaya are configuration voltages set by physically bonding pads FP1 and FP0 (FIG. 33) to ground or V_{CC}. Mr. Henneman further pointed out that, once pads FP1 and FP0 are bonded (i.e., the device is physically configured), the "control signals" remain constant, as shown in Table 1 (col. 13, lines 42-54), and are not sequenced in any way. Therefore, the control signals could not be considered to be "a sequence of program instructions." Examiner Pokrzywa indicated that he would need additional time to fully consider this argument.

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REMARKS/ARGUMENTS

In response to the Office Action dated January 26, 2009, Applicants respectfully request reconsideration and allowance.

Response to Arguments

Applicants thank the Examiner for the withdrawal of the rejections from the Office Action dated June 25, 2008.

Claims Subject to Reexamination

Claims 1-13 issued as part of U.S. 6,598,148 (the '148 patent) and remain in this patent. Claims 4, 7, 8, and 10 were initially subject to reexamination. Claims 14-25 were previously added, claims 15-18 and 21-24 were previously canceled without prejudice, and by this Response claims 8, 10, 20, and 25 have been canceled without prejudice, leaving claims 4, 7, 14, and 19 subject to reexamination. Claim 9, which is not subject to reexamination and which previously depended from independent claim 8, has been amended into independent form including the limitations of claim 8.

Rejections Under 35 USC §103

Kajigaya in view of Tanimura

Claims 4, 7, 8, 10, 14, 19, 20, and 25 stand rejected under 35 USC §103(a) as being anticipated by by U.S. Pat. No. 4,956,811 (Kajigaya) in view of U.S. Pat. No. 4,660,180 (Tanimura). Claims 8, 10, 20, and 25 have been canceled without prejudice, rendering the rejection of these claims moot.

Kajigaya

Kajigaya discusses a semiconductor memory as opposed to a microprocessor integrated circuit as recited in claim 4, albeit in the preamble. In FIG. 32, an overall block

diagram of a DRAM according to Kajigaya, a DRAM includes a redundant address control circuit (RAC), a voltage generating circuit (VG), and a timing generating circuit (TG).

The Examiner has agreed that Kajigaya does not teach a ring oscillator clocking a processor unit as recited, but asserted that Kajigaya teaches a "processing unit operating in accordance with a predefined *sequence* of program instructions" (emphasis supplied) as recited in the claims. Office Action dated January 26, 2009 (OA) at paragraphs 4-5. The Examiner cited column 4, lines 34-39 of Kajigaya, that read:

> "Each circuit of the dynamic type RAM is supplied with internal control signals SC, NE, SR and MS for setting an operating mode from a common section COM of a timing generating circuit TG, the internal control signals being combined with each other in correspondence with the designated operating mode. More specifically, the internal control signals SC, NE, SR and MS are formed in a predetermined combination by selectively bonding the operating mode setting pads FP0, FP1 and the circuit ground potential or the power supply voltage Vcc."

The Examiner then concluded that the internal control signals were "instruction signals" that were combined in "predefined combinations" to control the circuit, include processing unit RAC. *Id.* From this, the Examiner concluded that the internal control signal taught a "predefined *sequence* of program instructions" (emphasis supplied) that operated the processing unit, RAC. OA at ¶¶ 5, 12.

Kajigaya's control signals noted by the Examiner set one of a defined set of operating modes, and are not the recited sequence of program instructions. There is no suggestion that any *sequence* of these control signals is needed to set an operating mode. In fact, it is clear that were Kajigaya's control signals to change in a sequence, no reliable operating mode could be set, nor would the circuit operate.

Tanimura

Tanimura discusses a DRAM with an "improved" data refreshing arrangement. Referring to FIGS. 1-2, a timer circuit TM supplies a timing pulse φ_T for use in periodically starting a refresh circuit REFC. Col. 10, ll. 52-56. The refresh circuit REFC supplies address

signals to a multiplexer MPX to indicate memory cells to be refreshed. Col. 11, ll. 39-43; Col. 12, ll. 2-4. The multiplexer MPX supplies the address signals to a row address decoder R-DCR that uses the address signals to form word line selection signals for selecting word lines in a memory array. Col. 3, ll. 24-30. A column address decoder C-DCR uses address signals to form and supply data line selection signals to the memory array. Col. 3, ll. 34-40.

The REFC circuit includes a ring oscillator that controls the time interval between refreshes. Circuit timing, however, is provided by circuit element TG. The timing circuit TG operates independently of the refresh circuit REFC. The REFC circuit provides no circuit timing, let alone a system clock.

Claims 4, 7, 14, and 19

Applicants respectfully assert that claims 4, 7, 14, and 19 are patentable over Kajigaya in view of Tanimura. Kajigaya and Tanimura fail to teach, disclose, or suggest at least: (1) a processing unit operating in accordance with a predefined *sequence* of program instructions, or (2) a ring oscillator that provides a *system clock* to the processing unit, as recited in independent claim 4, and thus also in claims 7, 14, and 19 that depend from claim 4.

Kajigaya's RAC Fails to Teach the Recited Processing Unit

The Examiner asserted that FIGS. 23-24 and 32-33, and col. 4, lines 18-44 and col. 15, lines 10-51 teach the recited processing unit operating in accordance with a sequence of program instructions. OA, ¶12. The cited figures and text discuss a redundant address control circuit (RAC). The DRAM discussed in Kajigaya, including the RAC, has a number of operating modes: first page mode, static column mode, nibble mode, mask write mode, and serial mode that are set based on the bonding of mode setting external terminals FP0 and FP1. FIG. 1; col. 13, lines 27-54; col. 15, lines 24-39. The Examiner asserted that the RAC is operating in accordance with a predefined sequence of program instructions, i.e., the control signals SC, NE, SR, and MS of Kajigaya.

The processing unit operating in accordance with a predefined sequence of program instructions requires a device configured to execute the program instructions. The recitation in the preamble of claim 4 that the claim is to a microprocessor cabins the fair range of

construction of "a processing unit operating in accordance with a predefined sequence of program instructions." A microprocessor, as of the filing of the application that resulted in U.S. 6,598,148, was known by those skilled in the art to mean a "mechanism that accepts a program as input, prepares it for execution, and executes the process so defined with data to produce results." IEEE Standard Dictionary of Electrical and Electronics Terms, Fourth Edition, July 8, 1988 (definition of "processor"). Further, the specification shows that the broadest reasonable interpretation consistent with the specification of the recited processing unit is a device configured to execute the predefined sequence of program instructions. (Col. 4, ll. 1-3 "Microprocessor 50 includes a central processing unit (CPU) 70."; Col. 4, ll. 62-64 "Most instructions execute in 20 nanoseconds in the microprocessor 50. The microprocessor can therefore execute instructions at 50 peak MIPS . . . ."; Col. 5, ll. 41-52; Col. 10, ll. 35-43; Col. 14, ll. 2-4; Col. 14, ll. 6-8; Col. 16, ll. 43-51; Col. 17, ll. 23-24; Col. 18, ll. 13-16; Col. 18, ll. 44-46; Col. 22, l. 40 – Col. 25, l. 50).

Conversely, the RAC in Kajigaya is not a microprocessor processing unit operating in accordance with a predefined sequence of program instructions as recited in claim 4. First, while microprocessors universally operate using a "predefined sequence of program instructions," where instructions comprising opcodes such as "add," subtract" "load" and "store" are provided in sequence to the microprocessor for execution, DRAMs do not operate on anything even remotely analogous. DRAMs instead respond to addresses and control signals, such as read and write. While DRAM memories can be configured to operate in different modes as shown by Kajigaya, they will not and cannot operate on a sequence of such operating modes. Kajigaya is a DRAM memory and is not a microprocessor as claimed. Second, Kajigaya's control signals SC, NE, SR, and MS are not a sequence of program instructions. Kajigaya's control signals are signals for setting an operating mode (Col. 13, ll. 27-54), not program instructions. The control signals are produced by selectively bonding mode setting external terminals FP0 and FP1 (Abstract; Col. 4, ll. 17-23 and 39-44). Further, even if the control signals are assumed to be program instructions, there is no teaching of a predefined sequence of the program instructions. Indeed, the control signals are "formed in a predetermined combination by selectively bonding the operating mode setting pads FP0, FP1 and the circuit

ground potential or the power supply voltage Vcc." Col. 4, ll. 39-44. The control signals are thus fixed, as shown in Table 1 (Col. 13, ll. 42-54), and not a sequence of program instructions. Third, Kajigaya's RAC does not execute the control signals, which set the operating mode, but are not executable instructions.

Moreover, using the control signals in a predefined sequence runs counter to the discussion of Kajigaya. If the control signals were changed in a sequence akin to a microprocessor program, the operating modes would also change in the same sequence: e.g., from first page mode, to serial, to nibble, etc. Changing operating modes in this fashion would prevent the DRAM memory from being useful. It simply would not operate properly, if at all.

Tanimura's Multiplexer, Row Address Decoder, and Column Address Decoder Fail to Teach the Recited Processing Unit

The Examiner asserted that the multiplexer MPX, row address decoder R-DCR and column address decoder C-DCR are "a processing unit disposed upon an integrated circuit substrate." OA at p. 9. The Examiner did not assert or explain how these devices operate in accordance with a predefined sequence of program instructions. Indeed, they do not. The row and column decoders form word and data line selection signals, respectively, in accordance with address signals received from the multiplexer and a column address buffer C-ADB, respectively. FIG. 1. The multiplexer receives address signals from a row address buffer R-ADB and a reference circuit REF and supplies the address signals from either the row address buffer or the reference circuit in accordance with a switching signal φ_{MX}. Col. 4, ll. 8-17. There is no teaching that there is a predefined sequence, even if the address signals and switching signals are assumed to be program instructions. Therefore, Tanimura fails to teach or suggest the recited processing unit.

Tanimura's Ring Oscillator Does Not Provide a System Clock to a Processing Unit as Recited

The Examiner agreed with Applicants that Kajigaya fails to suggest that it's ring oscillator provides a system clock for the recited processing unit, but the Examiner asserted that Tanimura's timer circuit teaches the recited ring oscillator that provides a system clock to the

recited processing unit. OA, p. 9, citing Tanimura, col. 15, l. 67 – col. 16, l. 22. The cited text of Tanimura discusses that a timer circuit TM (FIG. 2) may include a ring oscillator. The timer circuit TM supplies a timing pulse φ_T for use in starting a refresh circuit REFC. Col. 10, ll. 52-56. The refresh circuit REFC supplies address signals to a multiplexer MPX to indicate memory cells to be refreshed. Col. 11, ll. 39-43; Col. 12, ll. 2-4. The timer circuit TM does not supply a system clock at all, let alone a system clock to a processing unit (that can execute instructions) operating in accordance with a predefined sequence of program instructions as recited. Indeed, timing signals are provided by a separate timing signal generator circuit TG.

For at least these reasons, Kajigaya and Tanimura fail to teach or suggest the recited processing unit operating in accordance with a predefined sequence of program instructions or to teach or suggest the recited ring oscillator that provides a system clock to the processing unit. Thus, for at least these reasons, independent claim 4 is, and claims 7, 14, and 19 that depend from claim 4 are, patentable over Kajigaya in view of Tanimura.

Bagula in view of Tanimura

Claims 4, 7, 8, 14, 19, 20 and 25 stand rejected under 35 USC §103(a) as being unpatentable over "A 5V Self-Adaptive Microcomputer with 16Kb of #2 Program Storage and Security," 1983 IEEE International Solid-State Circuits Conference, pp. 34-35 (Bagula) in view of Tanimura. Claims 8, 20, and 25 have been canceled without prejudice, rendering the rejection of these claims moot.

Bagula

Bagula discusses a microprocessor modified to include EEROM memory with program security features. Bagula includes RAM, ROM, EEROM, and employs an external, off-chip crystal oscillator that provides a 10 MHz input clock signal (FIG. 1) and a divider circuit that provides a 400 ns microcycle. p. 34, col. 2. The Bagula system clock is provided directly by the external oscillator. Bagula fails to disclose a ring oscillator associated in any fashion with the system clock.

Claims 4, 7, 14, and 19

Applicants respectfully assert that claims 4, 7, and 14-19 are patentable over Bagula in view of Hashimoto. Bagula in view of Hashimoto fails to teach, disclose, or suggest at least a processing unit operating in accordance with a predefined sequence of program instructions and a ring oscillator that provides a system clock to the processing unit, as recited in independent claim 4. This failure is further a failure to teach as least this same feature of claims 7, 14, and 19 that depend from claim 4.

The Examiner agreed that the use of a ring oscillator to provide a refresh signal to a memory, combined with Bagula, did not render obvious the recited ring oscillator that provides a system clock to a processing unit. On pages 4-5 of the Office Action, the Examiner agreed that Bagula's microprocessor in view of Hashimoto's (U.S. 4,882,710) ring oscillator that provides a read control signal RACT, a write control signal WACT, and (apparently) a refresh control signal RFACT, did not render obvious the ring oscillator as recited in claim 4.

The Examiner asserted that Bagula teaches an oscillator with a variable output frequency, but not a ring oscillator. OA at p. 16. The Examiner, however, asserted that Tanimura's timer circuit teaches the recited ring oscillator that provides a system clock to the recited processing unit. OA at p. 17, citing Tanimura, col. 15, l. 67 – col. 16, l. 22. The cited text of Tanimura discusses that a timer circuit TM (FIG. 2) may include a ring oscillator. The timer circuit TM supplies a timing pulse φ_T for use in starting a refresh circuit REFC. Col. 10, ll. 52-56. The refresh circuit REFC supplies address signals to a multiplexer MPX to indicate memory cells to be refreshed. Col. 11, ll. 39-43; Col. 12, ll. 2-4. The timer circuit TM thus does not supply a system clock at all, let alone a system clock to a processing unit (that can execute instructions) operating in accordance with a predefined sequence of program instructions as recited. Indeed, timing signals are provided by a separate timing signal generator circuit TG. Tanimura's timer circuit supplies a memory refresh signal, much like Hashimoto which the Examiner agreed does not, even when combined with Bagula, render obvious the recited ring oscillator that provides a system clock to a processing unit.

Further, there is no suggestion to combine Tanimura's ring oscillator with Bagula to achieve the microprocessor recited in claim 4. Tanimura's ring oscillator provides a start

signal to a refresh circuit of a DRAM, not a system clock to a mechanism such as Bagula's CPU. Thus, it would not have been obvious to a person of skill in the art to use Tanimura's ring oscillator to provide a system clock to Bagula's CPU as suggested by the Examiner. To combine Tanimura with Bagula to conclude that the recited microprocessor is obvious, is to infer teachings not present in the references, and then use improper hindsight to combine the improperly inferred teachings.

For at least these reasons, Bagula in view of Tanimura fails to teach or suggest the ring oscillator that provides a system clock to a processing unit operating in accordance with a sequence of program instructions as recited in claim 4. Thus, for at least these reasons independent claim 4 is, and claims 7, 14, and 19 that depend from claim 4 are, patentable over Bagula in view of Tanimura.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 269-279-8820.

Respectfully submitted,

March 27, 2009

/Larry E. Henneman, Jr./

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Original) A microprocessor integrated circuit comprising:

a program-controlled processing unit operative in accordance with a sequence of program instructions;

a memory coupled to said processing unit and capable of storing information provided by said processing unit;

a plurality of column latches coupled to the processing unit and the memory, wherein, during a read operation, a row of bits are read from the memory and stored in the column latch; and

a variable speed system clock having an output coupled to said processing unit;

said processing unit, said variable speed system clock, said plurality of column latches, and said memory fabricated on a single substrate, said memory using a greater area of said single substrate than said processing unit, said memory further using a majority of a total area of said single substrate.

2. (Original) The microprocessor integrated circuit of claim 1 wherein said memory is dynamic random-access memory.

3. (Original) The microprocessor integrated circuit of claim 1 wherein said memory is static random-access memory.

4. (Original) A microprocessor integrated circuit comprising:

a processing unit disposed upon an integrated circuit substrate, said processing unit operating in accordance with a predefined sequence of program instructions;

a memory coupled to said processing unit and capable of storing information provided by said processing unit, said memory occupying a larger area of said integrated circuit

substrate than said processing unit said memory further occupying a majority of a total area of said single substrate; and

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said integrated circuit substrate.

5. (Original) The microprocessor integrated circuit of claim 4 wherein said memory is dynamic random-access memory.

6. (Original) The microprocessor integrated circuit of claim 4 wherein said memory is static random-access memory.

7. (Original) The microprocessor integrated circuit of claim 4 wherein said memory is capable of supporting read and write operations.

8. (Cancelled).

9. (Amended) ~~The microprocessor integrated circuit of claim 8~~ A microprocessor integrated circuit comprising:

a processing unit having one or more interface ports for interprocessor communication, said processing unit being disposed on a single substrate;

a memory disposed upon said substrate and coupled to said processing unit, said memory occupying a greater area of said substrate than said processing unit, said memory further comprising a majority of a total area of said substrate; and

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said substrate;

wherein a first of said interface ports includes a column latch, said column latch facilitating serial communication through said first of said interface ports.

10. (Cancelled).

11. (Original) A microprocessor computational system comprising:

a first processing unit disposed upon a first substrate;

a first memory disposed upon said first substrate and coupled to said first processing unit, said first memory occupying a greater area of said first substrate than said first processing unit, said memory further occupying a majority of a total area of said substrate;

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said first substrate; and

a second processing unit coupled to said first processing unit and configured for interprocessor communication with said first processing unit.

12. (Original) The microprocessor computational system of claim 11 wherein said second processing unit and a second memory are disposed upon a second substrate, said second memory occupying a greater area of said second substrate than said second processing unit said second memory further occupying a majority of a total area of said substrate.

13. (Original) The multiprocessor computational system of claim 11 wherein said first processing unit includes an interface port for establishing said interprocessor communication between an internal register of said first processing unit and second processing unit.

14. (Previously Presented) The microprocessor integrated circuit of claim 4 wherein the memory comprises a plurality of physically separate memory portions.

15. (Canceled).

16. (Canceled).

17. (Canceled).

18. (Canceled).

19. (Previously Presented) The microprocessor integrated circuit of claim 4 wherein the total area is an area provided by an entire top surface of the single substrate.

1 20. (Canceled).

1 21. (Canceled).

1 22. (Canceled).

1 23. (Canceled).

1 24. (Canceled).

25. (Canceled).

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The Examiner asserted that FIGS. 23-24 and 32-33, and col. 4, lines 18-44 and col. 15, lines 10-51 teach the recited processing unit operating in accordance with a sequence of program instructions. OA, ¶12. The cited figures and text discuss a redundant address control circuit (RAC). The DRAM discussed in Kajigaya, including the RAC, has a number of operating modes: first page mode, static column mode, nibble mode, mask write mode, and serial mode that are set based on the bonding of mode setting external terminals FP0 and FP1. FIG. 1; col. 13, lines 27-54; col. 15, lines 24-39. The Examiner asserted that the RAC is operating in accordance with a predefined sequence of program instructions, i.e., the control signals SC, NE, SR, and MS of Kajigaya.

The processing unit operating in accordance with a predefined sequence of program instructions requires a device configured to execute the program instructions. The recitation in the preamble of claim 4 that the claim is to a microprocessor cabins the fair range of

construction of "a processing unit operating in accordance with a predefined sequence of program instructions." A microprocessor, as of the filing of the application that resulted in U.S. 6,598,148, was known by those skilled in the art to mean a "mechanism that accepts a program as input, prepares it for execution, and executes the process so defined with data to produce results." IEEE Standard Dictionary of Electrical and Electronics Terms, Fourth Edition, July 8, 1988 (definition of "processor"). Further, the specification shows that the broadest reasonable interpretation consistent with the specification of the recited processing unit is a device configured to execute the predefined sequence of program instructions. (Col. 4, ll. 1-3 "Microprocessor 50 includes a central processing unit (CPU) 70."; Col. 4, ll. 62-64 "Most instructions execute in 20 nanoseconds in the microprocessor 50. The microprocessor can therefore execute instructions at 50 peak MIPS . . . ."; Col. 5, ll. 41-52; Col. 10, ll. 35-43; Col. 14, ll. 2-4; Col. 14, ll. 6-8; Col. 16, ll. 43-51; Col. 17, ll. 23-24; Col. 18, ll. 13-16; Col. 18, ll. 44-46; Col. 22, l. 40 – Col. 25, l. 50).

Conversely, the RAC in Kajigaya is not a microprocessor processing unit operating in accordance with a predefined sequence of program instructions as recited in claim 4. First, while microprocessors universally operate using a "predefined sequence of program instructions," where instructions comprising opcodes such as "add," subtract" "load" and "store" are provided in sequence to the microprocessor for execution, DRAMs do not operate on anything even remotely analogous. DRAMs instead respond to addresses and control signals, such as read and write. While DRAM memories can be configured to operate in different modes as shown by Kajigaya, they will not and cannot operate on a sequence of such operating modes. Kajigaya is a DRAM memory and is not a microprocessor as claimed. Second, Kajigaya's control signals SC, NE, SR, and MS are not a sequence of program instructions. Kajigaya's control signals are signals for setting an operating mode (Col. 13, ll. 27-54), not program instructions. The control signals are produced by selectively bonding mode setting external terminals FP0 and FP1 (Abstract; Col. 4, ll. 17-23 and 39-44). Further, even if the control signals are assumed to be program instructions, there is no teaching of a predefined sequence of the program instructions. Indeed, the control signals are "formed in a predetermined combination by selectively bonding the operating mode setting pads FP0, FP1 and the circuit

ground potential or the power supply voltage Vcc." Col. 4, ll. 39-44. The control signals are thus fixed, as shown in Table 1 (Col. 13, ll. 42-54), and not a sequence of program instructions. Third, Kajigaya's RAC does not execute the control signals, which set the operating mode, but are not executable instructions.

Moreover, using the control signals in a predefined sequence runs counter to the discussion of Kajigaya. If the control signals were changed in a sequence akin to a microprocessor program, the operating modes would also change in the same sequence: e.g., from first page mode, to serial, to nibble, etc. Changing operating modes in this fashion would prevent the DRAM memory from being useful. It simply would not operate properly, if at all.

Tanimura's Multiplexer, Row Address Decoder, and Column Address Decoder Fail to Teach the Recited Processing Unit

The Examiner asserted that the multiplexer MPX, row address decoder R-DCR and column address decoder C-DCR are "a processing unit disposed upon an integrated circuit substrate." OA at p. 9. The Examiner did not assert or explain how these devices operate in accordance with a predefined sequence of program instructions. Indeed, they do not. The row and column decoders form word and data line selection signals, respectively, in accordance with address signals received from the multiplexer and a column address buffer C-ADB, respectively. FIG. 1. The multiplexer receives address signals from a row address buffer R-ADB and a reference circuit REF and supplies the address signals from either the row address buffer or the reference circuit in accordance with a switching signal φ_{MX}. Col. 4, ll. 8-17. There is no teaching that there is a predefined sequence, even if the address signals and switching signals are assumed to be program instructions. Therefore, Tanimura fails to teach or suggest the recited processing unit.

Tanimura's Ring Oscillator Does Not Provide a System Clock to a Processing Unit as Recited

The Examiner agreed with Applicants that Kajigaya fails to suggest that it's ring oscillator provides a system clock for the recited processing unit, but the Examiner asserted that Tanimura's timer circuit teaches the recited ring oscillator that provides a system clock to the

recited processing unit. OA, p. 9, citing Tanimura, col. 15, l. 67 – col. 16, l. 22. The cited text of Tanimura discusses that a timer circuit TM (FIG. 2) may include a ring oscillator. The timer circuit TM supplies a timing pulse φ_T for use in starting a refresh circuit REFC. Col. 10, ll. 52-56. The refresh circuit REFC supplies address signals to a multiplexer MPX to indicate memory cells to be refreshed. Col. 11, ll. 39-43; Col. 12, ll. 2-4. The timer circuit TM does not supply a system clock at all, let alone a system clock to a processing unit (that can execute instructions) operating in accordance with a predefined sequence of program instructions as recited. Indeed, timing signals are provided by a separate timing signal generator circuit TG.

For at least these reasons, Kajigaya and Tanimura fail to teach or suggest the recited processing unit operating in accordance with a predefined sequence of program instructions or to teach or suggest the recited ring oscillator that provides a system clock to the processing unit. Thus, for at least these reasons, independent claim 4 is, and claims 7, 14, and 19 that depend from claim 4 are, patentable over Kajigaya in view of Tanimura.

Bagula in view of Tanimura

Claims 4, 7, 8, 14, 19, 20 and 25 stand rejected under 35 USC §103(a) as being unpatentable over "A 5V Self-Adaptive Microcomputer with 16Kb of #2 Program Storage and Security," 1983 IEEE International Solid-State Circuits Conference, pp. 34-35 (Bagula) in view of Tanimura. Claims 8, 20, and 25 have been canceled without prejudice, rendering the rejection of these claims moot.

Bagula

Bagula discusses a microprocessor modified to include EEROM memory with program security features. Bagula includes RAM, ROM, EEROM, and employs an external, off-chip crystal oscillator that provides a 10 MHz input clock signal (FIG. 1) and a divider circuit that provides a 400 ns microcycle. p. 34, col. 2. The Bagula system clock is provided directly by the external oscillator. Bagula fails to disclose a ring oscillator associated in any fashion with the system clock.

Claims 4, 7, 14, and 19

Applicants respectfully assert that claims 4, 7, and 14-19 are patentable over Bagula in view of Hashimoto. Bagula in view of Hashimoto fails to teach, disclose, or suggest at least a processing unit operating in accordance with a predefined sequence of program instructions and a ring oscillator that provides a system clock to the processing unit, as recited in independent claim 4. This failure is further a failure to teach as least this same feature of claims 7, 14, and 19 that depend from claim 4.

The Examiner agreed that the use of a ring oscillator to provide a refresh signal to a memory, combined with Bagula, did not render obvious the recited ring oscillator that provides a system clock to a processing unit. On pages 4-5 of the Office Action, the Examiner agreed that Bagula's microprocessor in view of Hashimoto's (U.S. 4,882,710) ring oscillator that provides a read control signal RACT, a write control signal WACT, and (apparently) a refresh control signal RFACT, did not render obvious the ring oscillator as recited in claim 4.

The Examiner asserted that Bagula teaches an oscillator with a variable output frequency, but not a ring oscillator. OA at p. 16. The Examiner, however, asserted that Tanimura's timer circuit teaches the recited ring oscillator that provides a system clock to the recited processing unit. OA at p. 17, citing Tanimura, col. 15, l. 67 – col. 16, l. 22. The cited text of Tanimura discusses that a timer circuit TM (FIG. 2) may include a ring oscillator. The timer circuit TM supplies a timing pulse φ_T for use in starting a refresh circuit REFC. Col. 10, ll. 52-56. The refresh circuit REFC supplies address signals to a multiplexer MPX to indicate memory cells to be refreshed. Col. 11, ll. 39-43; Col. 12, ll. 2-4. The timer circuit TM thus does not supply a system clock at all, let alone a system clock to a processing unit (that can execute instructions) operating in accordance with a predefined sequence of program instructions as recited. Indeed, timing signals are provided by a separate timing signal generator circuit TG. Tanimura's timer circuit supplies a memory refresh signal, much like Hashimoto which the Examiner agreed does not, even when combined with Bagula, render obvious the recited ring oscillator that provides a system clock to a processing unit.

Further, there is no suggestion to combine Tanimura's ring oscillator with Bagula to achieve the microprocessor recited in claim 4. Tanimura's ring oscillator provides a start

signal to a refresh circuit of a DRAM, not a system clock to a mechanism such as Bagula's CPU. Thus, it would not have been obvious to a person of skill in the art to use Tanimura's ring oscillator to provide a system clock to Bagula's CPU as suggested by the Examiner. To combine Tanimura with Bagula to conclude that the recited microprocessor is obvious, is to infer teachings not present in the references, and then use improper hindsight to combine the improperly inferred teachings.

For at least these reasons, Bagula in view of Tanimura fails to teach or suggest the ring oscillator that provides a system clock to a processing unit operating in accordance with a sequence of program instructions as recited in claim 4. Thus, for at least these reasons independent claim 4 is, and claims 7, 14, and 19 that depend from claim 4 are, patentable over Bagula in view of Tanimura.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 269-279-8820.

Respectfully submitted,

March 26, 2009

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