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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/008,227	09/21/2006	6598148	0081-011D3C1X1	6167

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EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 12/11/2009

Please find below and/or attached an Office communication concerning this application or proceeding.

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CENTRAL REEXAMINATION UNIT

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/008,227* & *90/010,562*

PATENT NO. *6598148*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

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Office Action in Ex Parte Reexamination	Control No. 90/008,227 & 90/010,562	Patent Under Reexamination 6598148	
	Examiner JOSEPH R. POKRZYWA	Art Unit 3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

a☒ Responsive to the communication(s) filed on *29 October 2009* . b☐ This action is made FINAL.
c☐ A statement under 37 CFR 1.530 has not been received from the patent owner.

A shortened statutory period for response to this action is set to expire *2* month(s) from the mailing date of this letter. Failure to respond within the period for response will result in termination of the proceeding and issuance of an *ex parte* reexamination certificate in accordance with this action. 37 CFR 1.550(d). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).** If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☒ Information Disclosure Statement, PTO/SB/08.
3. ☐ Interview Summary, PTO-474.
4. ☐ _____.

Part II SUMMARY OF ACTION

1a. ☒ Claims *4,6,7,11 and 13-15* are subject to reexamination.
1b. ☒ Claims *1-3,5,9 and 12* are not subject to reexamination.
2. ☒ Claims *8 and 10* have been canceled in the present reexamination proceeding.
3. ☐ Claims _____ are patentable and/or confirmed.
4. ☒ Claims *4,6,7,11 and 13-15* are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ The drawings, filed on _____ are acceptable.
7. ☐ The proposed drawing correction, filed on _____ has been (7a)☐ approved (7b)☐ disapproved.
8. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
   a)☐ All b)☐ Some* c)☐ None of the certified copies have
   1☐ been received.
   2☐ not been received.
   3☐ been filed in Application No. _____ .
   4☐ been filed in reexamination Control No. _____.
   5☐ been received by the International Bureau in PCT application No. _____.
   * See the attached detailed Office action for a list of the certified copies not received.
9. ☐ Since the proceeding appears to be in condition for issuance of an *ex parte* reexamination certificate except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte* Quayle, 1935 C.D. 11, 453 O.G. 213.
10. ☐ Other: _____

cc: Requester (if third party requester)

DETAILED ACTION

Brief Summary of Proceedings

1. In accordance with the Office Paper mailed 10/2/2009, the reexamination proceedings of 90/008,227 (noted as "the '8227 proceeding") and of 90/010,562 (noted as "the '10562 proceeding") have been merged. Both the '8227 proceeding and the '10562 proceeding are reexaminations of U.S. Patent Number 6,598,148 (hereafter "the '148 Patent"), whereby claims 1-13 of the '148 Patent originally issued to Charles Moore *et al.* on July 22, 2003.

2. In the '8227 proceeding, the Third Party requested reexamination of claims 4, 7, 8, and 10 in the Request dated 9/21/2006. Subsequently, numerous Office actions and Patent Owner responses were mailed. Subsequently, in the '10562 proceeding, the Third Party requested reexamination of claims 4, 6, 7, 11, and 13 of the '148 Patent. Thus, with respect to the original claims of the '148 Patent, claims 4, 6, 7, 8, 10, 11, and 13 are subject to the current reexamination. Further, the current Patent Owner's Supplemental Amendment dated 11/23/2009 has been entered and made of record. With the amendment dated 11/23/2009, claims 8 and 10 have been cancelled, and claims 14 and 15 were newly added. Therefore, the current reexamination proceeding is presently drawn to claims 4, 6, 7, 11, 13-15.

3. The examiner notes that this action is directed only to the claims for which reexamination was requested. With respect to such claims, the Third Party Requester(s) has alleged that a substantial new question of patentability (SNQ) exists, and upon review, it has been determined that the alleged SNQ in fact is present for claims 4, 6, 7, 8, 10, 11, and 13. No determination was made with respect to the existence or nonexistence of an SNQ with respect to any claim for which reexamination was not specifically requested.

Information Disclosure Statement

4. The references listed in the Information Disclosure Statement submitted on 7/2/2009 have been received and entered into the record.

5. Continuing, the examiner notes that the numerous Office actions from related U.S. patent applications and the numerous Court documents submitted in the above noted Information Disclosure Statement have been received, and considered, but are not proper to be listed on an Information Disclosure Statement, as the documents are not proper be printed on the face of a Reexamination Certificate, once issued. Thus, these citations have been indicated as having a line through the citation in the Information Disclosure Statement.

6. Further, the examiner notes that MPEP 2256, under the heading "Prior Art Patents and Printed Publications Reviewed by Examiner in Reexamination" states, in part:

> Where patents, publications, and other such items of information are submitted by a party (patent owner or requester) in compliance with the requirements of the rules, **the requisite degree of consideration to be given to such information will be normally limited by the degree to which the party filing the information citation has explained the content and relevance of the information**. The initials of the examiner placed adjacent to the citations on the form PTO/SB/08A and 08B or its equivalent, without an indication to the contrary in the record, do not signify that the information has been considered by the examiner any further than to the extent noted above. [Emphasis added.]

7. Additionally, MPEP 609.05(b) states:

> The information contained in information disclosure statements which comply with both the content requirements of 37 CFR 1.98 and the requirements, based on the time of filing the statement, of 37 CFR 1.97 will be considered by the examiner. Consideration by the examiner of the information submitted in an IDS means that **the examiner will consider the documents in the same manner as other documents in Office search files are considered by the examiner while conducting a search of the prior art in a proper field of search**. The initials of the examiner placed adjacent to the citations on the ** PTO/SB/08A and 08B or its equivalent mean that the information has been considered by the examiner to the extent noted above. [Emphasis added.]

8. With this, the examiner notes that the prior art references listed in the Information Disclosure Statement submitted on 7/2/2009 have been considered by the examiner to at least the "degree to which the party filing the information citation has explained the content and relevance of the information", and in "the same manner as other documents in Office search files are considered by the examiner while conducting a search of the prior art in a proper field of search" (see attached PTO/SB/08A).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claims 4, 6, 7, 14, and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kajigaya *et al.* (U.S. Patent Number 4,956,811, hereafter "Kajigaya") in view of Tanimura *et al.* (U.S. Patent Number 4,660,180, hereafter "Tanimura").

Regarding independent ***claim 4***, Kajigaya teaches of a microprocessor integrated circuit [see col. 3, lines 44-60, wherein "Circuit elements constituting each block shown in Fig. 32 and each of the circuit elements shown in Figs. 1-30 are, although not necessarily limitative, formed on a single semiconductor substrate such as a single crystal silicon by a known semiconductor integrated circuit manufacturing technique."] comprising:

a processing unit disposed upon an integrated circuit substrate [PC2, which includes for instance, "redundant address control circuit RAC", as read on col. 15, lines 10-23, and seen in Figs. 32 and 33; also see Figs. 23 and 24, being "circuit diagrams showing one example of a redundant address control circuit of a dynamic type RAM to which the present invention is applied", as noted in col. 3, lines 10-13],

said processing unit operating in accordance with a predefined sequence of program instructions [see col. 4, lines 18-44, whereby when the DRAM is adapted for the x 1 bit pattern,

the operating modes are programmed as "a first page mode, static column mode, nybble mode, and serial mode", and when the DRAM is adapted for the x 4 bit pattern, the operating modes are programmed as "first page mode, static column mode and serial mode, and mask write mode"; also see col. 15, lines 24-51];

a memory coupled to said processing unit and capable of storing information provided by said processing unit [memory arrays MARY0-MARY3, also see Figs. 32 and 33],

said memory occupying a larger area of said integrated circuit substrate than said processing unit said memory further occupying a majority of a total area of said single substrate [see Fig. 33, whereby memory arrays MARY0-MARY3 occupy the majority of the total area of the substrate]; and

a ring oscillator having a variable output frequency [see col. 12, lines 55-58, wherein "Each of the substrate back bias voltage generating circuits includes a ring oscillator having five CMOS inverter circuits..."; also see Fig. 6, whereby the timing generating circuit TG includes a plurality of odd number of inverters, being the defining feature of a ring oscillator],

wherein the ring oscillator provides a system clock to the processing unit [see Fig. 6, being the timing generating circuit TG],

the ring oscillator disposed on said integrated circuit substrate [see col. 12, lines 55-58, wherein "Each of the substrate back bias voltage generating circuits includes a ring oscillator having five CMOS inverter circuits...", also see col. 15, lines 10-23, wherein "At one end of the semiconductor substrate SUB, ...a peripheral circuit PC1 which includes the timing generating circuit TG...is disposed between the pads TF to A9 and the memory arrays MARY0 to MARY3."].

However, Kajigaya is unclear if the ring oscillator provides a system clock to the processing unit, or if the timing circuits that provide a system clock to the processing unit include a ring oscillator, as in Kajigaya, the ring oscillator is noted to generate the back bias voltage.

Tanimura describes a microprocessor integrated circuit [see Figs. 1 and 3] comprising:

a processing unit disposed upon an integrated circuit substrate [multiplexer MPX, row address decoder R-DCR and column address detector C-DCR],

a memory coupled to said processing unit and capable of storing information provided by said processing unit [see Figs. 1 and 4, memory arrays, see col. 5, lines 41-48, wherein "Fig. 4 shows only the memory array that corresponds to the data input/output terminal D0 (Fig. 1). Memory arrays which are the same as the memory array of Fig. 4 have also been provided for the other data input/output terminals D1 to D7."]; and

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit [see col. 15, line 67-col. 16, line 22, wherein "When the timer circuit TM substantially consists of a ring oscillator constituted, for example, by inverters (logic circuits) and when the delay time which is required for (or is inevitably formed in) the refresh control circuit REFC to form various signals responsive to the starting signal Φ, is formed by a delay circuit that is constituted by cascade-connected inverters (logic circuits), the delay time of each of the inverters (l[o]gic circuits) will change depending upon variance in the manufacturing conditions."],

the ring oscillator disposed on said integrated circuit substrate [see Fig. 1].

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to utilize a ring oscillator, as described within the timer circuit TM by Tanimura, as the system clock, being within the clocks described and shown by Kajigaya. Kajigaya & Tanimura are combinable because they are from the same field of endeavor, being commonly owned integrated circuit memory devices, which have memory arrays, a processing unit, and clock generators. The suggestion/motivation for doing so would have been that Kajigaya's system would be easily implemented to include a ring oscillator on the same substrate as the processor, therein allowing an internal system clock for the processing, as ring oscillators were well known at the time and commonly used as system clocks, as shown by Tanimura in col. 15, lines 37-col. 16, line 22. Therefore, it would have been obvious to combine the teachings of Tanimura with the system of Kajigaya to obtain the invention as specified in claim 4.

Regarding ***claim 6***, Kajigaya and Tanimura disclose the microprocessor integrated circuit discussed above in claim 4, and Kajigaya further teaches that said memory is static random-access memory [see col. 17, line 51-col.18, line 4, wherein "the present invention may also be applied to various other types of semiconductor memory such as static type RAMs."].

Regarding ***claim 7***, Kajigaya and Tanimura disclose the microprocessor integrated circuit discussed above in claim 4, and Kajigaya further teaches that said memory is capable of supporting read and write operations [see col. 4, line 45-col. 5, line 10; also see col. 15, lines 24-51].

Regarding ***claim 14***, Kajigaya and Tanimura disclose the microprocessor integrated circuit discussed above in claim 4, and Kajigaya further teaches that the memory comprises a plurality of physically separate memory portions [see Figs. 32 and 33, being memory arrays MARY0, MARY1, MARY2, and MARY3].

Regarding ***claim 15***, Kajigaya and Tanimura disclose the microprocessor integrated circuit discussed above in claim 4, and Kajigaya further teaches that the total area is an area provided by an entire top surface of the single substrate [see Fig. 33, also see col. 14, lines 52-65, wherein "the dynamic type RAM is, although not necessarily limitative, formed on a semiconductor substrate SUB which is defined by one single crystal silicon."].

11. **Claims 4, 7, 14, and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over "A 5V Self-Adaptive Microcomputer with 16Kb of E2 Program Storage and Security", written by Mark Bagula *et al.*, 1983 IEEE International Solid-State Circuits Conference, pages 34-35 (hereafter "Bagula") in view of Tanimura *et al.* (U.S. Patent Number 4,660,180, hereafter "Tanimura").

Regarding independent ***claim 4***, Bagula teaches of a microprocessor integrated circuit [see Figs. 1-4] comprising:

a processing unit disposed upon an integrated circuit substrate [see Fig. 4, "ALU and Temp Reg."],

said processing unit operating in accordance with a predefined sequence of program instructions [see page 34, col. 1, wherein "This architecture was chosen as the basis for this circuit because its microcoded instruction set and generalized building block type layout greatly facilitated the instruction set change and control circuit modifications necessary to implement EEROM memory"];

a memory coupled to said processing unit and capable of storing information provided by said processing unit [being the Microcode ROM , RAM and EEPROM Arrays, which comprise 48% of the die area],

said memory occupying a larger area of said integrated circuit substrate than said processing unit said memory further occupying a majority of a total area of said single substrate [see Figure 4; also see Table 1, wherein the memory arrays, which comprise 48% of the die area utilization, with 21.9% being "Interconnect unused area and scribe"; Thus, 48% of the active

areas on the substrate comprises a majority of a total area of active areas on the single substrate. This interpretation is reasonable, especially in light of the newly added dependent claim 18, which states "wherein the total area consists of a sum of **active areas of the single substrate**"]; and

an oscillator having a variable output frequency [see "Clock Generator" in Figure 4],

wherein *the oscillator* provides a system clock to the processing unit [see Figs. 1-4 on page 35, being the "Clock Generator"],

the oscillator disposed on said integrated circuit substrate [see "Clock Generator" in Fig. 4, whereby the "Clock Generator" is disposed on the substrate].

However, Bagula does not expressly disclose if the "Clock Generator", interpreted as the claimed "oscillator", is a ring oscillator.

Tanimura describes a microprocessor integrated circuit [see Figs. 1 and 3] comprising:

a processing unit disposed upon an integrated circuit substrate [multiplexer MPX, row address decoder R-DCR and column address detector C-DCR],

a memory coupled to said processing unit and capable of storing information provided by said processing unit [see Figs. 1 and 4, memory arrays, see col. 5, lines 41-48, wherein "Fig. 4 shows only the memory array that corresponds to the data input/output terminal D0 (Fig. 1). Memory arrays which are the same as the memory array of Fig. 4 have also been provided for the other data input/output terminals D1 to D7."]; and

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit [see col. 15, line 67-col. 16, line 22, wherein "When the timer circuit TM substantially consists of a ring oscillator constituted, for example, by inverters (logic circuits) and when the delay time which is required for (or is inevitably formed in) the refresh control circuit REFC to form various signals responsive to the starting signal Φ, is formed by a delay circuit that is constituted by cascade-connected inverters (logic circuits), the delay time of each of the inverters (l[o]gic circuits) will change depending upon variance in the manufacturing conditions."],

the ring oscillator disposed on said integrated circuit substrate [see Fig. 1].

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to utilize a ring oscillator, as described within the timer circuit TM by Tanimura, as the system clock, being within the clocks described and shown by Bagula. Bagula & Tanimura are combinable because they are from the same field of endeavor, integrated circuit memory devices, which have memory arrays, a processing unit, and clock generators. The suggestion/motivation for doing so would have been that Bagula's system would be easily implemented to include a ring oscillator on the same substrate as the processor, therein allowing an internal system clock for the processing, as ring oscillators were well known at the time and commonly used as system clocks, as shown by Tanimura in col. 15, lines 37-col. 16, line 22. Therefore, it would have been obvious to combine the teachings of Tanimura with the system of Bagula to obtain the invention as specified in claim 4.

Regarding ***claim 7***, Bagula and Tanimura disclose the microprocessor integrated circuit discussed above in claim 4, and Bagula further teaches that said memory is capable of supporting read and write operations [see page 34, col. 2, "Signature Read" and "Block write/clear"].

Regarding ***claim 14***, Bagula and Tanimura disclose the microprocessor integrated circuits discussed above in claim 4, and Bagula further teaches that the memory comprises a plurality of physically separate memory portions [see Fig. 4, being the EEROM, the RAM, and the ROM].

Regarding ***claim 15***, Bagula and Tanimura disclose the microprocessor integrated circuits discussed above in claim 4, and Bagula further teaches that the total area is an area provided by an entire top surface of the single substrate [see Fig. 4; also see Table 1].

12. **Claims 4, 7, 11, and 13-15** are rejected under 35 U.S.C. 103(a) as being unpatentable over "A 553K- Transistor LISP Processor Chip", written by Patrick W. Bosshart *et al.*, IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 5, October 1987 (hereafter the "LISP reference"), further in view of "A 553K-Transistor LISP Processor Chip", also written by Patrick W. Bosshart et al., IEEE International Solid-State Circuits Conference, February 26, 1987, pages 202, 203, and 402 (hereafter the "LISP Conference reference"), and further in view of U.S. Patent Number 4,763,297, issued to Uhlenhoff on Aug. 9, 1988 (hereafter "Uhlenhoff").

Regarding independent ***claim 4***, the LISP reference teaches of a microprocessor integrated circuit [see Figure 1 on page 808] comprising:

a processing unit disposed upon an integrated circuit substrate [being the "execution unit", see page 809, cols. 1 and 2, wherein "The execution unit" consists primarily of the ALU and rotator/masker..."],

said processing unit operating in accordance with a predefined sequence of program instructions [see page 809, col. 1];

a memory coupled to said processing unit and capable of storing information provided by said processing unit [on-chip RAM memory, see page 808; also see Fig. 2 on page 809],

said memory occupying a larger area of said integrated circuit substrate than said processing unit said memory further occupying a majority of a total area of said single substrate [see page 808, col. 2, wherein "The on-chip RAM's, which dominate chip area and transistor count, are described in Section VI..."; also see page 814, col. 2, wherein "...the large fraction of chip area consumed by memory..."; also see page 816, col. 2, wherein "Since the memories

occupy a large fraction of the chip area..."; also see the additional LISP Conference reference on page 402, which shows the identical photomicrograph of the LISP chip seen in Fig. 1 on page 808 of the LISP reference, but labeled to show that the on-chip memory occupies a greater area than the "execution unit", and also occupies a majority of the total area of the substrate.]; and

and a "clock" provided a system clock to the processing unit, and disposed on said integrated circuit substrate [see page 811, col. 2, wherein "Due to the controlled timing environment, a simple clocked design can be implemented without address-transition sensing, resulting in low overhead area."; also see Fig. 4 on page 812, which shows a CLK signal].

However, the LISP reference does not expressly disclose if the "clock", is a ring oscillator, so that the system provides a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said integrated circuit substrate.

The reference of Uhlenhoff teaches of a microprocessor integrated circuit that comprises a processing unit disposed upon an integrated circuit substrate [serial data processing circuit 120, seen in col. 2, lines 24-68]; and a ring oscillator having a variable output frequency [see col. 1, line 40-col. 2, line 14], wherein the ring oscillator [clock oscillator 101] provides a system clock to the processing unit [see col. 1, lines 50-61, wherein "the actual clock signal produced internally by a clock oscillator consisting of an odd number of ring-connected inverting stages. In other words, a ring oscillator is used whose frequency depends on the selected integration technique, but makes use of the delaying properties on inverting stages, which are inherent to

each of the specific integration techniques."], the ring oscillator disposed on said integrated circuit substrate [see col. 1, line 50-col. 2, line 14].

The LISP reference & Uhlenhoff are combinable because they are from the same field of endeavor, being CMOS integrated digital circuits. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the internal ring oscillator, as disclosed by Uhlenhoff, within the system described in the LISP reference. The suggestion/motivation for doing so would have been that the integrated circuit in the LISP reference would reduce radio interference, as recognized by Uhlenhoff on col. 3, lines 18-24, and also that the integrated circuit in the LISP reference would additionally benefit from the capability of having increased speed, as recognized by Uhlenhoff on col. 1, lines 62-66. Therefore, it would have been obvious to combine the ring oscillator teachings of Uhlenhoff with the system of the LISP reference to obtain the invention as specified in claim 4.

Regarding ***claim 7***, the LISP reference and Uhlenhoff disclose the microprocessor integrated circuit discussed above in claim 4, and the LISP reference further teaches that said memory is capable of supporting read and write operations [see page 810, col. 2, wherein "From the pipeline diagram of Fig. 3 it can be seen that any memory may be required for a READ and a WRITE operation every cycle, nominally requiring the use of two-port memories."; also see Fig. 3 on page 810].

Regarding ***claim 11***, the Transputer Manual discloses a microprocessor computational system comprising:

a first processing unit upon a first substrate [being the "execution unit", see page 809, cols. 1 and 2, wherein "The execution unit consists primarily of the ALU and rotator/masker..."];

a first memory disposed upon said first substrate and coupled to said first processing unit [on-chip RAM memory, see page 808; also see Fig. 2 on page 809],

said first memory occupying a greater area of said first substrate than said first processing unit, said memory further occupying a majority of a total area of said substrate [see page 808, col. 2, wherein "The on-chip RAM's, which dominate chip area and transistor count, are described in Section VI..."; also see page 814, col. 2, wherein "...the large fraction of chip area consumed by memory..."; also see page 816, col. 2, wherein "Since the memories occupy a large fraction of the chip area..."; also see the additional LISP Conference reference on page 402, which shows the identical photomicrograph of the LISP chip seen in Fig. 1 on page 808 of the LISP reference, but labeled to show that the on-chip memory occupies a greater area than the "execution unit", and also occupies a majority of the total area of the substrate.];

a "clock" that provides a system clock to the processing unit, and disposed on said first substrate [see page 811, col. 2, wherein "Due to the controlled timing environment, a simple clocked design can be implemented without address-transition sensing, resulting in low overhead area."; also see Fig. 4 on page 812, which shows a CLK signal]; and

a second processing unit coupled to said first processing unit and configured for interprocessor communication with said first processing unit [see page 812, col. 1, wherein "the control section" includes "logic"; also see Fig. 4 on page 812, whereby the "control section" is

coupled to the "execution unit", as seen in the LISP Conference reference on page 402; with this, the control section and the execution unit are coupled together, and the control section would inherently be configured for interprocessor communication with the execution unit. Additionally, and alternatively, see page 809, col. 1, wherein "The microcode is contained off-chip in up to 32K words of 64-bit –wide writable control store."; also see page 816, cols. 1 and 2, wherein "Prior to initializing off-chip microinstruction memory and starting execution there, the chip executes a...test of all the on-chip RAM's."; thus, in an alternate interpretation, the off-chip processing can be considered as a "second processing unit"].

However, the LISP reference does not expressly disclose if the "clock", is a ring oscillator, so that the system provides a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said integrated circuit substrate.

The reference of Uhlenhoff teaches of a microprocessor system that comprises a processing unit disposed upon an integrated circuit substrate [serial data processing circuit 120, seen in col. 2, lines 24-68]; and a ring oscillator having a variable output frequency [see col. 1, line 40-col. 2, line 14], wherein the ring oscillator [clock oscillator 101] provides a system clock to the processing unit [see col. 1, lines 50-61, wherein "the actual clock signal produced internally by a clock oscillator consisting of an odd number of ring-connected inverting stages. In other words, a ring oscillator is used whose frequency depends on the selected integration technique, but makes use of the delaying properties on inverting stages, which are inherent to

each of the specific integration techniques."], the ring oscillator disposed on said integrated circuit substrate [see col. 1, line 50-col. 2, line 14].

The LISP reference & Uhlenhoff are combinable because they are from the same field of endeavor, being CMOS integrated digital circuits. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the internal ring oscillator, as disclosed by Uhlenhoff, within the system described in the LISP reference. The suggestion/motivation for doing so would have been that the integrated circuit in the LISP reference would reduce radio interference, as recognized by Uhlenhoff on col. 3, lines 18-24, and also that the integrated circuit in the LISP reference would additionally benefit from the capability of having increased speed, as recognized by Uhlenhoff on col. 1, lines 62-66. Therefore, it would have been obvious to combine the ring oscillator teachings of Uhlenhoff with the system of the LISP reference to obtain the invention as specified in claim 11.

Regarding ***claim 13***, the LISP reference and Ulenhoff discloses the microprocessor computational system discussed above in claim 11, and the LISP reference further teaches that said first processing unit includes an interface port for establishing said interprocessor communication between an internal register of said first processing unit and second processing unit [see the block diagram in Fig. 2 on page 809; also see Fig. 7 on page 815].

Regarding ***claim 14***, the LISP reference and Uhlenhoff disclose the microprocessor integrated circuit discussed above in claim 4, and the LISP reference further teaches that said memory comprises a plurality of physically separate memory portions [see Fig. 1 on page 808; also see Fig. 2 on page 809, having an A-memory, an M-memory, a PDL stack memory, and a dispatch memory; also see the LISP Conference reference on page 402, which show these separately labeled memory portions].

Regarding ***claim 15***, the LISP reference and Uhlenhoff disclose the microprocessor integrated circuit discussed above in claim 4, and the LISP reference further teaches that the total area is an area provided by ab entire top surface if the single substrate [see Fig. 1 on page 808].

Discussion of the Additional Proposed Combinations

13. The Third Party Requester in the '10562 proceeding additionally cited the reference of the "Transputer Reference Manual", published by Prentice Hall, having a copyright date of 1988 (noted as "Transputer"). The Transputer reference does not teach the limitation of "a memory occupying a larger area of said integrated circuit substrate than said processing unit said memory further occupying a majority of a total area of said single substrate." For this feature, the Third Party Requester cited that it would have been obvious to one of ordinary skill in the art to modify the Transputer chip with the teachings of LISP, which is seen as teaching of memory that occupies a larger area of the substrate than a processing unit, and also the memory occupies a majority of a total area of the substrate.

14. With this, the examiner notes that it is unclear what motivation one would have to redesign the Transputer chips to utilize the on-chip RAM disclosed in the LISP reference. The Transputer chip appears to utilize the in-chip memory for storing a small amount of programs and data. But a key feature of the Transputer device appears to be the External Memory Interface, whereby the Transputer reference even states on page 49 that "Where larger amounts of memory or programs in ROM are required, the processor has access to 4 Gbytes of memory via the External Memory Interface (EMI)." Thus, it is unclear how or why one of ordinary skill in the art would want to eliminate the external memory interface and instead provide a majority of the chip to be additional memory within the integrated circuit.

15. Further, the Third Party Requester cites page 124 of the Transputer reference as teaching of a ring oscillator, whereby the Transputer reference illustrates a phase-locked loop, and states "The internally derived power supply for internal clocks requires an external low leakage, low inductance 1uF capacitor to be connected between CapPlus and CapMinus." But with this teaching, even if a phase-locked loop indicates the presence of a ring oscillator, there is no clear teaching that the phase-locked loop disclosed in the Transputer reference provides a system clock to the processing unit. Further, as seen in Figure 3.1 on page 219 of the Transputer reference, an Xtal oscillator is shown, being external to the M212 Transputer chip. This oscillator may provide a system clock to the processor.

16. Thus, because of these reasons, the Transputer reference in view of the LISP reference, as proposed by the Third Party Requester in the '10562 proceeding, is not seen to teach each of the limitations of independent claims 4 and 11.

Conclusion

17. Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that *ex parte* reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extensions of time in *ex parte* reexamination proceedings are provided for in 37 CFR 1.550(c).

18. In order to ensure full consideration of any amendments, affidavits or declarations, or other documents as evidence of patentability, such documents must be submitted in response to this Office action. Submissions after the next Office action, which is intended to be a final action, will be governed by the requirements of 37 CFR 1.116, after final rejection and 37 CFR 41.33 after appeal, which will be strictly enforced.

19. The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent No. 6,598,148 throughout the course of this reexamination proceeding.

20. ALL correspondence relating to this ex parte reexamination proceeding should be directed as follows:

Please mail any communications to:

Attn: Mail Stop "Ex Parte Reexam"
Central Reexamination Unit
Commissioner for Patents
P. O. Box 1450
Alexandria VA 22313-1450

Please FAX any communications to:

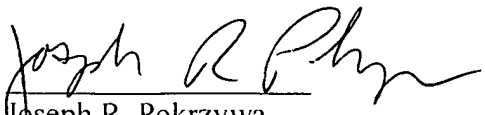
(571) 273-9900
Central Reexamination Unit

Please hand-deliver any communications to:

Customer Service Window
Attn: Central Reexamination Unit
Randolph Building, Lobby Level
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

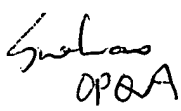
Signed:



Joseph R. Pokrzywa
Primary Examiner
Central Reexamination Unit 3992
(571) 272-7410

Conferees :

/r.g.f./



Notice of References Cited	Application/Control No. 90/008,227	Applicant(s)/Patent Under Reexamination 6598148	
	Examiner JOSEPH R. POKRZYWA	Art Unit 3992	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"A 553K-Transistor LISP Processor Chip", Bosshart et al., IEEE International Solid-State Circuits Conference, February 26, 1987, pages 202, 203, and 402
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Receipt date: 07/02/2009

PTO/SB/08a (02-09)

Substitute for form 1449/PTO				Complete if Known	
				Application Number	90/008,227
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	September 21, 2006
				First Named Inventor	----
				Art Unit	3992
(Use as many sheets as necessary)				Examiner Name	Joseph R. Pokrzywa
Sheet	1	of	30	Attorney Docket Number	0081-011D3C1X1

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/J.P./	AA	3,696,414	10-03-1972	Allen et al.	
/J.P./	AB	3,967,104	06-29-1976	Brantingham et al.	
/J.P./	AC	3,980,993	09-14-1976	Bredart et al.	
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/J.P./	BI	4,660,155	04-21-1987	Thaden et al.	

Examiner Signature	/Joseph Pokrzywa/	Date Considered	11/03/2009

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kind Codes of U.S. Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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PTO/SB/08a (02-09)

Substitute for form 1449/PTO				Complete if Known	
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				Art Unit	3992
(Use as many sheets as necessary)				Examiner Name	Joseph R. Pokrzywa
Sheet	2	of	30	Attorney Docket Number	0081-011D3C1X1

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/J.P./	BJ	4,665,495	05-12-1987	Thaden	
/J.P./	BK	4,670,837	06-02-1987	Sheets	
/J.P./	BL	4,698,750	10-06-1987	Wilkie et al.	
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Examiner Signature	/Joseph Pokrzywa/	Date Considered	11/03/2009

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/J.P./	DI	EP	0 208 287			NEC Corporation		☐

Examiner Signature	/Joseph Pokrzywa/	Date Considered	11/03/2009

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				Art Unit	3992
(Use as many sheets as necessary)				Examiner Name	Joseph R. Pokrzywa
Sheet	4	of	30	Attorney Docket Number	0081-011D3C1X1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	~~DJ~~	~~90/090,034 Non-Final Office Action dated 03-04-2008~~	
	~~DK~~	~~90/008,380 Reexam Ordered 04-08-2008~~	
	~~DL~~	~~90/008,380 Request for Reexamination dated 04-16-2008~~	
	~~DM~~	~~90 008,225 and 90 008,299 Final Office Action dated 12-05-08~~	
	DN	~~90,008,225 and 90,008,299 Notice of Intent to Issue a Reexam Certificate dated 04-21-09~~	
	DO	~~90 008,225 Notice of Failure to Comply with Ex Parte Reexamination Request Filing Requirements~~ dated 10-16-2006	
	DP	~~90 008,225 Response to Notice of Failure to Comply with Ex Parte Reexamination Request Filing~~ Requirements: Letter Accompany Replacement PTO Form, SB/42, dated 11-15-06	
	~~DQ~~	~~90 008,237 Examiner Interview Summary Record dated 08-13-08~~	
	~~DR~~	~~90 008,237 Non-Final Office Action dated 07-02-08~~	
	DS	~~90 008,237 Notice of Failure to Comply with Ex Parte Reexamination Request Filing Requirements~~ dated 10-19-2006	

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	DT	~~90/008,227 Response to Notice of Failure to Comply with Ex Parte Reexamination Request Filing~~ Requirements: Letter Accompanying Replacement PTO Form SB/42 dated 11-17-2006	
	DU	~~90/008,227 Response to Notice of Failure to Comply with Ex Parte Reexamination Request Filing~~ Requirements dated 10-19-2006	
	DV	~~90/008,227 Response to Non-Final Office Action dated 09-02-09~~	
	DW	~~90/008,227, 90/008,306, 90/008,474 Examiner Interview Summary Record dated 04-23-09~~	
	DX	~~90/008,227, 90/008,306, 90/008,474 Final Office Action dated 03-17-09~~	
	DY	~~90/008,306 Non-Final Office Action dated 07-02-08~~	
	DZ	~~90/008,306 Applicant Summary Interview with Examiner dated 08-08-08~~	
	EA	~~90/008,306 Reexam Ordered 04-06-09~~	
	EB	~~90/008,306 Request for Reexam dated 01-16-09~~	
	EC	~~90/008,457 Request for Reexamination dated 04-24-2009~~	

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/J.P./	EJ	Alliacense Product Report - Preliminary Review, USP 5,440,749; GPS Navigation System Main Microprocessor	
/J.P./	EK	Alliacense Product Report - Preliminary Review, USP 5,440,749; Kyocera Digital Camera Finecam S3R Image Processor	
/J.P./	EL	Alliacense Product Report - Preliminary Review, USP 5,440,749; PDA/Mobile Navigation, GPS Processor	
/J.P./	EM	ARM Datasheet, Part No. 1 85250 0360 0, Issue No. 1 (March 17, 1987)	

Examiner Signature	/Joseph Pokrzywa/	Date Considered	11/03/2009

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/J.P./	EO	BARRON et al., "The Transputer," Electronics, pages 109-115 (1983)	
/J.P./	EP	BAYKO, "Great Microprocessors of the Past and Present (V 11.7.0), downloaded from: <<http://web.archive.org/web/20010107210400/http://bwrc.eecs.berkeley.edu/CIC/Archive/cup_history.html>>, Feb 2007, 60 pages total.	
/J.P./	EQ	Books Review: Operating Systems A Systematic View, William S.Davis, Addison-Wesley Publishing Company, Inc., 1987; 26(4):453-454.	
/J.P./	ER	BOURKE, "Character Synchronization During Overrun Conditions," Delphion, IBM Technical Disclosure Bulletin, Dec 1977	
/J.P./	ES	Burroughs Corporation, "Burroughs B5500 Information Processing System Reference Manual," 1973.	
/J.P./	ET	Burroughs Corporation, "Burroughs B7700 Systems Reference Manual," 1973.	
/J.P./	EU	CAL RUN FORTRAN Guide, University of California, Computer Center, Berkeley, 292 pages total. (Sep 1974)	
	EV	~~Case no. 09-cv-4083, Sirius XM Radio Inc. vs. Technology Properties, Patriot, and Alliacense Ltd.,~~ Declaratory Judgment filed 04-24-09	
	EW	~~Case no. 2:05-cv-00404 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-8 Acorn~~ Processor Invalidity Chart	

Examiner Signature	/Joseph Pokrzywa/	Date Considered	11/03/2009

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				Filing Date	September 21, 2006
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				Art Unit	3992
(Use as many sheets as necessary)				Examiner Name	Joseph R. Pokrzywa
Sheet	8	of	30	Attorney Docket Number	0081-011D3C1X1

NON PATENT LITERATURE DOCUMENTS			
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	EX	~~Case No. 2:05-cv-00494 Federal Circuit Court Decision on TPL Appeal of Decision dated 5/9/08~~	
	EY	~~Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-1 CDC 6600~~ Invalidity Chart	
	EZ	~~Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-2 MIPS~~ Invalidity Chart	
	FA	~~Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-3 SPARC~~ Invalidity Chart	
	FB	~~Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-4 IBM RT PC~~ ROMP Invalidity Chart	
	FC	~~Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-5 Berkeley~~ RISC I and RISC II Invalidity Chart	
	FD	~~Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-6 Porter~~ Invalidity Chart - USP 3,976,977	
	FE	~~Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-7 CRAY-1~~ Invalidity Chart	
	FF	~~Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit B. RISC~~ References	
	FG	~~Case no. 2:05-cv-494 (TJW) Defendants MEI, PNA, and IVC Preliminary Invalidity Contentions filed~~ 9/18/06 EXHIBIT A - Claim Chart for '148 Patent	

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	FH	~~Case no. 2:05-cv-494 (TJW) Defendants MEI, PNA, and JVC Preliminary Invalidity Contentions filed~~ 9/18/06 EXHIBIT B - Claim Chart for '336 Patent	
	FI	~~Case no. 2:05-cv-494 (TJW) Defendants MEI, PNA, and JVC Preliminary Invalidity Contentions filed~~ 9/18/06 EXHIBIT C - Claim Chart for '336 Patent	
	FJ	~~Case no. 5:08-cv-00877 JF Acer and Gateway vs. TPL, Patriot, and Alliasonce, Preliminary Invalidity~~ Contentions (Patent L.R. 3-3)	
	FK	~~Case No. 5:08-cv-00877 JF Acer Declaration of Harold H. Davis in Support of Plaintiff's Motion to Stay~~ All Proceedings Pending Reexamination of the Patents-in-Suit, dated 05-01-09	
	FL	~~Case No. 5:08-cv-00877 JF Acer Inc. and Acer America Corporation Plaintiff's Motion and Motion to~~ Stay All Proceedings Pending Reexamination of the Patents-in-Suit, dated 05-01-09	
	FM	~~Case No. 5:08-cv-00877 JF Acer Inc. and Acer America Corporation's and Gateway First Amended~~ Complaint for Declaratory Judgment dated 02-09-09	
	FN	~~Case No. 5:08-cv-00877 JF Acer Inc. and Acer America Corporation's Responses to Defendant~~ Technology Properties Limited's First Set of Interrogatories, dated 04-03-09	
	FO	~~Case No. 5:08-cv-00877 JF Gateway, Inc.'s Responses to Defendants Technology Properties Limited's~~ First Set of Interrogatories dated 04-03-09	
	FP	~~Case no. 5:08-cv-00882 JF, HTC vs. TPL, Patriot, and Alliasonce, First Amended Complaint for~~ Declaratory Judgment filed 07-10-08	
	FQ	~~Case no. 5:08-cv-00884 JF Asustek and Asus vs. TPL, Patriot, MGM, and Alliasonce, Second Amended~~ Complaint filed 09-25-08	

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	FR	~~Case no. C0805308 JF, Barco's Patent Local Rule 3-3 Invalidity Contentions dated 04-06-2009~~	
	FS	~~Case no. C0805308, BARCO N.V. v. Technology Properties Ltd., Patriot Scientific Corp., and Alliacense~~ Ltd., Complaint for Declaratory Judgment, Demand for Jury Trial, dated 12-01-08	
/J.P./	FT	CDC 6000 Computer Systems - COBOL INSTANT 6000, Version 3; Control Data Publication No. 60327600A (Apr 1971)	
/J.P./	FU	CDC 6000 Computer Systems, 7600 Computer Systems: FORTRAN Extended Instant 6000 Version 3, 7600 Version 1; Control Publication No. 60305900A (May 1971)	
/J.P./	FV	CDC 6000 Computer Systems/ 7600 Computer Systems: FORTRAN Extended Reference Manual, 6000 Version 3, 7600 Version 1; Control Data Publication No. 60329100, Revision D (1972)	
/J.P./	FW	CDC 6000 Series Computer System, 6642 Distributive Data Path Operation and Programming Reference Manual; Control Data Publication No. 60376300C (Mar 1979)	
/J.P./	FX	CDC 6000 Series Computer Systems - Chippewa Operating System Documentation, Vol. I, Preliminary Edition (updated May 1966)	
/J.P./	FY	CDC 6000 Series Computer Systems - Chippewa Operating System Documentation, Vol. II, Preliminary Edition, Peripheral Packages and Overlays (Oct 1965)	
/J.P./	FZ	CDC 6000 Series Computer Systems - Chippewa Operating System Documentation, Vol. III, Preliminary Edition, DSD - The Systems Display, (Nov 1965)	
/J.P./	GA	CDC 6000 Series Computer Systems ASCENT General Information Manual; Control Data Publication No. 60135400 (Feb 66)	

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/J.P./	GB	CDC 6000 Series Computer Systems Chippewa Operating System Reference Manual; Control Data Publication No. 60134400 (Dec 1965)	
/J.P./	GC	CDC 6000 Series Computer Systems Hardware Reference Manual; Control Data Publication No. 60100000 (Aug 1978)	
/J.P./	GD	CDC 6000 Series Computer Systems/ 7600 Computer System: 6000 Compass Version 2, 7600 Versions 1 & 2 Reference Manual; Control Data Publication No. 60279900, Revision D, (1970, 1971, 1972)	
/J.P./	GE	CDC 6000 Series Computer Systems: Chippewa Operating System FORTRAN Reference Manual; Control Data Publication No. 60132700A (May 1966)	
/J.P./	GF	CDC 6000 Series Computer Systems: FORTRAN Extended General Information, Control Data Publication No. 60176400 (Oct 1966)	
/J.P./	GG	CDC 6000 Series Computer Systems: Peripheral Equipment Reference Manual; Control Data Publication No. 60156100, Revision J (Mar 1970)	
/J.P./	GH	CDC 6000 Series Computer Systems: Site Preparation and Installation Manual; Control Data Publication No. 60142400, Revision B (Sep 1965)	
/J.P./	GI	CDC 6000 Series FORTRAN Extended 4.0, Internal Maintenance Specifications, (1971)	
/J.P./	GJ	CDC 6000 Series Introduction and Peripheral Processors Training Manual, Second Edition; Control Data Publication No. 60250400 (Nov 1968)	
/J.P./	GK	CDC 6400 Central Processor; Control Data Publication No. 60257200 (Feb 1967)	

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/J.P./	GL	CDC 6400/6500/6600 ASCENT-TO-COMPASS TRANSLATOR; Control Data Publication No. 60191000 (Mar 1967)	
/J.P./	GM	CDC 6400/6500/6600 Computer System Input/Output Specification; Control Data Publication No. 60045100 (September 1967)	
/J.P./	GN	CDC 6400/6500/6600 Computer System Instant SMM; Control Data Publication No. 60299500 (Nov 1969)	
/J.P./	GO	CDC 6400/6500/6600 Computer Systems COMPASS Reference Manual; Data 60190900, Revision B (Mar 1969)	
/J.P./	GP	CDC 6400/6500/6600 Computer Systems Reference Manual; Control Data Publication No. 60100000, Revision K (Aug 1970)	
/J.P./	GQ	CDC 6400/6500/6600 Extended Core Storage Systems Reference Manual; Control Data Publication No. 60225100, (Feb 1968)	
/J.P./	GR	CDC 6400/6500/6600 Jovial General Information Manual; Control Data Publication No. 60252100A (Mar 1969)	
/J.P./	GS	CDC 6400/6600 Computer Systems: ASCENT/ASPER Reference Manual; Control Data Publication No. 60172700 (Jul 1966)	
/J.P./	GT	CDC 6400/6600 FORTAN Conversion Guide; Data Publication No. 60175500 (Aug 1966)	
/J.P./	GU	CDC 6400/6600 Systems Bulletin (10 Oct 1966), 84 pages	

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/J.P./	GV	CDC 6400/6600, Export/Import 8231 Reference Manual; Data Publication No. 60189100 (April 1967)	
/J.P./	GW	CDC 6600 Central Processor Vol. 1; Control & Memory; Data Control Publication No. 020167 (March 1967)	
/J.P./	GX	CDC 6600 Central Processor, Vol. 2, Functional Units; Control Data Publication No. 60239700 (Mar 1967)	
/J.P./	GY	CDC 6600 CHASSIS TABS; Control Data Publication No. 63016700A (Apr 1965)	
/J.P./	GZ	CDC 6600 CHASSIS TABS; Control Data Publication No. 63019800 (Mar 1965)	
/J.P./	HA	CDC 6600 Chippewa Operating System; Control Data Publication No. 60124500, Revision C (April 1965)	
/J.P./	HB	CDC 6600 Computer System 6601 A-J, 6613A/B/C, 6604A/B/C, 6614-A/B/C Central Processor (Including Functional Units) Vol. 1, Diagrams & Circuit Description; Control Data Publication No. 60119300BT(Jan 1968)	
/J.P./	HC	CDC 6600 Computer System 6601 A-J, 6613A/B/C, 6604A/B/C, 6614-A/B/C Peripheral and Control Processor/Central Memory/Clock/Extended Core Storage Coupler (Std Opt 10102 and/or Spec Opt 60080)/ Power Wiring, Vol. 2, Diagrams & Circuit Descriptions; Control Data Publication No. 60119300BT (Jan 1968)	
/J.P./	HD	CDC 6600 Computer System Operating System/Reference Manual, SIPROS66, 1st ed.; Control Data Publication No. 60101800A (1965)	
/J.P./	HE	CDC 6600 Computer System Programming System/Reference Manual, Vol. 1. ASCENT; Control Data Publication No. 60101600B (1965)	

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/J.P./	HF	CDC 6600 Computer System Programming System/Reference Manual, Vol. 2, ASPER; Control Data Publication No. 60101700B (1965)	
/J.P./	HG	CDC 6600 Computer System Programming Vol. 3, FORTRAN 66; Control Data Publication No. 60101500B (1965)	
/J.P./	HH	CDC 6600 Computer Training Manual Vol. 2, Preliminary Edition, Section 7.2 Shift Functional Units, 164 pages	
/J.P./	HI	CDC 6600 Data Channel Equipment 6602-B/6612-A, 6603-B, 6622-A, 6681-B, 6682-A/6683-A, S.O. 60022, 60028, 60029, Diagrams & Circuit Description' Control Data Publication No. 60125000, Revision G (June 1966)	
/J.P./	HJ	CDC 6600 Training Manual; Control Data Publication No. 60147400, Revision A (June 1965)	
/J.P./	HK	CDC 6603 - A/B/C Disk File Controller Reference Manual; Control Data Publication No. 60334000 (1970)	
/J.P./	HL	CDC 6638 Disk File Subsystem Training Supplement; Control Data Publication 602500800A (Oct 1968)	
/J.P./	HM	CDC 6638 Disk File System: Standard Option 10037-A, 6639-A/B File Controller -- Diagrams and Circuit Description/Maintenance/Maintenance Aids/Parts List/ Wire Lists/Chassis Tabs; Control Data No. 60227300, Revision H (Mar 1974)	
/J.P./	HN	CDC 6639 - A/B Disk File Controller Reference Manual; Control Data Publication No. 60334100E (Aug 1973)	
/J.P./	HO	CDC 6639 Disk Controller Training Manual Test Edition (Sep 1967), 28 pages.	

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/J.P./	HP	CDC APL Version 2 Reference Manual, CDC Operating Systems : NOS; Control Data Publication NO. 60454000F (Nov 1980)	
/J.P./	HQ	CDC Basic Version 3 Reference Manual: NOS 1 & NOS/BE 1; Control Data Publication No. 19983900G (Oct 1980)	
/J.P./	HR	CDC Chippewa Operating System, Document Class ERS, System No. E012, Version 1.1; External Reference Specifications - Chippewa Operating System, (Jun 1966)	
/J.P./	HS	CDC Chippewa Operating System, Document Class SIR, System No. E012, Version 1.0, (March 3, 1966)	
/J.P./	HT	CDC Chippewa Operating System, Document Class SIR, System No. E012, Version 1.1, (March 3, 1966)	
/J.P./	HU	CDC COBOL Version 4 Instant Manual, Cyber 170 Series, Cyber 70 Models 72, 73, 74, 6000 Series; Control Data Publication No. 60497000A (Feb 1976)	
/J.P./	HV	CDC COBOL Version 5 Instant Manual, Operating Systems: NOS 1/BE 1; Control Data Publication No. 60497300B (Feb 198)	
/J.P./	HW	CDC CODES/Control Data 6400/6500/6600 Computer Systems; Control Data Publication No. 60141900, Revision C (1966, 1967)	
/J.P./	HX	CDC CODES/Control Data 6400/6500/6600/6700 Computer Systems; Control Data Publication No. 60141900, Revision D (1966, 1967)	
/J.P./	HY	CDC CODES/Control Data 6600; Control Data Publication No. 60141900, Revision A (May 1965)	

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/J.P./	HZ	CDC COMPASS Version3 Instant, Operating Systems: NOS 1, NOS 2, NOS/ BE 1, SCOPE 2; Control Data Publication No. 60492800D (Jun 1982)	
/J.P./	IA	CDC Course No. FH4010-1C, NOS Analysis, Student Handout, Revision C (Apr 1980)	
/J.P./	IB	CDC Course No. FH4010-4C NOS Analysis, Study Dump (Apr 1980)	
/J.P./	IC	CDC Cyber 170 Models 720, 730, 740, 750 and 760 Model 176 (Level B/C) Computer Systems, Codes; Control Data Publication No. 60456920C, (Jun 1981)	
/J.P./	ID	CDC Cyber 70 Computer Systems Models 72, 73, 74, 6000 Computer Systems: FORTRAN Reference Manual Models 72, 73, 74 Version 2.3, 6000 Version 2.3; Control Data Publication No. 19980400, Revision F (July 1972)	
/J.P./	IE	CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems -- ALGOL Reference Manual, Cyber 70 Series Version 4, 6000 Series Version 4, 7600 Series Version 4; Control Data Publication No. 60384700A (Aug 1973)	
/J.P./	IF	CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems: COBOL INSTANT Models 72, 73, 74 Version 4, Model 76 Version 1, 6000 Version 4; Control Data Publication No. 60328400A (Dec 1971)	
/J.P./	IG	CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems: FORTRAN Extended Instant Models 72, 73, 74 Version 4, Model 76 Version 2, 7600 Version 2, 6000 Version 4; Control Data Publication No. 60357900A (Nov 1971)	
/J.P./	IH	CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems: FORTRAN Extended Reference Manual Models 72, 73, 74 Version 4, Model 76 Version 2, 6000 Version 4; Control Data Publication No. 60305600A (Oct 1971)	
/J.P./	II	CDC Cyber 70 Series 6000 Series Computer Systems: APL*Cyber Reference Manual; Control Data Publication No. 19980400B (July 1973)	

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/J.P./	IJ	CDC Cyber 70 Series Computer Systems 72, 73, 74, 6000 Series Computer Systems -- Kornos 2.1 Workshop Reference Manual; Control Data Publication No. 97404700D (1976)	
/J.P./	IK	CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, KRONO 2.1 Operator Guide; Control Data Guide; Control Data Publication 60407700A (Jun 1973)	
/J.P./	IL	CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, KRONOS 2.1 Installation Handbook; Control Data Publication no. 60407500A (Jun 1973)	
/J.P./	IM	CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, KRONOS 2.1 Installation Handbook; Control Data Publication no. 60407500A (Jun 1973)	
/J.P./	IN	CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, KRONOS 2.1 Time-Sharing User's Reference Manual; Control Data Publication No. 60407600B (May 1974)	
/J.P./	IO	CDC Cyber 70/ Model 76 Computer System, 7600 Computer System: FORTRAN Run, Version 2 Reference Manual; Control Data 60360700C (May 1974)	
/J.P./	IP	CDC Cyber Interactive Debug Version 1 Guide for Users of FORTRAN Extended Version 4, CDC Operating Systems: NOS 1, NOS/ BE 1, Control Data Publication No. 60482700A (Feb 1979)	
/J.P./	IQ	CDC Cyber Interactive Debug Version 1 Guide for Users of FORTRAN Version 5, Operating Systems: NOS 1, NOS/ BE 1; Control Data Publication No. 60484100C (Sep 1984)	
/J.P./	IR	CDC Cyber Interactive Debug Version 1 Reference Manual, NOS 1, NOS 2, NOS/ BE 1; Data Control Publication NO. 60481400D (Jun 1984)	
/J.P./	IS	CDC Cyber Loader Version 1 Instant, CDC Operating System NOS1, NOS/ BE 1; Control Data Publication No. 60449800C (Aug 1979)	

Examiner Signature	/Joseph Pokrzywa/	Date Considered	11/03/2009

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PTO/SB/08b (02-09)

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				Filing Date	September 21, 2006
				First Named Inventor	
				Art Unit	3992
(Use as many sheets as necessary)				Examiner Name	Joseph R. Pokrzywa
Sheet	18	of	30	Attorney Docket Number	0081-011D3C1X1

NON PATENT LITERATURE DOCUMENTS			
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/J.P./	IT	CDC Disk Storage Subsystem -- Operation and Programming Manual; Control Data Publication No. 60363900, Version T (1972 -1980)	
/J.P./	IU	CDC FORTRAN Extended 2.0, Document Class ERS, System No. C012, (Dec 1966)	
/J.P./	IV	CDC FORTRAN Extended 2.0, Document Class IMS, Internal Maintenance Specifications - 64/65//6600 V FORTRAN Extended Version 2 (Mar 1969)	
/J.P./	IW	CDC FORTRAN Extended Version 4 Instant Manual, Operating Systems: NOS 1, NOS/BE 1, SCOPE 2; Control Data Publication No. 60497900B (Jun 1981)	
/J.P./	IX	CDC FORTRAN Extended, Sales Technical Memorandum (May 1967)	
/J.P./	IY	CDC FORTRAN Version 5 Instant, CDC Operating Systems: NOS 1, NOS/ BE 1, SCOPE 2; Control Data Publication No. 60483900A (Jan 1981)	
/J.P./	IZ	CDC GED FORTRAN Extended 1.0, Product No. C012, Dept No. 254, Project No. 4P63FTN (Aug 1967)	
/J.P./	JA	CDC INSTANT 6400/3500/6500 SIMULA; Control Data Publication No. 60235100, Revision A (Feb 1969)	
/J.P./	JB	CDC INSTANT 6400/6500/6600 COMPASS; Control Data Publication No. 60191900, Revision A (1968)	
/J.P./	JC	CDC INSTANT FORTRAN 2.3 (6000 Series); Data Publication No. 60189500D (May 1969)	

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/J.P./	JD	CDC Internal Maintenance Specification: FORTRAN V5, ; Control Data Publication No. 77987506A	
/J.P./	JE	CDC Internal Maintenance Specification: FORTRAN V5, ; Control Data Publication No. 77987506A	
/J.P./	JF	CDC KRONOS 2.1 Reference Manual Volume 1 of 2; Control Data Cyber 70 Series Models 72/73/74, 6000 Serites Computer Systems; Control Data Publication No. 60407000D (Jun 1975)	
/J.P./	JG	CDC KRONOS 2.1 Time-Sharing User's Reference Manual, Cyber 70 Series Models 72, 73, 74, 6000 Series Computer Systems; Control Data Publication No. 60407600D (Jun 1975)	
/J.P./	JH	CDC Model dd 60A Computer Control Console/Customer Engineering Manual; Control Data Publication No. 82100010 (Mar 1965)	
/J.P./	JI	CDC Model dd60b Computer Control Console/Customer Engineering Manual; Control Data Publication No. 82103500 (Feb 1967)	
/J.P./	JJ	CDC Network Products: Network Access Method Version 1, Network Definition Language Reference Manual; Control Data Publication No. 60480000J (May 1981)	
/J.P./	JK	CDC Network Products: Network Terminal User's Instant -- Operating System NOS 1; Control Data Publication No. 60455270C, (Oct 1980)	
/J.P./	JL	CDC NOS 2 Operations Handbook; Control Data Publication No. 60459310, (Aug 1994)	
/J.P./	JM	CDC NOS Version 1 Applications Programmer's Instant, CDC Computer Systems: Cyber 170 Series, Cyber 70 Models 71, 72, 73 74, 6000 Series; Control Data Publication No. 60436000H (Jan 1980)	

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/J.P./	JN	CDC NOS Version 1 Internal Maintenance Specification Volume 1 of 3; Control Data Publication No. 60454300B (Aug 1979)	
/J.P./	JO	CDC NOS Version 1 Internal Maintenance Specification Volume 2 of 3; Control Data Publication No. 60454300B (Aug 1979)	
/J.P./	JP	CDC NOS Version 1 Internal Maintenance Specification Volume 3 of 3; Control Data Publication No. 60454300B (Aug 1979)	
/J.P./	JQ	CDC NOS Version 1 Operator's Guide, CDC Computer Systems: Cyber 170 Series, Cyber 70 Model 71, 72, 73 74, 6000 Series (Dec 1980)	
/J.P./	JR	CDC NOS Version 1 Reference Manual Volume 1 of 2, CDC Computer Systems: Cyber 170 Series, Cyber 70 Models 71, 72, 73, 74, 6000 Series; Control Data Publication No. 60435400J (1979)	
/J.P./	JS	CDC NOS Version 1 Reference Manual Volume 2 of 2, CDC Computer Systems: Cyber 170 Series, Cyber 70 Models 71, 72, 73, 74, 6000 Series; Control Data Publication No. 60445300E (1977)	
/J.P./	JT	CDC NOS Version 1 System Maintenance Reference Manual; Control Data Publication No. 60455380H (Apr 1981)	
/J.P./	JU	CDC NOS Version 2 Analysis Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60459300D (Oct 84)	
/J.P./	JV	CDC NOS Version 2 Analysis Handbook; Control Data Publication No. 60459300U (Jul 1994)	
/J.P./	JW	CDC NOS Version 2 Installation Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60459320E_ (Mar 1985)	

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/J.P./	JX	CDC NOS Version 2 Operation/Analysis Handbook, Cyber 170, Cyber 70 Models 71, 72, 73, 74 6000, Control Data Publication No. 60459310C (Oct 1983)	
/J.P./	JY	CDC NOS Version 2 System Maintenance Reference Manual, Cyber 170, Cyber 70 Models 71 , 72, 73 74, 6000; Control Data Publication No. 60459300C (Oct 1983)	
/J.P./	KA	CDC NOS/BE Version 1 Diagnostic Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60494400-V (1986)	
/J.P./	KB	CDC NOS/BE Version 1 Installation Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60494300AB (Dec 1986)	
/J.P./	KC	CDC NOS/BE Version 1 Reference Manual, Cyber 170 Series, Cyber 70 Models 71, 72, 73, 74, 6000 Series; Control Data Publication No. 60493800M 1981	
/J.P./	KD	CDC Outline of Reports on "Feasibility Study of 64/6600 FORTRAN Ver 3.0 and Conversational FORTRAN, FORTRAN Study Project, Product No. X010, Dept No. 254, Project No. 4P63, (Jun 1966)	
/J.P./	KE	CDC Pascal Version 1 Reference Manual, Operating Systems: NOS 2; Control Data Publication No. 60497700 (Sep 1983)	
/J.P./	KF	CDC Pascal Version 1 Reference Manual, Operating Systems: NOS 2; Control Data Publication No. 60497700A (Dec 1982)	
/J.P./	KG	CDC PL/1 Version 1 Instant, CDC Operating Systems: NOS 1, NOS/ BE 1; Control Data Publication No. 60483700A (Nov 1979)	
/J.P./	KH	CDC SIMSCRIPT 11.5 Instant; Control Data Publication No. 84000450B (Sep 1978)	

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/J.P./	KI	CDC Sort/Merge Version 4 and 1 Instant, Operating Systems: NOS 1, NOS/BE 1, SCOPE 2; Control Data Publication No. 60497600C (Jan 1981)	
/J.P./	KJ	CDC Sort/Merge Version 5 Reference Manual, Operating Systems: NOS 2, NOS/ BE 1; Control Data Publication No. 60484800C (Feb 1984)	
/J.P./	KK	CDC SYMPL Version 1 Instant, NOS 1, NOS/BE 1, SCOPE 2; Control Data Publication NO. 60482600A (May 1978)	
/J.P./	KL	CDC SYMPL Version 1 Users Guide, Operating Systems: NOS 1, NOS/BE 1, SCOPE 2; Control Data Publication No. 60499800B (Apr 1978)	
/J.P./	KM	CDC Update Instant, Cyber 170 Series, Cyber 70 Series, 6000 Series, 7600 Computer Systems; Control Data Publication No. 60450000A (Nov 75)	
/J.P./	KN	CDC Update Reference Manual Operating Systems: SCOPE 3.4, KRONOS 2.1; Control Data Publication No. 60342500, Revision H (1971 - 1978)	
/J.P./	KO	CDC XEDIT Version 3 Reference Manual, Operating System: NOS 1; Control Data Publication No. 60455730B (Aug 1979)	
/J.P./	KP	Chippewa Laboratories FORTRAN Compiler Run, Preliminary Edition, CDC 6000 Series Computer Systems, (Apr 1966)	
/J.P./	KQ	CHO et al., "The Memory Architecture and the Cache and Memory Management Unit for the Fairchild CLIPPER Processor," Report No. UCB/CSD 86/289, Computer Science Division (EECS), University of California (April 1986)	
/J.P./	KR	CHO et al., WAM 3.6: A 40K Cache Memory and Memory Management Unit," ISSCC '86, Feb 19, 1986.	

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/J.P./	KS	CORDELL, II et al., "Advanced Interactive Executive Program Development Environment," IBM Systems Journal, 1987; 26(4):361-382	
/J.P./	KT	CRAWFORD, "The i486 Executing Instructions in One Clock Cycle," IEEE Micro, pp. 28 - 36 (Feb 1990)	
/J.P./	KU	Disk Routines and Overlays, Chippewa Operating System, CDC Development Division - Applications, (Nov 1965)	
/J.P./	KV	DOWSING et al., "Computer Architecture: A First Course, Chapter 6: Architecture and the Designer," Van Nostrand Reinhold (UK) Co. Ltd., pp. 126-139.	
/J.P./	KW	EVANS et al., "An Experimental 512-bit Nonvolatile Memory with Ferroelectric Storage Cell," IEEE Journal of Solid-Sate Circuits, 23(5):1171-1175.	
/J.P./	KX	FIASCONARO, J., "Microarchitecture of the HP9000 Series 500 CPU," Microarchitecture of VLSI Computers, NATO ASI Series No. 96, Antognetti, eds., pages 55-81.	
/J.P./	KY	Field Maintenance Print Set, KA780-01-01 Rev. A,	
/J.P./	KZ	FISHER et al., "Very Long Instruction Word Architectures and the ELI-512," ACM pp. 140-150 (1983)	
/J.P./	LA	FURBER, VSLI RISC Architecture and Organization, Chapter 3: Commercial VLSI RISC, pp. 124 - 129, Marcel Dekker, Inc., 1989	
/J.P./	LB	GE 600 Series, publication	

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/J.P./	LC	GERSHON, Preface, IBM Systems Journal 26(4):324-325	
/J.P./	LD	GILL et al. Summary of MIPS Instruction. CSL Technical Note No. 237, Computer Systems Laboratory, Stanford University, November 1983. 50 pages total.	
/J.P./	LE	GREEN et al., "A Perspective on Advanced Peer-to-Peer Networking," IBM Systems Journal, 1987; 26(4):414-428.	
/J.P./	LF	GRIMES et al., "64 bit Processor, The Intel i860 64-Bit Processor: A General-Purpose CPU with 3D Graphics Capabilities", published by Intel, p. 85 (July 1989)	
/J.P./	LG	HANSEN, "A RISC Microprocessor with Integral MMU and Cache Interface," ICCD '86, pp. 145 - 148, 1986	
/J.P./	LH	HENNESSY et al., "Design of a High Performance VSL Processor, " Third Caltech Conference on Very Large Scale Integration," Bryant eds., California Institute of Technology, Computer Science Press, pp. 33-54. (1983)	
/J.P./	LI	HENNESSY et al., "Hardware/software Tradeoff for Increased Performance," Technical Report No. 228, Computer Systems Laboratory, Feb 1983, 24 pages	
/J.P./	LJ	HENNESSY et al., "The MIPS Machine", COMPCON, IEEE, Spring 1982, pp. 2-7.	
/J.P./	LK	HENNESSY, "Performance Issues in VLSI Processor Design," IEEE on VLSI in Computers, , pp. 153 - 156. (1983)	
/J.P./	LL	HINTON, "80960 -- Next Generation,"COMPCON Spring 89, IEEE, 13-16 (1989)	

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/J.P./	LM	HOLLINGSWORTH et al., "The Fairchild Clipper: Instruction Set Architecture and Processor Implementation," Report No. UCB/CSD 87/329, Computer Science Division (EECS), University of California Berkeley, California, (February 11, 1987)	
/J.P./	LN	HOROWITZ et al., "A 32b Microprocessor with On-Chip 2Kbyte Instruction Cache," IEEE International Solid State Circuits Conference, pp. 30, 31 and 328 (1987)	
/J.P./	LO	HP 9000 Instrument Controllers, Technical Specifications Guide, October, 1989.pdf	
/J.P./	LP	HP 9000 Series Computer Systems, HP-UX Reference 09000-090004, Preliminary November, 1982	
/J.P./	LQ	HUGHES, "Off-Chip Module Clock Controller," Delphion, IBM Technical Disclosure Bulletin, Sep 1989	
/J.P./	LR	HUNTER, "Introduction to the Clipper Architecture," IEEE Micro, pp. 6-26 (August 1987)	
/J.P./	LS	IBM RT PC, BYTE 1986 Extra Edition, Inside The IBM PCs, pp. 60-78	
/J.P./	LT	INMOS Limited, IMS T424 Transputer Reference Manual, 1984	
/J.P./	LU	Intel 386TM DX Microprocessor 32-Bit CHMOS Microprocessor With Integrated Memory Management (1995)	
/J.P./	LV	Intel 8080A/8080A-1/8080A-2, 8-Bit N-Channel Microprocessor, Order Number: 231453-001, Its Respective Manufacturer (Nov 1986)	

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/J.P./	LW	Intel 80960CA User's Manual published by Intel (1989)	
/J.P./	LX	Intel Architecture Optimization Manual, Order Number 242816-003, published by Intel (1997)	
/J.P./	LY	Intel Architecture Software Developer's Manual, Volume 1: Basic Architecture, published by Intel (1997)	
/J.P./	LZ	JOHNSON et al., "A Variable Delay Line PLL for CPU-Coprocessor Synchronization," IEEE Journal of Solid-State Circuits, 23(5): 1218-1223, October 1988	
/J.P./	MA	KATEVENIS et al., "Reduced Instruction Set Computer Architecture for VLSI," Doctoral Dissertation, Oct 1983	
/J.P./	MB	KATEVENIS et al., "The RISC II Micro-Architecture," Journal of VLSI and Computer Systems, 1(2):138-152 (1984)	
/J.P./	MC	KIPP, "Micron Technology Inc. Reports Financial Results," Business Wire, New York, Sep 26, 1988	
/J.P./	MD	KNAPP, "Frequency Stability Analysis of Transistorized Crystal Oscillator," IEEE Transactions on Instrumentation and Measurement, Vol. 12, No. 1, pp. 2-5. (June 1963)	
/J.P./	ME	KOHN et al., "Introducing INTEL i860 64-Bit Microprocessor," Intel Corporation, IEEE Micro (August 1989)	
/J.P./	MF	KOOPMAN, "RTX 4000," Proceedings of 1989 Rochester Forth Conference, pp. 84-86.	

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/J.P./	MG	KOOPMAN, "The WISC Concept: A proposal for a writable instruction set computer," BYTE, pp. 187-193. (April 1987)	
/J.P./	MH	KOOPMAN, Jr. et al. "MVP Microcoded CPU/16 Architecture," Proceedings of 1986 Rochester Forth Conference, pp. 277-280.	
/J.P./	MI	KOOPMAN, Jr. et al., "WISC Technologies, Inc., Writable Instruction Set, Stack Oriented Computers: The WISC Concept," 1987 Rochester Forth Conference, Journal of Forth Application and Research, 5(1):49-71.	
/J.P./	MJ	KOOPMAN, Jr., Stack Computers: the new wave, 1989	
/J.P./	MK	LOUCKS et al., "Advanced Interactive Executive (AIX) Operating System Overview," IBM Systems Journal, 1987; 26(4):326-345	
/J.P./	ML	MACGREGOR et al., "The Motorola MC68020," IEEE Micro, 4(4):103-118 (1984).	
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Examiner Signature	/Joseph Pokrzywa/	Date Considered	11/03/2009

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[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

Receipt date: 07/02/2009

PTO/SB/08b (02-09)

Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				**Application Number**	90/008,227
				Filing Date	September 21, 2006
				First Named Inventor	
				Art Unit	3992
(Use as many sheets as necessary)				Examiner Name	Joseph R. Pokrzywa
Sheet	28	of	30	Attorney Docket Number	0081-011D3C1X1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/J.P./	MQ	Motorola MC68020 32-bit Microprocessor User's Manual, 1985	
/J.P./	MR	Motorola MC68020 32-bit Microprocessor User's Manual, Prentice-Hall, 1984	
/J.P./	MS	MOUSSOURIS et al., "A CMOS RISC Processor Integrated System Functions," Proceedings of 31st IEEE Computer Society International Conference, Cathedral Hill Hotel, San Francisco, CA March 3-6, 1986, pp. 126 - 131, 1986.	
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/J.P./	NA	PROEBSTING et al., "A TTL Compatible 4096-Bit N-Channel RAM," IEEE International Solid State Circuits Conference, Volume: XVI, pp. 28-29 (February 1973)	
/J.P./	NB	PRZYBYISKI et al., "Organization and VLSI Implementation of MIPS," Technical Report: CSL-TR-84-259, Apr 1984	
/J.P./	NC	PRZYBYISKI, "The Design Verification and Testing of MIPS", 1984 Conference on Advanced Research in VLSI, pp. 100 - 109.	
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/J.P./	NF	RUBINFELD et al., "The CVAX CPU, A CMOS VAX Microprocessor Chip", International Conference on Computer Design, October, 1987.	
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/J.P./	NH	SCHOEFFLER, "Microprocessor Architecture," IEEE Transactions on Industrial Electronics and Control Instrumentation, Volume IECI-22, Issue 3, pp. 256-272. (August 1975)	
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/J.P./	NK	THORNTON, J. E., "Considerations in Computer Design Leading Up To the Control Data 6600," Control Data Chippewa Laboratory (1970).	
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/J.P./	NP	WALLS et al., "A Frequency-Lock System for Improved Quartz Crystal Oscillator Performance," IEEE Transactions on Instrumentation and Measurement, Vol. IM-27, No. 3, pp. 249-252 (September 1978)	
/J.P./	NQ	WATERS et al., "AIX Usability Enhancements and Human Factors," IBM Systems Journal, 1987; 26(4):383-394.	
/J.P./	NR	WILLIAMS, "Chip Set Tackles Laptop Design Issues, Offers Flat-Panel VGA Control," Computer Design, October 15, 1988; 27(19):21-22	

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Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination
90/008,227 & 90/010,562	6598148
Examiner	**Art Unit**
JOSEPH R. POKRZYWA	3992

SEARCHED			
Class	Subclass	Date	Examiner

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
reviewed prosecution history	11/2/2009	J.P.