I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent and Trademark Office on November 23, 2009.

/Larry E. Henneman, Jr./
By: Larry E. Henneman, Jr., Reg. No. 41,063

PATENT
Attorney Docket No.: 0081-011D3C1X1
Merged with: 0081-011D3C1X2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Ex Parte Reexamination:

Control No.: 90/008,227
Filed: September 21, 2006

merged with

Control No.: 90/010,562
Filed: May 29, 2009

For: HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

U.S. Patent No. 6,598,148

Examiner: Pokrzywa, Joseph R.

Technology Center/Art Unit: 3992

TRANSMITTAL FOR:

SUPPLEMENTAL AMENDMENT IN MERGED EX PARTE REEXAMINATION PROCEEDINGS

Mail Stop ***Ex Parte Reexamination***
Central Reexamination Unit
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith for filing in the above-referenced merged reexamination proceedings are the following documents:

1. Supplemental Amendment In Merged Ex Parte Reexamination Proceedings (5 pages); and
2. Certification of Service (2 pages).

November 23, 2009

Respectfully submitted,

/Larry E. Henneman, Jr./

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Sir:

Please enter the following amendments and remarks:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 5 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Original) A microprocessor integrated circuit comprising:

a program-controlled processing unit operative in accordance with a sequence of program instructions;

a memory coupled to said processing unit and capable of storing information provided by said processing unit;

a plurality of column latches coupled to the processing unit and the memory, wherein, during a read operation, a row of bits are read from the memory and stored in the column latch; and

a variable speed system clock having an output coupled to said processing unit;

said processing unit, said variable speed system clock, said plurality of column latches, and said memory fabricated on a single substrate, said memory using a greater area of said single substrate than said processing unit, said memory further using a majority of a total area of said single substrate.

2. (Original) The microprocessor integrated circuit of claim 1 wherein said memory is dynamic random-access memory.

3. (Original) The microprocessor integrated circuit of claim 1 wherein said memory is static random-access memory.

4. (Original) A microprocessor integrated circuit comprising:

a processing unit disposed upon an integrated circuit substrate, said processing unit operating in accordance with a predefined sequence of program instructions;

a memory coupled to said processing unit and capable of storing information provided by said processing unit, said memory occupying a larger area of said integrated circuit substrate than said processing unit said memory further occupying a majority of a total area of said single substrate; and

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said integrated circuit substrate.

5. (Original) The microprocessor integrated circuit of claim 4 wherein said memory is dynamic random-access memory.

6. (Original) The microprocessor integrated circuit of claim 4 wherein said memory is static random-access memory.

7. (Original) The microprocessor integrated circuit of claim 4 wherein said memory is capable of supporting read and write operations.

8. (Cancelled).

9. (Original) The microprocessor integrated circuit of claim 8 wherein a first of said interface ports includes a column latch, said column latch facilitating serial communication through said first of said interface ports.

10. (Cancelled).

11. (Original) A microprocessor computational system comprising:

a first processing unit disposed upon a first substrate;

a first memory disposed upon said first substrate and coupled to said first processing unit, said first memory occupying a greater area of said first substrate than said first processing unit, said memory further occupying a majority of a total area of said substrate;

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said first substrate; and

a second processing unit coupled to said first processing unit and configured for interprocessor communication with said first processing unit.

12. (Original) The microprocessor computational system of claim 11 wherein said second processing unit and a second memory are disposed upon a second substrate, said second memory occupying a greater area of said second substrate than said second processing unit said second memory further occupying a majority of a total area of said substrate.

13. (Original) The multiprocessor computational system of claim 11 wherein said first processing unit includes an interface port for establishing said interprocessor communication between an internal register of said first processing unit and second processing unit.

14. (Previously Presented) The microprocessor integrated circuit of claim 4 wherein the memory comprises a plurality of physically separate memory portions.

15. (Previously Presented) The microprocessor integrated circuit of claim 4 wherein the total area is an area provided by an entire top surface of the single substrate.

REMARKS

This supplemental amendment is filed to withdraw the prior amendment of Claim 9 and leave Claim 9 as originally issued.

Claims 8 and 10 were previously cancelled. Claims 1-7, 9, and 11-13 remain as originally issued. Claims 14 and 15 were previously added and remain as previously presented.

CONCLUSION

If the Examiner has any questions regarding this amendment, he is invited to telephone the undersigned at 269-279-8820.

Respectfully submitted,

November 23, 2009

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