UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/009,457	08/24/2009	5809336	0081-011D3X4	6398

40972 7590 07/19/2010

HENNEMAN & ASSOCIATES, PLC
70 N. MAIN ST.
THREE RIVERS, MI 49093

EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 07/19/2010

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

DO NOT USE IN PALM PRINTER

(THIRD PARTY REQUESTER'S CORRESPONDENCE ADDRESS)

FISH & RICHARDSON P.C.

PO BOX 1022

MINNEAPOLIS, MN 55440-1022

MAILED

JUL 19 2010

CENTRAL REEXAMINATION UNIT

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/009,457*.

PATENT NO. *5809336*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Notice of Intent to Issue Ex Parte Reexamination Certificate	Control No.	Patent Under Reexamination	
	90/009,457	5809336	
	Examiner	Art Unit	
	B. James Peikari	3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ Prosecution on the merits is (or remains) closed in this *ex parte* reexamination proceeding. This proceeding is subject to reopening at the initiative of the Office or upon petition. *Cf.* 37 CFR 1.313(a). A Certificate will be issued in view of
   - (a) ☐ Patent owner's communication(s) filed: _____.
   - (b) ☐ Patent owner's late response filed: _____.
   - (c) ☐ Patent owner's failure to file an appropriate response to the Office action mailed: _____.
   - (d) ☐ Patent owner's failure to timely file an Appeal Brief (37 CFR 41.31).
   - (e) ☒ Other: *Patent owner's consent to an examiner's amendment on July 14, 2010*.

   Status of *Ex Parte* Reexamination:
   - (f) Change in the Specification: ☒ Yes ☐ No
   - (g) Change in the Drawing(s): ☐ Yes ☒ No
   - (h) Status of the Claim(s):
     - (1) Patent claim(s) confirmed: *1,2,6,7 and 9-16*.
     - (2) Patent claim(s) amended (including dependent on amended claim(s)): _____
     - (3) Patent claim(s) cancelled: _____.
     - (4) Newly presented claim(s) patentable: _____.
     - (5) Newly presented cancelled claims: _____.

2. ☒ Note the attached statement of reasons for patentability and/or confirmation. Any comments considered necessary by patent owner regarding reasons for patentability and/or confirmation must be submitted promptly to avoid processing delays. Such submission(s) should be labeled: "Comments On Statement of Reasons for Patentability and/or Confirmation."

3. ☐ Note attached NOTICE OF REFERENCES CITED (PTO-892).

4. ☒ Note attached LIST OF REFERENCES CITED (PTO/SB/08).

5. ☐ The drawing correction request filed on _____ is: ☐ approved ☐ disapproved.

6. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
   a)☐ All b)☐ Some* c)☐ None of the certified copies have
   - ☐ been received.
   - ☐ not been received.
   - ☐ been filed in Application No. _____.
   - ☐ been filed in reexamination Control No. _____.
   - ☐ been received by the International Bureau in PCT Application No. _____.

   * Certified copies not received: _____.

7. ☒ Note attached Examiner's Amendment.

8. ☐ Note attached Interview Summary (PTO-474).

9. ☐ Other: _____.

cc: Requester (if third party requester)

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below.

All changes made by this examiner's amendment reflect the changes made in U.S. Patent No. 5,809,336 by the reexamination certificate issued on December 15, 2009.

Authorization for this examiner's amendment was given in a telephone interview with Larry E. Henneman, Jr. (Reg. No. 41,063) on July 14, 2010.

The amendments are as follows:

In the specification:

At col. 17, line 16, change "a synchronously" to "asynchronously".

In the claims:

Claim 1: A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly

constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.

Claims 3-5: Claims 3-5 are cancelled.

Claim 6: A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said

clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data With said central processing unit; and

an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.

Claim 8: Claim 8 is cancelled.

Claim 10: In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency

and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock and wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock.

Claim 11: A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a

second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein said central processing unit operates asynchronously to said input/output interface.

Claim 12: The microprocessor system of claim 11, in which said second clock is a fixed frequency clock.

Claim 13: A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;

an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency

independent of a clock frequency of said oscillator and further wherein said central processing unit operates asynchronously to said input/output interface.

Claim 14: The microprocessor system of claim 13 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

Claim 15: The microprocessor system of claim 13 wherein said oscillator comprises a ring oscillator.

Claim 16: In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central. processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency

and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock, wherein said central processing unit operates asynchronously to said input/output interface.

STATEMENT OF REASONS FOR PATENTABILITY AND/OR CONFIRMATION

The following is an examiner's statement of reasons for patentability and/or confirmation of the claims found patentable in this reexamination proceeding:

Timeline

To understand the prosecution history of this reexamination proceeding, the following abbreviated timeline may prove useful:

(1) On April 11, 2008, three copending reexamination proceedings, 90/008,306, 90/008,237 and 90/008,474, each of which was related to U.S. Patent No. 5,809,336, were merged.

(2) On September 8, 2008, an amendment adding new claims 11-20 was filed in the merged reexamination proceeding.

(3) On May 12, 2009, an amendment to modify original claims 1, 6, and 10, to cancel original claims 3-5 and 8, to modify new claims 11, 16 and 20, and to cancel new claims 13-15 and 18 was filed in the merged reexamination proceeding.

(3) On May 26, 2009, a request for reexamination was filed in a fourth copending reexamination proceeding, 90/010,551, also related to U.S. Patent No. 5,809,336.

(4) On July 31, 2009, the request for reexamination in 90/010,551 was denied.

(5) On August 24, 2009, a request for a fifth reexamination proceeding related to U.S. Patent No. 5,809,336, was filed. This fifth proceeding is the present proceeding, 90/009,457.

The arguments presented in the request were based on claims 1-10 as originally filed. Claims 11-20, as first proposed in the September 8, 2008 amendment to the copending merged reexamination proceeding, were also discussed.

(6) On September 11, 2009, a Notice of Intent to Issue a Reexamination Certificate (NIRC) was mailed in the merged reexamination proceeding. This Office action specified that the May 12, 2009 amendment should not be entered, but included examiner's amendments to modify the specification, to modify original claims 1, 6, and 10, to cancel original claims 3-5 and 8, to modify new claims 11, 16 and 20, and to cancel new claims 13-15 and 18. New claims 11-12, 16-17 and 19-20 were renumbered as claims 11-16.

(7) On November 14, 2009, an order granting reexamination in the present proceeding, 90/009,457, was mailed.

This order was based on the claims and references cited in U.S. Patent No. 5,809,336, as originally issued.

(8) On December 15, 2009, Reexamination Certificate was issued for U.S. Patent No. 5,809,336 in the merged reexamination proceeding. The Reexamination Certificate included the examiner's amendments made in the NIRC mailed on September 11, 2009.

Observations

With reference to the timeline above, the examiner notes that in the present reexamination proceeding, 90/009,457:

(1) The request for reexamination filed August 24, 2009 only discussed claims 1-10 as originally filed and claims 11-20, as first proposed in the September 8, 2008 amendment to the copending merged reexamination proceeding. *The request includes no discussion of the claims as presented in the Reexamination Certificate of December 15, 2009.*

(2) The order of November 14, 2009 was mailed within the statutory time limit of three months after the date of the request for reexamination. The three month time limit ended *before* the Reexamination Certificate was issued for U.S. Patent No. 5,809,336 in the copending merged reexamination proceeding. As a result, this order was based on the claims and references cited in U.S. Patent No. 5,809,336, *as originally issued.*

(3) Because a Reexamination Certificate has now issued for U.S. Patent No. 5,809,336 in the copending merged reexamination proceeding, reexamination in the present proceeding will rely on the claims *in view of the Reexamination Certificate* and will rely on the references cited both in the original prosecution of U.S. Patent No. 5,809,336 and in the copending merged reexamination proceeding.

In simpler terms, because the Reexamination Certificate had not issued at the time the order was mailed, the order was based on prosecution of the original patent.

This Office action, however, must rely on both the prosecution of the original patent and the copending merged reexamination proceeding, which culminated in the issuance of the Reexamination Certificate.

Discussion of the Cited References

The substantially new questions of patentability (SNQs) proposed in the request have been presented as relying on at least one of three base references: Mostek, Dozier and Richter. Each of these references is discussed below:

(1) With regard to Mostek, this reference was not cited during the prosecution of the original patent. However, in the copending reexamination proceeding 90/008,474, the relevance of Mostek to U.S. Patent No. 5,809,336 was discussed in detail (note the request filed January 30, 2007 in 90/008,474). Furthermore, it is clear from the order in the copending reexamination proceeding 90/008,474 that the examiner took the relevance of Mostek into consideration (note the order mailed April 5, 2007 in 90/008,474) when deciding whether to grant or deny reexamination. Reexamination proceeding 90/008,474 has now led to the issuance of a Reexamination Certificate which cites Mostek as prior art (see page 6 of the Reexamination Certificate).

Since the Reexamination Certificate has issued, the references discussed in 90/008,474, including Mostek, are now part of the prosecution history of U.S. Patent No. 5,809,336. Since Mostek has already been described in detail and considered, and since the features of Mostek have not been presented in a new light, there is no longer any substantial new question of patentability with regard to Mostek.

(2) With regard to Dozier, this reference was not cited during the prosecution of the original patent. However, in the copending merged reexamination proceeding noted above, Dozier was cited on an information disclosure statement. Dozier was not discussed in any detail by any of the requester, the patent owner or the examiner during the copending merged reexamination proceeding. Thus, the relevance of Dozier to U.S. Patent No. 5,809,336 as discussed in detail in the request filed August 24, 2009 in this reexamination proceeding presents Dozier in a new light.

Therefore, even though Dozier is of record in the prosecution history of U.S. Patent No. 5,809,336, there is a substantial new question of patentability with regard to Dozier.

The Dozier reference has been carefully considered with respect to the claims. It is noted that the request did not discuss the Dozier reference in relation to the claims as they appear in the Reexamination Certificate noted above.

The request argues that, since Appendix D, column 3, lines 54-57, of Dozier state, "the I/0 port 4 logic block will take the data from the data bus and supply it directly to its output pins at all times. This operation is not synchronized with the ϕC clock", then "This indicates that the I/O port 4 is receiving clocking signals from a clock other than the ϕC internal clock since the I/O port is not synchronized with the ϕC clock."

However, this argument is not convincing. A computer system may operate with many asynchronous (not synchronized) signals, any number of which may be ultimately derived from the same internal system clock.

The request suggests combining Dozier with various prior art systems, including several references that have not been made of record in any information disclosure statement (note, e.g., page 96 of the request), in order to demonstrate that using a second independent clock for an I/O interface was commonplace. However, the request has not set forth a convincing motivation to incorporate such a second clock in Dozier.

In many cases, it was far more efficient to modify the timing of an existing clock signal than to add an entirely separate clock generator to accomplish the same function. There is nothing in Dozier or in the corresponding arguments presented in the request to indicate that an entirely separate clock generator would have been desirable.

(3) With regard to Richter, this reference was not cited during the prosecution of the original patent. However, in the copending merged reexamination proceeding noted above, Richter was cited on an information disclosure statement. Dozier was not discussed in any detail by any of the requester, the patent owner or the examiner during the copending merged reexamination proceeding. Thus, the relevance of Richter to U.S. Patent No. 5,809,336 as discussed in detail in the request filed August 24, 2009 in this reexamination proceeding presents Richter in a new light.

Therefore, even though Richter is of record in the prosecution history of U.S. Patent No. 5,809,336, there is a substantial new question of patentability with regard to Dozier.

The Richter reference has been carefully considered with respect to the claims. It is noted that the request did not discuss the Richter reference in relation to the claims as they appear in the Reexamination Certificate noted above.

The request relies on column 4, lines 34-38, to demonstrate that Richter teaches that the microprocessor 2 and the serial interface may be clocked by separate clock generators.

However, this argument is not convincing. Column 4, lines 34-38, states:

"In certain preferred embodiments, the clock frequency signal 'ftakt' is used as the system clock for the first microprocessor 2. It is also contemplated to instead provide a separate system clock generator for the microprocessor 2. Also, it is contemplated to use the clock frequency signal 'ftakt' as the system clock for the data transmission of the serial interface of the first microprocessor 2, so that the reference signal generator functions as the system clock generator for the first microprocessor 2."

The request relies on the passage "It is also contemplated to instead provide a separate system clock generator for the microprocessor 2". However, this passage does not specify what other elements of the system would be separated from the clocking of the microprocessor – it certainly does not state that such a separate clock for microprocessor 2 will be different than the one used for its own serial interface.

In fact, the next sentence in the passage suggests that the microprocessor 2 and its serial interface always use the *same* system clock, whether it is the clock frequency signal "ftakt" or a separate system clock.

The request further suggests combining Richter with various prior art systems, including several references that have not been made of record in any information disclosure statement (note, e.g., page 126 of the request), in order to demonstrate that using a second independent clock for an I/O interface was commonplace. However, the request has not set forth a convincing motivation to incorporate separate clocks for the microprocessor 2 and its own serial interface in Richter.

In many cases, it was far more efficient to modify the timing of an existing clock signal than to add an entirely separate clock generator to accomplish the same function. There is nothing in Richter or in the corresponding arguments presented in the request to indicate that an entirely separate clock generator or the microprocessor 2 and its own serial interface would have been desirable.

Consequently, claims 1, 2, 6, 7 and 9-16 are confirmed and/or deemed patentable.

Information Disclosure Statement

Form PTO/SB/08, filed March 2, 2010, lists documents that are not patents or printed publications that are the basis of reexamination as described in 37 CFR 1.501(a), 37 CFR 1.510(a) and (b)(3), and MPEP 2256:

Regarding citations AB – AD, the information cited has been considered as described in the MPEP. Note that MPEP 2256 and 2656 indicate that degree of consideration to be given to such information will be normally limited by the degree to which the party filing the information citation has explained the content and relevance of the information. Information that does not appear to be "patents or printed publications" as identified in 35 U.S.C. 301 has been considered to that extent (unless otherwise noted), but has been lined through and will not be printed on any resulting reexamination certificate.

Conclusion

Any comments considered necessary by PATENT OWNER regarding the above statement must be submitted promptly to avoid processing delays. Such submission by the patent owner should be labeled: "Comments on Statement of Reasons for Patentability and/or Confirmation" and will be placed in the reexamination file.

All correspondence relating to this *ex parte* reexamination proceeding should be directed as follows:

By **U.S. Postal Service Mail** to:

Mail Stop *Ex Parte* Reexam
ATTN: Central Reexamination Unit
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand to: Customer Service Window
Randolph Building
401 Dulany St.
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

/B. James Peikari/

B. James Peikari
Primary Examiner
Central Reexamination Unit 3992

JESSICA HARRISON
SUPERVISORY PATENT EXAMINER