IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	Moore et al.
U.S. Patent No.:	5,809,336
Issue Date:	Sept. 15, 1998
Serial No.:	09/484,918
RX Control No.:	90/009,457
Filing Date:	June 7, 1995

Mail Stop Ex Parte Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CORRECTED REQUEST FOR EX PARTE REEXAMINATION UNDER 35 U.S.C. § 302 AND 37 C.F.R. § 1.510

On April 24, 2009 Requester filed a Request for *Ex Parte* Reexamination under 35 U.S.C. § 302 and 37 C.F.R. § 1.510 for all claims (i.e., claims 1-10) of U.S. Patent No. 5,809,336 which issued on September 15, 1998 to Moore et al. On July 23, 2009 the Examiner issued a Notice of Incomplete *Ex Parte* Reexamination Request. The present Corrected Request for *Ex Parte* Reexamination has been amended to address the issues raised in the Notice of Incomplete *Ex Parte* Reexamination Request. A summary of how the issues have been addressed is located in section II of this request. A more complete response to the Notice of Incomplete *Ex Parte* Reexamination Request is found in section VIII of this request. The remainder of the document has been formatted to comply with 37 CFR 1.510 as indicated by the Notice of Incomplete *Ex Parte* Reexamination Request. The Appendices were submitted with the original request and have not changed.

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TABLE OF CONTENTS

TABLE OF CONTENTS

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TABLE OF CONTENTS

TABLE OF CONTENTS

TABLE OF CONTENTS

APPENDICES

I. INTRODUCTION

The independent claims of the '336 patent are directed to a microprocessor system that includes a ring oscillator for a system clock and a central processing unit (CPU) on a single integrated circuit. The independent claims require the ring oscillator and CPU to be constructed of the same process technology so that the speed of the ring oscillator and the CPU vary together. The independent claims further require an on-chip input/output (I/O) interface, to which a second clock independent of the ring oscillator is connected.

During prosecution of the underlying application the Patent Owner amended the independent claims in response to a prior art rejection to recite the second clock independent of the variable speed system clock for clocking the I/O interface. A summary of an examiner interview conducted on April 23, 1998 indicated that the claims were allowed because the Examiner believed that the prior art contained no disclosure or suggestion of clocking an I/O interface with a second clock independent of the variable speed system clock.

The Mostek reference *(Appendix F)*, which was not before the original Examiner, discloses precisely this feature. Mostek describes a single semiconductor chip containing a main control logic that is clocked by a variable frequency internal oscillator. The chip includes a serial I/O port that is clocked by a fixed frequency external clock that is independent of the internal oscillator. *(Appendix F, pages III-105 and III-114 to III-115)* Furthermore, the Mostek reference teaches every other feature recited in each of the independent claims of the '336 patent with the sole exception that the Mostek reference does not explicitly state that the on-chip "variable speed oscillator" is a "ring oscillator" as recited in the claims. However, according to the Patent Owner, a variable speed oscillator qualifies as a ring oscillator as that term is used in the '336 patent. In connection with recent attempts to persuade major companies to take licenses under the '336 patent the Patent Owner has repeatedly asserted in writing that "industry best practices dictate" that clock generators include ring oscillators. If the Office accepts this premise, then the Mostek reference would be understood by one skilled in the art as disclosing a ring oscillator given that commercial clock generators have not substantially changed in material respect since the date of the Mostek reference. If interpreted in this way, the Mostek reference anticipates claims 1-7, 9, and 10 of the '336 patent.

In any case, one skilled in the art would have found apparent reasons to combine the Mostek reference with the ring oscillator system clock taught by the Kato reference *(Appendix H)*. One skilled in the art would realize the benefits of implementing Kato's ring oscillator as Mostek's variable oscillator to reduce power consumption during periods of lessened processing demand and to increase clock speed (and power consumption) during periods of increased processing demand. *(Appendix H, col. 11, lines 2-7).* As explained in more detail below, claims 1-10 of the '336 patent are at a minimum rendered obvious by Mostek in view of Kato.

Moreover, two additional references that were not before the Examiner – Richter *(Appendix D)* and Dozier *(Appendix E)* – each disclose the second, independent I/O clock thought to be missing from the prior art. Richter teaches clocking an on-chip I/O port with an oscillator independent of a system clock. Richter teaches a microprocessor system having a serial interface which is connected by an input/output port to a signal line of a serial bus system. Richter teaches a signal "ftakt" for clocking the serial I/O port of the microprocessor that is independent of the CPU clock: "the data transmission of the serial interface is supplied with the clock frequency signal 'ftakt', and the microprocessor of the microprocessor system 2 is equipped with its own system clock generator." *(Appendix D, col. 4, lines 34-43 and 58-62)* Richter describes the system clock of the microprocessor as a "separate system clock generator for the microprocessor" that is independent of the I/O clock signal. *(Appendix D, col. 4, lines 36-47)* The remaining features recited in the claims of the '336 patent are plainly disclosed in Richter. Dozier also discloses the above described features of the claims of the '336 patent. Both Richter and Dozier, alone or in combination with other references, at a minimum render obvious all claims of the '336 patent (i.e. claims 1-10) as explained in detail in the claim charts set forth below.

The foregoing questions of patentability are new even with respect to the reexamination requests previously filed against the '336 patent. Neither the Richter reference *(Appendix D)* nor the Dozier reference *(Appendix E)* were before the examiner during the original examination of the '336 patent and are not currently before the examiner in the pending merged reexamination proceeding *(Reexamination Control Number 90/008,306)*. As to

the Mostek reference, the arguments presented herein are substantially different than those presented in the reexamination request filed by the Public Patent Foundation on January 30, 2007. For example, that earlier request did not argue that the Mostek reference anticipates any claim of the '336 patent. The Mostek reference has not been relied upon to support a rejection in the pending reexamination proceedings (and as to the underlying application the Mostek reference was not of record).

II. SUMMARY OF RESPONSE TO NOTICE OF INCOMPLETE REEXAMINATION REQUEST

The Notice of Incomplete *Ex Parte* Reexamination Request for the '336 patent states, under Item I, that the requester has failed to explicitly identify the new technological teaching for each proposed rejection/application of the art that raises a substantial new question of patentability (SNQ).

A. The Mostek, Dozier, and Richter References present New, Non-Cumulative Technical and Highly Material Teachings that are Not Present in Any Prior Art of Record

In its original request for *ex parte* reexamination, Requester proposed substantial new questions of patentability based upon the Mostek, Kato, Dozier, Ledzius, Richter, McDermott, and IC Master prior art references. With regard to the Mostek reference, the Office has correctly pointed out that in the currently pending reexamination proceedings for the '336 patent (*Reexamination Control Number 90/008,474*) the examiner in those proceedings stated that "[e]ach of these prior art references have been considered... However, they are not applied in this particular action since they recite teachings which otherwise already exist in either Kato or Ledzius et al."

Requester respectfully submits that the Mostek reference is clearly not cumulative to the prior art of record. For instance, Kato teaches an integrated circuit having a first clock generator 14 which can be a ring oscillator and a second clock generator 15. However, while the second clock generator 15 taught by Kato is distinct from the first clock generator 14, the second clock generator 15 is not completely independent of the first clock generator 14 in that the second clock generator 15 generates clock signals based on a reference clock signal $\phi 0$

received from the first clock generator 14. In contrast, as described in greater detail **in section VIII (B) of this request**, the Mostek reference teaches an integrated circuit having an "on-chip oscillator circuit which provides an internal clock" for supplying clocking signals to the CPU, and a separate, completely independent second clock for providing clocking signals to the serial I/O port of the integrated circuit. The second clock taught by Mostek does not receive any inputs from the on-chip oscillator. This teaching of two completely independent clocks where the second clock is used to provide clocking signals to an I/O port is a non-cumulative technical teaching that is not present in any prior art of record and thus raises a substantial new question of patentability. Additionally, a second clock, independent of a variable speed system clock, for clocking an I/O interface as claimed in the '336 patent and taught by Mostek is preciously the functionality thought to be missing from the prior art of Record.

Furthermore, the Dozier reference is non-cumulative to the teachings of record and was not before the examiner in either the original prosecution or the reexamination of the '336 patent. For instance, as explained above, Kato teaches an integrated circuit having first and second clock generators where the second clock generator is not completely independent of the first clock generator in that the second clock generator generates clock signals based on a reference clock signal received from the first clock generator. In contrast, as described in greater detail in **section VIII (B) of this request**, the Dozier reference teaches an integrated circuit having "an internal oscillator which is activated when both the XTL 1 and XTL 2 pins are grounded" and a second clock, independent from the internal oscillator, for providing clocking signals to an I/O interface. Dozier's teaching of an internal clock and a second completely independent clock where the second clock is used to provide clocking signals to an I/O port is a non-cumulative teaching that is not present in any prior art of record and thus raises a substantial new question of patentability. Additionally, a second clock, independent of a variable speed system clock, for clocking an I/O interface as claimed in the '336 patent and taught by Dozier is preciously the functionality thought to be missing from the prior art of Record.

Furthermore, the Richter reference is non-cumulative to the teachings of record and was not before the examiner in either the original prosecution or the reexamination of the '336

patent. For instance, as explained above, Kato teaches an integrated circuit having first and second clock generators where the second clock generator is not completely independent of the first clock generator. In contrast, as described in greater detail in **section VIII(B) of this request**, the Richter reference teaches an integrated circuit having a "voltage-controlled oscillator" for generating "a clock pulse 'ftakt'" for providing clocking signals to an I/O port *(Appendix D, col. 3, lines 18-20)*. Richter teaches an embodiment in which the microprocessor is clocked by a "separate system clock generator for the microprocessor 2." *(Appendix D, col. 4, lines 34-38)*. This teaching of two completely independent voltage controlled oscillators where the first voltage controlled oscillator provides system clock signals and the second voltage controlled oscillator is used to provide clocking signals to an I/O port is a non-cumulative technical teaching that is not present in any prior art of record and thus raises a substantial new question of patentability. Additionally, a second clock, independent of a variable speed system clock, for clocking an I/O interface as claimed in the '336 patent and taught by Richter is preciously the functionality thought to be missing from the prior art of Record.

B. This Request has been Modified to Clearly Set forth Discrete SNQs as Directed in the Notice of Incomplete Reexamination Request

The Notice of Incomplete *Ex Parte* Reexamination Request for the '336 patent states, under Item II, that the "request has failed to provide the requisite detailed explanation of the pertinency and manner of applying the cited prior art to every claim for which reexamination is requested." As specific examples, the Examiner states that it is unclear whether claim 8 is proposed to be rejected under 35 U.S.C.l02(b) as being anticipated by Mostek, or whether claim 1 is proposed to be rejected under 35 U.S.C. 103(a) as being obvious over Mostek, or whether claim 1 is proposed to be rejected under 35 U.S.C. 103(a) as being obvious over Mostek in view of Kato, etc. The Corrected Request for E*x Parte* Reexamination has been ammended to more clearly lay out the manner of applying the cited prior art to every claim for which reexamination is requested. The claim charts and explanations for applying the cited prior art have been separated to distinctly indicate how each reference and each combination of

references are to be applied to each claim of the '336 patent in each of the proposed rejections.

The Notice of Incomplete *Ex Parte* Reexamination Request for the '336 patent additionally states that "the claim charts appear inconsistent with the proposed rejections in that they discuss prior art that is not identified as a basis for a substantial new question, and that is not cited in the proposed rejections." The Corrected Request for Ex Parte Reexamination has been amended to clearly indicate every reference and combination of references that presents an SNQ and to distinctly indicate how each reference and each combination of references are to be applied to each claim of the '336 patent in each of the proposed rejections.

C. This Request Properly Addresses the New Claims That Have Been Added in the Pending Reexamination Proceedings.

The Notice of Incomplete *Ex Parte* Reexamination Request for the '336 patent states, under Item III, that "[a]n SNQ may only be based on patents and printed publications, not on copending reexamination proceedings." Requester submits that this corrected request for reexamination clearly points out Significant New Questions of patentability for claims 1-10 of the '336 patent that are different from previously raised SNQs. Requester points out that MPEP § 2240, subsection II allows for the requester to "provide information raising a substantial new question of patentability with respect to any new or amended claim which has been proposed under 37 CFR 1.530(d) in the first (or prior) pending reexamination proceeding." Therefore, the discussion of claims 11-20 of the '336 patent which have been added in the copending merged reexamination proceeding (*Reexamination Control Number 90/008,474*) is proper.

D. This Request is Served Upon the Agent of Record at His New Correspondence Address

The Notice of Incomplete *Ex Parte* Reexamination Request for the '336 patent states, under Item IV, that "the correspondence address for the patent owner has been changed." The change in correspondence address for the patent owner has been noted. The corrected request as well as a copies of prior-filed papers will be served to the patent owner at the

current correspondence address indicated in the patent record as of the time of filing of this request.

III. CLAIMS FOR WHICH REEXAMINATION IS REQUESTED

Reexamination is requested for all claims (i.e., claims 1-10) of the '336 patent in view of the publications discussed below. A copy of the '336 patent (including a certificate of correction) were previously submitted as Appendix A of this document, and copies of the relevant portions of the '336 patent prosecution history were previously submitted as Appendix B.

IV. PATENTS AND PRINTED PUBLICATIONS PRESENTED TO SHOW SUBSTANTIAL NEW QUESTIONS OF PATENTABILITY

1. U.S. Patent No. 4,853,841 to Richter (hereinafter "Richter"), Appendix D.
2. U.S. Patent No. 4,348,743 to Dozier (hereinafter "Dozier"), Appendix E.
3. Mostek, 3870 Microcomputer Data Book (Feb. 1981) (hereinafter "Mostek") Appendix F.
4. U.S. Patent No. 4,931,748 to McDermott et al (hereinafter "McDermott") Appendix G.
5. U.S. Patent No. 4,766,567 to Kato (hereinafter "Kato") attached as Appendix H.
6. U.S. Patent No. 4,691,124 to Ledzius et al (hereinafter "Ledzius") Appendix I.
7. IC Master 1980 (United Technical Publications) (1980) (hereinafter "IC Master") Appendix J.

It is believed that the references in Appendices D-J were not before the Examiner during prosecution of the '336 patent. Further, it is believed that the references in Appendices D, E, and G are not before the Examiner in the below described reexaminations of the '336 patent. For convenience, the aforementioned references are cited on the previously submitted Form PTO-1449.

V. CO-PENDING PROSECUTION AND LITIGATION

Requester believes that the '336 patent has not yet been adjudged invalid or unenforceable. Three reexaminations of the '336 patent, control numbers 90/008,237, 90/008,306, and 90/008,474, have been merged and are ongoing as of this request's filing date. Requester is aware of several pending lawsuits involving the '336 patent:

- Acer, Inc. et al. v. Technology Properties Limited et al., CV 08-00877 HRL, Filed Feb. 8, 2008 (N.D. Cal.)
- HTC Corp. et al. v. Technology Properties Limited et al., CV 08-00882 JL, Filed Feb. 8, 2008 (N.D. Cal.)
- BARCO v. Technology Properties Limited et al., CV 08-05398, Filed Dec. 1, 2008 (N.D. Cal.)

VI. THE PROSECUTION HISTORY OF THE '336 PATENT

The application that matured into the '336 patent was filed on June 7, 1995 as a division of U.S. Patent No. 5,440,749 which itself was filed on August 3, 1989. The '336 application included 70 claims, although all but six were immediately cancelled. Claim 19, the only claim to survive the entire prosecution, eventually became Claim 1 of the '336 patent and originally read:

> A microprocessor system, comprising a central processing unit and a ring counter variable speed system clock connected to said central processing unit, said central processing unit and said ring counter variable speed system clock being provided in a single integrated circuit.

(Appendix B, Application, June 6, 1995, original page 68).

During examination of the '336 application, the Examiner issued four office actions and the Applicant amended the claims in response to each. The Examiner rejected the independent claims after each subsequent amendment by the Applicant. After the fourth office action, an Examiner interview was held on April 23, 1998. During the interview, the Examiner proposed amendment of original dependent claims 20, 66, 75, and 79 and indicated that the amended claims 20, 66, 75, and 79 would be allowable if rewritten in independent form. *(Appendix B, Applicant Remarks, April 24, 1998; Examiner Interview Summary Record, May 13, 1998)* Each of

original claims 20, 66, 75, and 79 included a limitation directed toward an input/output interface that is connected to a second clock which is independent of the ring oscillator. The Applicant accordingly amended the independent claims to include the limitations of original dependent claims 20, 66, 75, and 79. Namely, the independent claims were amended to recite an on-chip I/O interface and a second I/O clock that is independent of the ring oscillator. For example, claim 19 was amended:

> A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.

(Appendix B, Applicant Remarks, April 24, 1998 at Claim 19). The application was subsequently allowed.

Accordingly, the '336 patent was allowed principally because the prior art before the Examiner was believed not to disclose an integrated circuit with an on-chip I/O interface clocked by a second clock independent of the variable speed system clock.

VII. POSITIONS TAKEN BY PATENT OWNER THAT ARE MATERIAL TO PATENTABILITY

The Patent Owner has sent numerous communications to third parties in an attempt to solicit licenses under the '336 patent. The communications generally include claim charts stamped "confidential" that purport to show the correspondence between the third party processor systems and the claims of '336 patent.

In these claim charts the Patent Owner has taken various positions to the effect that any processors having certain features would necessarily have other features recited in the claims

of the '336 patent. These are particularly relevant to the Office's assessment of how one skilled in the art would interpret various prior art references. In particular, if the Patent Owner's assertions are accepted, then various prior art references explicitly teaching certain features would be understood by one skilled in the art as implicitly disclosing other features.

Where the Patent Owner has taken a position in third party correspondence which would dictate a finding that a certain feature would be understood to be present in a prior art system, that fact is noted in the claim charts set forth below.

The Office is encouraged to request from the Patent Owner the claim charts and related third party communications concerning the '336 patent under Rule 105.[1] Requester understands that scores of substantially similar claim charts have been sent to various companies throughout the semiconductor and other industries.

The Requester notes that the functionality of prior art processors are the same in material respect as commercial processors referred to by the Patent Owner in the above mentioned communications to third parties (e.g., with regard to on-chip oscillators, serial I/O ports, etc.). For example, the Mostek 3870 family of processors of the 1980's included serial I/O ports with independent I/O clocks for conducting asynchronous I/O functions. *(See, e.g., Mostek, 3870 Microcomputer Data Book (Feb. 1981) at page III-105).* Therefore, if the Patent Owner's assertions are true today as to commercial processors, then they are also true as to the prior art processors.

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[1] Requester submits that the Office is empowered to request this information under Rule 105, which provides in pertinent part:

> (a) (1) In the course of examining or treating a matter in a pending or abandoned application filed under 35 U.S.C. 111 or 371 (including a reissue application), in a patent, or in a reexamination proceeding, the examiner or other Office employee may require the submission, from individuals identified under § 1.56(c), or any assignee, of such information as may be reasonably necessary to properly examine or treat the matter, for example:
>
> . . .
>
> (viii) Technical information known to applicant. Technical information known to applicant concerning the related art, the disclosure, the claimed subject matter, other factual information pertinent to patentability, or concerning the accuracy of the examiner's stated interpretation of such items.

The assertions of infringement made by Patent Owner explicitly contain a technical assessment of architecture defining a ring oscillator, a second clock independent of the ring oscillator, and whether the ring oscillator and a CPU clocked by the ring oscillator inherently include a plurality of devices and whether the frequency of the ring oscillator and the speed of the CPU would vary together due to manufacturing due to manufacturing variations. Requestor respectfully submits that this information is clearly "factual information pertinent to patentability." The Office is accordingly urged to request that the Patent Owner produce claim charts and other materials submitted to third parties sufficient to demonstrate the technical and claim construction positions taken by the Patent Owner.

VIII. THE MOSTEK, DOZIER, AND RICHTER REFERENCES PRESENT NEW, NON-CUMULATIVE TECHNICAL TEACHINGS THAT ARE NOT PRESENT IN ANY PRIOR ART OF RECORD.

A. The Prior Art References Present a Substantial New Question of Patentability

The prior art references provided in this request present a substantial new question of patentability as to claims 1-10 of the '336 patent even with respect to the reexamination requests previously filed against the '336 patent. Both the Richter reference *(Appendix D)* and the Dozier reference *(Appendix E)* were not before the examiner during the original examination of the '336 patent and are not currently before the examiner in the pending merged reexamination proceeding *(Reexamination Control Number 90/008,306)*. As to the Mostek reference, the arguments presented herein are substantially different than those presented in the reexamination request filed by the Public Patent Foundation on January 30, 2007. For example, that earlier request did not argue that the Mostek reference anticipates any claim of the '336 patent. Furthermore, the Mostek reference has never been adopted for use in a rejection during the pending reexamination proceedings. The following sections set forth in detail the correspondence between claims 1-10 and the Mostek, Richter, and Dozier references.

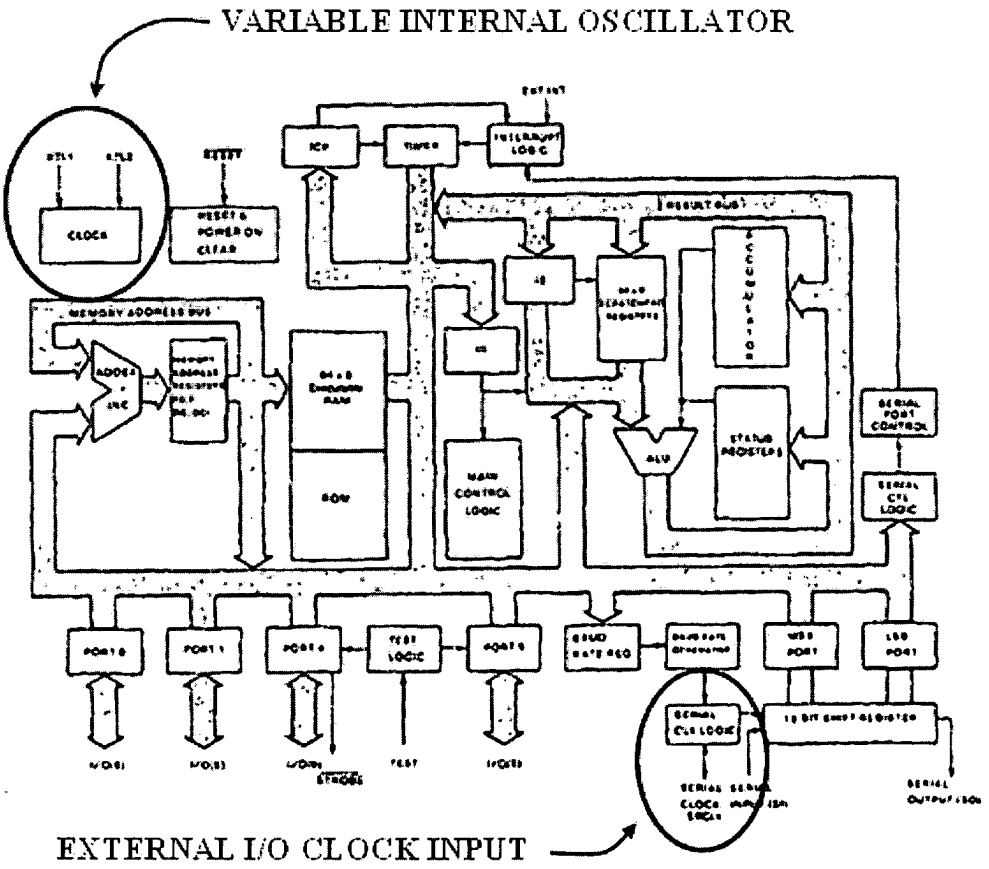
B. Response to Specific Issues Raised by the Notice of Incomplete *Ex Parte* Reexamination Request

1. Mostek is Highly Material and Non-cumulative

Requester respectfully submits that the Mostek reference is clearly not cumulative to the prior art of record. Mostek teaches a key feature which is not present in any of the previously considered prior art of record, namely, a second clock connected to an I/O port that is completely independent of a system clock, where the clock signal generated by the second clock is not based on a clock signal received from the first clock. As described in greater detail below, none of the prior art references of record teach this feature.

Mostek teaches a "single chip microcomputer" that includes an "on-chip oscillator circuit which provides an internal clock." *(Appendix F, pages III-114 to III-115)*. The frequency of the on-chip oscillator, and thus the processing speed of the main control logic, varies in

response to temperature and Vcc variations, as one skilled in the art would understand from reference to other data books describing the MK3873 microprocessor. *(Appendix J, Fig. 3; pages 2019 and 2024-2026).* Mostek further teaches a serial I/O port that is clocked by a second external clock independent of the on-chip oscillator circuit. *(Appendix F, pages III-105 and III-114 to III-115).* The second I/O clock taught by Mostek does not receive any inputs from the on-chip oscillator. Rather, Mostek teaches that the second clock "is derived from the SRCLK pulse. The SRCLK pulse . . . may be programmed as an input." *(Appendix F, page III-105).* Figure 1 of Mostek (below) shows the internal oscillator and the separate I/O clock.



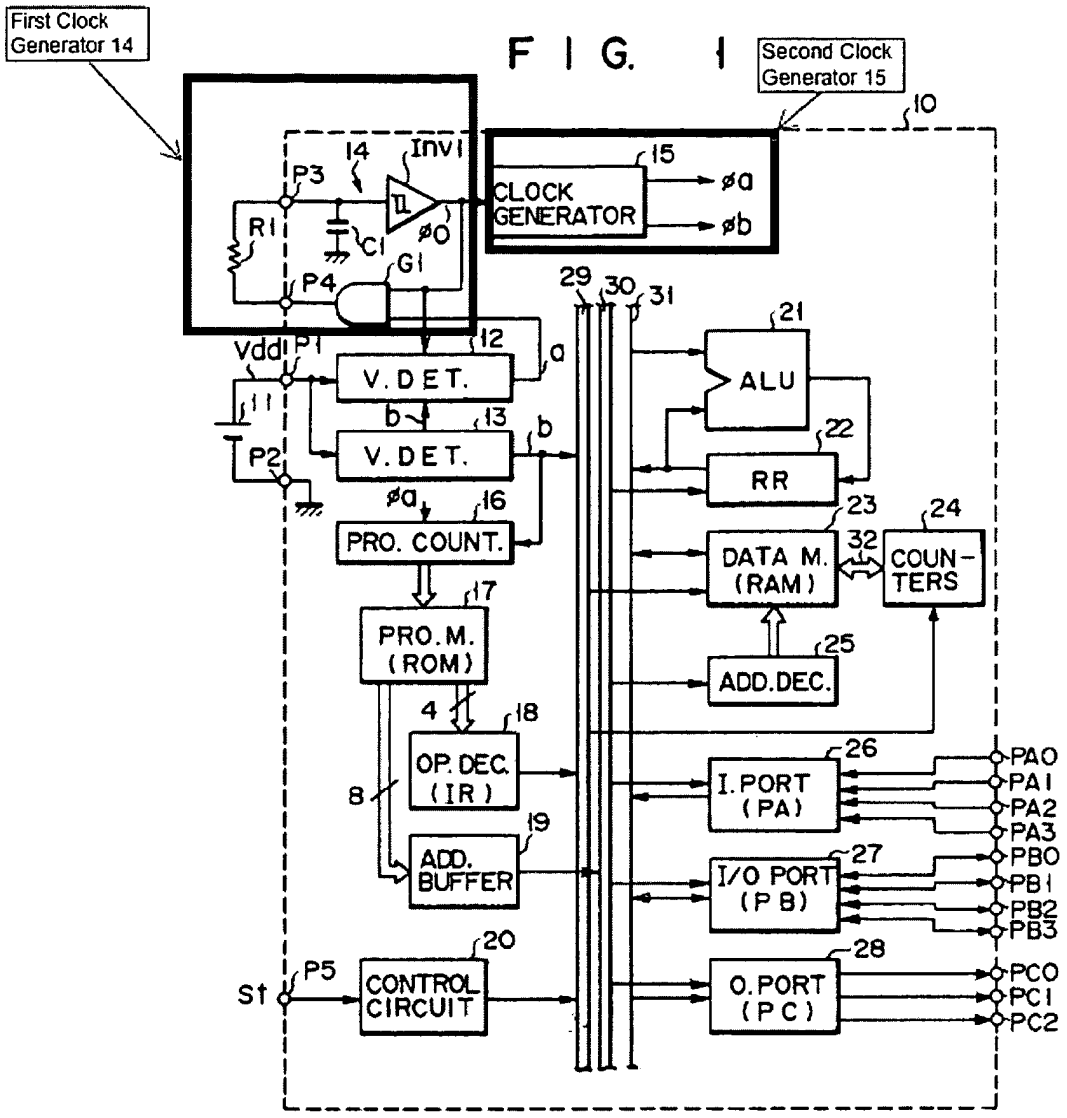
(Appendix F, Figure 1 at page III-103).

This teaching of two completely independent clocks where the first clock provides clocking signals to a CPU and the second clock is used to provide clocking signals to an I/O port without receiving clock signals from the first clock is a non-cumulative technical teaching that is

not present in any prior art of record. As outlined below, neither the Magar, Kato, nor Ledzius references teach this feature.

US Patent 4,503,500 to Magar (the Magar reference), which was cited in the original examination of the application that resulted in the '336 patent, does not teach this functionality. The Magar reference was used as the basis for rejections under 35 U.S.C. 103(a) in office actions dated April 3, 1997 and October 16, 1997. Magar teaches a clock generator 17 and a cpu fabricated on the same chip. The system taught by Magar additionally includes multiple I/O ports. However, there is no discussion in Magar of a separate clock connected to the I/O ports or of any clock other than the clock generator 17. Additionally, a summary of an examiner interview conducted on April 23, 1998 indicated that the claims of the '336 patent were allowed over the prior art of record (which included the Magar reference) after limitations relating to an on-chip I/O interface clocked by a second clock independent of the variable speed system clock were added to the independent claims.

US Patent 4,766,567 to Kato, which has been cited in the copending merged reexamination proceeding (*Reexamination Control Number 90/008,474*), additionally fails to teach this functionality. The Kato reference, in combination with Ledzius, was used as the basis for rejections under 35 U.S.C. 103(a) in office actions dated July 2, 2008 and March 17, 2009. Kato teaches an integrated circuit having a first clock generator 14 which can be a ring oscillator and a second clock generator 15. Fig. 2 of Kato (below) shows the first and second clock generator circuits.



F I G. 1

The second clock generator 15 taught by Kato is physically distinct from the first clock generator 14, in that the second clock generator 15 occupies a different space on the integrated circuit than the first clock generator 14. However, the second clock generator 15 is not completely independent of the first clock generator 14 in that the second clock generator 15 generates clock signals based on a reference clock signal ϕ0 received from the first clock generator 14. Fig. 2 (above) shows the clock signal ϕ0 being supplied from an output of the first clock generator 114 to an input of the second clock generator 115. Therefore, the second clock generator 15 is not completely independent of the first clock generator 114 and Kato therefore

does not teach two completely independent clocks where the first clock provides clocking signals to a CPU and the second clock is used to provide clocking signals to an I/O port without receiving clock signals from the first clock.

Further, US Patent 4,691,124 to Ledzius et al., which has been cited in the copending merged reexamination proceeding (Reexamination Control Number 90/008,474), does not teach this functionality. The Ledzius reference, in combination with Kato, was used as the basis for rejections under 35 U.S.C. 103(a) in office actions dated July 2, 2008 and March 17, 2009. The Ledzius reference was used as a secondary reference in combination with Kato in order to teach the limitation of the internal oscillator and the cpu being "correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit." Ledzius teaches a clock generator 18 for providing clock signals to various other components of an integrated circuit. The clock generator 18 varies to reflect process variations throughout the circuit and temperature variances. Ledzius teaches that the integrated circuit includes one or more data ports. However, there is no discussion in Ledzius of a second, separate clock connected to the data ports. Therefore Ledzius fails to teach two completely independent clocks where the first clock provides clocking signals to a CPU and the second clock is used to provide clocking signals to an I/O port without receiving clock signals from the first clock.

As can be seen from the above descriptions of the previously cited references, Mostek teaches a key feature which is not present in Magar, Kato, Ledzious, or any other previously considered prior art of record, namely, a second clock connected to an I/O port that is completely independent of a system clock, where the clock signal generated by the second clock is not based on a clock signal received from the first clock. This teaching of an internal clock and a second completely independent clock where the second clock is used to provide clocking signals to an I/O port is a non-cumulative technical teaching that is not present in any prior art of record and thus raises a substantial new question of patentability.

2. **Dozier is Highly Material and Non-cumulative**

US Patent 4,348,743 to Dozier is non-cumulative to the teachings of record and was not before the examiner in either the original prosecution or the reexamination of the '336 patent. Specifically, Dozer teaches a key feature which is not present in any of the previously considered prior art of record, namely, a second clock connected to an I/O port that is completely independent of a system clock, where the clock signal generated by the second clock is not based on a clock signal received from the first clock. As described above, none of the Magar, Kato, or Ledzious references teaches this functionality of a second clock connected to an I/O port that is completely independent of a system clock.

The Dozier reference teaches a microprocessor that is implemented on a single semiconductor chip, contains a main control logic that is clocked by an internal oscillator, and has input/output ports. Specifically, the reference discloses a "microprogrammed computer 10 which may be implemented by MOS/LSI techniques and which may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-63).* Dozier further teaches that the clock generator 38 of the microprogrammed computer includes "an internal oscillator which is activated when both the XTL 1 and XTL 2 pins are grounded." This internal oscillator provides clocking signals for the Main Control Logic taught by the Dozier reference. The ΦC (the main cycle clock) signal generated by the clock generator 38 "is the cycle clock for the computer system 10." *(Appendix E, col. 5, lines 9-14 and 5, lines 27-28).* Furthermore, the "main control logic 26" is a "principle functional section[] of the microcomputer 10." *(Appendix E, col. 2, lines 63-68).*

Dozier additionally teaches a test mode for the microprogrammed computer 10, whereby information on one of the ports is immediately fed into the data bus at a rate not synchronized with the clock generator, a form of serial communication. Specifically, in test mode "port 5 will take the information existing on its pins and drive it into the internal data bus [which] permits port 5 to be a dedicated input to the internal data bus." *(Appendix D, col. 3, lines 62-66).* Likewise, "the I/O port 4 logic block will take the data from the data bus and supply it directly to its output pins at all times. This operation is <u>not synchronized</u> with the ΦC clock." *(Appendix D, col. 3, lines 54-57) (emphasis added).* This indicates that the I/O port 4 is

receiving clocking signals from a clock other than the ΦC internal clock since the I/O port is not synchronized with the ΦC clock. Additionally the Patent Owner of the '336 patent has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8).* Therefore, the serial I/O port 4 taught by Dozier, satisfies the limitation of a second independent clock signal, according to the technical assertions made by the Patent Owner.

As can be seen from the above description, Dozier teaches a key feature which is not present in Magar, Kato, Ledzious, or any other previously considered prior art of record, namely, a second clock connected to an I/O port that is completely independent of a system clock, where the clock signal generated by the second clock is not based on a clock signal received from the first clock. This teaching of an internal clock and a second completely independent clock where the second clock is used to provide clocking signals to an I/O port is a non-cumulative technical teaching that is not present in any prior art of record and thus raises a substantial new question of patentability.

3. Richter is Highly Material and Non-cumulative

US Patent 4,853,841 to Richter is non-cumulative to the teachings of record and was not before the examiner in either the original prosecution or the reexamination of the '336 patent. Specifically, Richter teaches a key feature which is not present in any of the previously considered prior art of record, namely, a second clock connected to an I/O port that is completely independent of a system clock, where the clock signal generated by the second clock is not based on a clock signal received from the first clock. As described above, none of the Magar, Kato, or Ledzious references teaches this functionality of a second clock connected to an I/O port that is completely independent of a system clock.

The Richter reference teaches a microprocessor system 2 having a "voltage-controlled oscillator" for generating "a clock pulse 'ftakt' that acts upon the microprocessor system." *(Appendix D, col. 3, lines 18-20).* In some embodiments the 'ftakt' signal is used as both the system clock and a clock for the I/O port. *(Appendix D, col. 4, lines 34-43).* In other

embodiments Richter teaches that the microprocessor is clocked by a "separate system clock generator for the microprocessor 2." *(Appendix D, col. 4, lines 34-38).* It is inherent to use a second, voltage controlled oscillator as the separate system clock generator because Richter already teaches clocking the microprocessor with a voltage controlled oscillator in a different embodiment. Richter further teaches an embodiment in which the microprocessor system 2 is provided "in a one-chip system" with a microprocessor, RAM and ROM memory chips, a serial interface, and "other chips required for their operation." Therefore, the Richter reference teaches a single integrated circuit having two separate voltage controlled oscillators, one for providing system clock signals, and a second independent voltage controlled oscillator for generating the signal "ftakt" for clocking the I/O port. There is no indication in the Richter reference that the second independent clock receives input signals from the system clock or is in anyway dependent on the system clock for generating clock signals.

As can be seen from the above description, Richter teaches a key feature which is not present in Magar, Kato, Ledzious, or any other previously considered prior art of record, namely, a second clock connected to an I/O port that is completely independent of a system clock, where the clock signal generated by the second clock is not based on a clock signal received from the first clock. This teaching of an internal clock and a second completely independent clock where the second clock is used to provide clocking signals to an I/O port is a non-cumulative technical teaching that is not present in any prior art of record and thus raises a substantial new question of patentability.

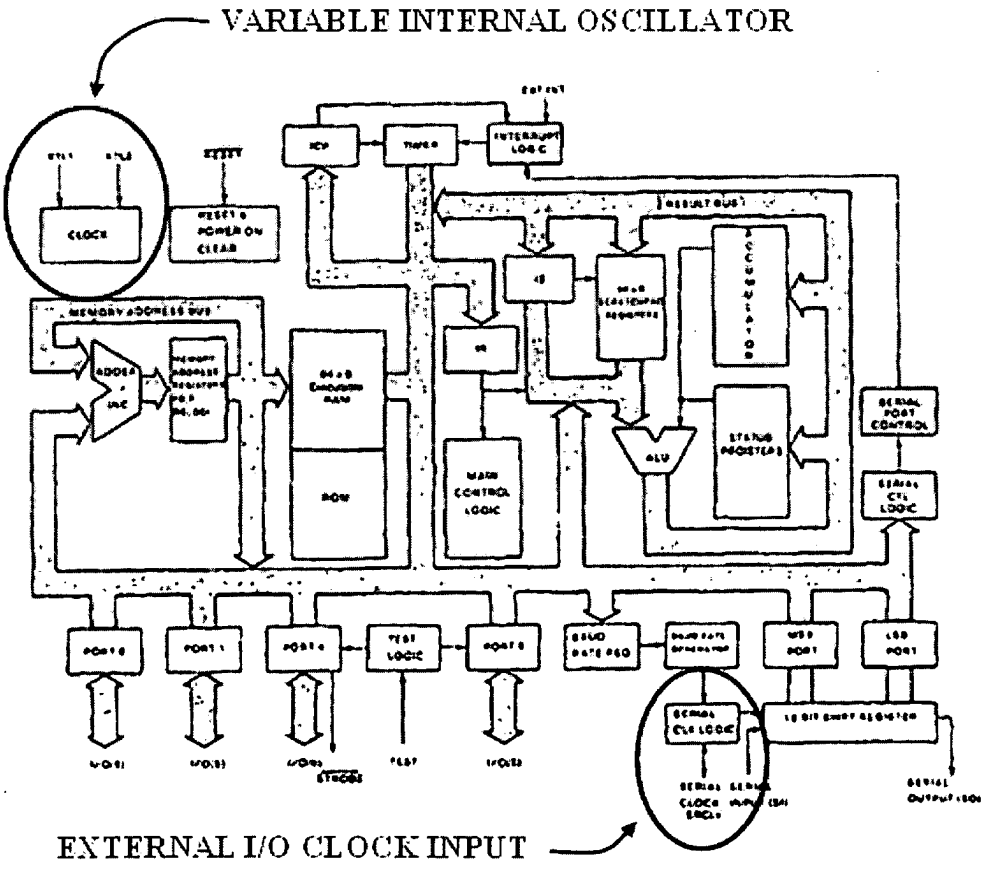
IX. THE MOSTEK REFERENCE, IN COMBINATION WITH THE IC MASTER, KATO, AND LEDZIUS REFERENCES RENDERS OBVIOUS CLAIMS 1-10 OF THE '336 PATENT

The prior art references provided in this request raise substantial new questions of patentability as to claims 1-10 of the '336 patent. Specifically, all claims (e.g. claims 1-10) are rendered obvious by Mostek in light of the IC Master, Kato, and Ledzius references.

A. Summary of the Teachings of the Mostek Reference

The Mostek, 3870 Microcomputer Data Book (Feb. 1981) ("Mostek") teaches the MK3873, which the data book describes as a single semiconductor chip containing a main control logic that is clocked by a variable internal oscillator. The MK3873 single semiconductor chip also includes a serial I/O port that can be clocked by a fixed frequency, external clock that is independent of the internal oscillator.

More specifically, Mostek teaches a "single chip microcomputer" that includes an "on-chip oscillator circuit which provides an internal clock." *(Appendix F, pages III-114 to III-115).* The frequency of the on-chip oscillator, and thus the processing speed of the main control logic, varies in response to temperature and Vcc variations, as one skilled in the art would understand from reference to other data books describing the MK3873 microprocessor. *(Appendix J, Fig. 3; pages 2019 and 2024-2026).*



(Appendix F, Figure 1 at page III-103).

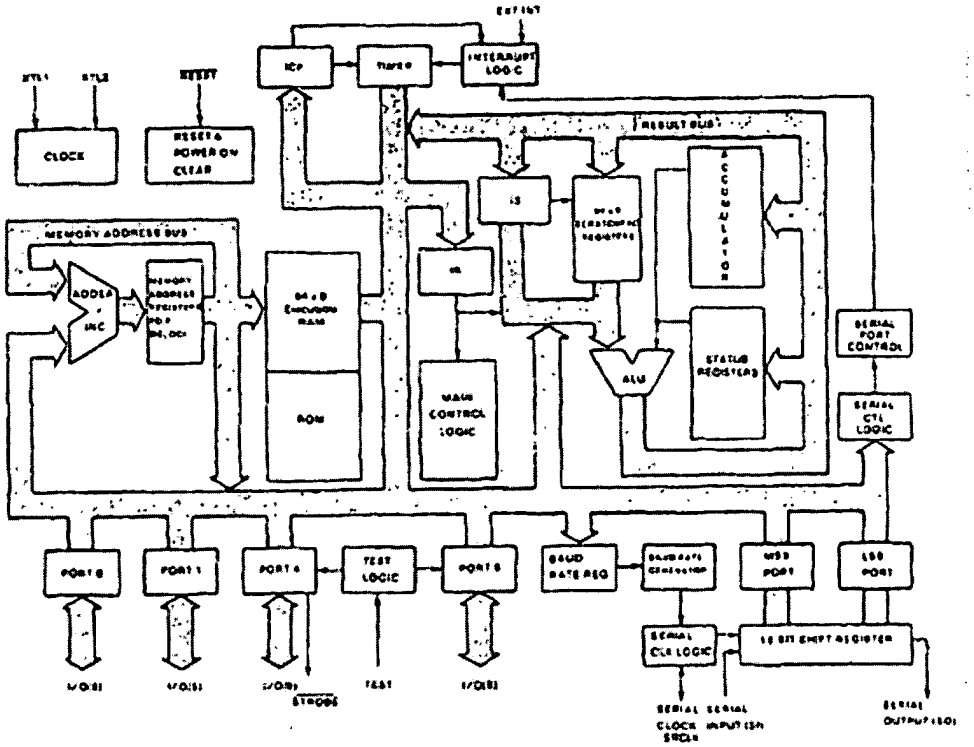
Mostek teaches a serial I/O port that is clocked by an external clock independent of the on-chip oscillator circuit. *(Appendix F, pages III-105 and III-114 to III-115).* The external clock may use a crystal to provide a fixed frequency signal. *(Appendix F, pages III-109 to III-110).* Additionally, the serial port is "very flexible so that it could be used . . . as an interface to . . . serial memory devices." *(Appendix F, page III-102, col. 1).*

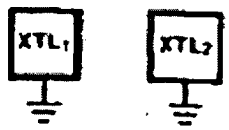
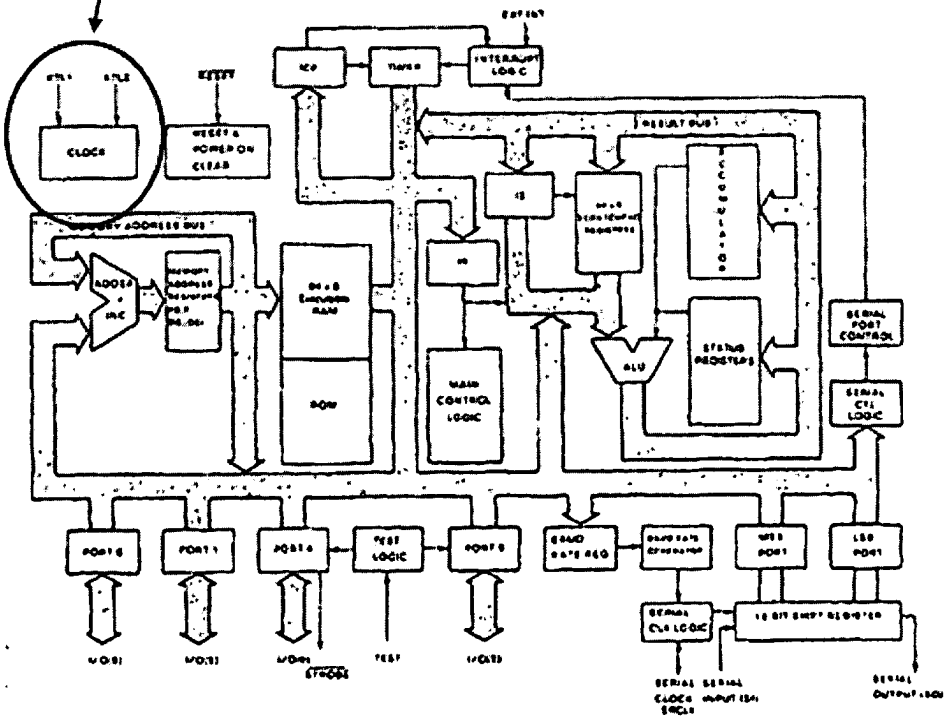
B. SNQ #1: The Mostek Reference, in Light of the IC Master Reference, Renders Obvious Claims 1-7, 9, and 10 of the '336 Patent

The '336 patent claims the same functionality described above in connection with the Mostek reference. The patent claims a microprocessor system comprising a single integrated circuit that includes a ring oscillator and a central processing unit (CPU), where the ring oscillator clocks the CPU. *(Appendix A, Claim 1).* The claimed ring oscillator and CPU include a plurality of electronic devices that are constructed of the same process technology so that the frequency of the central processing unit and the speed of the ring oscillator vary together. *(Appendix A, Claim 1).* The claimed integrated circuit also includes an on-chip I/O interface, to which a second clock independent of the ring oscillator is connected. *(Appendix A, Claim 1).*

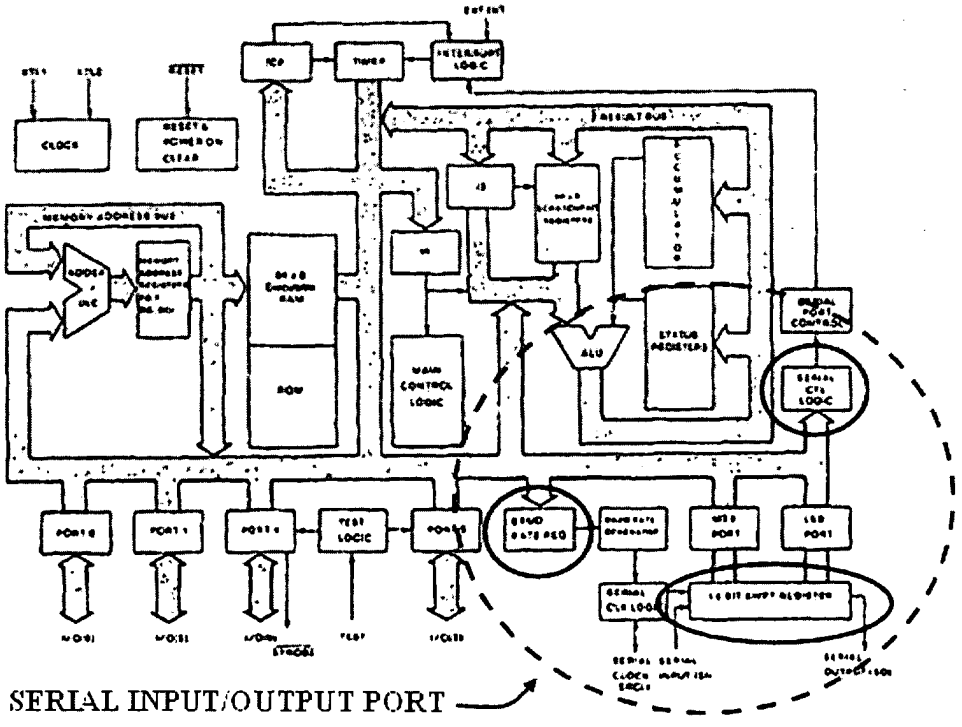
This is precisely the functionality taught by the Mostek reference. Mostek teaches a microcomputer implemented on a single chip that includes a main control logic clocked by an internal oscillator, where the frequency of the main control logic and the internal oscillator vary together due to variations in at least temperature and Vcc. The Patent Owner has asserted in correspondence with third parties that an internal oscillator indicates the presence of a ring oscillator and that a CPU and an on-chip oscillator inherently include a plurality of devices and are constructed of the same process technology. Significantly, Mostek discloses a serial input/output port that is clocked by an external clock that is independent of the variable speed oscillator.

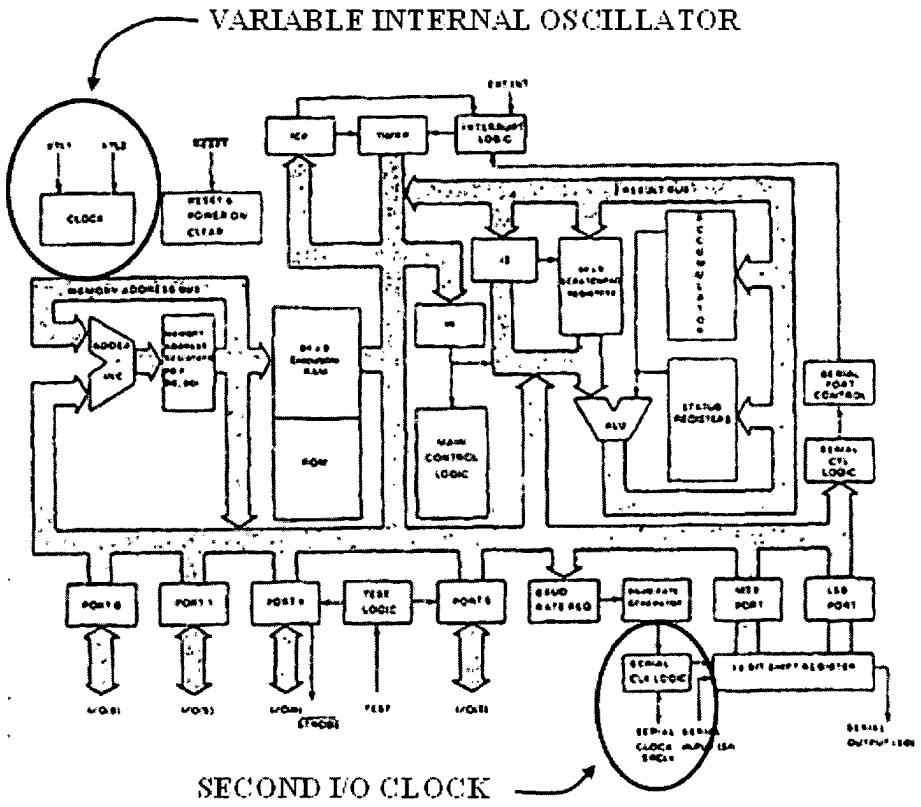
A detailed explanation of the pertinency and manner of applying the Mostek and IC Master references to claims 1-7, 9, and 10 of the '336 patent is shown in the following claim chart.

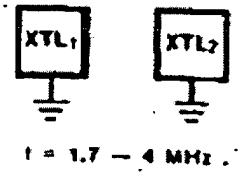
Claim Limitation Claim 1	Mostek in combination with IC Master
1. A microprocessor system, comprising a single integrated circuit	This feature is taught by Mostek, 3870 Microcomputer Data Book (Feb. 1981) ("Mostek"). The Mostek reference discloses a "*single chip microcomputer*" with features including a main control logic, executable RAM, ROM, and a serial input/output port. *(Appendix F, pages III-102 and III-103).*  *(Appendix F, Figure 1 at page III-103).*
including a central processing unit and	Mostek teaches a central processing unit, as indicated by discussion of the microcomputer's "CPU over head," "CPU instructions," "CPU Registers," and "processing . . . that occupies the CPU." *(Appendix F, pages III-102, III-104, and VI-8).* One skilled in the art would understand Mostek's Main Control Logic to disclose the recited CPU as the Main Control Logic "provides the necessary control gating signals to all circuit elements," as noted by another data book describing the 3870 family of chips *(Appendix J, page 2019).* The MK3873 described by Mostek includes architecture that is "identical to that of the rest of the devices in the 3870 family with the exception of the serial port logic." *(Appendix F, page III-102).*
an entire ring oscillator variable	Mostek teaches an "on-chip oscillator circuit which provides an internal clock." *(Appendix F, pages III-114 to III-115).* Additionally, Mostek states

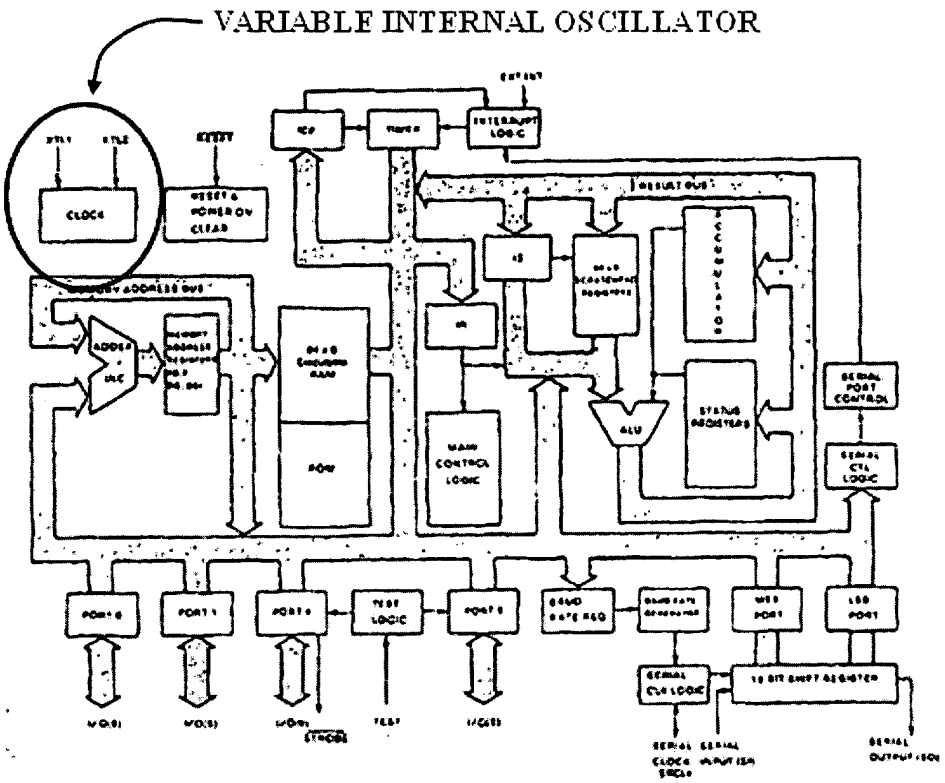
Claim Limitation	Mostek in combination with IC Master
speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	that "the architecture of the MK3873 is identical to that of the rest of the devices in the 3870 family with the exception of the serial port logic." *(Appendix F, page III-102).* One skilled in the art would know that the 3870 family of chips contain variable internal oscillators as described by the IC Master databook (IC Master 1980 (United Technical Publications) (1980)). For example, the IC Master databook states that "If timing is not critical, the F3870 will operate from its internal oscillator with no external components" *(Appendix J, page 2019) (emphasis added).* The internal oscillators of the 3870 family chips are disclosed to vary in frequency from 1.7 – 4 MHz when the chips are set to Internal Mode by grounding XTL_1 and XTL_2. *(Appendix J, Fig. 3; Pages 2024 and 2026).* **INTERNAL MODE**  f = 1.7 – 4 MHz . *(Appendix J, Fig. 4 at page 2029).* VARIABLE INTERNAL OSCILLATOR 

Claim Limitation	Mostek in combination with IC Master
	(Appendix F, Figure 1 at page III-103). The Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). The Requester notes that the functionality of prior art processors are the same in material respect to commercial processors referred to by the Patent Owner in the above mentioned communications to third parties. Therefore, such an allegation, if true with respect to today's processors, would also be true with regard to the Mostek 3870 family of processors. Accordingly, if the office accepts this premise, one skilled in the art would have understood Mostek to disclose a ring oscillator for clocking the central processing unit.
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	One skilled in the art would understand the on-chip oscillator circuit and the main control logic to include a plurality of electronic devices. With respect to the limitation of the CPU and ring oscillator being constructed of the same process technology, Mostek teaches a microprocessor system fabricated on a single chip, which would necessarily be constructed by a single process technology. Mostek describes the internal oscillator as an "on-chip oscillator circuit" indicating that the oscillator is fabricated on the same chip as the CPU and that the oscillator and CPU would therefore be constructed by the same process technology. *(Appendix F, page III-114)* It is noteworthy that the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).*
a processing frequency capability of said central processing unit and a	Mostek's microcomputer varies in frequency from 1.7-4MHz when operating from its internal oscillator due in part to a varying ambient temperature range of 0-70 °C and a varying VCC of +5V +/- 10%, as one skilled in the art would understand by referencing the IC Master data book

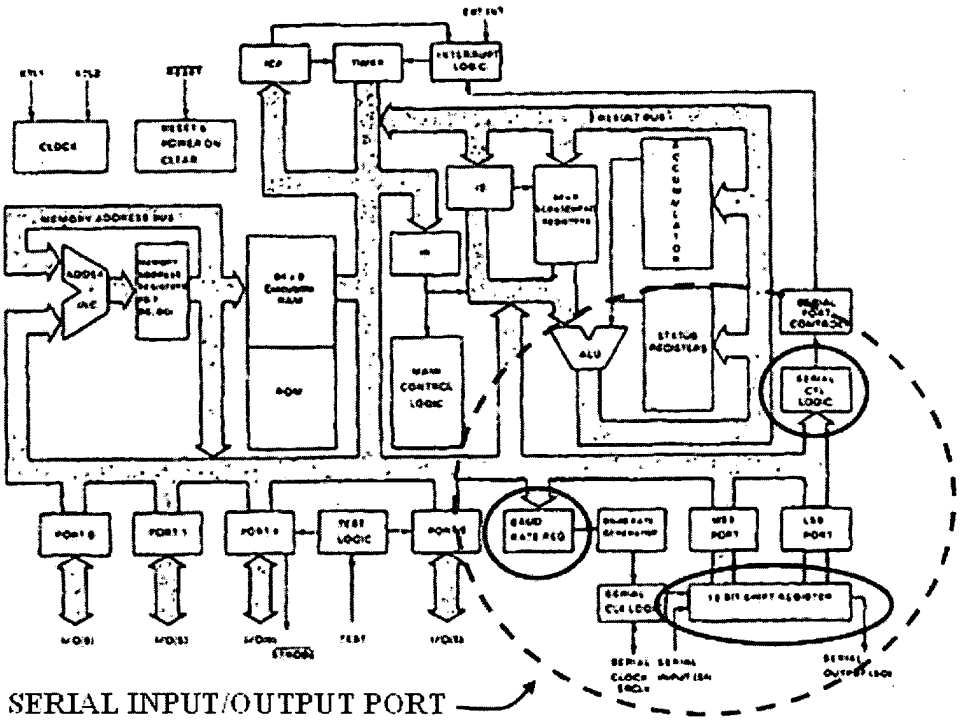
Claim Limitation	Mostek in combination with IC Master
speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	that describes the entire 3870 family. *(Appendix J, pages 2025-2026).* In any case, the Patent Owner has stated in correspondence to various third parties that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6.)*
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;	Mostek teaches a "Serial Input/Output Port [that] consists of a serial Shift Register, baud rate generator, and control logic." *(Appendix F, page III-105).* 

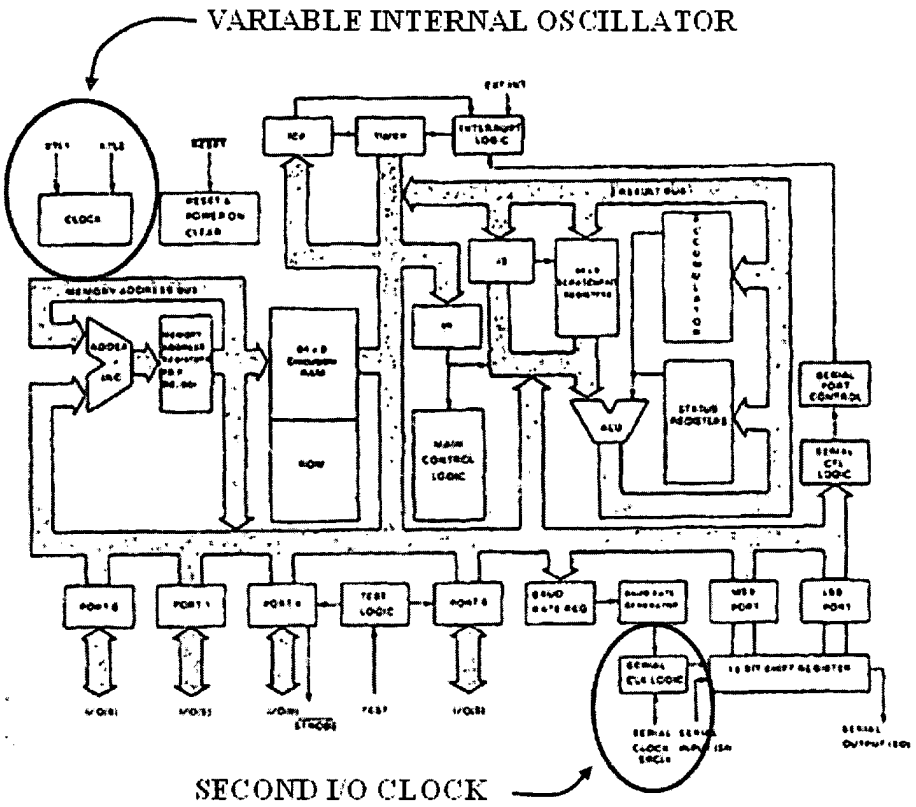
Claim Limitation	Mostek in combination with IC Master
	(Appendix F, Figure 1 at page III-103).
and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	Mostek teaches that "[d]ata is shifted into or out of the shift register at a rate determined by [an] external clock." *(Appendix F, page III-105).* The serial I/O port clocking signal "is derived from the SRCLK pulse. The SRCLK pulse . . . may be programmed as an input." *(Appendix F, page III-105).* Mostek's main control unit is clocked by the separate, independent "on-chip oscillator circuit." *(Appendix F, pages III-114 to III-115; Figure 1 at page III-103).*  *(Appendix F, Figure 1 at page III-103).*
Claim 2	
2. The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	Mostek teaches the use of a fixed frequency 3.6864MHz crystal with the second I/O clock. *(Appendix F, page III-109).* Additionally, Mostek notes that "any TTL compatible square wave input can be used to generate the clock for the serial port." *(Appendix F, page III-110).*
Claim 3	

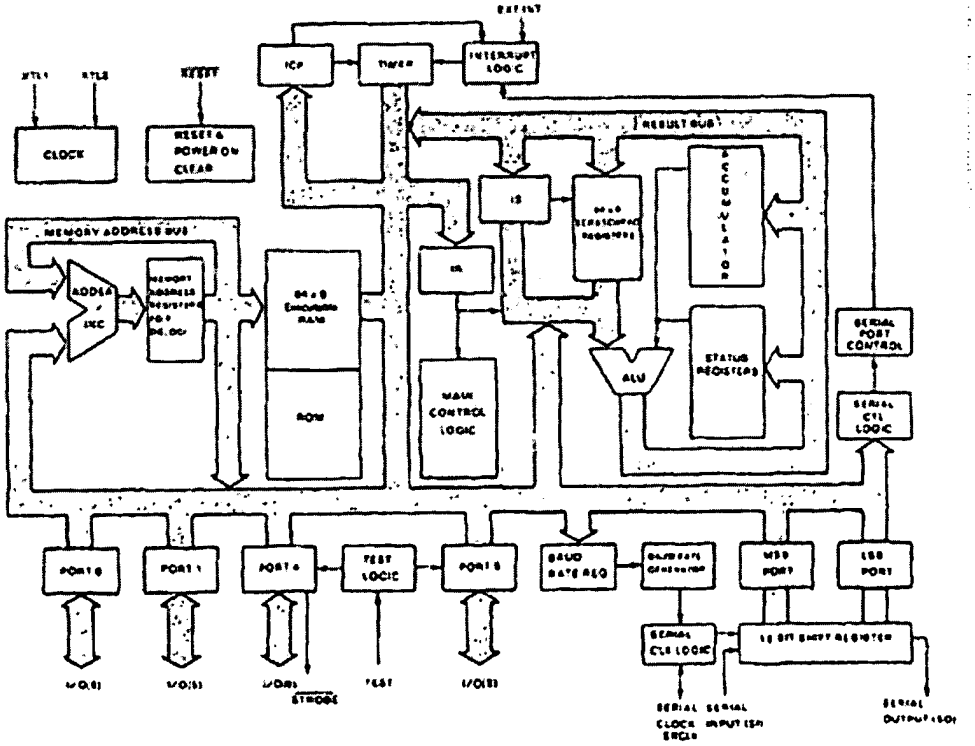
Claim Limitation	Mostek in combination with IC Master
3. In a microprocessor integrated circuit,	This feature is taught by Mostek, 3870 Microcomputer Data Book (Feb. 1981) ("Mostek"). The Mostek reference discloses a "*single chip microcomputer*" with features including a main control logic, executable RAM, ROM, and a serial input/output port. *(Appendix F, pages III-102 and III-103).*
a method for clocking the microprocessor within the integrated circuit, comprising the steps of: providing an entire ring oscillator system clock	Mostek teaches an "on-chip oscillator circuit which provides an internal clock." *(Appendix F, pages III-114 to III-115).* Additionally, Mostek states that "the architecture of the MK3873 is identical to that of the rest of the devices in the 3870 family with the exception of the serial port logic." *(Appendix F, page III-102).* One skilled in the art would know that the 3870 family of chips contain variable internal oscillators as described by the IC Master databook (IC Master 1980 (United Technical Publications) (1980)). For example, the IC Master databook states that "If timing is not critical, the F3870 will operate from its internal oscillator with no external components" *(Appendix J, page 2019) (emphasis added).* The internal oscillators of the 3870 family chips are disclosed to vary in frequency from 1.7 – 4 MHz when the chips are set to Internal Mode by grounding XTL_1 and XTL_2. *(Appendix J, Fig. 3; Pages 2024 and 2026).* INTERNAL MODE  *(Appendix J, Fig. 4 at page 2029).*

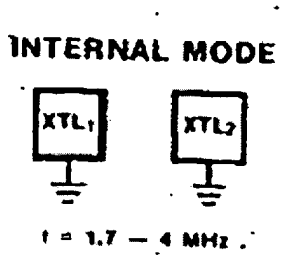
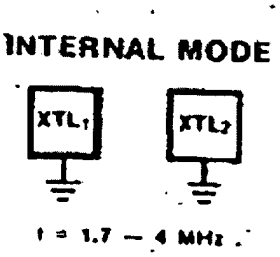
Claim Limitation	Mostek in combination with IC Master
	 *(Appendix F, Figure 1 at page III-103).* The Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). The Requester notes that the functionality of prior art processors are the same in material respect to commercial processors referred to by the Patent Owner in the above mentioned communications to third parties. Therefore, such an allegation, if true with respect to today's processors, would also be true with regard to the Mostek 3870 family of processors. Accordingly, if the office accepts this premise, one skilled in the art would have understood Mostek to disclose a ring oscillator for clocking the central processing unit.
constructed of electronic devices within the integrated circuit,	One skilled in the art would understand the on-chip oscillator circuit and the main control logic to include a plurality of electronic devices. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.

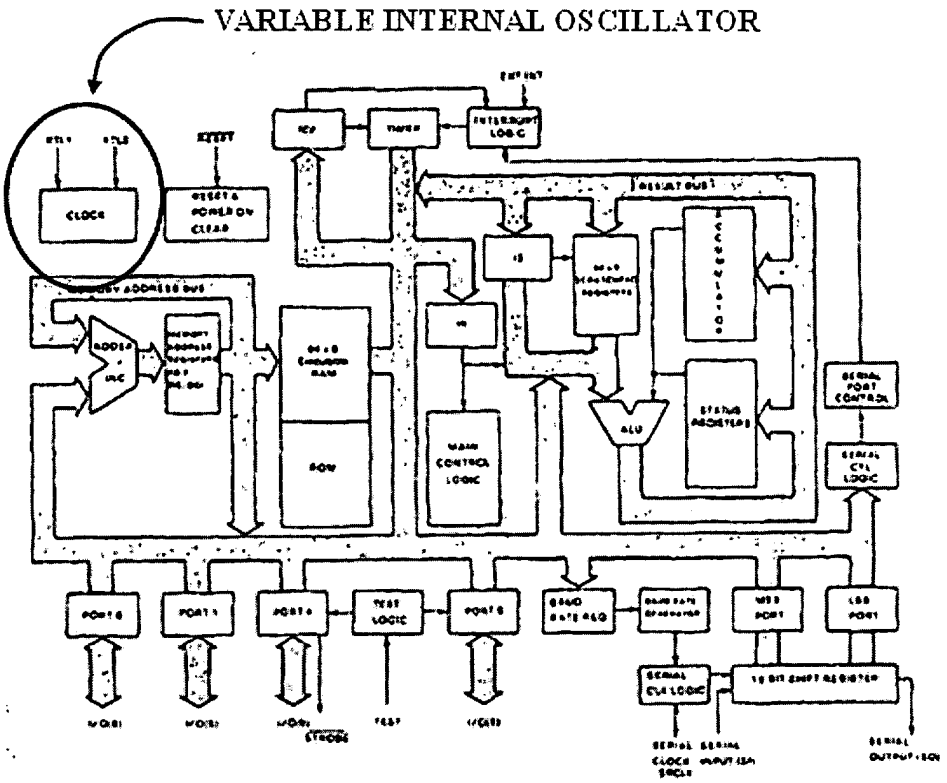
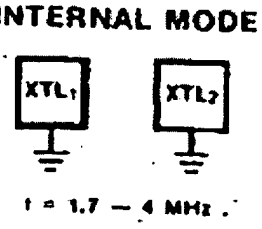
Claim Limitation	Mostek in combination with IC Master
said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;	Mostek teaches a microprocessor system fabricated on a single chip, which would necessarily be constructed by a single process technology. Mostek describes the internal oscillator as an "on-chip oscillator circuit" indicating that the oscillator is fabricated on the same chip as the CPU and that the oscillator and CPU would therefore be constructed by the same process technology. *(Appendix F, page III-114)* It is noteworthy that the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).*
using the ring oscillator system clock for clocking the microprocessor,	As explained above, Mostek teaches an "on-chip oscillator circuit which provides an internal clock" for clocking the microprocessor
said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;	Mostek's microcomputer varies in frequency from 1.7-4MHz when operating from its internal oscillator due in part to a varying ambient temperature range of 0-70 °C and a varying VCC of +5V +/- 10%, as one skilled in the art would understand by referencing the IC Master data book that describes the entire 3870 family. *(Appendix J, pages 2025-2026).* In any case, the Patent Owner has stated in correspondence to various third parties that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to

Claim Limitation	Mostek in combination with IC Master
	naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6.)*
providing an on chip input/output interface for the microprocessor integrated circuit; and	Mostek teaches a "Serial Input/Output Port [that] consists of a serial Shift Register, baud rate generator, and control logic." *(Appendix F, page III-105).*  *(Appendix F, Figure 1 at page III-103).*
clocking the input/output interface with a second clock independent of the ring oscillator system clock.	Mostek teaches that "[d]ata is shifted into or out of the shift register at a rate determined by [an] external clock." *(Appendix F, page III-105).* The serial I/O port clocking signal "is derived from the SRCLK pulse. The SRCLK pulse . . . may be programmed as an input." *(Appendix F, page III-105).* Mostek's main control unit is clocked by the separate, independent "on-chip oscillator circuit." *(Appendix F, pages III-114 to III-115; Figure 1 at page III-103).*

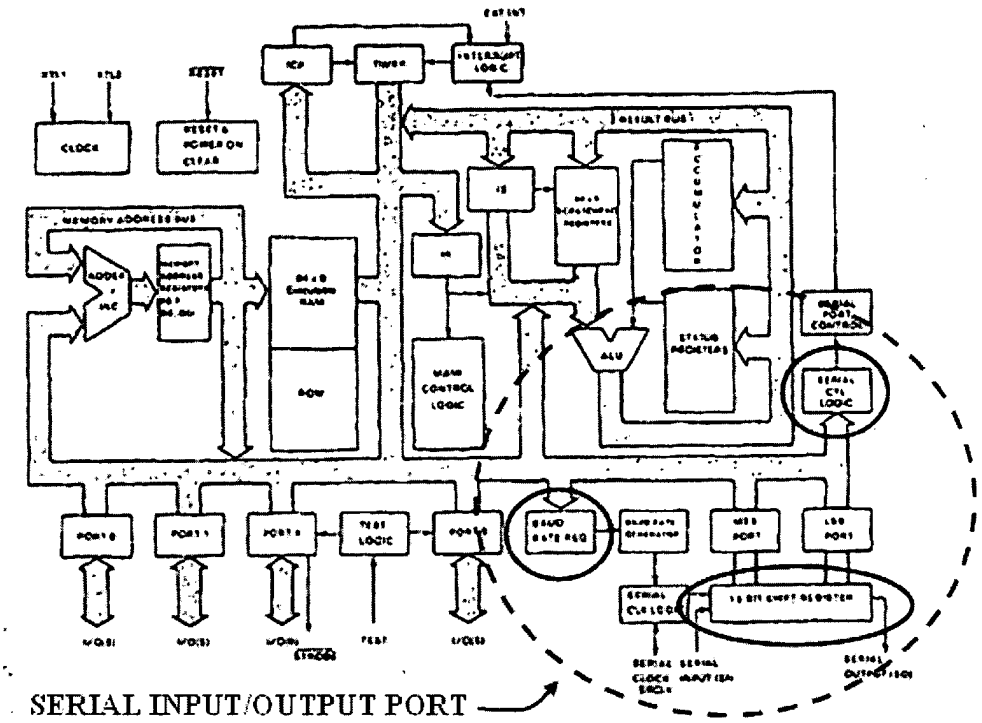
Claim Limitation	Mostek in combination with IC Master
	 *(Appendix F, Figure 1 at page III-103).*
Claim 4	
4. The method of claim 3 in which the second clock is a fixed frequency clock.	Mostek teaches the use of a fixed frequency 3.6864MHz crystal with the second I/O clock. *(Appendix F, page III-109).* Additionally, Mostek notes that "any TTL compatible square wave input can be used to generate the clock for the serial port." *(Appendix F, page III-110).*
Claim 5	
5. The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.	Mostek describes a machine "short cycle, during which time an op code fetch is performed." *(Appendix F, pages III-113).* One skilled in the art would understand that Mostek's main control logic performs the op code fetch. *(Appendix J, page 2019).* The short cycle is based on the time base frequency, which is established by the on-chip oscillator circuit. *(Appendix F, pages III-112 to III-114).*
Claim 6	

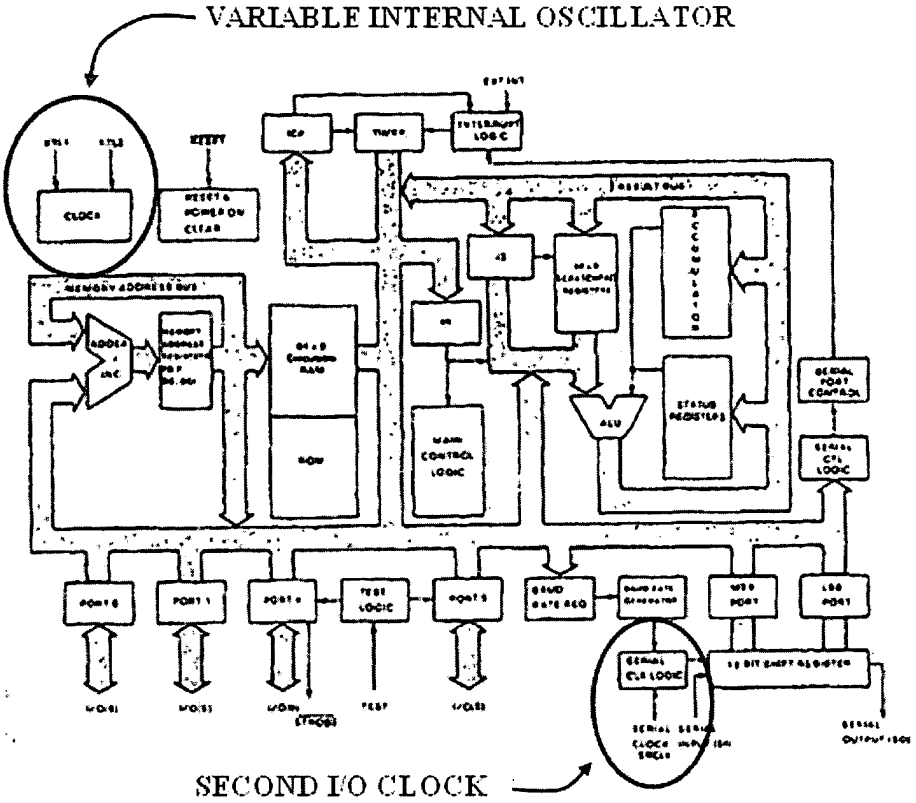
Claim Limitation	Mostek in combination with IC Master
6. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate,	This feature is taught by Mostek, 3870 Microcomputer Data Book (Feb. 1981) ("Mostek"). The Mostek reference discloses a "*single chip microcomputer*" with features including a main control logic, executable RAM, ROM, and a serial input/output port. *(Appendix F, pages III-102 and III-103).* Mostek teaches a central processing unit, as indicated by discussion of the microcomputer's "CPU over head," "CPU instructions," "CPU Registers," and "processing . . . that occupies the CPU." *(Appendix F, pages III-102, III-104, and VI-8).* One skilled in the art would understand Mostek's Main Control Logic to disclose the recited CPU as the Main Control Logic "provides the necessary control gating signals to all circuit elements," as noted by another data book describing the 3870 family of chips *(Appendix J, page 2019).* The MK3873 described by Mostek includes architecture that is "identical to that of the rest of the devices in the 3870 family with the exception of the serial port logic." *(Appendix F, page III-102).*  *(Appendix F, Figure 1 at page III-103).*
said central processing unit operating at a processing frequency	Mostek teaches an "on-chip oscillator circuit which provides an internal clock" for clocking the CPU. The internal oscillators of the 3870 family chips are disclosed to operate within a varying frequency range of 1.7 – 4 MHz when the chips are set to Internal Mode by grounding XTL_1 and XTL_2.

Claim Limitation	Mostek in combination with IC Master
and being constructed of a first plurality of electronic devices;	*(Appendix J, Fig. 3; Pages 2024 and 2026).*  *(Appendix J, Fig. 4 at page 2029).* One skilled in the art would understand the CPU to include a plurality of electronic devices.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit,	Mostek teaches an "on-chip oscillator circuit which provides an internal clock." *(Appendix F, pages III-114 to III-115).* Additionally, Mostek states that "the architecture of the MK3873 is identical to that of the rest of the devices in the 3870 family with the exception of the serial port logic." *(Appendix F, page III-102).* One skilled in the art would know that the 3870 family of chips contain variable internal oscillators as described by the IC Master databook (IC Master 1980 (United Technical Publications) (1980)). For example, the IC Master databook states that "If timing is not critical, the F3870 will operate from its internal oscillator with no external components" *(Appendix J, page 2019) (emphasis added).* The internal oscillators of the 3870 family chips are disclosed to vary in frequency from 1.7 – 4 MHz when the chips are set to Internal Mode by grounding XTL_1 and XTL_2. *(Appendix J, Fig. 3; Pages 2024 and 2026).*  *(Appendix J, Fig. 4 at page 2029).*

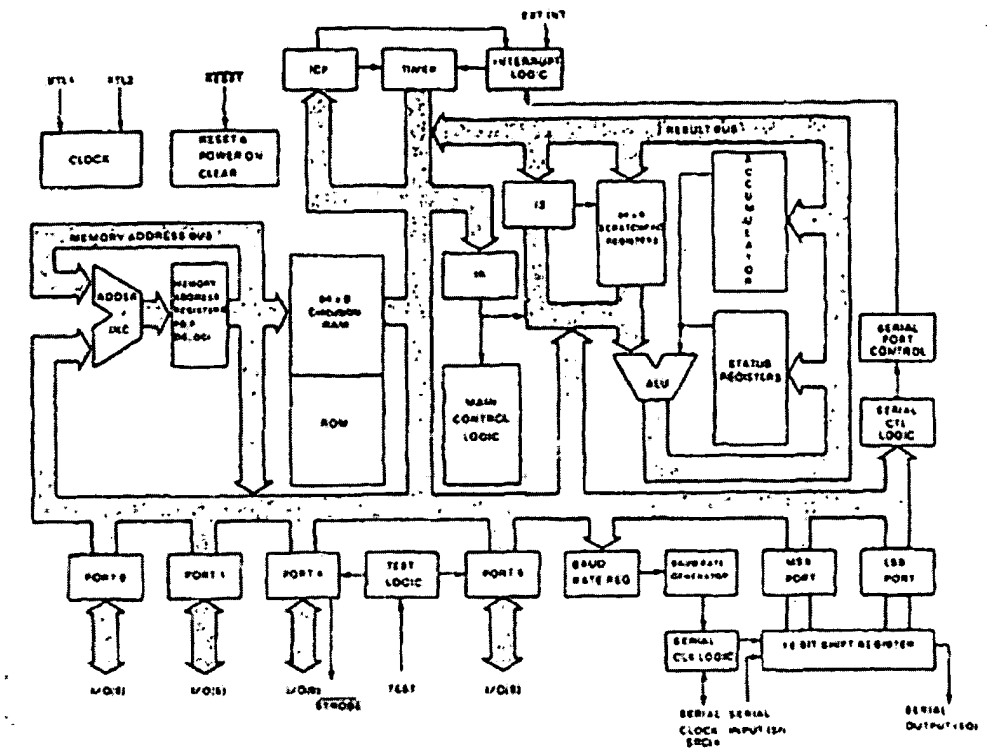
Claim Limitation	Mostek in combination with IC Master
	 *(Appendix F, Figure 1 at page III-103).*
said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,	Mostek teaches an "on-chip oscillator circuit which provides an internal clock" for clocking the CPU. The internal oscillators of the 3870 family chips are disclosed to operate within a varying frequency range of 1.7 – 4 MHz when the chips are set to Internal Mode by grounding XTL_1 and XTL_2. *(Appendix J, Fig. 3; Pages 2024 and 2026).*  *(Appendix J, Fig. 4 at page 2029).* One skilled in the art would understand the oscillator to include a plurality

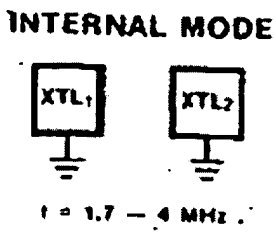
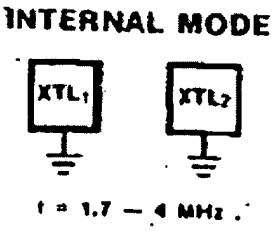
Claim Limitation	Mostek in combination with IC Master
	of electronic devices. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	Mostek teaches a microprocessor system fabricated on a single chip, which would necessarily be constructed by a single process technology. Mostek describes the internal oscillator as an "on-chip oscillator circuit" indicating that the oscillator is fabricated on the same chip as the CPU and that the oscillator and CPU would therefore be constructed by the same process technology. *(Appendix F, page III-114)* It is noteworthy that the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).*
an on-chip input/output interface, connected between said said [sic] central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	Mostek teaches a "Serial Input/Output Port [that] consists of a serial Shift Register, baud rate generator, and control logic." *(Appendix F, page III-105).* Mostek teaches that the serial port is "very flexible so that it could be used for other purposes such as an interface to . . . serial memory devices." *(Appendix F, page III-102, col. 1).*

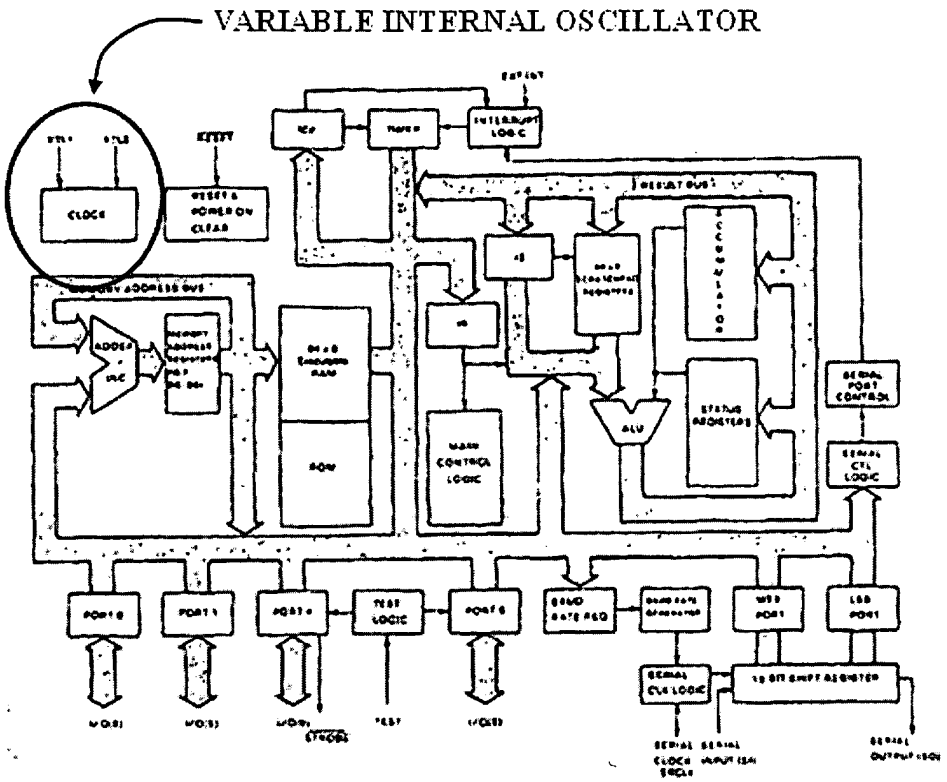
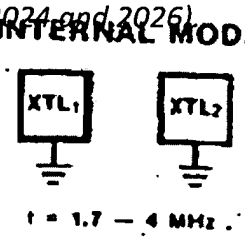
Claim Limitation	Mostek in combination with IC Master
	 *(Appendix F, Figure 1 at page III-103).*
an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	Mostek teaches that "[d]ata is shifted into or out of the shift register at a rate determined by [an] external clock." *(Appendix F, page III-105).* The serial I/O port clocking signal "is derived from the SRCLK pulse. The SRCLK pulse . . . may be programmed as an input." *(Appendix F, page III-105).* Mostek's main control unit is clocked by the separate, independent "on-chip oscillator circuit." *(Appendix F, pages III-114 to III-115; Figure 1 at page III-103).*

Claim Limitation	Mostek in combination with IC Master
	 *(Appendix F, Figure 1 at page III-103).*
Claim 7	
7. The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	Mostek's microcomputer varies in frequency from 1.7-4MHz when operating from its internal oscillator due in part to a varying ambient temperature range of 0-70 °C and a varying VCC of +5V +/- 10%, as one skilled in the art would understand by referencing the IC Master data book that describes the entire 3870 family. *(Appendix J, pages 2025-2026).* In any case, the Patent Owner has stated in correspondence to various third parties that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).*
Claim 9	

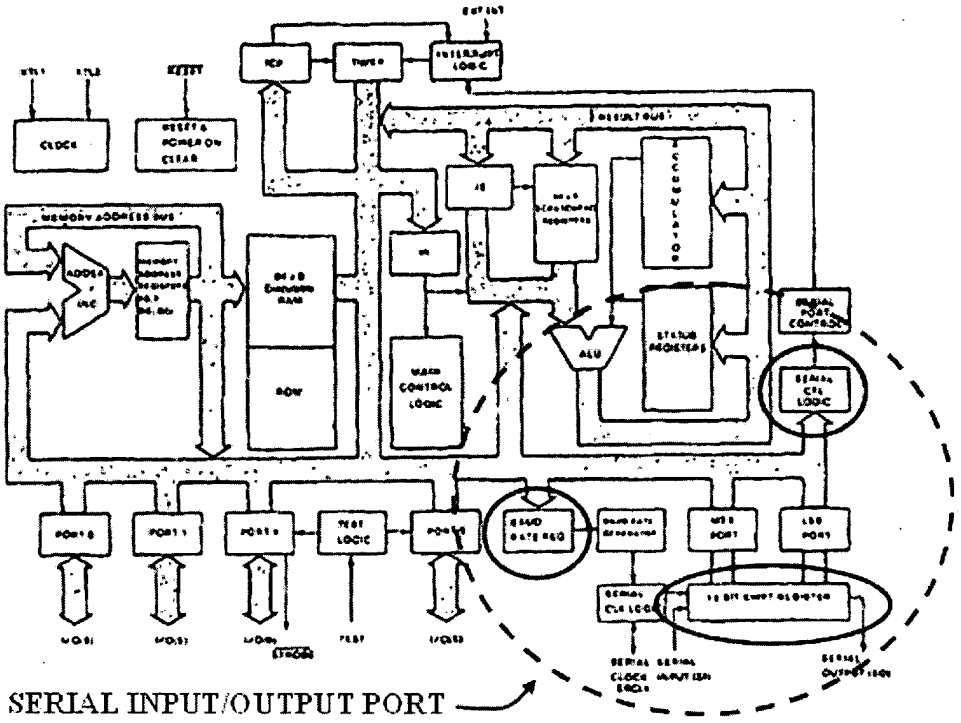
Claim Limitation	Mostek in combination with IC Master
9. The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	The Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). The Requester notes that the functionality of prior art processors are the same in material respect to commercial processors referred to by the Patent Owner in the above mentioned communications to third parties. Therefore, such an allegation, if true with respect to today's processors, would also be true with regard to the Mostek 3870 family of processors. Accordingly, if the office accepts this premise, one skilled in the art would have understood Mostek to disclose a ring oscillator for clocking the central processing unit.
Claim 10	
10. In a microprocessor system including a central processing unit,	This feature is taught by Mostek, 3870 Microcomputer Data Book (Feb. 1981) ("Mostek"). The Mostek reference discloses a "*single chip microcomputer*" with features including a main control logic, executable RAM, ROM, and a serial input/output port. *(Appendix F, pages III-102 and III-103).* Mostek teaches a central processing unit, as indicated by discussion of the microcomputer's "CPU over head," "CPU instructions," "CPU Registers," and "processing . . . that occupies the CPU." *(Appendix F, pages III-102, III-104, and VI-8).* One skilled in the art would understand Mostek's Main Control Logic to disclose the recited CPU as the Main Control Logic "provides the necessary control gating signals to all circuit elements," as noted by another data book describing the 3870 family of chips *(Appendix J, page 2019).* The MK3873 described by Mostek includes architecture that is "identical to that of the rest of the devices in the 3870 family with the exception of the serial port logic." *(Appendix F, page III-102).*

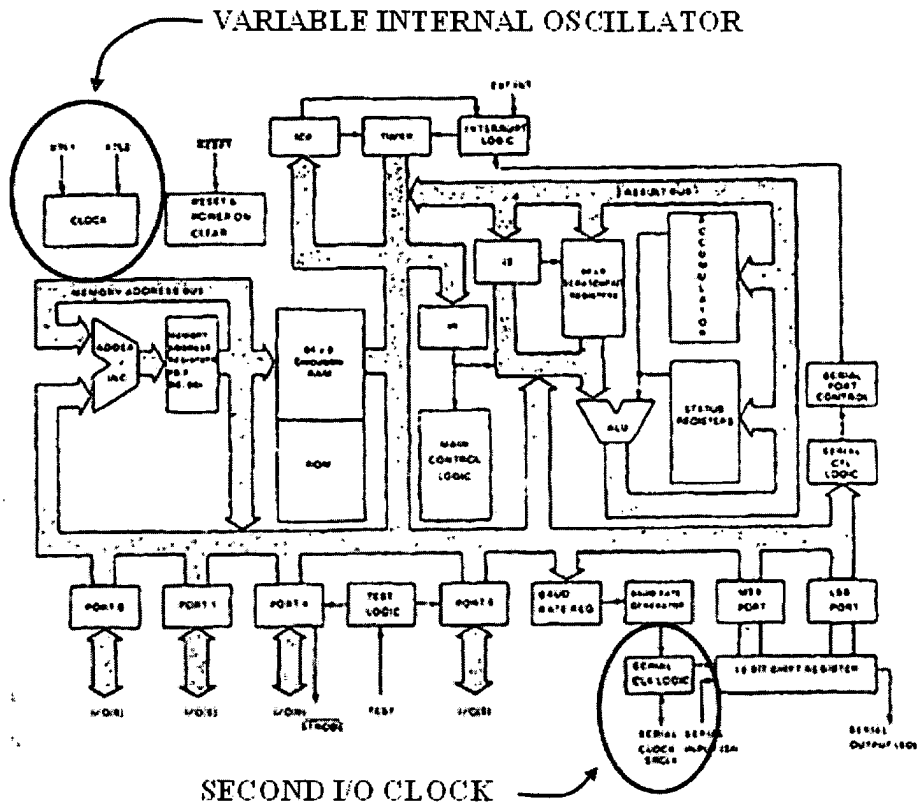
Claim Limitation	Mostek in combination with IC Master
	 *(Appendix F, Figure 1 at page III-103).*
a method for clocking said central processing unit comprising the steps of:	Mostek teaches an "on-chip oscillator circuit which provides an internal clock" for clocking the CPU.
providing said central processing unit upon an integrated circuit substrate,	The Mostek reference discloses a "*single chip microcomputer*" which includes a CPU as described above.
said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	One skilled in the art would understand the CPU to include a plurality of transistors. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of transistors. Mostek teaches an "on-chip oscillator circuit which provides an internal clock" for clocking the CPU. The internal oscillators of the 3870 family chips are disclosed to operate within a varying frequency range of 1.7 – 4

Claim Limitation	Mostek in combination with IC Master
	MHz when the chips are set to Internal Mode by grounding XTL_1 and XTL_2. *(Appendix J, Fig. 3; Pages 2024 and 2026).*  *(Appendix J, Fig. 4 at page 2029).*
providing an entire variable speed clock disposed upon said integrated circuit substrate,	Mostek teaches an "on-chip oscillator circuit which provides an internal clock." *(Appendix F, pages III-114 to III-115).* Additionally, Mostek states that "the architecture of the MK3873 is identical to that of the rest of the devices in the 3870 family with the exception of the serial port logic." *(Appendix F, page III-102).* One skilled in the art would know that the 3870 family of chips contain variable internal oscillators as described by the IC Master databook (IC Master 1980 (United Technical Publications) (1980)). For example, the IC Master databook states that "If timing is not critical, the F3870 will operate from its internal oscillator with no external components" *(Appendix J, page 2019) (emphasis added).* The internal oscillators of the 3870 family chips are disclosed to vary in frequency from 1.7 – 4 MHz when the chips are set to Internal Mode by grounding XTL_1 and XTL_2. *(Appendix J, Fig. 3; Pages 2024 and 2026).*  *(Appendix J, Fig. 4 at page 2029).*

Claim Limitation	Mostek in combination with IC Master
	 *(Appendix F, Figure 1 at page III-103).*
said variable speed clock being constructed of a second plurality of transistors;	One skilled in the art would understand the oscillator to include a plurality of transistors. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of transistors.
clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock	Mostek teaches an "on-chip oscillator circuit which provides an internal clock" for clocking the CPU. The internal oscillators of the 3870 family chips are disclosed to operate within a varying frequency range of 1.7 – 4 MHz when the chips are set to Internal Mode by grounding XTL_1 and XTL_2. *(Appendix J, Fig. 3; Pages 2024 and 2026).* 

Claim Limitation	Mostek in combination with IC Master
	(Appendix J, Fig. 4 at page 2029).
at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	The internal oscillators of the 3870 family chips are disclosed to operate within a varying frequency range of 1.7 – 4 MHz as described above. Mostek teaches a microprocessor system fabricated on a single chip, which would necessarily be constructed by a single process technology. Mostek describes the internal oscillator as an "on-chip oscillator circuit" indicating that the oscillator is fabricated on the same chip as the CPU and that the oscillator and CPU would therefore be constructed by the same process technology. *(Appendix F, page III-114)* It is noteworthy that the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).*
connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said	Mostek teaches a "Serial Input/Output Port [that] consists of a serial Shift Register, baud rate generator, and control logic." *(Appendix F, page III-105).* Mostek teaches that the serial port is "very flexible so that it could be used for other purposes such as an interface to . . . serial memory devices." *(Appendix F, page III-102, col. 1).*

Claim Limitation	Mostek in combination with IC Master
central processing unit; and	 *(Appendix F, Figure 1 at page III-103).*
clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said variable speed clock.	Mostek teaches that "[d]ata is shifted into or out of the shift register at a rate determined by [an] external clock." *(Appendix F, page III-105).* The serial I/O port clocking signal "is derived from the SRCLK pulse. The SRCLK pulse . . . may be programmed as an input." *(Appendix F, page III-105).* Mostek's main control unit is clocked by the separate, independent "on-chip oscillator circuit." *(Appendix F, pages III-114 to III-115; Figure 1 at page III-103).*

Claim Limitation	Mostek in combination with IC Master
	 *(Appendix F, Figure 1 at page III-103).*

From the foregoing chart, it can be seen that claims 1-7, 9, and 10 are rendered obvious by Mostek in combination with IC Master. Thus, claims 1-7, 9, and 10 are unpatentable as being obvious under U.S.C. § 103 by the Mostek reference in combination with the IC Master reference.

C. SNQ #2: The Mostek Reference, in Light of the IC Master and Ledzius References, Renders Obvious Claims 6, 7, and 10 of the '336 Patent

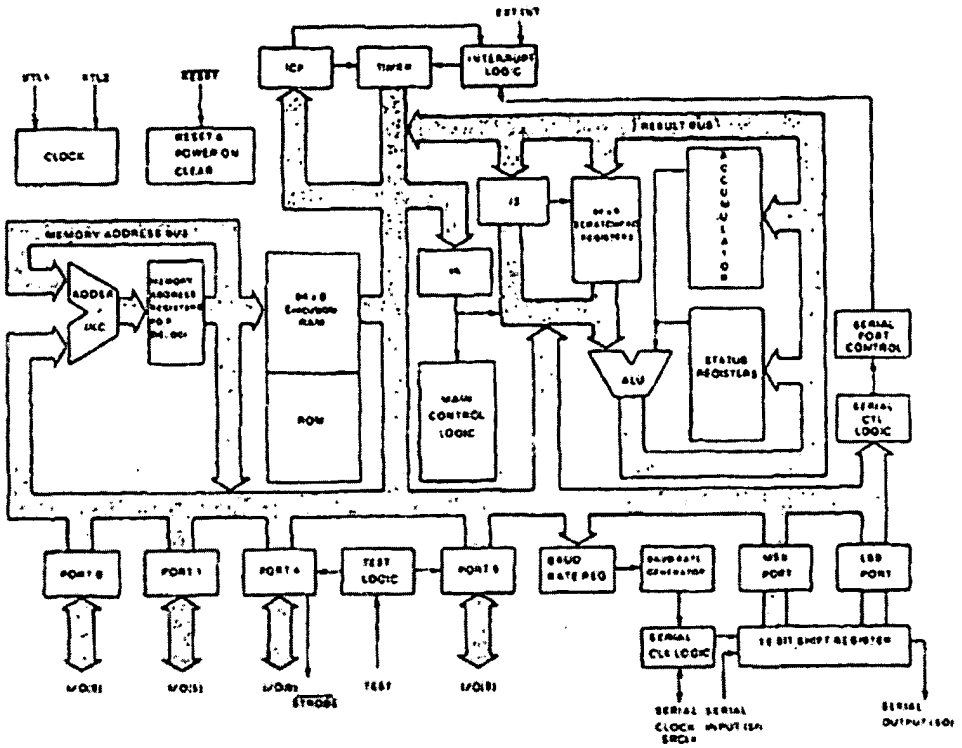
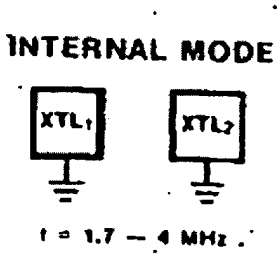
In addition to the manner of applying the Mostek and IC Master references to claims 1-7, 9, and 10 of the '336 patent outlined above, the Mostek reference, when viewed in light of the IC Master, and Ledzius references, further renders obvious several of the limitations of claims 6, 7, and 10 already taught by Mostek in combination with IC Master.

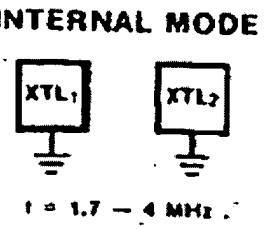
It would have been obvious to one skilled in the art to modify the teachings of the Mostek reference to use the "same batch and section of semiconductor wafer" in order to create corresponding manufacturing variations, as recited by the independent claims of the '336 patent. *(Appendix I, col. 4, lines 11-12).* This is because the Ledzius reference, which so teaches, is also an integrated circuit with a CPU and an on-chip clock. *(Appendix I, Abstract).*

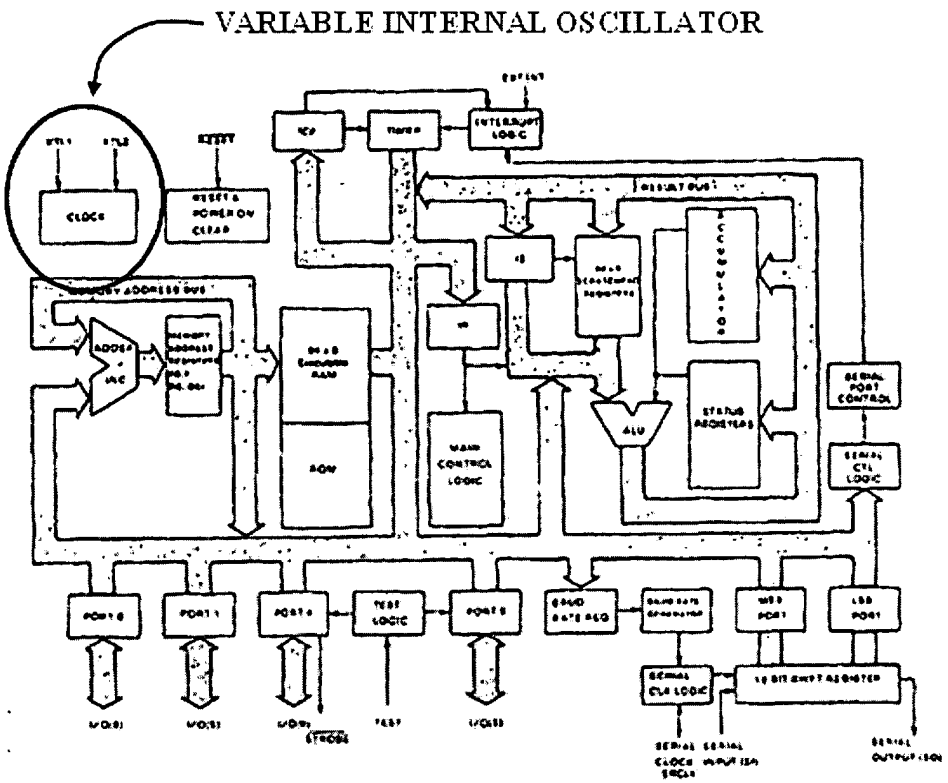
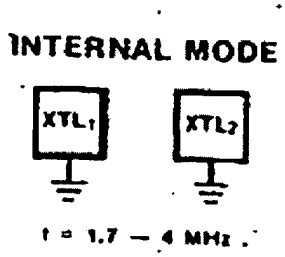
It would have been obvious to one skilled in the art to modify the teachings of the Mostek reference so that the "frequency of the clock signal produced by [the clock generator] varies to reflect process and temperature variances," as recited by the independent claims of the '336 patent. *(Appendix I, col. 4, lines 9-14).* This is because it would have been obvious to create the circuit of Mostek from the "same batch and section of semiconductor wafer" as taught by Ledzius. *(Id.)*

A detailed explanation of the pertinency and manner of applying the Mostek, IC Master, and Ledzius references to claims 6, 7, and 10 of the '336 patent is shown in the following claim chart.

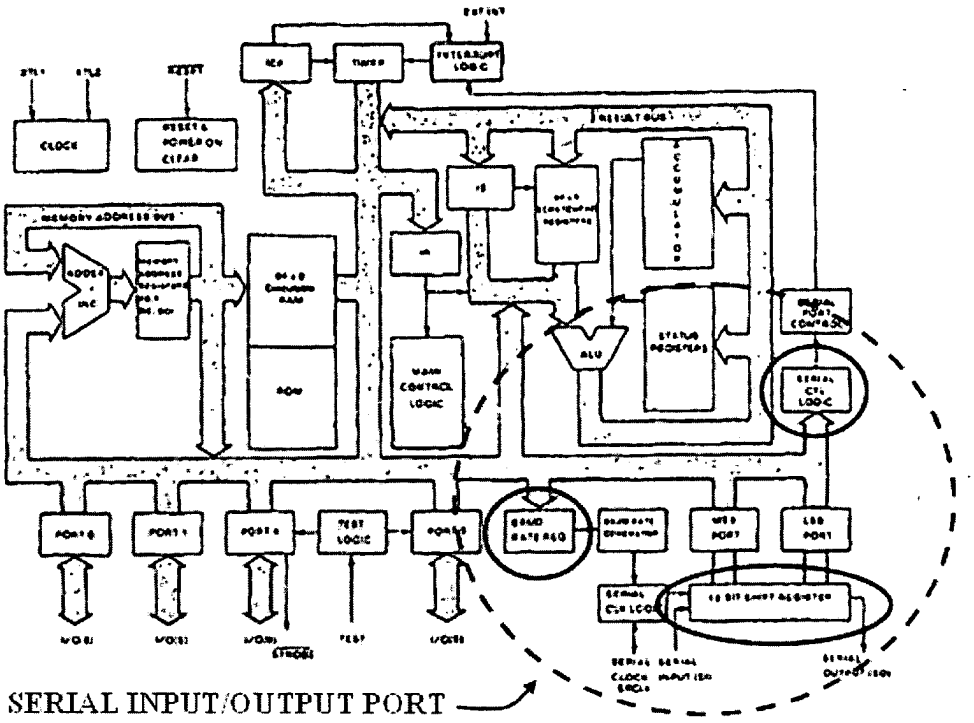
Claim Limitation Claim 6	Mostek in combination with IC Master and Ledzius
6. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate,	This feature is taught by Mostek, 3870 Microcomputer Data Book (Feb. 1981) ("Mostek"). The Mostek reference discloses a "*single chip microcomputer*" with features including a main control logic, executable RAM, ROM, and a serial input/output port. *(Appendix F, pages III-102 and III-103).* Mostek teaches a central processing unit, as indicated by discussion of the microcomputer's "CPU over head," "CPU instructions," "CPU Registers," and "processing . . . that occupies the CPU." *(Appendix F, pages III-102, III-104, and VI-8).* One skilled in the art would understand Mostek's Main Control Logic to disclose the recited CPU as the Main Control Logic "provides the necessary control gating signals to all circuit elements," as noted by another data book describing the 3870 family of chips *(Appendix J, page 2019).* The MK3873 described by Mostek includes architecture that is "identical to that of the rest of the devices in the 3870 family with the exception of the serial port logic." *(Appendix F, page III-102).*

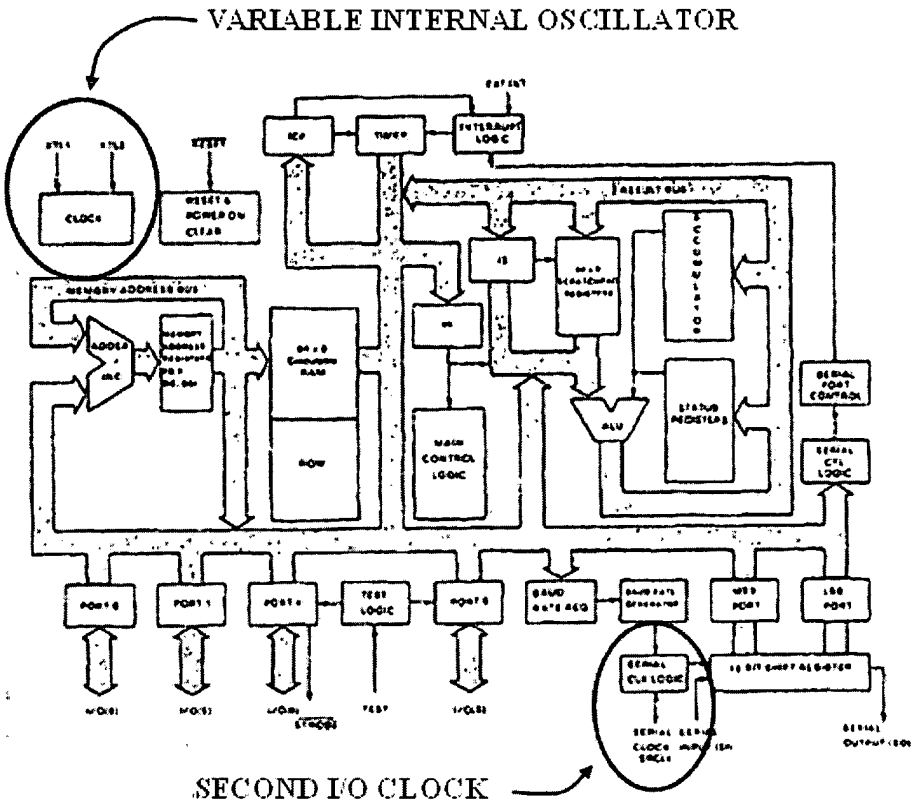
Claim Limitation	Mostek in combination with IC Master and Ledzius
	 *(Appendix F, Figure 1 at page III-103).*
said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;	Mostek teaches an "on-chip oscillator circuit which provides an internal clock" for clocking the CPU. The internal oscillators of the 3870 family chips are disclosed to operate within a varying frequency range of 1.7 – 4 MHz when the chips are set to Internal Mode by grounding XTL_1 and XTL_2. *(Appendix J, Fig. 3; Pages 2024 and 2026).*  *(Appendix J, Fig. 4 at page 2029).* One skilled in the art would understand the CPU to include a plurality of electronic devices.
an entire oscillator	Mostek teaches an "on-chip oscillator circuit which provides an internal

Claim Limitation	Mostek in combination with IC Master and Ledzius
disposed upon said integrated circuit substrate and connected to said central processing unit,	clock." *(Appendix F, pages III-114 to III-115).* Additionally, Mostek states that "the architecture of the MK3873 is identical to that of the rest of the devices in the 3870 family with the exception of the serial port logic." *(Appendix F, page III-102).* One skilled in the art would know that the 3870 family of chips contain variable internal oscillators as described by the IC Master databook (IC Master 1980 (United Technical Publications) (1980)). For example, the IC Master databook states that "If timing is not critical, the F3870 will operate from its internal oscillator with no external components" *(Appendix J, page 2019) (emphasis added).* The internal oscillators of the 3870 family chips are disclosed to vary in frequency from 1.7 – 4 MHz when the chips are set to Internal Mode by grounding XTL_1 and XTL_2. *(Appendix J, Fig. 3; Pages 2024 and 2026).*  *(Appendix J, Fig. 4 at page 2029).*

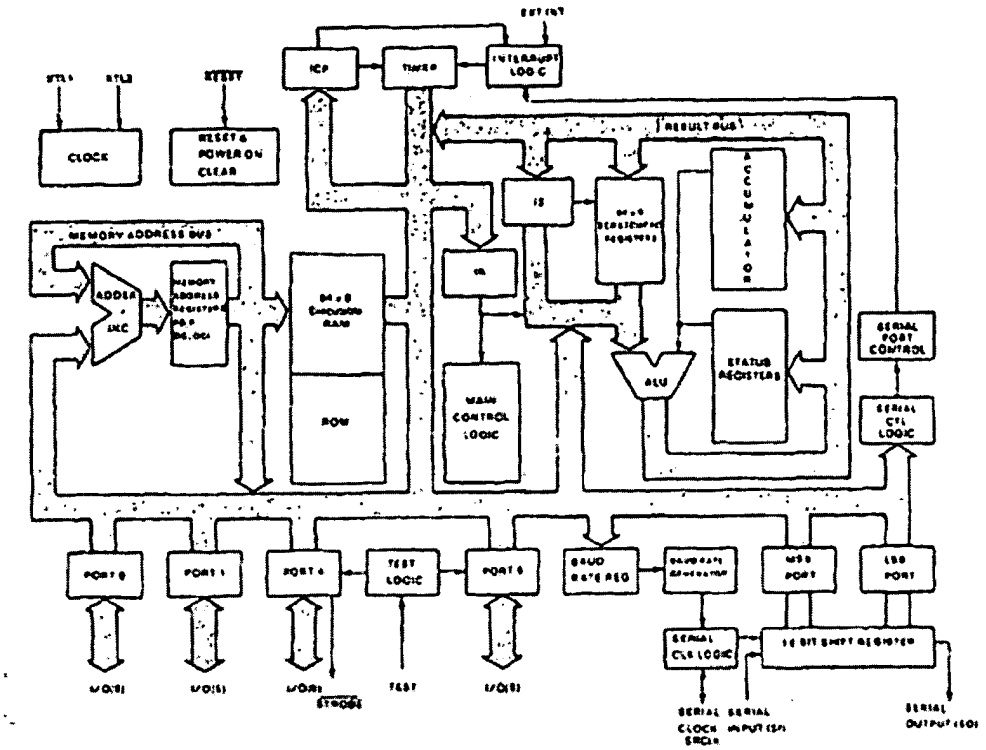
Claim Limitation	Mostek in combination with IC Master and Ledzius
	 *(Appendix F, Figure 1 at page III-103).*
said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,	Mostek teaches an "on-chip oscillator circuit which provides an internal clock" for clocking the CPU. The internal oscillators of the 3870 family chips are disclosed to operate within a varying frequency range of 1.7 – 4 MHz when the chips are set to Internal Mode by grounding XTL_1 and XTL_2. *(Appendix J, Fig. 3; Pages 2024 and 2026).*  *(Appendix J, Fig. 4 at page 2029).* One skilled in the art would understand the oscillator to include a plurality

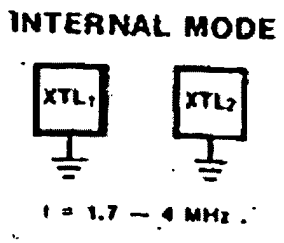
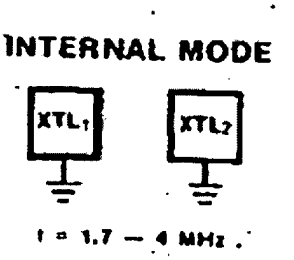
Claim Limitation	Mostek in combination with IC Master and Ledzius
	of electronic devices. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	Mostek teaches a microprocessor system fabricated on a single chip, which would necessarily be constructed by a single process technology. Mostek describes the internal oscillator as an "on-chip oscillator circuit" indicating that the oscillator is fabricated on the same chip as the CPU and that the oscillator and CPU would therefore be constructed by the same process technology. *(Appendix F, page III-114)* As noted above, the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Additionally, Requestor notes that this feature was commonplace at the time of filing, as shown by U.S. Patent No. 4,691,124 to Ledzius et al. ("Ledzius"). Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in process variations throughout the circuit. *(Appendix I, col. 4, lines 11-12).* Ledzius further teaches that the "frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances." *(Appendix I, col. 4, lines 9-11).* One skilled in the art would have found an apparent reason to combine Ledzius with Mostek, namely to produce Mostek's processor with minimal cost and defects.
an on-chip input/output interface, connected between said said [sic] central processing unit and an external memory	Mostek teaches a "Serial Input/Output Port [that] consists of a serial Shift Register, baud rate generator, and control logic." *(Appendix F, page III-105).* Mostek teaches that the serial port is "very flexible so that it could be used for other purposes such as an interface to . . . serial memory devices." *(Appendix F, page III-102, col. 1).*

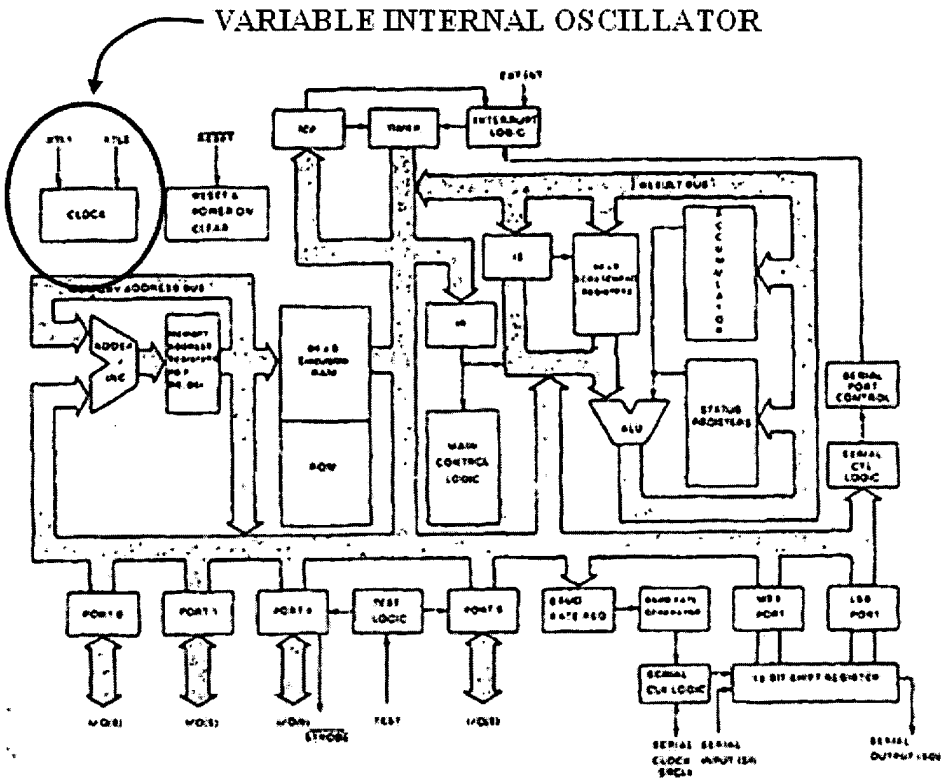
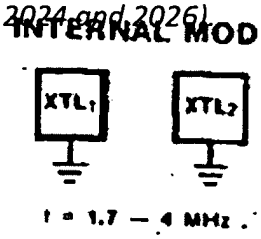
Claim Limitation	Mostek in combination with IC Master and Ledzius
bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	 *(Appendix F, Figure 1 at page III-103).*
an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	Mostek teaches that "[d]ata is shifted into or out of the shift register at a rate determined by [an] external clock." *(Appendix F, page III-105).* The serial I/O port clocking signal "is derived from the SRCLK pulse. The SRCLK pulse . . . may be programmed as an input." *(Appendix F, page III-105).* Mostek's main control unit is clocked by the separate, independent "on-chip oscillator circuit." *(Appendix F, pages III-114 to III-115; Figure 1 at page III-103).*

Claim Limitation	Mostek in combination with IC Master and Ledzius
	 *(Appendix F, Figure 1 at page III-103).*
Claim 7	
7. The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	Mostek's microcomputer varies in frequency from 1.7-4MHz when operating from its internal oscillator due in part to a varying ambient temperature range of 0-70 °C and a varying VCC of +5V +/- 10%, as one skilled in the art would understand by referencing the IC Master data book that describes the entire 3870 family. *(Appendix J, pages 2025-2026).* In any case, the Patent Owner has stated in correspondence to various third parties that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Additionally, Requestor notes that this feature was commonplace at the time of filing, as shown by U.S. Patent No. 4,691,124 to Ledzius et al.

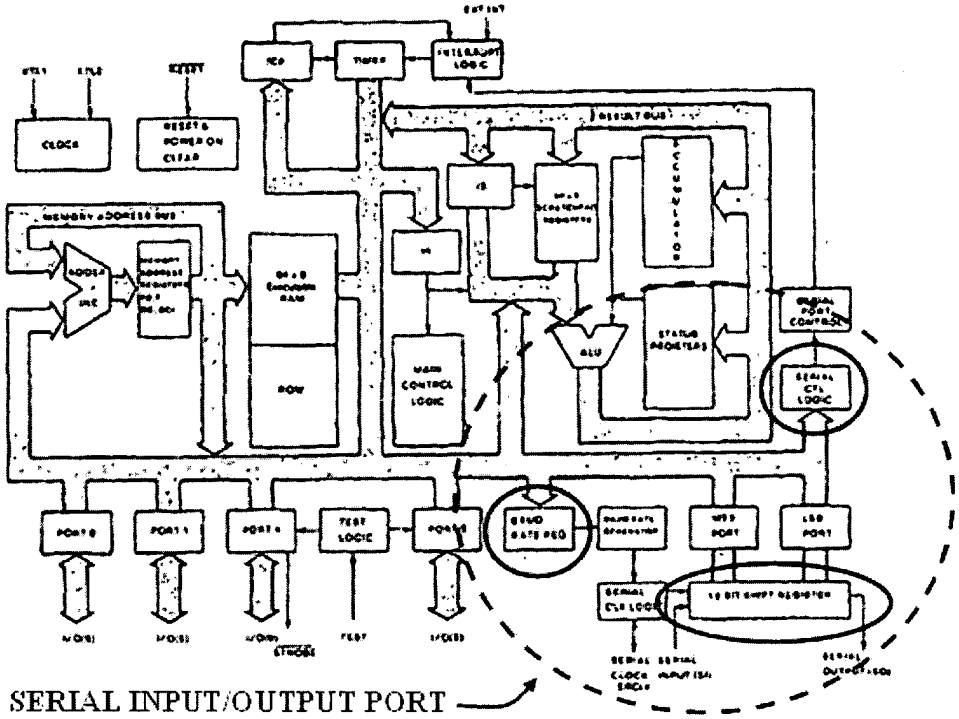
Claim Limitation	Mostek in combination with IC Master and Ledzius
	("Ledzius"). Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in process variations throughout the circuit. *(Appendix I, col. 4, lines 11-12).* Ledzius further teaches that the "frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances." *(Appendix I, col. 4, lines 9-11).* One skilled in the art would have found an apparent reason to combine Ledzius with Mostek, namely to produce Mostek's processor with minimal cost and defects.
Claim 10	
10. In a microprocessor system including a central processing unit,	This feature is taught by Mostek, 3870 Microcomputer Data Book (Feb. 1981) ("Mostek"). The Mostek reference discloses a "*single chip microcomputer*" with features including a main control logic, executable RAM, ROM, and a serial input/output port. *(Appendix F, pages III-102 and III-103).* Mostek teaches a central processing unit, as indicated by discussion of the microcomputer's "CPU over head," "CPU instructions," "CPU Registers," and "processing . . . that occupies the CPU." *(Appendix F, pages III-102, III-104, and VI-8).* One skilled in the art would understand Mostek's Main Control Logic to disclose the recited CPU as the Main Control Logic "provides the necessary control gating signals to all circuit elements," as noted by another data book describing the 3870 family of chips *(Appendix J, page 2019).* The MK3873 described by Mostek includes architecture that is "identical to that of the rest of the devices in the 3870 family with the exception of the serial port logic." *(Appendix F, page III-102).*

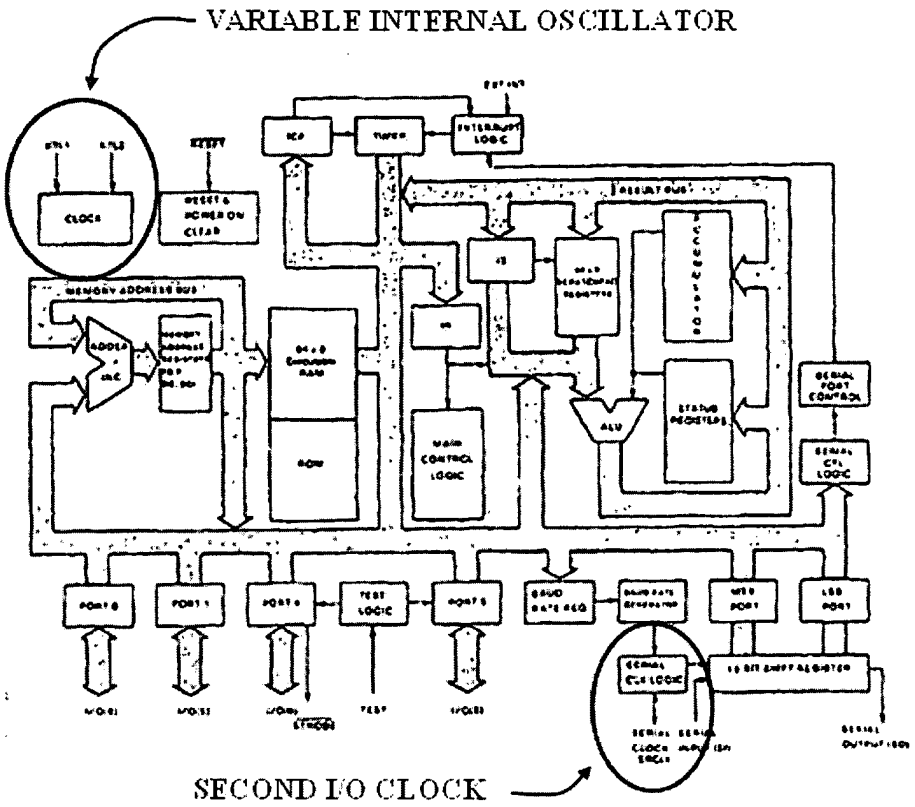
Claim Limitation	Mostek in combination with IC Master and Ledzius
	 *(Appendix F, Figure 1 at page III-103).*
a method for clocking said central processing unit comprising the steps of:	Mostek teaches an "on-chip oscillator circuit which provides an internal clock" for clocking the CPU.
providing said central processing unit upon an integrated circuit substrate,	The Mostek reference discloses a "*single chip microcomputer*" which includes a CPU as described above.
said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	One skilled in the art would understand the CPU to include a plurality of transistors. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of transistors. Mostek teaches an "on-chip oscillator circuit which provides an internal clock" for clocking the CPU. The internal oscillators of the 3870 family chips are disclosed to operate within a varying frequency range of 1.7 – 4

Claim Limitation	Mostek in combination with IC Master and Ledzius
	MHz when the chips are set to Internal Mode by grounding XTL_1 and XTL_2. *(Appendix J, Fig. 3; Pages 2024 and 2026).*  *(Appendix J, Fig. 4 at page 2029).*
providing an entire variable speed clock disposed upon said integrated circuit substrate,	Mostek teaches an "on-chip oscillator circuit which provides an internal clock." *(Appendix F, pages III-114 to III-115).* Additionally, Mostek states that "the architecture of the MK3873 is identical to that of the rest of the devices in the 3870 family with the exception of the serial port logic." *(Appendix F, page III-102).* One skilled in the art would know that the 3870 family of chips contain variable internal oscillators as described by the IC Master databook (IC Master 1980 (United Technical Publications) (1980)). For example, the IC Master databook states that "If timing is not critical, the F3870 will operate from its internal oscillator with no external components" *(Appendix J, page 2019) (emphasis added).* The internal oscillators of the 3870 family chips are disclosed to vary in frequency from 1.7 – 4 MHz when the chips are set to Internal Mode by grounding XTL_1 and XTL_2. *(Appendix J, Fig. 3; Pages 2024 and 2026).*  *(Appendix J, Fig. 4 at page 2029).*

Claim Limitation	Mostek in combination with IC Master and Ledzius
	 *(Appendix F, Figure 1 at page III-103).*
said variable speed clock being constructed of a second plurality of transistors;	One skilled in the art would understand the oscillator to include a plurality of transistors. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of transistors.
clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock	Mostek teaches an "on-chip oscillator circuit which provides an internal clock" for clocking the CPU. The internal oscillators of the 3870 family chips are disclosed to operate within a varying frequency range of 1.7 – 4 MHz when the chips are set to Internal Mode by grounding XTL_1 and XTL_2. *(Appendix J, Fig. 3; Pages 2024 and 2026).* 

Claim Limitation	Mostek in combination with IC Master and Ledzius
	(Appendix J, Fig. 4 at page 2029).
at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	The internal oscillators of the 3870 family chips are disclosed to operate within a varying frequency range of 1.7 – 4 MHz as described above. Mostek teaches a microprocessor system fabricated on a single chip, which would necessarily be constructed by a single process technology. Mostek describes the internal oscillator as an "on-chip oscillator circuit" indicating that the oscillator is fabricated on the same chip as the CPU and that the oscillator and CPU would therefore be constructed by the same process technology. *(Appendix F, page III-114)* As noted above, the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Additionally, Requestor notes that this feature was commonplace at the time of filing, as shown by U.S. Patent No. 4,691,124 to Ledzius et al. ("Ledzius"). Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in process variations throughout the circuit. *(Appendix I, col. 4, lines 11-12).* Ledzius further teaches that the "frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances." *(Appendix I, col. 4, lines 9-11).* One skilled in the art would have found an apparent reason to combine Ledzius with Mostek, namely to produce Mostek's processor with minimal cost and defects.
connecting an on chip input/output	Mostek teaches a "Serial Input/Output Port [that] consists of a serial Shift Register, baud rate generator, and control logic." *(Appendix F, page III-*

Claim Limitation	Mostek in combination with IC Master and Ledzius
interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	*105).* Mostek teaches that the serial port is "very flexible so that it could be used for other purposes such as an interface to . . . serial memory devices." *(Appendix F, page III-102, col. 1).*  *(Appendix F, Figure 1 at page III-103).*
clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said variable speed clock.	Mostek teaches that "[d]ata is shifted into or out of the shift register at a rate determined by [an] external clock." *(Appendix F, page III-105).* The serial I/O port clocking signal "is derived from the SRCLK pulse. The SRCLK pulse . . . may be programmed as an input." *(Appendix F, page III-105).* Mostek's main control unit is clocked by the separate, independent "on-chip oscillator circuit." *(Appendix F, pages III-114 to III-115; Figure 1 at page III-103).*

Claim Limitation	Mostek in combination with IC Master and Ledzius
	 *(Appendix F, Figure 1 at page III-103).*

From the foregoing chart, it can be seen that claims 6, 7, and 10 are rendered obvious by Mostek in combination with IC Master and Ledzius. Thus, claims 6, 7, and 10 are unpatentable as being obvious under U.S.C. § 103 by the Mostek reference in combination with the IC Master and Ledzius references.

D. SNQ #3: The Mostek Reference, in Light of the Kato, IC Master, and Ledzius References, Renders Obvious Claims 1-5, 8, and 9 of the '336 Patent

In addition to the manner of applying the Mostek and IC Master references to claims 1-7, 9 and 10 of the '336 patent outlined above, the Mostek reference, when viewed in light of the Kato, IC Master, and Ledzius references, further renders obvious several of the limitations already taught by Mostek in combination with IC Master.

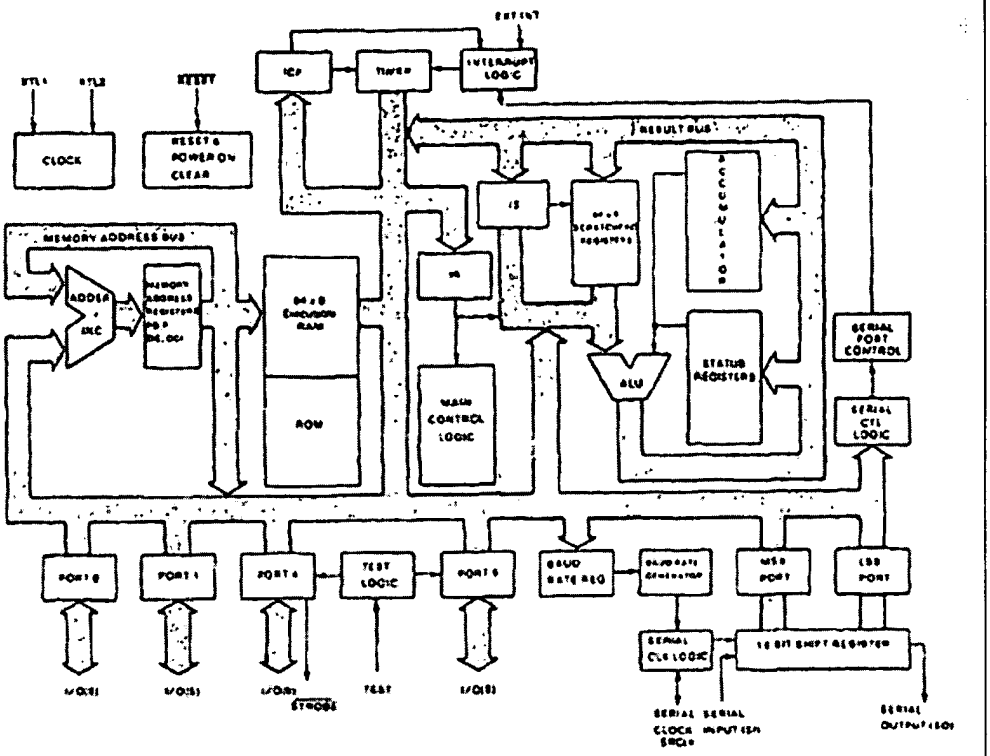
It would have been obvious for one skilled in the art to modify the teachings of Mostek so that a ring oscillator was implemented as Mostek's disclosed variable speed oscillator. This

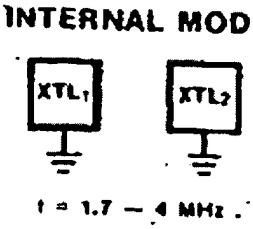
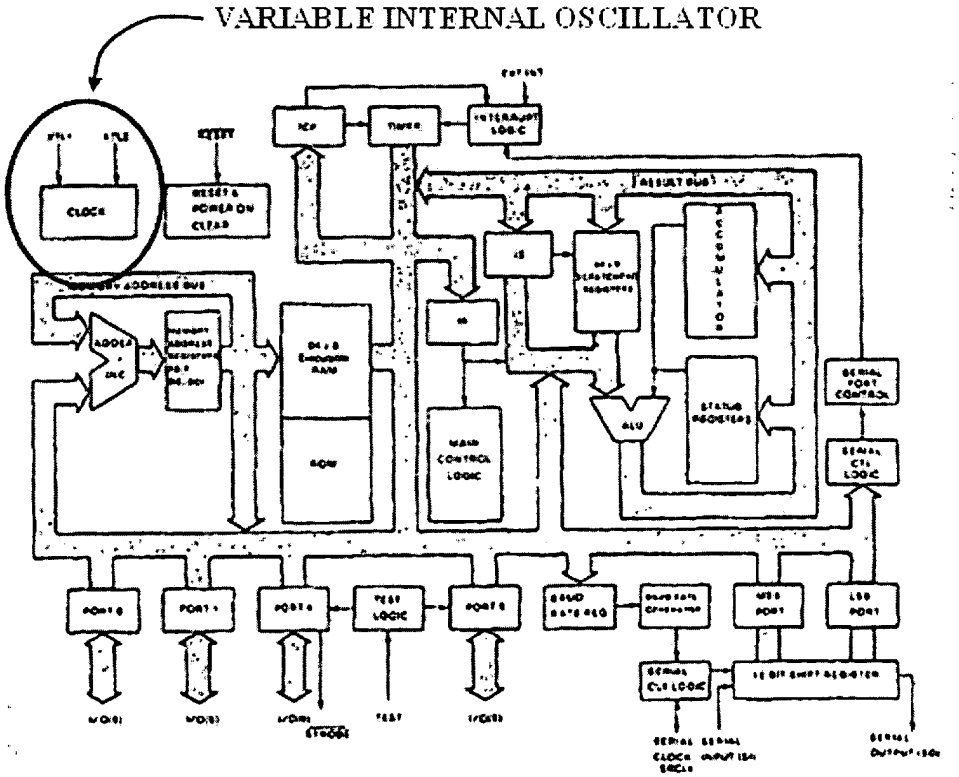
is because the Kato reference discloses a "one-chip semiconductor device" *(Appendix H, col. 1, lines 6-9)* that is clocked by a ring oscillator because the clock signal "need not have a very accurate frequency." *(Appendix H, col. 10, line 64 to col. 11, line 7).* The ring oscillator's "output frequency lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of power supply voltage." *(Appendix H, col. 11, lines 1-5).*

One skilled in the art would have seen an apparent reason to implement the variable speed oscillator disclosed in Mostek with Kato's ring oscillator, namely because the family of chips described by the Mostek data book also operate from their internal oscillators when "timing is not critical" and a ring oscillator is an obvious selection for an internal oscillator. *(Appendix J, page 2019).* One skilled in the art would realize the benefits of implementing Kato's ring oscillator as Mostek's variable oscillator to reduce power consumption during periods of lessened processing demand and to increase clock speed (and power consumption) during periods of increased processing demand. *(Appendix H, col. 11, lines 2-7).* Kato additionally teaches a second clock connected to the I/O port which operates synchronously relative to the ring oscillator as recited in claim 8 of the '336 patent. Therefore, claims 1-10 of the '336 patent are at a minimum rendered obvious by Mostek in view of Kato.

A detailed explanation of the pertinency and manner of applying the Mostek, Kato, IC Master, and Ledzius references to claims 1-5 and 8-10 of the '336 patent is shown in the following claim chart.

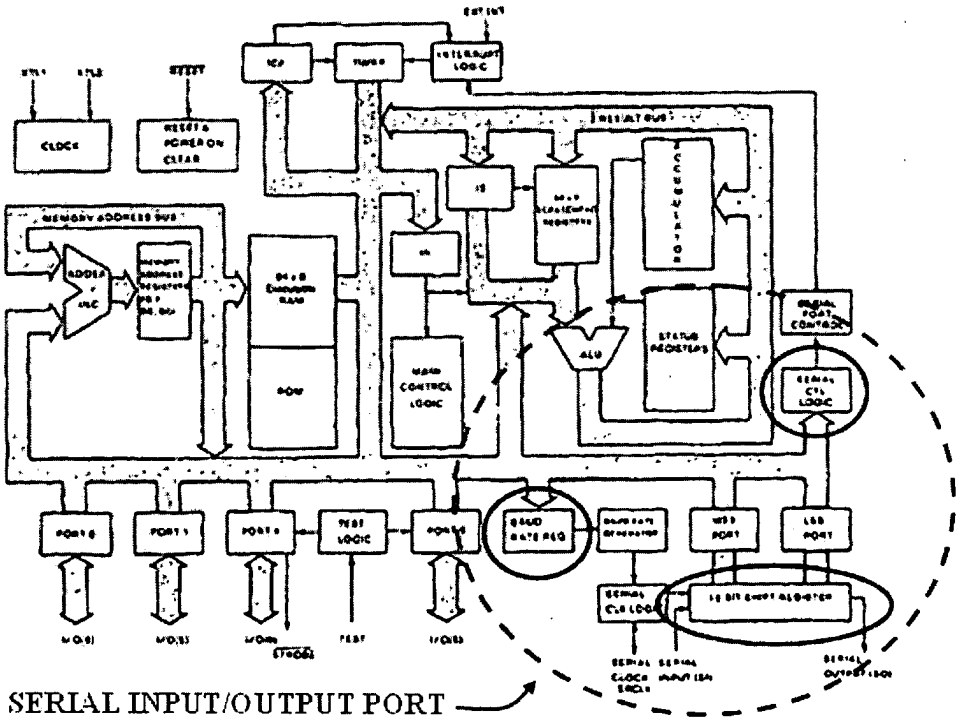
Claim Limitation Claim 1	Mostek in combination with Kato, IC Master, and Ledzius
1. A microprocessor system, comprising a single integrated circuit	This feature is taught by Mostek, 3870 Microcomputer Data Book (Feb. 1981) ("Mostek"). The Mostek reference discloses a "*single chip microcomputer*" with features including a main control logic, executable RAM, ROM, and a serial input/output port. *(Appendix F, pages III-102 and III-103).*

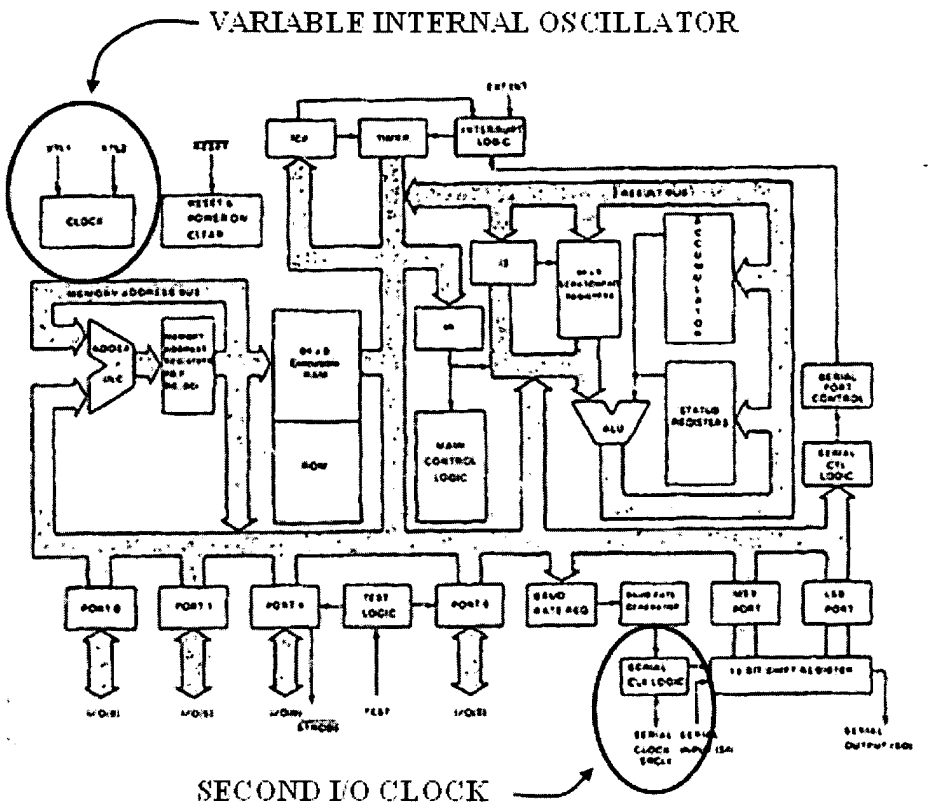
Claim Limitation	Mostek in combination with Kato, IC Master, and Ledzius
	 *(Appendix F, Figure 1 at page III-103).*
including a central processing unit and	Mostek teaches a central processing unit, as indicated by discussion of the microcomputer's "CPU over head," "CPU instructions," "CPU Registers," and "processing . . . that occupies the CPU." *(Appendix F, pages III-102, III-104, and VI-8).* One skilled in the art would understand Mostek's Main Control Logic to disclose the recited CPU as the Main Control Logic "provides the necessary control gating signals to all circuit elements," as noted by another data book describing the 3870 family of chips *(Appendix J, page 2019).* The MK3873 described by Mostek includes architecture that is "identical to that of the rest of the devices in the 3870 family with the exception of the serial port logic." *(Appendix F, page III-102).*
an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	Mostek teaches an "on-chip oscillator circuit which provides an internal clock." *(Appendix F, pages III-114 to III-115).* Additionally, Mostek states that "the architecture of the MK3873 is identical to that of the rest of the devices in the 3870 family with the exception of the serial port logic." *(Appendix F, page III-102).* One skilled in the art would know that the 3870 family of chips contain variable internal oscillators as described by the IC Master databook (IC Master 1980 (United Technical Publications) (1980)). For example, the IC Master databook states that "If timing is not critical, the F3870 will operate from its internal oscillator with no external components" *(Appendix J, page 2019) (emphasis added).* The internal

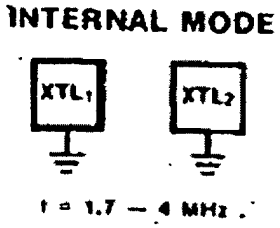
Claim Limitation	Mostek in combination with Kato, IC Master, and Ledzius
	oscillators of the 3870 family chips are disclosed to vary in frequency from 1.7 – 4 MHz when the chips are set to Internal Mode by grounding XTL_1 and XTL_2. *(Appendix J, Fig. 3; Pages 2024 and 2026).*  *(Appendix J, Fig. 4 at page 2029).*  *(Appendix F, Figure 1 at page III-103).* As explained above, the Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). Accordingly, if the office accepts this premise, one skilled in the art would have understood Mostek to disclose a

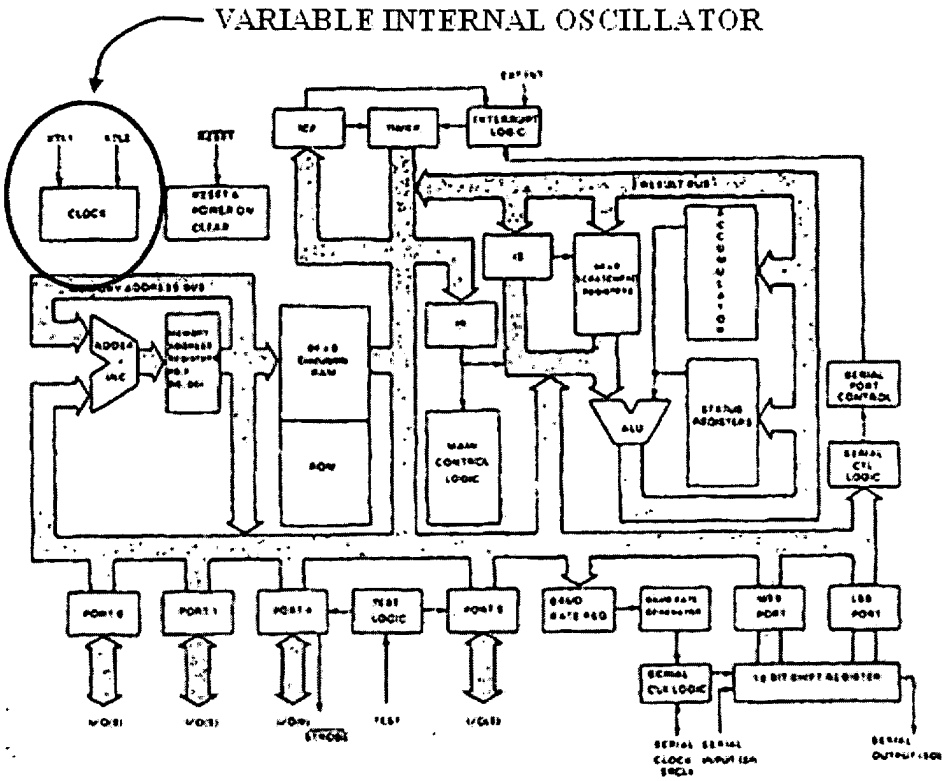
Claim Limitation	Mostek in combination with Kato, IC Master, and Ledzius
	ring oscillator for clocking the central processing unit. Additionally, the use of a ring oscillator as Mostek's variable internal oscillator is obvious in view of United States Patent No. 4,766,567 to Kato. Kato describes a ring oscillator that can be used to supply clock signals for the CPU described in Mostek. This is because Kato similarly describes a "one-chip semiconductor device" *(Appendix H, col. 1, lines 6-9)* that utilizes a ring oscillator because the device "need not have a very accurate frequency." *(Appendix H, col. 10, line 64 to col. 11, line 7).* The ring oscillator's "output frequency lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of power supply voltage." *(Appendix H, col. 11, lines 1-5).* One skilled in the art would have seen an apparent reason to implement Kato's ring oscillator as the variable speed oscillator of Mostek, namely because the family of chips described by the Mostek data book also operate from their internal oscillators when "timing is not critical" and a ring oscillator is an obvious selection for an internal oscillator. *(Appendix J, page 2019).* One skilled in the art would realize the benefits of implementing Kato's ring oscillator as Mostek's variable oscillator to reduce power consumption during periods of lessened processing demand and to increase clock speed (and power consumption) during periods of increased processing demand. *(Appendix H, col. 11, lines 2-7).*
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	One skilled in the art would understand the on-chip oscillator circuit and the main control logic to include a plurality of electronic devices. With respect to the limitation of the CPU and ring oscillator being constructed of the same process technology, Mostek teaches a microprocessor system fabricated on a single chip, which would necessarily be constructed by a single process technology. Mostek describes the internal oscillator as an "on-chip oscillator circuit" indicating that the oscillator is fabricated on the same chip as the CPU and that the oscillator and CPU would therefore be constructed by the same process technology. *(Appendix F, page III-114)* As explained above, the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit,

Claim Limitation	Mostek in combination with Kato, IC Master, and Ledzius
	vary together due to manufacturing variations." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Additionally, Requestor notes that this feature was commonplace at the time of filing, as shown by U.S. Patent No. 4,691,124 to Ledzius et al. ("Ledzius"). Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in process variations throughout the circuit. *(Appendix I, col. 4, lines 11-12).* Ledzius further teaches that the "frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances." *(Appendix I, col. 4, lines 9-11).* One skilled in the art would have found an apparent reason to combine Ledzius with Mostek, namely to produce Mostek's processor with minimal cost and defects.
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	Mostek's microcomputer varies in frequency from 1.7-4MHz when operating from its internal oscillator due in part to a varying ambient temperature range of 0-70 °C and a varying VCC of +5V +/- 10%, as one skilled in the art would understand by referencing the IC Master data book that describes the entire 3870 family. *(Appendix J, pages 2025-2026).* In any case, the Patent Owner has stated in correspondence to various third parties that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6.)* Additionally and as describe previously, one skilled in the art would see an apparent reason to implement the ring oscillator of Kato as the variable oscillator of Mostek. One skilled in the art would realize the benefits of implementing Kato's ring oscillator as Mostek's variable oscillator to reduce power consumption during periods of lessened processing demand and to increase clock speed (and power consumption) during periods of

Claim Limitation	Mostek in combination with Kato, IC Master, and Ledzius
	increased processing demand. *(Appendix H, col. 11, lines 2-7).* Additionally, Requestor notes that this feature was commonplace at the time of filing, as shown by U.S. Patent No. 4,691,124 to Ledzius et al. ("Ledzius"). Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in process variations throughout the circuit. *(Appendix I, col. 4, lines 11-12).* Ledzius further teaches that the "frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances." *(Appendix I, col. 4, lines 9-11).* One skilled in the art would have found an apparent reason to combine Ledzius with Mostek, namely to produce Mostek's processor with minimal cost and defects.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;	Mostek teaches a "Serial Input/Output Port [that] consists of a serial Shift Register, baud rate generator, and control logic." *(Appendix F, page III-105).*  *(Appendix F, Figure 1 at page III-103).*
and a second clock independent of said ring oscillator variable speed system clock	Mostek teaches that "[d]ata is shifted into or out of the shift register at a rate determined by [an] external clock." *(Appendix F, page III-105).* The serial I/O port clocking signal "is derived from the SRCLK pulse. The SRCLK pulse . . . may be programmed as an input." *(Appendix F, page III-105).*

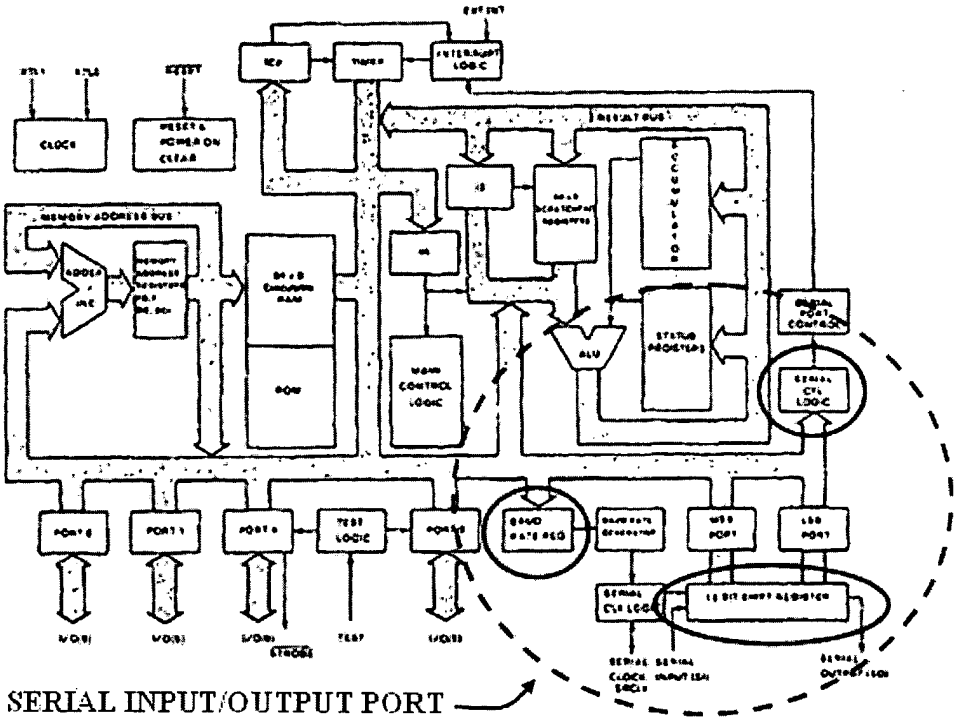
Claim Limitation	Mostek in combination with Kato, IC Master, and Ledzius
connected to said input/output interface.	Mostek's main control unit is clocked by the separate, independent "on-chip oscillator circuit." *(Appendix F, pages III-114 to III-115; Figure 1 at page III-103).*  *(Appendix F, Figure 1 at page III-103).*
Claim 2	
2. The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	Mostek teaches the use of a fixed frequency 3.6864MHz crystal with the second I/O clock. *(Appendix F, page III-109).* Additionally, Mostek notes that "any TTL compatible square wave input can be used to generate the clock for the serial port." *(Appendix F, page III-110).*
Claim 3	
3. In a microprocessor integrated circuit,	This feature is taught by Mostek, 3870 Microcomputer Data Book (Feb. 1981) ("Mostek"). The Mostek reference discloses a "*single chip microcomputer*" with features including a main control logic, executable RAM, ROM, and a serial input/output port. *(Appendix F, pages III-102 and III-103).*

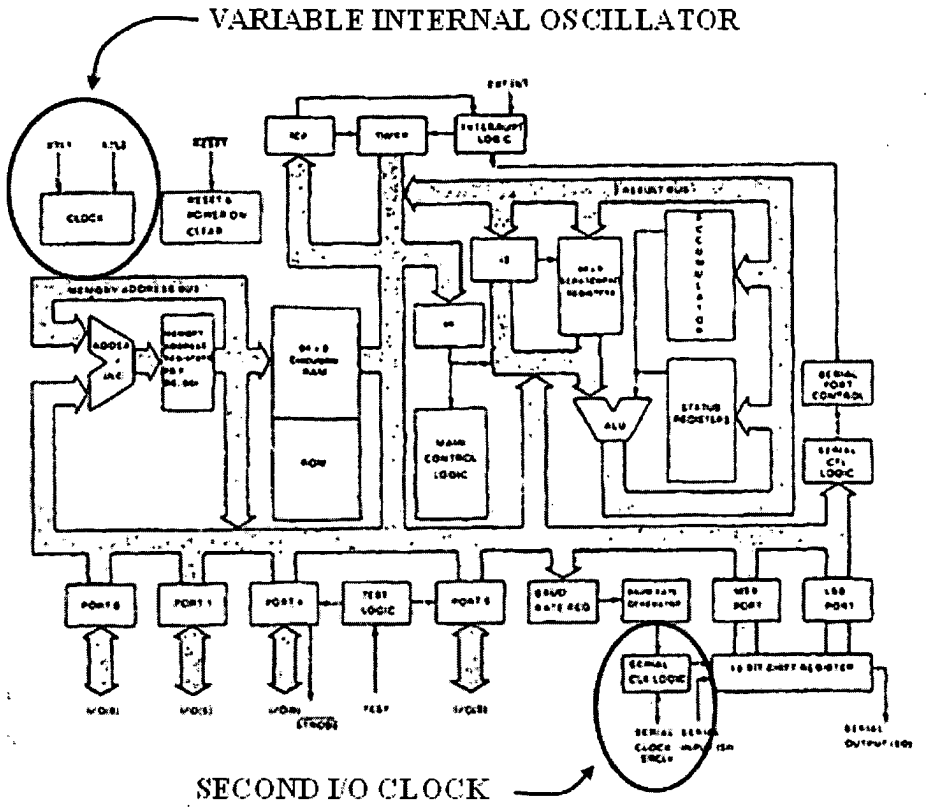
Claim Limitation	Mostek in combination with Kato, IC Master, and Ledzius
a method for clocking the microprocessor within the integrated circuit, comprising the steps of: providing an entire ring oscillator system clock	Mostek teaches an "on-chip oscillator circuit which provides an internal clock." *(Appendix F, pages III-114 to III-115).* Additionally, Mostek states that "the architecture of the MK3873 is identical to that of the rest of the devices in the 3870 family with the exception of the serial port logic." *(Appendix F, page III-102).* One skilled in the art would know that the 3870 family of chips contain variable internal oscillators as described by the IC Master databook (IC Master 1980 (United Technical Publications) (1980)). For example, the IC Master databook states that "If timing is not critical, the F3870 will operate from its internal oscillator with no external components" *(Appendix J, page 2019) (emphasis added).* The internal oscillators of the 3870 family chips are disclosed to vary in frequency from 1.7 – 4 MHz when the chips are set to Internal Mode by grounding XTL_1 and XTL_2. *(Appendix J, Fig. 3; Pages 2024 and 2026).*  *(Appendix J, Fig. 4 at page 2029).*

Claim Limitation	Mostek in combination with Kato, IC Master, and Ledzius
	 *(Appendix F, Figure 1 at page III-103).* As noted above, the Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). Accordingly, if the office accepts this premise, one skilled in the art would have understood Mostek to disclose a ring oscillator for clocking the central processing unit. In any case, the use of a ring oscillator as Mostek's variable internal oscillator is obvious in view of United States Patent No. 4,766,567 to Kato. Kato describes a ring oscillator that can be used to supply clock signals for the CPU described in Mostek. This is because Kato similarly describes a "one-chip semiconductor device" *(Appendix H, col. 1, lines 6-9)* that utilizes a ring oscillator because the device "need not have a very accurate frequency." *(Appendix H, col. 10, line 64 to col. 11, line 7).* The ring oscillator's "output frequency lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of power supply voltage." *(Appendix H, col. 11, lines 1-5).* One skilled in the art would have seen an apparent reason to implement Kato's ring oscillator as the variable

Claim Limitation	Mostek in combination with Kato, IC Master, and Ledzius
	speed oscillator of Mostek, namely because the family of chips described by the Mostek data book also operate from their internal oscillators when "timing is not critical" and a ring oscillator is an obvious selection for an internal oscillator. *(Appendix J, page 2019).* One skilled in the art would realize the benefits of implementing Kato's ring oscillator as Mostek's variable oscillator to reduce power consumption during periods of lessened processing demand and to increase clock speed (and power consumption) during periods of increased processing demand. *(Appendix H, col. 11, lines 2-7).*
constructed of electronic devices within the integrated circuit,	One skilled in the art would understand the on-chip oscillator circuit and the main control logic to include a plurality of electronic devices. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.
said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;	Mostek teaches a microprocessor system fabricated on a single chip, which would necessarily be constructed by a single process technology. Mostek describes the internal oscillator as an "on-chip oscillator circuit" indicating that the oscillator is fabricated on the same chip as the CPU and that the oscillator and CPU would therefore be constructed by the same process technology. *(Appendix F, page III-114)* As noted above, the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Additionally, Requestor notes that this feature was commonplace at the time of filing, as shown by U.S. Patent No. 4,691,124 to Ledzius et al. ("Ledzius"). Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in process variations throughout the circuit. *(Appendix I, col. 4, lines 11-12).* Ledzius further teaches that the "frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances."

Claim Limitation	Mostek in combination with Kato, IC Master, and Ledzius
	(Appendix I, col. 4, lines 9-11). One skilled in the art would have found an apparent reason to combine Ledzius with Mostek, namely to produce Mostek's processor with minimal cost and defects.
using the ring oscillator system clock for clocking the microprocessor,	As explained above, Mostek teaches an "on-chip oscillator circuit which provides an internal clock" for clocking the microprocessor
said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;	Mostek's microcomputer varies in frequency from 1.7-4MHz when operating from its internal oscillator due in part to a varying ambient temperature range of 0-70 °C and a varying VCC of +5V +/- 10%, as one skilled in the art would understand by referencing the IC Master data book that describes the entire 3870 family. *(Appendix J, pages 2025-2026).* In any case, the Patent Owner has stated in correspondence to various third parties that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6.)* Additionally and as describe previously, one skilled in the art would see an apparent reason to implement the ring oscillator of Kato as the variable oscillator of Mostek. One skilled in the art would realize the benefits of implementing Kato's ring oscillator as Mostek's variable oscillator to reduce power consumption during periods of lessened processing demand and to increase clock speed (and power consumption) during periods of increased processing demand. *(Appendix H, col. 11, lines 2-7).* Requestor further notes that this feature was commonplace at the time of filing, as shown by U.S. Patent No. 4,691,124 to Ledzius et al. ("Ledzius"). Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in process variations throughout

Claim Limitation	Mostek in combination with Kato, IC Master, and Ledzius
	the circuit. (Appendix I, col. 4, lines 11-12). Ledzius further teaches that the "frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances." (Appendix I, col. 4, lines 9-11). One skilled in the art would have found an apparent reason to combine Ledzius with Mostek, namely to produce Mostek's processor with minimal cost and defects.
providing an on chip input/output interface for the microprocessor integrated circuit; and	Mostek teaches a "Serial Input/Output Port [that] consists of a serial Shift Register, baud rate generator, and control logic." *(Appendix F, page III-105).*  *(Appendix F, Figure 1 at page III-103).*
clocking the input/output interface with a second clock independent of the ring oscillator system clock.	Mostek teaches that "[d]ata is shifted into or out of the shift register at a rate determined by [an] external clock." *(Appendix F, page III-105).* The serial I/O port clocking signal "is derived from the SRCLK pulse. The SRCLK pulse . . . may be programmed as an input." *(Appendix F, page III-105).* Mostek's main control unit is clocked by the separate, independent "on-chip oscillator circuit." *(Appendix F, pages III-114 to III-115; Figure 1 at page III-103).*

Claim Limitation	Mostek in combination with Kato, IC Master, and Ledzius
	 *(Appendix F, Figure 1 at page III-103).*
Claim 4	
4. The method of claim 3 in which the second clock is a fixed frequency clock.	Mostek teaches the use of a fixed frequency 3.6864MHz crystal with the second I/O clock. *(Appendix F, page III-109).* Additionally, Mostek notes that "any TTL compatible square wave input can be used to generate the clock for the serial port." *(Appendix F, page III-110).*
Claim 5	
5. The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.	Mostek describes a machine "short cycle, during which time an op code fetch is performed." *(Appendix F, pages III-113).* One skilled in the art would understand that Mostek's main control logic performs the op code fetch. *(Appendix J, page 2019).* The short cycle is based on the time base frequency, which is established by the on-chip oscillator circuit. *(Appendix F, pages III-112 to III-114).*

Claim Limitation Claim 8	Mostek in combination with Kato, IC Master, and Ledzius
8. The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.	As detailed in the above claim chart, claim 6 is rendered obvious by Mostek in view of IC Master and Ledzius. Mostek teaches the use of a fixed frequency 3.6864MHz crystal with the second I/O clock. *(Appendix F, page III-109).* The limitation of the I/O clock operating synchronously relative to the oscillator is taught by Kato. Kato teaches a microprocessor system having two clock. The first clock generator clocks the CPU and the second clock generator is connected to the I/O port. *(Appendix H, col. 4, lines 37-42 and FIG. 4)* Kato teaches that the first and second clock generators operate synchronously: "second clock generator 15 produces two clock signals ϕa and ϕb... Signals ϕa and ϕb are produced in synchronism with the signal from first clock generator 14." *(Appendix H, col. 4, lines 56-60)* As explained above, one skilled in the art would have found an apparent reason to combine the teachings of Kato and Mostek, namely to provide Mostek with a ring oscillator to reduce power consumption during periods of lessened processing demand and to increase clock speed (and power consumption) during periods of increased processing demand. *(Appendix H, col. 11, lines 2-7).*
Claim 9	
9. The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	As detailed in the above claim chart, claim 6 is rendered obvious by Mostek in view of IC Master and Ledzius. The Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). The Requester notes that the functionality of prior art processors are the same in material respect to commercial processors referred to by the Patent Owner in the above mentioned communications to third parties. Therefore, such an allegation, if true with respect to today's processors, would also be true with regard to the Mostek 3870 family of processors. Accordingly, if the office accepts this premise, one skilled in the art would have understood Mostek to disclose a ring oscillator for clocking the central processing unit. Alternatively, the use of a ring oscillator as Mostek's variable internal oscillator is obvious in view of United States Patent No. 4,766,567 to Kato. Kato describes a ring oscillator that can be used to supply clock signals for

Claim Limitation	Mostek in combination with Kato, IC Master, and Ledzius
	the CPU described in Mostek. This is because Kato similarly describes a "one-chip semiconductor device" *(Appendix H, col. 1, lines 6-9)* that utilizes a ring oscillator because the device "need not have a very accurate frequency." *(Appendix H, col. 10, line 64 to col. 11, line 7).* The ring oscillator's "output frequency lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of power supply voltage." *(Appendix H, col. 11, lines 1-5).* One skilled in the art would have seen an apparent reason to implement Kato's ring oscillator as the variable speed oscillator of Mostek, namely because the family of chips described by the Mostek data book also operate from their internal oscillators when "timing is not critical" and a ring oscillator is an obvious selection for an internal oscillator. *(Appendix J, page 2019).* One skilled in the art would realize the benefits of implementing Kato's ring oscillator as Mostek's variable oscillator to reduce power consumption during periods of lessened processing demand and to increase clock speed (and power consumption) during periods of increased processing demand. *(Appendix H, col. 11, lines 2-7).*

From the foregoing chart, it can be seen that claims 1-10 are rendered obvious by Mostek in combination with the IC Master, Kato, and Ledzius references. Thus, claims 1-10 are unpatentable as being obvious under U.S.C. § 103 by the Mostek reference in combination with the IC Master, Kato, and Ledzius references.

E. The Mostek Reference, in Light of the IC Master, Kato, and Ledzius References, Renders Obvious the Newly Introduced Claims of the '336 Patent

The Mostek reference, in light of the IC Master, Kato, and Ledzius references, renders obvious new claims added during the patent's ongoing merged reexamination. The Patent Owner added claims 11-20 which parallel respective original claims 1-10 except that they further include a limitation to "more clearly set forth the meaning of 'independent.'" *(Appendix C, Amendment, Sept. 8, 2008, original page 11).* The additional limitations append the parallel independent claims and recite: "thereby enabling decoupling a speed of said central processing unit from a speed of said input/output interface." *(Id.).*

The serial I/O port taught by Mostek is optionally clocked by an "external clock" that is distinct and decoupled in speed from the internal oscillator that provides the clock signal to the rest of the circuit. *(Appendix F, pages III-102 and III-105).* Accordingly, the input/output port generates an "end-of-word interrupt" in order to notify the CPU that a word has been received. *(Appendix F, pages III-105 and III-109).*

X. THE DOZIER REFERENCE ANTICIPATES OR, IN LIGHT OF THE MOSTEK, IC MASTER, KATO, AND LEDZIUS REFERENCES, RENDERS OBVIOUS CLAIMS 1-10 OF THE '336 PATENT

The prior art references provided in this request raise substantial new questions of patentability as to claims 1-10 of the '336 patent. Specifically, all claims are anticipated by the Dozier reference and are additionally rendered obvious over Dozier in light of the Mostek, IC Master, Kato, and Ledzius references.

A. Summary of the Teachings of the Dozier Reference

The Dozier reference teaches a microprocessor that is implemented on a single semiconductor chip, contains a main control logic that is clocked by an internal oscillator, and has input/output ports. Specifically, the reference discloses a "microprogrammed computer 10 which may be implemented by MOS/LSI techniques and which may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-63).* The reference discloses a preferred embodiment, in which "[t]he clock generator 38 includes an internal oscillator which is activated when both the XTL 1 and XTL 2 pins are grounded." *(Appendix E, col. 5, lines 24-26).* The clock generator produces several system clocks, one of which, the ΦC (the main cycle clock), "is the cycle clock for the computer system 10." *(Appendix E, col. 5, lines 9-14 and 5, lines 27-28).* The "main control logic 26" is a "principle functional section[] of the microcomputer 10." *(Appendix E, col. 2, lines 63-68).* Within these subsystems "are major buses and major logic elements." *(Appendix E, col. 18, lines 4-8).*

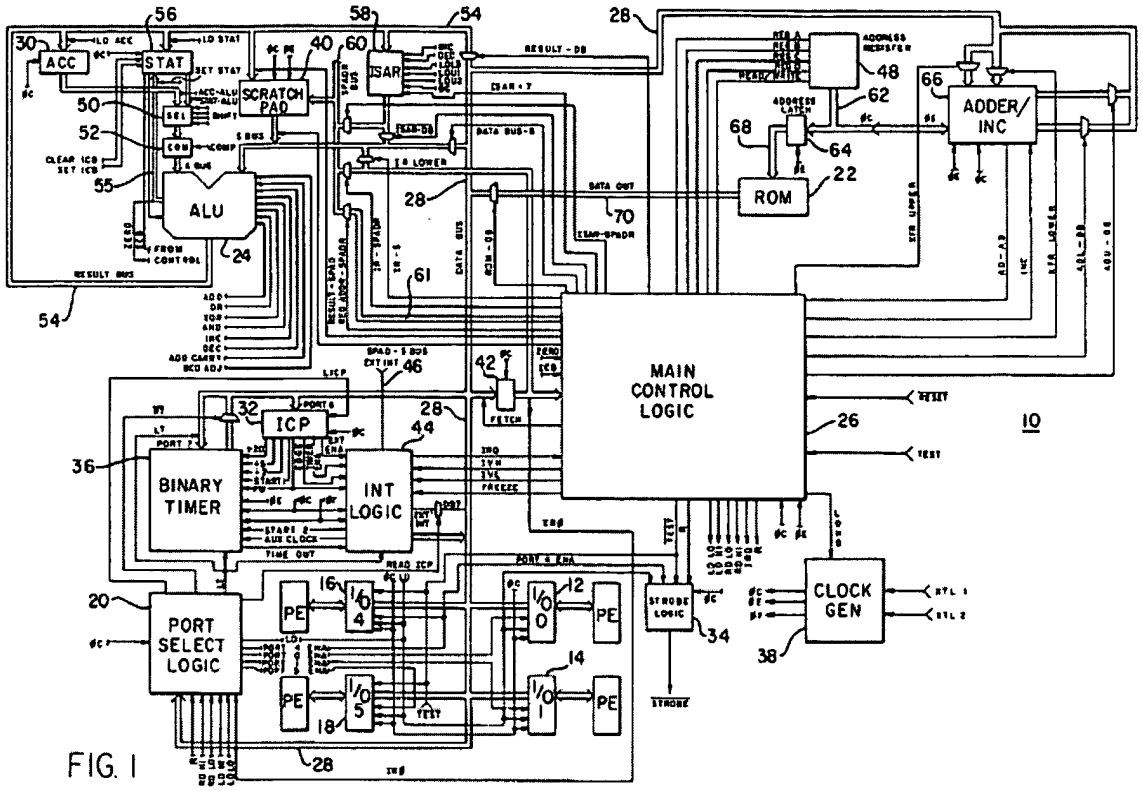


FIG. 1

(Appendix E, Figure 1).

The microprogrammed computer 10 further discloses I/O ports 12, 14, 16, and 18 – referred to as ports 0, 1, 4, and 5. *(Appendix E, col. 3, lines 14-19).* Dozier teaches a test mode, whereby information on one of the ports is immediately fed into the data bus. Specifically, in test mode "port 5 will take the information existing on its pins and drive it into the internal data bus [which] permits port 5 to be a dedicated input to the internal data bus." *(Appendix E, col. 3, lines 62-66).* Conversely, in test mode "the I/O port 4 logic block will take the data from the data bus and supply it directly to its output pins at all times. This operation is <u>not synchronized</u> with the ΦC clock." *(Appendix E, col. 3, lines 54-57) (emphasis added).*

B. SNQ #4: The Dozier Reference Anticipates Claims 1-10 of the '336 Patent

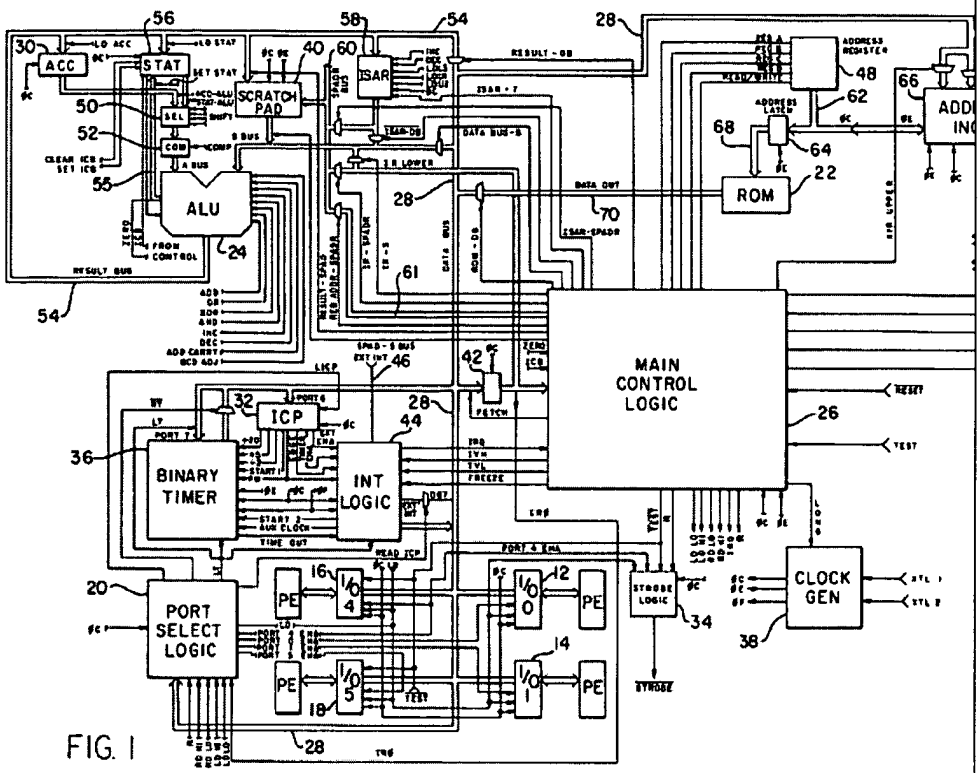
The '336 patent claims the same functionality described above in connection with the Dozier reference. The patent claims a microprocessor system comprising a single integrated

circuit that includes a ring oscillator and a central processing unit (CPU), where the ring oscillator clocks the CPU. *(Appendix A, Claim 1).* The claimed ring oscillator and CPU include a plurality of electronic devices that are constructed of the same process technology so that the frequency of the central processing unit and the speed of the ring oscillator vary together. *(Appendix A, Claim 1).* The claimed integrated circuit also includes an on-chip input/output interface, to which a second clock independent of the ring oscillator is connected. *(Appendix A, Claim 1).*

This is precisely the functionality taught by the Dozier reference. Dozier teaches a microcomputer implemented on a single chip that includes a main control logic clocked by an internal oscillator. Within these subsystems "are major buses and major logic elements." The Patent Owner has asserted in correspondence with third parties that an internal oscillator indicates the presence of a ring oscillator and that a CPU and an oscillator on the same chip are constructed of the same process technology. Further, Dozier teaches a test mode, whereby information on the ports is immediately fed into and out of the data bus, a form of serial communication which, according to the Patent Owner, satisfies the limitation of a second clock signal.

A detailed explanation of the pertinency and manner of applying the Dozier reference to claims 1-10 of the '336 patent is shown in the following claim chart.

Claim Limitation	Teaching of the Dozier Reference
1. A microprocessor system, comprising a single integrated circuit	The Dozier reference (US Patent No. 4,348,743) teaches a "microprogrammed computer 10 which may be implemented by MOS/LSI techniques and which may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-63).*
including a central processing unit and	Dozier teaches a "main control logic unit" that "directs the operations of the entire computer." *(Appendix E, col. 1, lines 46-64; 18, lines 1-14).* This main control logic is clearly displayed in Figure 1.

Claim Limitation	Teaching of the Dozier Reference
	 FIG. 1 *(Appendix E, Figure 1).*
an entire ring oscillator variable speed system clock in said single integrated circuit and	Dozier teaches a "clock generator 38 [that] includes an internal oscillator which is activated when both the XTL 1 and XTL 2 pins are grounded." *(Appendix E, col. 5, lines 24-26).* As noted above, the Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). The Requester notes that the functionality of prior art processors are the same in material respect to commercial processors referred to by the Patent Owner in the above mentioned communications to third parties. Therefore, such an allegation, if true with respect to today's processors, would also be true with regard to the processor taught by Dozier. Accordingly, if the office accepts this premise, one skilled in the art would have understood Dozier to disclose a ring oscillator for clocking the central processing unit.
connected to said	Figure 1 in Dozier clearly shows clock generator 38 connected to the Main

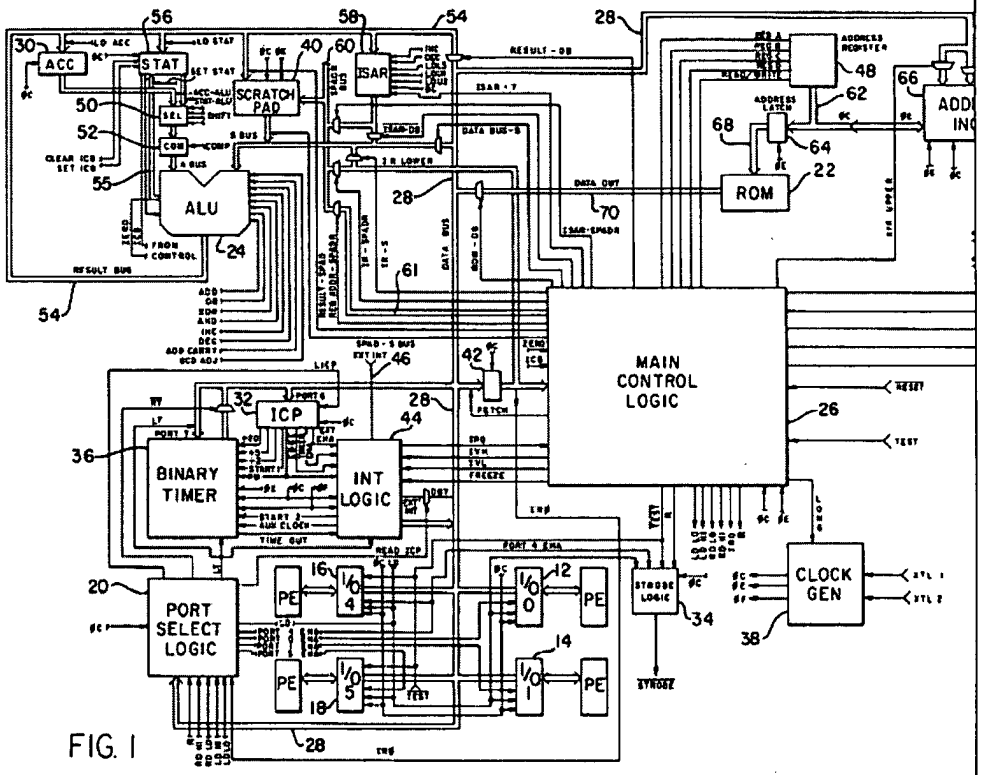
Claim Limitation	Teaching of the Dozier Reference
central processing unit for clocking said central processing unit,	Control Logic. *(Appendix E, Figure 1).* Further, Dozier teaches that the signal generated by the internal oscillator "is the cycle clock from the computer system 10." The main control logic is described as a "principal functional section[] of the microcomputer." *(Appendix E, col. 2, lines 63-68).*
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices	Dozier teaches that "[w]ithin every subsystem of the computer 10 are major buses and major logic elements." *(Appendix E, col. 18, lines 4-8).* Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.
correspondingly constructed of the same process technology with corresponding manufacturing variations,	As explained above, Dozier teaches a microprocessor system fabricated on a single chip, which would necessarily be constructed by a single process technology. It is noteworthy that the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).*
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and	The Patent Owner has stated in correspondence to various third parties that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." (*Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to

Claim Limitation	Teaching of the Dozier Reference
temperature of said single integrated circuit;	naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6) (emphasis added).*
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;	Dozier teaches four "input/output ports" 0, 1, 4, and 5 (labeled as 12, 14, 16, and 18 in Figure 1). *(Appendix E, col. 3, line12; Figure 1).* These ports are described as "principal functional sections of the microcomputer 10," "which may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-68).*
and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	The Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8).* Dozier teaches a test mode, whereby information on one of the ports is immediately fed into the data bus at a rate not synchronized with the clock generator, a form of serial communication which, according to the Patent Owner, satisfies the limitation of a second independent clock signal. Specifically, in test mode "port 5 will take the information existing on its pins and drive it into the internal data bus [which] permits port 5 to be a dedicated input to the internal data bus." *(Appendix D, col. 3, lines 62-66).* Likewise, "the I/O port 4 logic block will take the data from the data bus and supply it directly to its output pins at all times. This operation is <u>not synchronized</u> with the ΦC clock." *(Appendix D, col. 3, lines 54-57) (emphasis added).* Therefore, Dozier meets this claim limitation according to the technical assertions made by the Patent Owner In any case, Requestor notes that the use of a second independent clock for providing clocking signals to an I/O interface was commonplace at the time of filing. *(See, e.g., US Patent Nos. 4,443,845 (col. 17, lines 1-42; figs. 14A-14B); 4,409,665 (col. 5, lines 46-6, line 41; fig. 3c); 4,053,946 (col. 34, lines 15-31); 4,868,784 (col. 25, Table I, "Serial-clock control"); 5,142,637 (col. 6, line 59 to col. 7, line 5; col. 7, line 63 to col. 8, line 2; Figs. 12 & 13)).*
Claim 2	
2. The microprocessor system of claim 1 in which said second clock is a fixed	Dozier teaches that while in test mode, "an external tester may be utilized to input test signals on the internal data bus through port 5." *(Appendix E, col. 4, lines 1-4).* One skilled in the art would recognize that this external tester transmits data into port 5 at a fixed frequency.

Claim Limitation	Teaching of the Dozier Reference
frequency clock.	
Claim 3	
3. In a microprocessor integrated circuit,	The Dozier reference (US Patent No. 4,348,743) teaches a "microprogrammed computer 10 which may be implemented by MOS/LSI techniques and which may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-63).*
a method for clocking the microprocessor within the integrated circuit, comprising the steps of: providing an entire ring oscillator system clock	Dozier teaches a "clock generator 38 [that] includes an internal oscillator which is activated when both the XTL 1 and XTL 2 pins are grounded." *(Appendix E, col. 5, lines 24-26).* The Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). The Requester notes that the functionality of prior art processors are the same in material respect to commercial processors referred to by the Patent Owner in the above mentioned communications to third parties. Therefore, such an allegation, if true with respect to today's processors, would also be true with regard to the processor taught by Dozier. Accordingly, if the office accepts this premise, one skilled in the art would have understood Dozier to disclose a ring oscillator for clocking the central processing unit.
constructed of electronic devices within the integrated circuit,	Dozier teaches that "[w]ithin every subsystem of the computer 10 are major buses and major logic elements." *(Appendix E, col. 18, lines 4-8).* Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.
said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the	As explained above, Dozier teaches a microprocessor system fabricated on a single chip, which would necessarily be constructed by a single process technology. It is noteworthy that the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of

Claim Limitation	Teaching of the Dozier Reference
same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;	physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6) (emphasis added).*
using the ring oscillator system clock for clocking the microprocessor,	As explained above, Dozier teaches clocking the microprocessor with on-chip oscillator.
said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;	The Patent Owner has stated in correspondence to various third parties that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6) (emphasis added).*
providing an on chip input/output interface for the microprocessor integrated circuit; and	Dozier teaches four "input/output ports" 0, 1, 4, and 5 (labeled as 12, 14, 16, and 18 in Figure 1). *(Appendix E, col. 3, line12; Figure 1).* These ports are described as "principal functional sections of the microcomputer 10," "which may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-68).*

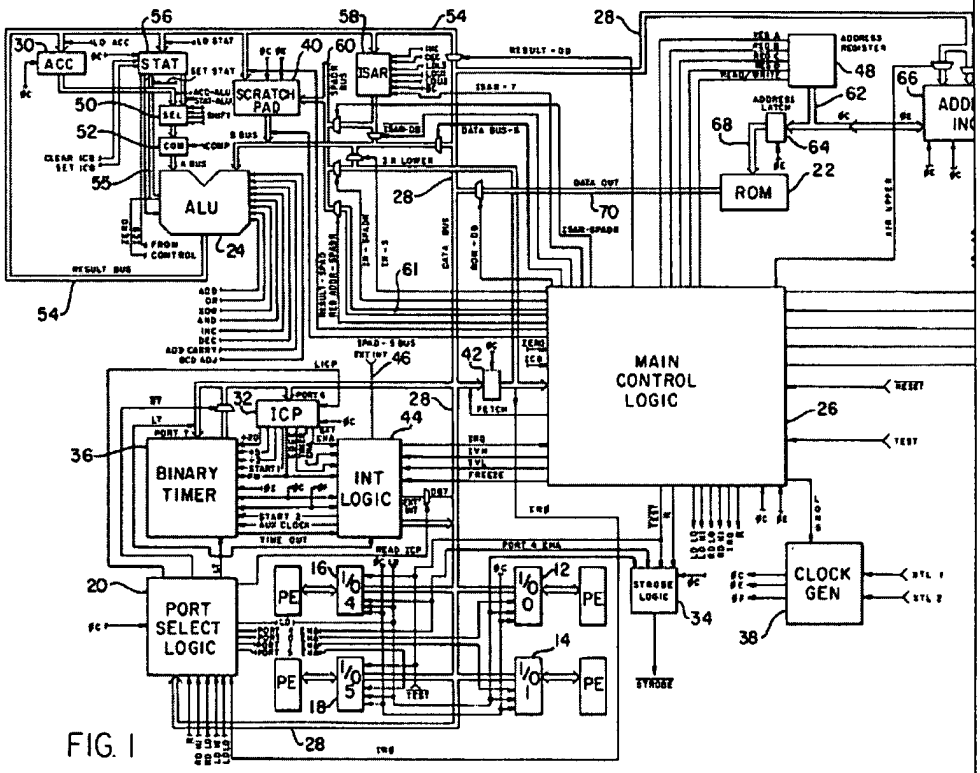
Claim Limitation	Teaching of the Dozier Reference
clocking the input/output interface with a second clock independent of the ring oscillator system clock,	The Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8).* Dozier teaches a test mode, whereby information on one of the ports is immediately fed into the data bus at a rate not synchronized with the clock generator, a form of serial communication which, according to the Patent Owner, satisfies the limitation of a second independent clock signal. Specifically, in test mode "port 5 will take the information existing on its pins and drive it into the internal data bus [which] permits port 5 to be a dedicated input to the internal data bus." *(Appendix D, col. 3, lines 62-66).* Likewise, "the I/O port 4 logic block will take the data from the data bus and supply it directly to its output pins at all times. This operation is <u>not synchronized</u> with the ΦC clock." *(Appendix D, col. 3, lines 54-57) (emphasis added).* Therefore, Dozier meets this claim limitation according to the technical assertions made by the Patent Owner In any case, Requestor notes that the use of a second independent clock for providing clocking signals to an I/O interface was commonplace at the time of filing. *(See, e.g., US Patent Nos. 4,443,845 (col. 17, lines 1-42; figs. 14A-14B); 4,409,665 (col. 5, lines 46-6, line 41; fig. 3c); 4,053,946 (col. 34, lines 15-31); 4,868,784 (col. 25, Table I, "Serial-clock control"); 5,142,637 (col. 6, line 59 to col. 7, line 5; col. 7, line 63 to col. 8, line 2; Figs. 12 & 13)).*
Claim 4	
4. The method of claim 3 in which the second clock is a fixed frequency clock.	Dozier teaches that while in test mode, "an external tester may be utilized to input test signals on the internal data bus through port 5." *(Appendix E, col. 4, lines 1-4).* One skilled in the art would recognize that this external tester transmits data into port 5 at a fixed frequency.
Claim 5	
5. The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.	One skilled in the art would understand that information is transferred to the main control logic at a frequency determined by the internal oscillator. Figure 1 in Dozier clearly shows clock generator 38 connected to the Main Control Logic. *(Appendix E, Figure 1).* Further, Dozier teaches that the signal generated by the internal oscillator "is the cycle clock from the computer system 10." The main control logic is described as a "principal functional section[] of the microcomputer." *(Appendix E, col. 2, lines 63-68).*

Claim Limitation Claim 6	Teaching of the Dozier Reference
6. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency	The Dozier reference (US Patent No. 4,348,743) teaches a "microprogrammed computer 10 which may be implemented by MOS/LSI techniques and which may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-63).* Dozier teaches a "main control logic unit" that "directs the operations of the entire computer." *(Appendix E, col. 1, lines 46-64; 18, lines 1-14).* This main control logic is clearly displayed in Figure 1.  FIG. 1 *(Appendix E, Figure 1).* Dozier teaches a "clock generator 38 [that] includes an internal oscillator which is activated when both the XTL 1 and XTL 2 pins are grounded" for clocking the microprocessor. *(Appendix E, col. 5, lines 24-26).*
and being constructed of a first plurality of electronic	Dozier teaches that "[w]ithin every subsystem of the computer 10 are major buses and major logic elements." *(Appendix E, col. 18, lines 4-8).*

Claim Limitation	Teaching of the Dozier Reference
devices;	Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and	Dozier teaches a "clock generator 38 [that] includes an internal oscillator which is activated when both the XTL 1 and XTL 2 pins are grounded." *(Appendix E, col. 5, lines 24-26).* Dozier teaches producing the "clock signal ΦC" for clocking the microprocessor. *(Appendix E, col. 3, line 26)*
being constructed of a second plurality of electronic devices,	Dozier teaches that "[w]ithin every subsystem of the computer 10 are major buses and major logic elements." *(Appendix E, col. 18, lines 4-8).* Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to	As explained above, Dozier teaches a microprocessor system fabricated on a single chip, which would necessarily be constructed by a single process technology. It is noteworthy that the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." (*Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various

Claim Limitation	Teaching of the Dozier Reference
said parameter variation;	parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6) (emphasis added).*
an on-chip input/output interface, connected between said said [sic] central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	Dozier teaches four "input/output ports" 0, 1, 4, and 5 (labeled as 12, 14, 16, and 18 in Figure 1). *(Appendix E, col. 3, line12; Figure 1).* These ports are described as "principal functional sections of the microcomputer 10," "which may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-68).* Dozier teaches that the control sections of computers often transmit data "into some output device to be stored on another storage media." *(Appendix E, col. 1:56-61).* The input/output ports of the microprogrammed computer taught by Dozier specifically disclose communicating with peripheral devices. *(Appendix E, col. 4, lines 28-29).*
an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	The Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8).* Dozier teaches a test mode, whereby information on one of the ports is immediately fed into the data bus at a rate not synchronized with the clock generator, a form of serial communication which, according to the Patent Owner, satisfies the limitation of a second independent clock signal. Specifically, in test mode "port 5 will take the information existing on its pins and drive it into the internal data bus [which] permits port 5 to be a dedicated input to the internal data bus." *(Appendix D, col. 3, lines 62-66).* Likewise, "the I/O port 4 logic block will take the data from the data bus and supply it directly to its output pins at all times. This operation is <u>not synchronized</u> with the ΦC clock." *(Appendix D, col. 3, lines 54-57) (emphasis added).* Therefore, Dozier meets this claim limitation according to the technical assertions made by the Patent Owner In any case, Requestor notes that the use of a second independent clock for providing clocking signals to an I/O interface was commonplace at the time of filing. *(See, e.g., US Patent Nos. 4,443,845 (col. 17, lines 1-42; figs. 14A-14B); 4,409,665 (col. 5, lines 46-6, line 41; fig. 3c); 4,053,946 (col. 34, lines 15-31); 4,868,784 (col. 25, Table I, "Serial-clock control"); 5,142,637 (col. 6, line 59 to col. 7, line 5; col. 7, line 63 to col. 8, line 2; Figs. 12 & 13)).*
Claim 7	

Claim Limitation	Teaching of the Dozier Reference
7. The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	The Patent Owner has stated in correspondence to various third parties that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." (*Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6) (emphasis added).*
Claim 8	
8. The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.	The test mode taught by Dozier describes a tester placing information onto the pins and therefore having it directly driven onto the data bus at a clock rate that is synchronized with the internal clock cycle. Specifically, "the strobe logic unit 34 is to provide a synchronizing clock to an external tester during the test mode to indicate what machine cycle the computer is in . . . . so that [the tester] can coordinate the forcing of information onto the data bus." *(Appendix E, col. 4, lines 34-45).*
Claim 9	
9. The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	The Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). The Requester notes that the functionality of prior art processors are the same in material respect to commercial processors referred to by the Patent Owner in the above mentioned communications to third parties. Therefore, such an allegation, if true with respect to today's processors, would also be true with regard to the processor taught by Dozier. Accordingly, if the office accepts this premise, one skilled in the art would have understood Dozier to disclose a ring oscillator for clocking the central processing unit.

Claim Limitation	Teaching of the Dozier Reference
Claim 10	
10. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:	The Dozier reference (US Patent No. 4,348,743) teaches a "microprogrammed computer 10 which may be implemented by MOS/LSI techniques and which may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-63).* Dozier teaches a "main control logic unit" that "directs the operations of the entire computer." *(Appendix E, col. 1, lines 46-64; 18, lines 1-14).* This main control logic is clearly displayed in Figure 1.  FIG. 1 *(Appendix E, Figure 1).* Dozier teaches a "clock generator 38 [that] includes an internal oscillator which is activated when both the XTL 1 and XTL 2 pins are grounded" for clocking the microprocessor. *(Appendix E, col. 5, lines 24-26).*
providing said central processing unit upon	As described above, Dozier teaches a "microprogrammed computer 10 which may be implemented by MOS/LSI techniques and which may be

Claim Limitation	Teaching of the Dozier Reference
an integrated circuit substrate,	fabricated on a single semiconductor chip." (Appendix E, col. 2, lines 60-63).
said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	See Dozier teaches that "[w]ithin every subsystem of the computer 10 are major buses and major logic elements." (Appendix E, col. 18, lines 4-8). Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices. Dozier teaches producing the "clock signal ΦC" for clocking the microprocessor. (Appendix E, col. 3, line 26)
providing an entire variable speed clock disposed upon said integrated circuit substrate,	Dozier teaches a "clock generator 38 [that] includes an internal oscillator which is activated when both the XTL 1 and XTL 2 pins are grounded." *(Appendix E, col. 5, lines 24-26).* Dozier teaches producing the "clock signal ΦC" for clocking the microprocessor. *(Appendix E, col. 3, line 26)* The Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). The Requester notes that the functionality of prior art processors are the same in material respect to commercial processors referred to by the Patent Owner in the above mentioned communications to third parties. Therefore, such an allegation, if true with respect to today's processors, would also be true with regard to the processor taught by Dozier. Accordingly, if the office accepts this premise, one skilled in the art would have understood Dozier to disclose a ring oscillator for clocking the central processing unit.
said variable speed clock being constructed of a second plurality of transistors;	Dozier teaches that "[w]ithin every subsystem of the computer 10 are major buses and major logic elements." *(Appendix E, col. 18, lines 4-8).* Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.
clocking said central processing unit at a clock rate using said variable speed clock	As described above, Dozier teaches a "clock generator 38 [that] includes an internal oscillator which is activated when both the XTL 1 and XTL 2 pins are grounded." *(Appendix E, col. 5, lines 24-26).* Dozier teaches producing the "clock signal ΦC" for clocking the microprocessor. *(Appendix E, col. 3, line 26)*

Claim Limitation	Teaching of the Dozier Reference
with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	As explained above, Dozier teaches a microprocessor system fabricated on a single chip, which would necessarily be constructed by a single process technology. It is noteworthy that the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to necessarily "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6) (emphasis added).*
connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	Dozier teaches four "input/output ports" 0, 1, 4, and 5 (labeled as 12, 14, 16, and 18 in Figure 1). *(Appendix E, col. 3, line12; Figure 1).* These ports are described as "principal functional sections of the microcomputer 10," "which may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-68).* Dozier teaches that the control sections of computers often transmit data "into some output device to be stored on another storage media." *(Appendix E, col. 1:56-61).* The input/output ports of the microprogrammed computer taught by Dozier specifically disclose communicating with peripheral devices. *(Appendix E, col. 4, lines 28-29).*

From the foregoing chart, it can be seen that claims 1-10 are anticipated by Dozier.

Thus, claims 1-10 are unpatentable as being anticipated under 35 U.S.C. § 102(b).

C. SNQ #5: The Dozier Reference, in Light of the Mostek, IC Master, Kato, and Ledzius References, Renders Obvious Claims 1-10 of the '336 Patent

In addition to Dozier's anticipation of the '336 patent described above, the Dozier reference, when viewed in light of the Mostek, IC Master, Kato, and Ledzius references, further renders obvious several of the limitations already taught by Dozier.

It would have been obvious to one skilled in the art to modify the Dozier teachings to add a serial I/O port, as recited by the independent claims of the '336 patent. This is because such functionality is taught by Mostek, a chip specification that is almost identical to the Dozier reference in all other respects. Mostek clearly teaches a "Serial Input/Output Port [which] consists of a serial Shift Register, baud rate generator, and control logic." *(Appendix F, page III-105)*. Dozier and Mostek share all other significant functionality, namely a "main control logic," "on-chip oscillator circuit," and I/O ports 0, 1, 4, and 5. *(Appendix F, page III-114; Figure 1)*. Because of these similarities, and because Mostek Corporation is listed as the Assignee of the Dozier patent, one skilled in the art would naturally combine the teachings of Dozier with those of Mostek. *(Appendix E, Abstract page)*.

If one skilled in the art modified the Dozier reference to include the serial I/O port taught by Mostek, the modified Dozier microprocessor would clock the serial I/O port with a second "external clock" that is distinct from the internal oscillator that provides the clock signal to the rest of the circuit, as recited by the independent claims of the '336 patent. *(Appendix F, pages III-102 and III-105)*.

If one skilled in the art modified the teachings of the Dozier reference to include the serial I/O port taught by Mostek, the modified system would also clock the I/O port with a second clock of fixed frequency, as recited by Claims 2, 4, and 8 of the '336 patent. Specifically, Mostek teaches the use of a 3.6864MHz crystal with the second I/O clock. *(Appendix F, page III-109)*. Additionally, Mostek notes that "any TTL compatible square wave input can be used to generate the clock for the serial port." *(Appendix F, page III-110)* (emphasis added). Mostek thus teaches the use of an external clock supplying a fixed frequency square wave.

If one skilled in the art modified the teachings of the Dozier reference to include the serial I/O port taught by Mostek, the modified system would transfer information to and from

the main control logic in synchrony with the internal clock, as recited by Claim 5 of the '336 patent. Specifically, Mostek describes a machine "short cycle, during which time an op code fetch is performed." *(Appendix F, pages III-113).* One skilled in the art would understand that Mostek's main control logic performs the op code fetch. *(Appendix J, page 2019).* The short cycle is based on the time base frequency, which is established by the on-chip oscillator circuit. *(Appendix F, pages III-112 to III-114).* One skilled in the art would have found an apparent reason to combine Mostek with Dozier for reasons discussed above.

If one skilled in the art modified the teachings of the Dozier reference to include the serial I/O port taught by Mostek, the added serial port is "very flexible so that it could be used for other purposes such as an interface to . . . serial memory devices." *(Appendix F, page III-102, col. 1).* Connecting the I/O interface between the central processing unit and an external memory bus is a limitation recited by Claims 6 and 10 of the '336 patent.

It would have been obvious to one skilled in the art to modify the teachings of the Dozier reference to use a ring oscillator variable speed system clock as the internal oscillator, as recited by the independent claims of the '336 patent. This is because such use of a ring oscillator is taught by the Kato reference, which, similar to Dozier, describes a single integrated circuit containing a central processing unit and an oscillator. *(Appendix H, col. 10, line65 to col. 11, line 7).* One skilled in the art would realize the benefits of implementing Kato's ring oscillator as Dozier's oscillator to reduce power consumption during periods of lessened processing demand and to increase clock speed (and power consumption) during periods of increased processing demand. *(Appendix H, col. 11, lines 2-7).*

If one skilled in the art modified the teachings of Dozier to use a ring oscillator variable speed system clock as taught by Kato, the output frequency of the clock would lower "in proportion to the speed of the data processing circuit," as recited by the independent claims of the '336 patent. *(Appendix H, col. 11, lines 2-7)*

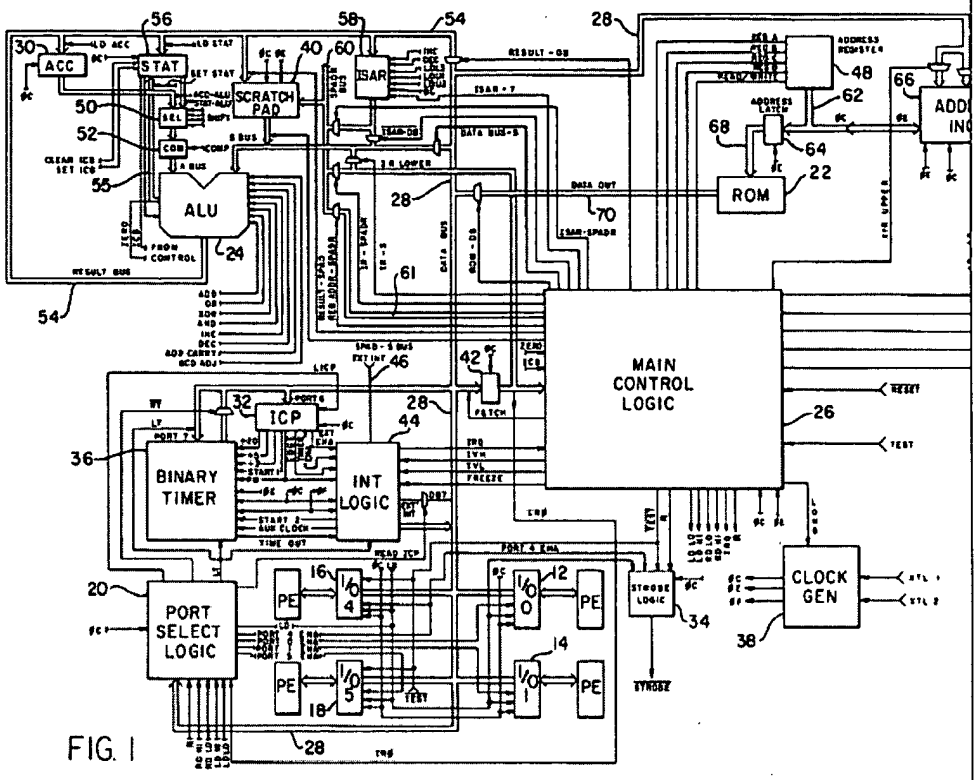
It would have been obvious to one skilled in the art to modify the teachings of the Dozier reference to use the "same batch and section of semiconductor wafer" in order to create corresponding manufacturing variations, as recited by the independent claims of the

'336 patent. *(Appendix I, col. 4, lines 11-12).* This is because the Ledzius reference, which so teaches, is also an integrated circuit with a CPU and an on-chip clock. *(Appendix I, Abstract).*

It would have been obvious to one skilled in the art to modify the teachings of the Dozier reference so that the "frequency of the clock signal produced by [the clock generator] varies to reflect process and temperature variances," as recited by the independent claims of the '336 patent. *(Appendix I, col. 4, lines 9-14).* This is because it would have been obvious to create the circuit of Dozier from the "same batch and section of semiconductor wafer" as taught by Ledzius. *(Id.)*

A detailed explanation of the pertinency and manner of applying the Dozier, Mostek, IC Master, Kato, and Ledzius references to claims 1-10 of the '336 patent is shown in the following claim chart.

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
1. A microprocessor system, comprising a single integrated circuit	The Dozier reference (US Patent No. 4,348,743) teaches a "microprogrammed computer 10 which may be implemented by MOS/LSI techniques and which may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-63).*
including a central processing unit and	Dozier teaches a "main control logic unit" that "directs the operations of the entire computer." *(Appendix E, col. 1, lines 46-64; 18, lines 1-14).* This main control logic is clearly displayed in Figure 1.

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	 FIG. 1 *(Appendix E, Figure 1).*
an entire ring oscillator variable speed system clock in said single integrated circuit and	Dozier teaches a "clock generator 38 [that] includes an internal oscillator which is activated when both the XTL 1 and XTL 2 pins are grounded." *(Appendix E, col. 5, lines 24-26).* As noted above, the Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). Accordingly, if the office accepts this premise, one skilled in the art would have understood Dozier to disclose a ring oscillator for clocking the central processing unit. In any case, this feature is obvious in view of United States Patent No. 4,766,567 to Kato. Kato describes a ring oscillator that can be used to supply clock signals for the main control logic described in Dozier. This is because Kato similarly describes a "one-chip semiconductor device" *(Appendix H, col. 1, lines 6-9)* that utilizes a ring oscillator because the device "need not have a very accurate frequency." *(Appendix H, col. 10, line 64 to col. 11, line 7).* The ring oscillator's "output frequency lowers in

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	proportion to the speed of the data processing circuit which is lowered due to the drop of power supply voltage." *(Appendix H, col. 11, lines 1-5).* One skilled in the art would have seen an apparent reason to implement the variable speed oscillator of Dozier as Kato's ring oscillator, namely because a ring oscillator is an obvious selection for an internal oscillator. One skilled in the art would realize the benefits of implementing Kato's ring oscillator as Dozier's oscillator to reduce power consumption during periods of lessened processing demand and to increase clock speed (and power consumption) during periods of increased processing demand. *(Appendix H, col. 11, lines 2-7).*
connected to said central processing unit for clocking said central processing unit,	Figure 1 in Dozier clearly shows clock generator 38 connected to the Main Control Logic. *(Appendix E, Figure 1).* Further, Dozier teaches that the signal generated by the internal oscillator "is the cycle clock from the computer system 10." The main control logic is described as a "principal functional section[] of the microcomputer." *(Appendix E, col. 2, lines 63-68).*
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices	Dozier teaches that "[w]ithin every subsystem of the computer 10 are major buses and major logic elements." *(Appendix E, col. 18, lines 4-8).* Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.
correspondingly constructed of the same process technology with corresponding manufacturing variations,	As explained above, Dozier teaches a microprocessor system fabricated on a single chip, which would necessarily be constructed by a single process technology. As noted above, the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Additionally, Requestor notes that this feature was commonplace at the

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	time of filing, as shown by U.S. Patent No. 4,691,124 to Ledzius et al. ("Ledzius"). Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in process variations throughout the circuit. *(Appendix I, col. 4, lines 11-12).* Ledzius further teaches that the "frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances." *(Appendix I, col. 4, lines 9-11).* One skilled in the art would have found an apparent reason to combine Ledzius with Dozier, namely to produce Dozier's processor with minimal cost and defects.
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	The Patent Owner has stated in correspondence to various third parties that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." (*Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6) (emphasis added).* In any case, Requestor notes that Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in frequency variations due to process and temperature variations throughout the circuit. *(Appendix I, col. 4, lines 3-21).* Dozier teaches that the entire "microprogrammed computer 10," which contains the clock generator 38 and the main control logic 26, "may be implemented by MOS/LSI techniques and [] may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-63; see Figure 2).* One skilled in the art would have found an apparent reason to combine Ledzius with Dozier, namely to produce the processor of Dozier with minimal cost and defects. Additionally and as described previously, one skilled in the art would see an apparent reason to combine the ring oscillator of Kato with Dozier. In such case, Kato teaches that "[w]hen a ring oscillator is used, its output frequency lowers in proportion to the speed of the data processing circuit, which is lowered due to the drop of power supply voltage." *(Appendix H, col. 11, lines 2-7).*

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	Further, IC Master discloses a microcomputer that varies in frequency from 1.7-4MHz when operating from its internal oscillator due in part to a varying ambient temperature range of 0-70 °C and a varying VCC of +5V +/- 10%. One skilled in the art would combine IC Master with Dozier because both references teach a "main control logic" that is clocked by an "internal oscillator" which is activated when both the XTL 1 and XTL 2 pins are grounded. *(Appendix E, col. 5, lines 24-26; Appendix J, pages 2025-2026).*
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;	Dozier teaches four "input/output ports" 0, 1, 4, and 5 (labeled as 12, 14, 16, and 18 in Figure 1). *(Appendix E, col. 3, line12; Figure 1).* These ports are described as "principal functional sections of the microcomputer 10," "which may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-68).* Additionally, Requestor notes that this feature was commonplace at the time of filing, see for example the Mostek reference. Mostek clearly teaches a "Serial Input/Output Port [which] consists of a serial Shift Register, baud rate generator, and control logic." *(Appendix F, page III-105).* This is a simple addition to the functionality shared between Dozier and Mostek, namely a "main control logic," "on-chip oscillator circuit," and I/O ports 0, 1, 4, and 5. *(Appendix F, page III-114; Figure 1).* One skilled in the art would have found an apparent reason to combine Mostek with Dozier, namely because the chip taught by Mostek is almost identical to the chip taught by the Dozier reference and because Mostek Corporation is listed as the Assignee of the Dozier patent (thus creating a practical presumption that the technologies are compatible). *(Appendix E, Abstract page).*
and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	The Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8).* Dozier teaches a test mode, whereby information on one of the ports is immediately fed into the data bus at a rate not synchronized with the clock generator, a form of serial communication which, according to the Patent Owner, satisfies the limitation of a second independent clock signal. Specifically, in test mode "port 5 will take the information existing on its pins and drive it into the internal data bus [which] permits port 5 to be a dedicated input to the internal data bus." *(Appendix D, col. 3, lines 62-66).* Likewise, "the I/O port 4 logic block will take the data from the data bus and supply it directly to its output pins at all times. This operation is <u>not synchronized</u> with the ΦC clock." *(Appendix D, col. 3, lines 54-57) (emphasis added).* Therefore,

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	Dozier meets this claim limitation according to the technical assertions made by the Patent Owner Alternatively, Requester submits that one skilled in the art would have found an apparent reason to combine Dozier with Mostek's serial I/O port. Mostek teaches that "[d]ata is shifted into or out of the shift register at a rate determined by [an] external clock." *(Appendix F, page III-105).* The serial I/O port clocking signal "is derived from the SRCLK pulse. The SRCLK pulse . . . may be programmed as an input." *(Appendix F, page III-105).* Mostek's main control unit is clocked by the separate, independent "on-chip oscillator circuit." *(Appendix F, pages III-114 to III-115; Figure 1 at page III-103).* One skilled in the art would have found an apparent reason to combine Mostek with Dozier because the chip taught by Mostek is almost identical to the chip taught by the Dozier reference and because Mostek Corporation is listed as the Assignee of the Dozier patent (thus creating a practical presumption that the technologies are compatible). In any case, Requestor notes that the use of a second independent clock for providing clocking signals to an I/O interface was commonplace at the time of filing. *(See, e.g., US Patent Nos. 4,443,845 (col. 17, lines 1-42; figs. 14A-14B); 4,409,665 (col. 5, lines 46-6, line 41; fig. 3c); 4,053,946 (col. 34, lines 15-31); 4,868,784 (col. 25, Table I, "Serial-clock control"); 5,142,637 (col. 6, line 59 to col. 7, line 5; col. 7, line 63 to col. 8, line 2; Figs. 12 & 13)).*
Claim 2	
2. The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	Dozier teaches that while in test mode, "an external tester may be utilized to input test signals on the internal data bus through port 5." *(Appendix E, col. 4, lines 1-4).* One skilled in the art would recognize that this external tester transmits data into port 5 at a fixed frequency. Alternatively, Requester submits that one skilled in the art would have found an apparent reason to combine Dozier with Mostek's I/O port. Mostek teaches the use of a fixed frequency 3.6864MHz crystal with the second I/O clock. *(Appendix F, page III-109).* Additionally, Mostek notes that "<u>any</u> TTL compatible square wave input can be used to generate the clock for the serial port." *(Appendix F, page III-110) (emphasis added).*
Claim 3	
3. In a microprocessor integrated circuit,	The Dozier reference (US Patent No. 4,348,743) teaches a "microprogrammed computer 10 which may be implemented by MOS/LSI techniques and which may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-63).*

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
a method for clocking the microprocessor within the integrated circuit, comprising the steps of: providing an entire ring oscillator system clock	Dozier teaches a "clock generator 38 [that] includes an internal oscillator which is activated when both the XTL 1 and XTL 2 pins are grounded." *(Appendix E, col. 5, lines 24-26).* As noted above, the Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). Accordingly, if the office accepts this premise, one skilled in the art would have understood Dozier to disclose a ring oscillator for clocking the central processing unit. Alternatively, this feature is obvious in view of United States Patent No. 4,766,567 to Kato. Kato describes a ring oscillator that can be used to supply clock signals for the main control logic described in Dozier. This is because Kato similarly describes a "one-chip semiconductor device" *(Appendix H, col. 1, lines 6-9)* that utilizes a ring oscillator because the device "need not have a very accurate frequency." *(Appendix H, col. 10, line 64 to col. 11, line 7).* The ring oscillator's "output frequency lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of power supply voltage." *(Appendix H, col. 11, lines 1-5).* One skilled in the art would have seen an apparent reason to implement the variable speed oscillator of Dozier as Kato's ring oscillator, namely because a ring oscillator is an obvious selection for an internal oscillator. One skilled in the art would realize the benefits of implementing Kato's ring oscillator as Dozier's oscillator to reduce power consumption during periods of lessened processing demand and to increase clock speed (and power consumption) during periods of increased processing demand. *(Appendix H, col. 11, lines 2-7).*
constructed of electronic devices within the integrated circuit,	Dozier teaches that "[w]ithin every subsystem of the computer 10 are major buses and major logic elements." *(Appendix E, col. 18, lines 4-8).* Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.
said electronic devices having operating characteristics which will, because said	As explained above, Dozier teaches a microprocessor system fabricated on a single chip, which would necessarily be constructed by a single process technology. As noted above, the Patent Owner has stated in correspondence to various

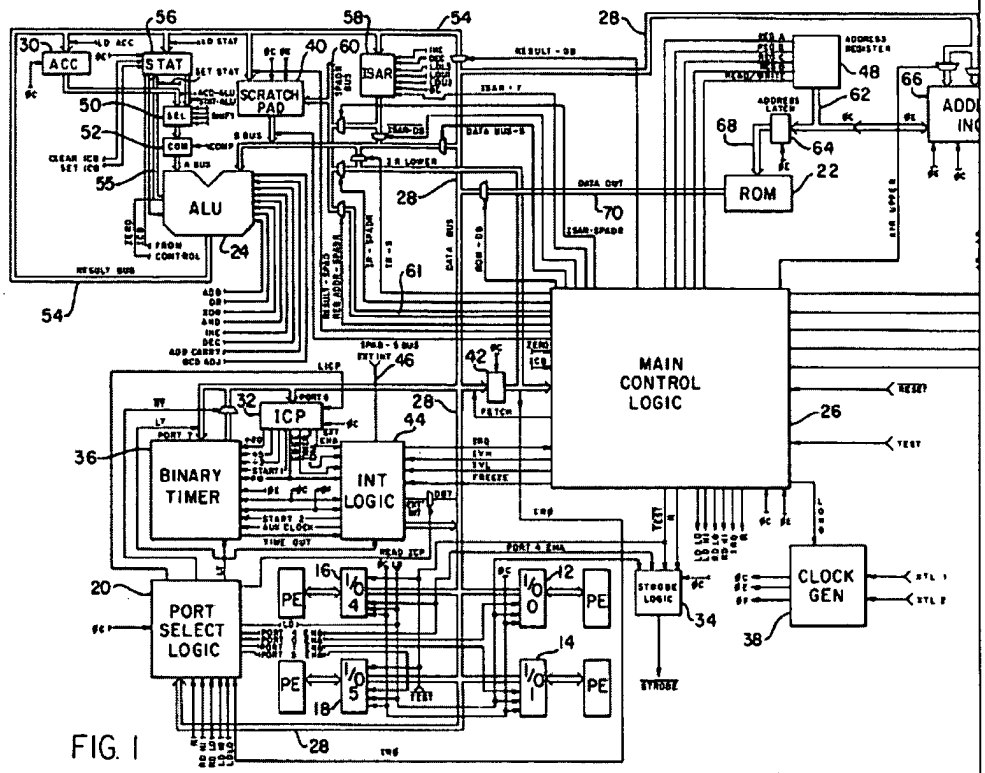
Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;	third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." (*Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6) (emphasis added).* Additionally, Requestor notes that this feature was commonplace at the time of filing, as shown by U.S. Patent No. 4,691,124 to Ledzius et al. ("Ledzius"). Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in process variations throughout the circuit. *(Appendix I, col. 4, lines 11-12).* Ledzius further teaches that the "frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances." *(Appendix I, col. 4, lines 9-11).* One skilled in the art would have found an apparent reason to combine Ledzius with Dozier, namely to produce Dozier's processor with minimal cost and defects. Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in frequency variations due to process and temperature variations throughout the circuit. *(Appendix I, col. 4, lines 3-21).* Dozier teaches that the entire "microprogrammed computer 10," which contains the clock generator 38 and the main control logic 26, "may be implemented by MOS/LSI techniques and [] may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-63; see Figure 2).* Additionally and as described previously, one skilled in the art would see an apparent reason to combine the ring oscillator of Kato with Dozier. In such case, Kato teaches that "[w]hen a ring oscillator is used, its output frequency lowers in proportion to the speed of the data processing circuit, which is lowered due to the drop of power supply voltage." *(Appendix H,*

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	col. 11, lines 2-7). Further, IC Master discloses a microcomputer that varies in frequency from 1.7-4MHz when operating from its internal oscillator due in part to a varying ambient temperature range of 0-70 °C and a varying VCC of +5V +/- 10%. One skilled in the art would combine IC Master with Dozier because both references teach a "main control logic" that is clocked by an "internal oscillator" which is activated when both the XTL 1 and XTL 2 pins are grounded. *(Appendix E, col. 5, lines 24-26; Appendix J, pages 2025-2026).*
using the ring oscillator system clock for clocking the microprocessor,	As explained above, Dozier teaches clocking the microprocessor with on-chip oscillator.
said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;	The Patent Owner has stated in correspondence to various third parties that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." (*Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6) (emphasis added).* As noted above, Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in frequency variations due to process and temperature variations throughout the circuit. *(Appendix I, col. 4, lines 3-21).* Dozier teaches that the entire "microprogrammed computer 10," which contains the clock generator 38 and the main control logic 26, "may be implemented by MOS/LSI techniques and [] may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-63; see Figure 2).* One skilled in the art would have found an apparent reason to combine Ledzius with Dozier, namely to produce the processor of Dozier with minimal cost and defects.

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	Additionally and as described previously, one skilled in the art would see an apparent reason to combine the ring oscillator of Kato with Dozier. In such case, Kato teaches that "[w]hen a ring oscillator is used, its output frequency lowers in proportion to the speed of the data processing circuit, which is lowered due to the drop of power supply voltage." *(Appendix H, col. 11, lines 2-7).* Further, IC Master discloses a microcomputer that varies in frequency from 1.7-4MHz when operating from its internal oscillator due in part to a varying ambient temperature range of 0-70 °C and a varying VCC of +5V +/- 10%. One skilled in the art would combine IC Master with Dozier because both references teach a "main control logic" that is clocked by an "internal oscillator" which is activated when both the XTL 1 and XTL 2 pins are grounded. *(Appendix E, col. 5, lines 24-26; Appendix J, pages 2025-2026).*
providing an on chip input/output interface for the microprocessor integrated circuit; and	Dozier teaches four "input/output ports" 0, 1, 4, and 5 (labeled as 12, 14, 16, and 18 in Figure 1). *(Appendix E, col. 3, line12; Figure 1).* These ports are described as "principal functional sections of the microcomputer 10," "which may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-68).* Additionally, Requestor notes that this feature was commonplace at the time of filing, see for example the Mostek reference. Mostek clearly teaches a "Serial Input/Output Port [which] consists of a serial Shift Register, baud rate generator, and control logic." *(Appendix F, page III-105).* This is a simple addition to the functionality shared between Dozier and Mostek, namely a "main control logic," "on-chip oscillator circuit," and I/O ports 0, 1, 4, and 5. *(Appendix F, page III-114; Figure 1).* One skilled in the art would have found an apparent reason to combine Mostek with Dozier, namely because the chip taught by Mostek is almost identical to the chip taught by the Dozier reference and because Mostek Corporation is listed as the Assignee of the Dozier patent (thus creating a practical presumption that the technologies are compatible). *(Appendix E, Abstract page).*
clocking the input/output interface with a second clock independent of the ring oscillator system clock,	The Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8).* Dozier teaches a test mode, whereby information on one of the ports is immediately fed into the data bus at a rate not synchronized with the clock generator, a form of serial communication which, according to the Patent Owner, satisfies the

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	limitation of a second independent clock signal. Specifically, in test mode "port 5 will take the information existing on its pins and drive it into the internal data bus [which] permits port 5 to be a dedicated input to the internal data bus." *(Appendix D, col. 3, lines 62-66).* Likewise, "the I/O port 4 logic block will take the data from the data bus and supply it directly to its output pins at all times. This operation is not synchronized with the ΦC clock." *(Appendix D, col. 3, lines 54-57) (emphasis added).* Therefore, Dozier meets this claim limitation according to the technical assertions made by the Patent Owner Alternatively, Requester submits that one skilled in the art would have found an apparent reason to combine Dozier with Mostek's serial I/O port would teach the features of this limitation. Mostek teaches that "[d]ata is shifted into or out of the shift register at a rate determined by [an] external clock." *(Appendix F, page III-105).* The serial I/O port clocking signal "is derived from the SRCLK pulse. The SRCLK pulse . . . may be programmed as an input." *(Appendix F, page III-105).* Mostek's main control unit is clocked by the separate, independent "on-chip oscillator circuit." *(Appendix F, pages III-114 to III-115; Figure 1 at page III-103).* One skilled in the art would have found an apparent reason to combine Mostek with Dozier because the chip taught by Mostek is almost identical to the chip taught by the Dozier reference and because Mostek Corporation is listed as the Assignee of the Dozier patent (thus creating a practical presumption that the technologies are compatible). In any case, Requestor notes that the use of a second independent clock for providing clocking signals to an I/O interface was commonplace at the time of filing. *(See, e.g., US Patent Nos. 4,443,845 (col. 17, lines 1-42; figs. 14A-14B); 4,409,665 (col. 5, lines 46-6, line 41; fig. 3c); 4,053,946 (col. 34, lines 15-31); 4,868,784 (col. 25, Table I, "Serial-clock control"); 5,142,637 (col. 6, line 59 to col. 7, line 5; col. 7, line 63 to col. 8, line 2; Figs. 12 & 13)).*
Claim 4	
4. The method of claim 3 in which the second clock is a fixed frequency clock.	Dozier teaches that while in test mode, "an external tester may be utilized to input test signals on the internal data bus through port 5." *(Appendix E, col. 4, lines 1-4).* One skilled in the art would recognize that this external tester transmits data into port 5 at a fixed frequency. Alternatively, Requester submits that one skilled in the art would have found an apparent reason to combine Dozier with Mostek's I/O port. Mostek teaches the use of a fixed frequency 3.6864MHz crystal with the second I/O clock. *(Appendix F, page III-109).* Additionally, Mostek notes that "any TTL compatible square wave input can be used to generate the

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	clock for the serial port." *(Appendix F, page III-110) (emphasis added).*
Claim 5	
5. The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.	One skilled in the art would understand that information is transferred to the main control logic at a frequency determined by the internal oscillator. Figure 1 in Dozier clearly shows clock generator 38 connected to the Main Control Logic. *(Appendix E, Figure 1).* Further, Dozier teaches that the signal generated by the internal oscillator "is the cycle clock from the computer system 10." The main control logic is described as a "principal functional section[] of the microcomputer." *(Appendix E, col. 2, lines 63-68).* Alternatively, this feature is obvious in view of the Mostek reference. Mostek describes a machine "short cycle, during which time an op code fetch is performed." *(Appendix F, pages III-113).* One skilled in the art would understand that Mostek's main control logic performs the op code fetch. *(Appendix J, page 2019).* The short cycle is based on the time base frequency, which is established by the on-chip oscillator circuit. *(Appendix F, pages III-112 to III-114).* One skilled in the art would have found an apparent reason to combine Mostek with Dozier for reasons discussed above.
Claim 6	
6. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency	The Dozier reference (US Patent No. 4,348,743) teaches a "microprogrammed computer 10 which may be implemented by MOS/LSI techniques and which may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-63).* Dozier teaches a "main control logic unit" that "directs the operations of the entire computer." *(Appendix E, col. 1, lines 46-64; 18, lines 1-14).* This main control logic is clearly displayed in Figure 1.

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	 FIG. 1 *(Appendix E, Figure 1).* Dozier teaches a "clock generator 38 [that] includes an internal oscillator which is activated when both the XTL 1 and XTL 2 pins are grounded" for clocking the microprocessor. *(Appendix E, col. 5, lines 24-26).*
and being constructed of a first plurality of electronic devices;	Dozier teaches that "[w]ithin every subsystem of the computer 10 are major buses and major logic elements." *(Appendix E, col. 18, lines 4-8).* Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing	Dozier teaches a "clock generator 38 [that] includes an internal oscillator which is activated when both the XTL 1 and XTL 2 pins are grounded." *(Appendix E, col. 5, lines 24-26).* Dozier teaches producing the "clock signal ΦC" for clocking the microprocessor. *(Appendix E, col. 3, line 26)*

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
unit, said oscillator clocking said central processing unit at a clock rate and	
being constructed of a second plurality of electronic devices,	Dozier teaches that "[w]ithin every subsystem of the computer 10 are major buses and major logic elements." *(Appendix E, col. 18, lines 4-8).* Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	As explained above, Dozier teaches a microprocessor system fabricated on a single chip, which would necessarily be constructed by a single process technology. It is noteworthy that the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6) (emphasis added).* Additionally, Requestor notes that this feature was commonplace at the time of filing, as shown by U.S. Patent No. 4,691,124 to Ledzius et al. ("Ledzius"). Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in process variations throughout the circuit. *(Appendix I, col. 4, lines 11-12).* Ledzius further teaches that the "frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances."

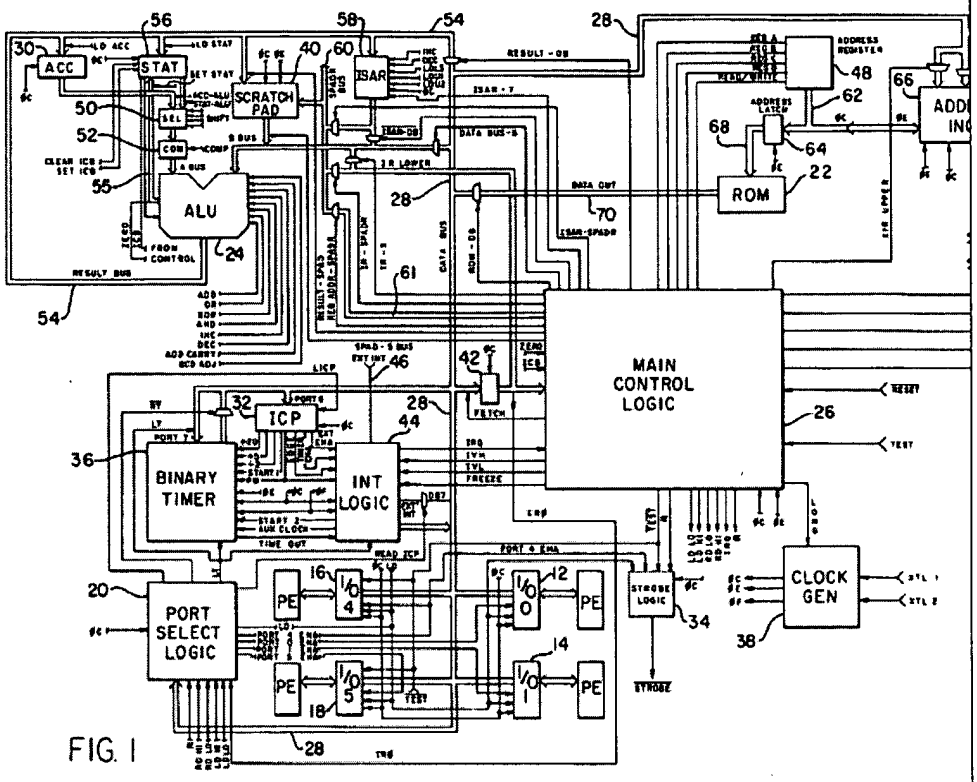
Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	(Appendix I, col. 4, lines 9-11). One skilled in the art would have found an apparent reason to combine Ledzius with Dozier, namely to produce Dozier's processor with minimal cost and defects. Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in frequency variations due to process and temperature variations throughout the circuit. *(Appendix I, col. 4, lines 3-21).* Dozier teaches that the entire "microprogrammed computer 10," which contains the clock generator 38 and the main control logic 26, "may be implemented by MOS/LSI techniques and [] may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-63; see Figure 2).* Additionally and as described previously, one skilled in the art would see an apparent reason to combine the ring oscillator of Kato with Dozier. In such case, Kato teaches that "[w]hen a ring oscillator is used, its output frequency lowers in proportion to the speed of the data processing circuit, which is lowered due to the drop of power supply voltage." *(Appendix H, col. 11, lines 2-7).* Further, IC Master discloses a microcomputer that varies in frequency from 1.7-4MHz when operating from its internal oscillator due in part to a varying ambient temperature range of 0-70 °C and a varying VCC of +5V +/- 10%. One skilled in the art would combine IC Master with Dozier because the chip taught by IC Master is in the same family of processors as the chip taught by the Dozier reference. *(Appendix E, col. 5, lines 24-26; Appendix J, pages 2025-2026).*
an on-chip input/output interface, connected between said said [sic] central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	Dozier teaches four "input/output ports" 0, 1, 4, and 5 (labeled as 12, 14, 16, and 18 in Figure 1). *(Appendix E, col. 3, line12; Figure 1).* These ports are described as "principal functional sections of the microcomputer 10," "which may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-68).* Dozier teaches that the control sections of computers often transmit data "into some output device to be stored on another storage media." *(Appendix E, col. 1:56-61).* The input/output ports of the microprogrammed computer taught by Dozier specifically disclose communicating with peripheral devices. *(Appendix E, col. 4, lines 28-29).* Alternatively, this feature is obvious in view of the Mostek reference. Mostek teaches that the serial port is "very flexible so that it could be used

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	for other purposes such as an interface to . . . serial memory devices." *(Appendix F, page III-102, col. 1)*. One skilled in the art would have found an apparent reason to combine Mostek with Dozier for reasons discussed above. As an aside, Requestor notes that this feature was commonplace at the time of filing, see for example the Mostek reference. Mostek clearly teaches a "Serial Input/Output Port [which] consists of a serial Shift Register, baud rate generator, and control logic." *(Appendix F, page III-105)*. This is a simple addition to the functionality shared between Dozier and Mostek, namely a "main control logic," "on-chip oscillator circuit," and I/O ports 0, 1, 4, and 5. *(Appendix F, page III-114; Figure 1)*. One skilled in the art would have found an apparent reason to combine Mostek with Dozier, namely because the chip taught by Mostek is almost identical to the chip taught by the Dozier reference and because Mostek Corporation is listed as the Assignee of the Dozier patent (thus creating a practical presumption that the technologies are compatible). *(Appendix E, Abstract page)*.
an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	The Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8)*. Dozier teaches a test mode, whereby information on one of the ports is immediately fed into the data bus at a rate not synchronized with the clock generator, a form of serial communication which, according to the Patent Owner, satisfies the limitation of a second independent clock signal. Specifically, in test mode "port 5 will take the information existing on its pins and drive it into the internal data bus [which] permits port 5 to be a dedicated input to the internal data bus." *(Appendix D, col. 3, lines 62-66)*. Likewise, "the I/O port 4 logic block will take the data from the data bus and supply it directly to its output pins at all times. This operation is <u>not synchronized</u> with the ΦC clock." *(Appendix D, col. 3, lines 54-57) (emphasis added)*. Therefore, Dozier meets this claim limitation according to the technical assertions made by the Patent Owner Moreover, Requester submits that one skilled in the art would have found an apparent reason to combine Dozier with Mostek's serial I/O port. Mostek teaches that "[d]ata is shifted into or out of the shift register at a rate determined by [an] external clock." *(Appendix F, page III-105)*. The serial I/O port clocking signal "is derived from the SRCLK pulse. The SRCLK pulse . . . may be programmed as an input." *(Appendix F, page III-105)*. Mostek's main control unit is clocked by the separate, independent "on-

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	chip oscillator circuit." *(Appendix F, pages III-114 to III-115; Figure 1 at page III-103).* One skilled in the art would have found an apparent reason to combine Mostek with Dozier for reasons discussed above. In any case, Requestor notes that the use of a second independent clock for providing clocking signals to an I/O interface was commonplace at the time of filing. *(See, e.g., US Patent Nos. 4,443,845 (col. 17, lines 1-42; figs. 14A-14B); 4,409,665 (col. 5, lines 46-6, line 41; fig. 3c); 4,053,946 (col. 34, lines 15-31); 4,868,784 (col. 25, Table I, "Serial-clock control"); 5,142,637 (col. 6, line 59 to col. 7, line 5; col. 7, line 63 to col. 8, line 2; Figs. 12 & 13)).*
Claim 7	
7. The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	The Patent Owner has stated in correspondence to various third parties that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." (*Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6) (emphasis added).* As an aside, Requestor notes that Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in frequency variations due to process and temperature variations throughout the circuit. *(Appendix I, col. 4, lines 3-21).* Dozier teaches that the entire "microprogrammed computer 10," which contains the clock generator 38 and the main control logic 26, "may be implemented by MOS/LSI techniques and [] may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-63; see Figure 2).* One skilled in the art would have found an apparent reason to combine Ledzius with Dozier, namely to produce the processor of Dozier with minimal cost and defects. Further, IC Master discloses a microcomputer that varies in frequency from 1.7-4MHz when operating from its internal oscillator due in part to a varying ambient temperature range of 0-70 °C and a varying VCC of +5V +/-

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	10%. One skilled in the art would combine IC Master with Dozier because the chip taught by IC Master is in the same family of processors as the chip taught by the Dozier reference. *(Appendix E, col. 5, lines 24-26; Appendix J, pages 2025-2026).*
Claim 8	
8. The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.	The test mode taught by Dozier describes a tester placing information onto the pins and therefore having it directly driven onto the data bus at a clock rate that is synchronized with the internal clock cycle. Specifically, "the strobe logic unit 34 is to provide a synchronizing clock to an external tester during the test mode to indicate what machine cycle the computer is in . . . . so that [the tester] can coordinate the forcing of information onto the data bus." *(Appendix E, col. 4, lines 34-45).* As an aside, the Requester notes that this limitation is also taught by Kato. Kato teaches a microprocessor system having two clock. The first clock generator clocks the CPU and the second clock generator is connected to the I/O port. *(Appendix H, col. 4, lines 37-42 and FIG. 4)* Kato teaches that the first and second clock generators operate synchronously: "second clock generator 15 produces two clock signals ϕa and ϕb... Signals ϕa and ϕb are produced in synchronism with the signal from first clock generator 14." *(Appendix H, col. 4, lines 56-60)* As explained above, one skilled in the art would have found an apparent reason to combine the teachings of Kato and Mostek, namely to provide Mostek with a ring oscillator to reduce power consumption during periods of lessened processing demand and to increase clock speed (and power consumption) during periods of increased processing demand. *(Appendix H, col. 11, lines 2-7).*
Claim 9	
9. The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	The Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). The Requester notes that the functionality of prior art processors are the same in material respect to commercial processors referred to by the Patent Owner in the above mentioned communications to third parties. Therefore, such an allegation, if true with respect to today's processors, would also be true with regard to the processor taught by Dozier. Accordingly, if the office accepts this premise, one skilled in the art would have understood Dozier to disclose a ring oscillator for clocking the central processing unit.

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	Alternatively, this feature is obvious in view of United States Patent No. 4,766,567 to Kato. Kato describes a ring oscillator that can be used to supply clock signals for the main control logic described in Dozier. This is because Kato similarly describes a "one-chip semiconductor device" *(Appendix H, col. 1, lines 6-9)* that utilizes a ring oscillator because the device "need not have a very accurate frequency." *(Appendix H, col. 10, line 64 to col. 11, line 7).* The ring oscillator's "output frequency lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of power supply voltage." *(Appendix H, col. 11, lines 1-5).* One skilled in the art would have seen an apparent reason to implement the variable speed oscillator of Dozier as Kato's ring oscillator, namely because a ring oscillator is an obvious selection for an internal oscillator. One skilled in the art would realize the benefits of implementing Kato's ring oscillator as Dozier's oscillator to reduce power consumption during periods of lessened processing demand and to increase clock speed (and power consumption) during periods of increased processing demand. *(Appendix H, col. 11, lines 2-7).*
Claim 10	
10. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:	The Dozier reference (US Patent No. 4,348,743) teaches a "microprogrammed computer 10 which may be implemented by MOS/LSI techniques and which may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-63).* Dozier teaches a "main control logic unit" that "directs the operations of the entire computer." *(Appendix E, col. 1, lines 46-64; 18, lines 1-14).* This main control logic is clearly displayed in Figure 1.

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	 FIG. 1 *(Appendix E, Figure 1).* Dozier teaches a "clock generator 38 [that] includes an internal oscillator which is activated when both the XTL 1 and XTL 2 pins are grounded" for clocking the microprocessor. *(Appendix E, col. 5, lines 24-26).*
providing said central processing unit upon an integrated circuit substrate,	As described above, Dozier teaches a "microprogrammed computer 10 which may be implemented by MOS/LSI techniques and which may be fabricated on a single semiconductor chip." (Appendix E, col. 2, lines 60-63).
said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	See Dozier teaches that "[w]ithin every subsystem of the computer 10 are major buses and major logic elements." (Appendix E, col. 18, lines 4-8). Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices. Dozier teaches producing the "clock signal ΦC" for clocking the

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	microprocessor. (Appendix E, col. 3, line 26)
providing an entire variable speed clock disposed upon said integrated circuit substrate,	Dozier teaches a "clock generator 38 [that] includes an internal oscillator which is activated when both the XTL 1 and XTL 2 pins are grounded." *(Appendix E, col. 5, lines 24-26).* Dozier teaches producing the "clock signal ΦC" for clocking the microprocessor. *(Appendix E, col. 3, line 26)* The Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). The Requester notes that the functionality of prior art processors are the same in material respect to commercial processors referred to by the Patent Owner in the above mentioned communications to third parties. Therefore, such an allegation, if true with respect to today's processors, would also be true with regard to the processor taught by Dozier. Accordingly, if the office accepts this premise, one skilled in the art would have understood Dozier to disclose a ring oscillator for clocking the central processing unit. Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in frequency variations due to process and temperature variations throughout the circuit. *(Appendix I, col. 4, lines 3-21).* Dozier teaches that the entire "microprogrammed computer 10," which contains the clock generator 38 and the main control logic 26, "may be implemented by MOS/LSI techniques and [] may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-63; see Figure 2).* Additionally and as described previously, one skilled in the art would see an apparent reason to combine the ring oscillator of Kato with Dozier. In such case, Kato teaches that "[w]hen a ring oscillator is used, its output frequency lowers in proportion to the speed of the data processing circuit, which is lowered due to the drop of power supply voltage." *(Appendix H, col. 11, lines 2-7).* Further, IC Master discloses a microcomputer that varies in frequency from 1.7-4MHz when operating from its internal oscillator due in part to a varying ambient temperature range of 0-70 °C and a varying VCC of +5V +/- 10%. One skilled in the art would combine IC Master with Dozier because the chip taught by IC Master is in the same family of processors as the chip taught by the Dozier reference. *(Appendix E, col. 5, lines 24-26; Appendix J, pages 2025-2026).*

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
said variable speed clock being constructed of a second plurality of transistors;	Dozier teaches that "[w]ithin every subsystem of the computer 10 are major buses and major logic elements." *(Appendix E, col. 18, lines 4-8).* Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.
clocking said central processing unit at a clock rate using said variable speed clock	As described above, Dozier teaches a "clock generator 38 [that] includes an internal oscillator which is activated when both the XTL 1 and XTL 2 pins are grounded." *(Appendix E, col. 5, lines 24-26).* Dozier teaches producing the "clock signal ΦC" for clocking the microprocessor. *(Appendix E, col. 3, line 26)*
with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	As explained above, Dozier teaches a microprocessor system fabricated on a single chip, which would necessarily be constructed by a single process technology. It is noteworthy that the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." (*Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to necessarily "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6) (emphasis added).* Additionally, Requestor notes that this feature was commonplace at the time of filing, as shown by U.S. Patent No. 4,691,124 to Ledzius et al. ("Ledzius"). Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in process variations throughout the circuit. *(Appendix I, col. 4, lines 11-12).* Ledzius further teaches that the "frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances." *(Appendix I, col. 4, lines 9-11).* One skilled in the art would have found an

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	apparent reason to combine Ledzius with Dozier, namely to produce Dozier's processor with minimal cost and defects. Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in frequency variations due to process and temperature variations throughout the circuit. *(Appendix I, col. 4, lines 3-21).* Dozier teaches that the entire "microprogrammed computer 10," which contains the clock generator 38 and the main control logic 26, "may be implemented by MOS/LSI techniques and [] may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-63; see Figure 2).* Additionally and as described previously, one skilled in the art would see an apparent reason to combine the ring oscillator of Kato with Dozier. In such case, Kato teaches that "[w]hen a ring oscillator is used, its output frequency lowers in proportion to the speed of the data processing circuit, which is lowered due to the drop of power supply voltage." *(Appendix H, col. 11, lines 2-7).* Further, IC Master discloses a microcomputer that varies in frequency from 1.7-4MHz when operating from its internal oscillator due in part to a varying ambient temperature range of 0-70 °C and a varying VCC of +5V +/- 10%. One skilled in the art would combine IC Master with Dozier is in the same family of processors. *(Appendix E, col. 5, lines 24-26; Appendix J, pages 2025-2026).*
connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	Dozier teaches four "input/output ports" 0, 1, 4, and 5 (labeled as 12, 14, 16, and 18 in Figure 1). *(Appendix E, col. 3, line12; Figure 1).* These ports are described as "principal functional sections of the microcomputer 10," "which may be fabricated on a single semiconductor chip." *(Appendix E, col. 2, lines 60-68).* Dozier teaches that the control sections of computers often transmit data "into some output device to be stored on another storage media." *(Appendix E, col. 1:56-61).* The input/output ports of the microprogrammed computer taught by Dozier specifically disclose communicating with peripheral devices. *(Appendix E, col. 4, lines 28-29).* Alternatively, this feature is obvious in view of the Mostek reference. Mostek teaches that the serial port is "very flexible so that it could be used for other purposes such as an interface to . . . serial memory devices." *(Appendix F, page III-102, col. 1).* One skilled in the art would have found

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	an apparent reason to combine Mostek with Dozier for reasons discussed above. As an aside, Requestor notes that this feature was commonplace at the time of filing, see for example the Mostek reference. Mostek clearly teaches a "Serial Input/Output Port [which] consists of a serial Shift Register, baud rate generator, and control logic." *(Appendix F, page III-105)*. This is a simple addition to the functionality shared between Dozier and Mostek, namely a "main control logic," "on-chip oscillator circuit," and I/O ports 0, 1, 4, and 5. *(Appendix F, page III-114; Figure 1)*. One skilled in the art would have found an apparent reason to combine Mostek with Dozier, namely because the chip taught by Mostek is almost identical to the chip taught by the Dozier reference and because Mostek Corporation is listed as the Assignee of the Dozier patent (thus creating a practical presumption that the technologies are compatible). *(Appendix E, Abstract page)*.
clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said variable speed clock.	The Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8)*. Dozier teaches a test mode, whereby information on one of the ports is immediately fed into the data bus at a rate not synchronized with the clock generator, a form of serial communication which, according to the Patent Owner, satisfies the limitation of a second independent clock signal. Specifically, in test mode "port 5 will take the information existing on its pins and drive it into the internal data bus [which] permits port 5 to be a dedicated input to the internal data bus." *(Appendix D, col. 3, lines 62-66)*. Likewise, "the I/O port 4 logic block will take the data from the data bus and supply it directly to its output pins at all times. This operation is <u>not synchronized</u> with the ΦC clock." *(Appendix D, col. 3, lines 54-57) (emphasis added)*. Therefore, Dozier meets this claim limitation according to the technical assertions made by the Patent Owner Alternatively, Requester submits that one skilled in the art would have found an apparent reason to combine Dozier with Mostek's serial I/O port. Mostek teaches that "[d]ata is shifted into or out of the shift register at a rate determined by [an] external clock." *(Appendix F, page III-105)*. The serial I/O port clocking signal "is derived from the SRCLK pulse. The SRCLK pulse . . . may be programmed as an input." *(Appendix F, page III-105)*. Mostek's main control unit is clocked by the separate, independent "on-chip oscillator circuit." *(Appendix F, pages III-114 to III-115; Figure 1 at page III-103)*. One skilled in the art would have found an apparent reason

Claim Limitation	Dozier in combination with Mostek, IC Master, Kato, and Ledzius
	to combine Mostek with Dozier because the chip taught by Mostek is almost identical to the chip taught by the Dozier reference and because Mostek Corporation is listed as the Assignee of the Dozier patent (thus creating a practical presumption that the technologies are compatible). In any case, Requestor notes that the use of a second independent clock for providing clocking signals to an I/O interface was commonplace at the time of filing. *(See, e.g., US Patent Nos. 4,443,845 (col. 17, lines 1-42; figs. 14A-14B); 4,409,665 (col. 5, lines 46-6, line 41; fig. 3c); 4,053,946 (col. 34, lines 15-31); 4,868,784 (col. 25, Table I, "Serial-clock control"); 5,142,637 (col. 6, line 59 to col. 7, line 5; col. 7, line 63 to col. 8, line 2; Figs. 12 & 13)).*

From the foregoing chart, it can be seen that claims 1-10 are rendered obvious under U.S.C. § 103 by Dozier in view of the Mostek, IC Master, Kato, and Ledzius references.

D. The Dozier Reference, in Light of the Mostek, IC Master, Kato, and Ledzius References, Renders Obvious the Newly Introduced Claims of the '336 Patent

The Dozier reference, in light of the Mostek, IC Master, Kato, and Ledzius references renders obvious new claims added during the patent's ongoing merged reexamination. The Patent Owner added claims 11-20 which parallel respective original claims 1-10 except that they further include a limitation to "more clearly set forth the meaning of 'independent.'" *(Appendix C, Amendment, Sept. 8, 2008, original page 11).* The additional limitations append the parallel independent claims and recite: "thereby enabling decoupling a speed of said central processing unit from a speed of said input/output interface." *(Id.).*

Specifically, Dozier teaches the test mode discussed above, whereby information on the data bus is immediately fed to one of the ports and conversely, information on another port is immediately fed into the data, a form of serial communication which, according to the Patent Owner, satisfies the limitation of a second clock signal. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8).* "This operation is not synchronized with the ΦC clock," which indicates a decoupling of speed of this serial communication from the speed of the main control logic. *(Appendix D, col. 3, lines 54-57) (emphasis added).*

In any case, if one skilled in the art modified the Dozier reference to include the serial I/O port taught by Mostek, Dozier would also be modified to include a second clock connected to the serial input/output port. Specifically, the serial input/output port taught by Mostek is clocked by an "external clock" that is distinct and decoupled in speed from the internal oscillator that provides the clock signal to the rest of the circuit. *(Appendix F, pages III-102 and III-105).*

XI. THE RICHTER REFERENCE ANTICIPATES OR, IN LIGHT OF THE MCDERMOTT, LEDZIUS, AND KATO REFERENCES, RENDERS OBVIOUS CLAIMS 1-10 OF THE '336 PATENT

The prior art references provided in this request raise substantial new questions of patentability as to claims 1-10 of the '336 patent. Specifically, all claims are anticipated by the Richter reference and additionally rendered obvious over Richter in light of the McDermott, Ledzius, and Kato references.

A. Summary of the Teachings of the Richter Reference

The Richter reference teaches a system for adapting the speed of a serial interface of a data processing system to the data transmission speed of a communication partner. *(Appendix D, col. 1, lines 46-60).* More specifically, this system consists of a microprocessor system 2 which is connected to several other microprocessor systems via a bus system. *(Appendix D, col. 2, lines 32-36).* The reference teaches an arrangement in which the microprocessor will "adjust itself to the individual transmission speeds of the respective communicating partners." *(Appendix D, col. 2, lines 50-54).* It is contemplated to provide the microprocessor system 2 "in a one-chip system" with a microprocessor, RAM and ROM memory chips, a serial interface, and "other chips required for their operation." *(Appendix D, col. 2, lines 63-65).* In some embodiments, the voltage controlled oscillator is "required" for the operation of the microprocessor.

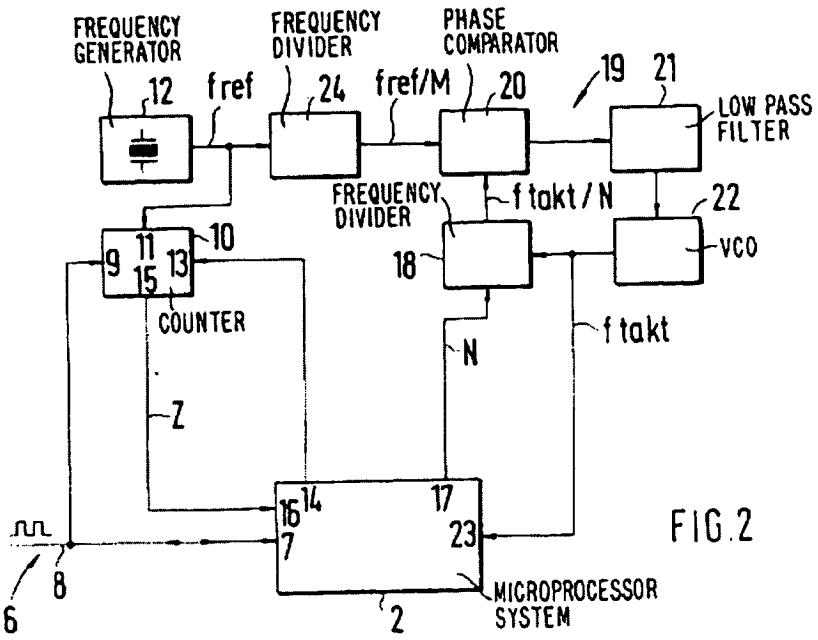


FIG.2

(Appendix D, Figure 2)

The circuit functions to operate the serial interface at the same frequency as the signals arriving at the interface. Specifically, a counter 10 counts signals that arrive on signal line 8 and informs the microprocessor system of the result at input 16. *(Appendix D, col. 3, lines 1-10).* The microprocessor system outputs a signal N on output 17 into a phase locking loop 19, which drives the signal for a voltage controlled oscillator 22. *(Appendix D, col. 3, lines 11-17).* "The voltage controlled oscillator 22 generates a clock pulse "ftakt" that acts upon the microprocessor system 2 through clock frequency input 23." *(Appendix D, col. 3, lines 18-20).* Due also to the input of a signal from a frequency generator 12, the "ftakt" signal settles upon an equilibrium of "(N/M) * fref" where M is fixed and N is the signal output to the phase locking loop by the microprocessor system. *(Appendix D, col. 3, lines 67 through col. 4, line 13).* The signal "ftakt" is used in various embodiments to clock the serial transmission interface. *(Appendix D, col. 4, lines 34-43).* In one embodiment, Richter teaches that a "a separate system clock generator" that is independent of the "ftakt" signal may serve as the system clock for the microprocessor 2. *(Appendix D, col. 4, lines 34-43).*

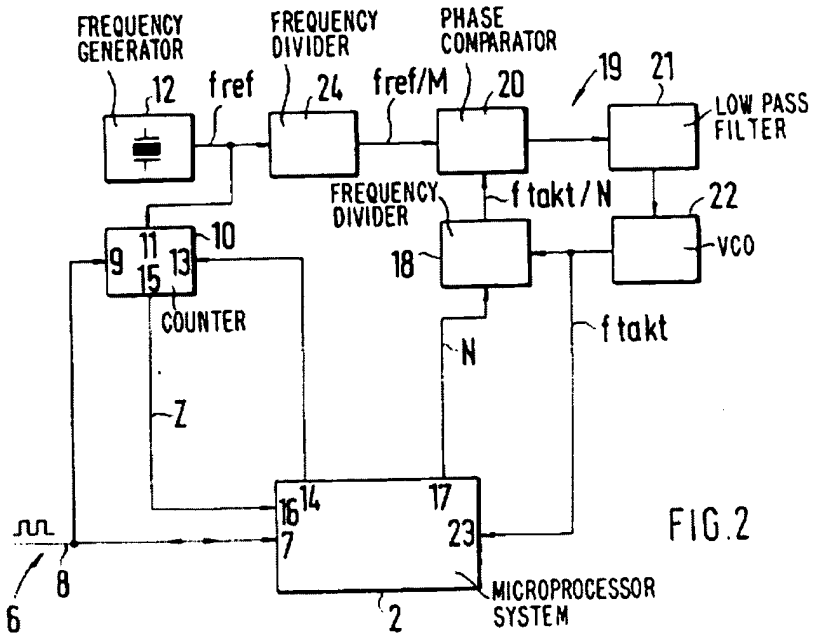
B. SNQ #6: The Richter Reference Anticipates Claims 1-10 of the '336 Patent

The '336 patent claims the same functionality described above in connection with the Richter reference. The patent teaches a single integrated circuit "microprocessor system" that includes a ring oscillator which clocks a central processing unit. *(Appendix A, Claim 1).* These components are claimed to include a plurality of devices and be "constructed of the same process technology" so that the speed of the central processing unit and the ring oscillator vary together. *(Appendix A, Claim 1).* The integrated circuit must also include an "on-chip input/output interface," to which a second clock independent of the ring oscillator is connected. *(Appendix A, Claim 1).*

This claimed functionality is taught by the Richter reference. Richter teaches a voltage controlled oscillator, a microprocessor, and an I/O port that may be provided in a "single-chip" system. In some embodiments the voltage controlled oscillator clocks both the serial I/O port and the microprocessor. Richter teaches additional embodiments where the microprocessor is clocked by a "separate system clock generator." It is inherent to use a second, voltage controlled oscillator as the separate system clock generator because Richter already teaches clocking the microprocessor with a voltage controlled oscillator. The Patent Owner has asserted in communication with various third parties that a voltage controlled oscillator is the equivalent of a ring oscillator. Further, the Patent Owner has asserted that an oscillator and a central processing unit provided on the same chip both include a plurality of devices and vary in speed together.

A detailed explanation of the pertinency and manner of applying the Richter reference to claims 1-10 of the '336 patent is shown in the following claim chart.

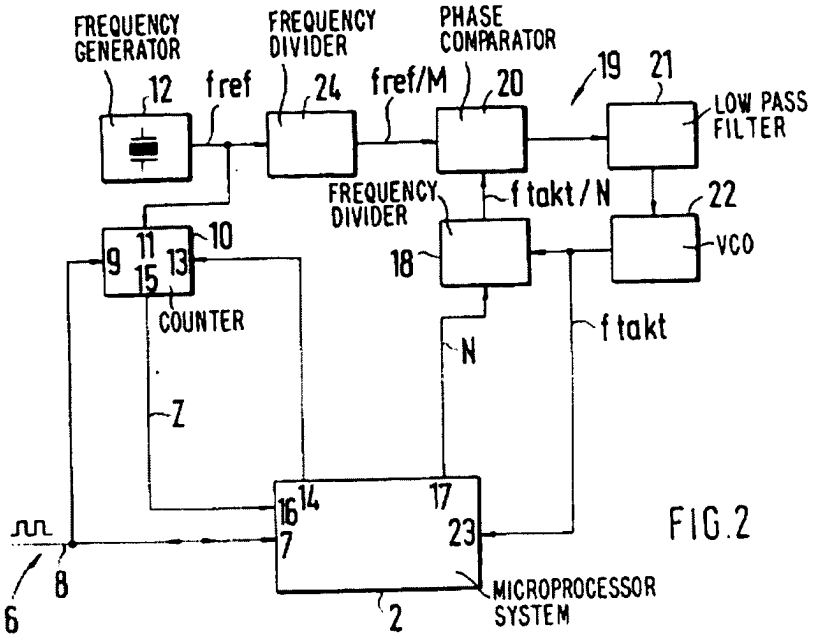
Claim Limitation Claim 1	Teaching of the Richter Reference
1. A microprocessor system, comprising a single integrated circuit	The Richter reference (U.S. Patent No. 4,853,841) teaches a "microprocessor system 2" that is contemplated to provide the functions of a microprocessor, RAM, ROM, a serial interface, and a parallel interface where "in a one-chip system." *(Appendix D, col. 2, lines 55-65).*

Claim Limitation	Teaching of the Richter Reference
	 FIG.2 *(Appendix D, Figure 2).*
including a central processing unit and	Richter teaches that the "microprocessor system" includes a "microprocessor." *(Appendix D, col. 2, lines 55-65).*
an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	Richter teaches that a "voltage-controlled oscillator generates a clock pulse 'ftakt' that acts upon the microprocessor system." *(Appendix D, col. 3, lines 18-20).* In some embodiments the 'ftakt' signal is used as both the system clock and a clock for the I/O port. *(Appendix D, col. 4, lines 34-43).* In other embodiments Richter teaches that the microprocessor is clocked by a "separate system clock generator for the microprocessor 2." *(Appendix D, col. 4, lines 34-38).* It is inherent to use a second, voltage controlled oscillator as the separate system clock generator because Richter already teaches clocking the microprocessor with a voltage controlled oscillator in a different embodiment. The Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). The Requester notes that the functionality of prior art processors are the same in material respect to commercial processors referred to by the Patent Owner in the above mentioned communications to third parties. Therefore, such an allegation, if true with respect to

Claim Limitation	Teaching of the Richter Reference
	today's processors, would also be true with regard to the processor taught by Richter. Accordingly, if the office accepts this premise, one skilled in the art would have understood Richter to disclose a ring oscillator for clocking the central processing unit. Further, Richter teaches that the voltage-controlled oscillator may be provided in the one-chip microprocessor system. Specifically, "[t]he first microprocessor system 2 is, for example, set up in a configuration comprising the microprocessor, volatile (RAM) and nonvolatile (ROM) memory chips, the serial interface and parallel input/output chips as well as other chips required for their operation. It is also contemplated to provide all these functions in a one-chip system." *(Appendix D, col. 2, lines 59-66).* The voltage-controlled oscillator, along with most of the other components displayed in Figure 2, are required for the operation of the microprocessor, and thus Richter teaches providing them on the one-chip system.
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	One skilled in the art would understand the on-chip oscillator circuit and the main control logic to include a plurality of electronic devices. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices. With respect to the limitation of the CPU and ring oscillator being constructed of the same process technology, Richter teaches implementing the microprocessor "in a one-chip system." *(Appendix D, col. 2, lines 55-65)*, which would necessarily be constructed by a single process technology. This indicates that the oscillator is fabricated on the same chip as the CPU and that the oscillator and CPU would therefore be constructed by the same process technology. *(Appendix F, page III-114)* It is noteworthy that the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).*

Claim Limitation	Teaching of the Richter Reference
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	The Patent Owner has stated in correspondence to various third parties that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6.)*
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;	Richter teaches that the "microprocessor system 2 has a serial interface (not shown) which is connected by the input/output port 7 to a signal line 8 of the serial bus system 6." *(Appendix D, col. 2, lines 55-58).*
and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	Richter teaches a signal "ftakt" for clocking the serial I/O port of the microprocessor that is independent of the CPU clock: "the data transmission of the serial interface is supplied with the clock frequency signal 'ftakt', and the microprocessor of the microprocessor system 2 is equipped with its own system clock generator." *(Col. 4, lines 34-43 and 58-62)* Richter describes the system clock as a "separate system clock generator for the microprocessor" that is independent of the I/O clock signal. *(Col. 4, lines 36-47)* Additionally, the Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8).* As previously described, Richter clearly teaches a serial interface. If the Patent Owner's assertions are true today as to commercial processors, then they are also true as to the prior art processors.

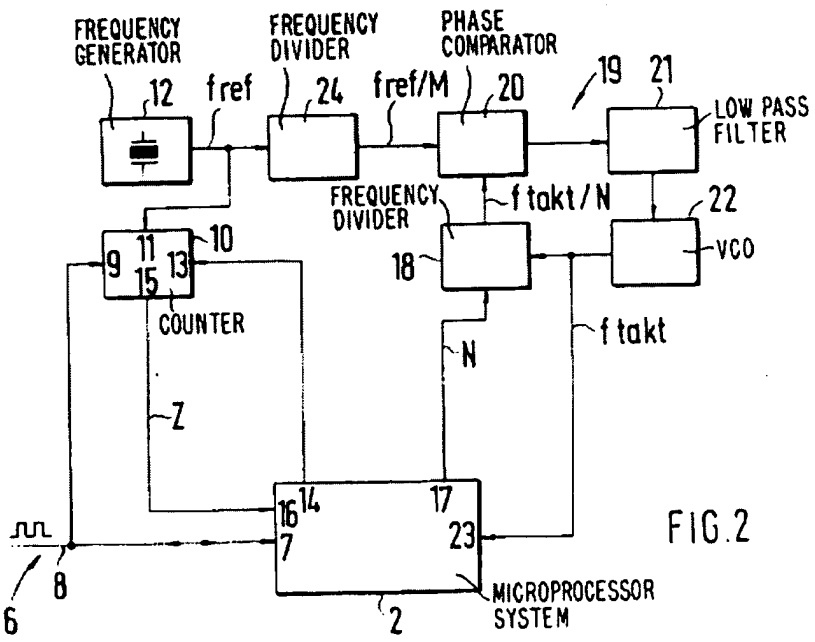
Claim Limitation	Teaching of the Richter Reference
	In any case, Requestor notes that the use of a second independent clock for providing clocking signals to an I/O interface was commonplace at the time of filing. *(See, e.g., US Patent Nos. 4,443,845 (col. 17, lines 1-42; figs. 14A-14B); 4,409,665 (col. 5, lines 46-6, lines 41; fig. 3c); 4,053,946 (col. 34, lines 15-31); 4,868,784 (col. 25, Table I, "Serial-clock control"); 5,142,637 (col. 6, line 59 to col. 7, line 5; col. 7, line 63 to col. 8, line 2; Figs. 12 & 13)).*
Claim 2	
2. The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	Richter teaches that "[t]he division ratio 1/M at the second frequency divider 24 is fixed. It determines the frequency increments by which the clock frequency signal 'ftakt' can be adjusted. It is fixed such that by means of a programmable, integer value of N, a suitable clock frequency 'ftakt' is adjusted. From this adjusted clock frequency 'ftakt', the desired transmission speeds v' can be derived with a required precision by integer division so that the microprocessor system can therefore be synchronized with the communication partner." *(Col. 4, lines 10-19)* One skilled in the art would understand that if the communication partner operates at a fixed frequency, the clock signal 'ftakt' would be a fixed frequency clock signal. The clock signal 'ftakt" taught by Richter is based on "clock frequency input 23." *(Col. 3, lines 18-20).* Requester notes that use of a fixed frequency clock as a clock input was well known in the art at the time of filing. *(See, e.g., the Mostek reference (Appendix F, page III-109);US 4,893,271 (col. 1, lines 17-18); US 4,751,565 (col. 1, lines 50-52); US 4,947,411 (Abstract); US 5,050,195 (Abstract); US 4,835,491 (col. 2, lines 24-25))* Additionally, the Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8).* If the Patent Owner's assertions are accepted, one skilled in the art would recognize that the incoming signal to the serial interface could be of fixed frequency, teaching the features of this limitation.
Claim 3	
3. In a microprocessor integrated circuit,	The Richter reference (U.S. Patent No. 4,853,841) teaches a "microprocessor system 2" that is contemplated to provide the functions of a microprocessor, RAM, ROM, a serial interface, and a parallel interface where "in a one-chip system." *(Appendix D, col. 2, lines 55-65).*

Claim Limitation	Teaching of the Richter Reference
	 *(Appendix D, Figure 2).*
a method for clocking the microprocessor within the integrated circuit, comprising the steps of: providing an entire ring oscillator system clock	Richter teaches that a "voltage-controlled oscillator generates a clock pulse 'ftakt' that acts upon the microprocessor system." *(Appendix D, col. 3, lines 18-20).* In some embodiments the 'ftakt' signal is used as both the system clock and a clock for the I/O port. *(Appendix D, col. 4, lines 34-43).* In other embodiments Richter teaches that the microprocessor is clocked by a "separate system clock generator for the microprocessor 2." *(Appendix D, col. 4, lines 34-38).* It is inherent to use a second, voltage controlled oscillator as the separate system clock generator because Richter already teaches clocking the microprocessor with a voltage controlled oscillator in a different embodiment. The Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). The Requester notes that the functionality of prior art processors are the same in material respect to commercial processors referred to by the Patent Owner in the above mentioned communications to third parties. Therefore, such an allegation, if true with respect to today's processors, would also be true with regard to the processor taught by Richter. Accordingly, if the office accepts this premise, one skilled in the art would have understood Richter to disclose a ring oscillator for clocking

Claim Limitation	Teaching of the Richter Reference
	the central processing unit. Further, Richter teaches that the voltage-controlled oscillator may be provided in the one-chip microprocessor system. Specifically, "[t]he first microprocessor system 2 is, for example, set up in a configuration comprising the microprocessor, volatile (RAM) and nonvolatile (ROM) memory chips, the serial interface and parallel input/output chips as well as other chips required for their operation. It is also contemplated to provide all these functions in a one-chip system." *(Appendix D, col. 2, lines 59-66)*. The voltage-controlled oscillator, along with most of the other components displayed in Figure 2, are required for the operation of the microprocessor, and thus Richter teaches providing them on the one-chip system.
constructed of electronic devices within the integrated circuit,	One skilled in the art would understand the on-chip oscillator circuit and the main control logic to include a plurality of electronic devices. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.
said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;	Richter teaches implementing the microprocessor "in a one-chip system." *(Appendix D, col. 2, lines 55-65)*, which would necessarily be constructed by a single process technology. This indicates that the oscillator is fabricated on the same chip as the CPU and that the oscillator and CPU would therefore be constructed by the same process technology. *(Appendix F, page III-114)* It is noteworthy that the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6)*. Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to

Claim Limitation	Teaching of the Richter Reference
	naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6.)*
using the ring oscillator system clock for clocking the microprocessor,	The voltage-controlled oscillator taught by Richter is used to clock the microprocessor as described above.
said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;	The Patent Owner has stated in correspondence to various third parties that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6.)*
providing an on chip input/output interface for the microprocessor integrated circuit; and	Richter teaches that the "microprocessor system 2 has a serial interface (not shown) which is connected by the input/output port 7 to a signal line 8 of the serial bus system 6." *(Appendix D, col. 2, lines 55-58).*
clocking the input/output interface with a second clock independent of the ring oscillator system clock,	Richter teaches a signal "ftakt" for clocking the serial I/O port of the microprocessor that is independent of the CPU clock: "the data transmission of the serial interface is supplied with the clock frequency signal 'ftakt', and the microprocessor of the microprocessor system 2 is equipped with its own system clock generator." *(Col. 4, lines 34-43 and 58-62)* Richter describes the system clock as a "separate system clock generator for the microprocessor" that is independent of the I/O clock signal. *(Col. 4, lines 36-47)*

Claim Limitation	Teaching of the Richter Reference
	Additionally, the Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8).* As previously described, Richter clearly teaches a serial interface. If the Patent Owner's assertions are true today as to commercial processors, then they are also true as to the prior art processors. In any case, Requestor notes that the use of a second independent clock for providing clocking signals to an I/O interface was commonplace at the time of filing. *(See, e.g., US Patent Nos. 4,443,845 (col. 17, lines 1-42; figs. 14A-14B); 4,409,665 (col. 5, lines 46-6, lines 41; fig. 3c); 4,053,946 (col. 34, lines 15-31); 4,868,784 (col. 25, Table I, "Serial-clock control"); 5,142,637 (col. 6, line 59 to col. 7, line 5; col. 7, line 63 to col. 8, line 2; Figs. 12 & 13)).*
Claim 4	
4. The method of claim 3 in which the second clock is a fixed frequency clock.	Richter teaches that "[t]he division ratio 1/M at the second frequency divider 24 is fixed. It determines the frequency increments by which the clock frequency signal 'ftakt' can be adjusted. It is fixed such that by means of a programmable, integer value of N, a suitable clock frequency 'ftakt' is adjusted. From this adjusted clock frequency 'ftakt', the desired transmission speeds v' can be derived with a required precision by integer division so that the microprocessor system can therefore be synchronized with the communication partner." *(Col. 4, lines 10-19)* One skilled in the art would understand that if the communication partner operates at a fixed frequency, the clock signal 'ftakt' would be a fixed frequency clock signal. The clock signal 'ftakt" taught by Richter is based on "clock frequency input 23." *(Col. 3, lines 18-20).* Requester notes that use of a fixed frequency clock as a clock input was well known in the art at the time of filing. *(See, e.g., the Mostek reference (Appendix F, page III-109);US 4,893,271 (col. 1, lines 17-18); US 4,751,565 (col. 1, lines 50-52); US 4,947,411 (Abstract); US 5,050,195 (Abstract); US 4,835,491 (col. 2, lines 24-25))* Additionally, the Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8).* If the Patent Owner's assertions are accepted, one skilled in the art would recognize that the incoming signal to the serial interface could be of fixed frequency, teaching the features of this limitation.
Claim 5	

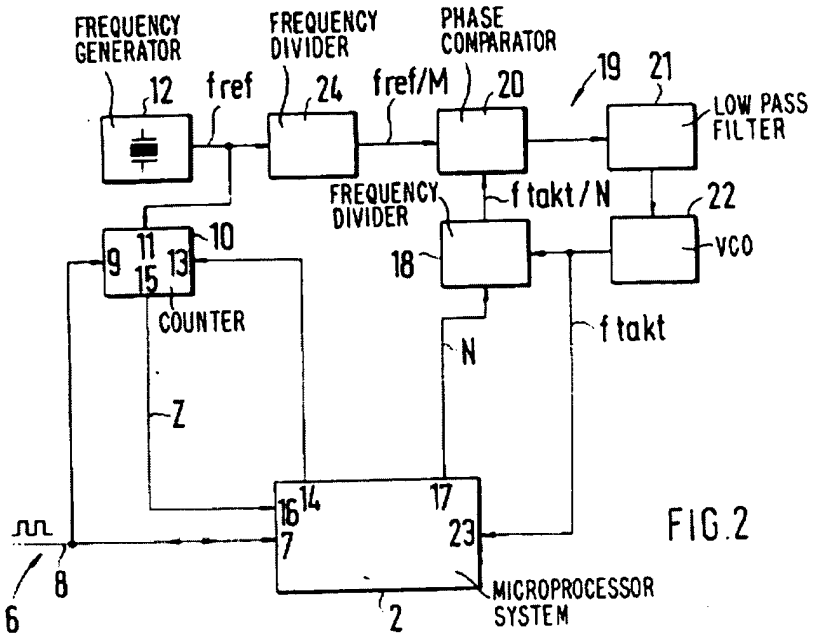
Claim Limitation	Teaching of the Richter Reference
5. The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.	As described in the teachings corresponding to Claim 1, a voltage controlled oscillator is taught as a "separate system clock generator for the microprocessor 2." *(Appendix D, col. 4, lines 34-38).* One skilled in the art would understand that information is transferred to and from the microprocessor in synchrony with the microprocessor's system clock.
Claim 6	
6. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate,	The Richter reference (U.S. Patent No. 4,853,841) teaches a "microprocessor system 2" that is contemplated to provide the functions of a microprocessor, RAM, ROM, a serial interface, and a parallel interface where "in a one-chip system." *(Appendix D, col. 2, lines 55-65).*  FIG.2 *(Appendix D, Figure 2).* Richter teaches that the "microprocessor system" includes a "microprocessor." *(Appendix D, col. 2, lines 55-65).*
said central processing unit operating at a processing frequency	Richter teaches that a "voltage-controlled oscillator generates a clock pulse 'ftakt' that acts upon the microprocessor system." *(Appendix D, col. 3, lines 18-20).* In some embodiments the 'ftakt' signal is used as both the system clock and a clock for the I/O port. *(Appendix D, col. 4, lines 34-43).*

Claim Limitation	Teaching of the Richter Reference
	In other embodiments Richter teaches that the microprocessor is clocked by a "separate system clock generator for the microprocessor 2." *(Appendix D, col. 4, lines 34-38).* It is inherent to use a second, voltage controlled oscillator as the separate system clock generator because Richter already teaches clocking the microprocessor with a voltage controlled oscillator in a different embodiment. The microprocessor operates at the frequency of the oscillator.
and being constructed of a first plurality of electronic devices;	One skilled in the art would understand the on-chip oscillator circuit and the main control logic to include a plurality of electronic devices. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and	Richter teaches that a "voltage-controlled oscillator generates a clock pulse 'ftakt' that acts upon the microprocessor system." *(Appendix D, col. 3, lines 18-20).* In some embodiments the 'ftakt' signal is used as both the system clock and a clock for the I/O port. *(Appendix D, col. 4, lines 34-43).* In other embodiments Richter teaches that the microprocessor is clocked by a "separate system clock generator for the microprocessor 2." *(Appendix D, col. 4, lines 34-38).* It is inherent to use a second, voltage controlled oscillator as the separate system clock generator because Richter already teaches clocking the microprocessor with a voltage controlled oscillator in a different embodiment. The microprocessor operates at the frequency of the oscillator.
being constructed of a second plurality of electronic devices,	One skilled in the art would understand the on-chip oscillator circuit and the main control logic to include a plurality of electronic devices. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a	Richter teaches implementing the microprocessor "in a one-chip system." *(Appendix D, col. 2, lines 55-65)*, which would necessarily be constructed by a single process technology. This indicates that the oscillator is fabricated on the same chip as the CPU and that the oscillator and CPU would therefore be constructed by the same process technology. *(Appendix F, page III-114)* It is noteworthy that the Patent Owner has stated in correspondence to

Claim Limitation	Teaching of the Richter Reference
function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6.)*
an on-chip input/output interface, connected between said said [sic] central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	Richter teaches that the "microprocessor system 2 has a serial interface (not shown) which is connected by the input/output port 7 to a signal line 8 of the serial bus system 6." *(Appendix D, col. 2, lines 55-58).* Richter teaches that the serial interface is connected to other microprocessor systems which contain various types of memory. *(Appendix D, col. 2, lines 32-68).*
an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	Richter teaches a signal "ftakt" for clocking the serial I/O port of the microprocessor that is independent of the CPU clock: "the data transmission of the serial interface is supplied with the clock frequency signal 'ftakt', and the microprocessor of the microprocessor system 2 is equipped with its own system clock generator." *(Col. 4, lines 34-43 and 58-62)* Richter describes the system clock as a "separate system clock generator for the microprocessor" that is independent of the I/O clock signal. *(Col. 4, lines 36-47)* Additionally, the Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second

Claim Limitation	Teaching of the Richter Reference
	independent clock. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8).* As previously described, Richter clearly teaches a serial interface. If the Patent Owner's assertions are true today as to commercial processors, then they are also true as to the prior art processors. In any case, Requestor notes that the use of a second independent clock for providing clocking signals to an I/O interface was commonplace at the time of filing. *(See, e.g., US Patent Nos. 4,443,845 (col. 17, lines 1-42; figs. 14A-14B); 4,409,665 (col. 5, lines 46-6, lines 41; fig. 3c); 4,053,946 (col. 34, lines 15-31); 4,868,784 (col. 25, Table I, "Serial-clock control"); 5,142,637 (col. 6, line 59 to col. 7, line 5; col. 7, line 63 to col. 8, line 2; Figs. 12 & 13)).*
Claim 7	
7. The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	It is noteworthy that the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6.)*
Claim 8	
8. The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said	Richter teaches that "[t]he division ratio 1/M at the second frequency divider 24 is fixed. It determines the frequency increments by which the clock frequency signal 'ftakt' can be adjusted. It is fixed such that by means of a programmable, integer value of N, a suitable clock frequency 'ftakt' is adjusted. From this adjusted clock frequency 'ftakt', the desired transmission speeds v' can be derived with a required precision by integer division so that the microprocessor system can therefore be synchronized with the communication partner." (Col. 4, lines 10-19) One skilled in the

Claim Limitation	Teaching of the Richter Reference
oscillator.	art would understand that if the communication partner operates at a fixed frequency, the clock signal 'ftakt' would be a fixed frequency clock signal. The clock signal 'ftakt" taught by Richter is based on "clock frequency input 23." (Col. 3, lines 18-20). Requester notes that use of a fixed frequency clock as a clock input was well known in the art at the time of filing. (See, e.g., the Mostek reference (Appendix F, page III-109);US 4,893,271 (col. 1, lines 17-18); US 4,751,565 (col. 1, lines 50-52); US 4,947,411 (Abstract); US 5,050,195 (Abstract); US 4,835,491 (col. 2, lines 24-25)) Additionally, the Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. (Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8). If the Patent Owner's assertions are accepted, one skilled in the art would recognize that the incoming signal to the serial interface could be of fixed frequency, teaching the features of this limitation. Richter teaches one embodiment where the system reaches a point of equilibrium so that frequency of the voltage controlled oscillator is synchronous to the frequency of the serial data transmission. *(Appendix D, Abstract)*.
Claim 9	
9. The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	The Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). The Requester notes that the functionality of prior art processors are the same in material respect to commercial processors referred to by the Patent Owner in the above mentioned communications to third parties. Therefore, such an allegation, if true with respect to today's processors, would also be true with regard to the processor taught by Richter. Accordingly, if the office accepts this premise, one skilled in the art would have understood Richter to disclose a ring oscillator for clocking the central processing unit.
Claim 10	
10. In a microprocessor	The Richter reference (U.S. Patent No. 4,853,841) teaches a "microprocessor system 2" that is contemplated to provide the functions

Claim Limitation	Teaching of the Richter Reference
system including a central processing unit, a method for clocking said central processing unit comprising the steps of:	of a microprocessor, RAM, ROM, a serial interface, and a parallel interface where "in a one-chip system." *(Appendix D, col. 2, lines 55-65).*  FIG.2 *(Appendix D, Figure 2).* Richter teaches that the "microprocessor system" includes a "microprocessor." *(Appendix D, col. 2, lines 55-65).*
providing said central processing unit upon an integrated circuit substrate,	Richter teaches a microprocessor system implemented as a "one-chip system" as described above.
said central processing unit being constructed of a first plurality of transistors and	One skilled in the art would understand the on-chip oscillator circuit and the main control logic to include a plurality of transistors. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of transistors.
being operative at a processing frequency;	Richter teaches that a "voltage-controlled oscillator generates a clock pulse 'ftakt' that acts upon the microprocessor system." *(Appendix D, col. 3, lines 18-20).* In some embodiments the 'ftakt' signal is used as both the system clock and a clock for the I/O port. *(Appendix D, col. 4, lines 34-43).* In other embodiments Richter teaches that the microprocessor is clocked

Claim Limitation	Teaching of the Richter Reference
	by a "separate system clock generator for the microprocessor 2." *(Appendix D, col. 4, lines 34-38).* It is inherent to use a second, voltage controlled oscillator as the separate system clock generator because Richter already teaches clocking the microprocessor with a voltage controlled oscillator in a different embodiment. The microprocessor operates at the frequency of the oscillator.
providing an entire variable speed clock disposed upon said integrated circuit substrate,	Richter teaches that a "voltage-controlled oscillator generates a clock pulse 'ftakt' that acts upon the microprocessor system." *(Appendix D, col. 3, lines 18-20).* In some embodiments the 'ftakt' signal is used as both the system clock and a clock for the I/O port. *(Appendix D, col. 4, lines 34-43).* In other embodiments Richter teaches that the microprocessor is clocked by a "separate system clock generator for the microprocessor 2." *(Appendix D, col. 4, lines 34-38).* It is inherent to use a second, voltage controlled oscillator as the separate system clock generator because Richter already teaches clocking the microprocessor with a voltage controlled oscillator in a different embodiment. The microprocessor operates at the frequency of the oscillator.
said variable speed clock being constructed of a second plurality of transistors;	One skilled in the art would understand the on-chip oscillator circuit and the main control logic to include a plurality of transistors. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of transistors.
clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock	Richter teaches that a "voltage-controlled oscillator generates a clock pulse 'ftakt' that acts upon the microprocessor system." *(Appendix D, col. 3, lines 18-20).* In some embodiments the 'ftakt' signal is used as both the system clock and a clock for the I/O port. *(Appendix D, col. 4, lines 34-43).* In other embodiments Richter teaches that the microprocessor is clocked by a "separate system clock generator for the microprocessor 2." *(Appendix D, col. 4, lines 34-38).* It is inherent to use a second, voltage controlled oscillator as the separate system clock generator because Richter already teaches clocking the microprocessor with a voltage controlled oscillator in a different embodiment. The microprocessor operates at the frequency of the oscillator.
at a variable frequency dependent upon variation in one or more fabrication or	Richter teaches implementing the microprocessor "in a one-chip system." *(Appendix D, col. 2, lines 55-65),* which would necessarily be constructed by a single process technology. This indicates that the oscillator is fabricated on the same chip as the CPU and that the oscillator and CPU would

Claim Limitation	Teaching of the Richter Reference
operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	therefore be constructed by the same process technology. *(Appendix F, page III-114)* It is noteworthy that the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6.)*
connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	Richter teaches that the "microprocessor system 2 has a serial interface (not shown) which is connected by the input/output port 7 to a signal line 8 of the serial bus system 6." *(Appendix D, col. 2, lines 55-58).* Richter teaches that the serial interface is connected to other microprocessor systems which contain various types of memory. *(Appendix D, col. 2, lines 32-68).*
clocking said input/output interface using an external clock wherein said external clock is operative at a	Richter teaches a signal "ftakt" for clocking the serial I/O port of the microprocessor that is independent of the CPU clock: "the data transmission of the serial interface is supplied with the clock frequency signal 'ftakt', and the microprocessor of the microprocessor system 2 is equipped with its own system clock generator." *(col. 4, lines 34-43 and 58-62)* Richter describes the system clock as a "separate system clock

Claim Limitation	Teaching of the Richter Reference
frequency independent of a clock frequency of said variable speed clock.	generator for the microprocessor" that is independent of the I/O clock signal. *(col. 4, lines 36-47)* Additionally, the Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8).* As previously described, Richter clearly teaches a serial interface. If the Patent Owner's assertions are true today as to commercial processors, then they are also true as to the prior art processors. In any case, Requestor notes that the use of a second independent clock for providing clocking signals to an I/O interface was commonplace at the time of filing. *(See, e.g., US Patent Nos. 4,443,845 (col. 17, lines 1-42; figs. 14A-14B); 4,409,665 (col. 5, lines 46-6, lines 41; fig. 3c); 4,053,946 (col. 34, lines 15-31); 4,868,784 (col. 25, Table I, "Serial-clock control"); 5,142,637 (col. 6, line 59 to col. 7, line 5; col. 7, line 63 to col. 8, line 2; Figs. 12 & 13)).*

From the foregoing chart, it can be seen that claims 1-10 are anticipated by Richter. Thus, claims 1-10 are unpatentable as being anticipated under 35 U.S.C. § 102(b).

C. SNQ #7: The Richter Reference, in Light of the Ledzius Reference Renders Obvious Claims 6, 7 and 10 of the '336 Patent

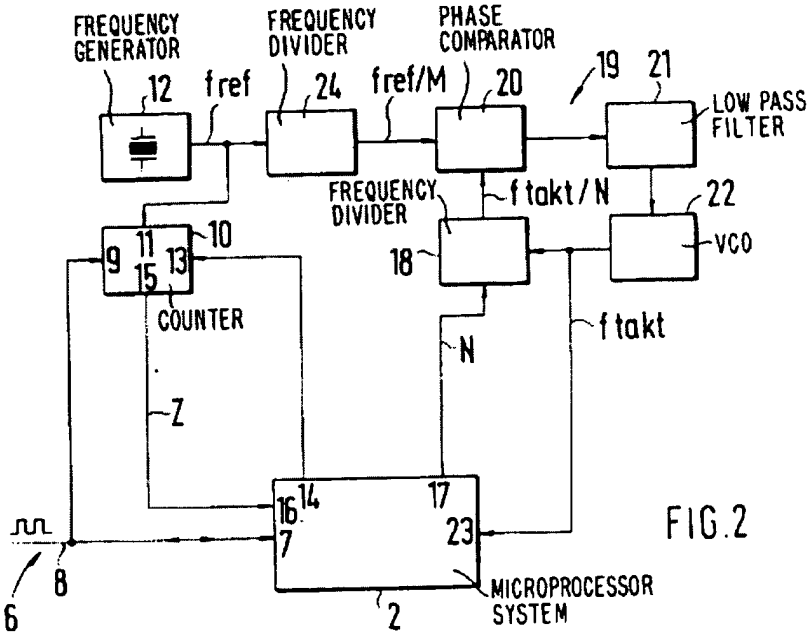
In addition to the manner of applying the Richter reference to claims 1-10 of the '336 patent outlined above, the Richter reference, when viewed in light of the Ledzius reference, further renders obvious several of the limitations of claims 6, 7, and 10 already taught by Richter.

It would have been obvious to one skilled in the art to modify the teachings of the Richter reference to use the "same batch and section of semiconductor wafer" in order to create corresponding manufacturing variations, as recited by the independent claims of the '336 patent. *(Appendix I, col. 4, lines 11-12).* This is because the Ledzius reference, which so teaches, is also an integrated circuit with a CPU and an on-chip clock. *(Appendix I, Abstract).*

It would have been obvious to one skilled in the art to modify the teachings of the Richter reference so that the "frequency of the clock signal produced by [the clock generator]

varies to reflect process and temperature variances," as recited by the independent claims of the '336 patent. *(Appendix I, col. 4, lines 9-14).* This is because it would have been obvious to create the circuit of Richter from the "same batch and section of semiconductor wafer" as taught by Ledzius. *(Id.)*

A detailed explanation of the pertinency and manner of applying the Richter and Ledzius references to claims 6, 7, and 10 of the '336 patent is shown in the following claim chart.

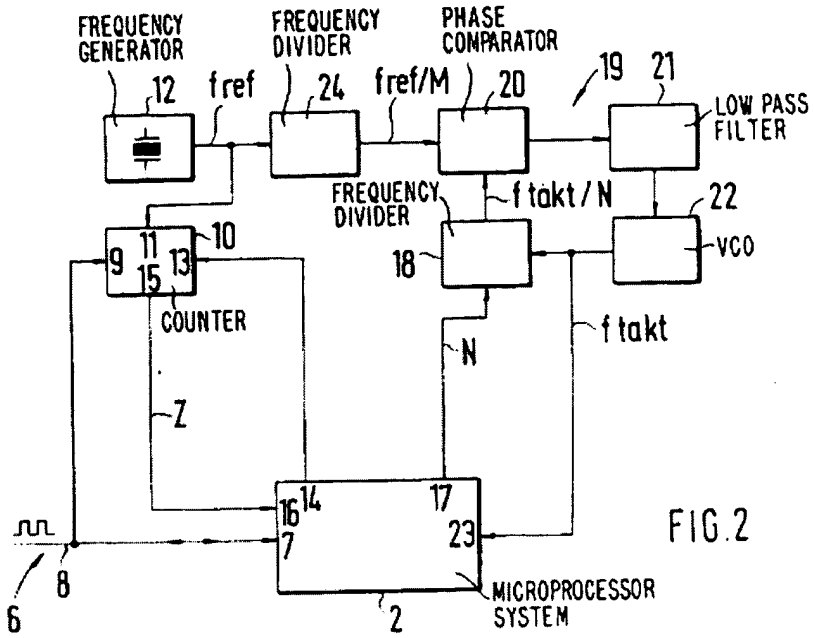
Claim Limitation Claim 6	Richter in combination with Ledzius
6. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate,	The Richter reference (U.S. Patent No. 4,853,841) teaches a "microprocessor system 2" that is contemplated to provide the functions of a microprocessor, RAM, ROM, a serial interface, and a parallel interface where "in a one-chip system." *(Appendix D, col. 2, lines 55-65).*  FIG.2 *(Appendix D, Figure 2).* Richter teaches that the "microprocessor system" includes a "microprocessor." *(Appendix D, col. 2, lines 55-65).*
said central processing unit operating at a processing frequency	Richter teaches that a "voltage-controlled oscillator generates a clock pulse 'ftakt' that acts upon the microprocessor system." *(Appendix D, col. 3, lines 18-20).* In some embodiments the 'ftakt' signal is used as both the system clock and a clock for the I/O port. *(Appendix D, col. 4, lines 34-43).* In other embodiments Richter teaches that the microprocessor is clocked

Claim Limitation	Richter in combination with Ledzius
	by a "separate system clock generator for the microprocessor 2." *(Appendix D, col. 4, lines 34-38).* It is inherent to use a second, voltage controlled oscillator as the separate system clock generator because Richter already teaches clocking the microprocessor with a voltage controlled oscillator in a different embodiment. The microprocessor operates at the frequency of the oscillator.
and being constructed of a first plurality of electronic devices;	One skilled in the art would understand the on-chip oscillator circuit and the main control logic to include a plurality of electronic devices. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and	Richter teaches that a "voltage-controlled oscillator generates a clock pulse 'ftakt' that acts upon the microprocessor system." *(Appendix D, col. 3, lines 18-20).* In some embodiments the 'ftakt' signal is used as both the system clock and a clock for the I/O port. *(Appendix D, col. 4, lines 34-43).* In other embodiments Richter teaches that the microprocessor is clocked by a "separate system clock generator for the microprocessor 2." *(Appendix D, col. 4, lines 34-38).* It is inherent to use a second, voltage controlled oscillator as the separate system clock generator because Richter already teaches clocking the microprocessor with a voltage controlled oscillator in a different embodiment. The microprocessor operates at the frequency of the oscillator.
being constructed of a second plurality of electronic devices,	One skilled in the art would understand the on-chip oscillator circuit and the main control logic to include a plurality of electronic devices. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter	Richter teaches implementing the microprocessor "in a one-chip system." *(Appendix D, col. 2, lines 55-65)*, which would necessarily be constructed by a single process technology. This indicates that the oscillator is fabricated on the same chip as the CPU and that the oscillator and CPU would therefore be constructed by the same process technology. *(Appendix F, page III-114)* It is noteworthy that the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an

Claim Limitation	Richter in combination with Ledzius
variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6.)* As an aside, Requestor notes that this feature was commonplace at the time of filing, as shown by U.S. Patent No. 4,691,124 to Ledzius et al. Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in process variations throughout the circuit. *(Appendix I, col. 4, lines 11-12).* One skilled in the art would have found an apparent reason to combine Ledzius with Richter, namely to produce the processor of Richter with minimal cost and defects. Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in frequency variations due to process and temperature variations throughout the circuit. *(Appendix I, col. 4, lines 3-21).* Richter contemplates providing all the chips required for the microprocessor's functioning on a "one-chip system." *(Appendix D, col. 2, lines 59-66).* One skilled in the art would have found an apparent reason to combine Ledzius with Richter, namely to produce the one-chip system of Richter with minimal cost and defects.
an on-chip input/output interface, connected between said said [sic] central processing unit and an external memory bus, for facilitating exchanging coupling	Richter teaches that the "microprocessor system 2 has a serial interface (not shown) which is connected by the input/output port 7 to a signal line 8 of the serial bus system 6." *(Appendix D, col. 2, lines 55-58).* Richter teaches that the serial interface is connected to other microprocessor systems which contain various types of memory. *(Appendix D, col. 2, lines 32-68).*

Claim Limitation	Richter in combination with Ledzius
control signals, addresses and data with said central processing unit; and	
an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	Richter teaches a signal "ftakt" for clocking the serial I/O port of the microprocessor that is independent of the CPU clock: "the data transmission of the serial interface is supplied with the clock frequency signal 'ftakt', and the microprocessor of the microprocessor system 2 is equipped with its own system clock generator." *(Col. 4, lines 34-43 and 58-62)* Richter describes the system clock as a "separate system clock generator for the microprocessor" that is independent of the I/O clock signal. *(Col. 4, lines 36-47)* Additionally, the Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8)*. As previously described, Richter clearly teaches a serial interface. If the Patent Owner's assertions are true today as to commercial processors, then they are also true as to the prior art processors. In any case, Requestor notes that the use of a second independent clock for providing clocking signals to an I/O interface was commonplace at the time of filing. *(See, e.g., US Patent Nos. 4,443,845 (col. 17, lines 1-42; figs. 14A-14B); 4,409,665 (col. 5, lines 46-6, lines 41; fig. 3c); 4,053,946 (col. 34, lines 15-31); 4,868,784 (col. 25, Table I, "Serial-clock control"); 5,142,637 (col. 6, line 59 to col. 7, line 5; col. 7, line 63 to col. 8, line 2; Figs. 12 & 13)).*
Claim 7	
7. The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	It is noteworthy that the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated

Claim Limitation	Richter in combination with Ledzius
	that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6.)* As an aside, Requestor notes that this feature was commonplace at the time of filing, as shown by U.S. Patent No. 4,691,124 to Ledzius et al. Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in process variations throughout the circuit. *(Appendix I, col. 4, lines 11-12).* One skilled in the art would have found an apparent reason to combine Ledzius with Richter, namely to produce the processor of Richter with minimal cost and defects. Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in frequency variations due to process and temperature variations throughout the circuit. *(Appendix I, col. 4, lines 3-21).* Richter contemplates providing all the chips required for the microprocessor's functioning on a "one-chip system." *(Appendix D, col. 2, lines 59-66).* One skilled in the art would have found an apparent reason to combine Ledzius with Richter, namely to produce the one-chip system of Richter with minimal cost and defects.
Claim 10	
10. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:	The Richter reference (U.S. Patent No. 4,853,841) teaches a "microprocessor system 2" that is contemplated to provide the functions of a microprocessor, RAM, ROM, a serial interface, and a parallel interface where "in a one-chip system." *(Appendix D, col. 2, lines 55-65).*

Claim Limitation	Richter in combination with Ledzius
	 FIG.2 *(Appendix D, Figure 2).* Richter teaches that the "microprocessor system" includes a "microprocessor." *(Appendix D, col. 2, lines 55-65).*
providing said central processing unit upon an integrated circuit substrate,	Richter teaches a microprocessor system implemented as a "one-chip system" as described above.
said central processing unit being constructed of a first plurality of transistors and	One skilled in the art would understand the on-chip oscillator circuit and the main control logic to include a plurality of transistors. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of transistors.
being operative at a processing frequency;	Richter teaches that a "voltage-controlled oscillator generates a clock pulse 'ftakt' that acts upon the microprocessor system." *(Appendix D, col. 3, lines 18-20).* In some embodiments the 'ftakt' signal is used as both the system clock and a clock for the I/O port. *(Appendix D, col. 4, lines 34-43).* In other embodiments Richter teaches that the microprocessor is clocked by a "separate system clock generator for the microprocessor 2." *(Appendix D, col. 4, lines 34-38).* It is inherent to use a second, voltage controlled oscillator as the separate system clock generator because

Claim Limitation	Richter in combination with Ledzius
	Richter already teaches clocking the microprocessor with a voltage controlled oscillator in a different embodiment. The microprocessor operates at the frequency of the oscillator.
providing an entire variable speed clock disposed upon said integrated circuit substrate,	Richter teaches that a "voltage-controlled oscillator generates a clock pulse 'ftakt' that acts upon the microprocessor system." *(Appendix D, col. 3, lines 18-20)*. In some embodiments the 'ftakt' signal is used as both the system clock and a clock for the I/O port. *(Appendix D, col. 4, lines 34-43)*. In other embodiments Richter teaches that the microprocessor is clocked by a "separate system clock generator for the microprocessor 2." *(Appendix D, col. 4, lines 34-38)*. It is inherent to use a second, voltage controlled oscillator as the separate system clock generator because Richter already teaches clocking the microprocessor with a voltage controlled oscillator in a different embodiment. The microprocessor operates at the frequency of the oscillator.
said variable speed clock being constructed of a second plurality of transistors;	One skilled in the art would understand the on-chip oscillator circuit and the main control logic to include a plurality of transistors. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of transistors.
clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock	Richter teaches that a "voltage-controlled oscillator generates a clock pulse 'ftakt' that acts upon the microprocessor system." *(Appendix D, col. 3, lines 18-20)*. In some embodiments the 'ftakt' signal is used as both the system clock and a clock for the I/O port. *(Appendix D, col. 4, lines 34-43)*. In other embodiments Richter teaches that the microprocessor is clocked by a "separate system clock generator for the microprocessor 2." *(Appendix D, col. 4, lines 34-38)*. It is inherent to use a second, voltage controlled oscillator as the separate system clock generator because Richter already teaches clocking the microprocessor with a voltage controlled oscillator in a different embodiment. The microprocessor operates at the frequency of the oscillator.
at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said	Richter teaches implementing the microprocessor "in a one-chip system." *(Appendix D, col. 2, lines 55-65)*, which would necessarily be constructed by a single process technology. This indicates that the oscillator is fabricated on the same chip as the CPU and that the oscillator and CPU would therefore be constructed by the same process technology. *(Appendix F, page III-114)*

Claim Limitation	Richter in combination with Ledzius
integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	It is noteworthy that the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6.)* As an aside, Requestor notes that this feature was commonplace at the time of filing, as shown by U.S. Patent No. 4,691,124 to Ledzius et al. Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in process variations throughout the circuit. *(Appendix I, col. 4, lines 11-12).* One skilled in the art would have found an apparent reason to combine Ledzius with Richter, namely to produce the processor of Richter with minimal cost and defects. Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in frequency variations due to process and temperature variations throughout the circuit. *(Appendix I, col. 4, lines 3-21).* Richter contemplates providing all the chips required for the microprocessor's functioning on a "one-chip system." *(Appendix D, col. 2, lines 59-66).* One skilled in the art would have found an apparent reason to combine Ledzius with Richter, namely to produce the one-chip system of Richter with minimal cost and defects.
connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging	Richter teaches that the "microprocessor system 2 has a serial interface (not shown) which is connected by the input/output port 7 to a signal line 8 of the serial bus system 6." *(Appendix D, col. 2, lines 55-58).* Richter teaches that the serial interface is connected to other microprocessor systems which contain various types of memory. *(Appendix D, col. 2, lines 32-68).*

Claim Limitation	Richter in combination with Ledzius
coupling control signals, addresses and data between said input/output interface and said central processing unit; and	
clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said variable speed clock.	Richter teaches a signal "ftakt" for clocking the serial I/O port of the microprocessor that is independent of the CPU clock: "the data transmission of the serial interface is supplied with the clock frequency signal 'ftakt', and the microprocessor of the microprocessor system 2 is equipped with its own system clock generator." *(col. 4, lines 34-43 and 58-62)* Richter describes the system clock as a "separate system clock generator for the microprocessor" that is independent of the I/O clock signal. *(col. 4, lines 36-47)* Additionally, the Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8)*. As previously described, Richter clearly teaches a serial interface. If the Patent Owner's assertions are true today as to commercial processors, then they are also true as to the prior art processors. In any case, Requestor notes that the use of a second independent clock for providing clocking signals to an I/O interface was commonplace at the time of filing. *(See, e.g., US Patent Nos. 4,443,845 (col. 17, lines 1-42; figs. 14A-14B); 4,409,665 (col. 5, lines 46-6, lines 41; fig. 3c); 4,053,946 (col. 34, lines 15-31); 4,868,784 (col. 25, Table I, "Serial-clock control"); 5,142,637 (col. 6, line 59 to col. 7, line 5; col. 7, line 63 to col. 8, line 2; Figs. 12 & 13))*.

From the foregoing chart, it can be seen that claims 6, 7, and 10 are rendered obvious by Richter in combination with Ledzius. Thus, claims 6, 7, and 10 are unpatentable as being obvious under U.S.C. § 103 by the Richter reference in combination with the Ledzius reference.

D. SNQ #8: The Richter Reference, in Light of the Ledzius and Kato References, Renders Obvious Claims 8 and 9 of the '336 Patent

In addition to Richter's anticipation of claims 8 and 9 of the '336 patent described above, the Ledzius and Kato references, when viewed in light of the Richter reference, further render obvious several of the limitations already taught by Richter.

It would have been obvious to one skilled in the art to modify the teachings of the Richter reference to use a ring oscillator variable speed system clock as the internal oscillator, as recited by the independent claims of the '336 patent. This is because such use of a ring oscillator is taught by the Kato reference, which, similar to Richter, describes a single integrated circuit containing a central processing unit and an oscillator. *(Appendix H, col. 10, lines 65 through 11, lines 7).* One skilled in the art would realize the benefits of implementing Kato's ring oscillator as Richter's variable oscillator to reduce power consumption during periods of lessened processing demand and to increase clock speed (and power consumption) during periods of increased processing demand. *(Appendix H, col. 11, lines 2-7).*

A detailed explanation of the pertinency and manner of applying the Richter, Ledzius, and Kato references to claims 8 and 9 of the '336 patent is shown in the following claim chart.

Claim Limitation Claim 8	Richter in combination with Ledzius and Kato
8. The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.	As detailed in the above claim chart, claim 6 is rendered obvious by Richter in view Ledzius. Richter teaches that "[t]he division ratio 1/M at the second frequency divider 24 is fixed. It determines the frequency increments by which the clock frequency signal 'ftakt' can be adjusted. It is fixed such that by means of a programmable, integer value of N, a suitable clock frequency 'ftakt' is adjusted. From this adjusted clock frequency 'ftakt', the desired transmission speeds v' can be derived with a required precision by integer division so that the microprocessor system can therefore be synchronized with the communication partner." (Col. 4, lines 10-19) One skilled in the art would understand that if the communication partner operates at a fixed frequency, the clock signal 'ftakt' would be a fixed frequency clock signal. The clock signal 'ftakt" taught by Richter is based on "clock frequency input 23." (Col. 3, lines 18-20). Requester notes that use of a fixed frequency clock as a clock input was well known in the art at the time of filing. (See,

Claim Limitation	Richter in combination with Ledzius and Kato
	e.g., the Mostek reference (Appendix F, page III-109);US 4,893,271 (col. 1, lines 17-18); US 4,751,565 (col. 1, lines 50-52); US 4,947,411 (Abstract); US 5,050,195 (Abstract); US 4,835,491 (col. 2, lines 24-25)) Additionally, the Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. (Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8). If the Patent Owner's assertions are accepted, one skilled in the art would recognize that the incoming signal to the serial interface could be of fixed frequency, teaching the features of this limitation. Richter teaches one embodiment where the system reaches a point of equilibrium so that frequency of the voltage controlled oscillator is synchronous to the frequency of the serial data transmission. *(Appendix D, Abstract).* As an aside, the Requester notes that this limitation is also taught by Kato. Kato teaches a microprocessor system having two clock. The first clock generator clocks the CPU and the second clock generator is connected to the I/O port. *(Appendix H, col. 4, lines 37-42 and FIG. 4)* Kato teaches that the first and second clock generators operate synchronously: "second clock generator 15 produces two clock signals ϕa and ϕb... Signals ϕa and ϕb are produced in synchronism with the signal from first clock generator 14." *(Appendix H, col. 4, lines 56-60)* As explained above, one skilled in the art would have found an apparent reason to combine the teachings of Kato and Mostek, namely to provide Mostek with a ring oscillator to reduce power consumption during periods of lessened processing demand and to increase clock speed (and power consumption) during periods of increased processing demand. *(Appendix H, col. 11, lines 2-7).*
Claim 9	
9. The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	As detailed in the above claim chart, claim 6 is rendered obvious by Richter in view Ledzius. The Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). The Requester notes that the functionality of prior art processors are the same in material respect to commercial processors referred to by the Patent Owner in the above mentioned communications

Claim Limitation	Richter in combination with Ledzius and Kato
	to third parties. Therefore, such an allegation, if true with respect to today's processors, would also be true with regard to the processor taught by Richter. Accordingly, if the office accepts this premise, one skilled in the art would have understood Richter to disclose a ring oscillator for clocking the central processing unit. Alternatively, this feature is obvious in view of U. S. Patent No. 4,766,567 to Kato ("Kato"). Kato describes a ring oscillator that can be used to supply clock signals for the CPU described in Richter. *(Appendix H, col. 10, line 64 to col. 11, line 7).* One skilled in the art would have seen an apparent reason to implement Kato's ring oscillator as the voltage controlled oscillator or separate system clock of Richter, namely because a ring oscillator is an obvious selection for an internal oscillator and Richter already teaches the use of a voltage controlled oscillator to clock the microprocessor. One skilled in the art would realize the benefits of implementing Kato's ring oscillator as Richter's variable oscillator to reduce power consumption during periods of lessened processing demand and to increase clock speed (and power consumption) during periods of increased processing demand. *(Appendix H, col. 11, lines 2-7).*

From the foregoing chart, it can be seen that claims 8 and 9 are rendered obvious by Richter in combination with Ledzius and Kato. Thus, claims 8 and 9 are unpatentable as being obvious under U.S.C. § 103 by the Richter reference in combination with the Ledzius and Kato references.

E. SNQ #9: The Richter Reference, in Light of the Ledzius, Kato, and McDermott References, Renders Obvious Claims 1-5 of the '336 Patent

In addition to Richter's anticipation of claims 1-5 of the '336 patent described above, the Ledzius, Kato, and McDermott references, when viewed in light of the Richter reference, further render obvious several of the limitations already taught by Richter.

It would have been obvious for one skilled in the art to modify the teachings of Richter so that a voltage controlled oscillator that clocks the microprocessor was included on the one-chip system, as recited by the independent '336 claims. This is because U.S. Patent No. 4,931,748 (the "McDermott" reference) teaches a "voltage controlled oscillator" that resides on a "single integrated circuit" and clocks the entire microcomputer. *(Appendix G, cols. 3, lines 17-*

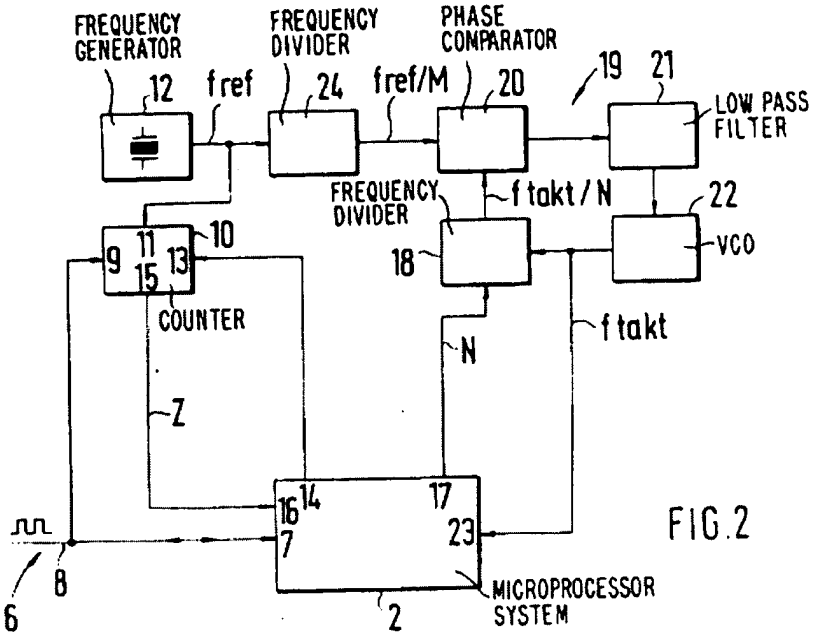
21; 3, lines 57-63; and 4, lines 24-29). It would have been obvious to combine the Richter and McDermott references because both references teach a single chip integrated circuit containing a central processing unit and a serial interface, where this central processing unit is clocked by a voltage controlled oscillator. *(Appendix G, col. 3, lines 17-21).*

As described above, it would have been obvious to one skilled in the art to modify the teachings of the Richter reference to use a ring oscillator variable speed system clock as the internal oscillator, as recited by the independent claims of the '336 patent. This is because such use of a ring oscillator is taught by the Kato reference, which, similar to Richter, describes a single integrated circuit containing a central processing unit and an oscillator. *(Appendix H, col. 10, lines 65 through 11, lines 7).* One skilled in the art would realize the benefits of implementing Kato's ring oscillator as Richter's variable oscillator to reduce power consumption during periods of lessened processing demand and to increase clock speed (and power consumption) during periods of increased processing demand. *(Appendix H, col. 11, lines 2-7).*

As described above, it would have been obvious for one skilled in art to modify the teachings of the Richter reference to use the "same batch and section of semiconductor wafer" in order to create "corresponding manufacturing variations" so that the speed of the ring oscillator and the system clock vary together, as recited by the independent '336 claims. *(Appendix I, col. 4, lines 11-12).* This is because the Ledzius reference, which so teaches, is also an integrated circuit with a central processing unit and an on-chip clock. *(Appendix I, Abstract).*

A detailed explanation of the pertinency and manner of applying the Richter, Ledzius, Kato, and McDermott references to claims 1-5 of the '336 patent is shown in the following claim chart.

Claim Limitation Claim 1	Teaching of the Richter Reference
1. A microprocessor system, comprising a single integrated circuit	The Richter reference (U.S. Patent No. 4,853,841) teaches a "microprocessor system 2" that is contemplated to provide the functions of a microprocessor, RAM, ROM, a serial interface, and a parallel interface where "in a one-chip system." *(Appendix D, col. 2, lines 55-65).*

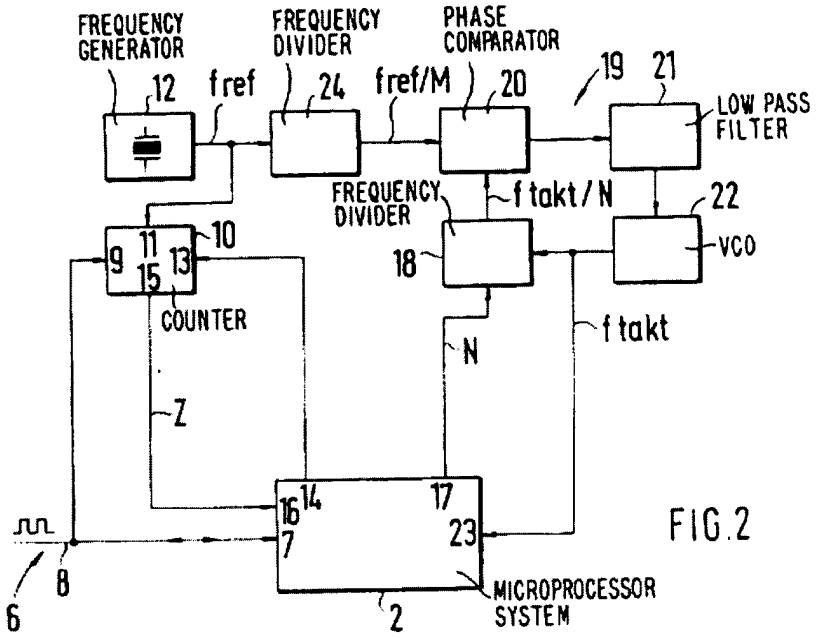
Claim Limitation	Teaching of the Richter Reference
	 FIG.2 *(Appendix D, Figure 2).*
including a central processing unit and	Richter teaches that the "microprocessor system" includes a "microprocessor." *(Appendix D, col. 2, lines 55-65).*
an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	Richter teaches that a "voltage-controlled oscillator generates a clock pulse 'ftakt' that acts upon the microprocessor system." *(Appendix D, col. 3, lines 18-20).* In some embodiments the 'ftakt' signal is used as both the system clock and a clock for the I/O port. *(Appendix D, col. 4, lines 34-43).* In other embodiments Richter teaches that the microprocessor is clocked by a "separate system clock generator for the microprocessor 2." *(Appendix D, col. 4, lines 34-38).* It is inherent to use a second, voltage controlled oscillator as the separate system clock generator because Richter already teaches clocking the microprocessor with a voltage controlled oscillator in a different embodiment. The Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). The Requester notes that the functionality of prior art processors are the same in material respect to commercial processors referred to by the Patent Owner in the above mentioned communications to third parties. Therefore, such an allegation, if true with respect to

Claim Limitation	Teaching of the Richter Reference
	today's processors, would also be true with regard to the processor taught by Richter. Accordingly, if the office accepts this premise, one skilled in the art would have understood Richter to disclose a ring oscillator for clocking the central processing unit. Alternatively, this feature is obvious in view of United States Patent No. 4,766,567 to Kato ("Kato"). Kato describes a ring oscillator that can be used to supply clock signals for the CPU described in Richter. *(Appendix H, col. 10, line 64 to col. 11, line 7).* One skilled in the art would have seen an apparent reason to implement Kato's ring oscillator as the voltage controlled oscillator or separate system clock of Richter, namely because a ring oscillator is an obvious selection for an internal oscillator and Richter already teaches the use of a voltage controlled oscillator to clock the microprocessor. One skilled in the art would realize the benefits of implementing Kato's ring oscillator as Richter's variable oscillator to reduce power consumption during periods of lessened processing demand and to increase clock speed (and power consumption) during periods of increased processing demand. *(Appendix H, col. 11, lines 2-7).* Further, Richter teaches that the voltage-controlled oscillator may be provided in the one-chip microprocessor system. Specifically, "[t]he first microprocessor system 2 is, for example, set up in a configuration comprising the microprocessor, volatile (RAM) and nonvolatile (ROM) memory chips, the serial interface and parallel input/output chips as well as other chips required for their operation. It is also contemplated to provide all these functions in a one-chip system." *(Appendix D, col. 2, lines 59-66).* The voltage-controlled oscillator, along with most of the other components displayed in Figure 2, are required for the operation of the microprocessor, and thus Richter teaches providing them on the one-chip system. As an aside, Requestor notes that this feature was commonplace at the time of filing, as shown by U.S. Patent No. 4,931,748 to McDermott et al. McDermott teaches a "voltage controlled oscillator" that resides on a "single integrated circuit" and clocks the entire microcomputer. *(Appendix G, col. 3, lines 17-21 and 57-63; col. 4, lines 24-29).* Both Richter and McDermott teach a single chip integrated circuit containing a central processing unit and a serial interface, where the central processing unit is clocked by a voltage controlled oscillator. *(Appendix G, col. 3, lines 17-21).* One skilled in the art would have found an apparent reason to combine Richter with McDermott, namely to provide the processor of Richter with a voltage controlled oscillator capable of generating clock signals across a wide range of frequencies.

Claim Limitation	Teaching of the Richter Reference
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	One skilled in the art would understand the on-chip oscillator circuit and the main control logic to include a plurality of electronic devices. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices. With respect to the limitation of the CPU and ring oscillator being constructed of the same process technology, Richter teaches implementing the microprocessor "in a one-chip system." *(Appendix D, col. 2, lines 55-65)*, which would necessarily be constructed by a single process technology. This indicates that the oscillator is fabricated on the same chip as the CPU and that the oscillator and CPU would therefore be constructed by the same process technology. *(Appendix F, page III-114)* It is noteworthy that the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Additionally, Requestor notes that this feature was commonplace at the time of filing, as shown by U.S. Patent No. 4,691,124 to Ledzius et al. ("Ledzius"). Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in process variations throughout the circuit. *(Appendix I, col. 4, lines 11-12).* Ledzius further teaches that the "frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances." *(Appendix I, col. 4, lines 9-11).* One skilled in the art would have found an apparent reason to combine Ledzius with Richter, namely to produce Richter's processor with minimal cost and defects.
a processing frequency capability of said central processing unit and a speed of said ring	The Patent Owner has stated in correspondence to various third parties that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing

Claim Limitation	Teaching of the Richter Reference
oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6.)* As an aside, Requestor notes that Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in frequency variations due to process and temperature variations throughout the circuit. *(Appendix I, col. 4, lines 3-21).* Richter contemplates providing all the chips required for the microprocessor's functioning on a "one-chip system." *(Appendix D, col. 2, lines 59-66).* One skilled in the art would have found an apparent reason to combine Ledzius with Richter, namely to produce the one-chip system of Richter with minimal cost and defects.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;	Richter teaches that the "microprocessor system 2 has a serial interface (not shown) which is connected by the input/output port 7 to a signal line 8 of the serial bus system 6." *(Appendix D, col. 2, lines 55-58).*
and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	Richter teaches a signal "ftakt" for clocking the serial I/O port of the microprocessor that is independent of the CPU clock: "the data transmission of the serial interface is supplied with the clock frequency signal 'ftakt', and the microprocessor of the microprocessor system 2 is equipped with its own system clock generator." *(Col. 4, lines 34-43 and 58-62)* Richter describes the system clock as a "separate system clock generator for the microprocessor" that is independent of the I/O clock signal. *(Col. 4, lines 36-47)* Additionally, the Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. *(Reexamination Control Number 90/008,306, Original*

Claim Limitation	Teaching of the Richter Reference
	Ex Parte Request by Third Party, Exhibit 12 at 7-8). As previously described, Richter clearly teaches a serial interface. If the Patent Owner's assertions are true today as to commercial processors, then they are also true as to the prior art processors. In any case, Requestor notes that the use of a second independent clock for providing clocking signals to an I/O interface was commonplace at the time of filing. *(See, e.g., US Patent Nos. 4,443,845 (col. 17, lines 1-42; figs. 14A-14B); 4,409,665 (col. 5, lines 46-6, lines 41; fig. 3c); 4,053,946 (col. 34, lines 15-31); 4,868,784 (col. 25, Table I, "Serial-clock control"); 5,142,637 (col. 6, line 59 to col. 7, line 5; col. 7, line 63 to col. 8, line 2; Figs. 12 & 13)).*
Claim 2	
2. The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	Richter teaches that "[t]he division ratio 1/M at the second frequency divider 24 is fixed. It determines the frequency increments by which the clock frequency signal 'ftakt' can be adjusted. It is fixed such that by means of a programmable, integer value of N, a suitable clock frequency 'ftakt' is adjusted. From this adjusted clock frequency 'ftakt', the desired transmission speeds v' can be derived with a required precision by integer division so that the microprocessor system can therefore be synchronized with the communication partner." *(Col. 4, lines 10-19)* One skilled in the art would understand that if the communication partner operates at a fixed frequency, the clock signal 'ftakt' would be a fixed frequency clock signal. The clock signal 'ftakt" taught by Richter is based on "clock frequency input 23." *(Col. 3, lines 18-20).* Requester notes that use of a fixed frequency clock as a clock input was well known in the art at the time of filing. *(See, e.g., the Mostek reference (Appendix F, page III-109);US 4,893,271 (col. 1, lines 17-18); US 4,751,565 (col. 1, lines 50-52); US 4,947,411 (Abstract); US 5,050,195 (Abstract); US 4,835,491 (col. 2, lines 24-25))* Additionally, the Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8).* If the Patent Owner's assertions are accepted, one skilled in the art would recognize that the incoming signal to the serial interface could be of fixed frequency, teaching the features of this limitation.
Claim 3	
3. In a microprocessor	The Richter reference (U.S. Patent No. 4,853,841) teaches a

Claim Limitation	Teaching of the Richter Reference
integrated circuit,	"microprocessor system 2" that is contemplated to provide the functions of a microprocessor, RAM, ROM, a serial interface, and a parallel interface where "in a one-chip system." *(Appendix D, col. 2, lines 55-65).*  FIG.2 *(Appendix D, Figure 2).*
a method for clocking the microprocessor within the integrated circuit, comprising the steps of: providing an entire ring oscillator system clock	Richter teaches that a "voltage-controlled oscillator generates a clock pulse 'ftakt' that acts upon the microprocessor system." *(Appendix D, col. 3, lines 18-20).* In some embodiments the 'ftakt' signal is used as both the system clock and a clock for the I/O port. *(Appendix D, col. 4, lines 34-43).* In other embodiments Richter teaches that the microprocessor is clocked by a "separate system clock generator for the microprocessor 2." *(Appendix D, col. 4, lines 34-38).* It is inherent to use a second, voltage controlled oscillator as the separate system clock generator because Richter already teaches clocking the microprocessor with a voltage controlled oscillator in a different embodiment. The Patent Owner has asserted in correspondence to various third parties that all on-chip oscillators are variable and that the presence of an on-chip clock generation circuit indicates the presence of a ring oscillator (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). The Requester notes that the functionality of prior art processors are the same in material respect to commercial processors referred to by the Patent Owner in the above mentioned communications

Claim Limitation	Teaching of the Richter Reference
	to third parties. Therefore, such an allegation, if true with respect to today's processors, would also be true with regard to the processor taught by Richter. Accordingly, if the office accepts this premise, one skilled in the art would have understood Richter to disclose a ring oscillator for clocking the central processing unit. Alternatively, this feature is obvious in view of U. S. Patent No. 4,766,567 to Kato ("Kato"). Kato describes a ring oscillator that can be used to supply clock signals for the CPU described in Richter. *(Appendix H, col. 10, line 64 to col. 11, line 7).* One skilled in the art would have seen an apparent reason to implement Kato's ring oscillator as the voltage controlled oscillator or separate system clock of Richter, namely because a ring oscillator is an obvious selection for an internal oscillator and Richter already teaches the use of a voltage controlled oscillator to clock the microprocessor. One skilled in the art would realize the benefits of implementing Kato's ring oscillator as Richter's variable oscillator to reduce power consumption during periods of lessened processing demand and to increase clock speed (and power consumption) during periods of increased processing demand. *(Appendix H, col. 11, lines 2-7).* Further, Richter teaches that the voltage-controlled oscillator may be provided in the one-chip microprocessor system. Specifically, "[t]he first microprocessor system 2 is, for example, set up in a configuration comprising the microprocessor, volatile (RAM) and nonvolatile (ROM) memory chips, the serial interface and parallel input/output chips as well as other chips required for their operation. It is also contemplated to provide all these functions in a one-chip system." *(Appendix D, col. 2, lines 59-66).* The voltage-controlled oscillator, along with most of the other components displayed in Figure 2, are required for the operation of the microprocessor, and thus Richter teaches providing them on the one-chip system. As an aside, Requestor notes that this feature was commonplace at the time of filing, as shown by U.S. Patent No. 4,931,748 to McDermott et al. McDermott teaches a "voltage controlled oscillator" that resides on a "single integrated circuit" and clocks the entire microcomputer. *(Appendix G, col. 3, lines 17-21 and 57-63; col. 4, lines 24-29).* Both Richter and McDermott teach a single chip integrated circuit containing a central processing unit and a serial interface, where the central processing unit is clocked by a voltage controlled oscillator. *(Appendix G, col. 3, lines 17-21).* One skilled in the art would have found an apparent reason to combine Richter with McDermott, namely to provide the processor of Richter with a voltage controlled oscillator capable of generating clock signals across a

Claim Limitation	Teaching of the Richter Reference
	wide range of frequencies.
constructed of electronic devices within the integrated circuit,	One skilled in the art would understand the on-chip oscillator circuit and the main control logic to include a plurality of electronic devices. Additionally, the Patent Owner has stated in correspondence to various third parties that all CPUs and clocks inherently include a plurality of electronic devices.
said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;	Richter teaches implementing the microprocessor "in a one-chip system." *(Appendix D, col. 2, lines 55-65)*, which would necessarily be constructed by a single process technology. This indicates that the oscillator is fabricated on the same chip as the CPU and that the oscillator and CPU would therefore be constructed by the same process technology. *(Appendix F, page III-114)* It is noteworthy that the Patent Owner has stated in correspondence to various third parties that the features of this limitation are inherent in an integrated circuit with a CPU and a clock (the Office is urged to require Patent Owner to produce this correspondence under Rule 105). As one specific example, the Patent Owner has stated that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6.)* Additionally, Requestor notes that this feature was commonplace at the time of filing, as shown by U.S. Patent No. 4,691,124 to Ledzius et al. ("Ledzius"). Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in process variations throughout the circuit. *(Appendix I, col. 4, lines 11-12).* Ledzius further teaches that the "frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances." *(Appendix I, col. 4, lines 9-11).* One skilled in the art would have found an apparent reason to combine Ledzius with Richter, namely to produce Richter's processor with minimal cost and defects.

Claim Limitation	Teaching of the Richter Reference
	Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in frequency variations due to process and temperature variations throughout the circuit. *(Appendix I, col. 4, lines 3-21).* Richter contemplates providing all the chips required for the microprocessor's functioning on a "one-chip system." *(Appendix D, col. 2, lines 59-66).* One skilled in the art would have found an apparent reason to combine Ledzius with Richter, namely to produce the one-chip system of Richter with minimal cost and defects.
using the ring oscillator system clock for clocking the microprocessor,	The voltage-controlled oscillator taught by Richter is used to clock the microprocessor as described above.
said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;	The Patent Owner has stated in correspondence to various third parties that because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 13 at 6).* Further, during the examination of the '336 patent, the Applicant stated that "the placement of [the ring oscillator clock and the microprocessor] within the same integrated circuit" causes the microprocessor and clock to naturally "vary commensurately in speed as a function of various parameters (e.g., temperature) affecting circuit performance." *(Appendix B, April 15, 1996 Applicant Arguments, original page 6.)* As an aside, Requestor notes that Ledzius teaches that manufacturing circuits from the "same batch and section of semiconductor wafer" results in frequency variations due to process and temperature variations throughout the circuit. *(Appendix I, col. 4, lines 3-21).* Richter contemplates providing all the chips required for the microprocessor's functioning on a "one-chip system." *(Appendix D, col. 2, lines 59-66).* One skilled in the art would have found an apparent reason to combine Ledzius with Richter, namely to produce the one-chip system of Richter with minimal cost and defects. Additionally and as described previously, one skilled in the art would see

Claim Limitation	Teaching of the Richter Reference
	an apparent reason to combine the ring oscillator of Kato with Richter. In such case, Kato teaches that "[w]hen a ring oscillator is used, its output frequency lowers in proportion to the speed of the data processing circuit, which is lowered due to the drop of power supply voltage." *(Appendix H, col. 11, lines 2-7).*
providing an on chip input/output interface for the microprocessor integrated circuit; and	Richter teaches that the "microprocessor system 2 has a serial interface (not shown) which is connected by the input/output port 7 to a signal line 8 of the serial bus system 6." *(Appendix D, col. 2, lines 55-58).*
clocking the input/output interface with a second clock independent of the ring oscillator system clock,	Richter teaches a signal "ftakt" for clocking the serial I/O port of the microprocessor that is independent of the CPU clock: "the data transmission of the serial interface is supplied with the clock frequency signal 'ftakt', and the microprocessor of the microprocessor system 2 is equipped with its own system clock generator." *(Col. 4, lines 34-43 and 58-62)* Richter describes the system clock as a "separate system clock generator for the microprocessor" that is independent of the I/O clock signal. *(Col. 4, lines 36-47)* Additionally, the Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8).* As previously described, Richter clearly teaches a serial interface. If the Patent Owner's assertions are true today as to commercial processors, then they are also true as to the prior art processors. In any case, Requestor notes that the use of a second independent clock for providing clocking signals to an I/O interface was commonplace at the time of filing. *(See, e.g., US Patent Nos. 4,443,845 (col. 17, lines 1-42; figs. 14A-14B); 4,409,665 (col. 5, lines 46-6, lines 41; fig. 3c); 4,053,946 (col. 34, lines 15-31); 4,868,784 (col. 25, Table I, "Serial-clock control"); 5,142,637 (col. 6, line 59 to col. 7, line 5; col. 7, line 63 to col. 8, line 2; Figs. 12 & 13)).*
Claim 4	
4. The method of claim 3 in which the second clock is a fixed frequency clock.	Richter teaches that "[t]he division ratio 1/M at the second frequency divider 24 is fixed. It determines the frequency increments by which the clock frequency signal 'ftakt' can be adjusted. It is fixed such that by means of a programmable, integer value of N, a suitable clock frequency 'ftakt' is adjusted. From this adjusted clock frequency 'ftakt', the desired

Claim Limitation	Teaching of the Richter Reference
	transmission speeds v' can be derived with a required precision by integer division so that the microprocessor system can therefore be synchronized with the communication partner." *(Col. 4, lines 10-19)* One skilled in the art would understand that if the communication partner operates at a fixed frequency, the clock signal 'ftakt' would be a fixed frequency clock signal. The clock signal 'ftakt" taught by Richter is based on "clock frequency input 23." *(Col. 3, lines 18-20).* Requester notes that use of a fixed frequency clock as a clock input was well known in the art at the time of filing. *(See, e.g., the Mostek reference (Appendix F, page III-109);US 4,893,271 (col. 1, lines 17-18); US 4,751,565 (col. 1, lines 50-52); US 4,947,411 (Abstract); US 5,050,195 (Abstract); US 4,835,491 (col. 2, lines 24-25))* Additionally, the Patent Owner has stated in correspondence to various third parties that any serial interface satisfies the limitation of a second independent clock. *(Reexamination Control Number 90/008,306, Original Ex Parte Request by Third Party, Exhibit 12 at 7-8).* If the Patent Owner's assertions are accepted, one skilled in the art would recognize that the incoming signal to the serial interface could be of fixed frequency, teaching the features of this limitation.
Claim 5	
5. The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.	As described in the teachings corresponding to Claim 1, a voltage controlled oscillator is taught as a "separate system clock generator for the microprocessor 2." *(Appendix D, col. 4, lines 34-38).* One skilled in the art would understand that information is transferred to and from the microprocessor in synchrony with the microprocessor's system clock.

From the foregoing chart, it can be seen that claims 1-5 are rendered obvious by Richter in combination with Ledzius, Kato, and McDermott. Thus, claims 1-5 are unpatentable as being obvious under U.S.C. § 103 by the Richter reference in combination with the Ledzius, Kato, and McDermott references.

F. The Richter Reference, in Light of the Ledzius, Kato, and McDermott References, Renders Obvious the Newly Introduced Claims of the '336 Patent

The Richter reference in combination with the Ledzius, Kato, and McDermott references renders obvious new claims added during the patent's ongoing merged reexamination. Specifically, the Patent Owner added claims 11-20 which parallel respective original claims 1-10 except that they further include a limitation to "more clearly set forth the meaning of 'independent.'" *(Appendix C, Amendment, Sept. 8, 2008, original page 11).* The additional limitation appends the parallel independent claims and recites: "thereby enabling decoupling a speed of said central processing unit from a speed of said input/output interface." *(Id.)*

Richter teaches an embodiment where the clock for the serial interface and the speed of the serial interface is distinct from a "separate system clock generator for the microprocessor 2." *(Appendix D, col. 4, lines 34-38).* This separate system clock would not be tied to the serial interface and thus provides a decoupling of speed of the microprocessor from the serial interface.

XII. CONCLUSION

For the foregoing reasons, substantial and new questions of patentability have been raised with respect to all claims (1-10) of the '336 patent. The Mostek, Dozier, and Richter references anticipate or render obvious, either alone or in combination with other references as described in the foregoing charts, each of the claims of the '336 patent. The questions of patentability presented herein are new even with respect to the pending reexamination proceedings.

Respectfully submitted,

Date: 8/24/09

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CERTIFICATE OF SERVICE

I hereby certify, pursuant to 37 C.F.R. §1.510(b)(5), that on August 24, 2009 I caused a true and correct copy of the foregoing REQUEST FOR EX PARTE REEXAMINATION UNDER 35 U.S.C. § 302 AND 37 C.F.R. § 1.510 to be served via First Class U.S. Mail on the following:

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