IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of:	
	Charles H. Moore et al.
Patent No:	5,809,336
Issued:	September 15, 1998
Title:	HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

REQUEST FOR *EX PARTE* REEXAMINATION UNDER 35 U.S.C. § 302 AND 37 C.F.R. § 1.510

Mail Stop *Ex Parte* Reexam
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 35 U.S.C. § 302 and 37 C.F.R. § 1.510, the third party requester hereby requests reexamination of U.S. Patent No. 5,809,336 based on the prior art references cited in the accompanying Information Disclosure Statement. This patent -- which issued on September 15, 1998, and for which Reexamination Certificate No. 5,809,336 C1 issued on December 15, 2009 -- is still enforceable. The third party requester certifies that, in accordance with 37 C.F.R. §§ 1.33(c) and 1.510(b)(5), this request is being served in its entirety on the attorney of record in the patent.

I. Identification of Claims for which Reexamination is Requested

Reexamination is requested for claims 1, 2, 6, 7 and 9-16, as presented in Reexamination Certificate 5,809,336 C1 (hereinafter "the '336 reexamination certificate"), which issued on December 15, 2009.

II. Contents of Appendices

Appendix A provides a legible copy of the entire patent to be reexamined: U.S. Patent No. 5,809,336 (hereinafter "the '336 patent").

Appendix B provides a legible copy of a Certificate of Correction dated May 22, 2007, and issued for the '336 patent.

Appendix C provides a legible copy of the '336 reexamination certificate.

Appendix D provides a listing of all patents and publications relied upon in the present request.

Appendices E through I provide legible copies of U.S. patents and printed publications that are relied upon in the present request.

III. Prior and Concurrent Reexamination Proceedings

Five requests have previously been filed, requesting reexamination of the '336 patent.

1 - 3). Control Nos. 90/008,237, 90/008,306 and 90/008,474

The requests for reexamination in Control Nos. 90/008,237, 90/008,306 and 90/008,474 were granted. These three proceedings were subsequently merged into one proceeding. This proceeding resulted in the issuance of the '336 reexamination certificate on December 15, 2009.

This certificate provided:

> AS A RESULT OF REEXAMINATION, IT HAS BEEN DETERMINED THAT:
>
> Claims 3-5 and 8 are cancelled.
>
> Claims 1, 6 and 10 are determined to be patentable as amended.
>
> Claims 2, 7 and 9, dependent on an amended claim, are determined to be patentable.
>
> New claims 11-16 are added and determined to be patentable. ('336 reexamination certificate, col. 1, lines 45- 57.)

As such, claims 1, 2, 6, 7 and 9-16 were effectively presented in the '336 reexamination certificate.

4) Control No. 90/010,551

The request for reexamination in Control No. 90/010,551 was denied.

5) Control No. 90/009,457

The request for reexamination in Control No. 90/009,457 was granted. Although a reexamination certificate has not yet issued from this proceeding, prosecution has been closed. A Notice of Intent to Issue *Ex Parte* Reexamination Certificate was mailed on July 19, 2010.

In the July 19, 2010 Notice of Intent to Issue, claims 1, 2, 6, 7 and 9-16 of the '336 reexamination certificate were confirmed. (See July 19, 2010 Notice of Intent to Issue, page 1.)

On pages 2-8 of the Notice, an Examiner's Amendment was provided. Regarding the Examiner's Amendment, the Examiner stated that the amendments matched those entered in the proceeding that resulted in the '336 reexamination certificate. In more detail, the Examiner indicated: "All changes made by this examiner's amendment reflect the changes made in U.S. Patent No. 5,809,336 by the reexamination certificate issued on December 15, 2009." (July 19, 2010 Notice of Intent to Issue, page 2.)

IV. Statement of Substantial New Questions of Patentability

The claims of the '336 reexamination certificate are directed to a microprocessor system that includes a central processing unit (CPU) and an input/output interface for exchanging control signals, addresses and data with the CPU.

According to independent claim 1, the CPU is clocked by a variable speed system clock. A second clock that is independent of the variable speed system clock is connected to the input/output interface. A clock signal of the second clock originates from a source other than the variable speed system clock.

Similar features are recited in the other independent claims.

In the reexamination proceeding that resulted in the '336 reexamination certificate, the Examiner amended each of the independent claims by an Examiner's Amendment. Further, the Examiner provided a "Reasons for Allowance" section that identified specific claim limitations that

were not found in the four closest identified prior art references. The four closest references were identified as:

- U.S. Patent No. 4,766,567 to Kato (hereinafter "Kato");
- U.S. Patent No. 4,691,124 to Ledzius et al. (hereinafter "Ledzius");
- U.S. Patent No. 4,910,703 to Ikeda et al. (hereinafter "Ikeda"); and
- U.S. Patent No. 4,931,748 to McDermott et al. (hereinafter "McDermott"). (See September 11, 2009 Notice of Intent to Issue *Ex Parte* Reexamination Certificate, pages 8-11).

Regarding the patentability of independent claim 1, the Examiner stated:

> Claim 1: Entry of the examiner's amendment produces claim 1, which recites: '*a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.*'
>
> None of the references to Kato[,] Ledzius et al, Ikeda et al and McDermott et al incorporate these recited features, either alone or in combination. Additionally, these features are not present in the remaining prior art of record. Accordingly, claim 1 is determined to be allowable. (September 11, 2009 Notice of Intent to Issue *Ex Parte* Reexamination Certificate, pages 8-9.) (Underlining and italics in original.)

As such, the Examiner stated that independent claim 1 was determined to be allowable based on certain limitations that were not found in the prior art of record.

The Examiner made similar statements regarding the other independent claims. (See September 11, 2009 Notice of Intent to Issue *Ex Parte* Reexamination Certificate, pages 9-11.)

In view of the above-described findings in the prior reexamination proceeding, this request presents four Substantial New Questions (SNQs) of Patentability.

A) SNQ of Patentability based on Amano

U.S. Patent No. 4,482,955 to Amano et al. (hereinafter "Amano") is newly cited in the present request. Amano discloses a main processor that has a CPU and a keyboard interface unit. Further, Amano discloses a keyboard controller that is connected to the keyboard interface unit.

(See Amano, FIG. 2.) Regarding the CPU and the keyboard controller, Amano discloses that these units have independent clock generators. (See Amano, col. 7, lines 34-38.)

Amano expressly distinguishes its main processor from a prior art system, in which the keyboard controller clock is supplied from the main system. (See Amano, col. 7, lines 25-27.) Because Amano draws such a distinction between its main processor and a prior art system in which the keyboard controller clock originates from the main system, it follows that the clock signal of Amano's keyboard controller clock originates from a source other than the CPU clock.

Further, Amano at least implicitly discloses that the clock signal of the keyboard controller clock is connected to the keyboard interface unit. Amano discloses that the keyboard controller responds to CPU polling, according to its own independent clock generator. (See Amano, col. 7, lines 34-38.) In order for the main processor to properly interpret the keyboard controller's responses, one skilled in the art would understand that the clock of the keyboard controller (which controls the generation of the responses) is supplied to the keyboard interface unit. Therefore, Amano at least implicitly discloses that the keyboard controller clock is connected to the keyboard interface unit.

As such, Amano teaches the limitations that were added to independent claim 1 in order to render this claim allowable in the reexamination proceeding that produced the '336 reexamination certificate. The noted disclosures of Amano also teach the limitations that were added to the other independent claims in order to render these claims allowable in the same reexamination proceeding.

Therefore, Amano provides new, non-cumulative technological teachings that were not previously considered by the USPTO in the proceeding that produced the '336 reexamination certificate. Further, these new technological teachings were not previously considered by the USPTO in conjunction with any other requests for reexamination of the '336 patent (i.e., Control Nos. 90/010,551 and 90/009,457).

Therefore, the new technological teachings of Amano raise an SNQ of patentability with respect to the claims of the '336 reexamination certificate.

B) SNQ of Patentability based on Amano and Intel 8251A

As explained earlier, Amano is newly cited in the present request. Similarly, Intel 8251A/S2657 PROGRAMMING COMMUNICATION INTERFACE, Intel Component Data Catalog 1981, pages 8-43 to 8-48 (hereinafter "Intel 8251A") is also newly cited in the present request.

As explained earlier, Amano discloses that its main processor has a keyboard interface unit that is connected to a keyboard controller. Further, Amano discloses that the keyboard interface unit includes a communication interface unit for receiving serial data from the keyboard controller. (See Amano, col. 2, line 64 to col. 3, line 4, and FIG. 3.) Amano discloses that the communication interface unit may be implemented by the Intel 8251A programmable communication interface. (See Amano, col. 3, lines 8-17.)

This particular interface is described in Intel 8251A. Intel 8251A discloses that the received serial data is clocked to the Receiver Clock signal (RxC). (See Intel 8251A, page 8-47.) Intel 8251A also discloses that the pin corresponding to the RxC signal is an input pin. (See Intel 8251A, Fig. 4.) As such, Intel 8251A discloses that serial data received by the interface are clocked to the Receiver Clock, which is also received by the interface.

One skilled in the art would understand that, when the Intel 8251A interface is implemented as Amano's communication interface unit (as proposed in Amano), the Receiver Clock signal that is input to the Intel 8251A corresponds to the clock of the keyboard controller 34. As such, the teachings of Amano and Intel 8251A further support the proposition that the clock of Amano's keyboard controller is connected to its keyboard interface unit.

As previously explained, Amano discloses that the CPU and the keyboard controller have independent clock generators and that the clock signal of its keyboard controller clock originates from a source other than the CPU clock.

Therefore, Amano and Intel 8251A provide new, non-cumulative technological teachings that were not previously considered by the USPTO in the proceeding that produced the '336 reexamination certificate. Further, these new technological teachings were not previously considered by the USPTO in conjunction with any other requests for reexamination of the '336 patent (i.e., Control Nos. 90/010,551 and 90/009,457).

Therefore, the new technological teachings of Amano and Intel 8251A raise an SNQ of patentability with respect to the claims of the '336 reexamination certificate.

C) SNQ of Patentability based on Amano and Nowatzyk

As explained earlier, Amano is newly cited in the present request. Similarly, "A Communication Architecture for Multiprocessor Networks," by Andreas Nowatzyk, April 1989 (hereinafter "Nowatzyk") is also newly cited in the present request.

Nowatzyk discloses asynchronous systems in which each processing element may use its own, independent clock. (See Nowatzyk, page 22.) For example, Nowatzyk discloses that descendants of one particular system (i.e., Caltech's Cosmic Cube) favor independent clocks and asynchronous channel protocols. (See Nowatzyk, page 59.) Furthermore, Nowatzyk discloses benefits of using such protocols: it discloses that asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution. (Nowatzyk, page 59.)

As such, in addition to the teachings of Amano itself, Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify previously cited references (e.g., Kato) according to Amano.

As previously explained, Amano discloses that the CPU and the keyboard controller have independent clock generators and that the clock signal of its keyboard controller clock originates from a source other than the CPU clock. Also, Amano at least implicitly discloses that the keyboard controller clock is connected to the keyboard interface unit.

Therefore, Amano and Nowatzyk provide new, non-cumulative technological teachings that were not previously considered by the USPTO in the proceeding that produced the '336 reexamination certificate. Further, these new technological teachings were not previously considered by the USPTO in conjunction with any other requests for reexamination of the '336 patent (i.e., Control Nos. 90/010,551 and 90/009,457).

Therefore, the new technological teachings of Amano and Nowatzyk raise an SNQ of patentability with respect to the claims of the '336 reexamination certificate.

D) SNQ of Patentability based on Amano, Intel 8251A and Nowatzyk

As explained earlier, Amano, Intel 8251A and Nowatzyk are all newly cited in the present request.

As previously explained, Amano discloses that the CPU and the keyboard controller have independent clock generators and that the clock signal of its keyboard controller clock originates from a source other than the CPU clock. Also, Amano at least implicitly discloses that the keyboard controller clock is connected to the keyboard interface unit.

As also previously explained, the teachings of Amano and Intel 8251A further support the proposition that the clock of Amano's keyboard controller is connected to its keyboard interface unit.

As also previously explained, Nowatzyk provides further teaching, suggestion and

motivation that would have led one of ordinary skill to modify a previously cited reference (e.g., Kato) according to Amano.

Therefore, Amano, Intel 8251A and Nowatzyk provide new, non-cumulative technological teachings that were not previously considered by the USPTO in the proceeding that produced the '336 reexamination certificate. Further, these new technological teachings were not previously considered by the USPTO in conjunction with any other requests for reexamination of the '336 patent (i.e., Control Nos. 90/010,551 and 90/009,457).

Therefore, the new technological teachings of Amano, Intel 8251A and Nowatzyk raise an SNQ of patentability with respect to the claims of the '336 reexamination certificate.

V. Detailed Explanation for Proposed Rejections

A) Detailed Explanation for Proposed Rejections Based on Amano

Requester respectfully submits that claims 1, 2, 6, 7 and 9-16 of the '336 reexamination certificate are rendered obvious under 35 U.S.C. § 103 by previously cited references Kato and Ledzius in view of newly cited Amano.

Table 1 below details how Kato, Ledzius and Amano disclose each and every limitation recited in claims 1, 2, 6, 7 and 9-16 of the '336 reexamination certificate.

Kato issued on August 23, 1988. Ledzius issued on September 1, 1987. Amano issued on November 13, 1984. Accordingly, each of Kato, Ledzius and Amano constitutes effective prior art under 35 U.S.C. § 103.

Kato is directed to a one-chip semiconductor device that comprises a semiconductor substrate with power supply terminals and data terminals. (See Kato, Abstract.)

Ledzius is directed to an integrated circuit which contains an on-chip clock that operates the integrated circuit at its true maximum speed. (See Ledzius, Abstract.)

Amano is directed to a data entry system that includes a main processor having a central processing unit (CPU) and a keyboard unit including a microprocessor. Amano discloses that provision of the microprocessor at the keyboard enables physical separation of the keyboard unit from the CPU by means of only a single bi-directional cable. Further, Amano discloses that the CPU periodically sends polling data in serial data format via the bi-directional cable to the keyboard microprocessor, which then controls a keyboard matrix scanning operation in performing the commands represented by the polling data. Further, Amano discloses that the microprocessor

then controls serial transmission of keyboard data to the CPU via the bi-directional cable. (See Amano, Abstract.)

Table 1
Comparison of the '336 reexamination certificate claims to Kato, Ledzius and Amano

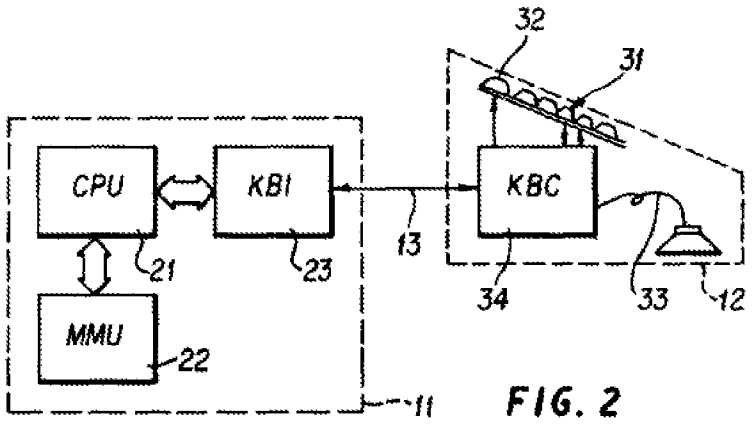
Claim 1	Kato, Ledzius and Amano
1. A microprocessor system, comprising a single integrated circuit including	This feature is taught by Kato. Kato discloses a "one-chip semiconductor device comprising a semiconductor substrate and a data processing IC, e.g., a microcomputer and a microprocessor, formed on the substrate." (Kato, col. 1, lines 7-10.)
a central processing unit and	This feature is taught by Kato. Kato discloses that the one-chip semiconductor device comprises a "data processing IC, e.g., a microcomputer and a microprocessor, formed on the substrate." (Kato, col. 1, lines 7-10).
an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	This feature is taught by Kato. Kato discloses that "The one-chip semiconductor device shown in FIG. 4 includes a data processing circuit comprised of dynamic circuit elements. A first clock generating circuit 14 comprises a first clock generating section 141[.]" (Kato, col. 8, lines 20-23.) Further, Kato discloses that the "first clock generating section 141 may be replaced by a ring oscillator of the known type or a CR clock oscillator similar which is completely built on semiconductor substrate 10. When a ring oscillator is used, its output frequency lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of power supply voltage." (Kato, col. 10, line 67 to col. 11, line 5.)

	Further, Kato discloses that the first clock generating section 141 is for clocking the data processing IC. Kato discloses that the "[f]irst clock generating section 141 is comprised of an external resistor R1, a capacitor C1 and inverters Inv9-Inv10. It generates a first clock signal Φ01 of a first frequency f0 determined by the logical threshold voltage of inverter Inv9, the resistance of resistor R1 and the capacitance of capacitor C1." (Kato, col. 8, lines 25-30.) Either the first clock signal Φ01 or another clock signal (i.e., second clock signal Φ02) is sent to the second clock generating circuit 15. (See Kato, col. 8, lines 35-39.) Signals generated by the second clock generating circuit 15 are supplied to the components of the data processing circuit. (See Kato, col. 4, lines 56-62.) Because Kato discloses that the first clock generating section 141 is connected to the data processing circuit via the second clock generating circuit 15, Kato discloses that the first clock generating section 141 is connected to the data processing circuit for clocking the data processing circuit.
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process	This feature is taught by Kato, as modified by Ledzius. Kato discloses that the "one-chip semiconductor device shown in FIG. 4 includes a data processing circuit comprised of dynamic circuit elements." (Kato, col. 8, lines 20-22.) (See also Kato, FIG. 4.) Kato discloses that the first clock generating section 141 includes a plurality of electronic devices. In more detail, Kato discloses that the "[f]irst clock generating section 141 is comprised of an external resistor R1, a capacitor C1 and inverters Inv9-Inv10." (Kato, col. 8, lines 25-27.)

technology with corresponding manufacturing variations,	(See also Kato, FIG. 4.) Kato does not explicitly disclose that electronic devices are constructed of the same process technology with corresponding manufacturing variations. Ledzius discloses electronic devices constructed of the same process technology with corresponding manufacturing variations. In more detail, Ledzius discloses: "The frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances. Accordingly, process caused variations are compensated because clock generator 18 is always physically made from the same batch and section of a semiconductor wafer as functional circuit 16." (Ledzius, col. 4, lines 9-14.) **Reason for modifying Kato according to Ledzius**: The prior art itself (i.e., Ledzius) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Ledzius to arrive at the claimed invention. In more detail, Ledzius provides that "process caused variations are compensated because clock generator 18 is always physically made from the same batch and section of a semiconductor wafer as functional circuit 16." (Ledzius, col. 4, lines 11-14.) Because Ledzius teaches that making components from the same batch and section of a semiconductor wafer compensates for process caused variations, Ledzius provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Ledzius. Therefore, it would have been obvious to modify Kato according to Ledzius.

a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	This feature is taught by Kato, modified by Ledzius. Kato discloses that a speed of the data processing circuit and a frequency of a ring oscillator vary together due to an operating voltage. In more detail, Kato discloses: "When a ring oscillator is used, its output frequency lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of power supply voltage." (Kato, col. 11, lines 2-5.) Kato does not expressly disclose that a speed of the data processing circuit and a frequency of a ring oscillator vary together due to process variations and due to temperature. Ledzius discloses that a speed of functional circuit 16 and a frequency of clock generator 18 vary together due to process variations and due to temperature. In more detail, Ledzius discloses: "The frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances . . . Slowest signal path 38 of functional circuit 16 controls the true maximum speed. Accordingly, process variations which affect slowest signal path 38 also affect clock generator 18. Likewise, clock generator 18 physically resides near slowest signal path 38. Thus, a temperature change that affects slowest signal path 38 also affects clock generator 18." (Ledzius, col. 4, lines 9-11 and 15-21.) **Reason for modifying Kato according to Ledzius**: The prior art itself (i.e., Ledzius) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Ledzius to arrive at the claimed invention.

	In more detail, Ledzius provides that "process caused variations are compensated because clock generator 18 is always physically made from the same batch and section of a semiconductor wafer as functional circuit 16." (Ledzius, col. 4, lines 11-14.) Because Ledzius teaches that making components from the same batch and section of a semiconductor wafer compensates for process caused variations, Ledzius provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Ledzius. Therefore, it would have been obvious to modify Kato according to Ledzius.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and	This feature is taught by Kato. Kato discloses that the data processing circuit includes input-output port (PB) 27. (See Kato, col. 4, line 63 to col. 5, line 2, and FIG. 4, element 27.) In addition, Kato discloses that the "data processing circuit has a control bus 29 for supplying control signals to its components, and an address bus 30 for supplying address signals to some of its components, and a data bus 31 for transmitting data 5 to and from its components." (Kato, col. 5, lines 2-6.) (See also Kato, FIG. 4, elements 29, 30 and 31.)
a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface,	This feature is taught by Kato, modified by Amano. Kato discloses that the clock generating circuit comprises a first clock generator 14 and a second clock generator 15. (See Kato, col. 4, lines 37-38.) Regarding the second clock generator 15, Kato discloses that the "second clock generator 15 produces two clock signals Φa and Φb from the reference clock signal Φ0 output by first clock generator 14 . . . They are supplied to the components of the data processing circuit." (Kato, col.

	4, lines 56-62.) Kato does not expressly disclose that the second clock is independent of the system clock. Amano teaches a second clock independent of a system clock connected to said input/output interface.  FIG. 2 With reference to FIG. 2 (see above), Amano discloses that the main processor 11 has a CPU 21 and a keyboard interface unit (KBI) 23. Also, Amano discloses that the keyboard 12 has a keyboard controller (KBC) 34. (See Amano, col. 2, lines 59-63.) Further, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. (See Amano, col. 2, lines 57-59.) First, Amano teaches a second clock independent of a system clock. In this regard, Amano discloses that the clock of the keyboard controller 34 is independent of a system clock of the CPU 21. In more detail, Amano discloses: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling." (Amano, col. 7, lines 34-38.)

	Amano explicitly distinguishes its invention from the prior art, where the keyboard controller clock is supplied by the main system. Amano discloses: "In the prior art, the keyboard controller clock of the DEC VT-100 full keyboard is supplied from the main system, and the polling (from the CPU) period and the response (from the keyboard) period is defined by a synchronization clock, that is, the data transmission control between the CPU and the keyboard is done using a time multiplex method." (Amano, col. 7, lines 25-31.) Therefore, Amano discloses a second clock independent of a system clock. In addition, Amano at least implicitly discloses that the clock of the keyboard controller is connected to said input/output interface. As noted previously regarding FIG. 2, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. More specifically, FIG. 2 shows that the keyboard interface unit 23 and the keyboard controller 34 are connected by bidirectional line 13. As previously explained, Amano discloses that the keyboard controller 34 has an independent clock generator. Amano at least implicitly discloses that the independent clock generator controls generation of the keyboard controller's responses to the CPU polling. (See Amano, col. 7, lines 34-38: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling.") In order for Amano's main processor 11 to properly interpret the responses generated by the keyboard controller 34, one skilled in the art would understand that the clock of the keyboard controller 34 (which

	controls the generation of the responses) is supplied to the keyboard interface unit 23 via bidirectional line 13. Because it would be understood by one skilled in the art that Amano's keyboard controller clock is supplied to the keyboard interface unit 23, Amano at least implicitly discloses that the clock of the keyboard controller 34 is connected to the input/output interface (i.e., keyboard interface unit 23). **Reason for modifying Kato according to Amano**: The prior art itself (i.e., Amano) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "limit[s] the duty time of the central processing unit and its memory by designing the keyboard with a keyboard controller integrally fabricated as a single chip microprocessor." (Amano, col. 1, lines 53-59.) Further, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "reduces the number of signals between the main processor and the keyboard such that a very thin bidirectional cable therebetween can be used." (Amano, col. 7, lines 14-17.) Because Amano discloses that implementing independent clock generators limits the duty time of the CPU and its memory and reduces the number of signals between the main processor and the keyboard, Amano provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Amano. Therefore, it would have been obvious to modify Kato according to Amano.

wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.	Kato does not expressly disclose that the clock signal of the second clock originates from a source other than the first clock. This feature is disclosed in Amano. In more detail, Amano discloses "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling." (Amano, col. 7, lines 34-38.) Distinguishing its invention from the prior art, Amano discloses: "In the prior art, the keyboard controller clock of the DEC VT-100 full keyboard is supplied from the main system . . ." (Amano, col. 7, lines 25-27.) As such, Amano discloses that the keyboard controller clock is independent of the main system (CPU) clock and that the keyboard controller clock is unlike prior art, where the keyboard controller clock is supplied by the main system (CPU). Therefore, Amano discloses that a clock signal of the keyboard controller clock originates from a source other than the main system (CPU) clock. **Reason for modifying Kato according to Amano**: The prior art itself (i.e., Amano) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "limit[s] the duty time of the central processing unit and its memory by designing the keyboard with a keyboard controller integrally

	fabricated as a single chip microprocessor." (Amano, col. 1, lines 53-59.) Further, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "reduces the number of signals between the main processor and the keyboard such that a very thin bidirectional cable therebetween can be used." (Amano, col. 7, lines 14-17.) Because Amano discloses that implementing independent clock generators limits the duty time of the CPU and its memory and reduces the number of signals between the main processor and the keyboard, Amano provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Amano. Therefore, it would have been obvious to modify Kato according to Amano.
Claim 2	**Kato, Ledzius and Amano**
2. The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	As explained above, Kato, Ledzius and Amano disclose the limitations of base claim 1. Kato does not disclose that the second clock is a fixed frequency clock. This feature is at least implicitly disclosed in Amano. As previously noted, Amano discloses that the keyboard controller clock controls generation of responses by the keyboard controller 34 responsive to polling by the CPU 21. Amano discloses that the responses are sent according to a designed (fixed) timing. Regarding the transmission of the responses from the keyboard controller 34 to the main system 11, Amano discloses that "to transmit the keyboard data to the side of the main processor, the microprocessor [of the

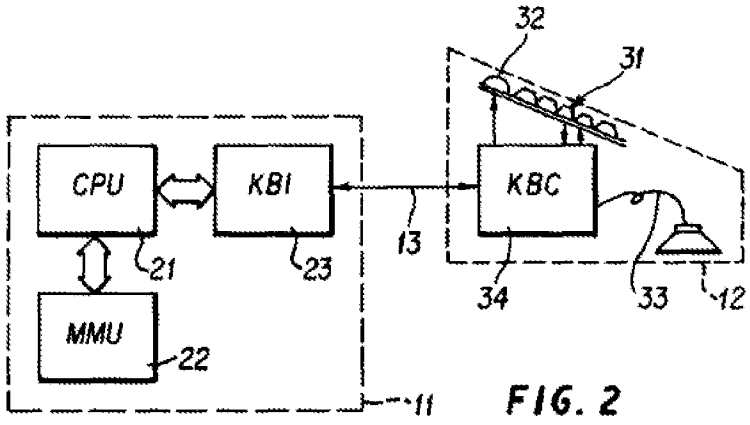
	keyboard controller 23] makes its P27 terminal zero and the communication interface unit 41 makes its RCV terminal active. The microprocessor 46 sends the start bit in this way and then transmits the succeeding data, parity bit and stop bits in the requisite order to the main processor 11 at the designed timing." (Amano, col. 5, lines 46-53.) Because Amano discloses that the sending of data (which is controlled by the keyboard controller clock) is performed at a designed (fixed) timing, Amano at least implicitly discloses that the keyboard controller clock is a fixed frequency clock. Therefore, Amano at least implicitly discloses that the second clock is a fixed frequency clock. **Reason for modifying Kato according to Amano**: It would have been obvious to modify Kato according to Amano because one of ordinary skill in the art could have substituted the fixed frequency clock of Amano in Kato in order to obtain predictable results. For example, as disclosed in Amano, a fixed frequency clock may be used to send data at a designed (fixed) timing. Because the result of sending data at a designed (fixed) timing would have been predictable, it would have been obvious to modify Kato according to Amano by substituting the fixed frequency clock of Amano in Kato.
Claim 6	**Kato, Ledzius and Amano**
6. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate,	This feature is taught by Kato. Kato discloses a "one-chip semiconductor device comprising a semiconductor substrate and a data processing IC, e.g., a microcomputer and a microprocessor, formed on the substrate." (Kato, col. 1, lines 7-10.)
said central	This feature is taught by Kato.

processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices:	Kato discloses that the clock generating circuit comprises a first clock generator 14 and a second clock generator 15. Kato discloses that signals produced by the second clock generator 15 are supplied to the data processing circuit. (See Kato, col. 4, lines 56-62: the "second clock generator 15 produces two clock signals Φa and Φb from the reference clock signal Φ0 output by first clock generator 14 . . . They are supplied to the components of the data processing circuit.") Therefore, Kato discloses that the data processing circuit operates at a processing frequency. Kato discloses that the "one-chip semiconductor device shown in FIG. 4 includes a data processing circuit comprised of dynamic circuit elements." (Kato, col. 8, lines 20-22.) (See also Kato, FIG. 4.) Therefore, Kato discloses the data processing circuit is constructed of a plurality of electronic devices.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit,	This feature is taught by Kato. In more detail, Kato discloses that the "first clock generating section 141 may be replaced by a ring oscillator of the known type or a CR clock oscillator similar which is completely built on semiconductor substrate 10. When a ring oscillator is used, its output frequency lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of power supply voltage." (Kato, col. 10, line 67 to col. 11, line 5.) Further, Kato discloses that the first clock generating section 141 is connected to the data processing IC. For example, Kato discloses that the "[f]irst clock generating section 141 is comprised of an external resistor R1, a capacitor C1 and inverters Inv9-Inv10. It generates a first clock signal Φ01 of a first frequency f0 determined by the logical threshold

	voltage of inverter Inv9, the resistance of resistor R1 and the capacitance of capacitor C1." (Kato, col. 8, lines 25-30.) Either the first clock signal Φ01 or another clock signal (i.e., second clock signal Φ02) is sent to the second clock generating circuit 15. (See Kato, col. 8, lines 35-39.) As previously noted, signals generated by the second clock generating circuit 15 are supplied to the components of the data processing circuit. (See Kato, col. 4, lines 56-62.) Because Kato discloses that the first clock generating section 141 is connected to the data processing circuit via the second clock generating circuit 15, Kato discloses that the first clock generating section 141 is connected to the data processing circuit.
said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,	This feature is disclosed in Kato. As previously noted, Kato discloses that the first clock generating section 141 produces a first clock signal. In more detail, Kato discloses that the "[f]irst clock generating section 141 is comprised of an external resistor R1, a capacitor C1 and inverters Inv9-Inv10. It <u>generates a first clock signal Φ01 of a first frequency f0</u> determined by the logical threshold voltage of inverter Inv9, the resistance of resistor R1 and the capacitance of capacitor C1." (Kato, col. 8, lines 25-30.) Therefore, Kato discloses that the first clock generating section 141 clocks the data processing IC at a clock rate. Also, Kato discloses that the first clock generating section 141 is constructed of a plurality of electronic devices – i.e., external resistor R1, a capacitor C1 and inverters Inv9-Inv10 (see Kato, col. 8, lines 25-27, and FIG. 4, element 141.)
thus varying the processing frequency	This feature is disclosed in Kato, modified by Ledzius.

of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	Kato does not expressly disclose these features. Ledzius discloses that a signal path of a functional circuit (which controls the true maximum speed) and a clock generator vary in the same way as a function of fabrication (process) or operational (temperature) parameters, thereby enabling the signal path speed to track the clock generator in response to said variation (e.g., a temperature change that affects slowest signal path 38 also affects clock generator 18). In more detail, Ledzius discloses: "The frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances. Accordingly, process caused variations are compensated because clock generator 18 is always physically made from the same batch and section of a semiconductor wafer as functional circuit 16. Slowest signal path 38 of functional circuit 16 controls the true maximum speed. Accordingly, process variations which affect slowest signal path 38 also affect clock generator 18. Likewise, clock generator 18 physically resides near slowest signal path 38. Thus, a temperature change that affects slowest signal path 38 also affects clock generator 18." (Ledzius, col. 4, lines 9-21.) **Reason for modifying Kato according to Ledzius**: The prior art itself (i.e., Ledzius) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Ledzius to arrive at the claimed invention. In more detail, Ledzius provides that "process caused variations are compensated because clock generator 18 is always physically made from the same batch and section of a semiconductor wafer as functional circuit 16." (Ledzius, col. 4, lines 11-14.)

	Because Ledzius teaches that making components from the same batch and section of a semiconductor wafer compensates for process caused variations, Ledzius provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Ledzius. Therefore, it would have been obvious to modify Kato according to Ledzius.
an on-chip input/output interface connected between said central processing unit and an off-chip external memory bus for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	This feature is disclosed by Kato. Kato discloses that the data processing circuit includes input-output port (PB) 27. (See Kato, col. 4, line 63 to col. 5, line 2, and FIG. 4, element 27.) Also, Kato discloses that "[t]he data processing circuit processes the data input from the external device through terminals . . . PBO-PB3 and supplies the processed data to the external device through terminals PBO-PB3[.]" Therefore, Kato discloses an on-chip input/output interface connected between the central processing unit (data processing circuit) and an off-chip external memory bus (it is inherent that the external device is off-chip and that the external device has a memory bus). In addition, Kato discloses that the "data processing circuit has a control bus 29 for supplying control signals to its components, and an address bus 30 for supplying address signals to some of its components, and a data bus 31 for transmitting data 5 to and from its components." (Kato, col. 5, lines 2-6.) (See also Kato, FIG. 4, elements 29, 30 and 31.) Therefore, Kato discloses an on-chip input/output interface connected between the CPU (data processing circuit) and an off-chip external memory bus for facilitating exchange of control signals, addresses and

	data with the CPU.
an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and	This feature is taught by Kato, modified by Amano. Kato discloses that the clock generating circuit comprises a first clock generator 14 and a second clock generator 15. (See Kato, col. 4, lines 37-38.) Regarding the second clock generator 15, Kato discloses that the "second clock generator 15 produces two clock signals Φa and Φb from the reference clock signal Φ0 output by first clock generator 14 . . . They are supplied to the components of the data processing circuit." (Kato, col. 4, lines 56-62.) Kato does not expressly disclose that that the second clock is off-chip, independent of the first clock, and operative at a frequency independent of a clock frequency of the first clock. Amano teaches an off-chip external clock independent of a system clock, connected to said input/output interface, wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock.  FIG. 2 With reference to FIG. 2 (see above), Amano discloses that the main processor 11 has a CPU 21 and a keyboard interface unit (KBI) 23. Also, Amano discloses that the keyboard 12 has a keyboard controller (KBC) 34. (See Amano, col. 2, lines 59-63.) Further, Amano discloses that the

	main processor 11 and the keyboard 12 are connected through bidirectional line 13. (See Amano, col. 2, lines 57-59.) First, Amano teaches an off-chip external clock independent of a system clock, wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock. In this regard, Amano discloses that the clock of the keyboard controller 34 is independent of a system clock of the CPU 21, wherein the keyboard controller clock is operative at a frequency independent of a clock frequency of the system clock. In more detail, Amano discloses: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling." (Amano, col. 7, lines 34-38.) Amano explicitly distinguishes its invention from the prior art, where the keyboard controller clock is supplied by the main system. Amano discloses: "In the prior art, the keyboard controller clock of the DEC VT-100 full keyboard is supplied from the main system, and the polling (from the CPU) period and the response (from the keyboard) period is defined by a synchronization clock, that is, the data transmission control between the CPU and the keyboard is done using a time multiplex method." (Amano, col. 7, lines 25-31.) Therefore, Amano discloses an external clock independent of the system oscillator. In addition, Amano at least implicitly discloses that the clock of the keyboard controller is connected to the input/output interface. As noted previously regarding FIG. 2, Amano discloses that the main

	processor 11 and the keyboard 12 are connected through bidirectional line 13. More specifically, FIG. 2 shows that the keyboard interface unit 23 and the keyboard controller 34 are connected by bidirectional line 13. As previously explained, Amano discloses that the keyboard controller 34 has an independent clock generator. Amano at least implicitly discloses that the independent clock generator controls generation of the keyboard controller's responses to the CPU polling. (See Amano, col. 7, lines 34-38: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling.") In order for Amano's main processor 11 to properly interpret the responses generated by the keyboard controller 34, one skilled in the art would understand that the clock of the keyboard controller 34 (which controls the generation of the responses) is supplied to the keyboard interface unit 23 via bidirectional line 13. Because it would be understood by one skilled in the art that Amano's keyboard controller clock is supplied to the keyboard interface unit 23, Amano at least implicitly discloses that the clock of the keyboard controller 34 is connected to the input/output interface (i.e., keyboard interface unit 23). **Reason for modifying Kato according to Amano**: The prior art itself (i.e., Amano) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard

	controller) "limit[s] the duty time of the central processing unit and its memory by designing the keyboard with a keyboard controller integrally fabricated as a single chip microprocessor." (Amano, col. 1, lines 53-59.) Further, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "reduces the number of signals between the main processor and the keyboard such that a very thin bidirectional cable therebetween can be used." (Amano, col. 7, lines 14-17.) Because Amano discloses that implementing independent clock generators limits the duty time of the CPU and its memory and reduces the number of signals between the main processor and the keyboard, Amano provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Amano. Therefore, it would have been obvious to modify Kato according to Amano.
wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.	Kato does not expressly disclose that a clock signal of the second clock originates from a source other than the first clock signal. This feature is disclosed in Amano. In more detail, Amano discloses "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling." (Amano, col. 7, lines 34-38.) Distinguishing its invention from the prior art, Amano discloses: "In the prior art, the keyboard controller clock of the DEC VT-100 full keyboard is supplied from the main system . . ." (Amano, col. 7, lines 25-27.)

	As such, Amano discloses that the keyboard controller clock is independent of the main system (CPU) clock and that the keyboard controller clock is unlike prior art, where the keyboard controller clock is supplied by the main system (CPU). Therefore, Amano discloses that a clock signal of the keyboard controller clock originates from a source other than the main system (CPU) clock. **Reason for modifying Kato according to Amano**: The prior art itself (i.e., Amano) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "limit[s] the duty time of the central processing unit and its memory by designing the keyboard with a keyboard controller integrally fabricated as a single chip microprocessor." (Amano, col. 1, lines 53-59.) Further, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "reduces the number of signals between the main processor and the keyboard such that a very thin bidirectional cable therebetween can be used." (Amano, col. 7, lines 14-17.) Because Amano discloses that implementing independent clock generators limits the duty time of the CPU and its memory and reduces the number of signals between the main processor and the keyboard, Amano provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Amano. Therefore, it would have been obvious to modify Kato according to Amano.
Claim 7	**Kato, Ledzius and Amano**

7. The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	As explained above, Kato, Ledzius and Amano disclose the limitations of base claim 6. The limitations of claim 7 are disclosed in Kato. Kato discloses that a speed of the data processing circuit and a frequency of a ring oscillator vary together due to an operating voltage. In more detail, Kato discloses: "When a ring oscillator is used, its output frequency lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of power supply voltage." (Kato, col. 11, lines 2-5.)
Claim 9	**Kato, Ledzius and Amano**
9. The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	As explained above, Kato, Ledzius and Amano disclose the limitations of base claim 6. The limitations of claim 9 are disclosed in Kato. Kato discloses that the "first clock generating section 141 may be replaced by a ring oscillator of the known type or a CR clock oscillator similar which is completely built on semiconductor substrate 10. When a ring oscillator is used, its output frequency lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of power supply voltage." (Kato, col. 10, line 67 to col. 11, line 5.)
Claim 10	**Kato, Ledzius and Amano**
In a microprocessor system including a central processing unit, a method for clocking said central processing unit	This feature is taught by Kato. Kato discloses a "one-chip semiconductor device comprising a semiconductor substrate and a data processing IC, e.g., a microcomputer and a microprocessor, formed on the substrate." (Kato, col. 1, lines 7-10.) Further, Kato discloses "The clock generating circuit generates clock

comprising the steps of:	signals and supplies them to the data processing circuit." (Kato, col. 4, lines 34-36.)
providing said central processing unit upon an integrated circuit substrate,	This feature is taught by Kato. Kato discloses a "one-chip semiconductor device comprising a semiconductor substrate and a data processing IC, e.g., a microcomputer and a microprocessor, formed on the substrate." (Kato, col. 1, lines 7-10.)
said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	This feature is taught by Kato. Kato discloses that the "one-chip semiconductor device shown in FIG. 4 includes a data processing circuit comprised of dynamic circuit elements." (Kato, col. 8, lines 20-22.) (See also Kato, FIG. 4.) Therefore, Kato discloses the data processing circuit is constructed of a plurality of electronic devices. It is inherent that these electronic devices (e.g., program counter 16, program memory (ROM) 167, instruction decoder (IR) 18, etc.) may be constructed of a plurality of transistors. Kato discloses that the clock generating circuit comprises a first clock generator 14 and a second clock generator 15. Kato discloses that signals produced by the second clock generator 15 are supplied to the data processing circuit. (See Kato, col. 4, lines 56-62: the "second clock generator 15 produces two clock signals Φa and Φb from the reference clock signal Φ0 output by first clock generator 14 . . . They are supplied to the components of the data processing circuit.") Therefore, Kato discloses that the data processing circuit operates at a processing frequency.
providing an entire variable speed clock disposed upon said	This feature is taught by Kato. In more detail, Kato discloses that the "first clock generating section 141

integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	may be replaced by a ring oscillator of the known type or a CR clock oscillator similar which is completely built on semiconductor substrate 10. When a ring oscillator is used, its output frequency lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of power supply voltage." (Kato, col. 10, line 67 to col. 11, line 5.) Further, Kato discloses that the "[f]irst clock generating section 141 is comprised of an external resistor R1, a capacitor C1 and inverters Inv9-Inv10." (Kato, col. 8, lines 25-27.) It is inherent that at least some of these parts (e.g., the inverters) may be constructed of a plurality of transistors.
clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one	This feature is disclosed in Kato, modified by Ledzius. Kato does not expressly disclose such features. Ledzius discloses that the frequency of the clock signal varies depending on process and temperature variances. Also, Ledzius discloses that a signal path of a functional circuit (which controls the true maximum speed) and the clock generator vary in the same way relative to variations in fabrication (process) or operational (temperature) parameters. In more detail, Ledzius discloses: "The frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances. Accordingly, process caused variations are compensated because clock generator 18 is always physically made from the same batch and section of a semiconductor wafer as functional circuit 16. Slowest signal path 38 of functional circuit 16 controls the true maximum speed. Accordingly, process variations which affect slowest signal path 38 also affect clock generator 18. Likewise, clock generator 18 physically resides near slowest signal path 38. Thus, a temperature change that affects slowest signal path 38 also affects clock generator 18." (Ledzius, col. 4, lines 9-21.)

or more fabrication or operational parameters associated with said integrated circuit substrate;	**Reason for modifying Kato according to Ledzius**: The prior art itself (i.e., Ledzius) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Ledzius to arrive at the claimed invention. In more detail, Ledzius provides that "process caused variations are compensated because clock generator 18 is always physically made from the same batch and section of a semiconductor wafer as functional circuit 16." (Ledzius, col. 4, lines 11-14.) Because Ledzius teaches that making components from the same batch and section of a semiconductor wafer compensates for process caused variations, Ledzius provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Ledzius. Therefore, it would have been obvious to modify Kato according to Ledzius.
connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	This feature is disclosed by Kato. Kato discloses that the data processing circuit includes input-output port (PB) 27. (See Kato, col. 4, line 63 to col. 5, line 2, and FIG. 4, element 27.) Also, Kato discloses that "[t]he data processing circuit processes the data input from the external device through terminals . . . PBO-PB3 and supplies the processed data to the external device through terminals PBO-PB3[.]" Therefore, Kato discloses connecting an on-chip input/output interface between the central processing unit (data processing circuit) and an off-chip external memory bus (it is inherent that the external device is off-chip and that the external device has a memory bus).

	In addition, Kato discloses that the "data processing circuit has a control bus 29 for supplying control signals to its components, and an address bus 30 for supplying address signals to some of its components, and a data bus 31 for transmitting data 5 to and from its components." (Kato, col. 5, lines 2-6.) (See also Kato, FIG. 4, elements 29, 30 and 31.) Therefore, Kato discloses exchange of control signals, addresses and data between the input/output interface and the CPU (data processing circuit).
clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock and	This feature is taught by Kato, modified by Amano. Kato discloses that the clock generating circuit comprises a first clock generator 14 and a second clock generator 15. (See Kato, col. 4, lines 37-38.) Regarding the second clock generator 15, Kato discloses that the "second clock generator 15 produces two clock signals Φa and Φb from the reference clock signal Φ0 output by first clock generator 14 . . . They are supplied to the components of the data processing circuit." (Kato, col. 4, lines 56-62.) Kato does not expressly disclose that second clock is off-chip and operative at a frequency independent of a clock frequency of the first clock. Amano teaches an off-chip external clock for clocking said input/output interface, wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock.

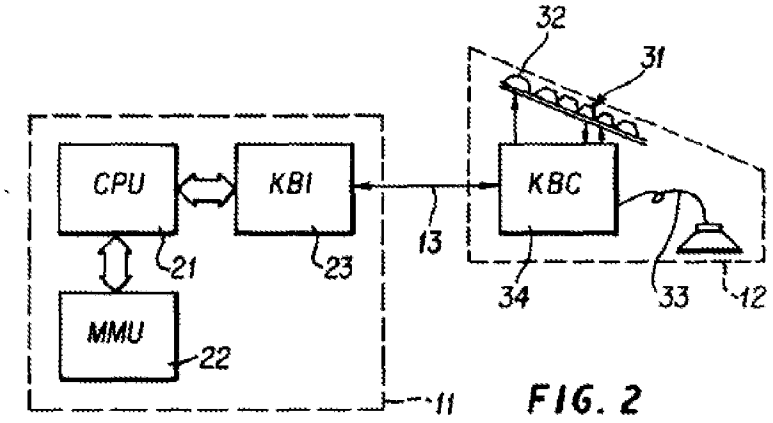


FIG. 2

With reference to FIG. 2 (see above), Amano discloses that the main processor 11 has a CPU 21 and a keyboard interface unit (KBI) 23. Also, Amano discloses that the keyboard 12 has a keyboard controller (KBC) 34. (See Amano, col. 2, lines 59-63.) Further, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. (See Amano, col. 2, lines 57-59.)

First, Amano teaches an off-chip external clock independent of a system clock, wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock.
In this regard, Amano discloses that the clock of the keyboard controller 34 is independent of a system clock of the CPU 21, wherein the keyboard controller clock is operative at a frequency independent of a clock frequency of the system clock.

In more detail, Amano discloses: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling." (Amano, col. 7, lines 34-38.)

Amano explicitly distinguishes its invention from the prior art, where the keyboard controller clock is supplied by the main system.

	Amano discloses: "In the prior art, the keyboard controller clock of the DEC VT-100 full keyboard is supplied from the main system, and the polling (from the CPU) period and the response (from the keyboard) period is defined by a synchronization clock, that is, the data transmission control between the CPU and the keyboard is done using a time multiplex method." (Amano, col. 7, lines 25-31.) Therefore, Amano teaches an off-chip external clock independent of a system clock, wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock. In addition, Amano at least implicitly discloses that the clock of the keyboard controller is for clocking the input/output interface. As noted previously regarding FIG. 2, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. More specifically, FIG. 2 shows that the keyboard interface unit 23 and the keyboard controller 34 are connected by bidirectional line 13. As previously explained, Amano discloses that the keyboard controller 34 has an independent clock generator. Amano at least implicitly discloses that the independent clock generator controls generation of the keyboard controller's responses to the CPU polling. (See Amano, col. 7, lines 34-38: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling.") In order for Amano's main processor 11 to properly receive and interpret the responses generated by the keyboard controller 34, one skilled in the art would understand that the clock of the keyboard controller 34 (which controls the generation of the responses) is supplied to the keyboard interface unit 23 via bidirectional line 13.

	Because it would be understood by one skilled in the art that Amano's keyboard controller clock is supplied to the keyboard interface unit 23, Amano at least implicitly discloses that the clock of the keyboard controller 34 is connected to the input/output interface (i.e., keyboard interface unit 23) for clocking the input/output interface. **Reason for modifying Kato according to Amano**: The prior art itself (i.e., Amano) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "limit[s] the duty time of the central processing unit and its memory by designing the keyboard with a keyboard controller integrally fabricated as a single chip microprocessor." (Amano, col. 1, lines 53-59.) Further, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "reduces the number of signals between the main processor and the keyboard such that a very thin bidirectional cable therebetween can be used." (Amano, col. 7, lines 14-17.) Because Amano discloses that implementing independent clock generators limits the duty time of the CPU and its memory and reduces the number of signals between the main processor and the keyboard, Amano provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Amano. Therefore, it would have been obvious to modify Kato according to Amano.
wherein a clock signal from said off-chip external clock	Kato does not expressly disclose such features. This feature is disclosed in Amano.

originates from a source other than said variable speed clock.	In more detail, Amano discloses "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling." (Amano, col. 7, lines 34-38.) Distinguishing its invention from the prior art, Amano discloses: "In the prior art, the keyboard controller clock of the DEC VT-100 full keyboard is supplied from the main system . . ." (Amano, col. 7, lines 25-27.) As such, Amano discloses that the keyboard controller clock is independent of the main system (CPU) clock and that the keyboard controller clock is unlike prior art, where the keyboard controller clock is supplied by the main system (CPU). Therefore, Amano discloses that a clock signal of the keyboard controller clock originates from a source other than the main system (CPU) clock. **Reason for modifying Kato according to Amano**: The prior art itself (i.e., Amano) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "limit[s] the duty time of the central processing unit and its memory by designing the keyboard with a keyboard controller integrally fabricated as a single chip microprocessor." (Amano, col. 1, lines 53-59.) Further, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "reduces the number of signals between the main processor

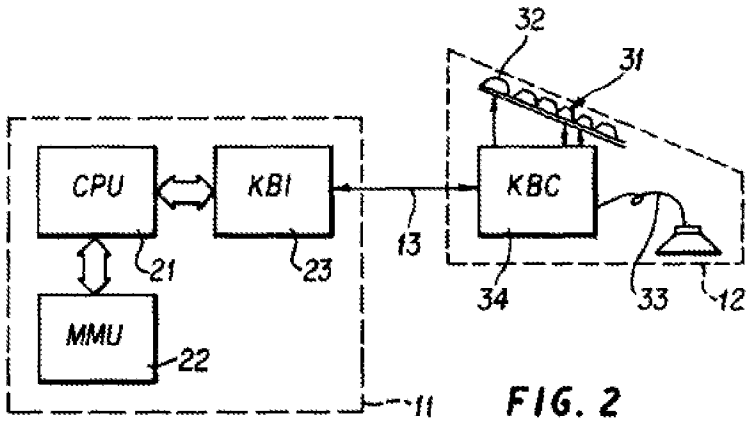
	and the keyboard such that a very thin bidirectional cable therebetween can be used." (Amano, col. 7, lines 14-17.) Because Amano discloses that implementing independent clock generators limits the duty time of the CPU and its memory and reduces the number of signals between the main processor and the keyboard, Amano provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Amano. Therefore, it would have been obvious to modify Kato according to Amano.
Claim 11	**Kato, Ledzius and Amano**
11. A microprocessor system, comprising a single integrated circuit including	This feature is taught by Kato. Kato discloses a "one-chip semiconductor device comprising a semiconductor substrate and a data processing IC, e.g., a microcomputer and a microprocessor, formed on the substrate." (Kato, col. 1, lines 7-10.)
a central processing unit and	This feature is taught by Kato. Kato discloses that the one-chip semiconductor device comprises a "data processing IC, e.g., a microcomputer and a microprocessor, formed on the substrate." (Kato, col. 1, lines 7-10 4:27).
an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	This feature is taught by Kato. Kato discloses that "The one-chip semiconductor device shown in FIG. 4 includes a data processing circuit comprised of dynamic circuit elements. A first clock generating circuit 14 comprises a first clock generating section 141[.]" (Kato, col. 8, lines 20-23.) Further, Kato discloses that the "first clock generating section 141 may be replaced by a ring oscillator of the known type or a CR clock oscillator similar which is completely built on semiconductor substrate 10. When a ring oscillator is used, its output frequency lowers in proportion to the

	speed of the data processing circuit which is lowered due to the drop of power supply voltage." (Kato, col. 10, line 67 to col. 11, line 5.) Further, Kato discloses that the first clock generating section 141 is for clocking the data processing IC. For example, Kato discloses that the "[f]irst clock generating section 141 is comprised of an external resistor R1, a capacitor C1 and inverters Inv9-Inv10. It generates a first clock signal Φ01 of a first frequency f0 determined by the logical threshold voltage of inverter Inv9, the resistance of resistor R1 and the capacitance of capacitor C1." (Kato, col. 8, lines 25-30.) Either the first clock signal Φ01 or another clock signal (i.e., second clock signal Φ02) is sent to the second clock generating circuit 15. (See Kato, col. 8, lines 35-39.) Signals generated by the second clock generating circuit 15 are supplied to the components of the data processing circuit. (See Kato, col. 4, lines 56-62.) Because Kato discloses that the first clock generating section 141 is connected to the data processing circuit via the second clock generating circuit 15, Kato discloses that the first clock generating section 141 is connected to the data processing circuit for clocking the data processing circuit.
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process	This feature is taught by Kato, as modified by Ledzius. Kato discloses that the "one-chip semiconductor device shown in FIG. 4 includes a data processing circuit comprised of dynamic circuit elements." (Kato, col. 8, lines 20-22.) (See also Kato, FIG. 4.) Kato discloses that the first clock generating section 141 includes a plurality of electronic devices. In more detail, Kato discloses that the "[f]irst clock generating section 141 is comprised of an external resistor R1, a capacitor C1 and inverters Inv9-Inv10." (Kato, col. 8, lines 25-27.)

technology with corresponding manufacturing variations,	(See also Kato, FIG. 4.) Kato does not expressly disclose that the electronic devices are correspondingly constructed of the same process technology with corresponding manufacturing variations, Ledzius discloses electronic devices constructed of the same process technology with corresponding manufacturing variations. In more detail, Ledzius discloses: "The frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances. Accordingly, process caused variations are compensated because clock generator 18 is always physically made from the same batch and section of a semiconductor wafer as functional circuit 16." (Ledzius, col. 4, lines 9-14.) **Reason for modifying Kato according to Ledzius**: The prior art itself (i.e., Ledzius) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Ledzius to arrive at the claimed invention. In more detail, Ledzius provides that "process caused variations are compensated because clock generator 18 is always physically made from the same batch and section of a semiconductor wafer as functional circuit 16." (Ledzius, col. 4, lines 11-14.) Because Ledzius teaches that making components from the same batch and section of a semiconductor wafer compensates for process caused variations, Ledzius provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Ledzius. Therefore, it would have been obvious to modify Kato according to

	Ledzius.
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	This feature is taught by Kato, modified by Ledzius. Kato discloses that a speed of the data processing circuit and a frequency of a ring oscillator vary together due to an operating voltage. In more detail, Kato discloses: "When a ring oscillator is used, its output frequency lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of power supply voltage." (Kato, col. 11, lines 2-5.) Kato does not expressly disclose that these parameters vary together due to manufacturing variations and due to temperature. Ledzius discloses that a speed of functional circuit 16 and a frequency of clock generator 18 vary together due to process variations and due to temperature. In more detail, Ledzius discloses: "The frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances . . . Slowest signal path 38 of functional circuit 16 controls the true maximum speed. Accordingly, process variations which affect slowest signal path 38 also affect clock generator 18. Likewise, clock generator 18 physically resides near slowest signal path 38. Thus, a temperature change that affects slowest signal path 38 also affects clock generator 18." (Ledzius, col. 4, lines 9-11 and 15-21.) **Reason for modifying Kato according to Ledzius**: The prior art itself (i.e., Ledzius) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Ledzius to arrive at the claimed invention.

	In more detail, Ledzius provides that "process caused variations are compensated because clock generator 18 is always physically made from the same batch and section of a semiconductor wafer as functional circuit 16." (Ledzius, col. 4, lines 11-14.) Because Ledzius teaches that making components from the same batch and section of a semiconductor wafer compensates for process caused variations, Ledzius provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Ledzius. Therefore, it would have been obvious to modify Kato according to Ledzius.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and	This feature is taught by Kato. Kato discloses that the data processing circuit includes input-output port (PB) 27. (See Kato, col. 4, line 63 to col. 5, line 2, and FIG. 4, element 27.) In addition, Kato discloses that the "data processing circuit has a control bus 29 for supplying control signals to its components, and an address bus 30 for supplying address signals to some of its components, and a data bus 31 for transmitting data 5 to and from its components." (Kato, col. 5, lines 2-6.) (See also Kato, FIG. 4, elements 29, 30 and 31.)
a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface,	This feature is taught by Kato, modified by Amano. Kato discloses that the clock generating circuit comprises a first clock generator 14 and a second clock generator 15. (See Kato, col. 4, lines 37-38.) Regarding the second clock generator 15, Kato discloses that the "second clock generator 15 produces two clock signals Φa and Φb from the reference clock signal Φ0 output by first clock generator 14 . . . They are supplied to the components of the data processing circuit." (Kato, col.

	4, lines 56-62.) Kato does not expressly disclose that the second clock is independent of the first clock. Amano teaches a second clock independent of a system clock connected to said input/output interface.  FIG. 2 With reference to FIG. 2 (see above), Amano discloses that the main processor 11 has a CPU 21 and a keyboard interface unit (KBI) 23. Also, Amano discloses that the keyboard 12 has a keyboard controller (KBC) 34. (See Amano, col. 2, lines 59-63.) Further, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. (See Amano, col. 2, lines 57-59.) First, Amano teaches a second clock independent of a system clock. In this regard, Amano discloses that the clock of the keyboard controller 34 is independent of a system clock of the CPU 21. In more detail, Amano discloses: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling." (Amano, col. 7, lines 34-38.)

	Amano explicitly distinguishes its invention from the prior art, where the keyboard controller clock is supplied by the main system. Amano discloses: "In the prior art, the keyboard controller clock of the DEC VT-100 full keyboard is supplied from the main system, and the polling (from the CPU) period and the response (from the keyboard) period is defined by a synchronization clock, that is, the data transmission control between the CPU and the keyboard is done using a time multiplex method." (Amano, col. 7, lines 25-31.) Therefore, Amano teaches a second clock independent of a system clock. In addition, Amano at least implicitly discloses that the clock of the keyboard controller is connected to said input/output interface. As noted previously regarding FIG. 2, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. More specifically, FIG. 2 shows that the keyboard interface unit 23 and the keyboard controller 34 are connected by bidirectional line 13. As previously explained, Amano discloses that the keyboard controller 34 has an independent clock generator. Amano at least implicitly discloses that the independent clock generator controls generation of the keyboard controller's responses to the CPU polling. (See Amano, col. 7, lines 34-38: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling.") In order for Amano's main processor 11 to properly interpret the responses generated by the keyboard controller 34, one skilled in the art would understand that the clock of the keyboard controller 34 (which controls the generation of the responses) is supplied to the keyboard

	interface unit 23 via bidirectional line 13. Because it would be understood by one skilled in the art that Amano's keyboard controller clock is supplied to the keyboard interface unit 23, Amano at least implicitly discloses that the clock of the keyboard controller 34 is connected to the input/output interface (i.e., keyboard interface unit 23). **Reason for modifying Kato according to Amano**: The prior art itself (i.e., Amano) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "limit[s] the duty time of the central processing unit and its memory by designing the keyboard with a keyboard controller integrally fabricated as a single chip microprocessor." (Amano, col. 1, lines 53-59.) Further, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "reduces the number of signals between the main processor and the keyboard such that a very thin bidirectional cable therebetween can be used." (Amano, col. 7, lines 14-17.) Because Amano discloses that implementing independent clock generators limits the duty time of the CPU and its memory and reduces the number of signals between the main processor and the keyboard, Amano provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Amano. Therefore, it would have been obvious to modify Kato according to Amano.

wherein said central processing unit operates asynchronously to said input/output interface.	Kato does not expressly disclose that the CPU operates asynchronously to the input/output interface. This feature is disclosed in Amano. In more detail, Amano discloses "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling." (Amano, col. 7, lines 34-38.) Distinguishing its invention from the prior art, Amano discloses: "In the prior art, the keyboard controller clock of the DEC VT-100 full keyboard is supplied from the main system . . ." (Amano, col. 7, lines 25-27.) As such, Amano discloses that the keyboard controller clock is independent of the main system (CPU) clock and that the keyboard controller clock is unlike prior art, where the keyboard controller clock is supplied by the main system (CPU). Also, as previously explained, the keyboard controller clock is supplied to the input/output interface. Therefore, Amano discloses that the CPU -- which operates according to the main system (CPU) clock -- operates asynchronously to the keyboard interface --which operates according to the key controller clock that is independent of the main system (CPU) clock. **Reason for modifying Kato according to Amano**: The prior art itself (i.e., Amano) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention.

	In more detail, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "limit[s] the duty time of the central processing unit and its memory by designing the keyboard with a keyboard controller integrally fabricated as a single chip microprocessor." (Amano, col. 1, lines 53-59.) Further, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "reduces the number of signals between the main processor and the keyboard such that a very thin bidirectional cable therebetween can be used." (Amano, col. 7, lines 14-17.) Because Amano discloses that implementing independent clock generators limits the duty time of the CPU and its memory and reduces the number of signals between the main processor and the keyboard, Amano provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Amano. Therefore, it would have been obvious to modify Kato according to Amano.
Claim 12	**Kato, Ledzius and Amano**
The microprocessor system of claim 11, in which said second clock is a fixed frequency clock.	As explained above, Kato, Ledzius and Amano disclose the limitations of base claim 11. The limitations of claim 12 are at least implicitly disclosed in Amano. As previously noted, Amano discloses that the keyboard controller clock controls generation of responses by the keyboard controller 34 responsive to polling by the CPU 21. Amano discloses that the responses are sent according to a designed (fixed) timing.

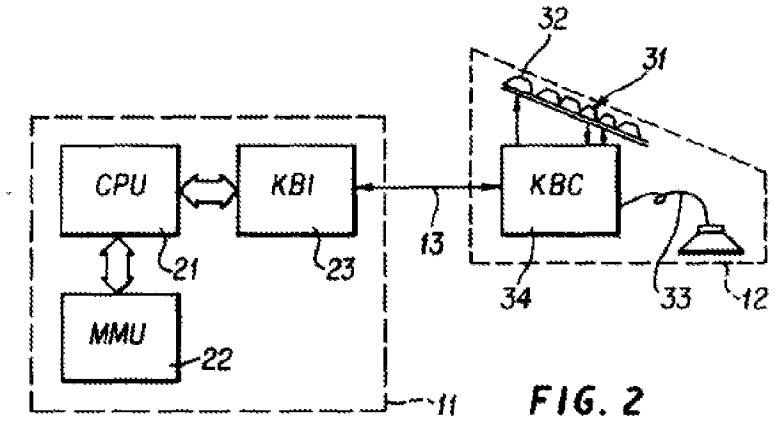
	Regarding the transmission of the responses from the keyboard controller 34 to the main system 11, Amano discloses that "to transmit the keyboard data to the side of the main processor, the microprocessor [of the keyboard controller 23] makes its P27 terminal zero and the communication interface unit 41 makes its RCV terminal active. The microprocessor 46 sends the start bit in this way and then transmits the succeeding data, parity bit and stop bits in the requisite order to the main processor 11 at the designed timing." (Amano, col. 5, lines 46-53.) Because Amano discloses that the sending of data (which is controlled by the keyboard controller clock) is performed at a designed (fixed) timing, Amano at least implicitly discloses that the keyboard controller clock is a fixed frequency clock. Therefore, Amano at least implicitly discloses that the second clock is a fixed frequency clock. **Reason for modifying Kato according to Amano**: It would have been obvious to modify Kato according to Amano because one of ordinary skill in the art could have substituted the fixed frequency clock of Amano in Kato in order to obtain predictable results. For example, as disclosed in Amano, a fixed frequency clock may be used to send data at a designed (fixed) timing. Because such a result would have been predictable, it would have been obvious to modify Kato according to Amano by substituting the fixed frequency clock of Amano in Kato.
Claim 13	**Kato, Ledzius and Amano**
13. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit	This feature is taught by Kato. Kato discloses a "one-chip semiconductor device comprising a semiconductor substrate and a data processing IC, e.g., a microcomputer and a microprocessor, formed on the substrate." (Kato, col. 1, lines 7-10.)

substrate,	
said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;	This feature is taught by Kato. Kato discloses that the clock generating circuit comprises a first clock generator 14 and a second clock generator 15. Kato discloses that signals produced by the second clock generator 15 are supplied to the data processing circuit. (See Kato, col. 4, lines 56-62: the "second clock generator 15 produces two clock signals Φa and Φb from the reference clock signal Φ0 output by first clock generator 14 . . . They are supplied to the components of the data processing circuit.") Therefore, Kato discloses that the data processing circuit operates at a processing frequency. Kato discloses that the "one-chip semiconductor device shown in FIG. 4 includes a data processing circuit comprised of dynamic circuit elements." (Kato, col. 8, lines 20-22.) (See also Kato, FIG. 4.) Therefore, Kato discloses the data processing circuit is constructed of a plurality of electronic devices.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit,	This feature is taught by Kato. In more detail, Kato discloses that the "first clock generating section 141 may be replaced by a ring oscillator of the known type or a CR clock oscillator similar which is completely built on semiconductor substrate 10. When a ring oscillator is used, its output frequency lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of power supply voltage." (Kato, col. 10, line 67 to col. 11, line 5.) Further, Kato discloses that the first clock generating section 141 is connected to the data processing IC. For example, Kato discloses that the "[f]irst clock generating section 141 is comprised of an external resistor

	R1, a capacitor C1 and inverters Inv9-Inv10. It generates a first clock signal Φ01 of a first frequency f0 determined by the logical threshold voltage of inverter Inv9, the resistance of resistor R1 and the capacitance of capacitor C1." (Kato, col. 8, lines 25-30.) Either the first clock signal Φ01 or another clock signal (i.e., second clock signal Φ01) is sent to the second clock generating circuit 15. (See Kato, col. 7, lines 35-39.) As previously noted, signals generated by the second clock generating circuit 15 are supplied to the components of the data processing circuit. (See Kato, col. 4, lines 56-62.) Because Kato discloses that the first clock generating section 141 is connected to the data processing circuit via the second clock generating circuit 15, Kato discloses that the first clock generating section 141 is connected to the data processing circuit.
said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,	This feature is disclosed in Kato. As previously noted, Kato discloses that the first clock generating section 141 produces a first clock signal. In more detail, Kato discloses that the "[f]irst clock generating section 141 is comprised of an external resistor R1, a capacitor C1 and inverters Inv9-Inv10. It generates a first clock signal Φ01 of a first frequency f0 determined by the logical threshold voltage of inverter Inv9, the resistance of resistor R1 and the capacitance of capacitor C1." (Kato, col. 8, lines 25-30.) Therefore, Kato discloses that the first clock generating section 141 clocks the data processing IC at a clock rate. Also, Kato discloses that the first clock generating section 141 is constructed of a plurality of electronic devices – i.e., external resistor R1, a capacitor C1 and inverters Inv9-Inv10 (see Kato, col. 8, lines 25-27, and FIG. 4, element 141.)

thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	This feature is disclosed in Kato, modified by Ledzius. Kato does not expressly disclose these features. Ledzius discloses that a signal path of a functional circuit (which controls the true maximum speed) and a clock generator vary in the same way as a function of fabrication (process) or operational (temperature) parameters, thereby enabling the signal path to track the clock generator in response to said variation (e.g., a temperature change that affects slowest signal path 38 also affects clock generator 18). In more detail, Ledzius discloses: "The frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances. Accordingly, process caused variations are compensated because clock generator 18 is always physically made from the same batch and section of a semiconductor wafer as functional circuit 16. Slowest signal path 38 of functional circuit 16 controls the true maximum speed. Accordingly, process variations which affect slowest signal path 38 also affect clock generator 18. Likewise, clock generator 18 physically resides near slowest signal path 38. Thus, a temperature change that affects slowest signal path 38 also affects clock generator 18." (Ledzius, col. 4, lines 9-21.) **Reason for modifying Kato according to Ledzius**: The prior art itself (i.e., Ledzius) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Ledzius to arrive at the claimed invention. In more detail, Ledzius provides that "process caused variations are compensated because clock generator 18 is always physically made from the same batch and section of a semiconductor wafer as functional circuit

	16." (Ledzius, col. 4, lines 11-14.) Because Ledzius teaches that making components from the same batch and section of a semiconductor wafer compensates for process caused variations, Ledzius provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Ledzius. Therefore, it would have been obvious to modify Kato according to Ledzius.
an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	This feature is disclosed by Kato. Kato discloses that the data processing circuit includes input-output port (PB) 27. (See Kato, col. 4, line 63 to col. 5, line 2, and FIG. 4, element 27.) Also, Kato discloses that "[t]he data processing circuit processes the data input from the external device through terminals . . . PBO-PB3 and supplies the processed data to the external device through terminals PBO-PB3[.]" Therefore, Kato discloses an on-chip input/output interface connected between the central processing unit (data processing circuit) and an off-chip external memory bus (it is inherent that the external device is off-chip and that the external device has a memory bus). In addition, Kato discloses that the "data processing circuit has a control bus 29 for supplying control signals to its components, and an address bus 30 for supplying address signals to some of its components, and a data bus 31 for transmitting data 5 to and from its components." (Kato, col. 5, lines 2-6.) (See also Kato, FIG. 4, elements 29, 30 and 31.) Therefore, Kato discloses an on-chip input/output interface connected

	between the CPU (data processing circuit) and an off-chip external memory bus for facilitating exchange of control signals, addresses and data with the CPU.
an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and	This feature is taught by Kato, modified by Amano. Kato discloses that the clock generating circuit comprises a first clock generator 14 and a second clock generator 15. (See Kato, col. 4, lines 37-38.) Regarding the second clock generator 15, Kato discloses that the "second clock generator 15 produces two clock signals Φa and Φb from the reference clock signal Φ0 output by first clock generator 14 . . . They are supplied to the components of the data processing circuit." (Kato, col. 4, lines 56-62.) Kato does not expressly disclose that the second clock is off-chip, independent of the first clock generator and operative at a frequency independent of a clock frequency of the first clock generator. Amano teaches an off-chip external clock independent of a system clock, connected to said input/output interface, wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock.  FIG. 2 With reference to FIG. 2 (see above), Amano discloses that the main processor 11 has a CPU 21 and a keyboard interface unit (KBI) 23. Also,

	Amano discloses that the keyboard 12 has a keyboard controller (KBC) 34. (See Amano, col. 2, lines 59-63.) Further, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. (See Amano, col. 2, lines 57-59.) First, Amano teaches an off-chip external clock independent of a system clock, wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock. In this regard, Amano discloses that the clock of the keyboard controller 34 is independent of a system clock of the CPU 21, wherein the keyboard controller clock is operative at a frequency independent of a clock frequency of the system clock. In more detail, Amano discloses: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling." (Amano, col. 7, lines 34-38.) Amano explicitly distinguishes its invention from the prior art, where the keyboard controller clock is supplied by the main system. Amano discloses: "In the prior art, the keyboard controller clock of the DEC VT-100 full keyboard is supplied from the main system, and the polling (from the CPU) period and the response (from the keyboard) period is defined by a synchronization clock, that is, the data transmission control between the CPU and the keyboard is done using a time multiplex method." (Amano, col. 7, lines 25-31.) Therefore, Amano teaches an off-chip external clock independent of a system clock, wherein the off-chip external clock is operative at a

	frequency independent of a clock frequency of the system clock. In addition, Amano at least implicitly discloses that the clock of the keyboard controller is connected to the input/output interface. As noted previously regarding FIG. 2, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. More specifically, FIG. 2 shows that the keyboard interface unit 23 and the keyboard controller 34 are connected by bidirectional line 13. As previously explained, Amano discloses that the keyboard controller 34 has an independent clock generator. Amano at least implicitly discloses that the independent clock generator controls generation of the keyboard controller's responses to the CPU polling. (See Amano, col. 7, lines 34-38: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling.") In order for Amano's main processor 11 to properly interpret the responses generated by the keyboard controller 34, one skilled in the art would understand that the clock of the keyboard controller 34 (which controls the generation of the responses) is supplied to the keyboard interface unit 23 via bidirectional line 13. Because it would be understood by one skilled in the art that Amano's keyboard controller clock is supplied to the keyboard interface unit 23, Amano at least implicitly discloses that the clock of the keyboard controller 34 is connected to the input/output interface (i.e., keyboard interface unit 23). **Reason for modifying Kato according to Amano**: The prior art itself (i.e., Amano) provides teaching, suggestion, and motivation that would

	have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "limit[s] the duty time of the central processing unit and its memory by designing the keyboard with a keyboard controller integrally fabricated as a single chip microprocessor." (Amano, col. 1, lines 53-59.) Further, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "reduces the number of signals between the main processor and the keyboard such that a very thin bidirectional cable therebetween can be used." (Amano, col. 7, lines 14-17.) Because Amano discloses that implementing independent clock generators limits the duty time of the CPU and its memory and reduces the number of signals between the main processor and the keyboard, Amano provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Amano. Therefore, it would have been obvious to modify Kato according to Amano.
further wherein said central processing unit operates asynchronously to said input/output interface.	Kato does not expressly disclose that the CPU operates asynchronously the input/output interface. This feature is disclosed in Amano. In more detail, Amano discloses "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling." (Amano, col. 7, lines 34-38.)

	Distinguishing its invention from the prior art, Amano discloses: "In the prior art, the keyboard controller clock of the DEC VT-100 full keyboard is supplied from the main system . . ." (Amano, col. 7, lines 25-27.) As such, Amano discloses that the keyboard controller clock is independent of the main system (CPU) clock and that the keyboard controller clock is unlike prior art, where the keyboard controller clock is supplied by the main system (CPU). Also, as previously explained, the keyboard controller clock is supplied to the input/output interface. Therefore, Amano discloses that the CPU -- which operates according to the main system (CPU) clock -- operates asynchronously to the keyboard interface --which operates according to the key controller clock that is independent of the main system (CPU) clock. **Reason for modifying Kato according to Amano**: The prior art itself (i.e., Amano) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "limit[s] the duty time of the central processing unit and its memory by designing the keyboard with a keyboard controller integrally fabricated as a single chip microprocessor." (Amano, col. 1, lines 53-59.) Further, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "reduces the number of signals between the main processor

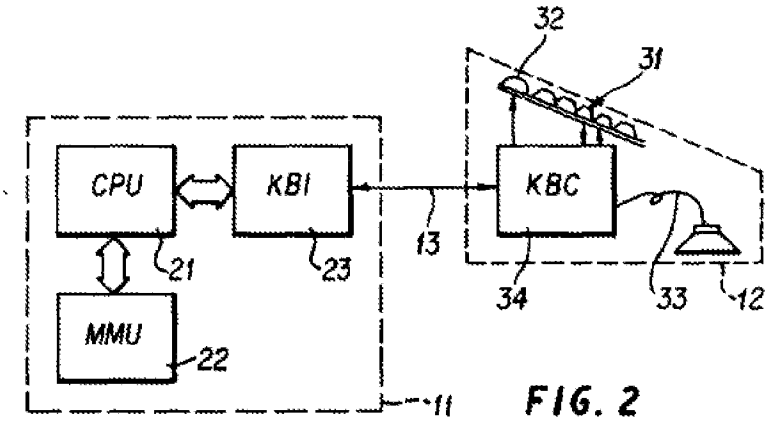
	and the keyboard such that a very thin bidirectional cable therebetween can be used." (Amano, col. 7, lines 14-17.) Because Amano discloses that implementing independent clock generators limits the duty time of the CPU and its memory and reduces the number of signals between the main processor and the keyboard, Amano provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Amano. Therefore, it would have been obvious to modify Kato according to Amano.
Claim 14	**Kato, Ledzius and Amano**
14. The microprocessor system of claim 13, wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	As explained above, Kato, Ledzius and Amano disclose the limitations of base claim 13. The limitations of claim 14 are disclosed in Kato. Kato discloses that a speed of the data processing circuit and a frequency of a ring oscillator vary together due to an operating voltage. In more detail, Kato discloses: "When a ring oscillator is used, its output frequency lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of power supply voltage." (Kato, col. 11, lines 2-5.)
Claim 15	**Kato, Ledzius and Amano**
15. The microprocessor system of claim 13 wherein said oscillator comprises a ring oscillator.	As explained above, Kato, Ledzius and Amano disclose the limitations of base claim 13. The limitations of claim 15 are disclosed in Kato. Kato discloses that the "first clock generating section 141 may be replaced by a ring oscillator of the known type or a CR clock oscillator similar which is completely built on semiconductor substrate 10. When a ring oscillator is used, its output frequency lowers in proportion to the

	speed of the data processing circuit which is lowered due to the drop of power supply voltage." (Kato, col. 10, line 67 to col. 11, line 5.)
Claim 16	**Kato, Ledzius and Amano**
16. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:	This feature is taught by Kato. Kato discloses a "one-chip semiconductor device comprising a semiconductor substrate and a data processing IC, e.g., a microcomputer and a microprocessor, formed on the substrate." (Kato, col. 1, lines 7-10.) Further, Kato discloses "The clock generating circuit generates clock signals and supplies them to the data processing circuit." (Kato, col. 4, lines 34-36.)
providing said central processing unit upon an integrated circuit substrate,	This feature is taught by Kato. Kato discloses a "one-chip semiconductor device comprising a semiconductor substrate and a data processing IC, e.g., a microcomputer and a microprocessor, formed on the substrate." (Kato, col. 1, lines 7-10.)
said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	This feature is taught by Kato. Kato discloses that the "one-chip semiconductor device shown in FIG. 4 includes a data processing circuit comprised of dynamic circuit elements." (Kato, col. 8, lines 20-22.) (See also Kato, FIG. 4.) Therefore, Kato discloses the data processing circuit is constructed of a plurality of electronic devices. It is inherent that these electronic devices (e.g., program counter 16, program memory (ROM) 167, instruction decoder (IR) 18, etc.) may be constructed of a plurality of transistors. Kato discloses that the clock generating circuit comprises a first clock generator 14 and a second clock generator 15. Kato discloses that signals produced by the second clock generator 15 are supplied to the data

	processing circuit. (See Kato, col. 4, lines 56-62: the "second clock generator 15 produces two clock signals Φa and Φb from the reference clock signal Φ0 output by first clock generator 14 . . . They are supplied to the components of the data processing circuit.") Therefore, Kato discloses that the data processing circuit operates at a processing frequency.
providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	This feature is taught by Kato. In more detail, Kato discloses that the "first clock generating section 141 may be replaced by a ring oscillator of the known type or a CR clock oscillator similar which is completely built on semiconductor substrate 10. When a ring oscillator is used, its output frequency lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of power supply voltage." (Kato, col. 10, line 67 to col. 11, line 5.) Further, Kato discloses that the "[f]irst clock generating section 141 is comprised of an external resistor R1, a capacitor C1 and inverters Inv9-Inv10." (Kato, col. 8, lines 25-27.) It is inherent that such devices (e.g., the inverters) may be constructed of a plurality of transistors.
clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or	This feature is disclosed in Kato, modified by Ledzius. Kato does not expressly disclose these features. Ledzius discloses that the frequency of the clock signal varies depending on process and temperature variances. Also, Ledzius discloses that a signal path of a functional circuit (which controls the true maximum speed) and the clock generator vary in the same way relative to variations in fabrication (process) or operational (temperature) parameters. In more detail, Ledzius discloses: "The frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances. Accordingly, process caused variations are compensated

operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	because clock generator 18 is always physically made from the same batch and section of a semiconductor wafer as functional circuit 16. Slowest signal path 38 of functional circuit 16 controls the true maximum speed. Accordingly, process variations which affect slowest signal path 38 also affect clock generator 18. Likewise, clock generator 18 physically resides near slowest signal path 38. Thus, a temperature change that affects slowest signal path 38 also affects clock generator 18." (Ledzius, col. 4, lines 9-21.) **Reason for modifying Kato according to Ledzius**: The prior art itself (i.e., Ledzius) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Ledzius to arrive at the claimed invention. In more detail, Ledzius provides that "process caused variations are compensated because clock generator 18 is always physically made from the same batch and section of a semiconductor wafer as functional circuit 16." (Ledzius, col. 4, lines 11-14.) Because Ledzius teaches that making components from the same batch and section of a semiconductor wafer compensates for process caused variations, Ledzius provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Ledzius. Therefore, it would have been obvious to modify Kato according to Ledzius.
connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and	This feature is disclosed by Kato. Kato discloses that the data processing circuit includes input-output port (PB) 27. (See Kato, col. 4, line 63 to col. 5, line 2, and FIG. 4, element 27.)

exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	Also, Kato discloses that "[t]he data processing circuit processes the data input from the external device through terminals . . . PBO-PB3 and supplies the processed data to the external device through terminals PBO-PB3[.]" Therefore, Kato discloses connecting an on-chip input/output interface between the central processing unit (data processing circuit) and an off-chip external memory bus (it is inherent that the external device is off-chip and that the external device has a memory bus). In addition, Kato discloses that the "data processing circuit has a control bus 29 for supplying control signals to its components, and an address bus 30 for supplying address signals to some of its components, and a data bus 31 for transmitting data 5 to and from its components." (Kato, col. 5, lines 2-6.) (See also Kato, FIG. 4, elements 29, 30 and 31.) Therefore, Kato discloses exchange of control signals, addresses and data between the input/output interface and the CPU (data processing circuit).
clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock,	This feature is taught by Kato, modified by Amano. Kato discloses that the clock generating circuit comprises a first clock generator 14 and a second clock generator 15. (See Kato, col. 4, lines 37-38.) Regarding the second clock generator 15, Kato discloses that the "second clock generator 15 produces two clock signals Φa and Φb from the reference clock signal Φ0 output by first clock generator 14 . . . They are supplied to the components of the data processing circuit." (Kato, col. 4, lines 56-62.) Kato does not expressly disclose that the second clock is off-chip and operative at a frequency independent of a clock frequency of the first clock generator.

	Amano teaches an off-chip external clock for clocking said input/output interface, wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock.  FIG. 2 With reference to FIG. 2 (see above), Amano discloses that the main processor 11 has a CPU 21 and a keyboard interface unit (KBI) 23. Also, Amano discloses that the keyboard 12 has a keyboard controller (KBC) 34. (See Amano, col. 2, lines 59-63.) Further, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. (See Amano, col. 2, lines 57-59.) First, Amano teaches an off-chip external clock independent of a system clock, wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock. In this regard, Amano discloses that the clock of the keyboard controller 34 is independent of a system clock of the CPU 21, wherein the keyboard controller clock is operative at a frequency independent of a clock frequency of the system clock. In more detail, Amano discloses: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling." (Amano, col. 7,

	lines 34-38.) Amano explicitly distinguishes its invention from the prior art, where the keyboard controller clock is supplied by the main system. Amano discloses: "In the prior art, the keyboard controller clock of the DEC VT-100 full keyboard is supplied from the main system, and the polling (from the CPU) period and the response (from the keyboard) period is defined by a synchronization clock, that is, the data transmission control between the CPU and the keyboard is done using a time multiplex method." (Amano, col. 7, lines 25-31.) Therefore, Amano teaches an off-chip external clock independent of a system clock, wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock. In addition, Amano at least implicitly discloses that the clock of the keyboard controller is for clocking the input/output interface. As noted previously regarding FIG. 2, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. More specifically, FIG. 2 shows that the keyboard interface unit 23 and the keyboard controller 34 are connected by bidirectional line 13. As previously explained, Amano discloses that the keyboard controller 34 has an independent clock generator. Amano at least implicitly discloses that the independent clock generator controls generation of the keyboard controller's responses to the CPU polling. (See Amano, col. 7, lines 34-38: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling.") In order for Amano's main processor 11 to properly interpret the

	responses generated by the keyboard controller 34, one skilled in the art would understand that the clock of the keyboard controller 34 (which controls the generation of the responses) is supplied to the keyboard interface unit 23 via bidirectional line 13. Because it would be understood by one skilled in the art that Amano's keyboard controller clock is supplied to the keyboard interface unit 23, Amano at least implicitly discloses that the clock of the keyboard controller 34 is connected to the input/output interface (i.e., keyboard interface unit 23) for clocking the input/output interface. **Reason for modifying Kato according to Amano**: The prior art itself (i.e., Amano) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "limit[s] the duty time of the central processing unit and its memory by designing the keyboard with a keyboard controller integrally fabricated as a single chip microprocessor." (Amano, col. 1, lines 53-59.) Further, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "reduces the number of signals between the main processor and the keyboard such that a very thin bidirectional cable therebetween can be used." (Amano, col. 7, lines 14-17.) Because Amano discloses that implementing independent clock generators limits the duty time of the CPU and its memory and reduces the number of signals between the main processor and the keyboard, Amano provides teaching, suggestion and motivation that would have led

	one of ordinary skill to modify Kato according to Amano. Therefore, it would have been obvious to modify Kato according to Amano.
wherein said central processing unit operates asychronously to said input/output interface.	Kato does not expressly disclose that the CPU operates asynchronously to the input/output interface. This feature is disclosed in Amano. In more detail, Amano discloses "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling." (Amano, col. 7, lines 34-38.) Distinguishing its invention from the prior art, Amano discloses: "In the prior art, the keyboard controller clock of the DEC VT-100 full keyboard is supplied from the main system . . ." (Amano, col. 7, lines 25-27.) As such, Amano discloses that the keyboard controller clock is independent of the main system (CPU) clock and that the keyboard controller clock is unlike prior art, where the keyboard controller clock is supplied by the main system (CPU). Also, as previously explained, the keyboard controller clock is supplied to the input/output interface. Therefore, Amano discloses that the CPU -- which operates according to the main system (CPU) clock -- operates asynchronously to the keyboard interface --which operates according to the key controller clock that is independent of the main system (CPU) clock. **Reason for modifying Kato according to Amano**: The prior art itself (i.e., Amano) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to

	arrive at the claimed invention. In more detail, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "limit[s] the duty time of the central processing unit and its memory by designing the keyboard with a keyboard controller integrally fabricated as a single chip microprocessor." (Amano, col. 1, lines 53-59.) Further, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "reduces the number of signals between the main processor and the keyboard such that a very thin bidirectional cable therebetween can be used." (Amano, col. 7, lines 14-17.) Because Amano discloses that implementing independent clock generators limits the duty time of the CPU and its memory and reduces the number of signals between the main processor and the keyboard, Amano provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Amano. Therefore, it would have been obvious to modify Kato according to Amano.

B) Detailed Explanation for Proposed Rejections Based on Amano and Intel 8251A

Requester respectfully submits that claims 1, 2, 6, 7 and 9-16 of the '336 reexamination certificate are rendered obvious under 35 U.S.C. § 103 by previously cited references Kato and Ledzius in view of newly cited Amano, further in view of Intel 8251A.

Table 2 below details how Kato, Ledzius, Amano and Intel 8251A disclose each and every limitation recited in claims 1, 2, 6, 7 and 9-16 of the '336 reexamination certificate.

As previously explained, Kato, Ledzius and Amano constitute effective prior art under 35 U.S.C. § 103.

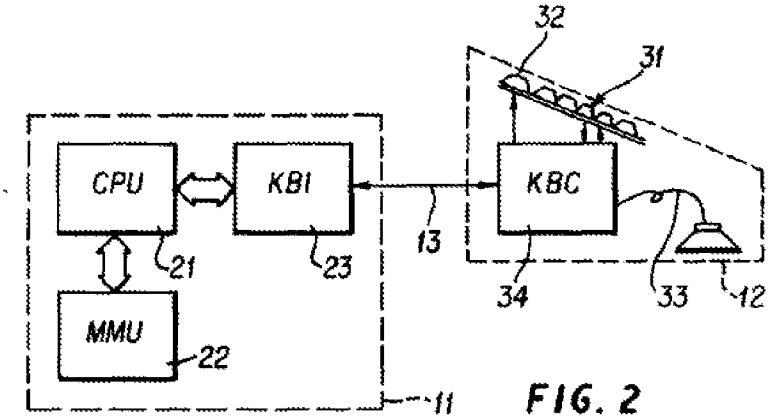
Intel 8251A was published not later than 1981. Accordingly, Intel 8251A also constitutes effective prior art under 35 U.S.C. § 103.

Intel 8251A is directed to the enhanced version of the Intel 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART). Intel 8251A discloses that the 8251A is programmed by the CPU to operate using any serial data transmission technique. The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. (See Intel 8251A, page 8-43.)

Table 2
Comparison of the '336 reexamination certificate claims to Kato, Ledzius, Amano and Intel 8251A

Claim 1	Kato, Ledzius, Amano and Intel 8251A
1. A microprocessor system, comprising a single integrated circuit including	Please see corresponding analysis in Table 1.
a central processing unit and	Please see corresponding analysis in Table 1.
an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	Please see corresponding analysis in Table 1.
said central processing unit and said ring oscillator variable speed system clock each including	Please see corresponding analysis in Table 1.

a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	Please see corresponding analysis in Table 1.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central	Please see corresponding analysis in Table 1.

processing unit; and	
a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface,	This feature is taught by Kato, modified by Amano, in view of Intel 8251A. Kato discloses that the clock generating circuit comprises a first clock generator 14 and a second clock generator 15. (See Kato, col. 4, lines 37-38.) Regarding the second clock generator 15, Kato discloses that the "second clock generator 15 produces two clock signals Φa and Φb from the reference clock signal Φ0 output by first clock generator 14 . . . They are supplied to the components of the data processing circuit." (Kato, col. 4, lines 56-62.) Kato does not expressly disclose that the second clock is independent of the first clock. Amano, in view of Intel 8251A, teaches a second clock independent of a system clock connected to said input/output interface.  FIG. 2 With reference to FIG. 2 (see above), Amano discloses that the main processor 11 has a CPU 21 and a keyboard interface unit (KBI) 23. Also, Amano discloses that the keyboard 12 has a keyboard controller (KBC) 34. (See Amano, col. 2, lines 59-63.) Further, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. (See Amano, col. 2, lines 57-59.)

	First, Amano teaches a second clock independent of a system clock. In this regard, Amano discloses that the clock of the keyboard controller 34 is independent of a system clock of the CPU 21. In more detail, Amano discloses: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling." (Amano, col. 7, lines 34-38.) Amano explicitly distinguishes its invention from the prior art, where the keyboard controller clock is supplied by the main system. Amano discloses: "In the prior art, the keyboard controller clock of the DEC VT-100 full keyboard is supplied from the main system, and the polling (from the CPU) period and the response (from the keyboard) period is defined by a synchronization clock, that is, the data transmission control between the CPU and the keyboard is done using a time multiplex method." (Amano, col. 7, lines 25-31.) Therefore, Amano discloses a second clock independent of a system clock. In addition, Amano at least implicitly discloses that the clock of the keyboard controller is connected to said input/output interface. As noted previously regarding FIG. 2, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. More specifically, FIG. 2 shows that the keyboard interface unit 23 and the keyboard controller 34 are connected by bidirectional line 13.

	As previously explained, Amano discloses that the keyboard controller 34 has an independent clock generator. Amano at least implicitly discloses that the independent clock generator controls generation of the keyboard controller's responses to the CPU polling. (See Amano, col. 7, lines 34-38: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling.") In order for Amano's main processor 11 to properly interpret the responses generated by the keyboard controller 34, one skilled in the art would understand that the clock of the keyboard controller 34 (which controls the generation of the responses) is supplied to the keyboard interface unit 23 via bidirectional line 13. Because it would be understood by one skilled in the art that Amano's keyboard controller clock is supplied to the keyboard interface unit 23, Amano at least implicitly discloses that the clock of the keyboard controller 34 is connected to the input/output interface (i.e., keyboard interface unit 23). Furthermore, Amano in view of Intel 8251A discloses that the clock of the keyboard controller is connected to said input/output interface. As noted previously regarding FIG. 2, Amano discloses that the main processor 11 has the CPU 21 and the keyboard interface unit (KBI) 23. The keyboard interface unit (KBI) 23 is connected to the keyboard controller 34 by bidirectional line 13.

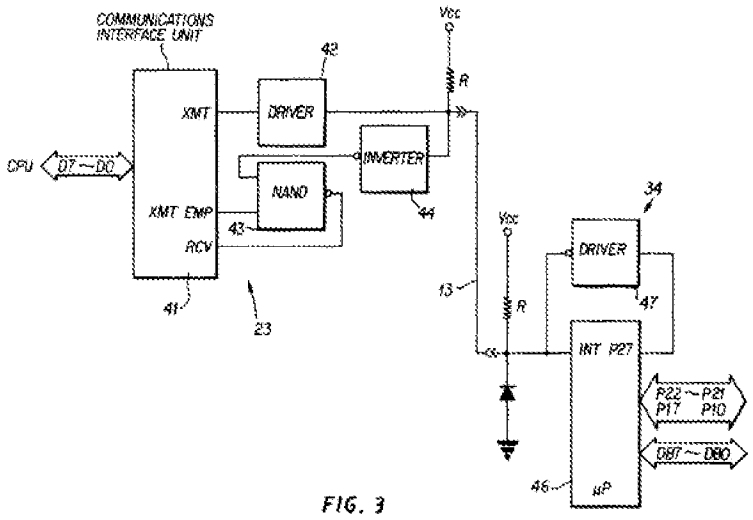


FIG. 3

With reference to FIG. 3 (see above), Amano discloses that the keyboard interface unit 23 includes a communication interface unit 41 for receiving series data from the keyboard controller 34 and for converting the series data to parallel data for transmission to the CPU. (See Amano, col. 2, line 64 to col. 3, line 4.)

Regarding the communication interface unit 41, Amano discloses that this unit may be implemented by the Intel 8251A programmable communication interface. In more detail, Amano discloses: "In this embodiment, the communication interface unit 41 used is a programmable communication interface I 8251A produced by Intel Corp. The programmable communication interface is a programmable element used as peripheral circuits for microprocessors, and is capable of performing the functions as explained above. The programmable communication interface I 8251A is explained in detail in the Intel Component Data Catalog 1979 P11.24-P11.31." (Amano, col. 3, lines 8-17.)

It is believed that relevant portions of Intel 8251A (which corresponds to the Intel Component Data Catalog 1981) are substantially similar to the 1979 catalog referenced by Amano.

As previously noted, Amano discloses that the communication interface unit 41 (i.e., the Intel 8251A interface) receives series data from the keyboard controller. Regarding the receiving of data, Amano discloses: "The communication interface unit 41 [i.e., the Intel 8251A interface] performs functions identified by the output leads as a transmitter data terminal (XMT), a transmitter empty terminal (XMT EMP) and a receiver terminal (RCV) . . . RCV: The terminal receives series characters from the keyboard to convert them to parallel characters for data of the CPU." (Amano, col. 3, lines 17-21 and 38-41.) Further, Amano discloses: "The series data from the keyboard controller are received at the RCV terminal of the communication interface unit 41 where the data are processed as the data of the keyboard." (Amano, col. 5, lines 31-34.)

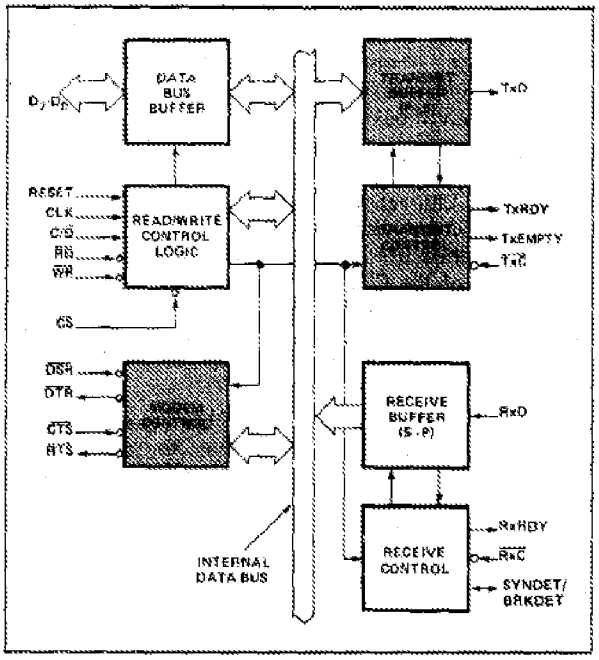


Figure 4. 8251A Block Diagram Showing Modem and Transmitter Buffer and Control Functions

Regarding the receiving function, Intel 8251A discloses that the Receive Buffer (see Figure 4, above) performs the functions described in Amano. Intel 8251A discloses that the "Receiver accepts serial data,

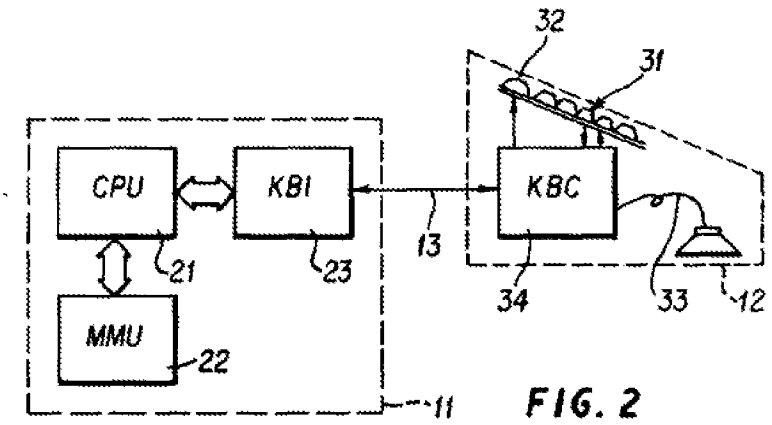
	converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an 'assembled' character to the CPU." (Intel 8251A, page 8-47.) Further, Intel 8251A discloses that the received serial data is clocked to the Receiver Clock signal (RxC). In more detail, Intel 8251A discloses: "Serial data is input to RxD pin, and is clocked in on the rising edge of RxC." (Intel 8251A, page 8-47.) Figure 4 of Intel 8251A shows that both the RxD pin and the RxC pin are input pins. Regarding the Receiver Clock that is input to the RxC pin, Intel 8251A discloses: "The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the Baud Rate (1x) is equal to the actual frequency of RxC. In Asynchronous Mode, the Baud Rate is a fraction of the actual RxC frequency." (Intel 8251A, page 8-47.) As such, Intel 8251A discloses that serial data received by the interface are clocked to rising edges of the Receiver Clock, which is also received by the interface. One skilled in the art would understand that, when the Intel 8251A interface is implemented as the communication interface unit 41 of Amano, the Receiver Clock input to the Intel 8251A corresponds to the clock of the keyboard controller 34. As previously noted, the keyboard controller clock controls the generation of the polling responses by the keyboard controller 34. Because Amano in view of Intel 8251A discloses that the keyboard controller clock is input to the input/output interface (i.e., to the RxC input pin of the Intel 8251A interface), Amano in view of Intel 8251A

	discloses that the clock of the keyboard controller 34 is input to the input/output interface (i.e., keyboard interface unit 23). Therefore, Amano in view of Intel 8251A discloses that the second clock is connected to the input/output interface. **Reason for modifying Kato according to Amano in view of Intel 8251A**: The prior art itself (i.e., Amano) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A to arrive at the claimed invention. In more detail, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "limit[s] the duty time of the central processing unit and its memory by designing the keyboard with a keyboard controller integrally fabricated as a single chip microprocessor." (Amano, col. 1, lines 53-59.) Further, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "reduces the number of signals between the main processor and the keyboard such that a very thin bidirectional cable therebetween can be used." (Amano, col. 7, lines 14-17.) Because Amano discloses that implementing independent clock generators limits the duty time of the CPU and its memory and reduces the number of signals between the main processor and the keyboard, Amano provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A. Therefore, it would have been obvious to modify Kato

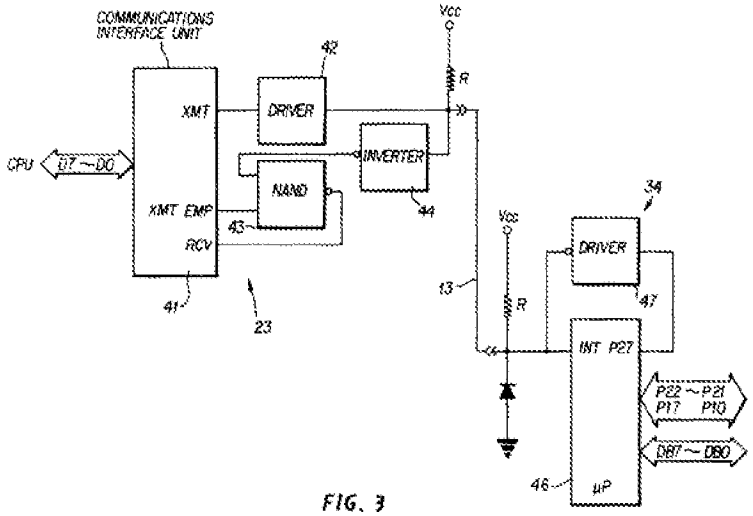
	according to Amano in view of Intel 8251A.
wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.	Please see corresponding analysis in Table 1.
Claim 2	**Kato, Ledzius, Amano and Intel 8251A**
2. The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	Please see corresponding analysis in Table 1.
Claim 6	**Kato, Ledzius, Amano and Intel 8251A**
6. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate,	Please see corresponding analysis in Table 1.
said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices:	Please see corresponding analysis in Table 1.
an entire oscillator disposed upon said	Please see corresponding analysis in Table 1.

integrated circuit substrate and connected to said central processing unit,	
said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,	Please see corresponding analysis in Table 1.
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to	Please see corresponding analysis in Table 1.

said parameter variation;	
an on-chip input/output interface connected between said central processing unit and an off-chip external memory bus for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	Please see corresponding analysis in Table 1.
an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and	This feature is taught by Kato, modified by Amano in view of Intel 8251A. Kato discloses that the clock generating circuit comprises a first clock generator 14 and a second clock generator 15. (See Kato, col. 4, lines 37-38.) Regarding the second clock generator 15, Kato discloses that the "second clock generator 15 produces two clock signals Φa and Φb from the reference clock signal Φ0 output by first clock generator 14 . . . They are supplied to the components of the data processing circuit." (Kato, col. 4, lines 56-62.) Kato does not expressly disclose that the second clock is off-chip, independent of the first clock generator and operative at a frequency independent of a clock frequency of the first clock generator. Amano, in view of Intel 8251A, teaches an off-chip external clock independent of a system clock, connected to said input/output interface,

	wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock.  FIG. 2 With reference to FIG. 2 (see above), Amano discloses that the main processor 11 has a CPU 21 and a keyboard interface unit (KBI) 23. Also, Amano discloses that the keyboard 12 has a keyboard controller (KBC) 34. (See Amano, col. 2, lines 59-63.) Further, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. (See Amano, col. 2, lines 57-59.) First, Amano teaches an off-chip external clock independent of a system clock, wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock. In this regard, Amano discloses that the clock of the keyboard controller 34 is independent of a system clock of the CPU 21, wherein the keyboard controller clock is operative at a frequency independent of a clock frequency of the system clock. In more detail, Amano discloses: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling." (Amano, col. 7, lines 34-38.)

	Amano explicitly distinguishes its invention from the prior art, where the keyboard controller clock is supplied by the main system. Amano discloses: "In the prior art, the keyboard controller clock of the DEC VT-100 full keyboard is supplied from the main system, and the polling (from the CPU) period and the response (from the keyboard) period is defined by a synchronization clock, that is, the data transmission control between the CPU and the keyboard is done using a time multiplex method." (Amano, col. 7, lines 25-31.) Therefore, Amano discloses an external clock independent of the system oscillator. In addition, Amano at least implicitly discloses that the clock of the keyboard controller is connected to the input/output interface. As noted previously regarding FIG. 2, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. More specifically, FIG. 2 shows that the keyboard interface unit 23 and the keyboard controller 34 are connected by bidirectional line 13. As previously explained, Amano discloses that the keyboard controller 34 has an independent clock generator. Amano at least implicitly discloses that the independent clock generator controls generation of the keyboard controller's responses to the CPU polling. (See Amano, col. 7, lines 34-38: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling.") In order for Amano's main processor 11 to properly interpret the

	responses generated by the keyboard controller 34, one skilled in the art would understand that the clock of the keyboard controller 34 (which controls the generation of the responses) is supplied to the keyboard interface unit 23 via bidirectional line 13. Because it would be understood by one skilled in the art that Amano's keyboard controller clock is supplied to the keyboard interface unit 23, Amano at least implicitly discloses that the clock of the keyboard controller 34 is connected to the input/output interface (i.e., keyboard interface unit 23). In addition, Amano in view of Intel 8251A discloses that the clock of the keyboard controller is connected to said input/output interface. As noted previously regarding FIG. 2, Amano discloses the main processor 11 has the CPU 21 and the keyboard interface unit (KBI) 23. The keyboard interface unit (KBI) 23 is connected to the keyboard controller 34 by bidirectional line 13.  FIG. 3 With reference to FIG. 3 (see above), Amano discloses that the keyboard interface unit 23 includes a communication interface unit 41 for receiving series data from the keyboard controller 34 and for converting the series data to parallel data for transmission to the CPU.

	(See Amano, col. 2, line 64 to col. 3, line 4.) Regarding the communication interface unit 41, Amano discloses that this unit may be implemented by the Intel 8251A programmable communication interface. In more detail, Amano discloses: "In this embodiment, the communication interface unit 41 used is a programmable communication interface I 8251A produced by Intel Corp. The programmable communication interface is a programmable element used as peripheral circuits for microprocessors, and is capable of performing the functions as explained above. The programmable communication interface I 8251A is explained in detail in the Intel Component Data Catalog 1979 P11.24-P11.31." (Amano, col. 3, lines 8-17.) It is believed that relevant portions of Intel 8251A (which corresponds to the Intel Component Data Catalog 1981) are substantially similar to the 1979 catalog referenced by Amano. As previously noted, Amano discloses that the communication interface unit 41 (i.e., the Intel 8251A interface) receives series data from the keyboard controller. Regarding the receiving of data, Amano discloses: "The communication interface unit 41 [i.e., the Intel 8251A interface] performs functions identified by the output leads as a transmitter data terminal (XMT), a transmitter empty terminal (XMT EMP) and a receiver terminal (RCV) . . . RCV: The terminal receives series characters from the keyboard to convert them to parallel characters for data of the CPU." (Amano, col. 3, lines 17-21 and 38-41.) Further, Amano discloses: "The series data from the keyboard controller are received t the RCV terminal of the communication interface unit 41 where the data are processed as the data of the keyboard." (Amano, col. 5, lines 31-34.)

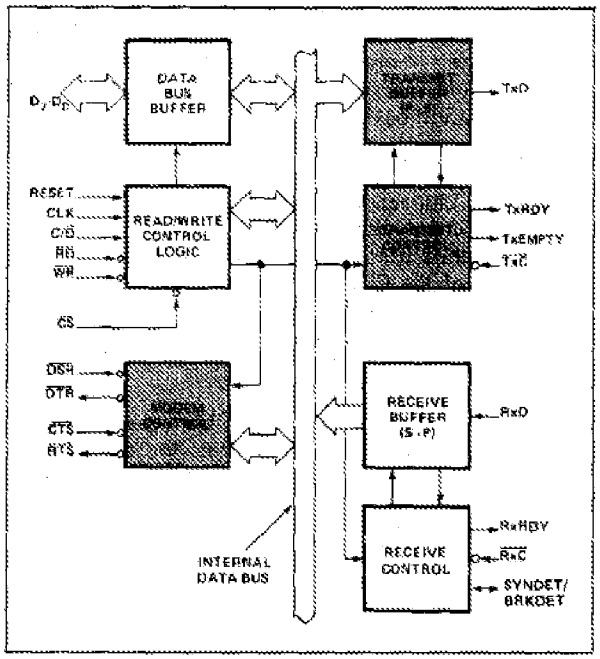


Figure 4. 8251A Block Diagram Showing Modem and Transmitter Buffer and Control Functions

Regarding the receiving function, Intel 8251A discloses that the Receive Buffer (see Figure 4, above) performs the functions described in Amano. Intel 8251A discloses that the "Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an 'assembled' character to the CPU." (Intel 8251A, page 8-47.)

Further, Intel 8251A discloses that the received serial data is clocked to the Receiver Clock signal (RxC). In more detail, Intel 8251A discloses: "Serial data is input to RxD pin, and is clocked in on the rising edge of RxC." (Intel 8251A, page 8-47.)

Figure 4 of Intel 8251A shows that both the RxD pin and the RxC pin are input pins. Regarding the Receiver Clock that is input to the RxC pin, Intel 8251A discloses: "The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the Baud Rate (1x) is equal to the actual frequency of RxC. In Asynchronous

	Mode, the Baud Rate is a fraction of the actual RxC frequency." (Intel 8251A, page 8-47.) As such, Intel 8251A discloses that serial data received by the interface are clocked to rising edges of the Receiver Clock, which is also received by the interface. One skilled in the art would understand that, when the Intel 8251A interface is implemented as the communication interface unit 41 of Amano, the Receiver Clock input to the Intel 8251A corresponds to the clock of the keyboard controller 34. As previously noted, the keyboard controller clock controls the generation of the polling responses by the keyboard controller 34. Because Amano in view of Intel 8251A discloses that the keyboard controller clock is input to the input/output interface (i.e., to the RxC input pin of the Intel 8251A interface), Amano in view of Intel 8251A discloses that the clock of the keyboard controller 34 is connected to the input/output interface (i.e., keyboard interface unit 23). **Reason for modifying Kato according to Amano in view of Intel 8251A**: The prior art itself (i.e., Amano) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A to arrive at the claimed invention. In more detail, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "limit[s] the duty time of the central processing unit and its memory by designing the keyboard with a keyboard controller integrally fabricated as a single chip microprocessor."

	(Amano, col. 1, lines 53-59.) Further, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "reduces the number of signals between the main processor and the keyboard such that a very thin bidirectional cable therebetween can be used." (Amano, col. 7, lines 14-17.) Because Amano discloses that implementing independent clock generators limits the duty time of the CPU and its memory and reduces the number of signals between the main processor and the keyboard, Amano provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A. Therefore, it would have been obvious to modify Kato according to Amano in view of Intel 8251A.
wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.	Please see corresponding analysis in Table 1.
Claim 7	**Kato, Ledzius, Amano and Intel 8251A**
7. The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of	Please see corresponding analysis in Table 1.

said substrate.	
Claim 9	**Kato, Ledzius, Amano and Intel 8251A**
9. The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	Please see corresponding analysis in Table 1.
Claim 10	**Kato, Ledzius, Amano and Intel 8251A**
10. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:	Please see corresponding analysis in Table 1.
providing said central processing unit upon an integrated circuit substrate,	Please see corresponding analysis in Table 1.
said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	Please see corresponding analysis in Table 1.
providing an entire variable speed clock	Please see corresponding analysis in Table 1.

disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	
clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated	Please see corresponding analysis in Table 1.

with said integrated circuit substrate;	
connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	Please see corresponding analysis in Table 1.
clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock and	This feature is taught by Kato, modified by Amano, in view of Intel 8251A. Kato discloses that the clock generating circuit comprises a first clock generator 14 and a second clock generator 15. (See Kato, col. 4, lines 37-38.) Regarding the second clock generator 15, Kato discloses that the "second clock generator 15 produces two clock signals Φa and Φb from the reference clock signal Φ0 output by first clock generator 14 . . . They are supplied to the components of the data processing circuit." (Kato, col. 4, lines 56-62.) Kato does not expressly disclose that the second clock is off-chip and operative at a frequency independent of a clock frequency of the system clock. Amano, in view of Intel 8251A, teaches an off-chip external clock for

clocking said input/output interface, wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock.

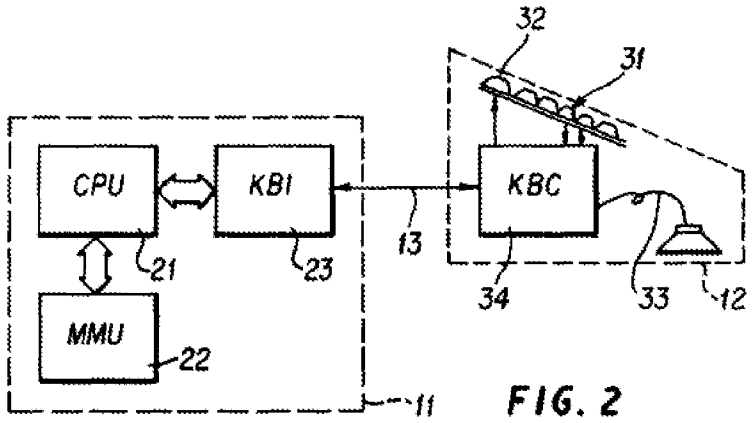


FIG. 2

With reference to FIG. 2 (see above), Amano discloses that the main processor 11 has a CPU 21 and a keyboard interface unit (KBI) 23. Also, Amano discloses that the keyboard 12 has a keyboard controller (KBC) 34. (See Amano, col. 2, lines 59-63.) Further, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. (See Amano, col. 2, lines 57-59.)

First, Amano teaches an off-chip external clock independent of a system clock, wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock.

In this regard, Amano discloses that the clock of the keyboard controller 34 is independent of a system clock of the CPU 21, wherein the keyboard controller clock is operative at a frequency independent of a clock frequency of the system clock.

In more detail, Amano discloses: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling."

	(Amano, col. 7, lines 34-38.) Amano explicitly distinguishes its invention from the prior art, where the keyboard controller clock is supplied by the main system. Amano discloses: "In the prior art, the keyboard controller clock of the DEC VT-100 full keyboard is supplied from the main system, and the polling (from the CPU) period and the response (from the keyboard) period is defined by a synchronization clock, that is, the data transmission control between the CPU and the keyboard is done using a time multiplex method." (Amano, col. 7, lines 25-31.) Therefore, Amano teaches an off-chip external clock independent of a system clock, wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock. In addition, Amano at least implicitly discloses that the clock of the keyboard controller is for clocking the input/output interface. As noted previously regarding FIG. 2, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. More specifically, FIG. 2 shows that the keyboard interface unit 23 and the keyboard controller 34 are connected by bidirectional line 13. As previously explained, Amano discloses that the keyboard controller 34 has an independent clock generator. Amano at least implicitly discloses that the independent clock generator controls generation of the keyboard controller's responses to the CPU polling. (See Amano, col. 7, lines 34-38: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock

generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling.")

In order for Amano's main processor 11 to properly receive and interpret the responses generated by the keyboard controller 34, one skilled in the art would understand that the clock of the keyboard controller 34 (which controls the generation of the responses) is supplied to the keyboard interface unit 23 via bidirectional line 13.

Because it would be understood by one skilled in the art that Amano's keyboard controller clock is supplied to the keyboard interface unit 23, Amano at least implicitly discloses that the clock of the keyboard controller 34 is connected to the input/output interface (i.e., keyboard interface unit 23) for clocking the input/output interface.

In addition, Amano in view of Intel 8251A discloses that the clock of the keyboard controller is for clocking said input/output interface.
As noted previously regarding FIG. 2, Amano discloses the main processor 11 has a CPU 21 and a keyboard interface unit (KBI) 23. The keyboard interface unit (KBI) 23 is connected to the keyboard controller 34 by bidirectional line 13.

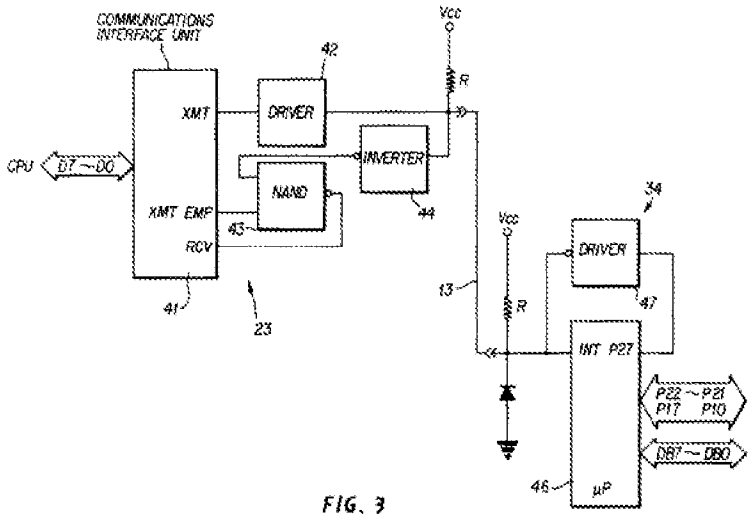
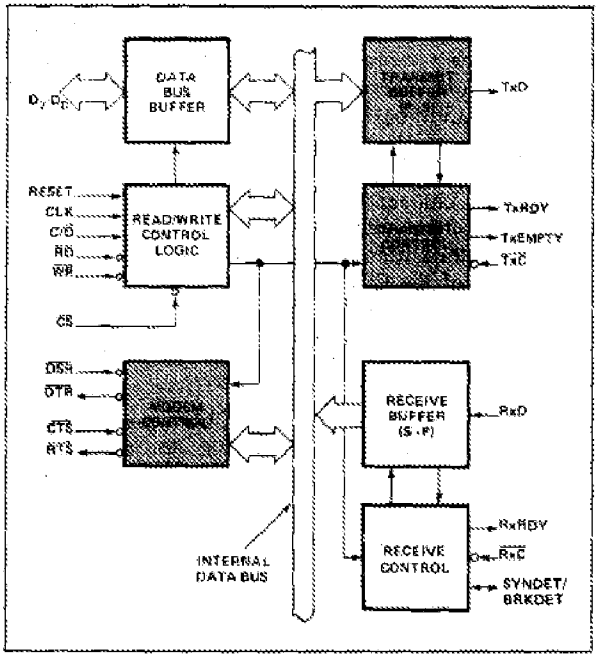


FIG. 3

	With reference to FIG. 3 (see above), Amano discloses that the keyboard interface unit 23 includes a communication interface unit 41 for receiving series data from the keyboard controller 34 and converting the series data to parallel data for transmission to the CPU. (See Amano, col. 2, line 64 to col. 3, line 4.) Regarding the communication interface unit 41, Amano discloses that this unit may be implemented by the Intel 8251A programmable communication interface. In more detail, Amano discloses: "In this embodiment, the communication interface unit 41 used is a programmable communication interface I 8251A produced by Intel Corp. The programmable communication interface is a programmable element used as peripheral circuits for microprocessors, and is capable of performing the functions as explained above. The programmable communication interface I 8251A is explained in detail in the Intel Component Data Catalog 1979 P11.24-P11.31." (Amano, col. 3, lines 8-17.) It is believed that relevant portions of Intel 8251A (which corresponds to the Intel Component Data Catalog 1981) are substantially similar to the 1979 catalog referenced by Amano. As previously noted, Amano discloses that the communication interface unit 41 (i.e., the Intel 8251A interface) receives series data from the keyboard controller. Regarding the receiving of data, Amano discloses: "The communication interface unit 41 [i.e., the Intel 8251A interface] performs functions identified by the output leads as a transmitter data terminal (XMT), a transmitter empty terminal (XMT EMP) and a receiver terminal (RCV) . . . RCV: The terminal receives series characters from the keyboard to convert them to parallel characters for data of the CPU." (Amano, col. 3, lines 17-21 and 38-41.) Further,

	Amano discloses: "The series data from the keyboard controller are received t the RCV terminal of the communication interface unit 41 where the data are processed as the data of the keyboard." (Amano, col. 5, lines 31-34.)  **Figure 4. 8251A Block Diagram Showing Modem and Transmitter Buffer and Control Functions** Regarding the receiving function, Intel 8251A discloses that the Receive Buffer (see Figure 4, above) performs the functions described in Amano. Intel 8251A discloses that the "Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an 'assembled' character to the CPU." (Intel 8251A, page 8-47.) Further, Intel 8251A discloses that the serial data is clocked to the Receiver Clock signal (RxC). In more detail, Intel 8251A discloses: "Serial data is input to RxD pin, and is clocked in on the rising edge of RxC." (Intel 8251A, page 8-47.) Figure 4 of Intel 8251A shows that both the RxD pin and the RxC pin

	are input pins. Regarding the Receiver Clock that is input to the RxC pin, Intel 8251A discloses: "The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the Baud Rate (1x) is equal to the actual frequency of RxC. In Asynchronous Mode, the Baud Rate is a fraction of the actual RxC frequency." (Intel 8251A, page 8-47.) As such, Intel 8251A discloses that serial data received by the interface are clocked to rising edges of the Receiver Clock, which is also received by the interface. One skilled in the art would understand that, when the Intel 8251A interface is implemented as the communication interface unit 41 of Amano, the Receiver Clock input to the Intel 8251A corresponds to the clock of the keyboard controller 34. As previously noted, the keyboard controller clock controls the generation of the polling responses by the keyboard controller 34. Because Amano in view of Intel 8251A discloses that the keyboard controller clock is input to the input/output interface (i.e., to the RxC input pin of the Intel 8251A interface), Amano in view of Intel 8251A discloses that the clock of the keyboard controller 34 is for clocking the input/output interface (i.e., keyboard interface unit 23). **Reason for modifying Kato according to Amano in view of Intel 8251A**: The prior art itself (i.e., Amano) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A to arrive at the claimed invention. In more detail, Amano discloses that its invention (which implements

	independent clock generators in the main system (CPU) and the keyboard controller) "limit[s] the duty time of the central processing unit and its memory by designing the keyboard with a keyboard controller integrally fabricated as a single chip microprocessor." (Amano, col. 1, lines 53-59.) Further, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "reduces the number of signals between the main processor and the keyboard such that a very thin bidirectional cable therebetween can be used." (Amano, col. 7, lines 14-17.) Because Amano discloses that implementing independent clock generators limits the duty time of the CPU and its memory and reduces the number of signals between the main processor and the keyboard, Amano provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A. Therefore, it would have been obvious to modify Kato according to Amano in view of Intel 8251A.
wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock.	Please see corresponding analysis in Table 1.
Claim 11	**Kato, Ledzius, Amano and Intel 8251A**
11. A microprocessor system, comprising a single integrated circuit including	Please see corresponding analysis in Table 1.
a central processing	Please see corresponding analysis in Table 1.

unit and	
an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	Please see corresponding analysis in Table 1.
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	Please see corresponding analysis in Table 1.
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable	Please see corresponding analysis in Table 1.

speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and	Please see corresponding analysis in Table 1.
a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface,	This feature is taught by Kato, modified by Amano in view of Intel 8251A. Kato discloses that the clock generating circuit comprises a first clock generator 14 and a second clock generator 15. (See Kato, col. 4, lines 37-38.) Regarding the second clock generator 15, Kato discloses that the "second clock generator 15 produces two clock signals Φa and Φb from the reference clock signal Φ0 output by first clock generator 14 . . . They are supplied to the components of the data processing circuit." (Kato, col. 4, lines 56-62.) Kato does not expressly disclose that the second clock is independent of the first clock.

Amano, in view of Intel 8251A, teaches a second clock independent of a system clock connected to said input/output interface.

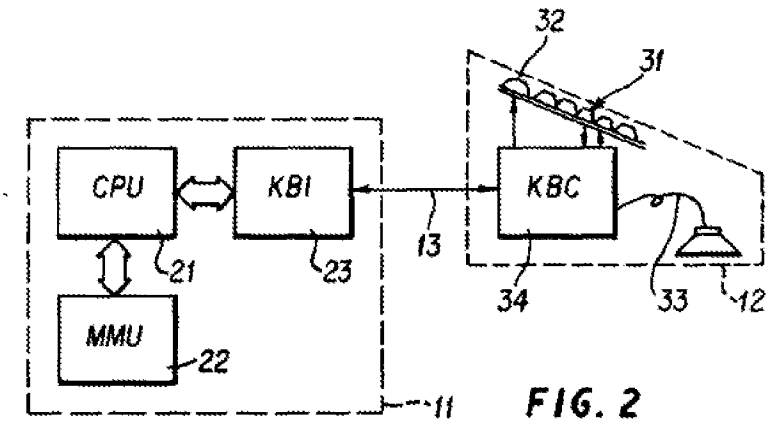


FIG. 2

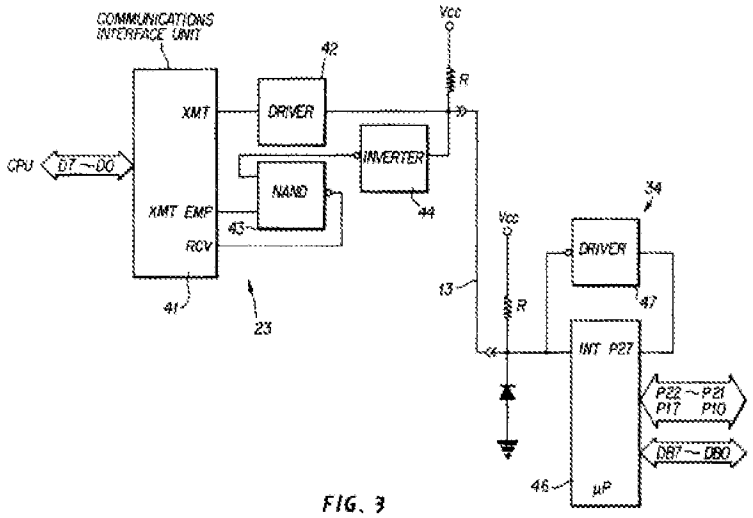
With reference to FIG. 2 (see above), Amano discloses that the main processor 11 has a CPU 21 and a keyboard interface unit (KBI) 23. Also, Amano discloses that the keyboard 12 has a keyboard controller (KBC) 34. (See Amano, col. 2, lines 59-63.) Further, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. (See Amano, col. 2, lines 57-59.)

First, Amano teaches a second clock independent of a system clock. In this regard, Amano discloses that the clock of the keyboard controller 34 is independent of a system clock of the CPU 21.

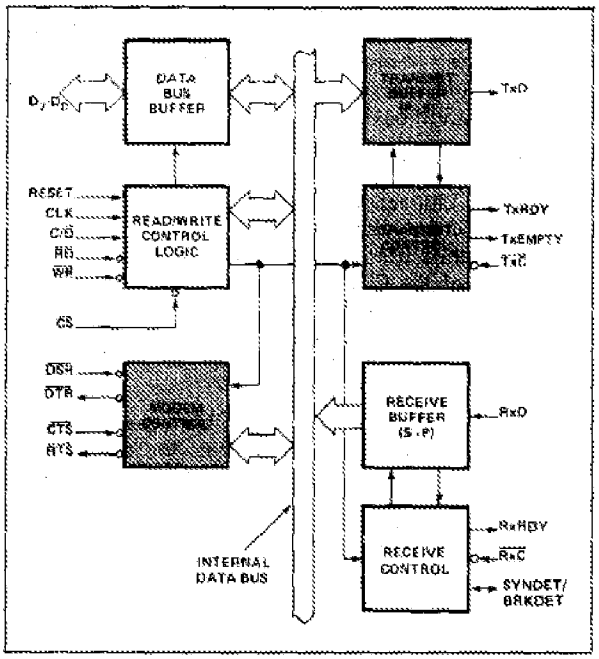
In more detail, Amano discloses: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling." (Amano, col. 7, lines 34-38.)

Amano explicitly distinguishes its invention from the prior art, where the keyboard controller clock is supplied by the main system. Amano discloses: "In the prior art, the keyboard controller clock of the DEC VT-100 full keyboard is supplied from the main system, and the

	polling (from the CPU) period and the response (from the keyboard) period is defined by a synchronization clock, that is, the data transmission control between the CPU and the keyboard is done using a time multiplex method." (Amano, col. 7, lines 25-31.) Therefore, Amano teaches a second clock independent of a system clock. In addition, Amano at least implicitly discloses that the clock of the keyboard controller is connected to said input/output interface. As noted previously regarding FIG. 2, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. More specifically, FIG. 2 shows that the keyboard interface unit 23 and the keyboard controller 34 are connected by bidirectional line 13. As previously explained, Amano discloses that the keyboard controller 34 has an independent clock generator. Amano at least implicitly discloses that the independent clock generator controls generation of the keyboard controller's responses to the CPU polling. (See Amano, col. 7, lines 34-38: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling.") In order for Amano's main processor 11 to properly interpret the responses generated by the keyboard controller 34, one skilled in the art would understand that the clock of the keyboard controller 34 (which controls the generation of the responses) is supplied to the keyboard interface unit 23 via bidirectional line 13.

	Because it would be understood by one skilled in the art that Amano's keyboard controller clock is supplied to the keyboard interface unit 23, Amano at least implicitly discloses that the clock of the keyboard controller 34 is connected to the input/output interface (i.e., keyboard interface unit 23). In addition, Amano in view of Intel 8251A discloses that the clock of the keyboard controller is connected to said input/output interface. As noted previously regarding FIG. 2, Amano discloses the main processor 11 has the CPU 21 and the keyboard interface unit (KBI) 23. The keyboard interface unit (KBI) 23 is connected to the keyboard controller 34 by bidirectional line 13.  FIG. 3 With reference to FIG. 3 (see above), Amano discloses that the keyboard interface unit 23 includes a communication interface unit 41 for receiving series data from the keyboard controller 34 and for converting the series data to parallel data for transmission to the CPU. (See Amano, col. 2, line 64 to col. 3, line 4.) Regarding the communication interface unit 41, Amano discloses that this unit may be implemented by the Intel 8251A programmable communication interface. In more detail, Amano discloses: "In this

	embodiment, the communication interface unit 41 used is a programmable communication interface I 8251A produced by Intel Corp. The programmable communication interface is a programmable element used as peripheral circuits for microprocessors, and is capable of performing the functions as explained above. The programmable communication interface I 8251A is explained in detail in the Intel Component Data Catalog 1979 P11.24-P11.31." (Amano, col. 3, lines 8-17.) It is believed that relevant portions of Intel 8251A (which corresponds to the Intel Component Data Catalog 1981) are substantially similar to the 1979 catalog referenced by Amano. As previously noted, Amano discloses that the communication interface unit 41 (i.e., the Intel 8251A interface) receives series data from the keyboard controller. Regarding the receiving of data, Amano discloses: "The communication interface unit 41 [i.e., the Intel 8251A interface] performs functions identified by the output leads as a transmitter data terminal (XMT), a transmitter empty terminal (XMT EMP) and a receiver terminal (RCV) . . . RCV: The terminal receives series characters from the keyboard to convert them to parallel characters for data of the CPU." (Amano, col. 3, lines 17-21 and 38-41.) Further, Amano discloses: "The series data from the keyboard controller are received t the RCV terminal of the communication interface unit 41 where the data are processed as the data of the keyboard." (Amano, col. 5, lines 31-34.)



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Further, Intel 8251A discloses that the received serial data is clocked to the Receiver Clock signal (RxC). In more detail, Intel 8251A discloses: "Serial data is input to RxD pin, and is clocked in on the rising edge of RxC." (Intel 8251A, page 8-47.)

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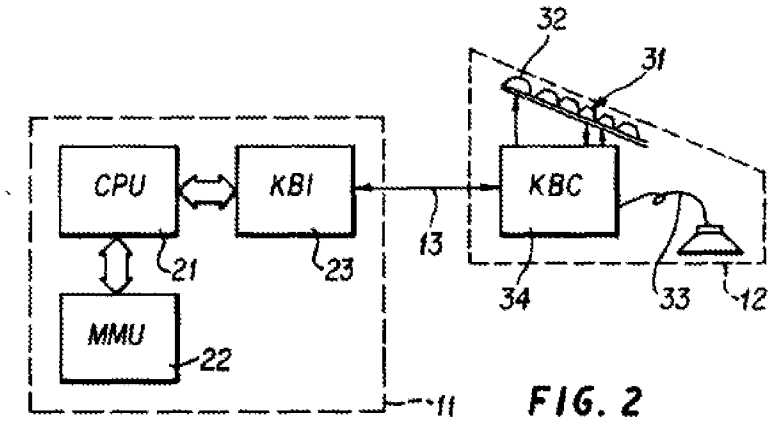
	Mode, the Baud Rate is a fraction of the actual RxC frequency." (Intel 8251A, page 8-47.) As such, Intel 8251A discloses that serial data received by the interface are clocked to rising edges of the Receiver Clock, which is also received by the interface. One skilled in the art would understand that, when the Intel 8251A interface is implemented as the communication interface unit 41 of Amano, the Receiver Clock input to the Intel 8251A corresponds to the clock of the keyboard controller 34. As previously noted, the keyboard controller clock controls the generation of the polling responses by the keyboard controller 34. Because Amano in view of Intel 8251A discloses that the keyboard controller clock is input to the input/output interface (i.e., to the RxC input pin of the Intel 8251A interface), Amano in view of Intel 8251A discloses that the clock of the keyboard controller 34 is connected to the input/output interface (i.e., keyboard interface unit 23). **Reason for modifying Kato according to Amano in view of Intel 8251A**: The prior art itself (i.e., Amano) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A to arrive at the claimed invention. In more detail, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "limit[s] the duty time of the central processing unit and its memory by designing the keyboard with a keyboard controller integrally fabricated as a single chip microprocessor."

	(Amano, col. 1, lines 53-59.) Further, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "reduces the number of signals between the main processor and the keyboard such that a very thin bidirectional cable therebetween can be used." (Amano, col. 7, lines 14-17.) Because Amano discloses that implementing independent clock generators limits the duty time of the CPU and its memory and reduces the number of signals between the main processor and the keyboard, Amano provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A. Therefore, it would have been obvious to modify Kato according to Amano in view of Intel 8251A.
wherein said central processing unit operates asynchronously to said input/output interface.	Please see corresponding analysis in Table 1.
Claim 12	**Kato, Ledzius, Amano and Intel 8251A**
The microprocessor system of claim 11, in which said second clock is a fixed frequency clock.	Please see corresponding analysis in Table 1.
Claim 13	**Kato, Ledzius, Amano and Intel 8251A**
13. A microprocessor system comprising: a central processing	Please see corresponding analysis in Table 1.

unit disposed upon an integrated circuit substrate,	
said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;	Please see corresponding analysis in Table 1.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit,	Please see corresponding analysis in Table 1.
said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,	Please see corresponding analysis in Table 1.
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices	Please see corresponding analysis in Table 1.

in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	
an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	Please see corresponding analysis in Table 1.
an off-chip external clock, independent of said oscillator, connected to said	This feature is taught by Kato, modified by Amano, in view of Intel 8251A. Kato discloses that the clock generating circuit comprises a first clock

input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and	generator 14 and a second clock generator 15. (See Kato, col. 4, lines 37-38.) Regarding the second clock generator 15, Kato discloses that the "second clock generator 15 produces two clock signals Φa and Φb from the reference clock signal Φ0 output by first clock generator 14 . . . They are supplied to the components of the data processing circuit." (Kato, col. 4, lines 56-62.) Kato does not expressly disclose that the second clock is off-chip, and operative at a frequency independent of the system clock. Amano, in view of Intel 8251A, teaches an off-chip external clock independent of a system clock, connected to said input/output interface, wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock.  FIG. 2 With reference to FIG. 2 (see above), Amano discloses that the main processor 11 has a CPU 21 and a keyboard interface unit (KBI) 23. Also, Amano discloses that the keyboard 12 has a keyboard controller (KBC) 34. (See Amano, col. 2, lines 59-63.) Further, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. (See Amano, col. 2, lines 57-59.) First, Amano teaches an off-chip external clock independent of a system clock, wherein the off-chip external clock is operative at a frequency

	independent of a clock frequency of the system clock. In this regard, Amano discloses that the clock of the keyboard controller 34 is independent of a system clock of the CPU 21, wherein the keyboard controller clock is operative at a frequency independent of a clock frequency of the system clock. In more detail, Amano discloses: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling." (Amano, col. 7, lines 34-38.) Amano explicitly distinguishes its invention from the prior art, where the keyboard controller clock is supplied by the main system. Amano discloses: "In the prior art, the keyboard controller clock of the DEC VT-100 full keyboard is supplied from the main system, and the polling (from the CPU) period and the response (from the keyboard) period is defined by a synchronization clock, that is, the data transmission control between the CPU and the keyboard is done using a time multiplex method." (Amano, col. 7, lines 25-31.) Therefore, Amano teaches an off-chip external clock independent of a system clock, wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock. In addition, Amano at least implicitly discloses that the clock of the keyboard controller is connected to the input/output interface. As noted previously regarding FIG. 2, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. More specifically, FIG. 2 shows that the keyboard interface unit 23 and the keyboard controller 34 are connected by bidirectional

	line 13. As previously explained, Amano discloses that the keyboard controller 34 has an independent clock generator. Amano at least implicitly discloses that the independent clock generator controls generation of the keyboard controller's responses to the CPU polling. (See Amano, col. 7, lines 34-38: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling.") In order for Amano's main processor 11 to properly interpret the responses generated by the keyboard controller 34, one skilled in the art would understand that the clock of the keyboard controller 34 (which controls the generation of the responses) is supplied to the keyboard interface unit 23 via bidirectional line 13. Because it would be understood by one skilled in the art that Amano's keyboard controller clock is supplied to the keyboard interface unit 23, Amano at least implicitly discloses that the clock of the keyboard controller 34 is connected to the input/output interface (i.e., keyboard interface unit 23). In addition, Amano in view of Intel 8251A discloses that the clock of the keyboard controller is connected to said input/output interface. As noted previously regarding FIG. 2, Amano discloses the main processor 11 has the CPU 21 and the keyboard interface unit (KBI) 23. The keyboard interface unit (KBI) 23 is connected to the keyboard controller 34 by bidirectional line 13.

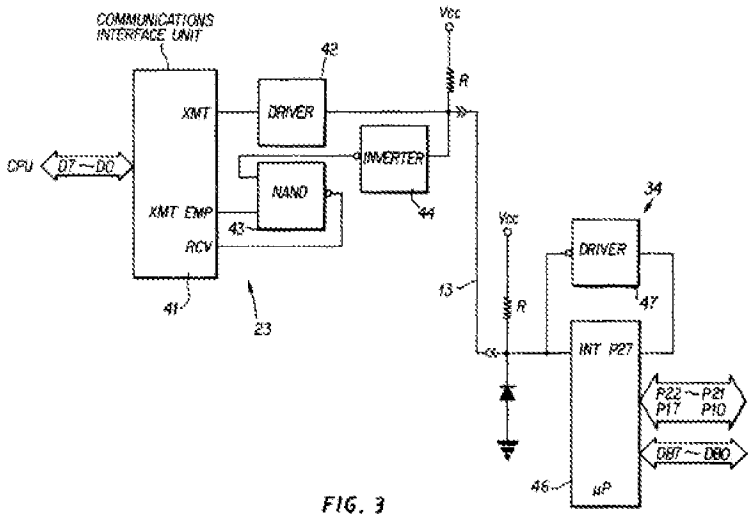


FIG. 3

With reference to FIG. 3 (see above), Amano discloses that the keyboard interface unit 23 includes a communication interface unit 41 for receiving series data from the keyboard controller 34 and for converting the series data to parallel data for transmission to the CPU. (See Amano, col. 2, line 64 to col. 3, line 4.)

Regarding the communication interface unit 41, Amano discloses that this unit may be implemented by the Intel 8251A programmable communication interface. In more detail, Amano discloses: "In this embodiment, the communication interface unit 41 used is a programmable communication interface I 8251A produced by Intel Corp. The programmable communication interface is a programmable element used as peripheral circuits for microprocessors, and is capable of performing the functions as explained above. The programmable communication interface I 8251A is explained in detail in the Intel Component Data Catalog 1979 P11.24-P11.31." (Amano, col. 3, lines 8-17.)

It is believed that relevant portions of Intel 8251A (which corresponds to the Intel Component Data Catalog 1981) are substantially similar to the 1979 catalog referenced by Amano.

As previously noted, Amano discloses that the communication interface unit 41 (i.e., the Intel 8251A interface) receives series data from the keyboard controller. Regarding the receiving of data, Amano discloses: "The communication interface unit 41 [i.e., the Intel 8251A interface] performs functions identified by the output leads as a transmitter data terminal (XMT), a transmitter empty terminal (XMT EMP) and a receiver terminal (RCV) . . . RCV: The terminal receives series characters from the keyboard to convert them to parallel characters for data of the CPU." (Amano, col. 3, lines 17-21 and 38-41.) Further, Amano discloses: "The series data from the keyboard controller are received t the RCV terminal of the communication interface unit 41 where the data are processed as the data of the keyboard." (Amano, col. 5, lines 31-34.)

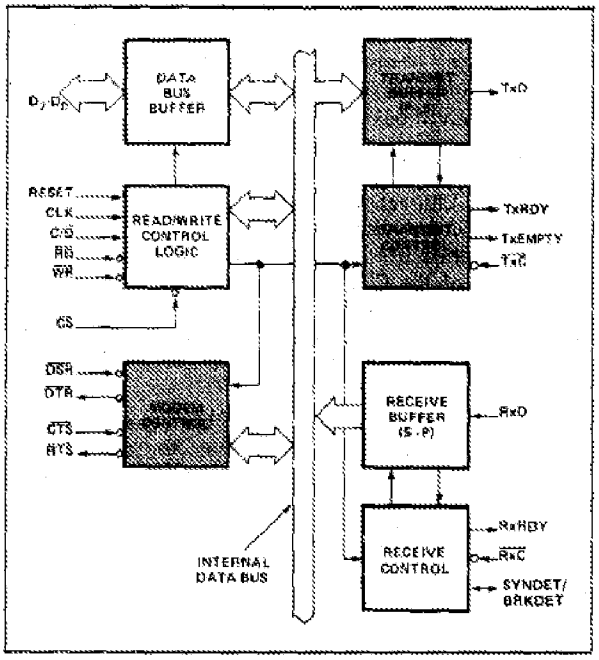


Figure 4. 8251A Block Diagram Showing Modem and Transmitter Buffer and Control Functions

Regarding the receiving function, Intel 8251A discloses that the Receive Buffer (see Figure 4, above) performs the functions described in Amano. Intel 8251A discloses that the "Receiver accepts serial data,

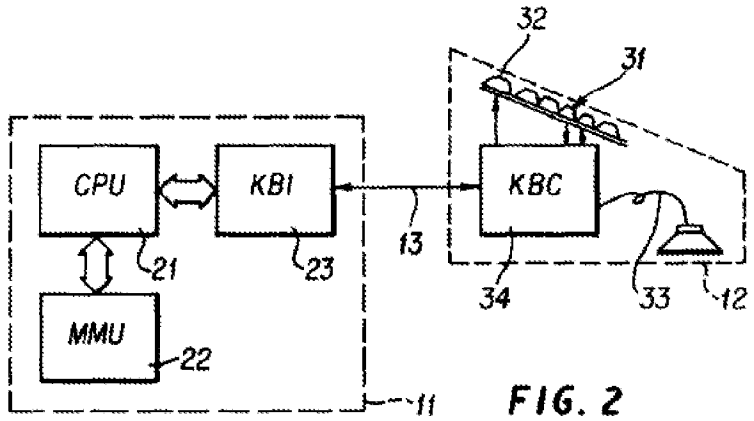
	converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an 'assembled' character to the CPU." (Intel 8251A, page 8-47.) Further, Intel 8251A discloses that the received serial data is clocked to the Receiver Clock signal (RxC). In more detail, Intel 8251A discloses: "Serial data is input to RxD pin, and is clocked in on the rising edge of RxC." (Intel 8251A, page 8-47.) Figure 4 of Intel 8251A shows that both the RxD pin and the RxC pin are input pins. Regarding the Receiver Clock that is input to the RxC pin, Intel 8251A discloses: "The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the Baud Rate (1x) is equal to the actual frequency of RxC. In Asynchronous Mode, the Baud Rate is a fraction of the actual RxC frequency." (Intel 8251A, page 8-47.) As such, Intel 8251A discloses that serial data received by the interface are clocked to rising edges of the Receiver Clock, which is also received by the interface. One skilled in the art would understand that, when the Intel 8251A interface is implemented as the communication interface unit 41 of Amano, the Receiver Clock input to the Intel 8251A corresponds to the clock of the keyboard controller 34. As previously noted, the keyboard controller clock controls the generation of the polling responses by the keyboard controller 34. Because Amano in view of Intel 8251A discloses that the keyboard controller clock is input to the input/output interface (i.e., to the RxC input pin of the Intel 8251A interface), Amano in view of Intel 8251A

	discloses that the clock of the keyboard controller 34 is connected to the input/output interface (i.e., keyboard interface unit 23). **Reason for modifying Kato according to Amano in view of Intel 8251A**: The prior art itself (i.e., Amano) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A to arrive at the claimed invention. In more detail, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "limit[s] the duty time of the central processing unit and its memory by designing the keyboard with a keyboard controller integrally fabricated as a single chip microprocessor." (Amano, col. 1, lines 53-59.) Further, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "reduces the number of signals between the main processor and the keyboard such that a very thin bidirectional cable therebetween can be used." (Amano, col. 7, lines 14-17.) Because Amano discloses that implementing independent clock generators limits the duty time of the CPU and its memory and reduces the number of signals between the main processor and the keyboard, Amano provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A. Therefore, it would have been obvious to modify Kato according to Amano in view of Intel 8251A.
further wherein said central processing	Please see corresponding analysis in Table 1.

unit operates asynchronously to said input/output interface.	
Claim 14	**Kato, Ledzius, Amano and Intel 8251A**
14. The microprocessor system of claim 13, wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	Please see corresponding analysis in Table 1.
Claim 15	**Kato, Ledzius, Amano and Intel 8251A**
15. The microprocessor system of claim 13 wherein said oscillator comprises a ring oscillator.	Please see corresponding analysis in Table 1.
Claim 16	**Kato, Ledzius, Amano and Intel 8251A**
16. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps	Please see corresponding analysis in Table 1.

of:	
providing said central processing unit upon an integrated circuit substrate,	Please see corresponding analysis in Table 1.
said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	Please see corresponding analysis in Table 1.
providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	Please see corresponding analysis in Table 1.
clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent	Please see corresponding analysis in Table 1.

upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	
connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	Please see corresponding analysis in Table 1.
clocking said input/output interface	This feature is taught by Kato, modified by Amano in view of Intel 8251A.

using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock,	Kato discloses that the clock generating circuit comprises a first clock generator 14 and a second clock generator 15. (See Kato, col. 4, lines 37-38.) Regarding the second clock generator 15, Kato discloses that the "second clock generator 15 produces two clock signals Φa and Φb from the reference clock signal Φ0 output by first clock generator 14 . . . They are supplied to the components of the data processing circuit." (Kato, col. 4, lines 56-62.) Kato does not expressly disclose that the second clock is off-chip, and operative at a frequency independent of a clock frequency of the system clock. Amano, in view of Intel 8251A, teaches an off-chip external clock for clocking said input/output interface, wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock.  FIG. 2 With reference to FIG. 2 (see above), Amano discloses that the main processor 11 has a CPU 21 and a keyboard interface unit (KBI) 23. Also, Amano discloses that the keyboard 12 has a keyboard controller (KBC) 34. (See Amano, col. 2, lines 59-63.) Further, Amano discloses that the main processor 11 and the keyboard 12 are connected through bidirectional line 13. (See Amano, col. 2, lines 57-59.)

	First, Amano teaches an off-chip external clock independent of a system clock, wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock. In this regard, Amano discloses that the clock of the keyboard controller 34 is independent of a system clock of the CPU 21, wherein the keyboard controller clock is operative at a frequency independent of a clock frequency of the system clock. In more detail, Amano discloses: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling." (Amano, col. 7, lines 34-38.) Amano explicitly distinguishes its invention from the prior art, where the keyboard controller clock is supplied by the main system. Amano discloses: "In the prior art, the keyboard controller clock of the DEC VT-100 full keyboard is supplied from the main system, and the polling (from the CPU) period and the response (from the keyboard) period is defined by a synchronization clock, that is, the data transmission control between the CPU and the keyboard is done using a time multiplex method." (Amano, col. 7, lines 25-31.) Therefore, Amano teaches an off-chip external clock independent of a system clock, wherein the off-chip external clock is operative at a frequency independent of a clock frequency of the system clock. In addition, Amano at least implicitly discloses that the clock of the keyboard controller is for clocking the input/output interface. As noted previously regarding FIG. 2, Amano discloses that the main

	processor 11 and the keyboard 12 are connected through bidirectional line 13. More specifically, FIG. 2 shows that the keyboard interface unit 23 and the keyboard controller 34 are connected by bidirectional line 13. As previously explained, Amano discloses that the keyboard controller 34 has an independent clock generator. Amano at least implicitly discloses that the independent clock generator controls generation of the keyboard controller's responses to the CPU polling. (See Amano, col. 7, lines 34-38: "In the present invention, on the other hand, the main system (CPU) and the keyboard controller have independent clock generators, and the CPU sends the polling periodically and the keyboard controller responds to each polling.") In order for Amano's main processor 11 to properly interpret the responses generated by the keyboard controller 34, one skilled in the art would understand that the clock of the keyboard controller 34 (which controls the generation of the responses) is supplied to the keyboard interface unit 23 via bidirectional line 13. Because it would be understood by one skilled in the art that Amano's keyboard controller clock is supplied to the keyboard interface unit 23, Amano at least implicitly discloses that the clock of the keyboard controller 34 is connected to the input/output interface (i.e., keyboard interface unit 23) for clocking the input/output interface. In addition, Amano in view of Intel 8251A discloses that the clock of the keyboard controller is for clocking said input/output interface. As noted previously regarding FIG. 2, Amano discloses the main processor 11 has the CPU 21 and the keyboard interface unit (KBI) 23. The keyboard interface unit (KBI) 23 is connected to the keyboard

controller 34 by bidirectional line 13.

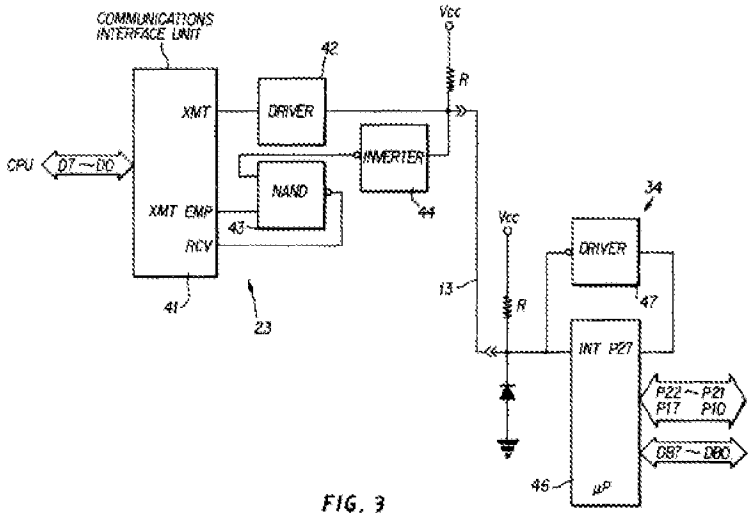
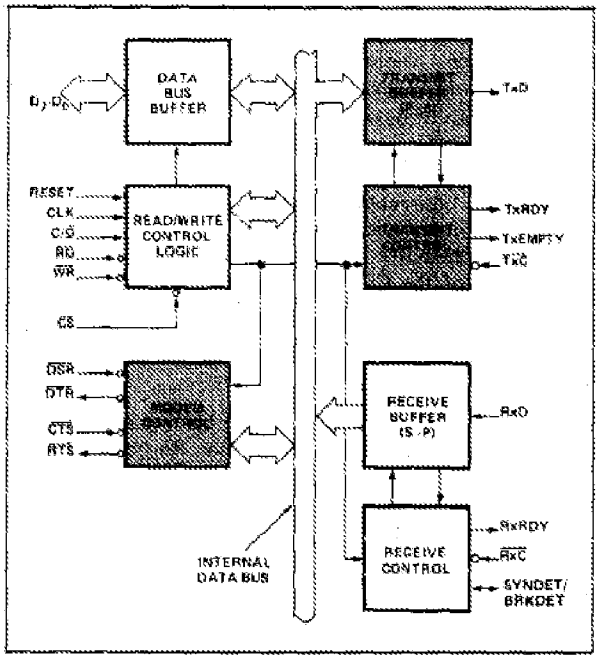


FIG. 3

With reference to FIG. 3 (see above), Amano discloses that the keyboard interface unit 23 includes a communication interface unit 41 for receiving series data from the keyboard controller 34 and converting the series data to parallel data for transmission to the CPU. (See Amano, col. 2, line 64 to col. 3, line 4.)

Regarding the communication interface unit 41, Amano discloses that this unit may be implemented by the Intel 8251A programmable communication interface. In more detail, Amano discloses: "In this embodiment, the communication interface unit 41 used is a programmable communication interface I 8251A produced by Intel Corp. The programmable communication interface is a programmable element used as peripheral circuits for microprocessors, and is capable of performing the functions as explained above. The programmable communication interface I 8251A is explained in detail in the Intel Component Data Catalog 1979 P11.24-P11.31." (Amano, col. 3, lines 8-17.)

It is believed that relevant portions of Intel 8251A (which corresponds to the Intel Component Data Catalog 1981) are substantially similar to

	the 1979 catalog referenced by Amano. As previously noted, Amano discloses that the communication interface unit 41 (i.e., the Intel 8251A interface) receives series data from the keyboard controller. Regarding the receiving of data, Amano discloses: "The communication interface unit 41 [i.e., the Intel 8251A interface] performs functions identified by the output leads as a transmitter data terminal (XMT), a transmitter empty terminal (XMT EMP) and a receiver terminal (RCV) . . . RCV: The terminal receives series characters from the keyboard to convert them to parallel characters for data of the CPU." (Amano, col. 3, lines 17-21 and 38-41.) Further, Amano discloses: "The series data from the keyboard controller are received t the RCV terminal of the communication interface unit 41 where the data are processed as the data of the keyboard." (Amano, col. 5, lines 31-34.)  **Figure 4. 8251A Block Diagram Showing Modem and Transmitter Buffer and Control Functions** Regarding the receiving function, Intel 8251A discloses that the Receive Buffer (see Figure 4, above) performs the functions described in

	Amano. Intel 8251A discloses that the "Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an 'assembled' character to the CPU." (Intel 8251A, page 8-47.) Further, Intel 8251A discloses that the received serial data is clocked to the Receiver Clock signal (RxC). In more detail, Intel 8251A discloses: "Serial data is input to RxD pin, and is clocked in on the rising edge of RxC." (Intel 8251A, page 8-47.) Figure 4 of Intel 8251A shows that both the RxD pin and the RxC pin are input pins. Regarding the Receiver Clock that is input to the RxC pin, Intel 8251A discloses: "The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the Baud Rate (1x) is equal to the actual frequency of RxC. In Asynchronous Mode, the Baud Rate is a fraction of the actual RxC frequency." (Intel 8251A, page 8-47.) As such, Intel 8251A discloses that serial data received by the interface are clocked to rising edges of the Receiver Clock, which is also received by the interface. One skilled in the art would understand that, when the Intel 8251A interface is implemented as the communication interface unit 41 of Amano, the Receiver Clock input to the Intel 8251A corresponds to the clock of the keyboard controller 34. As previously noted, the keyboard controller clock controls the generation of the polling responses by the keyboard controller 34. Because Amano in view of Intel 8251A discloses that the keyboard controller clock is input to the input/output interface (i.e., to the RxC

	input pin of the Intel 8251A interface), Amano in view of Intel 8251A discloses that the clock of the keyboard controller 34 is for clocking the input/output interface (i.e., keyboard interface unit 23). **Reason for modifying Kato according to Amano in view of Intel 8251A**: The prior art itself (i.e., Amano) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A to arrive at the claimed invention. In more detail, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "limit[s] the duty time of the central processing unit and its memory by designing the keyboard with a keyboard controller integrally fabricated as a single chip microprocessor." (Amano, col. 1, lines 53-59.) Further, Amano discloses that its invention (which implements independent clock generators in the main system (CPU) and the keyboard controller) "reduces the number of signals between the main processor and the keyboard such that a very thin bidirectional cable therebetween can be used." (Amano, col. 7, lines 14-17.) Because Amano discloses that implementing independent clock generators limits the duty time of the CPU and its memory and reduces the number of signals between the main processor and the keyboard, Amano provides teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A. Therefore, it would have been obvious to modify Kato according to Amano in view of Intel 8251A.
wherein said central	Please see corresponding analysis in Table 1.

processing unit operates asynchronously to said input/output interface.	

C) Detailed Explanation for Proposed Rejections Based on Amano and Nowatzyk

Requester respectfully submits that claims 1, 2, 6, 7 and 9-16 of the '336 reexamination certificate are rendered obvious under 35 U.S.C. § 103 by previously cited references Kato and Ledzius in view of newly cited Amano, further in view of Nowatzyk.

Table 3 below details how Kato, Ledzius, Amano and Nowatzyk disclose each and every limitation recited in claims 1, 2, 6, 7 and 9-16 of the '336 reexamination certificate.

As previously explained, Kato, Ledzius and Amano constitute effective prior art under 35 U.S.C. § 103.

Nowatzyk apparently was published in April 1989. (A date of "April 1989" appears on the cover of this reference.) Accordingly, it is believed that Nowatzyk constitutes effective prior art under 35 U.S.C. § 103.

Nowatzyk is an academic thesis proposing a communication architecture for multiprocessor networks that presents the user with a logically uniform address space shared by all processors. (See Nowatzyk, Abstract.)

Table 3
Comparison of the '336 patent claims to Kato, Ledzius, Amano and Nowatzyk

Claim 1	Kato, Ledzius, Amano and Nowatzyk
1. A microprocessor system, comprising a single integrated circuit including	See corresponding analysis in Table 1.
a central processing unit and	See corresponding analysis in Table 1.
an entire ring oscillator variable speed system clock	See corresponding analysis in Table 1.

in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	See corresponding analysis in Table 1.
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	See corresponding analysis in Table 1.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and	See corresponding analysis in Table 1.

a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface,	See corresponding analysis in Table 1. **Further Reason for modifying Kato according to Amano**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano.
wherein a clock signal of said	See corresponding analysis in Table 1.

second clock originates from a source other than said ring oscillator variable speed system clock.	**<u>Further Reason for modifying Kato according to Amano</u>:** The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano.
Claim 2	**Kato, Ledzius, Amano and Nowatzyk**
2. The microprocessor	See corresponding analysis in Table 1.

system of claim 1 in which said second clock is a fixed frequency clock.	
Claim 6	**Kato, Ledzius, Amano and Nowatzyk**
6. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate,	See corresponding analysis in Table 1.
said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices:	See corresponding analysis in Table 1.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit,	See corresponding analysis in Table 1.
said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,	See corresponding analysis in Table 1.
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter	See corresponding analysis in Table 1.

variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	
an on-chip input/output interface connected between said central processing unit and an off-chip external memory bus for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	See corresponding analysis in Table 1.
an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and	See corresponding analysis in Table 1. **Further Reason for modifying Kato according to Amano**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols."

	(Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano.
wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.	See corresponding analysis in Table 1. **Further Reason for modifying Kato according to Amano**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.)

	Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano.
Claim 7	**Kato, Ledzius, Amano and Nowatzyk**
7. The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	See corresponding analysis in Table 1.
Claim 9	**Kato, Ledzius, Amano and Nowatzyk**
9. The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	See corresponding analysis in Table 1.
Claim 10	**Kato, Ledzius, Amano and Nowatzyk**
In a microprocessor system	See corresponding analysis in Table 1.

including a central processing unit, a method for clocking said central processing unit comprising the steps of:	
providing said central processing unit upon an integrated circuit substrate,	See corresponding analysis in Table 1.
said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	See corresponding analysis in Table 1.
providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	See corresponding analysis in Table 1.
clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said	See corresponding analysis in Table 1.

integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	
connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	See corresponding analysis in Table 1.
clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock and	See corresponding analysis in Table 1. **Further Reason for modifying Kato according to Amano**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk

	discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano.
wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock.	See corresponding analysis in Table 1. **Further Reason for modifying Kato according to Amano**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to

	favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano.
Claim 11	**Kato, Ledzius, Amano and Nowatzyk**
11. A microprocessor system, comprising a single integrated circuit including	See corresponding analysis in Table 1.
a central processing unit and	See corresponding analysis in Table 1.
an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	See corresponding analysis in Table 1.

said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	See corresponding analysis in Table 1.
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	See corresponding analysis in Table 1.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and	See corresponding analysis in Table 1.
a second clock independent of said ring oscillator variable speed system clock connected to said	See corresponding analysis in Table 1. **Further Reason for modifying Kato according to Amano**: The prior art itself (i.e., Nowatzyk) provides teaching,

input/output interface,	suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano.
wherein said central processing unit operates asynchronously to said input/output interface.	See corresponding analysis in Table 1. **Further Reason for modifying Kato according to Amano**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary

	skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano.
Claim 12	**Kato, Ledzius, Amano and Nowatzyk**
The microprocessor system of claim 11, in which said second clock is a fixed frequency clock.	See corresponding analysis in Table 1.
Claim 13	**Kato, Ledzius, Amano and Nowatzyk**

13. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate,	See corresponding analysis in Table 1.
said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;	See corresponding analysis in Table 1.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit,	See corresponding analysis in Table 1.
said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,	See corresponding analysis in Table 1.
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit	See corresponding analysis in Table 1.

substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	
an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	See corresponding analysis in Table 1.
an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and	See corresponding analysis in Table 1. **Further Reason for modifying Kato according to Amano**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato.

	Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano.
further wherein said central processing unit operates asynchronously to said input/output interface.	See corresponding analysis in Table 1. **Further Reason for modifying Kato according to Amano**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses:

	"Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano.
Claim 14	**Kato, Ledzius, Amano and Nowatzyk**
14. The microprocessor system of claim 13, wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	See corresponding analysis in Table 1.
Claim 15	**Kato, Ledzius, Amano and Nowatzyk**
15. The microprocessor system of claim 13 wherein said oscillator comprises a ring oscillator.	See corresponding analysis in Table 1.
Claim 16	**Kato, Ledzius, Amano and Nowatzyk**
16. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising	See corresponding analysis in Table 1.

the steps of:	
providing said central processing unit upon an integrated circuit substrate,	See corresponding analysis in Table 1.
said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	See corresponding analysis in Table 1.
providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	See corresponding analysis in Table 1.
clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said	See corresponding analysis in Table 1.

variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	
connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	See corresponding analysis in Table 1.
clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock,	See corresponding analysis in Table 1. **Further Reason for modifying Kato according to Amano**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.)

	Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano.
wherein said central processing unit operates asychronously to said input/output interface.	See corresponding analysis in Table 1. **Further Reason for modifying Kato according to Amano**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation

	that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano.

D) Detailed Explanation for Proposed Rejections Based on Amano, Intel 8251A and Nowatzyk

Requester respectfully submits that claims 1, 2, 6, 7 and 9-16 of the '336 reexamination certificate are rendered obvious under 35 U.S.C. § 103 by previously cited references Kato and Ledzius in view of newly cited Amano, further in view of Intel 8251A and further in view of Nowatzyk.

Table 4 below details how Kato, Ledzius, Amano, Intel 8251A and Nowatzyk disclose each and every limitation recited in claims 1, 2, 6, 7 and 9-16 of the '336 reexamination certificate.

As previously explained, Kato, Ledzius, Amano, Intel 8251A and Nowatzyk constitute effective prior art under 35 U.S.C. § 103.

Table 4
Comparison of the '336 patent claims to Kato, Ledzius, Amano, Intel 8251A and Nowatzyk

Claim 1	Kato, Ledzius, Amano, Intel 8251A and Nowatzyk
1. A microprocessor system,	See corresponding analysis in Table 1.

comprising a single integrated circuit including	
a central processing unit and	See corresponding analysis in Table 1.
an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	See corresponding analysis in Table 1.
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	See corresponding analysis in Table 1.
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	See corresponding analysis in Table 1.

an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and	See corresponding analysis in Table 1.
a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface,	See corresponding analysis of claim 1 **in Table 2**. **Further Reason for modifying Kato according to Amano**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to

	remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano in view of Intel 8251A.
wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.	See corresponding analysis of claim 1 **in Table 2**. **Further Reason for modifying Kato according to Amano in view of Intel 8251A**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that

	would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano in view of Intel 8251A.
Claim 2	**Kato, Ledzius, Amano, Intel 8251A and Nowatzyk**
2. The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	See corresponding analysis in Table 1.
Claim 6	**Kato, Ledzius, Amano, Intel 8251A and Nowatzyk**
6. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate,	See corresponding analysis in Table 1.
said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices:	See corresponding analysis in Table 1.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit,	See corresponding analysis in Table 1.
said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,	See corresponding analysis in Table 1.
thus varying the processing	See corresponding analysis in Table 1.

frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	
an on-chip input/output interface connected between said central processing unit and an off-chip external memory bus for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	See corresponding analysis in Table 1.
an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a	See corresponding analysis of claim 6 **in Table 2**. **Further Reason for modifying Kato according to Amano in view of Intel 8251A**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A to arrive at the claimed invention.

clock frequency of said oscillator and	In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano in view of Intel 8251A.
wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.	See corresponding analysis of claim 6 **in Table 2**. **Further Reason for modifying Kato according to Amano in view of Intel 8251A**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A to arrive at the claimed invention.

	In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano in view of Intel 8251A.
Claim 7	**Kato, Ledzius, Amano, Intel 8251A and Nowatzyk**
7. The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	See corresponding analysis in Table 1.
Claim 9	**Kato, Ledzius, Amano, Intel 8251A and Nowatzyk**

9. The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	See corresponding analysis in Table 1.
Claim 10	**Kato, Ledzius, Amano, Intel 8251A and Nowatzyk**
10. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:	See corresponding analysis in Table 1.
providing said central processing unit upon an integrated circuit substrate,	See corresponding analysis in Table 1.
said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	See corresponding analysis in Table 1.
providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	See corresponding analysis in Table 1.
clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked	See corresponding analysis in Table 1.

by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	
connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	See corresponding analysis in Table 1.
clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency	See corresponding analysis of claim 10 **in Table 2**. **Further Reason for modifying Kato according to Amano in view of Intel 8251A**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have

independent of a clock frequency of said variable speed clock and	led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano in view of Intel 8251A.
wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock.	See corresponding analysis of claim 10 **in Table 2**. **Further Reason for modifying Kato according to Amano in view of Intel 8251A**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano in

	view of Intel 8251A to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano in view of Intel 8251A.
Claim 11	**Kato, Ledzius, Amano, Intel 8251A and Nowatzyk**
11. A microprocessor system, comprising a single integrated circuit including	See corresponding analysis in Table 1.
a central processing unit and	See corresponding analysis in Table 1.
an entire ring oscillator	See corresponding analysis in Table 1.

variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	See corresponding analysis in Table 1.
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	See corresponding analysis in Table 1.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data	See corresponding analysis in Table 1.

with said central processing unit; and	
a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface,	See corresponding analysis of claim 11 **in Table 2**. **Further Reason for modifying Kato according to Amano in view of Intel 8251A**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato

	according to Amano in view of Intel 8251A.
wherein said central processing unit operates asynchronously to said input/output interface.	See corresponding analysis of claim 11 **in Table 2**. **Further Reason for modifying Kato according to Amano in view of Intel 8251A**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano in view of Intel 8251A.

Claim 12	Kato, Ledzius, Amano, Intel 8251A and Nowatzyk
The microprocessor system of claim 11, in which said second clock is a fixed frequency clock.	See corresponding analysis in Table 1.
Claim 13	**Kato, Ledzius, Amano, Intel 8251A and Nowatzyk**
13. A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate,	See corresponding analysis in Table 1.
said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;	See corresponding analysis in Table 1.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit,	See corresponding analysis in Table 1.
said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,	See corresponding analysis in Table 1.
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic	See corresponding analysis in Table 1.

devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	
an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	See corresponding analysis in Table 1.
an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and	See corresponding analysis of claim 13 **in Table 2**. **Further Reason for modifying Kato according to Amano in view of Intel 8251A**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk

	discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano in view of Intel 8251A.
further wherein said central processing unit operates asynchronously to said input/output interface.	See corresponding analysis of claim 13 **in Table 2**. **Further Reason for modifying Kato according to Amano in view of Intel 8251A**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to

	favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano in view of Intel 8251A.
Claim 14	**Kato, Ledzius, Amano, Intel 8251A and Nowatzyk**
14. The microprocessor system of claim 13, wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	See corresponding analysis in Table 1.
Claim 15	**Kato, Ledzius, Amano, Intel 8251A and Nowatzyk**
15. The microprocessor system of claim 13 wherein said oscillator comprises a ring oscillator.	See corresponding analysis in Table 1.

Claim 16	Kato, Ledzius, Amano, Intel 8251A and Nowatzyk
16. In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:	See corresponding analysis in Table 1.
providing said central processing unit upon an integrated circuit substrate,	See corresponding analysis in Table 1.
said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	See corresponding analysis in Table 1.
providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	See corresponding analysis in Table 1.
clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or	See corresponding analysis in Table 1.

operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	
connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	See corresponding analysis in Table 1.
clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock,	See corresponding analysis of claim 16 **in Table 2**. **Further Reason for modifying Kato according to Amano in view of Intel 8251A**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems,

	where "each processing element may use its own, independent clock." (Nowatzyk, page 22.) For example, Nowatzyk discloses that "Descendants of Caltech's Cosmic Cube tend to favor independent clocks and asynchronous channel protocols." (Nowatzyk, page 59.) Nowatzyk provides further teaching, suggestion and motivation that would have led one of ordinary skill to modify Kato. Regarding asynchronous systems, Nowatzyk discloses: "Asynchronous protocols can tolerate a wide range of channel delays and do not require a carefully designed clock distribution, instead they need carefully designed synchronizers." (Nowatzyk, page 59.) Therefore, Nowatzyk provides further teaching, suggestion and motivation (i.e., to tolerate a wide range of channel delays, to remove the need for a carefully designed clock distribution) that would have led one of ordinary skill to modify Kato. Therefore, it would have been obvious to modify Kato according to Amano in view of Intel 8251A.
wherein said central processing unit operates asynchronously to said input/output interface.	See corresponding analysis of claim 16 **in Table 2**. **Further Reason for modifying Kato according to Amano in view of Intel 8251A**: The prior art itself (i.e., Nowatzyk) provides teaching, suggestion, and motivation that would have led one of ordinary skill to modify Kato according to Amano in view of Intel 8251A to arrive at the claimed invention. In more detail, Nowatzyk discloses asynchronous systems, where "each processing element may use its own, independent

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VI. Conclusion

For the reasons explained above, the following combinations of newly cited references raise SNQs of patentability with respect to the claims of the '336 reexamination certificate: Amano; Amano and Intel 8251A; Amano and Nowatzyk; and Amano, Intel 8251A and Nowatzyk. Therefore, reexamination of claims 1, 2, 6, 7 and 9-16 of the '336 reexamination certificate is respectfully requested.

Respectfully Submitted,

Date: August 20, 2010

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