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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/008,237	11/17/2006	5809336	0081-011D3X2	8857
40972	7590	07/30/2009	EXAMINER	
HENNEMAN & ASSOCIATES, PLC 70 N. MAIN ST. THREE RIVERS, MI 49093			ART UNIT	PAPER NUMBER

DATE MAILED: 07/30/2009

Please find below and/or attached an Office communication concerning this application or proceeding.



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MAILED

SEP 11 2009

CENTRAL REEXAMINATION UNIT

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. 90/008,237.

PATENT NO. 5809336.

ART UNIT 3992.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

**Notice of Intent to Issue
Ex Parte Reexamination Certificate**

Control No.	90/008,237		Patent Under Reexamination
	90/008,306		5809336
	90/008,474		
Examiner	Art Unit		
Sam Rimell	3992		

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ Prosecution on the merits is (or remains) closed in this *ex parte* reexamination proceeding. This proceeding is subject to reopening at the initiative of the Office or upon petition. Cf. 37 CFR 1.313(a). A Certificate will be issued in view of
 - (a) ☐ Patent owner's communication(s) filed: _____.
 - (b) ☐ Patent owner's late response filed: _____.
 - (c) ☐ Patent owner's failure to file an appropriate response to the Office action mailed: _____.
 - (d) ☐ Patent owner's failure to timely file an Appeal Brief (37 CFR 41.31).
 - (e) ☒ Other: Examiner's Amendment of 8/6/09.

Status of *Ex Parte* Reexamination:

 - (f) Change in the Specification: ☒ Yes ☐ No
 - (g) Change in the Drawing(s): ☐ Yes ☒ No
 - (h) Status of the Claim(s):
 - (1) Patent claim(s) confirmed: _____.
 - (2) Patent claim(s) amended (including dependent on amended claim(s)): 1,2,6,7,9 and 10
 - (3) Patent claim(s) cancelled: 3-5 and 8.
 - (4) Newly presented claim(s) patentable: 11-12, 16-17, 19-20 (re-numbered 11-16).
 - (5) Newly presented cancelled claims: 13-15 and 18.
2. ☒ Note the attached statement of reasons for patentability and/or confirmation. Any comments considered necessary by patent owner regarding reasons for patentability and/or confirmation must be submitted promptly to avoid processing delays. Such submission(s) should be labeled: "Comments On Statement of Reasons for Patentability and/or Confirmation."
3. ☐ Note attached NOTICE OF REFERENCES CITED (PTO-892).
4. ☒ Note attached LIST OF REFERENCES CITED (PTO/SB/08).
5. ☐ The drawing correction request filed on _____ is: ☐ approved ☐ disapproved.
6. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the certified copies have
 - ☐ been received.
 - ☐ not been received.
 - ☐ been filed in Application No. _____.
 - ☐ been filed in reexamination Control No. _____.
 - ☐ been received by the International Bureau in PCT Application No. _____.

* Certified copies not received: _____.
7. ☒ Note attached Examiner's Amendment.
8. ☒ Note attached Interview Summary (PTO-474).
9. ☐ Other: _____.

/William H. Wood/
Primary Examiner, Art Unit 3992

/Sue Lao/
OPQA

/Sam Rimell/
Primary Examiner, Art Unit 3992

cc: Requester (if third party requester)

U.S. Patent and Trademark Office
PTOL-469 (Rev.08-06)

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Part of Paper No 20090810

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Examiner's Amendment

• An examiner's amendment to the record appears below. The changes made by this examiner's amendment will be reflected in the reexamination certificate to issue in due course.

• The examiner's amendment was authorized by patent owner in the interview of August 6, 2009. The entry of this amendment is made within patent owner's period for reply, and in accordance with the provisions of 37 CFR 41.33, 37 CFR 1.116. Additionally, MPEP 2274, Section I states:

"Where the appeal brief is not filed, but within the period allowed for filing the brief an amendment is presented which places the claims of the patent under reexamination in a patentable condition, the amendment may be entered."

• Patent owner's proposed reply of 5/12/09 shall not be entered, with the following examiner's amendment entered.

Specification:

At col. 17, line 16, change "a synchronously" to "asynchronously".

Claims:

Claim 1: A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system

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clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface [.] , wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.

Claims 3-5: Claims 3-5 are cancelled.

Claim 6: A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby

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enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator[.] and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.

Claim 8: Claim 8 is cancelled.

Claim 10: In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with

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said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock [.] and wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock.

Claim 11: A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and

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a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein said central processing unit operates asynchronously to said input/output interface.

Claim 12: The microprocessor system of claim 11, in which said second clock is a fixed frequency clock.

Claim 13: A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;

an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;

an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and

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an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and further wherein said central processing unit operates asynchronously to said input/output interface.

Claim 14: The microprocessor system of claim 13 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.

Claim 15: The microprocessor system of claim 13 wherein said oscillator comprises a ring oscillator.

Claim 16: In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with

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said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;

connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and

clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock, wherein said central processing unit operates asynchronously to said input/output interface.

Reasons for Allowability

Preliminary Note: The amendment to the specification at col. 17, line 16 is to correct a typographical error. US application 08/484,918, which matured into US patent 5,809,336 includes an originally filed specification (dated 6/17/95) in which the language corresponding to col. 17, line 16 appears at page 32, line 7. The term "asynchronously" appears instead of "a synchronously", so this examiner's amendment enters the correction.

Allowability of claims: Claims, 1-2, 6-7 and 9-16 are amended by entry of examiner's amendment, based on the agreement of August 6, 2009. The closest identified prior art are:

- Kato (U.S. Patent 4,766,567)

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- Ledzius et al (U.S. Patent 4,691,124)
- Ikeda et al (U.S. Patent 4,910,703)
- McDermott et al (U.S. Patent 4,931,748)

Claim 1: Entry of the examiner's amendment produces claim 1, which recites:

"a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock."

None of the references to Kato Ledzius et al, Ikeda et al and McDermott et al incorporate these recited features, either alone or in combination. Additionally, these features are not present in the remaining prior art of record. Accordingly, claim 1 is determined to be allowable.

Claim 2: Claim 2 has not been amended, and depends on claim 1. Accordingly, claim 2 is allowable based upon its dependence on claim 1.

Claim 6: Entry of the examiner's amendment produces claim 6, which recites:

"an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator."

None of the references to Kato Ledzius et al, Ikeda et al and McDermott et al incorporate these recited features, either alone or in combination. Additionally, these features are not present in the remaining prior art of record. Accordingly, claim 6 is determined to be allowable.

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Claim 7: Claim 7 has not been amended, and depends on claim 6. Accordingly, claim 7 is allowable based upon its dependence on claim 6.

Claim 9: Claim 9 has not been amended, and depends on claim 6. Accordingly, claim 9 is allowable based upon its dependence on claim 6.

Claim 10: Entry of the examiner's amendment produces claim 10, which recites:

"clocking said input/output interface using an off-chip_external clock wherein said off-chip_external clock is operative at a frequency independent of a clock frequency of said variable speed clock and wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock."

None of the references to Kato Ledzius et al, Ikeda et al and McDermott et al incorporate these recited features, either alone or in combination. Additionally, these features are not present in the remaining prior art of record. Accordingly, claim 10 is determined to be allowable.

Claim 11: Entry of the examiner's amendment produces claim 11, which recites:

"a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein said central processing unit operates asynchronously to said input/output interface."

None of the references to Kato Ledzius et al, Ikeda et al and McDermott et al incorporate these recited features, either alone or in combination. Additionally, these features are not present in the remaining prior art of record. Accordingly, claim 11 is determined to be allowable.

Claim 12: Entry of the examiner's amendment produces claim 12 which depends on claim 11. Accordingly, claim 12 is allowable based upon its dependence on claim 11

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Claim 13: Entry of the examiner's amendment produces claim 13, which recites:

"an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and further wherein said central processing unit operates asynchronously to said input/output interface."

None of the references to Kato Ledzius et al, Ikeda et al and McDermott et al incorporate these recited features, either alone or in combination. Additionally, these features are not present in the remaining prior art of record. Accordingly, claim 13 is determined to be allowable.

Claim 14: Entry of the examiner's amendment produces claim 14 which depends on claim 13. Accordingly, claim 14 is allowable based upon its dependence on claim 13.

Claim 15: Entry of the examiner's amendment produces claim 15 which depends on claim 13. Accordingly, claim 15 is allowable based upon its dependence on claim 13.

Claim 16: Entry of the examiner's amendment produces claim 16, which recites:

"clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock, wherein said central processing unit operates asynchronously to said input/output interface."

None of the references to Kato Ledzius et al, Ikeda et al and McDermott et al incorporate these recited features, either alone or in combination. Additionally, these features are not present in the remaining prior art of record. Accordingly, claim 16 is determined to be allowable.

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90/008,237;
90/008,474

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known			
		Application Number	90/008,237, 90/008,306, & 90/008,474		
		Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan, 30, 2007		
		First Named Inventor	—		
		Art Unit	3992		
		Examiner Name	Sam Rimell		
Sheet	1	of	1	Attorney Docket Number	0081-011D3X2

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			

FOREIGN PATENT DOCUMENTS							
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		Country Code ³	Number ⁴	Kind Code ⁵ (if known)			

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
<i>h</i>	A	Intel 80386 Programmer's Reference Manual, published by Intel (1986)	
<i>h</i>	B	Fairchild Microcomputers, F8/3870, F6800, BIT Slice, IC Master 1980, pages 1, 2016-2040 (1980).	
<i>h</i>	C	Mostek Corp., "Mostek 1981 3870/F8 Microcomputer Data Book", February 1981, pp. III-76 through III-77, III-100 through III-129, and VI-1 through VI-11.	
<i>h</i>	D	90-009,457 Request for Reexamination dated 04-24-2009, 98 pages	
<i>h</i>	E	90-040,551 Request for Reexamination dated 05-22-2009, 75 pages	
<i>h</i>	F	90-040,620 Request for Reexamination dated 04-30-2009, 106 pages	
<i>h</i>	G	90-040,562 Request for Reexamination dated 05-29-2009, 62 pages	

Examiner Signature	<i>Sam Rimell</i>	Date Considered	<i>7/10/09</i>
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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

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Examination Unit Form 1448A/PTOINFORMATION DISCLOSURE
STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	12
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Complete if Known

Application Number	90/008,306, 90/008,237, and 90/008,474
Filing Date	October 19, 2006, November 17, 2006, & January 30, 2007
First Named Inventor	Moore
Art Unit	3992
Examiner Name	Joseph R. Pokrzywa
Attorney Docket Number	0081-011D3X1

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
<i>df</i>	AA	US-5,241,636	08-31-1993	Kohn	
<i>df</i>	AB	US-5,127,092	06-30-1992	Gupta et al.	
<i>df</i>	AC	US-5,127,091	06-30-1992	Boufarah et al.	
<i>df</i>	AD	US-5,121,502	06-09-1992	Rau et al.	
<i>df</i>	AE	US-5,091,846	02-25-1992	Sachs et al.	
<i>df</i>	FE	US-5,031,092	07-09-1991	Edwards et al.	
<i>df</i>	FF	US-4,989,133	01-29-1991	May et al.	
<i>df</i>	FG	US-4,980,821	12-25-1990	Koopman et al.	
<i>df</i>	AF	US-4,967,326	10-30-1990	May	
<i>df</i>	AG	US-4,933,835	06-12-1990	Sachs	
<i>df</i>	AH	US-4,926,323	05-15-1990	Baror et al.	
<i>df</i>	AI	US-4,899,275	02-06-1990	Sachs et al.	
<i>df</i>	AJ	US-4,833,599	05-23-1989	Colwell et al.	
<i>df</i>	FH	US-4,819,151	04-04-1989	May	
<i>df</i>	FI	US-4,794,526	12-27-1988	May et al.	
<i>df</i>	FJ	US-4,758,948	07-19-1988	May et al.	
<i>df</i>	FK	US-4,724,517	02-09-1988	May	
<i>df</i>	AK	US-4,714,994	12-22-1987	Oklobdzija	
<i>df</i>	FL	US-4,704,678	11-03-1987	May	
<i>df</i>	AL	US-4,680,698	07-14-1987	Edwards et al.	
<i>df</i>	AM	US-4,566,063	01-21-1986	Zolnowsky	
<i>df</i>	AN	US-4,462,073	07-24-1984	Grondalski	
<i>df</i>	AO	US-4,402,042	08-30-1983	Guttag	
<i>df</i>	AP	US-4,390,946	06-28-1983	Lane	
<i>df</i>	AQ	US-4,348,743	09-07-1982	Dozier	
<i>df</i>	AR	US-4,295,193	10-13-1981	Pomerene	
<i>df</i>	AS	US-3,976,977	08-27-1976	Porter et al.	

Examiner Signature	<i>[Signature]</i>	Date Considered	8/5/09
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Application Number	90/008,306, 90/008,237 & 90/008,474
				Filing Date	October 19, 2006, November 17, 2006, & January 30, 2007
				First Named Inventor	Moore
				Art Unit	3992
				Examiner Name	Joseph R. Pokrzywa
Sheet	2	of	12	Attorney Docket Number	0081-011D3X1

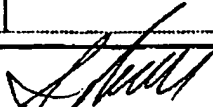
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Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²	
<i>sl</i>	AT	IBM Systems Reference Library, IBM System/360 Model 67 Functional Characteristics, File No. S360-01, Form A27-2719-0, published by IBM (1967).		
<i>sl</i>	AU	ANDERSON, D.W., "The IBM System/360 Model 91: Machine Philosophy and Instruction Handling, IBM Journal, (1967).		
<i>sl</i>	AV	GE-625 / 635 Programming Reference Manual, revised January 1966.		
<i>sl</i>	AW	CLIPPER™ 32-Bit Microprocessor, Introductions to the CLIPER Architecture, published by Fairchild in 1986.		
<i>sl</i>	AX	SIMPSON et al., "The IBM RT PC ROMP processor and Memory management unit architecture," <u>IBM systems Journal</u> , 26(4):346-360.		
<i>sl</i>	AY	M68300 Family MC68332 User's Manual, published by Motorola, Inc. in 1995.		
<i>sl</i>	AZ	DITZEL et al., "The Hardware Architecture of the CRISP Microprocessor," AT & T Information Systems, ACM, pages 309-319 and table of contents (1987).		
<i>sl</i>	BA	i860 64-Bit Microprocessor, published by Intel Corporation February 1989.		
<i>sl</i>	BB	RAU et al., "The Cydra 5 Departmental Supercomputer, Design Philosophies, Decisions, and Trade-offs," <u>IEEE</u> , pages 12-36 (1989).		
<i>sl</i>	BC	Datasheet for Intel 4004 Single Chip 4-Bit 9-Channel Microprocessor, pages 8-15 to 8-23.		
<i>sl</i>	BD	Intel MCS-4 Micro Computer Set (November 1971)		

Examiner Signature	<i>sl</i>	Date Considered	8/27/09
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		Application Number	90/008,306, 90/008,237 & 90/008,474		
		Filing Date	October 19, 2008, November 17, 2008, & January 30, 2007		
		First Named Inventor	Moore		
		Art Unit	3992		
		Examiner Name	Joseph R. Pokrzywa		
Sheet	3	of	12	Attorney Docket Number	0081-011D3X1

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Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), data, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
A	BE	Intel 8008 8-Bit Parallel Central Processor Unit published by Intel (November 1972)	
A	BF	iAPX 386 High Performance 32-Bit Microprocessor Product Review, published by Intel (April 1984)	
A	BG	Intel 80386 Programmer's Reference Manual, published by Intel (1986)	
A	BH	Motorola MC68020 32-Bit Microprocessor User's Manual (1984)	
A	BI	THORNTON, J. E., "Design of a Computer, The Control Data 6600," published by Advanced Design Laboratory (1970).	
A	BJ	6400/6500/6600 Computer Reference Manual, published by Control Data® (1965, 1966, 1967).	
A	BK	GRISHMAN, R., "Assembly Language Programming for the Control Data 6600 and Cyber Series Algorithmics,"	
A	BL	HENNESSY et al., "MIPS: A Microprocessor Architecture," IEEE, pages 17-22 (1982).	
A	BM	HENNESSY et al., "Hardware/software tradeoff for increased performance," <u>Proceedings of the Symposium on Architectural Support for Programming Languages and Operating Systems</u> , pages 2-11. ACM, April 1982	
A	BN	HENNESSY et al., "MIPS: A VLSI Processor Architecture, Technical Report 223," Computer Systems Laboratory, Department of Electrical Engineering and Computer Science, Stanford University November 1981	
A	BO	GROSS et al., "Measurement and evaluation of MIPS architecture and processor," <u>ACM Trans. Computer Systems</u> , pp.229-257 August 1988.	
Examiner Signature			Date Considered 8/5/09

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Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete If Known	
				Application Number	90/008,306, 90/008,237 & 90/008,474
				Filing Date	October 19, 2006, November 17, 2006, & January 30, 2007
				First Named Inventor	Moore
				Art Unit	3992
				Examiner Name	Joseph R. Pokrzywa
Sheet	4	of	12	Attorney Docket Number	0081-011D3X1

NON PATENT LITERATURE DOCUMENTS					
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²		
<i>A</i>	BP	BIT SPARC Integer Unit B5000 Datasheet attached to a presentation by Anant Agrawal in 1989			
<i>el</i>	BQ	SEQUIN et al., "Design and Implementation of RISC I," pages 276-298 from <i>VLSI Architecture</i> , B. Randell and P.C. Treleaven, editors, Prentice Hall, 1983.			
<i>d</i>	BR	UNGAR et al., "Architecture of SOAR: Smalltalk on a RISC," <u>Proceedings of the 11th Annual International Symposium on Computer Architecture ISCA '84</u> , ACM Press, New York, NY, pages 188-197 (1984).			
<i>d</i>	BS	Cray-1 Computer System Hardware Reference Manual, Publication No. 2240004, Rev C, November 4, 1997			
<i>d</i>	BT	Acorn Computers, Ltd., Acorn RISC Machine CPU Software Manual, Issue 1.00 October 1985			
<i>d</i>	BU	PATTERSON et al., "Architecture of a VLSI Instruction Cache for A RISC," <u>ACM</u> , pages 108-116 (1983).			
<i>d</i>	BV	PATTERSON, D. A., "Reduced Instruction Set Computers" <u>Communication of the ACM</u> , 28(1): 8-21, January 1985			
<i>d</i>	BW	PATTERSON, D. A., "RISC watch", pages 11-19 (March 1984).			
<i>d</i>	BX	SHERBURNE, R. W., "Processor Design Tradeoffs in VLSI," U.C. Berkeley, May, 1984. PhD Dissertation.			
<i>d</i>	BY	Excerpt from A Seymour Cray Perspective http://research.microsoft.com/users/gbell/craytalk/sld001.htm (Slide 1)			
<i>d</i>	BZ	Excerpt from A Seymour Cray Perspective http://research.microsoft.com/users/gbell/craytalk/sld029.htm (Slide 29)			
Examiner Signature	<i>[Signature]</i>			Date Considered	8/5/09

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		Filing Date	October 19, 2006, November 17, 2006, & January 30, 2007		
		First Named Inventor	Moore		
		Art Unit	3992		
		Examiner Name	Joseph R. Pokrzywa		
Sheet	5	of	12	Attorney Docket Number	0081-011D3X1

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dl	CA	RISC Roots: CDC 6600 (1965)	
/	CB	http://www.bitsavers.org/pdf/cdc/6x00/	
dl	CC	SIMPSON, R.O., "The IBM RT Personal computer," <u>BYTE</u> 11(11):43-78 (October 1986).	
dl	CD	RYAN, D.P., "Intel's 80960: An Architecture Optimized for Embedded Control," <u>IEEE Micro</u> , published in June 1988.	
dl	CE	WATERS, F., "IBM RT Personal Computer Technology," IBM Corp. 1986.	
dl	CF	Alliacense Product Report, USP 5784584, TLCS-900/H1 Series TMP92C820, Toshiba Microcontroller TMP92C820 / TLCS-900/H1 Series 16-bit Microcontroller, pages 1-9, filed 8/14/06 in 2:05-CV-00494-TJW	
dl	CG	Alliacense Product Report, NEC Microcomputer, USP 5784584, V850E2 32 Bit Microcontroller, pp.1-8 (2006)	
	CH	Application Serial No. 08/484,935, Amendment of June 12, 1997.	
	CI	Office action of 12/21/07 in application no. 90/008,237.	
	CJ	Interview summary of 2/12/08 in application no. 90/008,237.	
	CK	Request for Reexamination of US Patent 5,809,336 as filed 1/30/07 (Public Patent Foundation)	

Examiner Signature	<i>[Signature]</i>	Date Considered	8/5/09
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				Art Unit	3992
				Examiner Name	Joseph R. Pokrzywa
Sheet	6	of	12	Attorney Docket Number	0081-011D3X1

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*	CL	Office action of 4/5/07 in application no. 90/008,474	
*	CM	Request for Reexamination of US Patent 5,809,336 as filed 9/21/06 (NEC)	
*	CN	Office action of 1/19/07 in application no. 90/008,237	
*	CO	Request for Reexamination of US Patent 5,784,584 as filed by NEC 9/21/06.	
*	CP	Office action of 2/9/07 in application 90/008,225	
*	CQ	Office action of 2/12/07 in application 90/008,225	
*	CR	Decision of 6/14/07 Merging application nos. 90/008,225 and 90/008,299.	
*	CS	Office action of 6/26/07 in application no. 90/008,225	
*	CT	Request by Toshiba for Reexamination of US Patent 5,784,584 as filed 10/19/06.	
*	CU	Office action of 12/22/06 in application no. 90/008,299	
*	CV	Office action of 6/26/07 in combined case 90/008,225 and 90/008,299.	

Examiner Signature	<i>[Signature]</i>	Date Considered	8/5/09
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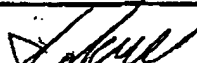
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				Art Unit	3992
				Examiner Name	Joseph R. Pokrzywa
Sheet	7	of	12	Attorney Docket Number	0081-011D3X1

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	CW	Office action response of 9/26/07 in combined case 90/008,225 and 90/008,299.	
	CX	Supp. office action response of 11/13/07 in combined case 90/008,225 and 90/008,299.	
	CY	Daniels Deposition transcript, 8/10/07, in 2:05CV-494 (TIW).	
	CZ	Exhibit 1 to Daniels deposition of 8/10/07 in 2:05CV-494 (TIW). Subpoena of 8/1/07 for Gary Daniels in 2:05CV-494 (TIW).	
	DA	Exhibit 2 to Daniels deposition of 8/10/07 in 2:05CV-494 (TIW). Motorola Semiconductor Products Sector, Microprocessor Products Group, Milestones for Management Review.	
	DB	Exhibit 3 to Daniels deposition of 8/10/07 in 2:05CV-494 (TIW). "How to Take Control" product brochure by Motorola (1988).	
	DC	Exhibit 4 to Daniels deposition of 8/10/07 in 2:05CV-494 (TIW). "Embedded Control Solutions, Powered by Motorola" product brochure by Motorola.	
	DD	Exhibit 5 to Daniels deposition of 8/10/07 in 2:05CV-494 (TIW). 10/20/88 Letter to Daniels from Fisher.	
	DE	Exhibit 6 to Daniels deposition of 8/10/07 in 2:05CV-494 (TIW). List of Motorola Microcontroller business major goals for 1989.	
	DF	Exhibit 7 to Daniels deposition of 8/10/07 in 2:05CV-494 (TIW). Sales brochure, "Motorola Microcontroller Division, Customer Management Briefing Summary".	
	DG	Exhibit 8 to Daniels deposition of 8/10/07 in 2:05CV-494 (TIW). Document titled "Motorola's MC68332 Microcontroller".	

Examiner Signature		Date Considered	8/15/09
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		Filing Date	October 19, 2006, November 17, 2006, & January 30, 2007		
		First Named Inventor	Moore		
		Art Unit	3992		
		Examiner Name	Joseph R. Pokrzywa		
Sheet	8	of	12	Attorney Docket Number	0081-011D3X1

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Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
*	DH	Exhibit 9 to Daniels deposition of 8/10/07 in 2-05CV-494 (TIW): Die photo	
*	DI	Exhibit 10 to Daniels deposition of 8/10/07 in 2-05CV-494 (TIW): Article by Daniels, "A Participant's Perspective," IEEE Micro, 16(6):31-31 plus cover page and 2 unnumbered pages at back of document (1996).	
*	DJ	Exhibit 11 to Daniels deposition of 8/10/07 in 2-05CV-494 (TIW): "A legacy of leadership," Mos Talk, 77(9): 41 pages (1997)	
*	DK	Exhibit 12 to Daniels deposition of 8/10/07 in 2-05CV-494 (TIW): Photo of 68332 with other support chips	
*	DL	McDermott Deposition transcript, 8/9/07, in 2-05CV-494 (TIW)	
*	DM	Exhibit 1 to McDermott deposition of 8/9/07 in 2-05CV-494 (TIW): Subpoena of 8/1/07 for Mark McDermott in 2-05CV-494 (TIW)	
*	DN	Exhibit 2 to McDermott deposition of 8/9/07 in 2-05CV-494 (TIW): "Motorola's MC68332 Microcontroller" layout design	
*	DO	Exhibit 3 to McDermott deposition of 8/9/07 in 2-05CV-494 (TIW): Photos of wafers pre-chip I and II and final wafer and die photo of chip	
*	DP	Exhibit 4 to McDermott deposition of 8/9/07 in 2-05CV-494 (TIW): Photo of Motorola's GMBX 32-bit Microcontroller	
*	DQ	Exhibit 5 to McDermott deposition of 8/9/07 in 2-05CV-494 (TIW): Photo of individual die from pre-chip I, II and the final chip	
*	DR	Exhibit 7 to McDermott deposition of 8/9/07 in 2-05CV-494 (TIW): Patent Application transmittal letter received by USPTO 8/26/88 for application 237022	

Examiner Signature	<i>[Signature]</i>	Date Considered	8/27/09
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		Examiner Name	Joseph R. Pokrzywa		
Sheet	9	of	12	Attorney Docket Number	0081-011D3X1

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	DS	Exhibit 8 to McDermott deposition of 8/9/07 in 2-05CV-494 (TIW). Schematic used to lay out chip	
	DT	Exhibit 10 to McDermott deposition of 8/9/07 in 2-05CV-494 (TIW). McDermott et al., "Testability Features Of the MC68332 Modular Microcontroller," 1989 International Test Conference, paper 28.2, pages 615-623 (1989)	
	DU	Exhibit 11 to McDermott deposition of 8/9/07 in 2-05CV-494 (TIW). McDermott et al., "Modular Design of a High Performance 32-bit Microcontroller," IEEE 1989 Custom Integrated Circuits Conference, pages 21.8.1-21.8.4 (1989)	
	DV	Exhibit 12 to McDermott deposition of 8/9/07 in 2-05CV-494 (TIW). Notes from class taken at University of Texas (September 1987).	
	DW	1/15/08 letter by fax from Rangel (PT) to McFarlane, Hoge, Agarwal & Spears re: non-confidential status of deposition transcripts of Daniels and McDermott	
	DX	10/7/08 letter via e-mail from McFarlane to Hoge, Agarwal, & Spears re: "Attorney Eyes Only" status of depositions of Daniels and McDermott	
	DY	"8 bit Dual 1-chip Microcomputer MN1890 Series User's Manual," translation of original Japanese language document, by Matsushita Electric Industrial Co., Ltd. Semiconductor Sales Division	
	DZ	"Public Availability Date Request," from max Antonelli of Weil Gotshal & Manger LLP re: Transputer Reference Manual, INMOS Ltd, 1988	
	EA	SIBIGTROT, J. M., "Motorola's MC68HC11: Definition and Design of a VLSI Microprocessor," IEEE Micro, 4(1):54-65 (1984)	
	EB	"Specification Sheet, MN18882 (Book)," translation of the Japanese language original, Code No. MIG0175, Matsushita Electronics Industry Corporation, Microcomputer Products Division, 10/2/90	
	EC	"DS5000 Soft Microcontroller User's Guide Preliminary V 1.0," Dallas Semiconductor	
Examiner Signature	<i>[Signature]</i>		Date Considered
			8/6/09

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				First Named Inventor	Moore
				Art Unit	3992
				Examiner Name	Joseph R. Pokrzywa
Sheet	10	of	12	Attorney Docket Number	0081-011D3X1

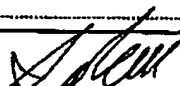
NON PATENT LITERATURE DOCUMENTS					
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	ED	MEI Invalidity Contentions on '148 and '336 patents filed 8/21/07 in case # 2-05CV-494 (TIW)			
	EE	MEI claim charts on MOSTEK 3873 chip, filed 9/8/07 in case # 2-05CV-494 (TIW)			
	EF	Defendants MEI, PNA, and JVC Preliminary Invalidity Contentions filed 9/18/06 in case # 2-05CV-494 (TIW)			
	EG	Defendant NEC Preliminary Invalidity Contentions filed 9/18/06 in case # 2-05CV-494 (TIW)			
	EH	Defendant Toshiba Preliminary Invalidity Contentions filed 9/18/06 in case # 2-05CV-494 (TIW)			
	EI	Defendant NEC Preliminary Invalidity Contentions filed 9/18/06 in case # 2-05CV-494 (TIW)			
	EJ	Defendant ARM Preliminary Invalidity Contentions filed 10/12/06 in case # 2-05CV-494 (TIW)			
	EK	MN188166 User's Manual, Japanese language document with English translation.			
	EL	Complaint for Declaratory Judgment filed 2/8/08 by HTC vs. TPL, Patriot, and Allsource, case # C-08-00882-JB			
	EM	First Amended Complaint filed 2/11/07 by Asustek and Asus vs. TPL, Patriot, MCM, and Allsource, case # C-08-00884-EMC			
	EN	Complaint for Declaratory Judgment filed 2/8/08 by Acer and Gateway vs. TPL, Patriot, and Allsource, case # C-08-00877-HRL			
Examiner Signature	<i>[Signature]</i>			Date Considered	8/6/09

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		Art Unit	3992		
		Examiner Name	Joseph R. Pokrzywa		
Sheet	11	of	12	Attorney Docket Number	0081-011D3X1

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*	EO	Complaint for Declaratory Judgment filed 2/8/08 by Autodesk vs. TPL, Patriot, and Alliacense, case # C08-00884-EMC	
*	EP	Order of Dismissal of NEC Electronics of 12/20/07, case # 3:05-CV-00494 (TIW)	
*	EQ	Order of Dismissal of Matsushita, Panasonic, JVC America, and Toshiba of 12/20/07, case # 3:05-CV-00494 (TIW)	
*	ER	Order of Partial Judgment of Non-Infringement of 9/12/07, case # 3:05-CV-00494 (TIW)	
/	ES	Alliacense Product Report - Preliminary Review, USP 5,440,749; GPS Car Navigation Main Processor	
/	ET	Alliacense Product Report - Preliminary Review, USP 5,440,749; GPS Navigation System GPS Chipset	
/	EU	Alliacense Product Report - Preliminary Review, USP 5,440,749; GPS Navigation System Main Microprocessor	
/	EV	Alliacense Product Report - Preliminary Review, USP 5,440,749; Kyocera Digital Camera Finccam S3R Image Processor	
/	EW	Alliacense Product Report - Preliminary Review, USP 5,440,749; PDA/Mobile Navigation, GPS Processor	
/	EX	Motorola MC68020 32-bit Microprocessor User's Manual, 2nd Edition, Rev. 1, Prentice-Hall, 1985.	
/	EY	BARRON et al., "The Transputer," <u>Electronics</u> pages 109-115 (1983)	
Examiner Signature			Date Considered
		8/6/09	

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				First Named Inventor	Moore
				Art Unit	3992
				Examiner Name	Joseph R. Pokrzywa
Sheet	12	of	12	Attorney Docket Number	0081-011D3X1

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<i>h</i>	EZ	Burroughs Corporation, "Burroughs B7700 Systems Reference Manual," 1973		
<i>h</i>	FA	FIASCONARO, J., "Microarchitecture of the HP9000 Series 500 CPU," <u>Microarchitecture of VLSI Computers, NATO ASI Series No. 96</u> , Antognetti, eds., pages 55-81.		
<i>h</i>	FB	MACGREGOR et al., "The Motorola MC68020," <u>IEEE Micro</u> , 4(4):103-118 (1984).		
<i>h</i>	FC	Request for Reexamination of US Patent 5,440,740 as filed 2/11/08 (ARM)		
<i>h</i>	FD	Office action of 6/26/07 in application no. 90/008,299.		
<i>h</i>	FE	Request for Reexamination of US Patent 5,809,336 as filed 10/19/06 (Toshiba)		
<i>h</i>	FF	Office action of 1/16/07 in application no. 90/008,306		

Examiner Signature	<i>[Signature]</i>	Date Considered	8/6/09
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		Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan. 30, 2007		
		First Named Inventor	---		
		Art Unit	3992		
		Examiner Name	Sam Rimell		
Sheet	1	of	14	Attorney Docket Number	0081-011D3X1

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cao No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
<i>[initials]</i>	AA	3,603,934	09-07-1971	Heath, Jr. et al.	
<i>[initials]</i>	AB	3,849,765	11-19-1974	Hamano	
<i>[initials]</i>	AC	3,878,513	04-15-1975	Werner	
<i>[initials]</i>	AD	3,924,245	12-02-1975	Eaton et al.	
<i>[initials]</i>	AE	3,968,501	07-06-1976	Gilbert	
<i>[initials]</i>	AF	4,003,033	01-11-1977	O'Keefe et al.	
<i>[initials]</i>	AG	4,037,090	07-19-1977	Raymond, Jr.	
<i>[initials]</i>	AH	4,050,058	09-20-1977	Garlic	
<i>[initials]</i>	AI	4,067,058	01-03-1978	Brandstaetter et al.	
<i>[initials]</i>	AJ	4,067,059	01-03-1978	Darchak	
<i>[initials]</i>	AK	4,075,691	02-21-1978	Davis et al.	
<i>[initials]</i>	AL	4,079,455	03-14-1978	Ozga	
<i>[initials]</i>	AM	4,110,822	08-28-1978	Porter et al.	
<i>[initials]</i>	AN	4,125,871	11-14-1978	Martin	
<i>[initials]</i>	AO	4,128,873	12-05-1978	Lamiaux	
<i>[initials]</i>	AP	4,144,562	03-13-1979	Cooper	
<i>[initials]</i>	AQ	4,217,637	08-12-1980	Faulkner et al.	
<i>[initials]</i>	AR	4,224,676	09-23-1980	Appelt	
<i>[initials]</i>	AS	4,236,152	11-25-1980	Masuzawa et al.	
<i>[initials]</i>	AT	4,253,785	03-03-1981	Bronstein	
<i>[initials]</i>	BA	4,255,785	03-10-1981	Chamberlin	
<i>[initials]</i>	BB	4,292,668	09-29-1981	Miller et al.	
<i>[initials]</i>	BC	4,315,308	02-09-1982	Jackson	
<i>[initials]</i>	BD	4,320,467	03-16-1982	Glass	
<i>[initials]</i>	BE	4,321,706	03-23-1982	Craft	
<i>[initials]</i>	BF	4,328,557	05-04-1982	Gastinel	
<i>[initials]</i>	BG	4,335,447	06-15-1982	Jerrim	
<i>[initials]</i>	BH	4,354,228	10-12-1982	Moore et al.	
<i>[initials]</i>	BI	4,361,869	11-30-1982	Johnson et al.	
<i>[initials]</i>	BJ	4,376,977	03-15-1983	Bruinshorst	
<i>[initials]</i>	BK	4,382,279	05-03-1983	Ugon	
<i>[initials]</i>	BL	4,398,265	08-09-1983	Puhl et al.	
<i>[initials]</i>	BM	4,403,303	09-06-1983	Howes et al.	

Examiner Signature	<i>[Signature]</i>	Date Considered	7/10/09
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Substitute for form 1449/PTO		Complete if Known	
		Application Number	90/008,237, 90/008,306, & 90/008,474
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan. 30, 2007
		First Named Inventor	---
		Art Unit	3992
		Examiner Name	Sam Rimell
Sheet	2	of	14
		Attorney Docket Number	0081-011D3X1

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
<i>h</i>	BN	4,449,201	05-15-1984	Clark	
<i>h</i>	BO	4,450,519	05-22-1984	Gutttag et al.	
<i>h</i>	BP	4,463,421	07-31-1984	Laws	
<i>h</i>	BQ	4,488,217	12-11-1984	Binder et al.	
<i>h</i>	BR	4,509,115	04-02-1985	Manton et al.	
<i>h</i>	BS	4,538,239	08-27-1985	Magar	
<i>h</i>	BT	4,541,045	09-10-1985	Kromer, III	
<i>h</i>	BU	4,541,111	09-10-1985	Takashima et al.	
<i>h</i>	BV	4,562,537	12-31-1985	Barnett et al.	
<i>h</i>	CA	4,577,282	03-18-1986	Caudel et al.	
<i>h</i>	CB	4,607,332	08-19-1986	Goldberg	
<i>h</i>	CC	4,616,338	10-07-1986	Helen et al.	
<i>h</i>	CD	4,626,985	12-02-1986	Briggs	
<i>h</i>	CE	4,626,988	12-02-1986	George	
<i>h</i>	CF	4,630,195	12-16-1986	Hester et al.	
<i>h</i>	CG	4,649,471	03-10-1987	Briggs et al.	
<i>h</i>	CH	4,679,166	07-07-1987	Berger et al.	
<i>h</i>	CI	4,709,329	11-24-1987	Hecker	
<i>h</i>	CJ	4,713,749	12-15-1987	Magar et al.	
<i>h</i>	CK	4,720,812	01-19-1988	Kao et al.	
<i>h</i>	CL	4,760,521	07-26-1988	Rehwalder et al.	
<i>h</i>	CM	4,772,888	09-20-1988	Kimura	
<i>h</i>	CN	4,777,591	10-11-1988	Chang et al.	
<i>h</i>	CO	4,787,032	03-18-1986	Caudel et al.	
<i>h</i>	CP	4,803,621	02-07-1989	Kelly	
<i>h</i>	CQ	4,805,091	02-14-1989	Thiel et al.	
<i>h</i>	CR	4,809,169	02-28-1989	Sfarti et al.	
<i>h</i>	CS	4,809,269	02-28-1989	Gulick	
<i>h</i>	CT	4,811,208	03-07-1989	Myers et al.	
<i>h</i>	CU	4,835,738	05-30-1989	Niehaus et al.	
<i>h</i>	DA	4,837,682	06-06-1989	Culler	
<i>h</i>	DB	4,860,198	08-22-1989	Takenaka	
<i>h</i>	DC	4,868,735	09-19-1989	Moller et al.	

Examiner Signature	<i>Sam Rimell</i>	Date Considered	7/10/09
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		Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan. 30, 2007		
		First Named Inventor	—		
		Art Unit	3992		
		Examiner Name	Sam Rimell		
Sheet	3	of	14	Attorney Docket Number	0081-011D3X1



U.S. PATENT DOCUMENTS					
Examiner Initials ¹	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
<i>[initials]</i>	DD	4,870,562	09-26-1989	Kimoto et al.	
<i>[initials]</i>	DE	4,890,225	12-26-1989	Ellis, Jr. et al.	
<i>[initials]</i>	DF	4,907,225	03-06-1990	Gulick et al.	
<i>[initials]</i>	DG	4,912,632	03-27-1990	Gach et al.	
<i>[initials]</i>	DH	4,914,578	04-03-1990	MacGregor et al.	
<i>[initials]</i>	DI	4,931,986	06-05-1990	Daniel et al.	
<i>[initials]</i>	DJ	4,942,553	07-17-1990	Dalrymple et al.	
<i>[initials]</i>	DK	4,959,782	09-25-1990	Tulpule et al.	
<i>[initials]</i>	DL	4,967,326	10-30-1990	May	
<i>[initials]</i>	DM	4,967,398	10-30-1990	Jamova et al.	
<i>[initials]</i>	DN	4,979,102	12-18-1990	Tokuume	
<i>[initials]</i>	DO	5,021,991	06-04-1991	MacGregor et al.	
<i>[initials]</i>	DP	5,047,921	09-10-1991	Kinter et al.	
<i>[initials]</i>	DQ	5,068,781	11-26-1991	Gillett, Jr. et al.	
<i>[initials]</i>	DR	5,081,574	01-14-1992	Larsen et al.	
<i>[initials]</i>	DS	5,097,437	03-17-1992	Larson et al.	
<i>[initials]</i>	DT	5,103,499	04-07-1992	Miner et al.	
<i>[initials]</i>	DU	5,134,701	07-28-1992	Mueller et al.	
<i>[initials]</i>	DV	5,148,592	07-28-1992	Mueller et al.	
<i>[initials]</i>	DW	5,148,385	09-15-1992	Frazier	
<i>[initials]</i>	DX	5,179,734	01-12-1993	Candy et al.	
<i>[initials]</i>	EA	5,226,147	07-06-1993	Fujishima et al.	
<i>[initials]</i>	EB	5,239,631	08-24-1993	Boury et al.	
<i>[initials]</i>	EC	5,261,057	11-09-1993	Coyle et al.	
<i>[initials]</i>	ED	5,261,109	11-09-1993	Cadambi et al.	
<i>[initials]</i>	EE	5,325,513	06-28-1994	Tanaka et al.	
<i>[initials]</i>	EF	5,339,448	08-16-1994	Tanaka et al.	
<i>[initials]</i>	EG	5,353,417	10-04-1994	Fuoco et al.	
<i>[initials]</i>	EH	5,353,427	10-04-1994	Fujishima et al.	
<i>[initials]</i>	EI	5,379,438	01-03-1995	Bell et al.	
<i>[initials]</i>	EJ	5,410,654	04-25-1995	Foster et al.	
<i>[initials]</i>	EK	5,410,682	04-25-1995	Sites et al.	
<i>[initials]</i>	EL	5,414,862	05-09-1995	Suzuki et al.	

Examiner Signature	<i>[Signature]</i>	Date Considered	7/10/09
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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known			
		Application Number	90/008,237, 90/008,306, & 90/008,474		
		Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan. 30, 2007		
		First Named Inventor	—		
		Art Unit	3992		
		Examiner Name	Sam Rimell		
Sheet	4	of	14	Attorney Docket Number	0081-011D3X1

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (Patent)			
	EM	5,421,000	05-30-1995	Fortino et al.	
	EN	5,459,846	10-17-1995	Hyatt	
	EO	5,530,890	06-25-1996	Moore et al.	
	EP	5,604,915	02-18-1997	Moore et al.	
	EQ	5,659,703	08-19-1997	Moore et al.	

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
	ER	JP	05-189383		07-30-1998	Foster		<input type="checkbox"/>
	ES	EP	0288649		11-02-1988	IBM		<input type="checkbox"/>

Examiner Signature	<i>[Signature]</i>	Date Considered	7/10/07
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		First Named Inventor	—		
		Art Unit	3992		
		Examiner Name	Sam Rimell		
Sheet	5	of	14	Attorney Docket Number	0081-011D3X1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
<i>SL</i>	ET	BEST et al., "An Advanced-Architecture CMOS/SOS Microprocessor", IEEE Micro, vol. 2, No. 3, Vol. 2, No. 3 (July 1982), pp. 10-26	
<i>SL</i>	EU	TECHNOLOGY PROPERTIES LIMITED (TPL), Moore Microprocessor Patent (MMP) Portfolio, downloaded from << www.tplgroup.net/patents/index.php>> downloaded on August 3, 2006, 3 pages total.	
<i>X</i>	EV	U.S. Appin No. 07/389,334, Amendment After Notice of Allowance dated March 22, 1995, 2 pages total	
<i>X</i>	EW	U.S. Appin No. 07/389,334, Amendment dated February 28, 1995, 2 pages total	
<i>X</i>	EX	U.S. Appin No. 07/389,334, Amendment dated June 03, 1992, 18 pages total	
<i>X</i>	EY	U.S. Appin No. 07/389,334, Amendment dated June 30, 1993, 18 pages total	
<i>X</i>	FA	U.S. Appin No. 07/389,334, Amendment dated March 17, 1994, 7 pages total	
<i>X</i>	FB	U.S. Appin No. 08/480,206, Amendment dated March 4, 1996, 5 pages total	
<i>X</i>	FC	U.S. Appin No. 07/389,334, Amendment dated November 9, 1994, 2 pages total.	
<i>X</i>	FD	U.S. Appin No. 07/389,334, Amendment dated October 26, 1994, 2 pages total	

Examiner Signature	<i>SL</i>	Date Considered	7/00/09
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				Application Number	90/008,237, 90/008,306, & 90/008,474
				Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan. 30, 2007
				First Named Inventor	---
				Art Unit	3992
				Examiner Name	Sam Rimell
Sheet	6	of	14	Attorney Docket Number	0081-011D3X1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
*	FE	U.S. Appl. No. 07/389,334, Final Office Action dated June 9, 1994, 6 pages total	
*	FF	U.S. Appl. No. 07/389,334, Notice of Allowance dated November 20, 1994, 4 pages total	
*	FG	U.S. Appl. No. 07/389,334, Office Action dated December 3, 1991, 9 pages total	
*	FH	U.S. Appl. No. 07/389,334, Office Action dated December 31, 1992, 10 pages total	
*	FI	U.S. Appl. No. 07/389,334, Office Action dated November 2, 1993, 5 pages total	
*	FJ	U.S. Appl. No. 07/389,334, Requirement for Restriction dated August 31, 1992, 4 pages total	
*	FK	U.S. Appl. No. 07/389,334, Response to Restriction Requirement dated September 29, 1992, 2 pages total	
*	FL	U.S. Appl. No. 08/480,206, Supplemental Notice of Allowability dated April 2, 1996, 2 pages total	
*	FM	U.S. Appl. No. 08/480,206, Notice of Allowance dated December 12, 1995, 7 pages total	
*	FN	U.S. Appl. No. 08/480,462, Amendment dated April 6, 1998, 7 pages total	

Examiner Signature		Date Considered	7/12/09
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		Application Number	90/008,237, 90/008,306, & 90/008,474		
		Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan, 30, 2007		
		First Named Inventor	---		
		Art Unit	3992		
		Examiner Name	Sam Rimell		
Sheet	7	of	14	Attorney Docket Number	0081-011D3X1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
*	FO	U.S. Appl. No. 08/480,462, Office Action dated December 8, 1995, 4 pages total	
*	FP	U.S. Appl. No. 08/480,462, Office Action dated July 12, 1996, 6 pages total	
*	FQ	U.S. Appl. No. 08/480,901, Amendment dated May 9, 1996, 7 pages total.	
*	FR	U.S. Appl. No. 08/480,901, Non-Final Office Action dated July 30, 1996, 4 pages total.	
*	FS	U.S. Appl. No. 08/480,901, Non-Final Office Action dated November 14, 1996, 3 pages total	
*	FT	U.S. Appl. No. 08/480,901, Notice of Abandonment dated March 17, 1997, 1 page total.	
*	FU	U.S. Appl. No. 08/480,911, Amendment dated May 15, 1996, 10 pages total	
*	FV	U.S. Appl. No. 08/480,911, Non-Final Office Action dated August 26, 1996, 5 pages total	
*	FW	U.S. Appl. No. 08/480,911, Non-Final Office Action dated November 15, 1995, 4 pages total	
*	FX	U.S. Appl. No. 08/480,911, Notice of Abandonment dated March 31, 1997, 1 page total	

Examiner Signature		Date Considered	7/10/09
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				Art Unit	3992
				Examiner Name	Sam Rimell
Sheet	8	of	14	Attorney Docket Number	0081-011D3X1

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	FY	U.S. Appl. No. 08/482,185, Amendment dated January 24, 1997, 8 pages total	
	FZ	U.S. Appl. No. 08/482,185, Amendment dated May 8, 1996, 12 pages total	
	GA	U.S. Appl. No. 08/482,185, Notice of Allowability dated March 7, 1997, 2 pages total	
	GB	U.S. Appl. No. 08/482,185, Office Action dated July 22, 1996, 6 pages total	
	GC	U.S. Appl. No. 08/482,185, Office Action dated November 8, 1995, 6 pages total	
	GD	U.S. Appl. No. 08/484,015, Amendment dated June 28, 1996, 7 pages total	
	GE	U.S. Appl. No. 08/484,015, Notice of Abandonment dated April 28, 1997, 1 page total	
	GF	U.S. Appl. No. 08/484,015, Office Action dated September 20, 1996, 5 pages total	
	GG	U.S. Appl. No. 08/484,015, Office Action dated January 4, 1996, 6 pages total	
	GH	U.S. Appl. No. 08/484,230, Amendment dated May 7, 1996, 8 pages total	

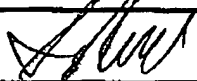
Examiner Signature	<i>[Signature]</i>	Date Considered	7/10/09
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PUBLICATION

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			Art Unit	3992	
			Examiner Name	Sam Rimell	
Sheet	9	of	14	Attorney Docket Number	0081-011D3X1

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*	GI	U.S. Appln No. 08/484,230, Office Action dated December 7, 1995, 5 pages total	
*	GJ	U.S. Appln No. 08/484,230, Office Action dated July 16, 1996, 6 pages total	
*	GK	U.S. Appln No. 08/484,230, Revised Amendment dated May 13, 1996, 8 pages total	
*	GL	U.S. Appln No. 08/484,918, Amendment dated April 11, 1996, 10 pages total	
*	GM	U.S. Appln No. 08/484,918, Amendment dated April 24, 1998, 3 pages total	
*	GN	U.S. Appln No. 08/484,918, Amendment dated February 6, 1998, 5 pages total	
*	GO	U.S. Appln No. 08/484,918, Amendment dated January 7, 1997, 2 pages total	
*	GP	U.S. Appln No. 08/484,918, Amendment dated January 8, 1997, 6 pages total	
*	GQ	U.S. Appln No. 08/484,918, Amendment dated July 3, 1997, 5 pages total	
*	GR	U.S. Appln No. 08/484,918, Final Office Action dated July 6, 1996, 5 pages total	

Examiner Signature		Date Considered	7/12/09
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
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4 NOT A PATENT OR PRINTED PUBLICATION

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known			
		Application Number	90/008,237, 90/008,306, & 90/008,474		
		Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan. 30, 2007		
		First Named Inventor	---		
		Art Unit	3992		
		Examiner Name	Sam Rimell		
Sheet	10	of	14	Attorney Docket Number	0081-011D3X1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
*	GS	U.S. Appln No. 08/484,918, Interview Summary dated May 13, 1998, 1 pages total	
*	GT	U.S. Appln No. 08/484,918, Notice of Allowance dated May 13, 1998, 4 pages total	
*	GU	U.S. Appln No. 08/484,918, Office Action dated April 3, 1997, 3 pages total	
*	GV	U.S. Appln No. 08/484,918, Office Action dated December 12, 1995, 4 pages total	
*	GW	U.S. Appln No. 08/484,918, Office Action dated October 16, 1997, 6 pages total	
*	GX	U.S. Appln No. 08/484,920, Notice of Abandonment dated June 25, 1996, 1 page total	
*	GY	U.S. Appln No. 08/484,920, Office Action dated November 22, 1995, 3 pages total	
*	GZ	U.S. Appln No. 08/484,935, Amendment dated April 8, 1996, 14 pages total	
*	HA	U.S. Appln No. 08/484,935, Amendment dated February 5, 1998, 9 pages total	
*	HB	U.S. Appln No. 08/484,935, Amendment dated June 12, 1997, 14 pages total	

Examiner Signature		Date Considered	7/10/09
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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

* NOT A PATENT OR PRINTED PUBLICATION

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known			
		Application Number	90/008,237, 90/008,306, & 90/008,474		
		Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan, 30, 2007		
		First Named Inventor	---		
		Art Unit	3992		
		Examiner Name	Sam Rimell		
Sheet	11	of	14	Attorney Docket Number	0081-011D3X1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
*	HC	U.S. Appl. No. 08/484,935, Amendment dated November 21, 1997, 11 pages total	
*	HD	U.S. Appl. No. 08/484,935, Notice of Allowance dated February 13, 1998, 2 pages total	
*	HE	U.S. Appl. No. 08/484,935, Office Action dated August 22, 1997, 4 pages total	
*	HF	U.S. Appl. No. 08/484,935, Office Action dated December 12, 1996, 5 pages total	
*	HG	U.S. Appl. No. 08/484,935, Office Action dated December 7, 1995, 7 pages total	
*	HH	U.S. Appl. No. 08/486,454, Amendment dated May 8, 1996, 7 pages total	
*	HI	U.S. Appl. No. 08/486,454, Final Office Action dated July 24, 1996, 4 pages total	
*	HJ	U.S. Appl. No. 08/486,454, Non-Final Office Action dated November 08, 1995, 4 pages total	
*	HK	U.S. Appl. No. 08/486,454, Notice of Abandonment dated March 4, 1997, 1 page total	
*	HL	U.S. Appl. No. 09/051,263, Amendment dated April 30, 2009, 9 pages total	

Examiner Signature		Date Considered	7/10/09
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				Application Number	90/008,237, 90/008,306, & 90/008,474
				Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan. 30, 2007
				First Named Inventor	---
				Art Unit	3992
				Examiner Name	Sam Rimell
Sheet	12	of	14	Attorney Docket Number	0081-011D3X1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
*	HM	U.S. Appl. No. 09/051,263, Amendment dated January 9, 2008, 10 pages total	
*	HN	U.S. Appl. No. 09/051,263, Amendment dated July 12, 2002, 4 pages total	
*	HO	U.S. Appl. No. 09/051,263, Office Action dated July 26, 2006, 6 pages total	
*	HP	U.S. Appl. No. 09/051,263, Amendment dated September 17, 2007, 5 pages total	
*	HQ	U.S. Appl. No. 09/051,263, Amendment dated September 25, 2006, 4 pages total	
*	HR	U.S. Appl. No. 09/051,263, Interview Summary dated September 14, 2006, 4 pages total	
*	HS	U.S. Appl. No. 09/051,263, Non-Compliant Amendment dated June 27, 2007, 14 pages total	
*	HT	U.S. Appl. No. 09/051,263, Notice of Non-Compliant Amendment dated July 17, 2007, 3 pages total	
*	HU	U.S. Appl. No. 09/051,263, Notice of Non-Compliant Amendment dated December 12, 2007, 3 pages total	
*	HV	U.S. Appl. No. 09/051,263, Office Action dated January 18, 2000, 2 pages total	

Examiner Signature		Date Considered	7/12/09
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				Application Number	90/008,237, 90/008,306, & 90/008,474
				Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan, 30, 2007
				First Named Inventor	---
				Art Unit	3992
				Examiner Name	Sam Rimell
Sheet	13	of	14	Attorney Docket Number	0081-011D3X1

NON PATENT LITERATURE DOCUMENTS			
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*	HW	U.S. Appl. No. 09/051,263, Office Action dated May 16, 2000, 2 pages total	
*	HX	U.S. Appl. No. 09/051,263, Office Action dated October 30, 2000, 14 pages total	
*	HY	U.S. Appl. No. 09/051,263, Response to Restriction Requirement dated August 8, 2000, 1 page total	
*	HZ	U.S. Appl. No. 09/051,263, Restriction Requirement dated April 8, 2000, 16 pages total	
*	IA	U.S. Appl. No. 09/051,263, Office Action Summary dated December 27, 2000, 23 pages total	
*	IB	U.S. Appl. No. 09/051,263, Restriction Requirement dated June 12, 2000, 6 pages total	
*	IC	U.S. Appl. No. 09/051,263, Notice of Abandonment dated December 22, 2000, 2 pages total	
*	ID	U.S. Appl. No. 09/124,623, Amendment dated April 29, 2002, 11 pages total	
*	IE	U.S. Appl. No. 09/124,623, Amendment dated December 6, 2002, 2 pages total	
*	IF	U.S. Appl. No. 09/124,623, Notice of Abandonment dated September 14, 2000, 2 pages total	

Examiner Signature		Date Considered	7/17/09
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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** NOT A PATENT OR PRINTED PUBLICATION*

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	90/008,237, 90/008,306, & 90/008,474
				Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan, 30, 2007
				First Named Inventor	---
				Art Unit	3992
				Examiner Name	Sam Rimell
Sheet	14	of	14	Attorney Docket Number	0081-011D3X1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
*	IG	U.S. Appl. No. 09/124,623, Notice of Allowance dated September 9, 2002, 2 pages total	
*	IH	U.S. Appl. No. 09/124,623, Office Action dated January 31, 2000, 5 pages total	
*	II	U.S. Appl. No. 09/124,623, Office Action dated June 10, 2003, 2 pages total	
*	IJ	U.S. Appl. No. 08/485,031, Office Action dated November 28, 1995, 6 pages total	
*	IK	U.S. Appl. No. 08/485,031, Amendment dated April 29, 1996, 10 pages total	
*	IL	U.S. Appl. No. 08/485,031, Notice of Allowance dated July 19, 1996, 2 pages total	

Examiner Signature		Date Considered	7/10/09
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* NOT A PATENT OR
PUBLISHED PUBLICATION

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		Application Number	90/008,237, 90/008,306, & 90/008,474		
		Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan, 30, 2007		
		First Named Inventor	—		
		Art Unit	3992		
		Examiner Name	Sam Rimell		
Sheet	1	of	28	Attorney Docket Number	0081-011D3X1

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
<i>h</i>	AA	4,988,892	01-29-1991	Needle	
<i>h</i>	AB	3,698,414	10-03-1972	Allen et al.	
<i>h</i>	AC	3,967,104	08-29-1976	Brantingham et al.	
<i>h</i>	AD	3,980,993	09-14-1976	Bredart et al.	
<i>h</i>	AE	4,003,028	01-11-1977	Bennett et al.	
<i>h</i>	AF	4,042,972	08-16-1977	Gruner et al.	
<i>h</i>	AG	4,050,096	09-20-1977	Bennett et al.	
<i>h</i>	AH	4,107,773	08-15-1978	Gilbreath et al.	
<i>h</i>	AI	4,112,490	09-05-1978	Pohlman et al.	
<i>h</i>	AJ	4,223,880	09-23-1980	Brems	
<i>h</i>	AK	4,242,735	12-30-1980	Sexion	
<i>h</i>	AL	4,305,045	12-08-1981	Metz et al.	
<i>h</i>	AM	4,315,305	02-09-1982	Jackson	
<i>h</i>	AN	4,317,227	02-23-1982	Skerlos	
<i>h</i>	AO	4,338,675	07-06-1982	Palmer et al.	
<i>h</i>	AP	4,348,720	09-07-1982	Blahut et al.	
<i>h</i>	AQ	4,348,743	09-07-1982	Dozier	
<i>h</i>	AR	4,358,728	11-09-1982	Hashimoto	
<i>h</i>	AS	4,364,112	12-14-1982	Onodera et al.	
<i>h</i>	AT	4,396,979	08-02-1983	Mor et al.	
<i>h</i>	AU	4,398,263	08-09-1983	Ito	
<i>h</i>	AV	4,412,283	10-25-1983	Mor et al.	
<i>h</i>	AW	4,425,628	01-10-1984	Bedard et al.	
<i>h</i>	AX	4,467,810	08-28-1984	Vollmann	
<i>h</i>	AY	4,471,426	09-11-1984	McDonough	
<i>h</i>	AZ	4,472,789	09-18-1984	Sibley	
<i>h</i>	BA	4,539,655	09-03-1985	Trussell et al.	
<i>h</i>	BB	4,553,201	11-12-1985	Pollack et al.	

Examiner Signature	<i>[Signature]</i>	Date Considered	7/9/09
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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known			
		Application Number	90/008,237, 90/008,306, & 90/008,474		
		Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan, 30, 2007		
		First Named Inventor	—		
		Art Unit	3992		
		Examiner Name	Sam Rimell		
Sheet	2	of	28	Attorney Docket Number	0081-011D3X1

U.S. PATENT DOCUMENTS					
Examiner Initials ¹	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
<i>h</i>	BC	4,556,063	12-03-1985	Thompson et al.	
<i>h</i>	BD	4,626,798	12-02-1986	Fried	
<i>h</i>	BE	4,627,082	12-02-1986	Pelgrom et al.	
<i>h</i>	BF	4,630,934	12-23-1986	Arber	
<i>h</i>	BG	4,641,246	02-03-1987	Halbert et al.	
<i>h</i>	MI	4,660,180	04-21-1987	Tanimura et al.	
<i>h</i>	BH	4,665,495	05-12-1987	Thaden	
<i>h</i>	BI	4,670,837	06-02-1987	Sheets	
<i>h</i>	BJ	4,698,750	10-06-1987	Wilkie et al.	
<i>h</i>	BK	4,701,884	10-20-1987	Aoki et al.	
<i>h</i>	BL	4,708,490	11-24-1987	Arber	
<i>h</i>	MH	4,713,749	12-15-1987	Magar et al.	
<i>h</i>	BM	4,739,475	04-19-1988	Mensch, Jr.	
<i>h</i>	BN	4,761,763	08-02-1988	Hicks	
<i>h</i>	BO	4,780,814	10-25-1988	Hayek	
<i>h</i>	BP	4,797,850	01-10-1989	Amitai	
<i>h</i>	BQ	4,816,989	03-25-1989	Finn et al.	
<i>h</i>	BR	4,837,563	06-06-1989	Mansfield et al.	
<i>h</i>	MJ	4,853,841	08-01-1989	Richter	
<i>h</i>	BS	4,882,710	11-21-1989	Hashimoto et al.	
<i>h</i>	BT	4,910,703	03-20-1990	Ikeda et al.	
<i>h</i>	MG	4,956,811	09-11-1990	Kajigaya et al.	
<i>h</i>	BU	4,967,352	10-30-1990	Keida et al.	
<i>h</i>	BV	4,974,157	11-27-1990	Winfield et al.	
<i>h</i>	BW	4,980,821	12-25-1990	Koopman et al.	
<i>h</i>	BX	4,989,113	01-29-1991	Hull, Jr. et al.	
<i>h</i>	BY	4,989,135	01-29-1991	Miki	
<i>h</i>	BZ	4,990,847	02-05-1991	Ishimaru et al.	

Examiner Signature	<i>Adler</i>	Date Considered	7/8/09
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				Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan. 30, 2007
				First Named Inventor	—
				Art Unit	3992
				Examiner Name	Sam Rimell
Sheet	3	of	28	Attorney Docket Number	0081-011D3X1

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		Number Kind Code ² (if known)				
<i>d</i>	CA	5,008,816	04-16-1991	Fogg, Jr. et al.		
<i>d</i>	CB	5,013,985	05-07-1991	Itoh et al.		
<i>d</i>	CC	5,022,395	06-11-1991	Russie		
<i>d</i>	CD	5,023,689	06-11-1991	Sugawara		
<i>d</i>	CE	5,031,092	07-09-1991	Edwards et al.		
<i>d</i>	CF	5,036,300	07-30-1991	Nicolai		
<i>d</i>	CG	5,036,460	07-30-1991	Takahira et al.		
<i>d</i>	CH	5,053,952	10-01-1991	Koopman, Jr. et al.		
<i>d</i>	CI	5,070,451	12-03-1991	Moore et al.		
<i>d</i>	CJ	5,109,495	04-28-1992	Fite et al.		
<i>d</i>	CK	5,157,772	10-20-1992	Watanabe		
<i>d</i>	CL	5,179,689	01-12-1993	Leach et al.		
<i>d</i>	CM	5,261,082	11-09-1993	Ito et al.		
<i>d</i>	CN	5,379,438	01-03-1995	Bell et al.		
<i>d</i>	CO	5,414,862	05-09-1995	Suzuki et al.		
<i>d</i>	CP	5,511,209	04-23-1996	Mensch, Jr.		
<i>d</i>	CQ	5,537,565	07-16-1996	Hyatt		

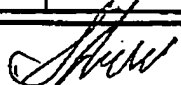
FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ^o
		Country Code ²	Number ³	Kind Code ³ (if known)				
<i>d</i>	CR	JP	62-145413		06-29-1987	NEC Corporation		<input type="checkbox"/>
<i>d</i>	CS	EP	0 200 797	A1	11-12-1986	ITT IND GMBH DEUTSCHE		<input type="checkbox"/>
<i>H</i>	CT	EP	0 208 287			NEC Corporation		<input type="checkbox"/>

Examiner Signature	<i>Sam Rimell</i>	Date Considered	7/9/09
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		Application Number	90/008,237, 90/008,306, & 90/008,474		
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		Art Unit	3992		
		Examiner Name	Sam Rimell		
Sheet	4	of	28	Attorney Docket Number	0081-011D3X1

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+	CU	90/009,034 Non-Final Office Action dated 03-04-2009	
+	CV	90/009,389 Reexam Ordered 04-08-2009	
+	CW	90/009,389 Request for Reexamination dated 01-16-2009	
+	CX	90-008,225 and 90-008,299 Final Office Action dated 12-05-08	
+	CY	90-008,225 and 90-008,299 Notice of Intent to Issue a Reexam Certificate dated 04-21-09	
+	CZ	90-008,225 Notice of Failure to Comply with Ex Parte Reexamination Request Filing Requirements dated 10-16-2006	
+	DA	90-008,225 Response to Notice of Failure to Comply with Ex Parte Reexamination Request Filing Requirements: Letter Accompany Replacement PTO Form, SB/42, dated 11-15-06	
+	DB	90-008,227 Examiner Interview Summary Record dated 03-03-09	
+	DC	90-008,227 Examiner Interview Summary Record dated 07-30-09	
+	DD	90-008,227 Non-Final Office Action dated 01-26-09	
Examiner Signature			Date Considered
			7/9/09

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		Art Unit	3992		
		Examiner Name	Sam Rimell		
Sheet	5	of	28	Attorney Docket Number	0081-011D3X1

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*	DE	90-008,227 Non-Final Office Action dated 06-25-08	
*	DF	90-008,227 Response to Non-Final Office Action 02-24-08	
*	DG	90-008,227 Response to Non-Final Office Action dated 08-25-08	
*	DH	90-008,227 Response to Non-Final Office Action dated 3-28-09	
*	DI	90-008,227 Response to Non-Final Office Action dated 3-27-09	
*	DJ	90-008,306 Non-Final Office Action dated 07-02-08	
*	DK	90-008,388 Reexam Ordered 04-08-09	
*	DL	90-008,388 Request for Reexam dated 01-16-09	
*	JF	90-008,457 Request for Reexam dated 04-24-09	
	DM	Acom's RISC Leapfrog, Acom User special issue, June 1987; 59: 149-153	

Examiner Signature		Date Considered	7/9/09
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PUBLICATION

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	90/008,237, 90/008,306, & 90/008,474
				Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan. 30, 2007
				First Named Inventor	—
				Art Unit	3992
				Examiner Name	Sam Rimell
Sheet	6	of	28	Attorney Docket Number	0081-011D3X1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	DN	AGRAWAL et al., "Design Considerations for a Bipolar Implementation of SPARC," Compcon Spring apos;88, Thirty-Third IEEE Computer Society International Conference, Digest of Papers, 29 Feb-3 Mar 1988, pp. 6 - 9	
	DO	AGRAWAL, "An 80 MHz Bipolar ECL Implementation of SPARC," Sun Microsystems, Inc., June 25, 1989, 40 pages total.	
	DP	ARM Datasheet, Part No. 1 85250 0360 0, Issue No. 1 (March 17, 1987)	
	DQ	ATMEL SPARC Instruction Set, "Assembly Language Syntax," Rev. 4168C-AERO-08/01, 2002	
	DR	BAGULA, "A 5V Self-Adaptive Microcomputer with 16Kb of #2 Program Storage and Security," IEEE International Solid-State Circuit Conference, 1983, pp. 34-5	
	DS	BAYKO, "Great Microprocessors of the Past and Present (V 11.7.0), downloaded from: << http://web.archive.org/web/20010107210400/http://bwrc.eecs.berkeley.edu/CIC/Archive/cup_history.html >>, Feb 2007, 60 pages total.	
	DT	Books Review: Operating Systems A Systematic View, William S. Davis, Addison-Wesley Publishing Company, Inc., 1987; 26(4):453-454.	
	DU	BOURKE, "Character Synchronization During Overrun Conditions," Delphion, IBM Technical Disclosure Bulletin, Dec 1977	
	DV	Burroughs Corporation, "Burroughs B5500 Information Processing System Reference Manual," 1973.	
	DW	CAL RUN FORTRAN Guide, University of California, Computer Center, Berkeley, 292 pages total. (Sep 1974)	


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		Art Unit	3992		
		Examiner Name	Sam Rimell		
Sheet	7	of	28	Attorney Docket Number	0081-011D3X1

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	DX	Case no. 09-cv-4083, Sirius XM Radio Inc. vs. Technology Properties, Patriot, and Allisconse Ltd., Declaratory Judgment filed 04-24-09	
	DY	Case no. 2:05-cv-00404 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-8 Acorn Processor Invalidity Chart	
	DZ	Case no. 2:05-cv-00404 (TJW) Defendant NEC Electronics America, Inc.'s Preliminary Invalidity Contentions Under Patent Rule 3-3, filed 09/19/05	
	EA	Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-1 GDO S600 Invalidity Chart	
	EB	Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-2 MIPS Invalidity Chart	
	EC	Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-3 SPARC Invalidity Chart	
	ED	Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-4 IBM RT-PC ROMP Invalidity Chart	
	EE	Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-5 Berkeley RISC I and RISC II Invalidity Chart	
	EF	Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-6 Porter Invalidity Chart - USP 3,976,977	
	EG	Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-7 CRAY 1 Invalidity Chart	

Examiner Signature		Date Considered	7/9/09
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		Examiner Name	Sam Rimell		
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*	EH	Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit B: RISC References	
*	EI	Case no. 2:05-cv-494 (TJW) Defendants MEI, PNA, and JVC Preliminary Invalidity Contentions filed 04/18/06 EXHIBIT A - Claim Chart for '148 Patent	
*	EJ	Case no. 2:05-cv-494 (TJW) Defendants MEI, PNA, and JVC Preliminary Invalidity Contentions filed 04/18/06 EXHIBIT B - Claim Chart for '336 Patent	
*	EK	Case no. 2:05-cv-494 (TJW) Defendants MEI, PNA, and JVC Preliminary Invalidity Contentions filed 04/18/06 EXHIBIT C - Claim Chart for '336 Patent	
*	EL	Case no. 5:08-cv-00877 JF Acer and Gateway vs. TPL, Patriot, and Allianceone, Preliminary Invalidity Contentions (Patent L.R. 3-2)	
*	EM	Case No. 5:08-cv-00877 JF Acer Declaration of Harold H. Davis in Support of Plaintiff's Motion to Stay All Proceedings Pending Reexamination of the Patents in Suit, dated 05-01-09	
*	EN	Case No. 5:08-cv-00877 JF Acer Inc. and Acer America Corporation Plaintiff's Motion and Motion to Stay All Proceedings Pending Reexamination of the Patents in Suit, dated 05-01-09	
*	EO	Case No. 5:08-cv-00877 JF Acer Inc. and Acer America Corporation's and Gateway First Amended Complaint for Declaratory Judgment dated 02-09-09	
*	EP	Case No. 5:08-cv-00877 JF Acer Inc. and Acer America Corporation's Responses to Defendant Technology Properties Limited's First Set of Interrogatories, dated 04-03-09	
*	EQ	Case No. 5:08-cv-00877 JF Gateway, Inc.'s Responses to Defendant's Technology Properties Limited's First Set of Interrogatories dated 04-03-09	

Examiner Signature		Date Considered	7/9/09
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		Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan, 30, 2007		
		First Named Inventor	—		
		Art Unit	3992		
		Examiner Name	Sam Rimell		
Sheet	9	of	28	Attorney Docket Number	0081-011D3X1

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*	ER	Case no. 5-08-cv-00882-JF, HTC vs. TPL, Patriot, and Alliacense, First Amended Complaint for Declaratory Judgment filed 07-10-08	
+	ES	Case no. 5-08-cv-00884-JF, AsusTek and Asus vs. TPL, Patriot, MCM, and Alliacense, Second-Amended Complaint filed 09-25-08	
+	ET	Case no. C0805398-JF, Barco's Patent Local Rule 3.3 Invalidity Contentions dated 04-06-2009	
+	EU	Case no. C0905398, BARCO N.V. v. Technology Properties Ltd., Patriot Scientific Corp., and Alliacense Ltd., Complaint for Declaratory Judgment, Demand for Jury Trial, dated 12-01-08	
A	EV	CDC 6000 Computer Systems - COBOL INSTANT 6000, Version 3; Control Data Publication No. 60327600A (Apr 1971)	
d	EW	CDC 6000 Computer Systems, 7600 Computer Systems: FORTRAN Extended Instant 6000 Version 3, 7600 Version 1; Control Publication No. 60305900A (May 1971)	
d	EX	CDC 6000 Computer Systems/ 7600 Computer Systems: FORTRAN Extended Reference Manual, 6000 Version 3, 7600 Version 1; Control Data Publication No. 60329100, Revision D (1972)	
d	EY	CDC 6000 Series Computer System, 6642 Distributive Data Path Operation and Programming Reference Manual; Control Data Publication No. 60376300C (Mar 1979)	
L	EZ	CDC 6000 Series Computer Systems - Chippewa Operating System Documentation, Vol. I, Preliminary Edition (updated May 1966)	
L	FA	CDC 6000 Series Computer Systems - Chippewa Operating System Documentation, Vol. II, Preliminary Edition, Peripheral Packages and Overlays (Oct 1965)	

Examiner Signature	<i>[Signature]</i>	Date Considered	7/9/09
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** NOT A PATENT OR PRINTED PUBLICATION*

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				Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan, 30, 2007
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				Art Unit	3992
				Examiner Name	Sam Rimell
Sheet	10	of	28	Attorney Docket Number	0081-011D3X1

NON PATENT LITERATURE DOCUMENTS			
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<i>d</i>	FB	CDC 6000 Series Computer Systems - Chippewa Operating System Documentation, Vol. III, Preliminary Edition, DSD - The Systems Display, (Nov 1965)	
<i>1</i>	FC	CDC 6000 Series Computer Systems ASCENT General Information Manual; Control Data Publication No. 60135400 (Feb 66)	
<i>d</i>	FD	CDC 6000 Series Computer Systems Chippewa Operating System Reference Manual; Control Data Publication No. 60134400 (Dec 1965)	
<i>d</i>	FE	CDC 6000 Series Computer Systems Hardware Reference Manual; Control Data Publication No. 60100000 (Aug 1978)	
<i>1</i>	FF	CDC 6000 Series Computer Systems/ 7600 Computer System: 6000 Compass Version 2, 7600 Versions 1 & 2 Reference Manual; Control Data Publication No. 60279900, Revision D, (1970, 1971, 1972)	
<i>L</i>	FG	CDC 6000 Series Computer Systems: Chippewa Operating System FORTRAN Reference Manual; Control Data Publication No. 60132700A (May 1966)	
<i>d</i>	FH	CDC 6000 Series Computer Systems: Peripheral Equipment Reference Manual; Control Data Publication No. 60156100, Revision J (Mar 1970)	
<i>1</i>	FI	CDC 6000 Series Computer Systems: Site Preparation and Installation Manual; Control Data Publication No. 60142400, Revision B (Sep 1965)	
<i>1</i>	FJ	CDC 6000 Series Computer Systems: FORTRAN Extended General Information, Control Data Publication No. 60176400 (Oct 1966)	
<i>1</i>	FK	CDC 6000 Series FORTRAN Extended 4.0, Internal Maintenance Specifications, (1971)	

Examiner Signature	<i>Sam Rimell</i>	Date Considered	<i>7/9/09</i>
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		First Named Inventor	—		
		Art Unit	3992		
		Examiner Name	Sam Rimell		
Sheet	11	of	28	Attorney Docket Number	0081-011D3X1

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SL	FL	CDC 6000 Series Introduction and Peripheral Processors Training Manual, Second Edition; Control Data Publication No. 60250400 (Nov 1968)	
SL	FM	CDC 6400 Central Processor; Control Data Publication No. 60257200 (Feb 1967)	
SL	FN	CDC 6400/6500/6600 ASCENT-TO-COMPASS TRANSLATOR; Control Data Publication No. 60191000 (Mar 1967)	
SL	FO	CDC 6400/6500/6600 Computer System Input/Output Specification; Control Data Publication No. 60045100 (September 1967)	
SL	FP	CDC 6400/6500/6600 Computer System Instant SMM; Control Data Publication No. 60299500 (Nov 1969)	
SL	FQ	CDC 6400/6500/6600 Computer Systems COMPASS Reference Manual; Data 60190900, Revision B (Mar 1969)	
SL	FR	CDC 6400/6500/6600 Computer Systems Reference Manual; Control Data Publication No. 60100000, Revision K (Aug 1970)	
SL	FS	CDC 6400/6500/6600 Extended Core Storage Systems Reference Manual; Control Data Publication No. 60225100, (Feb 1968)	
SL	FT	CDC 6400/6500/6600 Jovial General Information Manual; Control Data Publication No. 60252100A (Mar 1969)	
SL	FU	CDC 6400/6600 Computer Systems: ASCENT/ASPER Reference Manual; Control Data Publication No. 60172700 (Jul 1966)	

Examiner Signature		Date Considered	7/21/09
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		Art Unit	3992		
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Sheet	12	of	28	Attorney Docket Number	0081-011D3X1

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<i>dl</i>	FV	CDC 6400/6600 FORTAN Conversion Guide; Data Publication No. 60175500 (Aug 1966)	
<i>dl</i>	FW	CDC 6400/6600 Systems Bulletin (10 Oct 1966), 84 pages	
<i>dl</i>	FX	CDC 6400/6600, Export/Import 8231 Reference Manual; Data Publication No. 60189100 (April 1967)	
<i>dl</i>	FY	CDC 6600 Central Processor Vol 1; Control & Memory; Data Control Publication No. 020167 (March 1967)	
<i>dl</i>	FZ	CDC 6600 Central Processor, Vol. 2, Functional Units; Control Data Publication No. 60239700 (Mar 1967)	
<i>dl</i>	GA	CDC 6600 CHASSIS TABS; Control Data Publication No. 63016700A (Apr 1965)	
<i>dl</i>	GB	CDC 6600 CHASSIS TABS; Control Data Publication No. 63019800 (Mar 1965)	
<i>dl</i>	GC	CDC 6600 Chippewa Operating System; Control Data Publication No. 60124500, Revision C (April 1965)	
<i>dl</i>	GD	CDC 6600 Computer System 6601 A-J, 6613A/B/C, 6604A/B/C, 6614-A/B/C Central Processor (Including Functional Units) Vol. 1, Diagrams & Circuit Description; Control Data Publication No. 60119300BT (Jan 1968)	
<i>dl</i>	GE	CDC 6600 Computer System 6601 A-J, 6613A/B/C, 6604A/B/C, 6614-A/B/C Peripheral and Control Processor/Central Memory/Clock/Extended Core Storage Coupler (Std Opt 10102 and/or Spec Opt 60080) Power Wiring, Vol. 2, Diagrams & Circuit Descriptions; Control Data Publication No. 60119300BT (Jan 1968)	

Examiner Signature	<i>Sam Rimell</i>	Date Considered	7/9/09
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	GF	CDC 6600 Computer System Operating System/Reference Manual, SIPROS66, 1st ed.; Control Data Publication No. 60101800A (1965)	
	GG	CDC 6600 Computer System Programming System/Reference Manual, Vol. 1. ASCENT; Control Data Publication No. 60101600B (1965)	
	GH	CDC 6600 Computer System Programming System/Reference Manual, Vol. 2, ASPER; Control Data Publication No. 60101700B (1965)	
	GI	CDC 6600 Computer System Programming Vol. 3, FORTRAN 66; Control Data Publication No. 60101500B (1965)	
	GJ	CDC 6600 Computer Training Manual Vol. 2, Preliminary Edition, Section 7.2 Shift Functional Units, 164 pages	
	GK	CDC 6600 Data Channel Equipment 6602-B/6612-A, 6603-B, 6622-A, 6681-B, 6682-A/6683-A, S.O. 60022, 60028, 60029, Diagrams & Circuit Description; Control Data Publication No. 60125000, Revision G (June 1966)	
	GL	CDC 6600 Training Manual; Control Data Publication No. 60147400, Revision A (June 1965)	
	GM	CDC 6603 - A/B/C Disk File Controller Reference Manual; Control Data Publication No. 60334000 (1970)	
	GN	CDC 6638 Disk File Subsystem Training Supplement; Control Data Publication 602500800A (Oct 1968)	
	GO	CDC 6638 Disk File System: Standard Option 10037-A, 6639-A/B File Controller -- Diagrams and Circuit Description/Maintenance/Maintenance Aids/Parts List/ Wire Lists/Chassis Tabs; Control Data No. 60227300, Revision H (Mar 1974)	

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<i>A</i>	GP	CDC 6839 - A/B Disk File Controller Reference Manual; Control Data Publication No. 60334100E (Aug 1973)	
<i>A</i>	GQ	CDC 6639 Disk Controller Training Manual Test Edition (Sep 1967), 28 pages.	
<i>A</i>	GR	CDC APL Version 2 Reference Manual, CDC Operating Systems : NOS; Control Data Publication NO. 60454000F (Nov 1980)	
<i>A</i>	GS	CDC Basic Version 3 Reference Manual: NOS 1 & NOS/BE 1; Control Data Publication No. 19983900G (Oct 1980)	
<i>A</i>	GT	CDC Chippewa Operating System, Document Class ERS, System No. E012, Version 1.1; External Reference Specifications - Chippewa Operating System, (Jun 1966)	
<i>A</i>	GU	CDC Chippewa Operating System, Document Class SIR, System No. E012, Version 1.0, (March 3, 1966)	
<i>A</i>	GV	CDC Chippewa Operating System, Document Class SIR, System No. E012, Version 1.1, (March 3, 1966)	
<i>A</i>	GW	CDC COBOL Version 4 Instant Manual, Cyber 170 Series, Cyber 70 Models 72, 73, 74, 6000 Series; Control Data Publication No. 60497000A (Feb 1976)	
<i>A</i>	GX	CDC COBOL Version 5 Instant Manual, Operating Systems: NOS 1/BE 1; Control Data Publication No. 60497300B (Feb 198)	
<i>A</i>	GY	CDC CODES/Control Data 6400/6500/6600 Computer Systems; Control Data Publication No. 60141900, Revision C (1966, 1967)	

Examiner Signature	<i>[Signature]</i>	Date Considered	7/14/09
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<i>d</i>	GZ	CDC CODES/Control Data 6400/6500/6600/6700 Computer Systems; Control Data Publication No. 60141900, Revision D (1966, 1967)	
<i>d</i>	HA	CDC CODES/Control Data 6600; Control Data Publication No. 60141900, Revision A (May 1965)	
<i>d</i>	HB	CDC COMPASS Version3 Instant, Operating Systems: NOS 1, NOS 2, NOS/ BE 1, SCOPE 2; Control Data Publication No. 60492800D (Jun 1982)	
<i>d</i>	HC	CDC Course No. FH4010-1C, NOS Analysis, Student Handout, Revision C (Apr 1980)	
<i>d</i>	HD	CDC Course No. FH4010-4C NOS Analysis, Study Dump (Apr 1980)	
<i>d</i>	HE	CDC Cyber 170 Models 720, 730, 740, 750 and 760 Model 176 (Level B/C) Computer Systems, Codes; Control Data Publication No. 60456920C, (Jun 1981)	
<i>d</i>	HF	CDC Cyber 70 Computer Systems Models 72, 73, 74, 6000 Computer Systems: FORTRAN Reference Manual Models 72, 73, 74 Version 2.3, 6000 Version 2.3; Control Data Publication No. 19980400, Revision F (July 1972)	
<i>d</i>	HG	CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems - ALGOL Reference Manual, Cyber 70 Series Version 4, 6000 Series Version 4, 7600 Series Version 4; Control Data Publication No. 60384700A (Aug 1973)	
<i>d</i>	HH	CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems: COBOL INSTANT Models 72, 73, 74 Version 4, Model 76 Version 1, 6000 Version 4; Control Data Publication No. 60328400A (Dec 1971)	
<i>d</i>	HI	CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems: FORTRAN Extended Instant Models 72, 73, 74 Version 4, Model 76 Version 2, 7600 Version 2, 6000 Version 4; Control Data Publication No. 60357900A (Nov 1971)	

Examiner Signature	<i>Sam Rimell</i>	Date Considered	7/10/08
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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known			
		Application Number	90/008,237, 90/008,306, & 90/008,474		
		Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan, 30, 2007		
		First Named Inventor	—		
		Art Unit	3992		
		Examiner Name	Sam Rimell		
Sheet	16	of	28	Attorney Docket Number	0081-011D3X1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	HJ	CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems: FORTRAN Extended Reference Manual Models 72, 73, 74 Version 4, Model 76 Version 2, 6000 Version 4; Control Data Publication No. 60305600A (Oct 1971)	
	HK	CDC Cyber 70 Series 6000 Series Computer Systems: APL*Cyber Reference Manual; Control Data Publication No. 19980400B (July 1973)	
	HL	CDC Cyber 70 Series Computer Systems 72, 73, 74, 6000 Series Computer Systems – Kornos 2.1 Workshop Reference Manual; Control Data Publication No. 97404700D (1976)	
	HM	CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, KRONO 2.1 Operator Guide; Control Data Guide; Control Data Publication 60407700A (Jun 1973)	
	HN	CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, KRONOS 2.1 Installation Handbook; Control Data Publication no. 60407500A (Jun 1973)	
	HO	CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, KRONOS 2.1 Time-Sharing User's Reference Manual; Control Data Publication No. 60407600B (May 1974)	
	HP	CDC Cyber 70/ Model 76 Computer System, 7600 Computer System: FORTRAN Run, Version 2 Reference Manual; Control Data 60360700C (May 1974)	
	HQ	CDC Cyber Interactive Debug Version 1 Guide for Users of FORTRAN Extended Version 4, CDC Operating Systems: NOS 1, NOS/ BE 1, Control Data Publication No. 60482700A (Feb 1979)	
	HR	CDC Cyber Interactive Debug Version 1 Guide for Users of FORTRAN Version 5, Operating Systems: NOS 1, NOS/ BE 1; Control Data Publication No. 60484100C (Sep 1984)	
	HS	CDC Cyber Interactive Debug Version 1 Reference Manual, NOS 1, NOS 2, NOS/ BE 1; Data Control Publication NO. 60481400D (Jun 1984)	

Examiner Signature		Date Considered	7/13/09
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		Application Number	90/008,237, 90/008,306, & 90/008,474		
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		First Named Inventor	—		
		Art Unit	3992		
		Examiner Name	Sam Rimell		
Sheet	17	of	28	Attorney Docket Number	0081-011D3X1

NON PATENT LITERATURE DOCUMENTS			
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<i>d</i>	HT	CDC Cyber Loader Version 1 Instant, CDC Operating System NOS1, NOS/ BE 1; Control Data Publication No. 60449800C (Aug 1979)	
<i>d</i>	HU	CDC Disk Storage Subsystem — Operation and Programming Manual; Control Data Publication No. 60383900, Version T (1972-1980)	
<i>d</i>	HV	CDC FORTRAN Extended 2.0, Document Class ERS, System No. C012, (Dec 1966)	
<i>d</i>	HW	CDC FORTRAN Extended 2.0, Document Class IMS, Internal Maintenance Specifications - 64/65/6600 V FORTRAN Extended Version 2 (Mar 1969)	
<i>d</i>	HX	CDC FORTRAN Extended Version 4 Instant Manual, Operating Systems: NOS 1, NOS/BE 1, SCOPE 2; Control Data Publication No. 60497900B (Jun 1981)	
<i>d</i>	HY	CDC FORTRAN Extended, Sales Technical Memorandum (May 1967)	
<i>d</i>	HZ	CDC FORTRAN Version 5 Instant, CDC Operating Systems: NOS 1, NOS/ BE 1, SCOPE 2; Control Data Publication No. 60483900A (Jan 1981)	
<i>d</i>	IA	CDC GED FORTRAN Extended 1.0, Product No. C012, Dept No. 254, Project No. 4P63FTN (Aug 1967)	
<i>d</i>	IB	CDC INSTANT 6400/3500/6500 SIMULA; Control Data Publication No. 60235100, Revision A (Feb 1969)	
<i>d</i>	IC	CDC INSTANT 6400/6500/6600 COMPASS; Control Data Publication No. 60191900, Revision A (1968)	

Examiner Signature	<i>Sam Rimell</i>	Date Considered	7/13/09
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan, 30, 2007
		First Named Inventor	—
		Art Unit	3992
		Examiner Name	Sam Rimell
(Use as many sheets as necessary)		Attorney Docket Number	0081-011D3X1
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sl	ID	CDC INSTANT FORTRAN 2.3 (6000 Series); Data Publication No. 60189500D (May 1969)	
sl	IE	CDC Internal Maintenance Specification: FORTRAN V5, ; Control Data Publication No. 77987506A	
sl	IF	CDC Internal Maintenance Specification: FORTRAN V5, ; Control Data Publication No. 77987506A	
sl	IG	CDC KRONOS 2.1 Reference Manual Volume 1 of 2; Control Data Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems; Control Data Publication No. 60407000D (Jun 1975)	
sl	IH	CDC KRONOS 2.1 Time-Sharing User's Reference Manual, Cyber 70 Series Models 72, 73, 74, 6000 Series Computer Systems; Control Data Publication No. 60407600D (Jun 1975)	
sl	II	CDC Model dd 60A Computer Control Console/Customer Engineering Manual; Control Data Publication No. 82100010 (Mar 1965)	
sl	IJ	CDC Model dd60b Computer Control Console/Customer Engineering Manual; Control Data Publication No. 82103500 (Feb 1967)	
sl	IK	CDC Network Products: Network Access Method Version 1, Network Definition Language Reference Manual; Control Data Publication No. 60480000J (May 1981)	
sl	IL	CDC Network Products: Network Terminal User's Instant - Operating System NOS 1; Control Data Publication No. 60455270C, (Oct 1980)	
sl	IM	CDC NOS 2 Operations Handbook; Control Data Publication No. 60459310, (Aug 1994)	

Examiner Signature		Date Considered	7/13/09
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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
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				First Named Inventor	---
				Art Unit	3992
				Examiner Name	Sam Rimell
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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	IN	CDC NOS Version 1 Applications Programmer's Instant, CDC Computer Systems: Cyber 170 Series, Cyber 70 Models 71, 72, 73 74, 6000 Series; Control Data Publication No. 60436000H (Jan 1980)	
	IO	CDC NOS Version 1 Internal Maintenance Specification Volume 1 of 3; Control Data Publication No. 60454300B (Aug 1979)	
	IP	CDC NOS Version 1 Internal Maintenance Specification Volume 2 of 3; Control Data Publication No. 60454300B (Aug 1979)	
	IQ	CDC NOS Version 1 Internal Maintenance Specification Volume 3 of 3; Control Data Publication No. 60454300B (Aug 1979)	
	IR	CDC NOS Version 1 Operator's Guide, CDC Computer Systems: Cyber 170 Series, Cyber 70 Model 71, 72, 73 74, 6000 Series (Dec 1980)	
	IS	CDC NOS Version 1 Reference Manual Volume 1 of 2, CDC Computer Systems: Cyber 170 Series, Cyber 70 Models 71, 72, 73, 74, 6000 Series; Control Data Publication No. 60435400J (1979)	
	IT	CDC NOS Version 1 Reference Manual Volume 2 of 2, CDC Computer Systems: Cyber 170 Series, Cyber 70 Models 71, 72, 73, 74, 6000 Series; Control Data Publication No. 60445300E (1977)	
	IU	CDC NOS Version 1 System Maintenance Reference Manual; Control Data Publication No. 60455380H (Apr 1981)	
	IV	CDC NOS Version 2 Analysis Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60459300D (Oct 84)	
	IW	CDC NOS Version 2 Analysis Handbook; Control Data Publication No. 60459300U (Jul 1994)	

Examiner Signature		Date Considered	7/13/09
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Substitute for form 144B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
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				Art Unit	3992
				Examiner Name	Sam Rimell
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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
<i>SI</i>	IX	CDC NOS Version 2 Installation Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60459320E_ (Mar 1985)	
<i>SI</i>	IY	CDC NOS Version 2 Operation/Analysis Handbook, Cyber 170, Cyber 70 Models 71, 72, 73, 74 6000, Control Data Publication No. 60459310C (Oct 1983)	
<i>LI</i>	IZ	CDC NOS Version 2 System Maintenance Reference Manual, Cyber 170, Cyber 70 Models 71, 72, 73 74, 6000; Control Data Publication No. 60459300C (Oct 1983)	
<i>SI</i>	JA	CDC NOS/BE Version 1 Diagnostic Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60494400-V (1986)	
<i>LI</i>	JB	CDC NOS/BE Version 1 Installation Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60494300AB (Dec 1986)	
<i>LI</i>	JC	CDC NOS/BE Version 1 Reference Manual, Cyber 170 Series, Cyber 70 Models 71, 72, 73, 74, 6000 Series; Control Data Publication No. 60493800M 1981	
<i>LI</i>	JD	CDC Outline of Reports on "Feasibility Study of 64/6600 FORTRAN Ver 3.0 and Conversational FORTRAN, FORTRAN Study Project, Product No. X010, Dept No. 254, Project No. 4P63, (Jun 1966)	
<i>LI</i>	JE	CDC Pascal Version 1 Reference Manual, Operating Systems: NOS 2; Control Data Publication No. 60497700 (Sep 1983)	
<i>LI</i>	JF	CDC Pascal Version 1 Reference Manual, Operating Systems: NOS 2; Control Data Publication No. 60497700A (Dec 1982)	
<i>EL</i>	JG	CDC PL/1 Version 1 Instant, CDC Operating Systems: NOS 1, NOS/ BE 1; Control Data Publication No. 60483700A (Nov 1979)	

Examiner Signature	<i>[Signature]</i>	Date Considered	7/13/08
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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
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				Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan, 30, 2007
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				Art Unit	3992
				Examiner Name	Sam Rimell
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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
<i>dl</i>	JH	CDC SIMSCRIPT 11.5 Instant, Control Data Publication No. 84000450B (Sep 1978)	
<i>dl</i>	JL	CDC Sort/Merge Version 4 and 1 Instant, Operating Systems: NOS 1, NOS/BE 1, SCOPE 2; Control Data Publication No. 60497600C (Jan 1981)	
<i>dl</i>	JJ	CDC Sort/Merge Vision 5 Reference Manual, Operating Systems: NOS 2, NOS/BE 1; Control Data Publication No. 60484800C (Feb 1984)	
<i>dl</i>	JK	CDC SYMPL Version 1 Instant, NOS 1, NOS/BE 1, SCOPE 2; Control Data Publication NO. 60482600A (May 1978)	
<i>dl</i>	JL	CDC SYMPL Version 1 Users Guide, Operating Systems: NOS 1, NOS/BE 1, SCOPE 2; Control Data Publication No. 60499800B (Apr 1978)	
<i>dl</i>	JM	CDC Update Instant, Cyber 170 Series, Cyber 70 Series, 6000 Series, 7600 Computer Systems; Control Data Publication No. 60450000A (Nov 75)	
<i>dl</i>	JN	CDC Update Reference Manual Operating Systems: SCOPE 3.4, KRONOS 2.1; Control Data Publication No. 60342500, Revision H (1971 - 1976)	
<i>dl</i>	JO	CDC XEDIT Version 3 Reference Manual, Operating System: NOS 1; Control Data Publication No. 60455730B (Aug 1979)	
<i>dl</i>	JP	Chippewa Laboratories FORTRAN Compiler Run, Preliminary Edition, CDC 6000 Series Computer Systems, (Apr 1966)	
<i>dl</i>	JQ	CHO et al., WAM 3.6: A 40K Cache Memory and Memory Management Unit, ISSCC '86, Feb 19, 1986.	

Examiner Signature	<i>Sam Rimell</i>	Date Considered	7/14/09
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		Examiner Name	Sam Rimell		
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NON PATENT LITERATURE DOCUMENTS			
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<i>sl</i>	JR	CORDELL, II et al., "Advanced Interactive Executive Program Development Environment," IBM Systems Journal, 1987; 26(4):361-382	
<i>sl</i>	JS	CRAWFORD, "The i486 Executing Instructions in One Clock Cycle," IEEE Micro, pp. 28 - 36 (Feb 1990)	
<i>sl</i>	JT	Disk Routines and Overlays, Chippewa Operating System, CDC Development Division - Applications, (Nov 1965)	
<i>sl</i>	JU	DOWSING et al., "Computer Architecture: A First Course, Chapter 6: Architecture and the Designer," Van Nostrand Reinhold (UK) Co. Ltd., pp. 126-139.	
<i>sl</i>	JV	EVANS et al., "An Experimental 512-bit Nonvolatile Memory with Ferroelectric Storage Cell," IEEE Journal of Solid-State Circuits, 23(5):1171-1175.	
<i>sl</i>	JW	Field Maintenance Print Set, KA780-01-01 Rev. A.	
<i>sl</i>	JX	FISHER et al., "Very Long Instruction Word Architectures and the ELI-512," ACM pp. 140-150 (1983)	
<i>sl</i>	JY	FURBER, VLSI RISC Architecture and Organization, Chapter 3: Commercial VLSI RISC, pp. 124 - 129, Marcel Dekker, Inc., 1989	
<i>sl</i>	KA	GB Patent Application 8233733, INMOS, Ltd. Microcomputer, filed 11-26-1982	
<i>sl</i>	KB	GE 600 Series, publication	

Examiner Signature	<i>sl</i>	Date Considered	2/4/09
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<i>sl</i>	KC	GERSHON, Preface, IBM Systems Journal 26(4):324-325	
<i>sl</i>	KD	GREEN et al., "A Perspective on Advanced Peer-to-Peer Networking," IBM Systems Journal, 1987; 26(4):414-428.	
<i>sl</i>	KE	GRIMES et al., "64 bit Processor, The Intel i860 64-Bit Processor: A General-Purpose CPU with 3D Graphics Capabilities", published by Intel, p. 85 (July 1989)	
<i>sl</i>	KF	HANSEN, "A RISC Microprocessor with Integral MMU and Cache Interface," ICCD '86, pp. 145 - 148, 1986	
<i>sl</i>	KG	HENNESSY et al., "Hardware/software Tradeoff for Increased Performance," Technical Report No. 22.8, Computer Systems Laboratory, Feb 1983, 24 pages	
<i>sl</i>	KH	HENNESSY et al., "The MIPS Machine", COMPCON, IEEE, Spring 1982, pp. 2-7.	
<i>sl</i>	KI	HENNESSY, "Performance Issues in VLSI Processor Design," IEEE on VLSI in Computers, , pp. 153 - 156. (1983)	
<i>sl</i>	KJ	HINTON, "80960 -- Next Generation," COMPCON Spring 89, IEEE, 13-16 (1989)	
<i>sl</i>	KK	HOLLINGSWORTH et al., "The Fairchild Clipper: Instruction Set Architecture and Processor Implementation," Report No. UCB/CSD 87/329, Computer Science Division (EECS), University of California Berkeley, California, (February 11, 1987)	
<i>sl</i>	KL	HP 9000 Instrument Controllers, Technical Specifications Guide, October, 1989.pdf	

Examiner Signature	<i>[Signature]</i>	Date Considered	7/14/09
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al	KM	HP 9000 Series Computer Systems, HP-UX Reference 09000-090004, Preliminary November, 1982	
al	KN	HUGHES, "Off-Chip Module Clock Controller," Delphion, IBM Technical Disclosure Bulletin, Sep 1989	
al	KO	HUNTER, "Introduction to the Clipper Architecture," IEEE Micro, pp. 6-26 (August 1987)	
al	KP	IBM RT PC, BYTE 1986 Extra Edition, Inside The IBM PCs, pp. 60-78	
al	KQ	INMOS Limited, IMS T424 Transputer Reference Manual, 1984	
al	KR	Intel 386TM DX Microprocessor 32-Bit CMOS Microprocessor With Integrated Memory Management (1995)	
al	KS	Intel 80960CA User's Manual published by Intel (1989)	
al	KT	Intel Architecture Optimization Manual, Order Number 242816-003, published by Intel (1997)	
al	KU	Intel Architecture Software Developer's Manual, Volume 1: Basic Architecture, published by Intel (1997)	
al	KV	Intel 8080A/8080A-1/8080A-2, 8-Bit N-Channel Microprocessor, Order Number: 231453-001, Its Respective Manufacturer (Nov 1986)	

Examiner Signature		Date Considered	2/14/09
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<i>A</i>	KW	JOHNSON et al., "A Variable Delay Line PLL for CPU-Coprocessor Synchronization," IEEE Journal of Solid-State Circuits, 23(5): 1218-1223, October 1988	
<i>A</i>	KX	KATEVENIS et al., "Reduced Instruction Set Computer Architecture for VLSI," Doctoral Dissertation, Oct 1983	
<i>A</i>	KY	KATEVENIS et al., "The RISC II Micro-Architecture," Journal of VLSI and Computer Systems, 1(2):138-152 (1984)	
<i>A</i>	KZ	KIPP, "Micron Technology Inc. Reports Financial Results," Business Wire, New York, Sep 26, 1988	
<i>A</i>	LA	KOHN et al., "Introducing INTEL 860 64-Bit Microprocessor," Intel Corporation, IEEE Micro (August 1989)	
<i>A</i>	LB	KOOPMAN, "RTX 4000," Proceedings of 1989 Rochester Forth Conference, pp. 84-85.	
<i>A</i>	LC	KOOPMAN, "The WISC Concept: A proposal for a writable instruction set computer," BYTE, pp. 187-193. (April 1987)	
<i>A</i>	LD	KOOPMAN, Jr. et al. "MVP Microcoded CPU/16 Architecture," Proceedings of 1986 Rochester Forth Conference, pp. 277-280.	
<i>A</i>	LE	KOOPMAN, Jr. et al., "WISC Technologies, Inc., Writable Instruction Set, Stack Oriented Computers: The WISC Concept," 1987 Rochester Forth Conference, Journal of Forth Application and Research, 5(1):49-71.	
<i>A</i>	LF	KOOPMAN, Jr., Slack Computers: the new wave, 1989	

Examiner Signature	<i>Sam Rimell</i>	Date Considered	2/14/09
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Sheet	26	of	28	Attorney Docket Number	0081-011D3X1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
AL	LG	LOUCKS et al., "Advanced Interactive Executive (AIX) Operating System Overview," IBM Systems Journal, 1987; 28(4):326-345	
AL	LH	MATICK, "Self-Clocked Cache," Delphion, IBM Technical Disclosure Bulletin, Apr 1985	
AL	LI	MILLER, "Frequency Modulated Ring Oscillator for a Mode Regulated Substrate Bias Generator, Delphion, IBM Technical Disclosure Bulletin, Sep 1989	
AL	LJ	MILLS et al., "Box Structured Information Systems," IBM Systems Journal, 1987; 26(4):395-413	
AL	LK	MMP Portfolio, News Release: Roland Becomes 50th Licensee, Setting a Major Milestone in Moore Microprocessor Patent Licensing Program," 3 pages (May 1, 2009)	
AL	LL	MOUSSOURIS et al., "A CMOS RISC Processor Integrated System Functions," Proceedings of 31st IEEE Computer Society International Conference, Cathedral Hill Hotel, San Francisco, CA March 3-6, 1986, pp. 126 - 131, 1986.	
AL	LM	OLSON, "Semiconductor Die with Wiring Skirt (Packaging Structure), Delphion, IBM Technical Disclosure Bulletin, July 1978.	
AL	LN	O'Neil, "Pipeline Memory System for Drams", Delphion, IBM Technical Disclosure Bulletin, May 1989.	
	LO	Parent Continuity Data for 07/280,324 downloaded from PAIR	
AL	LP	PATTERSON et al., "RISC I: A Reduced Instruction Set VLSI Computer," Proceedings of the 8th annual symposium on Computer Architecture on Computer Architecture, Minneapolis, Minnesota, pp. 443 - 457 (May 1981)	

Examiner Signature	<i>[Signature]</i>	Date Considered	7/14/09
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

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	90/008,237, 90/008,306, & 90/008,474
				Filing Date	Nov. 17, 2006, Oct. 19, 2006, & Jan, 30, 2007
				First Named Inventor	---
				Art Unit	3992
				Examiner Name	Sam Rimell
Sheet	27	of	28	Attorney Docket Number	0081-011D3X1

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<i>SL</i>	LQ	POUNTAIN, "The Archimedeas A310," BYTE, 1987	
<i>SL</i>	LR	PRZYBYISKI et al., "Organization and VLSI Implementation of MIPS," Technical Report: CSL-TR-84-259, Apr 1984	
<i>SL</i>	LS	PRZYBYISKI, "The Design Verification and Testing of MIPS", 1984 Conference on Advanced Research in VLSI, pp. 100 - 109.	
<i>SL</i>	LT	ROCHE et al., "Method of Assuring a Two-Cycle Start, Zero Cycle Stop, Non-Chopping on Chip Clock Control Throughout a VLSI Clock System," Delphion, IBM Technical Disclosure Bulletin, Sep 1989	
<i>SL</i>	LU	ROWEN et al., "A Pipelined 32b NMOS Microprocessors and Microcontrollers," IEEE International Solida-State Circuits Conference, pp. 180 -181, 1984.	
<i>SL</i>	LV	RUBINFELD et al., "The CVAX CPU, A CMOS VAX Microprocessor Chip", International Conference on Computer Design, October, 1987.	
<i>SL</i>	LW	SANAMRAD et al., "A Hardware Syntactic Analysis Processor," IEEE, August 1987, pp. 73-80	
<i>SL</i>	LX	SHIH, "Microprogramming Heritage of RISC Design," Proceedings of the 23rd annual workshop and symposium on Microprogramming and microarchitecture, pp. 275-280. (1990)	
<i>SL</i>	LY	SULTAN et al., "Implementing System-36 Advanced Peer-to-Peer Networking," IBM Systems Journal, 1987; 26(4):429-452.	
<i>SL</i>	LZ	THORNTON, J. E., "Considerations in Computer Design Leading Up To the Control Data 6600," Control Data Chippewa Laboratory (1970).	

Examiner Signature	<i>Sam Rimell</i>	Date Considered	7/15/09
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	MA	VAX 11/780 Architecture Handbook Vol. 1, 1977-1978, 2-7 and G-8	
	MB	VAX 8800 System Technical Description Vol. 2, EK-KA88I-TD-PRE, Section 6, Instruction Box (IBOX), Preliminary Edition (July 1986)	
	MC	VAX Maintenance Handbook: VAX-11/780, EK-VAXV2-HB-002, 1983 Edition	
	MD	VL86C010 RISC Family Data Manual, Application Specific Logic Product Division, 1987	
	ME	WATERS et al., "AIX Usability Enhancements and Human Factors," IBM Systems Journal, 1987; 26(4):383-394.	
	MF	WILLIAMS, "Chip Set Tackles Laptop Design Issues, Offers Flat-Panel VGA Control," Computer Design, October 15, 1988; 27(19):21-22	

Examiner Signature		Date Considered	7/12/09
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