PTO/SB/57 (04-05)
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71338 U.S. PTO 900008306 10/19/06

(Also referred to as FORM PTO-1465)

REQUEST FOR *EX PARTE* REEXAMINATION TRANSMITTAL FORM

Address to:
Mail Stop *Ex Parte* Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attorney Docket No.: 076885.0102

Date: 10-19-06

1. [X] This is a request for *ex parte* reexamination pursuant to 37 CFR 1.510 of patent number 5,809,336 issued September 15, 1998. The request is made by:

   [ ] patent owner. [X] third party requester.

2. [X] The name and address of the person requesting reexamination is:

   Michael Hawes on Behalf of Toshiba Corporation

   Baker Botts L.L.P.

   910 Louisiana, Houston, TX 77002

3. [ ] a. A check in the amount of $_____ is enclosed to cover the reexamination fee, 37 CFR 1.20(c)(1);

   [X] b. The Director is hereby authorized to charge the fee as set forth in 37 CFR 1.20(c)(1) to Deposit Account No. 02-0383 (submit duplicative copy for fee processing); or

   [ ] c. Payment by credit card. Form PTO-2038 is attached.

4. [ ] Any refund should be made by [ ] check or [X] credit to Deposit Account No. 02-0383. 37 CFR 1.26(c). If payment is made by credit card, refund must be to credit card account.

5. [X] A copy of the patent to be reexamined having a double column format on one side of a separate paper is enclosed. 37 CFR 1.510(b)(4)

6. [ ] CD-ROM or CD-R in duplicate, Computer Program (Appendix) or large table
   [ ] Landscape Table on CD

7. [ ] Nucleotide and/or Amino Acid Sequence Submission
   If applicable, items a. – c. are required.

   a. [ ] Computer Readable Form (CRF)
   b. Specification Sequence Listing on:

      i. [ ] CD-ROM (2 copies) or CD-R (2 copies); **or**
      ii. [ ] paper

   c. [ ] Statements verifying identity of above copies

8. [ ] A copy of any disclaimer, certificate of correction or reexamination certificate issued in the patent is included.

9. [X] Reexamination of claim(s) 1-10 is requested.

10. [X] A copy of every patent or printed publication relied upon is submitted herewith including a listing thereof on Form PTO/SB/08, PTO-1449, or equivalent.

11. [X] An English language translation of all necessary and pertinent non-English language patents and/or printed publications is included.

10/31/2006 JMCDOUGA 00000001 020383 90008306
01 FC:1812 2520.00 DA

12. [X] The attached detailed request includes at least the following items:

a. A statement identifying each substantial new question of patentability based on prior patents and printed publications. 37 CFR 1.510(b)(1)
b. An identification of every claim for which reexamination is requested, and a detailed explanation of the pertinency and manner of applying the cited art to every claim for which reexamination is requested. 37 CFR 1.510(b)(2)

13. [ ] A proposed amendment is included (only where the patent owner is the requester). 37 CFR 1.510(e)

14. [X] a. It is certified that a copy of this request (if filed by other than the patent owner) has been served in its entirety on the patent owner as provided in 37 CFR 1.33(c).
The name and address of the party served and the date of service are:

Mr. Drew S. Hamilton

Knobbe, Martens, Olson & Bear, LLP

550 W C St. Suite 120, San Diego, CA 92101

Date of Service: October 19, 2006; or

[ ] b. A duplicate copy is enclosed since service on patent owner was not possible.

15. Correspondence Address: Direct all communication about the reexamination to:

[ ] The address associated with Customer Number:

OR

[X] Firm or Individual Name Michael Hawes

Address
Baker Botts L.L.P.
910 Louisiana

City	State	Zip
Houston	TX	77002

Country U.S.

Telephone	Email
713.229.1234	michael.hawes@bakerbotts.com

16. [X] The patent is currently the subject of the following concurrent proceeding(s):
[ ] a. Copending reissue Application No. _____
[X] b. Copending reexamination Control No. 90/008,237
[ ] c. Copending Interference No. _____
[X] d. Copending litigation styled:

Technology Properties Limited, Inc. v. Fujitsu Limited et al., Case No. 2:05-cv-00494-TWJ,

Federal District Court for the Eastern District of Texas, Marshall Division

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

Authorized Signature — Date: 10-19-2006

Michael Hawes — Typed/Printed Name; 38,487 — Registration No.

[ ] For Patent Owner Requester
[X] For Third Party Requester

PTO/SB/57 (04-05)
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a. A statement identifying each substantial new question of patentability based on prior patents and printed publications. 37 CFR 1.510(b)(1)
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Address

Baker Botts L.L.P.
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Houston	TX	77002

Country U.S.

Telephone	Email
713.229.1234	michael.hawes@bakerbotts.com

16. [X] The patent is currently the subject of the following concurrent proceeding(s):

[ ] a. Copending reissue Application No. _____
[X] b. Copending reexamination Control No. 90/008,237
[ ] c. Copending Interference No. _____
[X] d. Copending litigation styled:

Technology Properties Limited, Inc. v. Fujitsu Limited et al., Case No. 2:05-cv-00494-TWJ,

Federal District Court for the Eastern District of Texas, Marshall Division

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Authorized Signature

10-19-2006
Date

Michael Hawes
Typed/Printed Name

38,487
Registration No.

[ ] For Patent Owner Requester
[X] For Third Party Requester

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

U.S. Patent No. :	5,809,336
Serial No.:	484,918
Filing Date:	June 7, 1995
Patentees:	Charles H. Moore, Russell H. Fish III
Issued:	September 15, 1998
Title:	HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

Mail Stop *EX PARTE* REEXAM
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

This Request for *Ex Parte* Reexamination contains:

1. A statement pointing out each substantial new question of patentability based on prior patents and printed publications.

2. An identification of every claim for which reexamination is requested, and a detailed explanation of the pertinency and manner of applying the cited prior art to every claim for which reexamination is requested.

3. A copy of every patent or printed publication relied upon or referred to in paragraph (1) and (2) above accompanied by an English language translation of applicable non-English language patents or printed publications.

4. A copy of the entire patent including the front face, drawings, and specification/claims (in double column format) for which reexamination is requested.

5. A duplicate of the transmittal form is attached and the Commissioner is hereby authorized to charge any fee or credit any overpayment to Deposit Account No. 02-0383 of Baker Botts L.L.P.

Respectfully submitted,

BAKER BOTTS L.L.P.
Attorneys for Petitioner

Michael Hawes
Reg. No. 38,487

Date: October 19, 2006

Baker Botts LLP
910 Louisiana
Houston, TX 77002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

U.S. Patent No. :	5,809,336
Serial No.:	484,918
Filing Date:	June 7, 1995
Patentees:	Charles H. Moore, Russell. H. Fish III
Issued:	September 15, 1998
Title:	HIGH PERFORMANCE MICROPROCESSOR HAVING VARIABLE SPEED SYSTEM CLOCK

Mail Stop *EX PARTE* REEXAM
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

CERTIFICATE OF MAILING BY EXPRESS MAIL

I hereby certify that the attached Request for *Ex Parte* Reexamination under 37 C.F.R. § 1.510; two copies of Request for Ex Parte Reexamination transmittal; Information Disclosure Statement; Baker Botts acknowledgment return postcard; and this Certificate of Mailing by Express Mail is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on this 19th day of October 2006, addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Michael Hawes

Express Mail Receipt
No. EV588885930US
Attorney Docket No.: **076885.0102**

Reexamination Control No: (new)

In re: U.S. Patent No. 5,809,336

Reexamination Filing Date: October 19, 2006

For: **High Performance Microprocessor Having Variable Speed System Clock**

Mail Stop Ex Parte Reexam
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Request for Ex Parte Reexamination

I. REEXAMINATION REQUEST

Reexamination under 35 U.S.C. §§ 302-307 and 37 C.F.R. §1.510 is requested of United States Patent No. 5,809,336, which was issued September 15, 1998 to Charles H. Moore and Russell H. Fish, III (*Moore*). This patent remains in force.

Reexamination is requested as to claims 1-10 on the basis of new art not considered by the Examiner, namely, U.S. Patent No. 4,763,297, issued to *Uhlenhoff*; U.S. Patent No. 4,691,124 issued to *Ledzius*; U.S. Patent No. 5,237,699 issued to *Little*; U.S. Patent No. 4,931,748 issued to *McDermott*; U.S. Patent No. 4,689,581 issued to *Talbot* (and the references incorporated therein); U.S. Patent No. 4,766,567 issued to *Kato*; Engineering data IMS T414M transputer published in August 1987; TLCS-42, 47, 470 User's Manual Published in April 1986; SM550/SM551/SM552 4-bit Microcomputer (Controller) published in 1982, 1983; the Sharp SM550 Publication in view of U.S. Patent No. 4,766,567 to *Kato*; a publication by Robert C. Stanley, *Microprocessors in brief*, IBM J. Res. Develop. Vol. 29, No. 2 at 115-16 (March 1985); and Japanese Patent Application No. SHO 61[1986]-127228 to *Arai*, published on June 14, 1984 (attached as Exhibits 1-11 respectively). At least in view of the patent owner's interpretation of the claims of the '336 patent during pending litigation, each of these references anticipates all of the subject matter of these issued claims, including a microprocessor system comprising a single integrated circuit including a processing circuit and an entire ring oscillator variable speed system clock for clocking the processing circuit, and an on-chip input/output interface clocked according to a second clock independent of the ring oscillator.

A substantial new question of patentability as to claims 1 - 10 is raised by this new art, pursuant to 37 C.F.R. § 1.510(b)(1), and a detailed explanation of the pertinence and manner of applying the cited art to each such claim for which reexamination is requested is also included in this request, pursuant to 37 C.F.R. 1.510(b)(2). Specifically, the above cited references not only raise a substantial new question of patentability, but also anticipate at least claims 1 - 10 of

Moore. Accordingly, Requestor respectfully requests that the Director order reexamination of *Moore*.

II. RELEVANT ONGOING LITIGATION

Moore is the subject of ongoing litigation in the Eastern District of Texas, Marshall Division, in the case styled *TPL v. Fujitsu, et al.*, Civil Action No. 2:05-cv-00494. TPL is a current purported patent owner of *Moore*.

A. TPL's Admissions Establish that the Claims Encompass the Prior Art

TPL has made numerous assertions regarding the interpretation of several claim terms of *Moore*. "An admission by the patent owner of record in the file or in a court record may be utilized in combination with a patent or printed publication, for establishing a substantial new question of patentability." MPEP 2258, I. F. 1. On August 14, 2006, TPL filed a motion in the *TPL v. Fujitsu* case. As part of that motion, TPL entered its contentions regarding the claim scope into the court record. For example, TPL identified portions of the TC35273 product and corresponding claim language from all ten of the *Moore* claims. TPL's contentions regarding the TC35273 are attached as Exhibit 14.

According to the patent owner's statements in the court record, only a few basic features are required by the *Moore* claims. For example, claim 1 is satisfied by a "monolithic integrated circuit," *see* Exhibit 14 at 3, with an onboard processor, *see id.* at 4, a PLL, *see id.* at 4-5, and a serial input/output interface, *see id.* at 7-8. Each of these four features are also found in the prior art. For example, the *Talbot* reference (attached as Exhibit 5 and discussed in detail in section IV.I-J) teaches a monolithic integrated circuit (identified as single silicon chip 1 in Figure 1), an onboard processor (identified as CPU 12 in Figure 1 of the European Application, Exhibit 5 incorporated into Talbot at Col. 2, Lines 47-52), a PLL (identified as PLL 4 at Col. 3, Lines 5-7 of Talbot), and a serial input/output interface (identified as serial links 25 in Figure 1 of the incorporated European Application).

Significantly, the patent owner asserts that a large portion of the claim is satisfied inherently, without any reference to the TC35273, by citation of Zuchowski and Sundaresan. *See id.* at 5-6. The inherent text, underlined below, is half the language of claim 1:

> 1. A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, <u>said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;</u> an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said

ring oscillator variable speed system clock connected to said input/output interface.

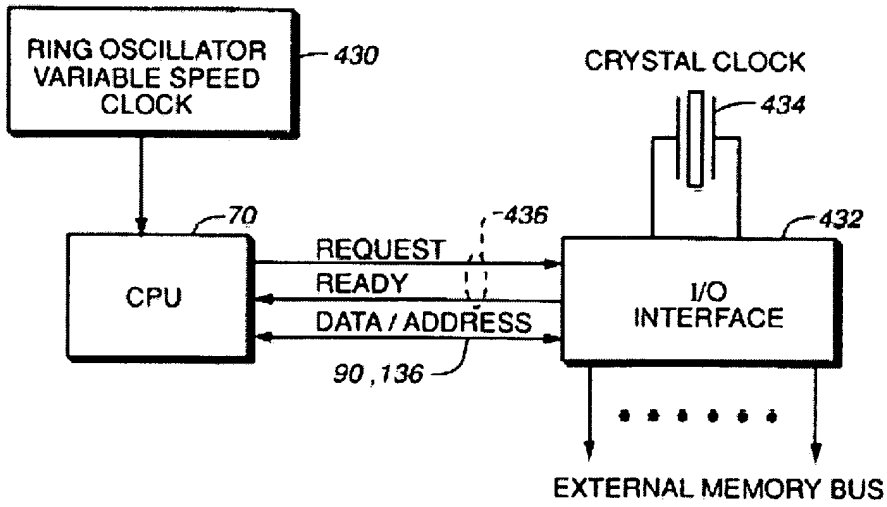
As discussed above, the remaining language, as applied by the patent owner, is taught by prior art reference such as Talbot.

B. Claims Given Their Broadest Reasonable Interpretation

In addition, Requestor understands that during reexamination, claims are given the broadest reasonable interpretation consistent with the specification, and that limitations in the specification are not read into the claims. *See* MPEP § 2258; In re Yamamoto, 740 F.2d 1569, 222 USPQ 934 (Fed. Cir. 1984). As a result, Requestor's comments regarding the claims do not necessarily reflect the interpretation those claims would receive in a district court action.

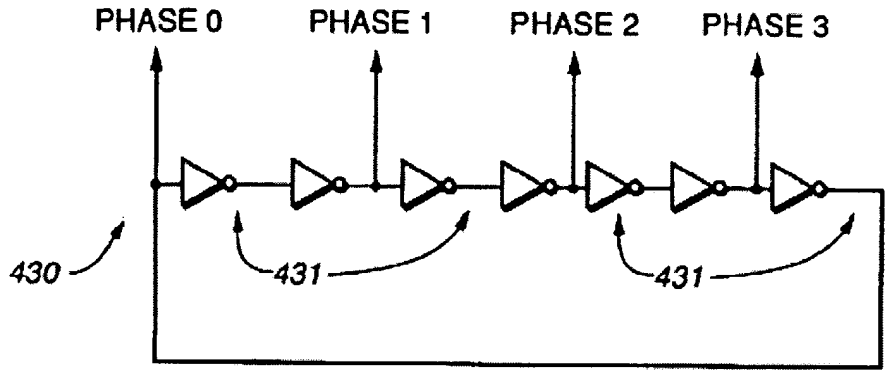
III. SUMMARY OF U.S. PATENT NO. 5,809,336

Claims 1-5 of *Moore* call for a system and method for clocking a microprocessor wherein the central processing unit ("CPU") of the microprocessor is clocked by a ring oscillator whose speed varies with the CPU speed by virtue of the "entire" ring oscillator clock being manufactured on the same integrated circuit as the CPU. The system also includes an on-chip input/output interface that is clocked by a second clock that is independent of the ring oscillator clock. Claims 6-10 of *Moore* call for a microprocessor system and method with a CPU that is clocked by one oscillator or clock, and an input/output interface that is clocked by a second external clock independent of the CPU clock. Figure 17 from *Moore*, reproduced below, illustrates the CPU and clock arrangement of claims 1-10.



All of *Moore's* claims state that the "entire" CPU clock is "variable" whose speed varies with the on-chip CPU speed as a result of being manufactured using the same process technology as the CPU and/or due to the operating voltage or temperature of the integrated circuit where both the CPU and clock are located. Figure 18 of *Moore*, reproduced below, illustrates the "entire" ring oscillator or clock of claims 1-10. A ring oscillator comprises a circuit with an odd-

number of inverters whose output is fed into the input of the circuit. The output of the circuit is the inverse of the input. Feeding back the output into the input causes the circuit to oscillate.



As discussed below, these systems and methods were explicitly taught in the prior art more than one year before *Moore's* earliest possible priority date.

IV. PATENTS, PRINTED PUBLICATIONS, AND ADMISSIONS BY THE PATENT OWNER RELIED UPON OR REFERRED TO

Every patent or printed publication relied upon or referred to is attached as follows and is also cited on the attached modified Form PTO/SB/42. In addition, pursuant to MPEP 2258, I.F.1., admissions by the patent owner of record in court records are attached as follows.

EXHIBIT NO.	REFERENCE
EXHIBIT 1	U.S. Patent No. 4,763,297 issued to *Uhlenhoff*
EXHIBIT 2	U.S. Patent No. 4,691,124 issued to *Ledzius*
EXHIBIT 3	U.S. Patent No. 5,237,699 issued to *Little*
EXHIBIT 4	U.S. Patent No. 4,931,748 issued to *McDermott*
EXHIBIT 5	U.S. Patent No. 4,689,581 issued to *Talbot* (and the references incorporated therein)
EXHIBIT 6	U.S. Patent No. 4,766,567 issued to *Kato*
EXHIBIT 7	Engineering data IMS T414M transputer published in August 1987
EXHIBIT 8	TLCS-42, 47, 470 User's Manual Published in April 1986
EXHIBIT 9	SM550/SM551/SM552 4-bit Microcomputer (Controller) published in 1982, 1983
EXHIBIT 10	Robert C. Stanley, *Microprocessors in brief*, IBM J. Res. Develop. Vol. 29, No. 2 at 115-16 (March 1985)

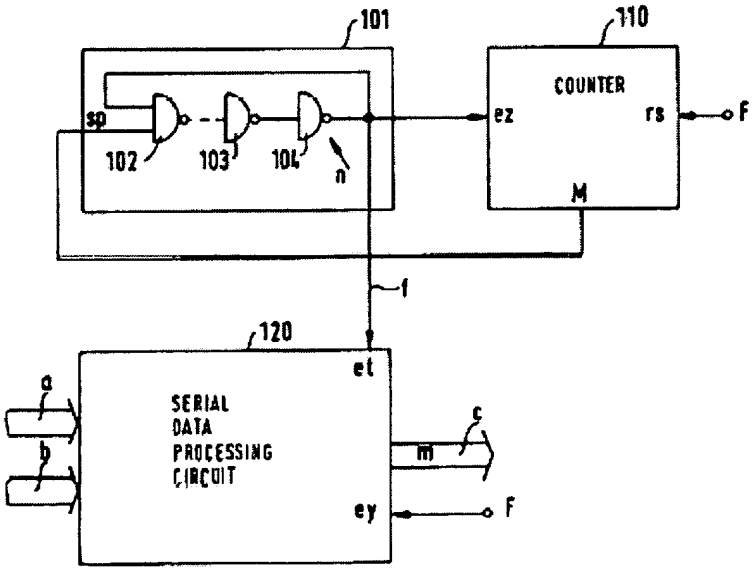
EXHIBIT 11	Japanese Patent Application No. SHO 61[1986]-127228 to *Arai*, published on June 14, 1984
EXHIBIT 12	TPL Infringement Contention for the TLCS-900/L Series
EXHIBIT 13	TPL Infringement Contention for Toshiba Microcontroller
EXHIBIT 14	TPL Infringement Contention for Toshiba TC35273

V. DISCUSSION OF THE PRIOR ART AND SUBSTANTIAL NEW QUESTIONS OF PATENTABILITY

A. Unites States Patent No. 4,763,297 to *Uhlenhoff*

United States Patent No. 4,763,297 to *Uhlenhoff* (Exhibit 1) was filed in the U.S. on May 7, 1986 and issued August 9, 1988. *Uhlenhoff* claims a Foreign Application Priority Date of May 7, 1985 through European Patent Off. No. 85105578.0. *Uhlenhoff* was also published as a European patent application on November 12, 1986, publication number 0200797A1. Because *Moore* claims a priority date of August 3, 1989, the United States application of *Uhlenhoff* comprises prior art under 35 U.S.C. § 102(e) and the European publication of *Uhlenhoff* is prior art under 35 U.S.C. § 102(b).

The lone Figure of *Uhlenhoff* is reproduced below. *Uhlenhoff* presents a monolithic integrated circuit including at least one circuit for processing multi-digit signals 120 synchronized to an entire integrated clock oscillator 101. Circuits for processing multi-digit signals include "signal processors and microprocessors which are commercially available." Col. 1, ll. 12-14. The clock oscillator 101 includes an odd number of ring-connected inverting stages, or a ring oscillator. Col. 1, ll. 54-57. Ring oscillator 101 provides the clock signal that clocks the processing circuit 120. Col. 1, ll. 55-57. *Uhlenhoff* teaches that the entire ring oscillator 101 is manufactured on the same integrated circuit as the processing unit 120, and that the frequency



of ring oscillator 101 depends on the selected integration technique used for the integrated circuit and the delaying properties of inverting stages, which are inherent to each of the specific integration techniques. Col. 1, ll. 57-61. *Uhlenhoff* also teaches that the speed of the processing unit 120 will also depend on the integration technique of the integrated circuit, stating that "as development of faster integration techniques further continues, the invention will permit the then possible integrated digital circuits to be adapted automatically to this increase or advance in speed." Col. 1, ll. 57-61. The input and output (a, b, and c) of the processing unit 120 is synchronized to an independent system clock signal, shown in the Figure as F. Col. 2, ll. 48-55.

B. *Uhlenhoff* Raises a Substantial New Question of Patentability

Substantial new questions regarding the patentability of *Moore* exist in light of *Uhlenhoff*, which was not referenced by the Examiner. Requestor respectfully submits that *Uhlenhoff* recites every element of claims 1-10 of *Moore*, as explained above. For the Commissioner's convenience, claim charts mapping claims 1-10 of *Moore* to the teachings of *Uhlenhoff* are provided below.

Claim 1 of the '336 Patent – Filed August 3, 1989	**U.S. Patent No. 4,763,297 to *Uhlenhoff* - § 102(b) Art - Published in Europe November 18, 1986**
A microprocessor system, comprising a single integrated circuit including a central processing unit	*Uhlenhoff* discloses a monolithic integrated digital circuit comprising a data-processing circuit, which can be a microprocessor. Abstract; col. 1, ll. 12-14.
and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	*Uhlenhoff* teaches that an internal entire on-chip ring oscillator is used to clock the data processing circuit, which can be a microprocessor. "[T]he actual clock signal for the data processing there is used a clock signal produced internally by a clock oscillator consisting of an odd number of ring-connected inverter stages. In other words, a ring oscillator.." Col. 1, ll. 54-58.
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	*Uhlenhoff* teaches a ring oscillator that consists of a plurality of electronic devices including an odd number of inverting stages (Col. 1, ll. 55-57) and processors and microprocessors that consist of a plurality of electronic devices including data processing circuits. Col. 1, ll. 12-14. Both the clock and the processor are manufactured on a single integrated circuit using the same process technology or integration technique. Col. 1, ll. 33-40. *Uhlenhoff* teaches that the processing frequency capability of the processing unit and the speed of the ring oscillator will vary

	together due to manufacturing variations. "[A] ring oscillator is used whose frequency depends on the selected integration technique, but makes use of the delaying properties of inverting stages, which are inherent to each of the specific integration techniques." Col. 1, ll. 57-61. "As the development of faster integration techniques further continues, the invention will permit the then possible integrated digital circuits [such as microprocessors] to be adapted automatically to this increase or advance in speed." Col. 1, ll. 62-66. The frequency capability of the processor and speed of the ring oscillator of *Uhlenhoff* will inherently vary together due to manufacturing variations, temperature, and voltage as a result of being manufactured on the same integrated circuit using the same process.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;	The Figure shows an on-chip I/O interface for the data processing system (a, b, and c). The I/O interface exchanges data with the processing unit. Col. 2, ll. 41-48.
and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	*Uhlenhoff* teaches a second system clock that clocks the processing unit's on-chip I/O. "[T]he data signals a, b and the output signal c can be synchronized with the system clock . . ." Col. 2, ll. 51-52. The second system clock signal is shown as F in the Figure and is independent of the on-chip ring oscillator.

Claim 2 of the '336 Patent	**U.S. Patent No. 4,763,297 to *Uhlenhoff***
The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	*Uhlenhoff* teaches that the second system clock can be any system clock that is "commercially available." Col. 1, ll. 17-18. Fixed frequency clocks were readily available in at the time *Uhlenhoff* was published in 1988. For instance U.S. Patent 4,750,111 teaches a processor bus clocked by a clock whose frequency is fixed at 10 MHz. (col. 19, ll. 44-45).

Claim 3 of the '336 Patent	**U.S. Patent No. 4,763,297 to *Uhlenhoff***
In a microprocessor integrated circuit, a	*Uhlenhoff* discloses a monolithic integrated

method for clocking the microprocessor within the integrated circuit, comprising the steps of:	digital circuit comprising a data-processing circuit, which can be a microprocessor. Col. 1, ll. 8-13. *Uhlenhoff* also discloses a method for clocking the microprocessor. Col. 1, ll. 50-60.
providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;	An internal entire ring oscillator is used to clock the data processing circuit, which can be a microprocessor. "[T]he actual clock signal for the data processing there is used a clock signal produced by a clock oscillator consisting of an odd number of ring-connected inverter stages. In other words, a ring oscillator..." Col. 1, ll. 54-58. *Uhlenhoff* teaches that the operating characteristics of the ring oscillator and processing circuit will vary together due to being located within the same integrated circuit. "[A] ring oscillator is used whose frequency depends on the selected integration technique, but makes use of the delaying properties of inverting stages, which are inherent to each of the specific integration techniques." Col. 1, ll. 57-61. "As the development of faster integration techniques further continues, the invention will permit the then possible integrated digital circuits [such as microprocessors] to be adapted automatically to this increase or advance in speed." Col. 1, ll. 62-66.
using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;	An internal entire ring oscillator is used to clock the data processing circuit, which can be a microprocessor. "[T]he actual clock signal for the data processing there is used a clock signal produced by a clock oscillator consisting of an odd number of ring-connected inverter stages. In other words, a ring oscillator..." Col. 1, ll. 54-58. The processing circuit operates at a variable processing frequency depending on the variable speed of the ring oscillator clock. "[A] ring oscillator is used whose frequency depends on the selected integration technique, but makes use of the delaying properties of inverting stages, which are inherent to each of the specific integration techniques." Col. 1, ll.

	57-61.
providing an on chip input/output interface for the microprocessor integrated circuit; and	The Figure shows an on-chip I/O interface for the data processing system (labeled a, b, and c).
clocking the input/output interface with a second clock independent of the ring oscillator system clock.	*Uhlenhoff* teaches a second system clock that clocks the processing circuit's on-chip I/O. "[T]he data signals a, b and the output signal c can be synchronized with the system clock . . ." Col. 2, ll. 51-52. The second system clock signal is shown as F in the Figure and is independent of the on-chip ring oscillator.

Claim 4 of the '336 Patent	**U.S. Patent No. 4,763,297 to *Uhlenhoff***
The method of claim 3 in which the second clock is a fixed frequency clock.	*Uhlenhoff* teaches that the second system clock can be any system clock that is "commercially available." Col. 1, ll. 17-18. Fixed frequency clocks were readily available at the time *Uhlenhoff* was published in 1988. For instance U.S. Patent 4,750,111 teaches a processor bus clocked by a clock whose frequency is fixed at 10 MHz. Col. 19, ll. 44-45.

Claim 5 of the '336 Patent	**U.S. Patent No. 4,763,297 to *Uhlenhoff***
The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would include the interface of *Uhlenhoff*.

Claim 6 of the '336 Patent	**U.S. Patent No. 4,763,297 to *Uhlenhoff***
A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;	*Uhlenhoff* teaches a monolithic integrated digital circuit comprising a data-processing circuit, which can be a microprocessor. Abstract; col. 1, ll. 12-14. *Uhlenhoff* teaches processors and microprocessors that consist of a plurality of electronic devices including data processing circuits. Col. 1, ll. 12-14.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock	*Uhlenhoff* teaches an entire ring oscillator that consists of a plurality of electronic devices on the integrated circuit, including an odd number of inverting stages. Col. 1, ll. 55-57.

rate and being constructed of a second plurality of electronic devices,	*Uhlenhoff* teaches that an internal on-chip ring oscillator is used to clock the data processing circuit, which can be a microprocessor. "[T]he actual clock signal for the data processing there is used a clock signal produced internally by a clock oscillator consisting of an odd number of ring-connected inverter stages. In other words, a ring oscillator..." Col. 1, ll. 54-58.
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	Both the clock and the processor are manufactured on a single integrated circuit using the same process technology or integration technique. Col. 1, ll. 33-40. *Uhlenhoff* teaches that the processing frequency capability of the processing circuit and the speed of the ring oscillator will vary together due to manufacturing variations. "[A] ring oscillator is used whose frequency depends on the selected integration technique, but makes use of the delaying properties of inverting stages, which are inherent to each of the specific integration techniques." Col. 1, ll. 57-61. "As the development of faster integration techniques further continues, the invention will permit the then possible integrated digital circuits [such as microprocessors] to be adapted automatically to this increase or advance in speed." Col. 1, ll. 62-66. The frequency capability of the processor and speed of the ring oscillator of *Uhlenhoff* will inherently vary together due to manufacturing variations, temperature, and voltage as a result of being manufactured on the same integrated circuit using the same process.
an on-chip input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	The Figure shows an on-chip I/O interface for the data processing system (labeled a, b, and c). The I/O interface exchanges data with the processing circuit. Col. 2, ll. 41-48.
an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock	*Uhlenhoff* teaches a second system clock that clocks the processing circuit's on-chip I/O. "[T]he data signals a, b and the output signal c can be synchronized with the system clock . . ."

frequency of said oscillator.	Col. 2, ll. 51-52. The second system clock signal is shown as F in the Figure and is independent of the on-chip ring oscillator.

Claim 7 of the '336 Patent	**U.S. Patent No. 4,763,297 to *Uhlenhoff***
The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	*Uhlenhoff* teaches that the processing frequency capability of the processing circuit and the speed of the ring oscillator will vary together due to manufacturing variations. "[A] ring oscillator is used whose frequency depends on the selected integration technique, but makes use of the delaying properties of inverting stages, which are inherent to each of the specific integration techniques." Col. 1, ll. 57-61. "As the development of faster integration techniques further continues, the invention will permit the then possible integrated digital circuits [such as microprocessors] to be adapted automatically to this increase or advance in speed." Col. 1, ll. 62-66. The frequency capability of the processor and speed of the ring oscillator of *Uhlenhoff* will inherently vary together due to manufacturing variations, temperature, and voltage as a result of being manufactured on the same integrated circuit using the same process.

Claim 8 of the '336 Patent	**U.S. Patent No. 4,763,297 to *Uhlenhoff***
The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would include the input/output interface of *Uhlenhoff*.

Claim 9 of the '336 Patent	**U.S. Patent No. 4,763,297 to *Uhlenhoff***
The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	*Uhlenhoff* teaches that the on-chip oscillator can be a ring oscillator. "[T]he actual clock signal for the data processing there is used a clock signal produced by a clock oscillator consisting of an odd number of ring-connected inverter stages. In other words, a ring oscillator..." Col. 1, ll. 54-58.

Claim 10 of the '336 Patent	**U.S. Patent No. 4,763,297 to *Uhlenhoff***
In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of: providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	*Uhlenhoff* discloses a monolithic integrated digital circuit comprising a data-processing circuit, which can be a microprocessor. Col. 1, ll. 8-13. *Uhlenhoff* also discloses a method for clocking the microprocessor. Col. 1, ll. 50-60. *Uhlenhoff* teaches processors and microprocessors that consist of a plurality of electronic devices including data processing circuits. Col. 1, ll. 12-14. *Uhlenhoff* teaches semiconductor integration techniques including bipolar and MOS and, more specifically, I2L, N-channel, or CMOS. These techniques inherently construct processors with transistors.
providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	*Uhlenhoff* teaches that an internal on-chip ring oscillator is used to clock the data processing circuit, which can be a microprocessor. "[T]he actual clock signal for the data processing there is used a clock signal produced internally by a clock oscillator consisting of an odd number of ring-connected inverter stages. In other words, a ring oscillator..." Col. 1, ll. 54-58. *Uhlenhoff* teaches semiconductor integration techniques including bipolar and MOS and, more specifically, I2L, N-channel, or CMOS. These techniques inherently the inverters of the internal clock with transistors.

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	The internal ring oscillator is used to clock the data processing circuit, which can be a microprocessor. "[T]he actual clock signal for the data processing there is used a clock signal produced by a clock oscillator consisting of an odd number of ring-connected inverter stages. In other words, a ring oscillator..." Col. 1, ll. 54-58. The microprocessor is clocked at a variable frequency depending upon a variable speed of the ring oscillator. The processing frequency of the processing circuit and the clock rate of the clock will vary the same way relative to variations in fabrication or operational parameters associated with the integrated circuit substrate. "[A] ring oscillator is used whose frequency depends on the selected integration technique, but makes use of the delaying properties of inverting stages, which are inherent to each of the specific integration techniques." Col. 1, ll. 57-61. "As the development of faster integration techniques further continues, the invention will permit the then possible integrated digital circuits [such as microprocessors] to be adapted automatically to this increase or advance in speed." Col. 1, ll. 62-66.
connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	The Figure shows an on-chip I/O interface for the data processing system (labeled a, b, and c). The I/O interface exchanges data with the processing circuit. Col. 2, ll. 41-48.
clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	*Uhlenhoff* teaches a second system clock that clocks the processing circuit's on-chip I/O. "[T]he data signals a, b and the output signal c can be synchronized with the system clock . . ." Col. 2, ll. 51-52. The second system clock signal is shown as F in the Figure and is independent of the on-chip ring oscillator.

C. U.S. Patent No. 4,691,124 to *Ledzius*

United States Patent No. 4,691,124 to *Ledzius* (Exhibit 2) was issued on September 1, 1987 and is prior art to *Moore* under 35 U.S.C. § 102(b). *Ledzius* discloses "[a]n integrated circuit which contains an on-chip clock that operates the integrated circuit as its true maximum speed." Abstract. The integrated circuit is shown in FIG. 1 reproduced below.

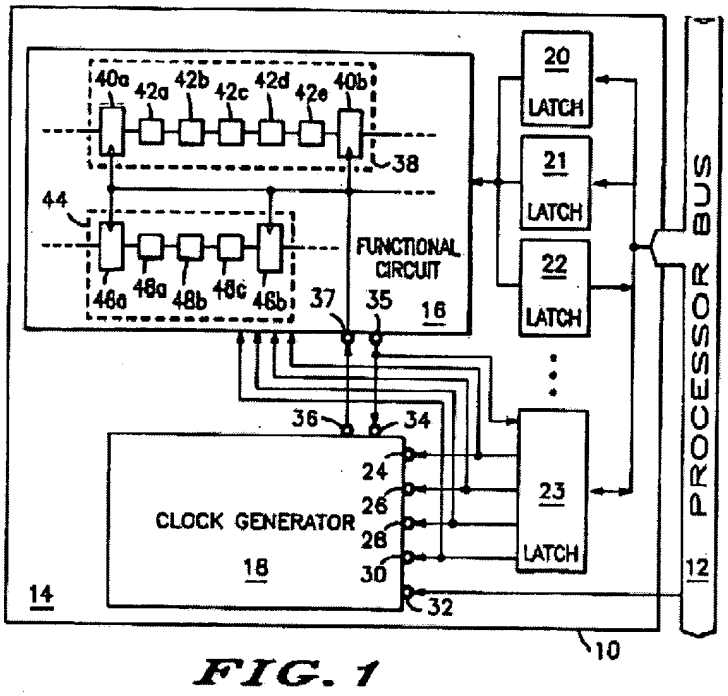


FIG. 1

The CPU is shown as functional circuit 16 and the on-chip clock is shown as clock generator 18. *Ledzius* discloses that Functional Circuit 16 may perform dedicated tasks such as "digital signal processing" and "cryptographic algorithms" but "need not be limited to a particular type of task" and can perform "a wide variety of diverse tasks." As of 1989, digital signal processors, as understood in the art, included programmable microprocessors with central processing units. See U.S. Patent No. 4,718,081 issued January 5, 1988, at col. 5, ll. 64-67 ("[c]ell site controller 26 may be any conventional digital signal processor, and preferably includes a central processing unit." *Ledzius* explicitly taught that the on-chip clock could comprise a circuit with an odd number of inverting elements arranged in a ring. See FIG. 2 below.

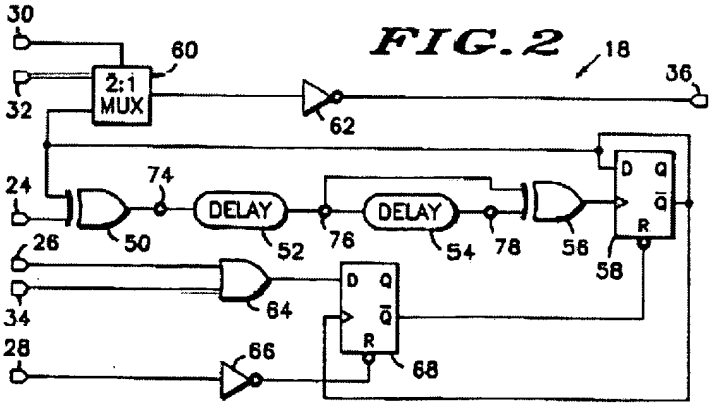


FIG. 2

Finally, *Ledzius* taught a second clock, from which the ring oscillator clock would be independent, which clocked the processor bus to which the integrated circuit was attached: "The integrated circuit operates asynchronously from a processor bus and contains circuitry for interfacing with the processor bus." Abstract.

D. *Ledzius* Raises a Substantial New Question of Patentability

Substantial new questions regarding the patentability of *Moore* exist in light of *Ledzius*, which was not referenced by the Examiner. Requestor respectfully submits that *Ledzius* recites every element of claims 1-10 of *Moore*, as explained above. For the Commissioner's convenience, claim charts mapping claims 1-10 of *Moore* to the teachings of *Ledzius* are provided below.

Claim 1 of the '336 Patent	**U.S. Patent No. 4,691,124 to *Ledzius* et al. issued September 1, 1987**
A microprocessor system, comprising a single integrated circuit including	The '124 patent discloses a microprocessor system comprising an integrated circuit. See Fig. 1; col. 2, ll. 24-32.
a central processing unit and	Functional circuit 16 shown in Fig. 1 is described as being capable of performing processes or jobs such as digital signal processing or a wide variety of other tasks. Col. 2, ll. 33-57. One of ordinary skill would recognize that Functional circuit 16 could be a microprocessor system with a central processing unit." As of 1989, digital signal processors, as understood in the art, included programmable microprocessors with central processing units. See U.S. Patent No. 4,718,081 issued January 5, 1988, at col. 5, ll. 64-67 ("[c]ell site controller 26 may be any conventional digital signal processor, and preferably includes a central processing unit."
an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	The '124 patent discloses an entire ring oscillator variable speed system clock on the single integrated circuit. Figure 2 shows clock generator 18 which is part of the integrated circuit shown in Fig. 1. Clock generator 18 has a D-Flip Flop 58 connected in ring form. The arrangement comprises an odd number of inverting elements connected in a ring to form a oscillation. The ring oscillator 18 is connected to the CPU and clocks the CPU. Fig. 1; col. 3, line 64 - col. 4, line 2.
said central processing unit and said ring	The CPU 16 and ring oscillator 18 are

oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	constructed of the same process technology. Col. 4, lines 5-14.
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	As a result of being manufactured on the same integrated circuit as the microprocessor, the oscillator varies together with operating characteristics of electronic devices included within the microprocessor. "Since both clock generator 18 and function circuit 16 are constructed on substrate 14, clock generator 18 compensates for temperature and process caused variations in the true maximum speed of functional circuit 16. The frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances." Col. 4, lines 5-14.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;	Figure 1 of the '124 patent indicates that the CPU and processor bus are connected by an on-chip input/output interface comprising a number of latches 20-23 and control registers that exchange coupling control signals, address, and data. Col. 3, lines 32-42.
and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	The input/output interface, latches 20-23, communicates asynchronously with a second processor across processor bus 12, with its own external clock signal 32. "The integrated circuit operates asynchronously from a processor bus and contains circuitry for interfacing with the processor bus." Abstract. The processor bus clock is the clock for input/output latches 20-23 when the clock generator is disabled in favor of the external clock, since it is the only available clock. Col. 6, lines 11-16.

Claim 2 of the '336 Patent	**U.S. Patent No. 4,691,124 to *Ledzius* et al. issued September 1, 1987**
The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	*Ledzius* teaches that the processor bus is asynchronous relative to the integrated circuit. It was well known in 1989 that a processor bus could be clocked by a fixed frequency clock.

	For instance U.S. Patent 4,750,111 teaches a processor bus clocked by a clock whose frequency is fixed at 10 MHz. (col. 19, ll. 44-45).

Claim 3 of the '336 Patent	U.S. Patent No. 4,691,124 to *Ledzius* et al. issued September 1, 1987
In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:	The '124 patent discloses a microprocessor system comprising an integrated circuit and a method for clocking the microprocessor. See Fig. 1; col. 2, ll. 24-32.
providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;	The '124 patent discloses an entire ring oscillator variable speed system clock on the single integrated circuit. Figure 2 shows clock generator 18 which is part of the integrated circuit shown in Fig. 1. Clock generator 18 has a D-Flip Flop 58 connected in ring form. The arrangement comprises an odd number of inverting elements connected in a ring to form a oscillation. The CPU 16 and ring oscillator 18 are constructed of the same process technology. Col. 4, lines 5-14. As a result of being manufactured on the same integrated circuit as the microprocessor, the oscillator varies together with operating characteristics of electronic devices included within the microprocessor. "Since both clock generator 18 and function circuit 16 are constructed on substrate 14, clock generator 18 compensates for temperature and process caused variations in the true maximum speed of functional circuit 16. The frequency of the clock signal produced by clock generator 18 varies to reflect process and temperature variances." Col. 4, lines 5-14.

using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;	The ring oscillator 18 is connected to the microprocessor 16 and clocks the microprocessor 16. Fig. 1; col. 3, line 64 - col. 4, line 2. The microprocessor operates at a variable processing frequency depending on the variable speed of the ring oscillator 18.
providing an on chip input/output interface for the microprocessor integrated circuit; and	Figure 1 of the '124 patent indicates that the CPU and processor bus are connected by an on-chip input/output interface comprising a number of latches 20-23 and control registers that exchange coupling control signals, address, and data. Col. 3, lines 32-42.
clocking the input/output interface with a second clock independent of the ring oscillator system clock.	The input/output interface, latches 20-23, communicates asynchronously with a second processor across processor bus 12, with its own external clock signal 32. The processor bus clock is the clock for input/output latches 20-23 when the clock generator is disabled in favor of the external clock, since it is the only available clock. Col. 6, lines 11-16.

Claim 4 of the '336 Patent	**U.S. Patent No. 4,691,124 to *Ledzius* et al. issued September 1, 1987**
The method of claim 3 in which the second clock is a fixed frequency clock.	*Ledzius* teaches that the processor bus is asynchronous relative to the integrated circuit. It was well known in 1989 that a processor bus could be clocked by a fixed frequency clock. For instance U.S. Patent 4,750,111 teaches a processor bus clocked by a clock whose frequency is fixed at 10 MHz. (col. 19, ll. 44-45).

Claim 5 of the '336 Patent	**U.S. Patent No. 4,691,124 to *Ledzius* et al. issued September 1, 1987**
The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would include the latches 20-23 of *Ledzius*. See Exhibit 12 at 29.

Claim 6 of the '336 Patent	U.S. Patent No. 4,691,124 to *Ledzius* et al. issued September 1, 1987
A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;	The '124 patent discloses a microprocessor system comprising an integrated circuit. See Fig. 1; col. 2, ll. 24-32.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	Functional circuit 16 shown in Fig. 1 is described as being capable of performing processes or jobs such as digital signal processing or a wide variety of other tasks. Col. 2, ll. 33-57. One of ordinary skill would recognize that Functional circuit 16 could be a microprocessor system with a central processing unit.
an on-chip input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	Figure 1 of the '124 patent indicates that the CPU and processor bus are connected by an on-chip input/output interface comprising a number of latches 20-23 and control registers that exchange coupling control signals, address, and data. Col. 3, lines 32-42.
an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	The input/output interface, latches 20-23, communicates asynchronously with a second processor across processor bus 12, with its own external clock signal 32. The processor bus clock is the clock for input/output latches 20-23 when the clock generator is disabled in favor of the external clock, since it is the only available clock. Col. 6, lines 11-16.

Claim 7 of the '336 Patent	U.S. Patent No. 4,691,124 to *Ledzius* et al. issued September 1, 1987
The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate	TPL has asserted in its infringement contentions that any on-chip ring oscillator satisfies this limitation. This would include the

or operating voltage of said substrate.	on-chip ring oscillator of *Ledzius*. See Exhibit 13 at 28.

Claim 8 of the '336 Patent	**U.S. Patent No. 4,691,124 to *Ledzius* et al. issued September 1, 1987**
The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would include the latches 20-23 of *Ledzius*. See Exhibit 12 at 29.

Claim 9 of the '336 Patent	**U.S. Patent No. 4,691,124 to *Ledzius* et al. issued September 1, 1987**
The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	Clock generator 18 shown in Figure 2 is a ring oscillator.

Claim 10 of the '336 Patent	**U.S. Patent No. 4,691,124 to *Ledzius* et al. issued September 1, 1987**
In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of: providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	The '124 patent discloses a microprocessor system comprising an integrated circuit. See Fig. 1; col. 2, ll. 24-32.
providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	Functional circuit 16 shown in Fig. 1 is described as being capable of performing processes or jobs such as digital signal processing or a wide variety of other tasks. Col. 2, ll. 33-57. One of ordinary skill would recognize that Functional circuit 16 could be a microprocessor system with a central processing unit.

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	The '124 patent discloses an entire ring oscillator variable speed system clock on the single integrated circuit. Figure 2 shows clock generator 18 which is part of the integrated circuit shown in Fig. 1. Clock generator 18 has a D-Flip Flop 58 connected in ring form. The arrangement comprises an odd number of inverting elements connected in a ring to form a oscillation. The ring oscillator 18 is connected to the CPU and clocks the CPU. Fig. 1; col. 3, line 64 - col. 4, line 2.
connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	Figure 1 of the '124 patent indicates that the CPU and processor bus are connected by an on-chip input/output interface comprising a number of latches 20-23 and control registers that exchange coupling control signals, address, and data. Col. 3, lines 32-42.
clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	The input/output interface, latches 20-23, communicates asynchronously with a second processor across processor bus 12, with its own external clock signal 32. The processor bus clock is the clock for input/output latches 20-23 when the clock generator is disabled in favor of the external clock, since it is the only available clock. Col. 6, lines 11-16.

E. U.S. Patent No. 5,237,699 Issued to *Little*

United States Patent No. 5,237,699 issued to *Little* (Exhibit 3) is a continuation of U.S. application No. 238,809 filed on August 31, 1988. As a result, *Little* is prior art against the Moore patent under 35 U.S.C. § 102(e). *Little* discloses a microprocessor with an internal ring oscillator which can clock the microprocessor. *Little* also discloses a serial interface that can be clocked by a second external clock. FIG. 6B of *Little*, reproduced below shows a microprocessor system and central processing unit according to *Little* including the serial interface 650. Col. 4, 59-68.

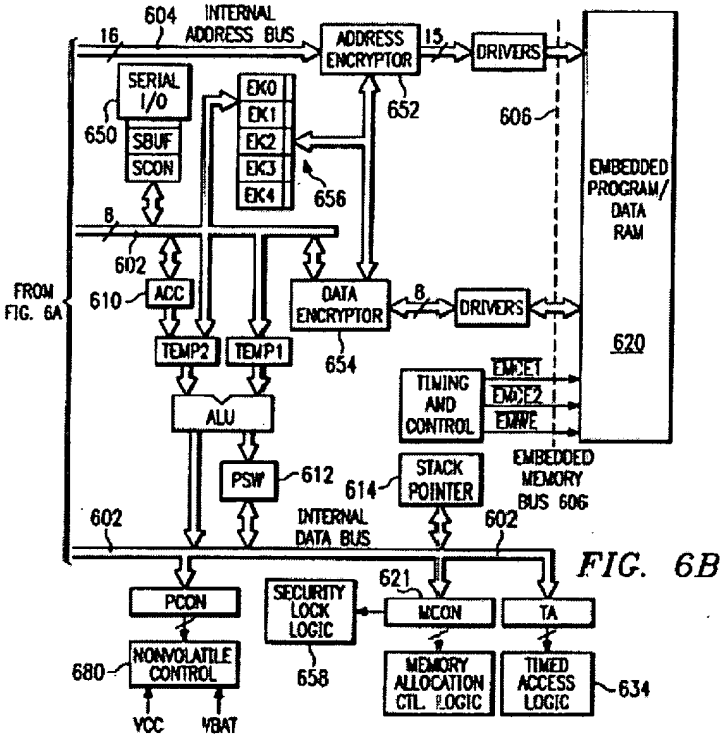


FIG. 6B

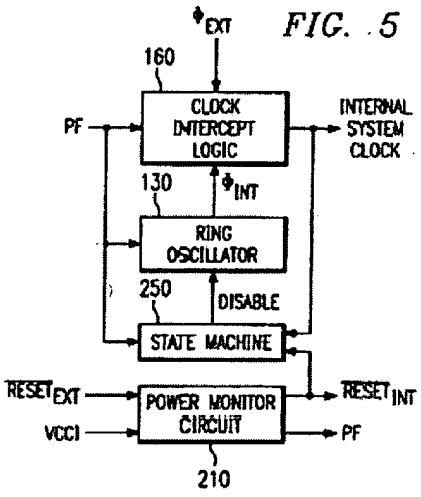


FIG. 5

In addition, FIG. 5 shows the on-chip ring oscillator 130 of *Little* which can be used to clock the microprocessor and CPU.

F. *Little* Raises a Substantial New Question of Patentability

Substantial new questions regarding the patentability of *Moore* exist in light of *Little*, which was not referenced by the Examiner. Requestor respectfully submits that *Little* recites every element of claims 1-10 of *Moore*, as explained above. For the Commissioner's convenience, claim charts mapping claims 1-10 of *Moore* to the teachings of *Little* are provided below.

Claim 1 of the '336 Patent	**U.S. Patent No. 5,237,699 to *Little* et al. Issued August 17, 1993**
A microprocessor system, comprising a single	The Abstract discloses a microprocessor

integrated circuit including	integrated circuit.
a central processing unit and	Figure 6B shows the microprocessor's central processing unit.
an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	Figure 5 item 130 shows an on-chip ring oscillator. The Abstract refers to 130 as "an internal clock generator." It is also referred to as a "local oscillator." Col. 8, ll. 5. It is an entire ring oscillator and not crystal controlled: "note that the ring oscillator 130 is not crystal-controlled, since this frequency source does not have to have as much precision." Col. 8, ll. 9-12. The internal ring oscillator 130 is used as a "system clock" during reset or low power state: "As VCCI declines further to below V.sub.CCmin (+4.5 volts), the output of the comparator 34 switches from a logical 1 to a logical 0 level, which activates reset lines all over the chip, and causes the microcontroller to go into a reset or low power state until the external power supply voltage again goes above +4.5 volts. At this time the transistors 122 and 124 will switched by clock intercept logic 160, as discussed above, to connect the internal system clock lines to the signal phi.sub.Int generated by ring oscillator 130 rather than signal phi.sub.Ext generated by crystal-controlled clock generator 690 (which uses an off-chip resonator or a system clock)." Col. 14, ll. 51-62.
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	The internal ring oscillator 130 is used as a "system clock" during reset or low power state. As a result of being manufactured on the same integrated circuit as the microprocessor, the ring oscillator varies together with operating characteristics of electronic devices included within the microprocessor.
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	The ring oscillator and processing unit of *Little* are manufactured on the same integrated circuit. According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary

	together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;	Figure 6A shows an on chip serial I/O 650.
and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	Serial I/O 650 in Figure 6A is inherently clocked by an external second clock that is independent of the ring oscillator system clock. The use of an external clock to clock a serial interface was well known in 1989. For instance, in a paper published as early as 1980, an external clock for clocking a serial interface is taught. Electronic Components and Applications, Vol. 3, No. 1, November 1980 at 38. The serial interface of this article can be clocked by an external clock source while acting as either a slave receiver or slave transmitter. Id. at 41.

Claim 2 of the '336 Patent	**U.S. Patent No. 5,237,699 to *Little* et al. Issued August 17, 1993**
The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	According to TPL, "in serial communications the transmitting device sends data and clock at a fixed frequency." See Exhibit 12 at 10. This would include the serial interface of *Little*.

Claim 3 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 5,237,699 to *Little* et al. Issued August 17, 1993**
In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:	The Abstract discloses a microprocessor integrated circuit.
providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;	Figure 5 item 130 shows an on-chip ring oscillator. The Abstract refers to 130 as "an internal clock generator." It is also referred to as a "local oscillator." Col. 8, ll. 5. It is an entire ring oscillator and not crystal controlled: "note that the ring oscillator 130 is not crystal-controlled, since this frequency source does not have to have as much precision." Col. 8, ll. 9-12.

using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;	Figure 5 item 130 shows an on-chip ring oscillator. The Abstract refers to 130 as "an internal clock generator." It is also referred to as a "local oscillator." Col. 8, ll. 5. It is an entire ring oscillator and not crystal controlled: "note that the ring oscillator 130 is not crystal-controlled, since this frequency source does not have to have as much precision." Col. 8, ll. 9-12. The internal ring oscillator 130 is used as a "system clock" during reset or low power state: "As VCCI declines further to below V.sub.CCmin (+4.5 volts), the output of the comparator 34 switches from a logical 1 to a logical 0 level, which activates reset lines all over the chip, and causes the microcontroller to go into a reset or low power state until the external power supply voltage again goes above +4.5 volts. At this time the transistors 122 and 124 will switched by clock intercept logic 160, as discussed above, to connect the internal system clock lines to the signal phi.sub.Int generated by ring oscillator 130 rather than signal phi.sub.Ext generated by crystal-controlled clock generator 690 (which uses an off-chip resonator or a system clock)." Col. 14, ll. 51-62.
providing an on chip input/output interface for the microprocessor integrated circuit; and	Figure 6A shows an on chip serial I/O 650.
clocking the input/output interface with a second clock independent of the ring oscillator system clock.	Serial I/O 650 in Figure 6A is inherently clocked by an external second clock that is independent of the ring oscillator system clock. The use of an external clock to clock a serial interface was well known in 1989. For instance, in a paper published as early as 1980, an external clock for clocking a serial interface is taught. Electronic Components and Applications, Vol. 3, No. 1, November 1980 at 38. The serial interface of this article can be clocked by an external clock source while acting as either a slave receiver or slave transmitter. Id. at 41.

Claim 4 of the '336 Patent	**U.S. Patent No. 5,237,699 to *Little* et al. Issued August 17, 1993**

The method of claim 3 in which the second clock is a fixed frequency clock.	According to TPL, "in serial communications the transmitting device sends data and clock at a fixed frequency." See Exhibit 12 at 10. This would include the serial interface of *Little*.

Claim 5 of the '336 Patent	**U.S. Patent No. 5,237,699 to *Little* et al. Issued August 17, 1993**
The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would include the serial interface of *Little*. See Exhibit 12 at 29.

Claim 6 of the '336 Patent	**U.S. Patent No. 5,237,699 to *Little* et al. Issued August 17, 1993**
A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;	The Abstract discloses a microprocessor integrated circuit.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	Figure 5 item 130 shows an on-chip ring oscillator. The Abstract refers to 130 as "an internal clock generator." It is also referred to as a "local oscillator." Col. 8, ll. 5. It is an entire ring oscillator and not crystal controlled: "note that the ring oscillator 130 is not crystal-controlled, since this frequency source does not have to have as much precision." Col. 8, ll. 9-12. The internal ring oscillator 130 is used as a "system clock" during reset or low power state: "As VCCI declines further to below V.sub.CCmin (+4.5 volts), the output of the comparator 34 switches from a logical 1 to a logical 0 level, which activates reset lines all over the chip, and causes the microcontroller to go into a reset or low power state until the external power supply voltage again goes above +4.5 volts. At this time the transistors 122 and 124 will switched by clock intercept logic 160, as discussed above, to connect the internal system clock lines to the signal

	phi.sub.Int generated by ring oscillator 130 rather than signal phi.sub.Ext generated by crystal-controlled clock generator 690 (which uses an off-chip resonator or a system clock)." Col. 14, ll. 51-62. The ring oscillator and processing unit of *Little* are manufactured on the same integrated circuit. According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
an on-chip input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	Figure 6A shows an on chip serial I/O 650.
an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	Serial I/O 650 in Figure 6A is inherently clocked by an external second clock that is independent of the ring oscillator system clock. The use of an external clock to clock a serial interface was well known in 1989. For instance, in a paper published as early as 1980, an external clock for clocking a serial interface is taught. Electronic Components and Applications, Vol. 3, No. 1, November 1980 at 38. The serial interface of this article can be clocked by an external clock source while acting as either a slave receiver or slave transmitter. Id. at 41.

Claim 7 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 5,237,699 to *Little* et al. Issued August 17, 1993**
The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary

	together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.

Claim 8 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 5,237,699 to *Little* et al. Issued August 17, 1993**
The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would include the serial interface of *Little*.

Claim 9 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 5,237,699 to *Little* et al. Issued August 17, 1993**
The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	Figure 5 item 130 shows an on-chip ring oscillator. The Abstract refers to 130 as "an internal clock generator." It is also referred to as a "local oscillator." Col. 8, ll. 5. It is an entire ring oscillator and not crystal controlled: "note that the ring oscillator 130 is not crystal-controlled, since this frequency source does not have to have as much precision." Col. 8, ll. 9-12.

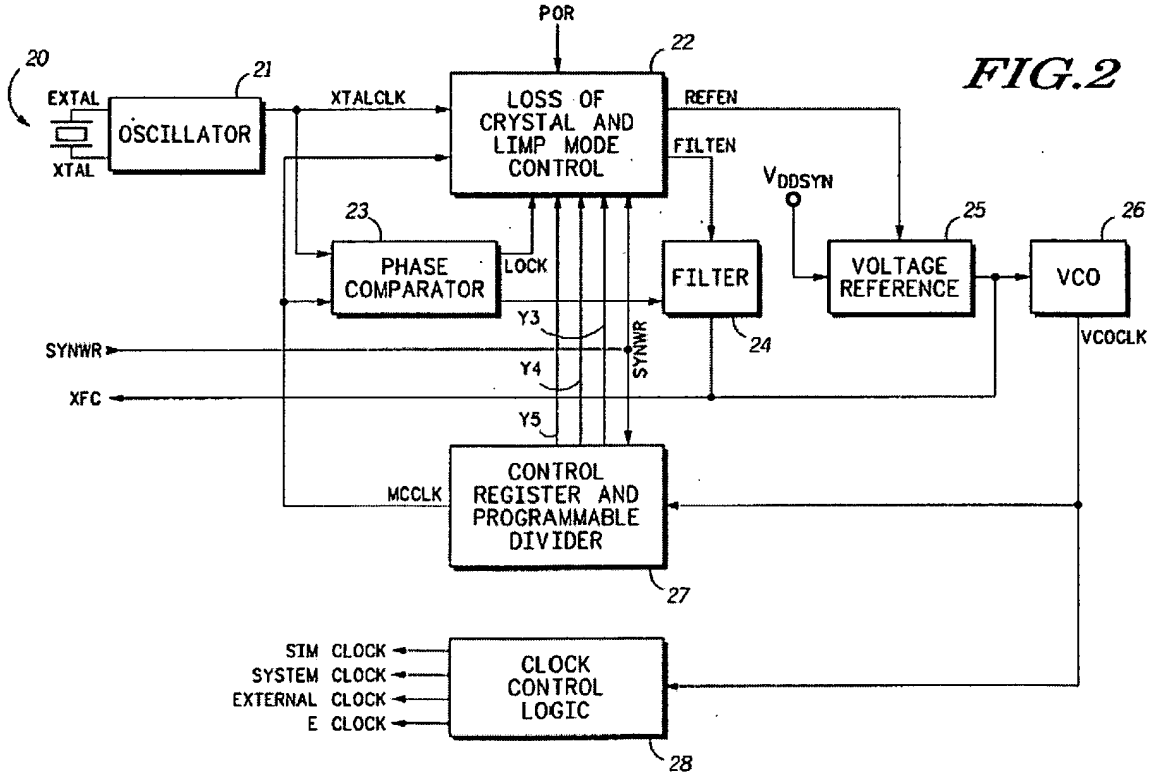
Claim 10 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 5,237,699 to *Little* et al. Issued August 17, 1993**
In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of: providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	The Abstract discloses a microprocessor integrated circuit.
providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	Figure 5 item 130 shows an on-chip ring oscillator. The Abstract refers to 130 as "an internal clock generator." It is also referred to as a "local oscillator." Col. 8, ll. 5. It is an entire ring oscillator and not crystal controlled: "note that the ring oscillator 130 is not crystal-

	controlled, since this frequency source does not have to have as much precision." Col. 8, ll. 9-12.
clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	The internal ring oscillator 130 is used as a "system clock" during reset or low power state: "As VCCI declines further to below V.sub.CCmin (+4.5 volts), the output of the comparator 34 switches from a logical 1 to a logical 0 level, which activates reset lines all over the chip, and causes the microcontroller to go into a reset or low power state until the external power supply voltage again goes above +4.5 volts. At this time the transistors 122 and 124 will switched by clock intercept logic 160, as discussed above, to connect the internal system clock lines to the signal phi.sub.Int generated by ring oscillator 130 rather than signal phi.sub.Ext generated by crystal-controlled clock generator 690 (which uses an off-chip resonator or a system clock)." Col. 14, ll. 51-62. The ring oscillator and processing unit of *Little* are manufactured on the same integrated circuit. According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	Figure 6A shows an on chip serial I/O 650.
clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	Serial I/O 650 in Figure 6A is inherently clocked by an external second clock that is independent of the ring oscillator system clock. The use of an external clock to clock a serial interface was well known in 1989. For instance, in a paper published as early as 1980,

	an external clock for clocking a serial interface is taught. Electronic Components and Applications, Vol. 3, No. 1, November 1980 at 38. The serial interface of this article can be clocked by an external clock source while acting as either a slave receiver or slave transmitter. Id. at 41.

G. U.S. Patent No. 4,931,748 issued to *McDermott* et al.

United States Patent No. 4,931,748 issued to *McDermott* et al. (Exhibit 4) from an application filed on June 9, 1989. As a result, *McDermott* is prior art against *Moore* under 35 U.S.C. § 102(e). *McDermott* discloses a microcomputer to be manufactured on a single integrated circuit that includes a CPU and a voltage controlled oscillator 26 that clocks the CPU both during power up and when a crystal clock signal is lost. *See* Col. 4, ll. 58-col. 5, ll. 10. *McDermott*'s microcomputer is disclosed as also including a serial I/O interface that can be clocked by a second external clock. FIG. 2 of *McDermott*, reproduced below shows the microcomputer and the voltage controlled oscillator 26 (VCO).



In addition, FIG. 1 shows the serial interface 13 of *McDermott*.

H. *McDermott* Raises a Substantial New Question of Patentability

Substantial new questions regarding the patentability of *Moore* exist in light of *McDermott*, which was not referenced by the Examiner. Requestor respectfully submits that *McDermott* teaches every element of claims 1-10 of *Moore*, as explained above. For the Commissioner's convenience, claim charts mapping claims 1-10 of *Moore* to the teachings of *McDermott* are provided below.

Claim 1 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,931,748 to *McDermott* et al. Issued June 5, 1990**
A microprocessor system, comprising a single integrated circuit including	Abstract describes a microprocessor integrated circuit.
a central processing unit and	Figure 1 of *McDermott* shows that the microprocessor integrated circuit comprises a CPU 11. "Fig. 1 illustrates a microcomputer . . . . Microcomputer 10, which is intended for manufacture on a single integrated circuit, comprises a CPU 11 . . ."
an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	*McDermott* teaches a voltage controlled oscillator 26 shown in Figure 2. *McDermott* states that an example of a microprocessor with such a VCO is the MC146805H2 by Motorola. In the MC146805H2, the VCO is an entire ring oscillator variable speed system clock. *McDermott* teaches that the VCO is on the single integrated circuit and provides a clock signal during power up or loss of the crystal signal. VCO 26 in Figure 2 provides a system clock signal during power up or loss of the crystal signal. This operation is described below: "Whenever logic 22 detects the powering-up of the microcomputer 10, or the loss of the crystal reference signal, or the occurrence of other events described below, the FILTEN signal is negated causing the output of loop filter 24 to disconnect from the input of VCO 26, and the REFEN signal is asserted causing the output of the voltage reference circuit 25 to connect to the input of VCO 26. Thus, the operation of VCO 26 is no longer dependent on the control voltage signal produced by loop filter 24 to determine its operating frequency. Instead, the operating frequency of VCO 26 is determined solely by the chosen output voltage of the voltage reference circuit 25. The reference

	voltage will usually, but not necessarily, be chosen to provide a much lower frequency VCOCLK than is provided in normal operation. The purpose is not to maintain system operation as if the crystal signal had not been lost, but to provide a fall-back mode of operation in which microcomputer 10 can either perform an orderly shutdown or continue to operate at a much-reduced level of capacity." Col. 4, ll. 58-col. 5, ll. 10.
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	The VCO 26 and CPU 11 of *McDermott* are constructed of the same process technology with corresponding manufacturing variations. The Abstract of *McDermott* teaches a microprocessor or other integrated circuit including a clock generator. *McDermott* teaches that during the loss of an external crystal signal, the reference voltage used to control the frequency should be chosen relative to the process variations: "A voltage reference suitable for this application should have a relatively stable output over the specified temperature range of microcomputer 10 and should be relatively stable over variations in the process used to manufacture the integrated circuit." Col. 5, lines 11-18.
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	*McDermott* teaches that he processing frequency capability of the CPU and speed of the ring oscillator vary according manufacturing variations, voltage and temperature. *McDermott* teaches that during the loss of an external crystal signal, a reference voltage is used to control the frequency and should be chosen relative to the process variations: "A voltage reference suitable for this application should have a relatively stable output over the specified temperature range of microcomputer 10 and should be relatively stable over variations in the process used to manufacture the integrated circuit." Col. 5, lines 11-18. According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing

	frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;	Figure 1 shows a serial I/O interface 13.
and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	TPL has asserted that any serial interface satisfies this limitation. Exhibit 12 at 7-8. Figure 1 of *McDermott* shows a serial I/O interface 13.

Claim 2 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,931,748 to *McDermott* et al. Issued June 5, 1990**
The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	According to TPL, "in serial communications the transmitting device sends data and clock at a fixed frequency." See Exhibit 13 at 10. This would include the serial interface of *McDermott*.

Claim 3 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,931,748 to *McDermott* et al. Issued June 5, 1990**
In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:	Abstract describes a microprocessor integrated circuit.
providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;	Figure 1 of *McDermott* shows that the microprocessor integrated circuit comprises a CPU 11. "Fig. 1 illustrates a microcomputer . . . . Microcomputer 10, which is intended for manufacture on a single integrated circuit, comprises a CPU 11 . . ." *McDermott* teaches that the processing frequency capability of the CPU and speed of the ring oscillator vary according manufacturing variations, voltage and temperature.

	McDermott teaches that during the loss of an external crystal signal, a reference voltage is used to control the frequency and should be chosen relative to the process variations: "A voltage reference suitable for this application should have a relatively stable output over the specified temperature range of microcomputer 10 and should be relatively stable over variations in the process used to manufacture the integrated circuit." Col. 5, lines 11-18.
using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;	*McDermott* teaches a voltage controlled oscillator 26 shown in Figure 2. *McDermott* states that an example of a microprocessor with such a VCO is the MC146805H2 by Motorola. In the MC146805H2, the VCO is an entire ring oscillator variable speed system clock. *McDermott* teaches that the VCO is on the single integrated circuit and provides a clock signal during power up or loss of the crystal signal. VCO 26 in Figure 2 provide a system clock signal during power up or loss of the crystal signal. This operation is described below: "Whenever logic 22 detects the powering-up of the microcomputer 10, or the loss of the crystal reference signal, or the occurrence of other events described below, the FILTEN signal is negated causing the output of loop filter 24 to disconnect from the input of VCO 26, and the REFEN signal is asserted causing the output of the voltage reference circuit 25 to connect to the input of VCO 26. Thus, the operation of VCO 26 is no longer dependent on the control voltage signal produced by loop filter 24 to determine its operating frequency. Instead, the operating frequency of VCO 26 is determined solely by the chosen output voltage of the voltage reference circuit 25. The reference voltage will usually, but not necessarily, be chosen to provide a much lower frequency VCOCLK than is provided in normal operation. The purpose is not to maintain system operation as if the crystal signal had not been lost, but to provide a fall-back mode of operation in which microcomputer 10 can

	either perform an orderly shutdown or continue to operate at a much-reduced level of capacity." Col. 4, ll. 58-col. 5, ll. 10.
providing an on chip input/output interface for the microprocessor integrated circuit; and	Figure 1 shows a serial I/O interface 13.
clocking the input/output interface with a second clock independent of the ring oscillator system clock.	TPL has asserted that any serial interface satisfies this limitation. Figure 1 of *McDermott* shows a serial I/O interface 13.

Claim 4 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,931,748 to *McDermott* et al. Issued June 5, 1990**
The method of claim 3 in which the second clock is a fixed frequency clock.	According to TPL, "in serial communications the transmitting device sends data and clock at a fixed frequency." See Exhibit 13 at 10. This would include the serial interface of *McDermott*.

Claim 5 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,931,748 to *McDermott* et al. Issued June 5, 1990**
The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would include the serial interface of *McDermott*.

Claim 6 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,931,748 to *McDermott* et al. Issued June 5, 1990**
A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;	Abstract describes a microprocessor integrated circuit.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of	Figure 1 of *McDermott* shows that the microprocessor integrated circuit comprises a CPU 11. "Fig. 1 illustrates a microcomputer . . . . Microcomputer 10, which is intended for manufacture on a single integrated circuit, comprises a CPU 11 . . ."

electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	*McDermott* teaches that he processing frequency capability of the CPU and speed of the ring oscillator vary according manufacturing variations, voltage and temperature. *McDermott* teaches that during the loss of an external crystal signal, a reference voltage is used to control the frequency and should be chosen relative to the process variations: "A voltage reference suitable for this application should have a relatively stable output over the specified temperature range of microcomputer 10 and should be relatively stable over variations in the process used to manufacture the integrated circuit." Col. 5, lines 11-18. *McDermott* teaches a voltage controlled oscillator 26 shown in Figure 2. *McDermott* states that an example of a microprocessor with such a VCO is the MC146805H2 by Motorola. In the MC146805H2, the VCO is an entire ring oscillator variable speed system clock. *McDermott* teaches that the VCO is on the single integrated circuit and provides a clock signal during power up or loss of the crystal signal. VCO 26 in Figure 2 provide a system clock signal during power up or loss of the crystal signal. This operation is described below: "Whenever logic 22 detects the powering-up of the microcomputer 10, or the loss of the crystal reference signal, or the occurrence of other events described below, the FILTEN signal is negated causing the output of loop filter 24 to disconnect from the input of VCO 26, and the REFEN signal is asserted causing the output of the voltage reference circuit 25 to connect to the input of VCO 26. Thus, the operation of VCO 26 is no longer dependent on the control voltage signal produced by loop filter 24 to determine its operating frequency. Instead, the operating frequency of VCO 26 is determined

	solely by the chosen output voltage of the voltage reference circuit 25. The reference voltage will usually, but not necessarily, be chosen to provide a much lower frequency VCOCLK than is provided in normal operation. The purpose is not to maintain system operation as if the crystal signal had not been lost, but to provide a fall-back mode of operation in which microcomputer 10 can either perform an orderly shutdown or continue to operate at a much-reduced level of capacity." Col. 4, ll. 58-col. 5, ll. 10. According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
an on-chip input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	Figure 1 shows a serial I/O interface 13.
an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	TPL has asserted that any serial interface satisfies this limitation. Figure 1 of *McDermott* shows a serial I/O interface 13.

Claim 7 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,931,748 to *McDermott* et al. Issued June 5, 1990**
The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	TPL has asserted in its infringement contentions that any on-chip ring oscillator satisfies this limitation. This would include the on-chip ring oscillator of *McDermott*.

Claim 8 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,931,748 to *McDermott* et al. Issued June 5, 1990**

The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would include the serial interface of *McDermott*.

Claim 9 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,931,748 to *McDermott* et al. Issued June 5, 1990**
The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	VCO 26 of *McDermott* comprises a ring oscillator.

Claim 10 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,931,748 to *McDermott* et al. Issued June 5, 1990**
In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of: providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	Abstract describes a microprocessor integrated circuit. Figure 1 of *McDermott* shows that the microprocessor integrated circuit comprises a CPU 11. "Fig. 1 illustrates a microcomputer . . . . Microcomputer 10, which is intended for manufacture on a single integrated circuit, comprises a CPU 11 . . ."
providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	*McDermott* teaches a voltage controlled oscillator 26 shown in Figure 2. *McDermott* states that an example of a microprocessor with such a VCO is the MC146805H2 by Motorola. In the MC146805H2, the VCO is an entire ring oscillator variable speed system clock. *McDermott* teaches that the VCO is on the single integrated circuit and provides a clock signal during power up or loss of the crystal signal.

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	*McDermott* teaches a voltage controlled oscillator 26 shown in Figure 2. *McDermott* states that an example of a microprocessor with such a VCO is the MC146805H2 by Motorola. In the MC146805H2, the VCO is an entire ring oscillator variable speed system clock. *McDermott* teaches that the VCO is on the single integrated circuit and provides a clock signal during power up or loss of the crystal signal. *McDermott* teaches that he processing frequency capability of the CPU and speed of the ring oscillator vary according manufacturing variations, voltage and temperature. *McDermott* teaches that during the loss of an external crystal signal, a reference voltage is used to control the frequency and should be chosen relative to the process variations: "A voltage reference suitable for this application should have a relatively stable output over the specified temperature range of microcomputer 10 and should be relatively stable over variations in the process used to manufacture the integrated circuit." Col. 5, lines 11-18. VCO 26 in Figure 2 provide a system clock signal during power up or loss of the crystal signal. This operation is described below: "Whenever logic 22 detects the powering-up of the microcomputer 10, or the loss of the crystal reference signal, or the occurrence of other events described below, the FILTEN signal is negated causing the output of loop filter 24 to disconnect from the input of VCO 26, and the REFEN signal is asserted causing the output of the voltage reference circuit 25 to connect to the input of VCO 26. Thus, the operation of VCO 26 is no longer dependent on the control voltage signal produced by loop filter 24 to determine its operating frequency. Instead, the operating frequency of VCO 26 is determined solely by the chosen output voltage of the voltage reference circuit 25. The reference

	voltage will usually, but not necessarily, be chosen to provide a much lower frequency VCOCLK than is provided in normal operation. The purpose is not to maintain system operation as if the crystal signal had not been lost, but to provide a fall-back mode of operation in which microcomputer 10 can either perform an orderly shutdown or continue to operate at a much-reduced level of capacity." Col. 4, ll. 58-col. 5, ll. 10.
connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	Figure 1 shows a serial I/O interface 13. "Serial interface 13 and timer 15 are each coupled to a number of pins, or connectors, for communication with devices external to microcomputer 10." Col. 3, ll. 27-29.
clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	TPL has asserted that any serial interface satisfies this limitation. Figure 1 of *McDermott* shows a serial I/O interface 13.

I. U.S. Patent No. 4,689,581 issued to *Talbot*

United States Patent No. 4,689,581 issued to *Talbot* (Exhibit 5) on August 25, 1987. As a result, *Talbot* is prior art against *Moore* under 35 U.S.C. § 102(b). *Talbot* discloses a phase locked loop and teaches that the timing pulses it generates may be used by a microcomputer of the type described in European patent application 83307078.2 (EP application). The EP application was published, indexed by its application number, and available to the public on July 18, 1984. EP Publication No. 0 113 516 is attached as Exhibit 5. The microcomputer disclosed by the EP application is shown below.

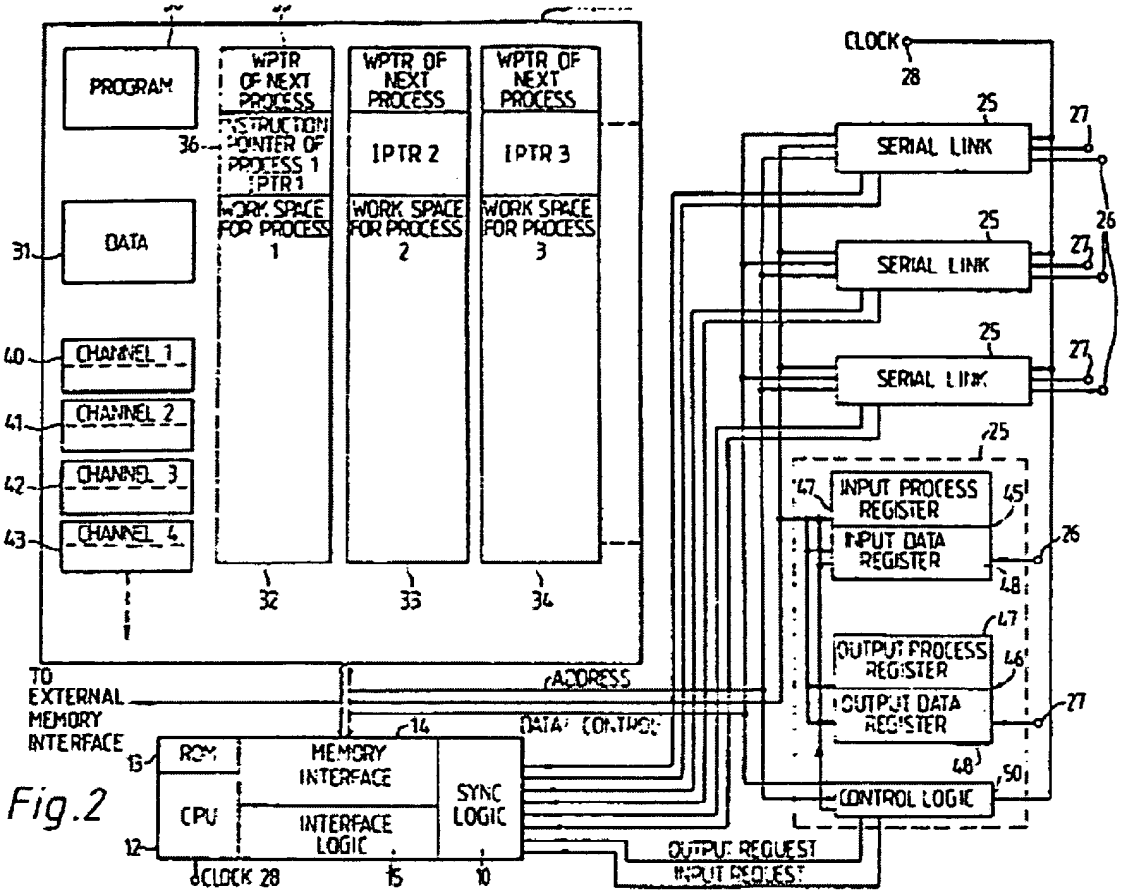


Fig.2

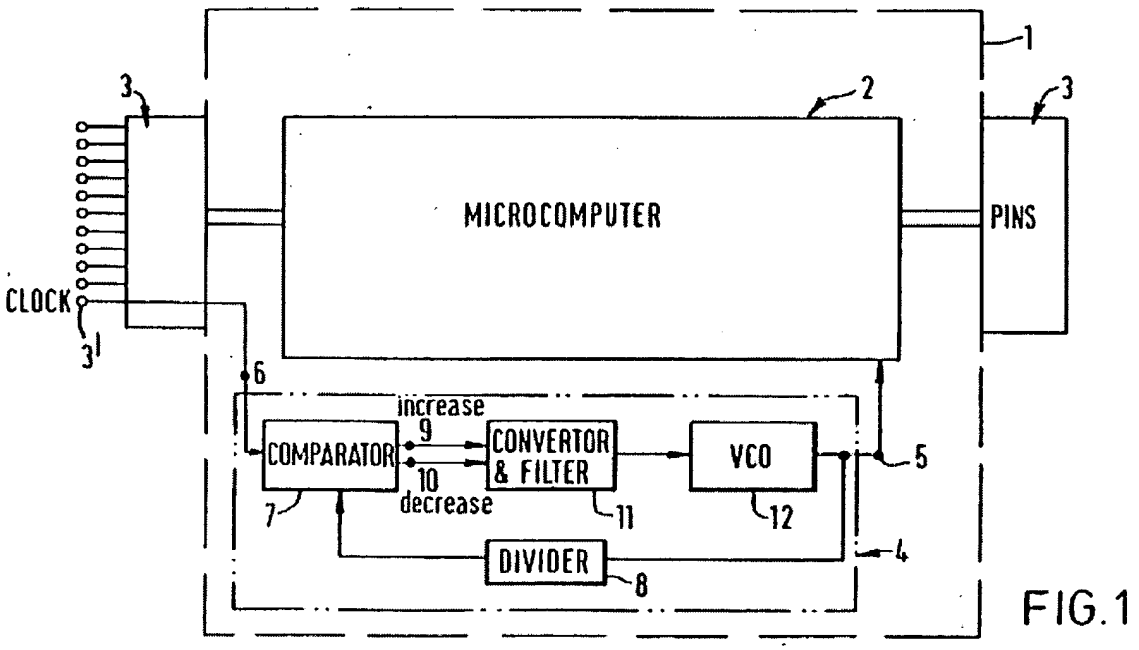


FIG.1

For anticipation purposes, the EP application is incorporated into *Talbot* and its teachings together with those explicitly made in *Talbot* can establish anticipation. *See Advanced Display Sys., Inc. v. Kent State University*, 212 F.3d 1272, 1282 (Fed. Cir. 2000). The microprocessor system in the EP application is manufactured on a single silicon chip that includes a CPU. *Talbot* teaches that a phase-locked loop (PLL) is included on chip including a ring oscillator as

part of a voltage controlled oscillator. Fig. 1; col. 2, ll. 34-35 and 43-45. The microprocessor system of the EP application, which is clocked by *Talbot*'s PLL includes on-chip input/output interface that is clocked by an independent clock signal 22. Figure 1 of *Talbot* shows the PLL 4 on the same chip 1 with the microprocessor system 2.

In addition, FIG. 15 of the EP application above shows the on-chip input/output interface.

J. *Talbot* Raises a Substantial New Question of Patentability

Substantial new questions regarding the patentability of *Moore* exist in light of *Talbot*, which was not referenced by the Examiner. Requestor respectfully submits that *Talbot* teaches every element of claims 1-10 of *Moore*, as explained above. For the Commissioner's convenience, claim charts mapping claims 1-10 of *Moore* to the teachings of *Talbot* are provided below.

Claim 1 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,689,581 to *Talbot* et al. issued August 25, 1987**
A microprocessor system, comprising a single integrated circuit including	*Talbot* incorporates the teachings of European application 83307078.2, which teaches a microprocessor system comprising a single integrated circuit. "The microcomputer described herein is an example of a Transputer microcomputer and comprises a single silicon chip having both a processor and a memory as well as links to permit external communications." p. 2, ll. 45-47.
a central processing unit and	The European application teaches that the microprocessor system comprises a central processing unit. See Figs. 1-2; p. 4, line 15.
an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	*Talbot* shows a PLL with an ring oscillator on-chip. Fig. 1; col. 2, ll. 34-35 and 43-45. The PLL includes a VCO which comprises a series of inverting elements that connect in a loop to form a ring oscillator. Fig. 3. The PLL is connected to the CPU and clocks the CPU. Fig. 1.
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	Both *Talbot* and the European Application describe that their components are manufactured on a single integrated circuit chip and thus of the same process technology. *Talbot*, Fig. 1; col. 2, ll. 34-35 and 43-45; The European application, p. 2.
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations	As a result of being manufactured on the same integrated circuit as the microprocessor, the oscillator varies together with operating characteristics of electronic devices included

and due to at least operating voltage and temperature of said single integrated circuit;	within the microprocessor.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;	The European application describes an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit. Fig. 1; col. 4, ll. 54-56. In Fig. 1, a processor bus 16 interconnects the CPU and the serial output/input interface 25. Coupling control signals are described in The European application at p. 29, ll. 34-38.
and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	The input/output receives a second external clock signal. Fig. 15 of The European application shows the on-chip input/output interface receiving clock signal 22.

Claim 2 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,689,581 to *Talbot* et al. issued August 25, 1987**
The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	According to TPL, "in serial communications the transmitting device sends data and clock at a fixed frequency." See Exhibit 13 at 10. This would include the serial interface of *Talbot*.

Claim 3 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,689,581 to *Talbot* et al. issued August 25, 1987**
In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:	*Talbot* incorporates the teachings of European application 83307078.2, which teaches a microprocessor system comprising an single integrated circuit. "The microcomputer described herein is an example of a Transputer microcomputer and comprises a single silicon chip having both a processor and a memory as well as links to permit external communications. p. 2, ll. 45-47.

providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;	The European application teaches that the microprocessor system comprises a central processing unit. See Figs. 1-2; p. 4, line 15.
using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;	*Talbot* shows a PLL with an ring oscillator on-chip. Fig. 1; col. 2, ll. 34-35 and 43-45. The PLL includes a VCO which comprises a series of inverting elements that connect in a loop to form a ring oscillator. Fig. 3. The PLL is connected to the CPU and clocks the CPU. Fig. 1.
providing an on chip input/output interface for the microprocessor integrated circuit; and	Both *Talbot* and the European application describe that their components are manufactured on a single integrated circuit chip and thus of the same process technology. *Talbot,* Fig. 1; col. 2, ll. 34-35 and 43-45; The European application, p. 2, ll. 45-47.
clocking the input/output interface with a second clock independent of the ring oscillator system clock.	As a result of being manufactured on the same integrated circuit as the microprocessor, the oscillator varies together with operating characteristics of electronic devices included within the microprocessor.

Claim 4 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,689,581 to *Talbot* et al. issued August 25, 1987**
The method of claim 3 in which the second clock is a fixed frequency clock.	According to TPL, "in serial communications the transmitting device sends data and clock at a fixed frequency." See Exhibit 13 at 10. This would include the serial interface of *Talbot.*

Claim 5 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,689,581 to *Talbot* et al. issued August 25, 1987**
The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would

	include the serial interface disclosed by Hill.

Claim 6 of the '336 Patent	ANTICIPATION U.S. Patent No. 4,689,581 to *Talbot* et al. issued August 25, 1987
A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;	*Talbot* incorporates the teachings of European application 83307078.2, which teaches a microprocessor system comprising an single integrated circuit. "The microcomputer described herein is an example of a Transputer microcomputer and comprises a single silicon chip having both a processor and a memory as well as links to permit external communications. p. 2, ll. 45-47.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	The European application teaches that the microprocessor system comprises a central processing unit. See Figs. 1-2; p. 4, line 15.
an on-chip input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	*Talbot* shows a PLL with an ring oscillator on-chip. Fig. 1; col. 2, ll. 34-35 and 43-45. The PLL includes a VCO which comprises a series of inverting elements that connect in a loop to form a ring oscillator. Fig. 3. The PLL is connected to the CPU and clocks the CPU. Fig. 1.
an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	Both *Talbot* and the European application describe that their components are manufactured on a single integrated circuit chip and thus of the same process technology. *Talbot,* Fig. 1; col. 2, ll. 34-35 and 43-45; The European application, p. 2, ll. 45-47.

Claim 7 of the '336 Patent	ANTICIPATION U.S. Patent No. 4,689,581 to *Talbot* et al. issued August 25, 1987
The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	TPL has asserted in its infringement contentions that any on-chip ring oscillator satisfies this limitation. This would include the on-chip ring oscillator of *Talbot*.

Claim 8 of the '336 Patent	ANTICIPATION U.S. Patent No. 4,689,581 to *Talbot* et al. issued August 25, 1987
The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.	TPL has asserted in its infringement contentions that any serial interface satisfies this limitation. This would include the serial interface taught by the European application.

Claim 9 of the '336 Patent	ANTICIPATION U.S. Patent No. 4,689,581 to *Talbot* et al. issued August 25, 1987
The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	*Talbot* describes that the PLL includes a VCO which comprises a series of inverting elements that connect in a loop to form a ring oscillator. Fig. 3.

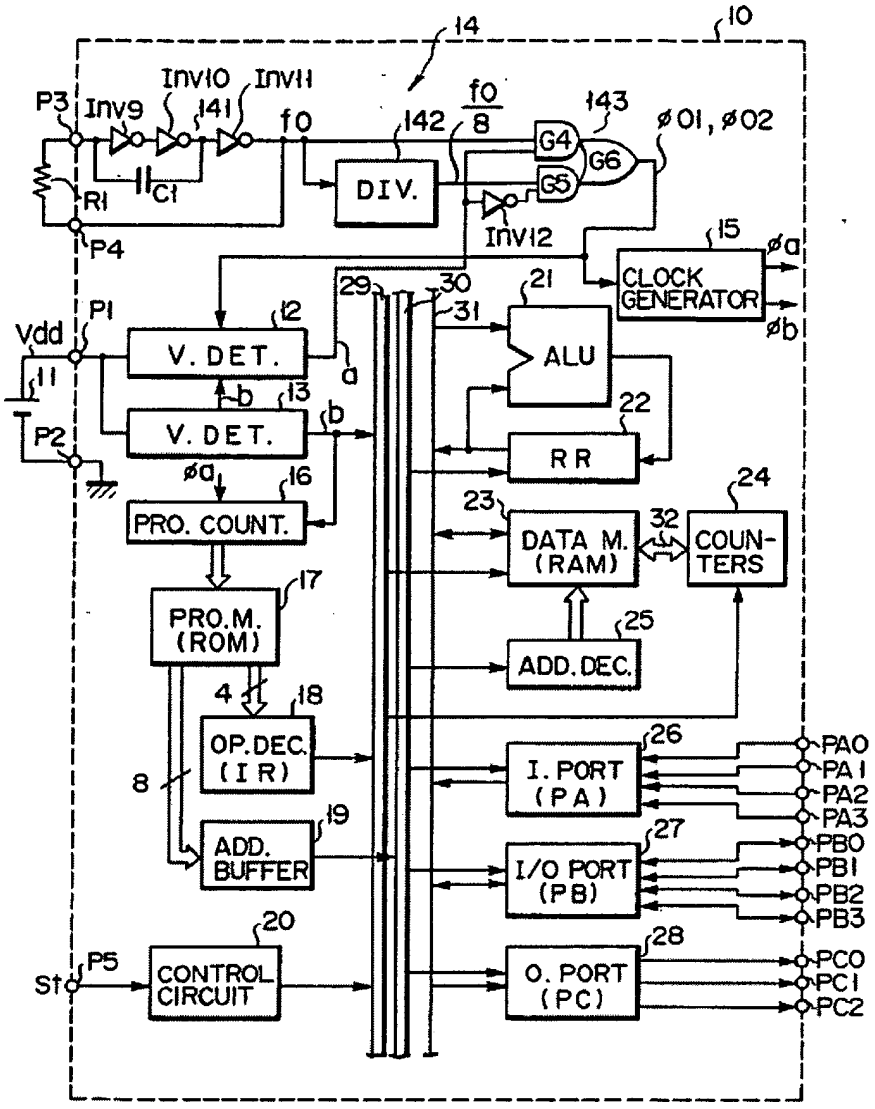
Claim 10 of the '336 Patent	ANTICIPATION U.S. Patent No. 4,689,581 to *Talbot* et al. issued August 25, 1987
In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of: providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	*Talbot* incorporates the teachings of European application 83307078.2, which teaches a microprocessor system comprising an single integrated circuit. The microcomputer by The European application is an example of a Transputer microcomputer and comprises a single silicon chip having both a processor and a memory as well as links to permit external communications. The European application at p. 2.
providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	*Talbot* shows a PLL with an ring oscillator on-chip. Fig. 1; col. 2, ll. 34-35 and 43-45. The PLL includes a VCO which comprises a series of inverting elements that connect in a loop to form a ring oscillator. Fig. 3. The PLL is

	connected to the CPU and clocks the CPU. Fig. 1.
clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	*Talbot* shows a PLL with an ring oscillator on-chip. Fig. 1; col. 2, ll. 34-35 and 43-45. The PLL includes a VCO which comprises a series of inverting elements that connect in a loop to form a ring oscillator. Fig. 3. Both *Talbot* and the European application describe that their components are manufactured on a single integrated circuit chip and thus of the same process technology. *Talbot,* Fig. 1; col. 2, ll. 34-35 and 43-45; the European application, p. 2. The PLL is connected to the CPU and clocks the CPU. Fig. 1.
connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	The European application describes an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit. Fig. 1; col. 4, ll. 54-56. In Fig. 1, a processor bus 16 interconnects the CPU and the serial output/input interface 25. Coupling control signals are described in the European application at p. 70-71.
clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	The input/output receives a second external clock signal. Fig. 15 of the European application shows the on-chip input/output interface receiving clock signal 22.

K. U.S. Patent No. 4,766,567 issued to *Kato*

United States Patent No. 4,766,567 issued to *Kato* (Exhibit 6) from an application filed on April 11, 1985. As a result, *Kato* is prior art against *Moore* under 35 U.S.C. § 102(e). *Kato* discloses a processor provided on a single integrated circuit and teaches that an on-chip ring oscillator can be used to clock the processor. *See* Fig. 4; col. 10, line 67 - col. 11, line 2. *Kato*'s single chip processor is disclosed as also including an I/O interface including an I/O port. The ring oscillator signal, however, is only supplied to the processor so that the I/O port is taught as being clocked by an independent clock. FIG. 4 of *Kato*, reproduced below shows the processor 21-25 and the ring oscillator 141, together with the I/O port 27.

F I G. 4



L. *Kato* Raises a Substantial New Question of Patentability

Substantial new questions regarding the patentability of *Moore* exist in light of *Kato*, which was not referenced by the Examiner. Requestor respectfully submits that *Kato* teaches every element of claims 1-10 of *Moore*, as explained above. For the Commissioner's convenience, claim charts mapping claims 1-10 of *Moore* to the teachings of *Kato* are provided below.

Claim 1 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,766,567 to *Kato* Issued August 23, 1988.**
A microprocessor system, comprising a single	The '567 patent describes a single integrated

integrated circuit including a central processing unit	circuit microprocessor having a central processing unit. See col. 1, ll. 6-10; col. 4, ll. 63-68.
and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	The '567 patent describes an on-chip ring oscillator in Figure 4. Oscillator 141 contains an odd number of inverting stages comprising a ring oscillator. *Kato* discloses that oscillator 141 can be replaced by a ring oscillator that is "completely built on the semiconductor substrate 10." Col. 10, line 67 - col. 11, line 2.
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	The '567 patent discloses that the ring oscillator is disposed on the same circuit substrate as the CPU. The '567 patent also discloses that the on chip ring oscillator will vary according voltage. Col. 10, line 63 - col. 11, line 7. According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;	The '567 patent discloses a PIO interface. It is well known in the art that a PIO interface may also be used as a serial or SIO interface.
and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	If a PIO interface is used as an SIO interface, it is clocked by a second clock independent of the ring oscillator.

Claim 2 of the '336 Patent	**ANTICIPATION U.S. Patent No. 4,766,567 to *Kato* Issued August 23, 1988.**
The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	According to TPL, "in serial communications the transmitting device sends data and clock at a fixed frequency." See Exhibit 13 at 10. This would include the PIO interface of *Kato*.

Claim 3 of the '336 Patent	**ANTICIPATION U.S. Patent No. 4,766,567 to *Kato* Issued**

	August 23, 1988.
In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:	The '567 patent describes a single integrated circuit microprocessor having a central processing unit. See col. 1, ll. 6-10; col. 4, ll. 63-68.
providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;	The '567 patent describes an on-chip ring oscillator in Figure 1. Oscillator 141 contains an odd number of inverting stages comprising a ring oscillator. *Kato* discloses that oscillator 141 can be replaced by a ring oscillator that is "completely built on the semiconductor substrate 10." Col. 10, line 67 - col. 11, line 2. The '567 patent discloses that the ring oscillator is disclosed on the same circuit substrate as the CPU. The '567 patent also discloses that the on chip ring oscillator will vary according voltage. Col. 10, line 63 - col. 11, line 7. According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;	The '567 patent discloses that the ring oscillator is disposed on the same circuit substrate as the CPU. The '567 patent also discloses that the on chip ring oscillator will vary according voltage. Col. 10, line 63 - col. 11, line 7. The microprocessor operates at a variable processing speed depending on the speed of the ring oscillator.
providing an on chip input/output interface for the microprocessor integrated circuit; and	The '567 patent discloses a PIO interface. It is well known in the art that a PIO interface may also be used as a serial or SIO interface.
clocking the input/output interface with a second clock independent of the ring oscillator system clock.	If a PIO interface is used as an SIO interface, it can be clocked by a second clock independent of the ring oscillator.

Claim 4 of the '336 Patent	ANTICIPATION U.S. Patent No. 4,766,567 to *Kato* Issued August 23, 1988.
The method of claim 3 in which the second clock is a fixed frequency clock.	According to TPL, "in serial communications the transmitting device sends data and clock at a fixed frequency." See Exhibit 13 at 10. This would include the PIO interface of *Kato*.

Claim 5 of the '336 Patent	ANTICIPATION U.S. Patent No. 4,766,567 to *Kato* Issued August 23, 1988.
The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would include a serial interface.

Claim 6 of the '336 Patent	ANTICIPATION U.S. Patent No. 4,766,567 to *Kato* Issued August 23, 1988.
A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;	The '567 patent describes a single integrated circuit microprocessor having a central processing unit. See col. 1, ll. 6-10; col. 4, ll. 63-68.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,	The '567 patent describes an on-chip ring oscillator in Figure 1. Oscillator 141 contains an odd number of inverting stages comprising a ring oscillator. *Kato* discloses that oscillator 141 can be replaced by a ring oscillator that is "completely built on the semiconductor substrate 10." Col. 10, line 67 - col. 11, line 2.
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	The '567 patent discloses that the ring oscillator is disposed on the same circuit substrate as the CPU. The '567 patent also discloses that the on chip ring oscillator will vary according voltage. Col. 10, line 63 - col. 11, line 7. According to TPL, because of "the laws of physics and the state of the art of

	microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
an on-chip input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	The '567 patent discloses a PIO interface. It is well known in the art that a PIO interface may also be used as a serial or SIO interface.
an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	If a PIO interface is used as an SIO interface, it can be clocked by a second clock independent of the ring oscillator.

Claim 7 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,766,567 to *Kato* Issued August 23, 1988.**
The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	The '567 patent discloses that the ring oscillator is disposed on the same circuit substrate as the CPU. The '567 patent also discloses that the on chip ring oscillator will vary according voltage. Col. 10, line 63 - col. 11, line 7. According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.

Claim 8 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,766,567 to *Kato* Issued August 23, 1988.**
The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would

relative to said oscillator.	include the PIO interface of the '567 patent.

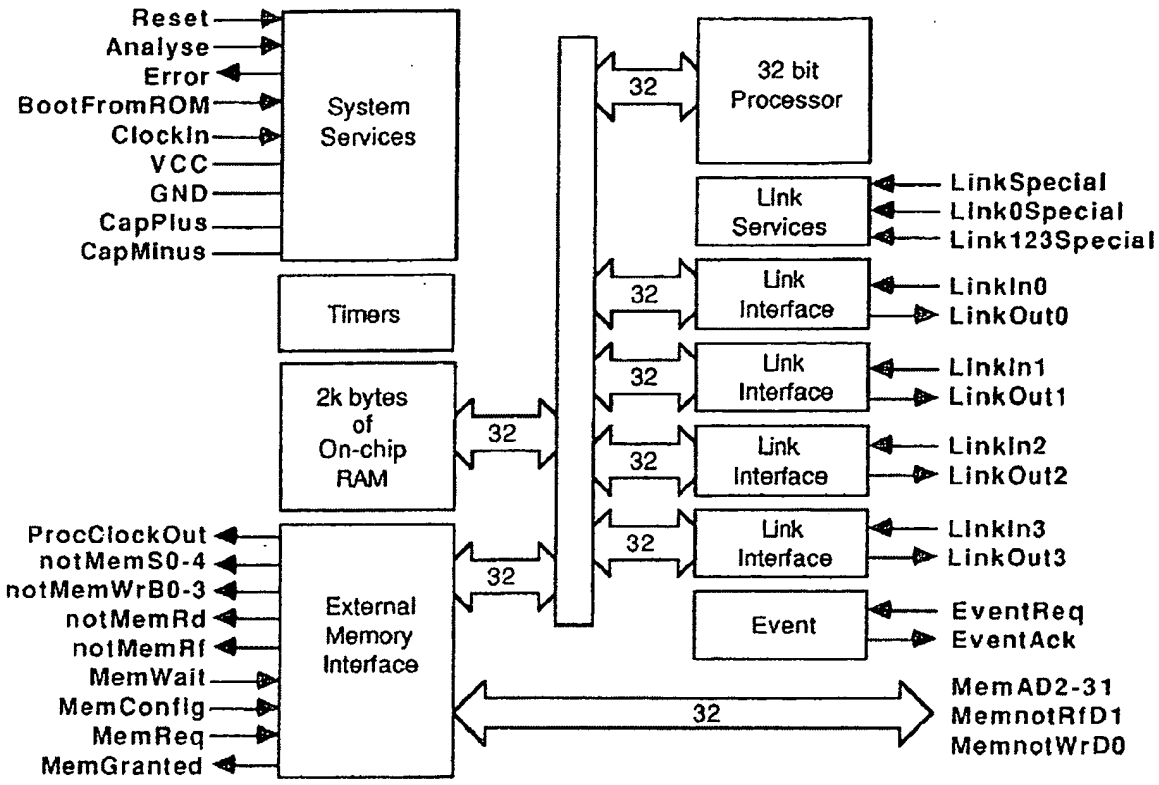
Claim 9 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,766,567 to *Kato* Issued August 23, 1988.**
The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	The '567 patent discloses that the ring oscillator is disposed on the same circuit substrate as the CPU. The '567 patent also discloses that the on chip ring oscillator will vary according voltage. Col. 10, line 63 - col. 11, line 7.

Claim 10 of the '336 Patent	**ANTICIPATION** **U.S. Patent No. 4,766,567 to *Kato* Issued August 23, 1988.**
In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of: providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	The '567 patent describes a single integrated circuit microprocessor having a central processing unit. See col. 1, ll. 6-10; col. 4, ll. 63-68.
providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	The '567 patent describes an on-chip ring oscillator in Figure 1. Oscillator 141 contains an odd number of inverting stages comprising a ring oscillator. *Kato* discloses that oscillator 141 can be replaced by a ring oscillator that is "completely built on the semiconductor substrate 10." Col. 10, line 67 - col. 11, line 2.

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	The '567 patent discloses that the ring oscillator is disclosed on the same circuit substrate as the CPU. The '567 patent also discloses that the on chip ring oscillator will vary according voltage. Col. 10, line 63 - col. 11, line 7. The microprocessor operates at a variable processing speed depending on the speed of the ring oscillator. According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	The '567 patent discloses a PIO interface for exchanging control signals, addresses, and data with the CPU. It is well known in the art that a PIO interface may also be used as a serial or SIO interface.
clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	If a PIO interface is used as an SIO interface, it can be clocked by a second clock independent of the ring oscillator.

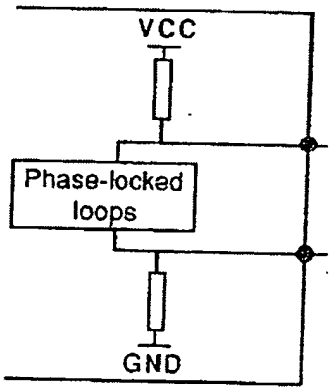
G. T414M Transputer Publication

In a publication from August 1987, a microprocessor called the T414M Transputer was disclosed which contained an on-chip phase-locked-loop for clocking the microprocessor and an on-chip link interface that can be clocked by a second external clock. Engineering data IMS T414M transputer, attached as Exhibit 7. This publication is prior art against Moore under 35 U.S.C. § 102(b). The microprocessor system according the publication is shown below. The illustration includes the on-chip link interfaces and the CPU or 32-bit processor.



IMS T414M Block Diagram

In addition, the phase-locked-loop of the publication is illustrated below (page 13) According to TPL, the "presence of a PLL indicates the presence of a ring oscillator." See Exhibit 13 at 12.



H. The T414M Transputer Publication Raises a Substantial New Question of Patentability

Substantial new questions regarding the patentability of *Moore* exist in light of the T414M Transputer Publication, which was not referenced by the Examiner. Requestor respectfully submits that the T414M Transputer Publication recites every element of claims 1-10 of *Moore*, as explained above. For the Commissioner's convenience, claim charts mapping claims 1-10 of *Moore* to the teachings of the T414M Transputer Publication are provided below.

Claim 1 of the '336 Patent	Engineering data IMS T414M transputer Published August 1987
A microprocessor system, comprising a single integrated circuit including	The T414M teaches a microprocessor system comprising an single integrated circuit. Engineering data IMS T414M transputer at 1.
a central processing unit and	The T414M teaches that the microprocessor system comprises a central processing unit (the 32-bit Processor illustrated above). Id.
an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	The T414M includes an on-chip PLL. Id. at 13. According to TPL, the "presence of a PLL indicates the presence of a ring oscillator." See Exhibit 13 at 12.
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,	The T414M's PLL and CPU are manufactured on a single integrated circuit chip and thus of the same process technology. Id.
a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;	The T414M includes an on-chip serial peripheral interface for exchanging coupling control signals, addresses, and data. Id. at 37-39.
and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	The serial peripheral interface can be connected to a second clock independent of the ring oscillator. "Links are not synchronised with ClockIn or ProcClockOut and are insensitive to their phases. Thus links from independently clocked systems may communicate . . ." Id.

Claim 2 of the '336 Patent	Engineering data IMS T414M transputer Published August 1987
The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	According to TPL, "in serial communications the transmitting device sends data and clock at a fixed frequency." See Exhibit 13 at 10. This would include the serial peripheral interface of

	the T414M.

Claim 3 of the '336 Patent	Engineering data IMS T414M transputer Published August 1987
In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:	The T414M teaches a microprocessor system comprising an single integrated circuit. Engineering data IMS T414M transputer at 1. The T414M includes a method for clocking the microprocessor.
providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;	The T414M includes an on-chip PLL. Id. at 13. According to TPL, the "presence of a PLL indicates the presence of a ring oscillator." See Exhibit 13 at 12. According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;	The T414M's PLL is used for clocking the microprocessor. The microprocessor operates at a variable processing frequency depending on the variable speed of the PLL. Id. at 13.
providing an on chip input/output interface for the microprocessor integrated circuit; and	The T414M includes an on-chip serial peripheral interface for exchanging coupling control signals, addresses, and data. Id. at 37-39.
clocking the input/output interface with a second clock independent of the ring oscillator system clock.	The serial peripheral interface can be connected to a second clock independent of the ring oscillator. "Links are not synchronised with ClockIn or ProcClockOut and are insensitive to their phases. Thus links from independently clocked systems may communicate . . ." Id.

Claim 4 of the '336 Patent	Engineering data IMS T414M transputer Published August 1987

The method of claim 3 in which the second clock is a fixed frequency clock.	According to TPL, "in serial communications the transmitting device sends data and clock at a fixed frequency." See Exhibit 13 at 10. This would include the serial peripheral interface of the T414M.

Claim 5 of the '336 Patent	**Engineering data IMS T414M transputer Published August 1987**
The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would include the serial interface disclosed by the T414M.

Claim 6 of the '336 Patent	**Engineering data IMS T414M transputer Published August 1987**
A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;	The T414M teaches a microprocessor system comprising an single integrated circuit. Engineering data IMS T414M transputer at 1. The T414M teaches that the microprocessor system comprises a central processing unit. Id.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	The T414M includes an on-chip PLL. Id. at 13. According to TPL, the "presence of a PLL indicates the presence of a ring oscillator." See Exhibit 13 at 12. The T414M's PLL and CPU are manufactured on a single integrated circuit chip and thus of the same process technology. Id. According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
an on-chip input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses	The T414M includes an on-chip serial peripheral interface for exchanging coupling control signals, addresses, and data. Id. at 37.

and data with said central processing unit; and	
an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	The serial peripheral interface can be connected to a second clock independent of the ring oscillator. "Links are not synchronised with ClockIn or ProcClockOut and are insensitive to their phases. Thus links from independently clocked systems may communicate . . ." Id.

Claim 7 of the '336 Patent	**Engineering data IMS T414M transputer Published August 1987**
The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.

Operating Conditions

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
VCC	DC supply voltage	4.75		5.25	V	1
VI, VO	Input or output voltage	0		VCC	V	1,2
CL	Load capacitance on any pin			50	pF	
TA	Operating temperature range	-55		125	°C	3

Claim 8 of the '336 Patent	**Engineering data IMS T414M transputer Published August 1987**
The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.	TPL has asserted in its infringement contentions that any serial interface satisfies this limitation. This would include the serial interface taught by the T414M.

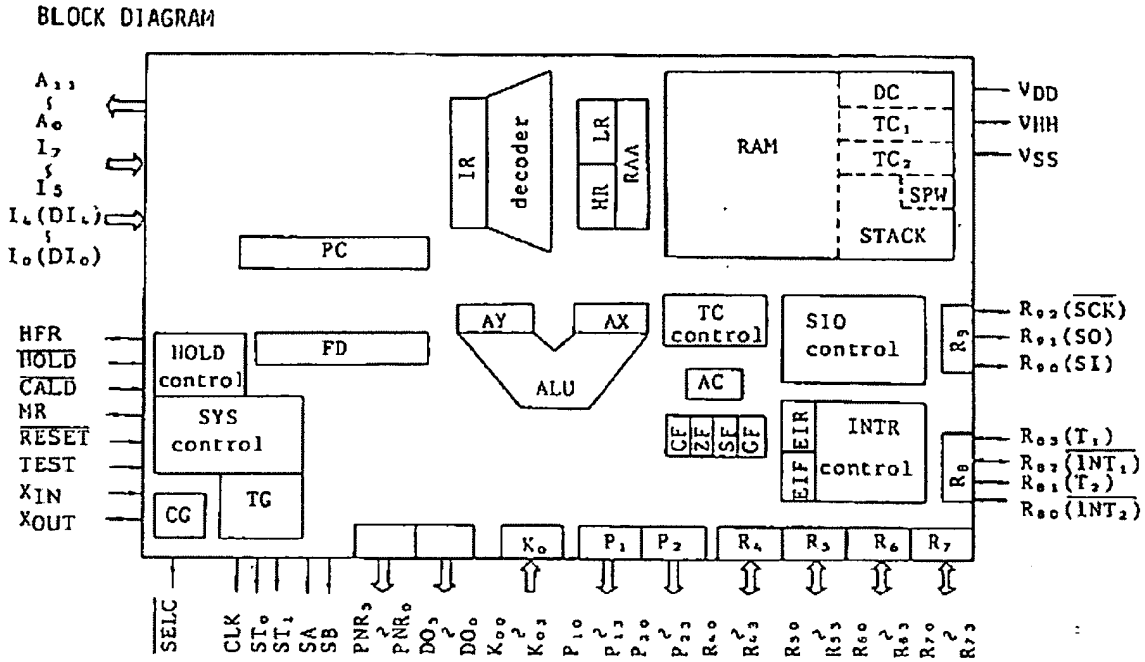
Claim 9 of the '336 Patent	**Engineering data IMS T414M transputer Published August 1987**
The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	The T414M includes an on-chip PLL. Id. at 13. According to TPL, the "presence of a PLL indicates the presence of a ring oscillator." See Exhibit 13 at 12.

Claim 10 of the '336 Patent	**Engineering data IMS T414M transputer Published August 1987**
In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:	The T414M teaches a microprocessor system comprising an single integrated circuit. Engineering data IMS T414M transputer at 1.

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	The T414M teaches that the microprocessor system comprises a central processing unit. Id.
providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	The T414M includes an on-chip PLL. Id. at 13. According to TPL, the "presence of a PLL indicates the presence of a ring oscillator." See Exhibit 13 at 12.
clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	The T414M's PLL and CPU are manufactured on a single integrated circuit chip and thus of the same process technology. Id. According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	The T414M includes an on-chip serial peripheral interface for exchanging coupling control signals, addresses, and data. Id. at 37-39.
clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	The serial peripheral interface can be connected to a second clock independent of the ring oscillator. "Links are not synchronised with ClockIn or ProcClockOut and are insensitive to their phases. Thus links from independently clocked systems may communicate . . ." Id.

I. TLCS-42, 47, 470 User's Manual

The TLCS-42, 47, 470 User's Manual ("Manual") was published in April 1986. See Exhibit 8. As a result, this reference is prior art against Moore under 35 U.S.C. § 102(b). The Manual discloses a 4-bit single chip microprocessor called the TLCS-47 that includes an on-chip clock shown as CG in the figure below. The TLCS-47 also includes an on-chip serial interface that is clocked by a second external clock. The serial interface is controlled by the SIO control shown in the figure and clocked by the SCK signal, which stands for serial clock.



The clock generated in the on-chip clock circuit is independent of the second external clock. In addition, the on-chip clock oscillator circuit is an oscillator which utilizes a single inverter in conjunction with a feedback register as a pair of MOSFETs by connecting X-tal or the resonator to external pins (Xin and Xout). This configuration is shown below.

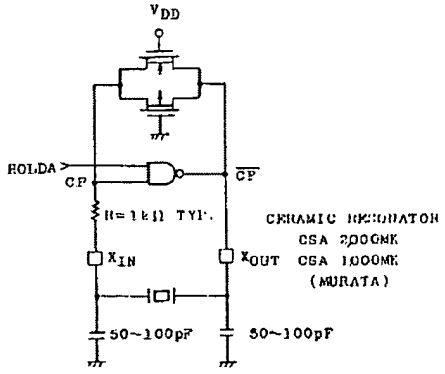
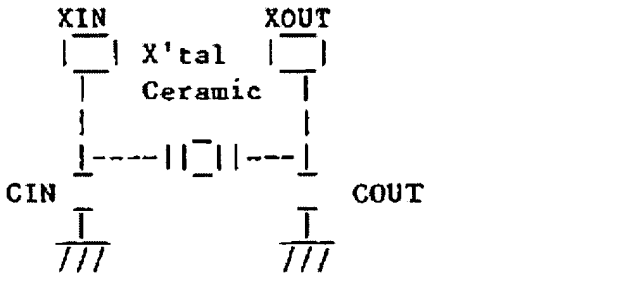


Fig. 3.2 (22) CMOS version Clock Generation Circuit



(a) For X'tal or ceramic resonator

J. The TLCS-42, 47, 470 User's Manual Raises a Substantial New Question of Patentability

Substantial new questions regarding the patentability of *Moore* exist in light of the TLCS-42, 47, 470 User's Manual, which was not referenced by the Examiner. Requestor respectfully submits that the TLCS-42, 47, 470 User's Manual recites every element of claims 1-10 of *Moore*, as explained above. For the Commissioner's convenience, claim charts mapping claims 1-10 of *Moore* to the teachings of the TLCS-42, 47, 470 User's Manual are provided below.

Claim 1 of the '336 Patent	**TLCS-42, 47, 470 User's Manual Published in April 1986.**
A microprocessor system, comprising a single integrated circuit including	The TLCS 47 comprises a single integrated circuit microprocessor. TLCS-42, 47, 470 User's Manual at i (Manual).
a central processing unit and	The TLCS 47 comprises a CPU. Manual at MCU47-118; 191; and 203.
an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	The TLCS 47 includes an on-chip clock oscillator. Manual at vii. An inverter with a resistor is implemented in the TLCS 47 creating a ring oscillator to clock the microprocessor. MCU42-15, and MCU47-117.
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;	The TLCS 47 contains an on chip serial interface (SIO) which can exchange control signals, addresses, and data with the CPU.
and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	The serial interface can be clocked by an external clock source SCK. Manual at MCU47-117; 145.

Claim 2 of the '336 Patent	**TLCS-42, 47, 470 User's Manual Published**

	in April 1986.
The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	According to TPL, "in serial communications the transmitting device sends data and clock at a fixed frequency." See Exhibit 13 at 10. This would include the serial interface of the TLCS 47.

Claim 3 of the '336 Patent	TLCS-42, 47, 470 User's Manual Published in April 1986.
In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:	The TLCS 47 comprises a single integrated circuit and provides a method for clocking the microprocessor. TLCS-42, 47, 470 User's Manual at i (Manual).
providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;	The TLCS 47 includes an on-chip clock oscillator. Manual at vii. An inverter with a resistor is implemented in the TLCS 47 creating a ring oscillator to clock the microprocessor. MCU42-15, and MCU47-117. According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;	The TLCS 47 includes an on-chip clock oscillator. Manual at vii. An inverter with a resistor is implemented in the TLCS 47 creating a ring oscillator to clock the microprocessor. MCU42-15, and MCU47-117.
providing an on chip input/output interface for the microprocessor integrated circuit; and	The TLCS 47 contains an on chip serial interface (SIO) which can exchange control signals, addresses, and data with the CPU.
clocking the input/output interface with a	The serial interface can be clocked by an

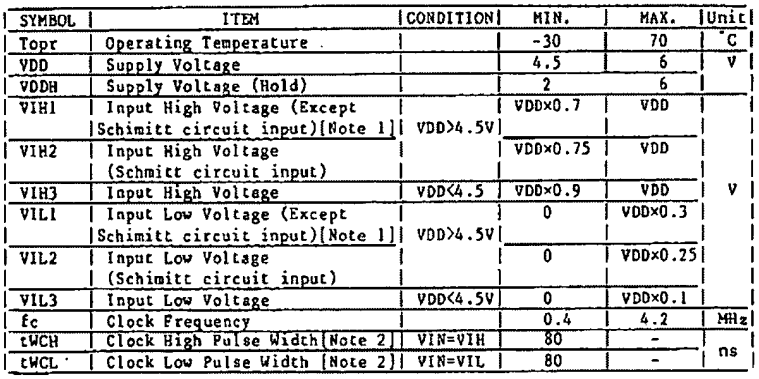
second clock independent of the ring oscillator system clock.	external clock source SCK. Manual at MCU47-117; 145.

Claim 4 of the '336 Patent	TLCS-42, 47, 470 User's Manual Published in April 1986.
The method of claim 3 in which the second clock is a fixed frequency clock.	According to TPL, "in serial communications the transmitting device sends data and clock at a fixed frequency." See Exhibit 13 at 10. This would include the serial interface of the TLCS 47.

Claim 5 of the '336 Patent	TLCS-42, 47, 470 User's Manual Published in April 1986.
The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would include the serial interface of TLCS 47.

Claim 6 of the '336 Patent	TLCS-42, 47, 470 User's Manual Published in April 1986.
A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;	The TLCS 47 comprises a single integrated circuit microprocessor. TLCS-42, 47 470 User's Manual at i (Manual). The TLCS 47 comprises a CPU. Manual at MCU47- 118; 191; and 203.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,	The TLCS 47 includes an on-chip clock oscillator. Manual at vii. An inverter with a resistor is implemented in the TLCS 47 creating a ring oscillator to clock the microprocessor. MCU42-15, and MCU47-117.
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.

an on-chip input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	The TLCS 47 contains an on chip serial interface (SIO) which can exchange control signals, addresses, and data with the CPU.
an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	The serial interface can be clocked by an external clock source SCK. Manual at MCU47-102; 117; 145.

Claim 7 of the '336 Patent	**TLCS-42, 47, 470 User's Manual Published in April 1986.**
The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6. MCU47- 185 and 186: 

SYMBOL	ITEM	CONDITION	MIN.	MAX.	Unit
Topr	Operating Temperature		-30	70	°C
VDD	Supply Voltage		4.5	6	V
VDDH	Supply Voltage (Hold)		2	6	
VIH1	Input High Voltage (Except Schimitt circuit input)[Note 1]	VDD>4.5V	VDD×0.7	VDD	V
VIH2	Input High Voltage (Schmitt circuit input)		VDD×0.75	VDD	
VIH3	Input High Voltage	VDD<4.5	VDD×0.9	VDD	
VIL1	Input Low Voltage (Except Schimitt circuit input)[Note 1]	VDD>4.5V	0	VDD×0.3	
VIL2	Input Low Voltage (Schimitt circuit input)		0	VDD×0.25	
VIL3	Input Low Voltage	VDD<4.5V	0	VDD×0.1	
fc	Clock Frequency		0.4	4.2	MHz
tWCH	Clock High Pulse Width[Note 2]	VIN=VIH	80	-	ns
tWCL	Clock Low Pulse Width [Note 2]	VIN=VIL	80	-	

A.C. CHARACTERISTICS (VSS=0V, VDD=5V±10%, Topr=-30 to 70°C)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
tcy	Instruction Cycle Time		1.9	--	20	μs
tSDH	Shift Data Hold Time	(Note 1)	0.5tcy - 300	--	--	ns

Claim 8 of the '336 Patent	**TLCS-42, 47, 470 User's Manual Published in April 1986.**
The microprocessor system of claim 6 wherein said external clock comprises a fixed-	TPL has asserted that any information transfer over a microprocessor interface satisfies this

frequency clock which operates synchronously relative to said oscillator.	limitation. See Exhibit 12 at 29. This would include the serial interface of TLCS 47.

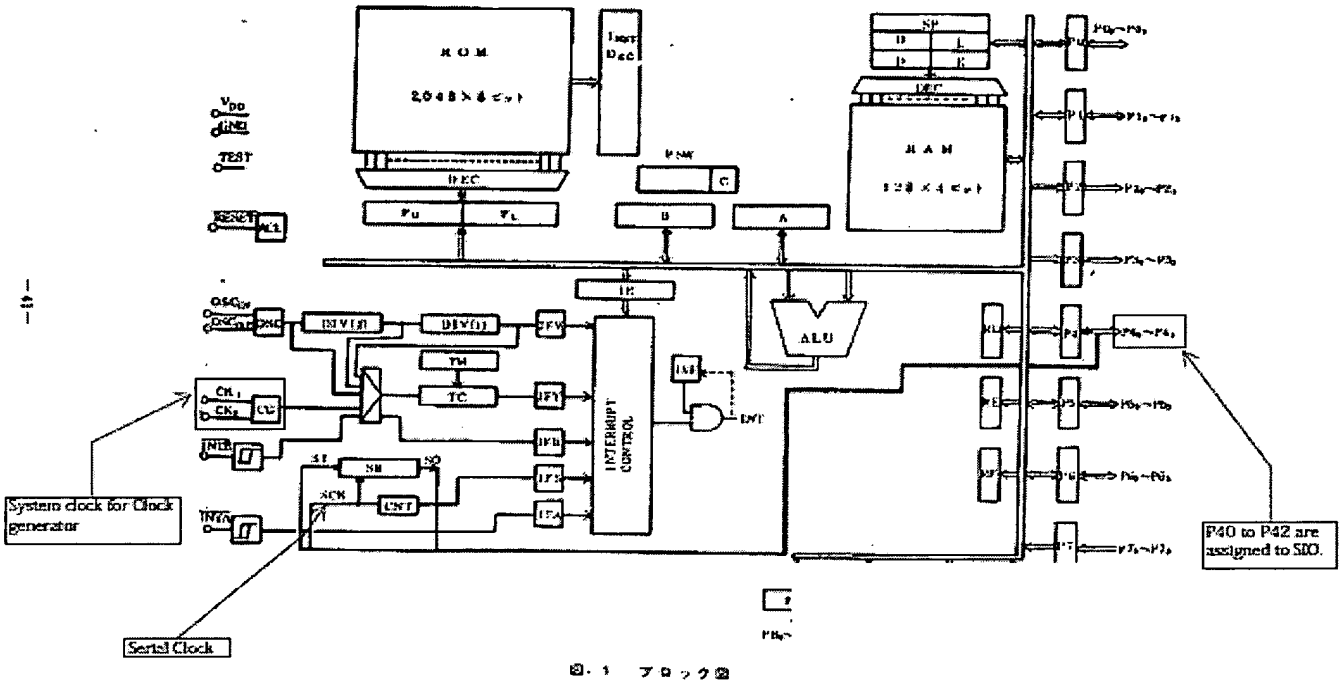
Claim 9 of the '336 Patent	**TLCS-42, 47, 470 User's Manual Published in April 1986.**
The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	The TLCS 47 includes an on-chip clock oscillator. Manual at vii. An inverter with a resistor is implemented in the TLCS 47 creating a ring oscillator to clock the microprocessor. MCU42-15, and MCU47-117.

Claim 10 of the '336 Patent	**TLCS-42, 47, 470 User's Manual Published in April 1986.**
In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of: providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	The TLCS 47 comprises a single integrated circuit microprocessor. TLCS-42, 47, 470 User's Manual at i (Manual). The TLCS 47 comprises a CPU. Manual at MCU47-118; 191; and 203.
providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	The TLCS 47 includes an on-chip clock oscillator. Manual at vii. An inverter with a resistor is implemented in the TLCS 47 creating a ring oscillator to clock the microprocessor. MCU42-15, and MCU47-117.

clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	The TLCS 47 includes an on-chip clock oscillator. Manual at vii. An inverter with a resistor is implemented in the TLCS 47 creating a ring oscillator to clock the microprocessor. MCU42-15, and MCU47-117. According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	The TLCS 47 contains an on chip serial interface (SIO) which can exchange control signals, addresses, and data with the CPU.
clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	The serial interface can be clocked by an external clock source SCK. Manual at MCU47-117; 145.

K. The SM550 High Speed CMOS 4-bit Microcomputer SM-550 Series Publication

The article, SM550 High Speed CMOS 4-bit Microcomputer SM-550 Series ("SM550), was published in 1982, 1983. See Exhibit 9. As a result, the SM550 is prior art against the Moore patent under 35 U.S.C. § 102(b). These documents were originally published in Japanese and an English language translation has been attached as Exhibit 9 for the convenience of the Patent Office. The SM550 discloses a microprocessor system (shown below) including a CPU, an on-chip oscillator (shown as CG), and an on-chip serial interface. The on-chip oscillator (CG) can be configured as ring oscillator by connecting a resistor and capacitor to form a ring. In addition, the on-chip serial interface can be clocked by an external serial clock, SCK.



L. The SM550 Raises a Substantial New Question of Patentability

Substantial new questions regarding the patentability of *Moore* exist in light of the SM550 Publication, which was not referenced by the Examiner. Requestor respectfully submits that the SM550 Publication recites every element of claims 1-10 of *Moore*, as explained above. For the Commissioner's convenience, claim charts mapping claims 1-10 of *Moore* to the teachings of the SM550 Publication are provided below.

Claim 1 of the '336 Patent	**SM550 High Speed CMOS 4-bit Microcomputer SM-550 Series Publication**
A microprocessor system, comprising a single integrated circuit including a central processing unit	The SM550 is a 4-bit microcomputer with integrated serial I/O and oscillator. SM550 High Speed CMOS 4-bit Microcomputer SM-

	550 Series at 41, 108. The Figure on pages 41, 108 show the CPU of the SM550.
and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	The SM550 contains an on-chip CR oscillator shown as "CG" in the figure on pages 45 and 108. Pages 45 and 108 describe a configuration of the CR oscillator as a ring oscillator. An external resistor "R" is connected between inputs CK1 and CK2 to control a system frequency. Id. at 45, 108.
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6. The tables on pages 46, 109 show the microprocessor operating frequency varying with voltage. Id.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;	The SM550 has a serial interface (SIO) that can input/output data using an external serial clock. Id.
and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	The SM550 teaches a second serial clock for clocking the serial interface. The SM550 has a serial interface (SIO) that can input/output data based on an external serial clock.

Claim 2 of the '336 Patent	**SM550 High Speed CMOS 4-bit Microcomputer SM-550 Series Publication**
The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	A SM550 discusses the use of a "serial clock." According to TPL, "in serial communications the transmitting device sends data and clock at a fixed frequency." See Exhibit 13 at 10.

Claim 3 of the '336 Patent	**SM550 High Speed CMOS 4-bit Microcomputer SM-550 Series Publication**
In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:	The SM550 is a 4-bit microcomputer with integrated serial I/O and oscillator. Id. at 45, 108.

providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;	The SM550 contains an on-chip CR oscillator shown as "CG" in the figure on pages 45, 108. Pages 45 and 108 describe a configuration of the CR oscillator as a ring oscillator. An external resistor "R" is connected between inputs CK1 and CK2 to control a system frequency. Id. at 45, 108 According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6. The tables on pages 45, 109 show the microprocessor operating frequency varying with voltage. Id.
using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;	The SM550 identifies an on-chip system clock oscillator. Id. at 45, 108. The processing frequency of the microprocessor will operate at a variable frequency depending on the speed of the ring oscillator.
providing an on chip input/output interface for the microprocessor integrated circuit; and	The SM550 has a serial interface (SIO) that can input/output data using an external serial clock. Id.
clocking the input/output interface with a second clock independent of the ring oscillator system clock.	The SM550 teaches a second serial clock for clocking the serial interface. The SM550 has a serial interface (SIO) that can input/output data based on an external serial clock.

Claim 4 of the '336 Patent	**SM550 High Speed CMOS 4-bit Microcomputer SM-550 Series Publication**
The method of claim 3 in which the second clock is a fixed frequency clock.	A SM550 discusses the use of a "serial clock." According to TPL, "in serial communications the transmitting device sends data and clock at a fixed frequency." See Exhibit 13 at 10.

Claim 5 of the '336 Patent	SM550 High Speed CMOS 4-bit Microcomputer SM-550 Series Publication
The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. See See Exhibit 12 at 29. This would include the serial interface of the SM550.

Claim 6 of the '336 Patent	SM550 High Speed CMOS 4-bit Microcomputer SM-550 Series Publication
A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;	The SM550 is a 4-bit microcomputer with integrated serial I/O and oscillator. Id. at 45, 108.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,	The SM550 contains an on-chip CR oscillator shown as "CG" in the figure on pages 45 and 108. Pages 45 and 108 describes a configuration of the CR oscillator as a ring oscillator. An external resistor "R" is connected between inputs CK1 and CK2 to control a system frequency. Id. at 45, 108
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6. The tables on pages 46, 109 show the microprocessor operating frequency varying with voltage. Id.
an on-chip input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	The SM550 teaches a serial interface (SIO) that can input/output data using an external serial clock. Id.
an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is	The SM550 teaches a second serial clock for clocking the serial interface. The SM550 has a serial interface (SIO) that can input/output data

operative at a frequency independent of a clock frequency of said oscillator.	based on an external serial clock.

Claim 7 of the '336 Patent	SM550 High Speed CMOS 4-bit Microcomputer SM-550 Series Publication
The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6. The tables on pages 46, 109 show the microprocessor operating frequency varying with voltage. Id.

Claim 8 of the '336 Patent	SM550 High Speed CMOS 4-bit Microcomputer SM-550 Series Publication
The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would include the serial interface of the SM550.

Claim 9 of the '336 Patent	SM550 High Speed CMOS 4-bit Microcomputer SM-550 Series Publication
The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	The SM550 contains an on-chip CR oscillator shown as "CG" in the figure on page 108. Pages 45 and 108 describes a configuration of the CR oscillator as a ring oscillator. An external resistor "R" is connected between inputs CK1 and CK2 to control a sytem frequency. Id. at 45, 108.

Claim 10 of the '336 Patent	SM550 High Speed CMOS 4-bit Microcomputer SM-550 Series Publication
In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:	The SM550 is a 4-bit microcomputer with a CPU and integrated serial I/O and oscillator. Id. at 45, 108.

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	
providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	The SM550 contains an on-chip CR oscillator shown as "CG" in the figure on pages 45 and 108. Pages 45 and 108 describe a configuration of the CR oscillator as a ring oscillator. An external resistor "R" is connectedbetween inputs CK1 and CK2, to control a system freqeuncy. Id. at 45, 108.
clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	The SM550 teaches an on-chip system clock oscillator. Id. at 45, 108. According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6. The tables on pages 46, 109 show the microprocessor operating frequency varying with voltage. Id.
connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	The SM550 has a serial interface (SIO) that can input/output data using an external serial clock. Id.
clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	The SM550 teaches a second serial clock for clocking the serial interface. The SM550 has a serial interface (SIO) that can input/output data based on an external serial clock.

M. The Sharp SM550 Processor in view of U.S. Patent No. 4,766,567 to *Kato*

United States Patent No. 4,766,567 to *Kato* (Exhibit 6) discussed above was issued on August 23, 1988 and teaches the use of an on-chip ring oscillator to clock the central processing unit of a microprocessor. Furthermore, *Kato* teaches substituting an on-chip ring oscillator system for a CR oscillator system such as used by the Sharp SM550 (Exhibit 9). As a result, one of ordinary skill in the art would have been motivated to use the on-chip ring oscillator taught by *Kato* in the microprocessor system taught by the Sharp SM550 4-bit Microcomputer publication from 1982. Both *Kato* and the Sharp SM550 publication discussed above are prior art under 35 U.S.C. § 103. Combined, the two references teach a microprocessor system with (1) a processing unit clocked by an on-chip ring oscillator and (2) an on-chip input/output serial interface clocked by a serial clock that is independent of the on-chip ring oscillator.

N. The Sharp SM550 Processor in view of U.S. Patent No. 4,766,567 to *Kato* Raises a Substantial New Question of Patentability

Substantial new questions regarding the patentability of *Moore* exist in light of the Sharp SM550 Processor in view of U.S. Patent No. 4,766,567 to *Kato*, which was not referenced by the Examiner. Requestor respectfully submits that the Sharp SM550 Processor in view of U.S. Patent No. 4,766,567 to *Kato* recites every element of claims 1-10 of *Moore*, as explained above. For the Commissioner's convenience, claim charts mapping claims 1-10 of *Moore* to the teachings of the Sharp SM550 Processor in view of U.S. Patent No. 4,766,567 to *Kato* are provided below.

Claim 1 of the '336 Patent	**OBVIOUSNESS** **Sharp SM 550 4-bit Microcomputer - In Use and/or Sold and/or Publicly Known in 1982 in view of U.S. Patent No. 4,766,567 to *Kato* Issued August 23, 1988.**
A microprocessor system, comprising a single integrated circuit including a central processing unit	The SM550 is a 4-bit microcomputer with integrated serial I/O and oscillator. SM550/SM551/SM552 4-bit Microcomputer (Controller) at 36. The Figure on page 38 shows the CPU of the SM550.
and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	The SM550 contains an on-chip CR oscillator shown as "CG" in the figure on page 37. Figure 4(a) shows a configuration of the CR oscillator as a ring oscillator. The external resistor "R" creates a ring between inputs CK1 and CK2. Id. at 45
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing	The SM550 identifies as a feature an on-chip CR clock oscillator. Id at 37. *Kato* teaches an on-chip ring oscillator comprising an odd number of inverters. It would have been obvious for one of ordinary skill in the art to combined the teachings of the

unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	SM550 with the teachings of the '567 patent. The motivation for the substitution of the ring oscillator of *Kato* for the CR oscillator of the SM550 is found in the '567 patent which teaches that by utilizing a built-in ring oscillator in place of a CR oscillator, the output frequency of the built-in ring oscillator lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of the power supply voltage. The frequency capability of the processor and speed of the ring oscillator of the SM550 will inherently vary together due to manufacturing variations, temperature, and voltage as a result of being manufactured on the same integrated circuit using the same process.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;	The SM550 has a serial interface (SIO) that can input/output data based on the "falling edge of the serial clock." Id
and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	The SM550 teaches a second serial clock for clocking the serial interface. The SM550 has a serial interface (SIO) that can input/output data based on the "falling edge of the serial clock."

Claim 2 of the '336 Patent	**OBVIOUSNESS** **Sharp SM 550 4-bit Microcomputer - In Use and/or Sold and/or Publicly Known in 1982 in view of U.S. Patent No. 4,766,567 to *Kato* Issued August 23, 1988.**
The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	A SM550 discusses the use of a "serial clock." According to TPL, "in serial communications the transmitting device sends data and clock at a fixed frequency." See Exhibit 13 at 10.

Claim 3 of the '336 Patent	**OBVIOUSNESS** **Sharp SM 550 4-bit Microcomputer - In Use and/or Sold and/or Publicly Known in 1982 in view of U.S. Patent No. 4,766,567 to *Kato* Issued August 23, 1988.**
In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:	The SM550 is a 4-bit microcomputer with integrated serial I/O and oscillator. Id.at 36.

providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;	The SM550 identifies as a feature an on-chip CR clock oscillator. Id.at 37. *Kato* teaches an on-chip ring oscillator comprising an odd number of inverters. It would have been obvious for one of ordinary skill in the art to combined the teachings of the SM550 with the teachings of the '567 patent. The motivation for the substitution of the ring oscillator of *Kato* for the CR oscillator of the SM550 is found in the '567 patent which teaches that by utilizing a built-in ring oscillator in place of a CR oscillator, the output frequency of the built-in ring oscillator lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of the power supply voltage. The frequency capability of the processor and speed of the ring oscillator of the SM550 will inherently vary together due to manufacturing variations, temperature, and voltage as a result of being manufactured on the same integrated circuit using the same process.
using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;	The processing frequency of the microprocessor will operate at a variable frequency depending on the speed of the ring oscillator.
providing an on chip input/output interface for the microprocessor integrated circuit; and	The SM550 has a serial interface (SIO) that can input/output data based on the "falling edge of the serial clock."
clocking the input/output interface with a second clock independent of the ring oscillator system clock.	The SM550 teaches a second serial clock for clocking the serial interface. The SM550 has a serial interface (SIO) that can input/output data based on the "falling edge of the serial clock."

Claim 4 of the '336 Patent	**OBVIOUSNESS** **Sharp SM 550 4-bit Microcomputer - In Use and/or Sold and/or Publicly Known in 1982 in view of U.S. Patent No. 4,766,567 to *Kato* Issued August 23, 1988.**
The method of claim 3 in which the second	A SM550 discusses the use of a "serial clock."

clock is a fixed frequency clock.	According to TPL, "in serial communications the transmitting device sends data and clock at a fixed frequency." See Exhibit 13 at 10.

Claim 5 of the '336 Patent	**OBVIOUSNESS** **Sharp SM 550 4-bit Microcomputer - In Use and/or Sold and/or Publicly Known in 1982 in view of U.S. Patent No. 4,766,567 to *Kato* Issued August 23, 1988.**
The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would include the serial interface of the SM550.

Claim 6 of the '336 Patent	**OBVIOUSNESS** **Sharp SM 550 4-bit Microcomputer - In Use and/or Sold and/or Publicly Known in 1982 in view of U.S. Patent No. 4,766,567 to *Kato* Issued August 23, 1988.**
A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;	The SM550 is a 4-bit microcomputer with integrated serial I/O and oscillator. Id. at 36.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,	The SM550 identifies as a feature an on-chip CR clock oscillator. Id.at 37. *Kato* teaches an on-chip ring oscillator comprising an odd number of inverters. It would have been obvious for one of ordinary skill in the art to combined the teachings of the SM550 with the teachings of the '567 patent. The motivation for the substitution of the ring oscillator of *Kato* for the CR oscillator of the SM550 is found in the '567 patent which teaches that by utilizing a built-in ring oscillator in place of a CR oscillator, the output frequency of the built-in ring oscillator lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of the power supply voltage. The frequency capability of the processor and

	speed of the ring oscillator of the SM550 will inherently vary together due to manufacturing variations, temperature, and voltage as a result of being manufactured on the same integrated circuit using the same process.
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	The SM550 identifies as a feature an on-chip system clock oscillator. SM550 at 37. The frequency capability of the processor and speed of the ring oscillator will inherently vary together due to manufacturing variations, temperature, and voltage as a result of being manufactured on the same integrated circuit using the same process.
an on-chip input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	The SM550 has a serial interface (SIO) that can input/output data based on the "falling edge of the serial clock."
an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	The SM550 teaches a second serial clock for clocking the serial interface. The SM550 has a serial interface (SIO) that can input/output data based on the "falling edge of the serial clock."

Claim 7 of the '336 Patent	**OBVIOUSNESS** **Sharp SM 550 4-bit Microcomputer - In Use and/or Sold and/or Publicly Known in 1982 in view of U.S. Patent No. 4,766,567 to *Kato* Issued August 23, 1988.**
The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	It would have been obvious for one of ordinary skill in the art to combined the teachings of the SM550 with the teachings of the '567 patent. The motivation for the substitution of the ring oscillator of *Kato* for the CR oscillator of the SM550 is found in the '567 patent which teaches that by utilizing a built-in ring oscillator in place of a CR oscillator, the output frequency of the built-in ring oscillator lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of the power supply voltage. The frequency capability of the processor and speed of the ring oscillator of the SM550 will

	inherently vary together due to manufacturing variations, temperature, and voltage as a result of being manufactured on the same integrated circuit using the same process.

Claim 8 of the '336 Patent	**OBVIOUSNESS** **Sharp SM 550 4-bit Microcomputer - In Use and/or Sold and/or Publicly Known in 1982 in view of U.S. Patent No. 4,766,567 to *Kato* Issued August 23, 1988.**
The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would include the serial interface of the SM 550.

Claim 9 of the '336 Patent	**OBVIOUSNESS** **Sharp SM 550 4-bit Microcomputer - In Use and/or Sold and/or Publicly Known in 1982 in view of U.S. Patent No. 4,766,567 to *Kato* Issued August 23, 1988.**
The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	The SM550 identifies as a feature an on-chip CR clock oscillator. Id.at 37. *Kato* teaches an on-chip ring oscillator comprising an odd number of inverters. It would have been obvious for one of ordinary skill in the art to combined the teachings of the SM550 with the teachings of the '567 patent. The motivation for the substitution of the ring oscillator of *Kato* for the CR oscillator of the SM550 is found in the '567 patent which teaches that by utilizing a built-in ring oscillator in place of a CR oscillator, the output frequency of the built-in ring oscillator lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of the power supply voltage.

Claim 10 of the '336 Patent	**OBVIOUSNESS** **Sharp SM 550 4-bit Microcomputer - In Use and/or Sold and/or Publicly Known in 1982 in view of U.S. Patent No. 4,766,567 to *Kato* Issued August 23, 1988.**

In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of: providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	The SM550 is a 4-bit microcomputer with integrated serial I/O and oscillator. SM550 at 36. The Figure on page 38 shows the CPU of the SM550.
providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	The SM550 identifies as a feature an on-chip CR clock oscillator. Id.at 37. *Kato* teaches an on-chip ring oscillator comprising an odd number of inverters. It would have been obvious for one of ordinary skill in the art to combined the teachings of the SM550 with the teachings of the '567 patent. The motivation for the substitution of the ring oscillator of *Kato* for the CR oscillator of the SM550 is found in the '567 patent which teaches that by utilizing a built-in ring oscillator in place of a CR oscillator, the output frequency of the built-in ring oscillator lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of the power supply voltage.
clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	The SM550 identifies as a feature an on-chip system clock oscillator. SM550 at 37. The '567 patent teaches that by utilizing a built-in ring oscillator in place of a CR oscillator, the output frequency of the built-in ring oscillator lowers in proportion to the speed of the data processing circuit which is lowered due to the drop of the power supply voltage. The frequency capability of the processor and speed of the ring oscillator of the SM550 will inherently vary together due to manufacturing variations, temperature, and voltage as a result of being manufactured on the same integrated circuit using the same process.
connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between	The SM550 has a serial interface (SIO) that can input/output data based on the "falling edge of the serial clock."

said input/output interface and said central processing unit; and	
clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	The SM550 teaches a second serial clock for clocking the serial interface. The SM550 has a serial interface (SIO) that can input/output data based on the "falling edge of the serial clock."

O. The Publication of "*Microprocessors in brief*"

An article by Robert C. Stanley called "*Microprocessors in brief*" was published in March 1985. Robert C. Stanley, *Microprocessors in brief*, IBM J. Res. Develop. Vol. 29, No. 2 at 115-16 (March 1985). See Exhibit 10. As a result, this article is prior art against the Moore patent under 35 U.S.C. § 102(b). The article discusses the state of the art as of 1985 regarding single chip microprocessors and reveals that these devices can contain, on a single chip, a CPU, a clock oscillator, a PLL or phase locked loop, and the ability to handle serial I/O.

P. The Publication of "*Microprocessors in brief*" Raises a Substantial New Question of Patentability

Substantial new questions regarding the patentability of *Moore* exist in light of the publication *Microprocessors in brief*, which was not referenced by the Examiner. Requestor respectfully submits that the publication *Microprocessors in brief* recites every element of claims 1-10 of *Moore*, as explained above. For the Commissioner's convenience, claim charts mapping claims 1-10 of *Moore* to the teachings of the publication *Microprocessors in brief* are provided below.

Claim 1 of the '336 Patent – Filed August 3, 1989	**Robert C. Stanley, *Microprocessors in brief*, IBM J. Res. Develop. Vol. 29, No. 2 at 115-16 (March 1985).**
A microprocessor system, comprising a single integrated circuit including	*Microprocessors in brief* Article describes a single chip microprocessor. Robert C. Stanley, *Microprocessors in brief*, IBM J. Res. Develop. Vol. 29, No. 2 at 115-16 (March 1985).
a central processing unit and	The microprocessor system includes a CPU. Id.
an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	The article describes a PLL as part of the single chip microprocessor: "There is a type of microprocessor that is generally referred to as a single-chip microprocessor, or microcontroller. The main feature of these devices is that an attempt has been made to place the entire system on one chip (This includes the CPU, RAM, ROM, clock oscillator, and I/O ports. . . .) . . . Some

	of the other features incorporated into microcontrollers to increase their control capability include . . . PLLs (phase-locked loops), and the ability to handle serial I/O." Id. According to TPL, the "presence of a PLL indicates the presence of a ring oscillator." See Exhibit 13 at 12.
said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;	As quoted above, the article above discloses an on chip serial I/O.
and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	A serial I/O can be clocked by a clock external to the system clock

Claim 2 of the '336 Patent	**Robert C. Stanley, *Microprocessors in brief*, IBM J. Res. Develop. Vol. 29, No. 2 at 115-16 (March 1985).**
The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	The microprocessor contains a serial interface. According to TPL, "in serial communications the transmitting device sends data and clock at a fixed frequency." See Exhibit 13 at 10.

Claim 3 of the '336 Patent	**Robert C. Stanley, *Microprocessors in brief*, IBM J. Res. Develop. Vol. 29, No. 2 at 115-16 (March 1985).**
In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:	*Microprocessors in brief* Article describes a single chip microprocessor and a method for clocking the processor.

providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;	The article describes a PLL as part of the single chip microprocessor: "There is a type of microprocessor that is generally referred to as a single-chip microprocessor, or microcontroller. The main feature of these devices is that an attempt has been made to place the entire system on one chip (This includes the CPU, RAM, ROM, clock oscillator, and I/O ports. . . .) . . . Some of the other features incorporated into microcontrollers to increase their control capability include . . . PLLs (phase-locked loops), and the ability to handle serial I/O." Id. According to TPL, the "presence of a PLL indicates the presence of a ring oscillator." See Exhibit 13 at 12. According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;	The processing frequency of the processor will vary according to the speed of the on-chip timing circuitry, or PLL.
providing an on chip input/output interface for the microprocessor integrated circuit; and	As quoted above, the article above discloses an on chip serial I/O.
clocking the input/output interface with a second clock independent of	A serial I/O can be clocked by a clock external to the system clock

the ring oscillator system clock.	

Claim 4 of the '336 Patent	**Robert C. Stanley, *Microprocessors in brief*, IBM J. Res. Develop. Vol. 29, No. 2 at 115-16 (March 1985).**
The method of claim 3 in which the second clock is a fixed frequency clock.	The microprocessor contains a serial interface. According to TPL, "in serial communications the transmitting device sends data and clock at a fixed frequency." See Exhibit 13 at 10.

Claim 5 of the '336 Patent	**Robert C. Stanley, *Microprocessors in brief*, IBM J. Res. Develop. Vol. 29, No. 2 at 115-16 (March 1985).**
The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would include the serial interface disclosed by the article.

Claim 6 of the '336 Patent	**Robert C. Stanley, *Microprocessors in brief*, IBM J. Res. Develop. Vol. 29, No. 2 at 115-16 (March 1985).**
A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;	*Microprocessors in brief* Article describes a single chip microprocessor. Robert C. Stanley, *Microprocessors in brief*, IBM J. Res. Develop. Vol. 29, No. 2 at 115-16 (March 1985). The microprocessor system includes a CPU. Id.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,	The article describes a PLL as part of the single chip microprocessor: "There is a type of microprocessor that is generally referred to as a single-chip microprocessor, or microcontroller. The main feature of these devices is that an attempt has been made to place the entire system on one chip (This includes the CPU, RAM, ROM, clock oscillator, and I/O ports. . . .) . . . Some of the other features incorporated into microcontrollers to increase their control

	capability include . . . PLLs (phase-locked loops), and the ability to handle serial I/O." Id. According to TPL, the "presence of a PLL indicates the presence of a ring oscillator." See Exhibit 13 at 12.
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
an on-chip input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	As quoted above, the article above discloses an on chip serial I/O.
an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	A serial I/O can be clocked by a clock external to the system clock

Claim 7 of the '336 Patent	**Robert C. Stanley, *Microprocessors in brief*, IBM J. Res. Develop. Vol. 29, No. 2 at 115-16 (March 1985).**
The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.

Claim 8 of the '336 Patent	**Robert C. Stanley, *Microprocessors in brief*, IBM J. Res. Develop. Vol. 29, No. 2 at 115-16 (March 1985).**

The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would include the serial interface disclosed by the article.

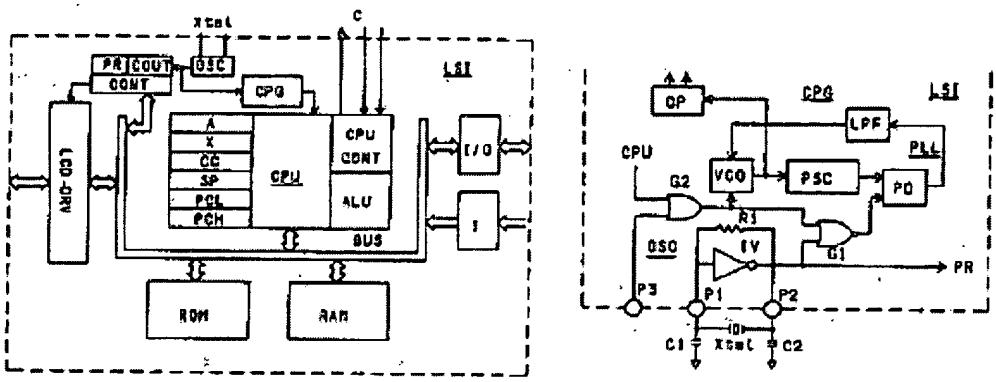
Claim 9 of the '336 Patent	**Robert C. Stanley, *Microprocessors in brief*, IBM J. Res. Develop. Vol. 29, No. 2 at 115-16 (March 1985).**
The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	The article describes a PLL as part of the single chip microprocessor: "There is a type of microprocessor that is generally referred to as a single-chip microprocessor, or microcontroller. The main feature of these devices is that an attempt has been made to place the entire system on one chip (This includes the CPU, RAM, ROM, clock oscillator, and I/O ports. . . .) . . . Some of the other features incorporated into microcontrollers to increase their control capability include . . . PLLs (phase-locked loops), and the ability to handle serial I/O." Id. According to TPL, the "presence of a PLL indicates the presence of a ring oscillator." See Exhibit 13 at 12.

Claim 10 of the '336 Patent	**Robert C. Stanley, *Microprocessors in brief*, IBM J. Res. Develop. Vol. 29, No. 2 at 115-16 (March 1985).**
In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of: providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	*Microprocessors in brief* Article describes a single chip microprocessor. Robert C. Stanley, *Microprocessors in brief*, IBM J. Res. Develop. Vol. 29, No. 2 at 115-16 (March 1985). The microprocessor system includes a CPU. Id.

providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	The article describes a PLL as part of the single chip microprocessor: "There is a type of microprocessor that is generally referred to as a single-chip microprocessor, or microcontroller. The main feature of these devices is that an attempt has been made to place the entire system on one chip (This includes the CPU, RAM, ROM, clock oscillator, and I/O ports. . . .) . . . Some of the other features incorporated into microcontrollers to increase their control capability include . . . PLLs (phase-locked loops), and the ability to handle serial I/O." Id. According to TPL, the "presence of a PLL indicates the presence of a ring oscillator." See Exhibit 13 at 12.
clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	The article describes the use of an on chip PLL for clocking the CPU. According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	As quoted above, the article above discloses an on chip serial I/O.
clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	A serial I/O can be clocked by a clock external to the system clock

Q. Japanese Patent Application No. SHO 61[1986]-127228 to *Arai*

Japanese Patent Application No. SHO 61[1986]-127228 to *Arai* was published on June 14, 1986. See Exhibit 11. The *Arai* patent discloses a digital information processing device that includes an on-chip phase-locked-loop, or PLL, that constitutes clock generating circuit CPG, shown below on the left hand side. The PLL contains a voltage controlled oscillator, or VCO shown below on the right hand side. The signal output of the PLL is used to clock the CPU. In addition, *Arai* teaches an on-chip input/output interface that receives display information and drives a liquid crystal electrode that is clocked by the clock signal provided by the OSC circuit, shown below on the left hand side.



R. *Arai* Raises a Substantial New Question of Patentability

Substantial new questions regarding the patentability of *Moore* exist in light of the *Arai* patent, which was not referenced by the Examiner. Requestor respectfully submits that the *Arai* patent recites every element of claims 1-10 of *Moore*, as explained above. For the Commissioner's convenience, claim charts mapping claims 1-10 of *Moore* to the teachings of the the *Arai* patent are provided below.

Claim 1 of the '336 Patent – Filed August 3, 1989	**Japanese Patent Application No. SHO 61[1986]-127228 to *Arai***
A microprocessor system, comprising a single integrated circuit including	Aria teaches a "one-chip microcomputer" that is an "integrated circuit LSI." *Arai* at 3.
a central processing unit and	The microprocessor system includes a CPU. Figure 1 at 10.
an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,	*Arai* describes a PLL as part of the single chip microprocessor. Figure 2. The PLL constitutes the CPG circuit shown in Figure 1. *Arai* at 5. According to TPL, the "presence of a PLL indicates the presence of a ring oscillator." See Exhibit 13 at 12.
said central processing unit and said ring oscillator variable speed system clock each	According to TPL, because of "the laws of physics and the state of the art of

including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;	microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit;	*Arai* teaches on on-chip "LCD-DRV" input/output interface. This interface that receives display information and drives a liquid crystal electrode. Id. at 4.
and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface.	The LCD-DRV interface is clocked by the clock signal generated by the OSC circuit shown in Figure 1. This OSC circuit is independent of the PLL within the CPG circuit. Id. at 4.

Claim 2 of the '336 Patent	**Japanese Patent Application No. SHO 61[1986]-127228 to *Arai***
The microprocessor system of claim 1 in which said second clock is a fixed frequency clock.	The microprocessor's LCD-DRV interface can be clocked by the OSC circuit driven by a fixed 32.768 KHz fixed frequency clock. Id. at 4.

Claim 3 of the '336 Patent	**Japanese Patent Application No. SHO 61[1986]-127228 to *Arai***
In a microprocessor integrated circuit, a method for clocking the microprocessor within the integrated circuit, comprising the steps of:	Aria teaches a "one-chip microcomputer" that is an "integrated circuit LSI." *Arai* at 3. *Arai* teaches a method for clocking the microprocessor. Id.
providing an entire ring oscillator system clock constructed of electronic devices within the integrated circuit, said electronic devices having operating characteristics which will, because said entire ring oscillator system clock and said microprocessor are located within the same integrated circuit, vary together with operating characteristics of electronic devices included within the microprocessor;	*Arai* describes a PLL as part of the single chip microprocessor. The PLL constitutes the CPG circuit shown in Figure 1. *Arai* at 5. According to TPL, the "presence of a PLL indicates the presence of a ring oscillator." See Exhibit 13 at 12. According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing

	frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
using the ring oscillator system clock for clocking the microprocessor, said microprocessor operating at a variable processing frequency dependent upon a variable speed of said ring oscillator system clock;	*Arai* describes a PLL as part of the single chip microprocessor. The PLL constitutes the CPG circuit shown in Figure 1. *Arai* at 5. The CPG is used to clock the CPU. Id. at 5-6; Figure 1.
providing an on chip input/output interface for the microprocessor integrated circuit; and	*Arai* teaches on on-chip "LCD-DRV" input/output interface. This interface that receives display information and drives a liquid crystal electrode. Id. at 4.
clocking the input/output interface with a second clock independent of the ring oscillator system clock.	The LCD-DRV interface is clocked by the clock signal generated by the OSC circuit shown in Figure 1. This OSC circuit is independent of the PLL within the CPG circuit. Id. at 4.

Claim 4 of the '336 Patent	**Japanese Patent Application No. SHO 61[1986]-127228 to *Arai***
The method of claim 3 in which the second clock is a fixed frequency clock.	The microprocessor's LCD-DRV interface can be clocked by the OSC circuit driven by a fixed 32.768 KHz fixed frequency clock. Id. at 4.

Claim 5 of the '336 Patent	Japanese Patent Application No. SHO 61[1986]-127228 to *Arai*
The method of claim 3 further including the step of: transferring information to and from said microprocessor in synchrony with said ring oscillator system clock.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would include the LCD-DRV interface of *Arai*.

Claim 6 of the '336 Patent	Japanese Patent Application No. SHO 61[1986]-127228 to *Arai*
A microprocessor system comprising: a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;	Aria teaches a "one-chip microcomputer" that is an "integrated circuit LSI." *Arai* at 3.
an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator clocking said central processing unit at a clock rate and being constructed of a second plurality of electronic devices,	*Arai* describes a PLL as part of the single chip microprocessor. Figure 2. The PLL constitutes the CPG circuit shown in Figure 1. *Arai* at 5. According to TPL, the "presence of a PLL indicates the presence of a ring oscillator." See Exhibit 13 at 12.
thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way as a function of parameter variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation;	According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
an on-chip input/output interface, connected between said central processing unit and an external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and	*Arai* teaches on on-chip "LCD-DRV" input/output interface. This interface that receives display information and drives a liquid crystal electrode. Id. at 4.
an external clock, independent of said oscillator, connected to said input/output interface wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	The LCD-DRV interface is clocked by the clock signal generated by the OSC circuit shown in Figure 1. This OSC circuit is independent of the PLL within the CPG circuit. Id. at 4.

Claim 7 of the '336 Patent	Japanese Patent Application No. SHO 61[1986]-127228 to *Arai*
The microprocessor system of claim 6 wherein said one or more operational parameters include operating temperature of said substrate or operating voltage of said substrate.	According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6. In addition, *Arai* teaches that "when control voltage VC is raised . . . the oscillation frequency is increased . . . On the other hand when the control voltage VC is lowered , , , the oscillation frequency is lowered." Id. at 7-8.

Claim 8 of the '336 Patent	Japanese Patent Application No. SHO 61[1986]-127228 to *Arai*
The microprocessor system of claim 6 wherein said external clock comprises a fixed-frequency clock which operates synchronously relative to said oscillator.	TPL has asserted that any information transfer over a microprocessor interface satisfies this limitation. See Exhibit 12 at 29. This would include the LCD-DRV interface disclosed by *Arai*.

Claim 9 of the '336 Patent	Japanese Patent Application No. SHO 61[1986]-127228 to *Arai*
The microprocessor system of claim 6 wherein said oscillator comprises a ring oscillator.	*Arai* describes a PLL as part of the single chip microprocessor. Figure 2. The PLL constitutes the CPG circuit shown in Figure 1. *Arai* at 5. According to TPL, the "presence of a PLL indicates the presence of a ring oscillator." See Exhibit 13 at 12.

Claim 10 of the '336 Patent	Japanese Patent Application No. SHO 61[1986]-127228 to *Arai*
In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:	Aria teaches a "one-chip microcomputer" that is an "integrated circuit LSI." *Arai* at 3.

providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a first plurality of transistors and being operative at a processing frequency;	
providing an entire variable speed clock disposed upon said integrated circuit substrate, said variable speed clock being constructed of a second plurality of transistors;	*Arai* describes a PLL as part of the single chip microprocessor. The PLL constitutes the CPG circuit shown in Figure 1. *Arai* at 5. The CPG is used to clock the CPU. Id. at 5-6; Figure 1. According to TPL, the "presence of a PLL indicates the presence of a ring oscillator." See Exhibit 13 at 12.
clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;	The CPG with the on chip PLL is used to clock the CPU. Id. at 5-6; Figure 1. According to TPL, because of "the laws of physics and the state of the art of microprocessor manufacturing, the processing frequency of said central processing unit and the speed of the ring oscillator, because they are located on the same integrated circuit, vary together due to manufacturing variations, operating voltage and temperature." See Exhibit 13 at 6.
connecting an on chip input/output interface between said central processing unit and an external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and	*Arai* teaches on on-chip "LCD-DRV" input/output interface. This interface that receives display information and drives a liquid crystal electrode. Id. at 4.
clocking said input/output interface using an external clock wherein said external clock is operative at a frequency independent of a clock frequency of said oscillator.	The LCD-DRV interface is clocked by the clock signal generated by the OSC circuit shown in Figure 1. This OSC circuit is independent of the PLL within the CPG circuit. Id. at 4.

VI. CONCLUSION

For these reasons, substantial new questions of patentability exist, as claims 1-10 do not satisfy the requirements of Title 35 U.S.C. § 100 et seq.

A Notice to this effect is requested.

Respectfully submitted,

By: 

Michael Hawes

Registration No. 38,487

ATTORNEY FOR REQUESTOR