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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/009,034	03/31/2008	5440749	0081-011X1	3309

40972 7590 02/11/2011

HENNEMAN & ASSOCIATES, PLC
70 N. MAIN ST.
THREE RIVERS, MI 49093

EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 02/11/2011

Please find below and/or attached an Office communication concerning this application or proceeding.

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MAILED

FEB 10 2011

CENTRAL REEXAMINATION UNIT

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. 90/009,034, 90/009,389, & 90/010,520

PATENT NO. 5440749.

ART UNIT 3992.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/009,389	01/16/2009	5440749	0081-011X2	9206

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/010,520	04/30/2009	5440749	0081-011X3	9626

40972 7590 02/11/2011

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CENTRAL REEXAMINATION UNIT

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. 90/009,034, 90/009,389, & 90/010,520.

PATENT NO. 5440749.

ART UNIT 3992.

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WASHINGTON, D.C. 20001

Date:

MAILED

FEB 10 2011

CENTRAL REEXAMINATION UNIT

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. : 90010520
PATENT NO. : 5440749
ART UNIT : 3992

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified ex parte reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the ex parte reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Notice of Intent to Issue Ex Parte Reexamination Certificate	Control No. 90/010,520 90/009,034, 90/009,389, &	Patent Under Reexamination 5440749	
	Examiner JOSEPH R. POKRZYWA	Art Unit 3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ Prosecution on the merits is (or remains) closed in this *ex parte* reexamination proceeding. This proceeding is subject to reopening at the initiative of the Office or upon petition. *Cf.* 37 CFR 1.313(a). A Certificate will be issued in view of
   - (a) ☒ Patent owner's communication(s) filed: *25 January 2011*.
   - (b) ☐ Patent owner's late response filed: _____.
   - (c) ☐ Patent owner's failure to file an appropriate response to the Office action mailed: _____.
   - (d) ☐ Patent owner's failure to timely file an Appeal Brief (37 CFR 41.31).
   - (e) ☐ Other: _____.

   Status of *Ex Parte* Reexamination:
   - (f) Change in the Specification: ☐ Yes ☒ No
   - (g) Change in the Drawing(s): ☐ Yes ☒ No
   - (h) Status of the Claim(s):
     - (1) Patent claim(s) confirmed: _____.
     - (2) Patent claim(s) amended (including dependent on amended claim(s)): *1-7 and 10-27*
     - (3) Patent claim(s) canceled: *8 and 9*.
     - (4) Newly presented claim(s) patentable: 30 and 34-62.
     - (5) Newly presented canceled claims: 31-33.
     - (6) Patent claim(s) ☐ previously ☐ currently disclaimed: _____
     - (7) Patent claim(s) not subject to reexamination: 28 and 29.

2. ☒ Note the attached statement of reasons for patentability and/or confirmation. Any comments considered necessary by patent owner regarding reasons for patentability and/or confirmation must be submitted promptly to avoid processing delays. Such submission(s) should be labeled: "Comments On Statement of Reasons for Patentability and/or Confirmation."
3. ☐ Note attached NOTICE OF REFERENCES CITED (PTO-892).
4. ☐ Note attached LIST OF REFERENCES CITED (PTO/SB/08 or PTO/SB/08 substitute).
5. ☐ The drawing correction request filed on _____ is: ☐ approved ☐ disapproved.
6. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
   a)☐ All b)☐ Some* c)☐ None of the certified copies have
   - ☐ been received.
   - ☐ not been received.
   - ☐ been filed in Application No. _____.
   - ☐ been filed in reexamination Control No. _____.
   - ☐ been received by the International Bureau in PCT Application No. _____.

   * Certified copies not received: _____.
7. ☒ Note attached Examiner's Amendment.
8. ☐ Note attached Interview Summary (PTO-474).
9. ☐ Other: _____.

cc: Requester (if third party requester)

DETAILED ACTION

Response to Amendment

1. The Patent Owner submitted an after-final amendment dated 1/25/2011, which has been fully considered, entered, and made of record.

Summary of Proceedings

2. Original claims 1-29 of U.S. Patent 5,440,749 (hereafter "the '749 Patent") issued on August 8, 1995 to Moore *et al.* In this reexamination proceeding, claims 28 and 29 were not requested to be reexamined, and are not subject to the current reexamination proceeding. Further, claims 1, 8, and 9 were the original patented independent claims. With the previous proposed after-final amendment filed 11/29/2010, claims 62 and 63 were newly proposed, and were indicated in the Advisory Action dated 12/16/2010 as containing patentable subject matter, while independent claims 1, 8, and 9 were discussed as remaining rejected.

3. Subsequently, in the current Patent Owner's amendment dated 1/25/2011, claim 1 has been amended to include features from the previously proposed claims, and claims 8 and 9 have been canceled. Further, in this regard, the corresponding dependent claims of claims 8 and 9 that were indicated as being rejected, have now been amended to change their dependency (directly and indirectly) to new claim 62, which was previously indicated as being patentable..

4. Thus, with the amendment dated 1/25/2011, claims 1-7, 10-27, and 34-62 remain subject to the current reexamination proceeding.

5. Continuing, the examiner notes that in the amendment dated 1/25/2011, claims 5, 7, 10, 13, 18, and 19 are shown improperly, as the newly added elements in each of these claims are not shown as being underlined. In this regard, 37 CFR 1.530 states, in part:

> (d) *Making amendments in a reexamination proceeding....*
>
> (2) *Claims* . An amendment paper must include the entire text of each patent claim which is being proposed to be changed by such amendment paper and of each new claim being proposed to be added by such amendment paper. For any claim changed by the amendment paper, a parenthetical expression "amended," "twice amended," etc., should follow the claim number. Each patent claim proposed to be changed and each proposed added claim must include markings pursuant to paragraph (f) of this section, except that a patent claim or proposed added claim should be canceled by a statement canceling the claim, without presentation of the text of the claim. ...
>
> (f) *Changes shown by markings* . Any changes **relative to the patent being reexamined** which are made to the specification, including the claims, must include the following markings:
>
> (1) The matter to be omitted by the reexamination proceeding must be enclosed in brackets; and
>
> (2) **The matter to be added by the reexamination proceeding must be underlined**. [Emphasis added].

6. With this, in the amendment dated 1/25/2011, the matter that was newly added in claims 5, 7, 10, 13, 18, and 19 was not shown as underlined. Thus, an examiners amendment to these claims appears below with the newly added matter being underlined.

Examiner's Amendment

7. An examiner's amendment to the record appears below. The changes made by this examiner's amendment will be reflected in the reexamination certificate to issue in due course. Claims 5, 7, 10, 13, 18, and 19 are now each shown with the newly added matter underlined, while a typographical error was fixed in claim 45.

Claim 5 should read:

5. (Currently Amended) The microprocessor system of claim 1 [additionally comprising an] wherein said instruction register for the multiple instructions is connected to said means for fetching instructions, means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession, means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions, said counter being connected to said means for decoding to receive incrementing and reset control signals from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and to supply a control signal to said means for fetching instructions in response to a SKIP instruction in the multiple instructions.

Claim 7 should read:

7. (Currently Amended) The microprocessor system of claim 1 [additionally comprising an] wherein said instruction register for the multiple instructions and a variable width operand to

be used with one of the multiple instructions is connected to said means for fetching instructions, means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession,

means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions, said counter being connected to said means for decoding to receive incrementing and reset control signals from said means for decoding, said means for decoding being configured to control said counter in response to an instruction utilizing the variable width operand stored in said instruction register, and means connected to said counter to select the variable width operand for use with the instruction utilizing the variable width operand in response to said counter.

Claim 10 should read:

10. (Currently Amended) The microprocessor system of claim [9] 62 additionally comprising a second push down stack, said means for storing a top item being connected to provide an input to said second push down stack and a control means connected between said means for storing a top item and said second push down stack for controlling provision of the input to said second push down stack.

Claim 13 should read:

13. (Currently Amended) The microprocessor system of claim 12 [additionally comprising an] wherein the instruction register for the multiple instructions is connected to said means for fetching instructions, means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession, means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions, said counter being connected to said means for decoding to receive incrementing and reset control signals from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and to supply a control signal to said means for fetching instructions in response to a SKIP instruction in the multiple instructions.

Claims 18 and 19 should read:

18. (Currently Amended) The microprocessor system of claim [9] 62 additionally comprising a programmable read only memory containing instructions connected to said bus, means connected to said bus for fetching instructions for said central processing unit on said bus, said means for fetching instructions including means for assembling a plurality of instructions from said programmable read only memory, storing the plurality of instructions in said dynamic random access memory and subsequently supplying the plurality of instructions from said dynamic random access memory to said central processing unit on said bus.

19. (Currently Amended) The microprocessor system of claim [9] 62 additionally comprising a direct memory access processing unit having the capacity to request and execute instructions, said bus connecting said direct memory access processing unit to said dynamic random access memory, said dynamic random access memory containing instructions for said central processing unit and said direct memory access processing unit, said direct memory access processing unit being connected to means for fetching instructions for said central processing unit on said bus and for fetching instructions for said direct memory access processing unit on said bus.

In **claim 45**, line 2, "hasa" is changed to read "has_a", such that claim 45 reads:

45. (Currently Amended) The microprocessor system of claim 1 wherein the instruction register has a plurality of instruction locations for storing the multiple sequential instructions, the plurality of instruction locations including a first location to be accessed before any other of the plurality of instruction locations, the central processing unit integrated circuit further including means, responsive to content of an instruction of the multiple sequential instructions in a location other than the first location, for accessing a next instruction at the first location.

STATEMENT OF REASONS FOR PATENTABILITY AND/OR CONFIRMATION

The following is an examiner's statement of reasons for patentability and/or confirmation of the claims found patentable in this reexamination proceeding:

Claims 21-27 are confirmed as patentable.

Claims 1-7, 10-20 are deemed as patentable, as amended.

Claims 30 and 34-62 are deemed as patentable.

Regarding ***claim 1***, in the examiner's opinion, it would not have been obvious to one of ordinary skill in the art to have the systems as claimed, further include the features of "supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle the multiple instructions fetched". This limitation is seen to clarify the function of the current invention, which is not expressly described in the closest cited prior art of the T414 Data Sheet, the May'948 reference, MacGregor, or Koopman. Thus, the claim, as presented in the amendment dated 1/25/2010, is rendered as patentable.

Regarding ***claims 5, 7, and 13***, in the examiner's opinion, it would not have been obvious to one of ordinary skill in the art at the time the invention was made to have the claimed system include "an instruction register for the multiple instructions connected to said means for fetching instructions, means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession". As

discussed above, upon reconsideration, the closest prior art of record, being the reference of MacGregor falls short of teaching of a counter to control a means for supplying the multiple instructions in succession from the instruction register. Because of this, the claims are rendered patentable.

Regarding ***claims 21 and 55***, in the examiner's opinion, it would not have been obvious to one of ordinary skill in the art at the time the invention was made to have the system defined in claim 9, further include the features that require said microprocessor system is configured to provide different memory access timing for different storing capacity sizes of said dynamic random access memory by including a sensing circuit and a driver circuit, and an output enable line connected between said dynamic random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level after a memory read operation as a function of different capacitance on said bus as a result of the different storing capacity sizes of said dynamic random access memory, said microprocessor system being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

Regarding ***claims 23 and 57***, in the examiner's opinion, it would not have been obvious to one of ordinary skill in the art have the system discussed in claim 9 further be configured to operate at variable clock speed, with said microprocessor system additionally comprising a ring counter variable speed system clock connected to said central processing unit, said central

processing unit and said ring counter variable speed system clock being provided in a single integrated circuit, said ring counter variable speed system clock being configured to provide different clock speed to said central processing unit as a result of transistor propagation delays, depending on at least one of temperature of said single integrated circuit, voltage and microprocessor fabrication process for said single integrated circuit.

Regarding ***claims 26 and 60***, in the examiner's opinion, it would not have been obvious to one of ordinary skill in the art at the time of the invention to have the system discussed above in claim 9, further include the features that require said first push down stack has a first plurality of stack registers having stack memory elements configured as latches, a second plurality of stack registers having stack memory elements configured as a random access memory, said first and second plurality of stack registers and said central processing unit being provided in a single integrated circuit with a top one of said second plurality of stack registers being connected to said a bottom one of said first plurality of stack registers, and a third plurality of stack registers having stack memory elements configured as a random access memory external to said single integrated circuit, with a top one of said third plurality of stack registers being connected to a bottom one of said second plurality of stack registers, said microprocessor system being configured to operate said first, second and third plurality of stack registers hierarchically as interconnected stacks.

Regarding ***claim 62***, in the examiner's opinion, it would not have been obvious to one of ordinary skill in the art to have the systems as claimed, further include the features of "supplying

the multiple sequential instructions in parallel to said instruction register during the same memory cycle the multiple instructions fetched". This limitation is seen to clarify the function of the current invention, which is not expressly described in the closest cited prior art of the T414 Data Sheet, the May'948 reference, MacGregor, or Koopman. Thus, the claim is rendered as patentable.

Any comments considered necessary by PATENT OWNER regarding the above statement must be submitted promptly to avoid processing delays. Such submission by the patent owner should be labeled: "Comments on Statement of Reasons for Patentability and/or Confirmation" and will be placed in the reexamination file.

Conclusion

8. **All** correspondence relating to this ex parte reexamination proceeding should be directed:

By Mail to: Mail Stop *Ex Parte* Reexam
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900
Central Reexamination Unit

By hand: Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Registered users of EFS-Web may alternatively submit such correspondence via the electronic filing system EFS-Web, at https://sportal.uspto.gov/authenticate/authenticateuserlocalepf.html. EFS-Web offers the benefit of quick submission to the particular area of the Office that needs to act on the correspondence. Also, EFS-Web submissions are "soft scanned" (i.e., electronically uploaded) directly into the official file for the reexamination proceeding, which offers parties the opportunity to review the content of their submissions after the "soft scanning" process is complete.

Any inquiry concerning this communication should be directed to Joseph R. Pokrzywa at telephone number 571-272-7410.

Signed:

Joseph R Pokrzywa
Primary Patent Examiner
Central Reexamination Unit 3992
(571) 272-7410

Conferees: /r.g.f./
ESK