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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/009,034	03/31/2008	5440749	0081-011X1	3309

40972 7590 11/19/2009

HENNEMAN & ASSOCIATES, PLC
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EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 11/19/2009

Please find below and/or attached an Office communication concerning this application or proceeding.

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CENTRAL REEXAMINATION UNIT

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EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. 90/009,034, 90/009,389, & 90/010,520

PATENT NO. 5440749.

ART UNIT 3992.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/009,389	01/16/2009	5440749	0081-011X2	9206

40972 7590 11/19/2009

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EXAMINER	
ART UNIT	PAPER NUMBER

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EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/009,034, 90/009,389, & 90/010,520*

PATENT NO. *5440749*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/010,520	04/30/2009	5440749	0081-011X3	9626

40972 7590 11/19/2009

HENNEMAN & ASSOCIATES, PLC
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EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 11/19/2009

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EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/009,034, 90/009,389 & 90/010,520*

PATENT NO. *5440749*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Office Action in Ex Parte Reexamination	Control No. 90/009,034, 90/009,389, & 90/010,520	Patent Under Reexamination 5440749	
	Examiner JOSEPH R. POKRZYWA	Art Unit 3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

a☒ Responsive to the communication(s) filed on *10/9/2009* . b☐ This action is made FINAL.
c☐ A statement under 37 CFR 1.530 has not been received from the patent owner.

A shortened statutory period for response to this action is set to expire 2 month(s) from the mailing date of this letter. Failure to respond within the period for response will result in termination of the proceeding and issuance of an *ex parte* reexamination certificate in accordance with this action. 37 CFR 1.550(d). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).** If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☒ Information Disclosure Statement, PTO/SB/08.
3. ☐ Interview Summary, PTO-474.
4. ☐ _____.

Part II SUMMARY OF ACTION

1a. ☒ Claims *1-27 and 30-54* are subject to reexamination.
1b. ☒ Claims *28 and 29* are not subject to reexamination.
2. ☐ Claims _____ have been canceled in the present reexamination proceeding.
3. ☒ Claims *21-27* are patentable and/or confirmed.
4. ☒ Claims *1-20 and 30-54* are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ The drawings, filed on _____ are acceptable.
7. ☐ The proposed drawing correction, filed on _____ has been (7a)☐ approved (7b)☐ disapproved.
8. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
   a)☐ All b)☐ Some* c)☐ None of the certified copies have
   1☐ been received.
   2☐ not been received.
   3☐ been filed in Application No. _____ .
   4☐ been filed in reexamination Control No. _____.
   5☐ been received by the International Bureau in PCT application No. _____.
   * See the attached detailed Office action for a list of the certified copies not received.
9. ☐ Since the proceeding appears to be in condition for issuance of an *ex parte* reexamination certificate except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte* Quayle, 1935 C.D. 11, 453 O.G. 213.
10. ☐ Other: _____

cc: Requester (if third party requester)

DETAILED ACTION

Response to Amendment

1. Patent Owner's amendment was received on 10/9/2009, and has been entered and made of record.

2. Original claims 1-29 issued on Aug. 8, 1995 of U.S. Patent Number 5,440,749 (hereafter "the '749 Patent"). The Patent Owner's amendment dated 10/9/2009 amends claim 1 and adds new claims 30-54.

3. Further, in accordance with the Office paper dated 9/24/2009, the reexamination proceedings of 90/009,034, 90/009,389, and 90/010,520, have been merged, with each being proceedings of the '749 Patent. In the '9034 proceeding, claim 1 is subject to reexamination, while claims 2-29 were not. In the '9389 proceeding, claims 1-27 are subject to reexamination, while claims 28 and 29 are not, and in the '10520 proceeding, claims 1, 9, 18, 23, and 24 are subject to reexamination, while claims 2-8, 10-17, 19-22, and 25-29 are not. Thus, with the merged proceedings, claims 1-27, and 30-54 of the '749 Patent are subject to reexamination, with claims 28 and 29 not being subject to reexamination.

4. This action is directed only to the claim for which reexamination was requested. With respect to such claims, requester(s) has alleged that a substantial new question of patentability

(SNQ) exists, and upon review, it has been determined that the alleged SNQ in fact is present for claims 1-27 of the '749 Patent. No determination was made with respect to the existence or nonexistence of an SNQ with respect to any claim for which reexamination was not specifically requested.

5. Further, the examiner notes that a Certificate of Correction was issued for the '749 Patent on May 26, 2009, which corrects the word "extend" in claim 1 to read "external", and corrects two placements of commas within the text of claim 1.

Information Disclosure Statement

6. The references listed in the Information Disclosure Statement submitted on 7/17/2009 have been received and entered into the record.

7. Continuing, the examiner notes that the numerous Office actions from related U.S. Patent Applications and the numerous Court documents submitted in the above noted Information Disclosure Statement have been received, and considered, but are not proper to be listed on an Information Disclosure Statement, as the documents are not proper be printed on the face of a Reexamination Certificate, once issued. Thus, these citations have been indicated as having a line through the citation in the Information Disclosure Statement.

8. Further, the examiner notes that MPEP 2256, under the heading "Prior Art Patents and Printed Publications Reviewed by Examiner in Reexamination" states, in part:

> Where patents, publications, and other such items of information are submitted by a party (patent owner or requester) in compliance with the requirements of the rules, **the requisite degree of consideration to be given to such information will be normally limited by the degree to which the party filing the information citation has explained the content and relevance of the information**. The initials of the examiner placed adjacent to the citations on the form PTO/SB/08A and 08B or its equivalent, without an indication to the contrary in the record, do not signify that the information has been considered by the examiner any further than to the extent noted above. [Emphasis added.]

9. Additionally, MPEP 609.05(b) states:

> The information contained in information disclosure statements which comply with both the content requirements of 37 CFR 1.98 and the requirements, based on the time of filing the statement, of 37 CFR 1.97 will be considered by the examiner. Consideration by the examiner of the information submitted in an IDS means that **the examiner will consider the documents in the same manner as other documents in Office search files are considered by the examiner while conducting a search of the prior art in a proper field of search**. The initials of the examiner placed adjacent to the citations on the ** PTO/SB/08A and 08B or its equivalent mean that the information has been considered by the examiner to the extent noted above. [Emphasis added.]

10. With this, the examiner notes that the prior art references listed in the Information Disclosure Statement submitted on 7/17/2009 have been considered by the examiner to at least the "degree to which the party filing the information citation has explained the content and relevance of the information", and in "the same manner as other documents in Office search files are considered by the examiner while conducting a search of the prior art in a proper field of search" (see attached PTO/SB/08A).

Claim Rejections - 35 USC § 112

11. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

12. **Claims 30 and 31** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

13. Particularly, the newly presented ***claims 30 and 31*** require that a means for executing multiple sequential instructions prior to fetching the next multiple sequential instructions. This feature is not believed to be expressly described in the specification of the '749 Patent. The Patent Owner states that the features are taught on col. 7, line 63- col. 8, line 16 of the '749 Patent. But in this section, the '749 Patent states "While the current instructions in instruction register 108 are executing, the memory controller obtains the address of the next set of four instructions...and obtains that set of instructions." Thus, with this, the executing appears to be at the same time as the fetching, and not "prior to fetching the next multiple sequential instructions."

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

15. **Claims 1, 9, and 18-20** are rejected under 35 U.S.C. 102(b) as being anticipated by the "IMS T414 Transputer Data Sheet", published by INMOS, Ltd., February 1987 (hereafter the "T414 Data Sheet").

Regarding ***claim 1***, the T414 Data Sheet discloses a microprocessor system, comprising

a central processing unit integrated circuit [see page 1, "The IMS T414 transputer is a 32-bit CMOS microcomputer with 2 Kbytes on-chip RAM."; also see page 3, wherein "The 32-bit processor contains instruction processing logic, instruction and work pointers, and an operand register.],

a memory external of said central processing unit integrated circuit [see page 19, wherein "The External Memory Interface (EMI) allows access to a 32bit address space, supporting dynamic and static RAM as well as ROM and EPROM."; also see the figure on page 26, whereby the Dynamic RAMs are external to the T414 integrated circuit],

a bus connecting said central processing unit integrated circuit to said memory [see figures on pages 1 and 26], and

means connected to said bus for fetching instructions for said central processing unit integrated circuit on said bus from said memory [see page 19, wherein "The External Memory Interface (EMI) allows access to a 32-bit address space, supporting dynamic and static RAM as well as ROM and EPROM."; also see the figure on page 26, whereby the T414 device is connected to external Dynamic RAM via a 32-bit multiplexed address/data bus; also see page 5, wherein "Furthermore, as memory is word addressed the processor will receive several instructions every fetch."],

said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle [see page 5, wherein "as memory is word accessed the processor will receive several instructions for every fetch", also wherein "a process is a sequence of instructions. A transputer can run several processes in parallel (concurrently)."; also see page 3, wherein "...six registers are used in the execution of a sequential process.", and also wherein "Each instruction consists of a single byte divided into two 4 bit parts."];

said bus having a width at least equal to a number of bits in each of the instructions times a number of the instructions fetched in parallel [see page 19, wherein "The External Memory Interface (EMI) allows access to a 32-bit address space, supporting dynamic and static RAM as well as ROM and EPROM."; also see page 3, wherein "Each instruction consists of a single byte divided into two 4-bit parts."],

said central processing unit integrated circuit including an arithmetic logic unit and a first push down stack connected to said arithmetic logic unit [see page 3, registers A, B, and C, wherein "A, B, and C are sources and destinations for most arithmetic and logical operations."],

said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input and means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input [see the figure on page 3; also see page 3, wherein "A, B, and C are sources and destinations for most arithmetic and logical operations. Loading a value into the stack pushes B into C, and A into B before loading A. Storing a value from A, pops B into A and C into B."],

a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack [see page 3, wherein "A, B, and C are sources and destinations for most arithmetic and logical operations. Loading a value into the stack pushes B into C, and A into B before loading A. Storing a value from A, pops B into A and C into B."],

said arithmetic logic unit having an output connected to said means for storing a top item [see figures on pages 1 and 3, also on page 3, wherein "A, B, and C are sources and destinations for most arithmetic and logical operations.", whereby the 32-bit processor that performs the arithmetic logic would thus inherently include a connection to the A register].

Regarding ***claim 9***, the T414 Data Sheet discloses a microprocessor system, comprising

a central processing unit [see page 1, "The IMS T414 transputer is a 32-bit CMOS microcomputer with 2 Kbytes on-chip RAM."; also see page 3, wherein "The 32-bit processor contains instruction processing logic, instruction and work pointers, and an operand register."],

a dynamic random access memory [see the figure on page 26, which includes external Dynamic RAM],

a bus connecting said central processing unit to said dynamic random access memory [see figures on pages 1 and 26], and

multiplexing means on said bus between said central processing unit and said dynamic random access memory [see page 26, "Row/Column address multiplexer"],

said multiplexing means being connected and configured to provide multiplexed row addresses, column addresses and data on said bus from said central processing unit to said dynamic random access memory and to provide data from said dynamic random access memory to said central processing unit [see figure on page 26], and

means connected to said bus for fetching instructions for said central processing unit on said bus from said dynamic random access memory [see figure on page 26],

said means for fetching instructions being configured to fetch multiple sequential instructions from said dynamic random access memory in parallel and supply the multiple instructions to said central processing unit during a single memory cycle [see page 5, wherein "as memory is word accessed the processor will receive several instructions for every fetch", also wherein "a process is a sequence of instructions. A transputer can run several processes in parallel (concurrently)."; also see page 3, wherein "...six registers are used in the execution of a

sequential process.", and also wherein "Each instruction consists of a single byte divided into two 4 bit parts."];

said central processing unit including an arithmetic logic unit and a first push down stack connected to said arithmetic logic unit [see page 3, registers A, B, and C, wherein "A, B, and C are sources and destinations for most arithmetic and logical operations."],

said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input [see figures on pages 1 and 3, also on page 3, wherein "A, B, and C are sources and destinations for most arithmetic and logical operations.", whereby the 32-bit processor that performs the arithmetic logic would thus inherently include a connection to the A register], and

means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input, a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack, said arithmetic logic unit having an output connected to said means for storing a top item [see figure on page 3, also see page 3, wherein "A, B, and C are sources and destinations for most arithmetic and logical operations. Loading a value into the stack pushes B into C, and A into B before loading A. Storing a value from A, pops B into A and C into B."].

Regarding ***claim 18***, the T414 Data Sheet discloses the system discussed above in claim 9, and further teaches of

a programmable read only memory containing instructions connected to said bus [see page 3, wherein "Where larger amount of memory or programs in ROM are required..."; also see page 16, wherein "The transputer can be bootstrapped either from a link or from external ROM. To facilitate debugging, BootFromRom may be dynamically changed, but must obey the specified timing restrictions."],

means connected to said bus for fetching instructions for said central processing unit on said bus [see page 19, wherein "The External Memory Interface (EMI) allows access to a 32-bit address space, supporting dynamic and static RAM as well as ROM and EPROM."; also see the figure on page 26, whereby the T414 device is connected to external Dynamic RAM via a 32-bit multiplexed address/data bus; also see page 5, wherein "Furthermore, as memory is word addressed the processor will receive several instructions every fetch."],

said means for fetching instructions including means for assembling a plurality of instructions from said programmable read only memory [see page 17, wherein "The IMS T414 has 2 Kbytes of fast of fast internal memory for high rates of data throughput....The transputer can also access 4 Gbytes of external memory space. Internal and external memory are part of the same linear address space."; also see page 18, wherein "Memory configuration data and ROM bootstrapping code must be in the most positive address space...Address space immediately below this is conventionally used for ROM based code."],

storing the plurality of instructions in said dynamic random access memory and subsequently supplying the plurality of instructions from said dynamic random access memory to said central processing unit on said bus [see page 20; also see pages 26 and 27].

Regarding ***claim 19***, the T414 Data Sheet discloses the system discussed above in claim 9, and further teaches of a direct memory access processing unit having the capacity to request and execute instructions [see front page, whereby the T414 Transputer includes an "Internal program continues during DMA"], said bus connecting said direct memory access processing unit to said dynamic random access memory [see illustration on page 26], said dynamic random access memory containing instructions for said central processing unit and said direct memory access processing unit, said direct memory access processing unit being connected to means for fetching instructions for said central processing unit on said bus and for fetching instructions for said direct memory access processing unit on said bus [see page 2, whereby the external memory interface includes the function for "direct memory access request" and "direct memory access granted"; also see the illustration on page 1; also see page 20, wherein "...DMA (memory request) activity takes place, when the bus will carry the appropriate external address or data."].

Regarding ***claim 20***, the T414 Data Sheet discloses the system discussed above in claim 19, and further teaches of a variable speed system clock connected to said central processing unit and a fixed speed system clock [see page 7, wherein "The transputer has two 32 bit timer clocks which "tick" periodically."; also see page 6, wherein "The time slice period is 5120 cycles of ClockIn, giving ticks approximately 1ms apart."; also see page 14] connected to control said

means for fetching instructions for said central processing unit and for fetching instructions for said direct memory access processing unit [see page 14, wherein "Memory request (DMA) must not occur whilst Reset is high but can occur before boot."; also see page 2, with the memory interface including the functions of "direct memory access request" and "direct memory access granted"].

16. **Claims 1-2, 7, 8, 30-53** are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent Number 4,758,948, issued to May *et al.* on July 19, 1988 (hereafter "May'948"), whereby the examiner notes that the reference of U.S. Patent Number 4,680,698, issued to Edwards *et al.* on Jul. 14, 1987 (hereafter "Edwards'698") was incorporated by reference in the May'948 reference on col. 5, lines 7-18.

Regarding ***claim 1***, May'948 discloses a microprocessor system [see Figs. 1 and 2], comprising

a central processing unit integrated circuit [CPU 12, see Fig. 1; also see col. 4, lines 42-49],

a memory external of said central processing unit integrated circuit [see col. 4, lines 62-65, wherein "An external memory interface 23 is provided and connected to a plurality of pins 24 for connection to an optional external memory."],

a bus connecting said central processing unit integrated circuit to said memory [see Figs. 1 and 2, bidirectional data bus 31, and bus 16; also see col. 7, lines 15-25], and

means connected to said bus for fetching instructions for said central processing unit integrated circuit on said bus from said memory [memory interface 14, see col. 4, lines 48-56],

said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle [col. 7, lines 26-27, wherein "each instruction consists of 8 bits..."; also see col. 6, lines 10-13, wherein "The processor accesses the memory in words...(in this particular example 16 bits).";

also see col. 7, lines 22-25, wherein "Communications between the CPU and the memory is effected via ...data bus 31."; also see Fig. 2, whereby the bus 31 is split so that instructions are transferred in parallel to another priority register bank;

said bus having a width at least equal to a number of bits in each of the instructions times a number of the instructions fetched in parallel [col. 7, lines 26-27, wherein "each instruction consists of 8 bits..."; also see col. 5, line 64-col. 6, line 13, wherein "...the particular wordlength of the example described is 16 bits but it will be understood that other wordlengths such as 8, 16, 24, 32 or other wordlengths may be used....The processor accesses the memory in words...(in this particular example 16 bits)."; also see col. 7, lines 61-62, where a register supplies data, being at least 16 bits, on data bus 31],

said central processing unit integrated circuit including an arithmetic logic unit and a first push down stack connected to said arithmetic logic unit [ALU 30, see Figs. 1 and 2; also see col. 3, lines 33-38],

said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input and means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input [see col. 8, lines 47-56, wherein "The A, B, and C register stack 54, 55, and 56 are...organised as a stack so that the loading of a value into the A register is preceded by relocating the existing contents of the B register into the C register and from the A register into the B register. Similarly storing a value derived from the A register causes the contents of the B register to be moved into the A register and the contents of the C register into the B register."],

a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack [see col. 8, lines 50-52, wherein "the loading of a value into the A register is preceded by relocating the existing contents of the B register into the C register..."],

said arithmetic logic unit having an output connected to said means for storing a top item [see col. 8, lines 47-49, wherein "The A, B, and C register stack 54, 55, and 56 are the sources and destinations for most arithmetic and logical operations."; also see Fig. 2].

Regarding ***claim 2***, May'948 discloses the system discussed above in claim 1, and further teaches of

means connected to said means for fetching multiple instructions for determining by decoding the multiple instructions if multiple instructions fetched by said means for fetching multiple instructions require a memory access [see col. 7, lines 26-39, wherein "each instruction consists of 8 bits having the format shown in Fig. 7. 4 bits represent the required function of the instruction and 4 bits are allocated for data. Each instruction derived from the program sequence for the process is fed into an instruction buffer 34 and the instruction is decoded by the decoder 35."],

said means for fetching multiple instructions fetching additional multiple instructions if decoding the multiple instructions shows that the multiple instructions do not require a memory access [see col. 9, lines 7-9 and 31-33].

Regarding ***claim*** *7*, May'948 discloses the system discussed above in claim 1, and further teaches of

an instruction register for the multiple instructions [see Fig. 2, "instruction buffer IB 34"; also see col. 7, lines 29-31, wherein "Each instruction derived from the program sequence for the process is fed to an instruction buffer 34."] and a variable width operand to be used with one of the multiple instructions connected to said means for fetching instructions [see Figs. 2 and 3, "O REG register 57"; also see col. 8, lines 25-28, wherein "An operand register 57 for receiving the data derived from an instruction in the instruction buffer 34, and used as a temporary register."],

means connected to said instruction register for supplying the multiple instructions in succession from said instruction register [see col. 7, lines 29-35, wherein "Each instruction derived from the program sequence for the process is fed to an instruction buffer 34 and the instruction is decoded by a decoder 35. The output of the decoder is fed through a condition multiplexer 36 to a microinstruction register 37 used for addressing the microinstruction ROM 13."],

a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession [see col. 35, lines 44-46, wherein "The IPTR REG (0) contains a pointer 180 to the next instruction in the program sequence 181 which is stored in memory", whereby the "instruction pointer IPTR" is considered as a "counter"],

means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions [see Fig. 2, "decoder 35"; also see col. 7, lines 29-35, wherein "Each instruction derived from the program

sequence for the process is fed to an instruction buffer 34 and the instruction is decoded by a decoder 35."],

said counter being connected to said means for decoding to receive incrementing and reset control signals from said means for decoding [see Fig. 2; also see Edwards'698 Fig. 3, and also in col. 21, lines 64-68, wherein "At the start of each instruction, the instruction pointer is incremented. Consequently the instruction pointer always points to the next instruction to be executed. As mentioned, the instruction pointer IPTR is stored in register 67."],

said means for decoding being configured to control said counter in response to an instruction utilizing the variable width operand stored in said instruction register, and means connected to said counter to select the variable width operand for use with the instruction utilizing the variable width operand in response to said counter [see col. 27, lines 1-18; also see Edwards'698 Patent, in col. 30, lines 37-46, wherein "The instruction to be executed next by the processor for the current process is pointed to by the contents of the IPTR register 67 which contains the instruction pointer. The jump instruction adds the contents of the operand register 65 to the instruction pointer."].

Regarding ***claim 8***, May'948 discloses a microprocessor system [see Figs. 1 and 2], comprising

a central processing unit [CPU 12, see Figs. 1 and 2],

a memory [RAM 19 and ROM 20],

a bus connecting said central processing unit to said memory [bidirectional data bus 31; also see col. 7, lines 15-25], and

means connected to said bus for fetching instructions for said central processing unit on said bus from said memory [see Fig. 2],

said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit during a single memory cycle [col. 7, lines 26-27, wherein "each instruction consists of 8 bits..."; also see col. 6, lines 10-13, wherein "The processor accesses the memory in words...(in this particular example 16 bits)."; also see col. 7, lines 22-25, wherein "Communications between the CPU and the memory is effected via ...data bus 31."; also see Fig. 2, whereby the bus 31 is split so that instructions are transferred in parallel to another priority register bank],

said central processing unit including an arithmetic logic unit [ALU 30] and a first push down stack [being the A, B, and C register stack 54, 55, and 56 in the priority 1 register bank 38, as seen in Fig. 2] connected to said arithmetic logic unit [see Fig. 2 and 10],

said first push down stack further including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input, means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input [see col. 8, lines 47-56, wherein "The A, B, and C register stack 54, 55, and 56 are...organised as a stack so that the loading of a value into the A register is preceded by relocating the existing contents of the B register into the C register and from the A register into the B register. Similarly storing a value derived from the A register causes the contents of the B register to be moved into the A register and the contents of the C register into the B register."],

said arithmetic logic unit having an output connected to said means for storing a top item see Fig. 2, whereby the Z Bus is connected to the A register 54],

a second push down stack [being the A, B, and C registers within the priority 0 register bank 39; also see col. 7, line 40-col. 8, line 43, wherein "Register bank 38 is provided for the priority 1 processes and a similar register bank 39 is provided for the high priority 0 processes. ...The bank of registers 39 for priority 0processes is the same as that already described for priority 1 processes."], said means for storing a top item being connected to provide an input to said second push down stack and a control means connected between said means for storing a top item and said second push down stack for controlling provision of the input to said second push down stack [see Fig. 2],

said second push down stack additionally being configured as a register file and said means for storing a top item and said second push down stack additionally configured as the register file being bidirectionally connected [see Fig. 2, whereby both register banks 38 and 39 are connected to bidirectional data bus 31].

Regarding ***claim 30***, May'948 discloses the system discussed above in claim 1, and further teaches that said central processing unit integrated circuit includes means for executing said multiple sequential instructions prior to said fetching means fetching next multiple sequential instructions [see col. 21, line 33-col. 22, line 2, wherein "The actions may be performed on behalf of the current process are to perform "StartNextProcess", to perform "BlockCopyStep" or to fetch, decode and execute an instruction.", and also wherein "Otherwise the processor will fetch, decode and execute an instruction if there is a current process."].

Regarding ***claim 31***, May'948 discloses the system discussed above in claim 30, and further teaches that said means for executing are configured to determine whether to execute said multiple sequential instructions prior to said fetching means fetching said next multiple sequential instructions based on said multiple sequential instructions [see col. 21, line 33-col. 22, line 2].

Regarding ***claim 32***, May'948 discloses the system discussed above in claim 1, and further teaches that said means for fetching are configured to selectively fetch next multiple sequential instructions in response to execution of said multiple sequential instructions [see col. 21, line 33-col. 22, line 2, wherein "The actions may be performed on behalf of the current process are to perform "StartNextProcess", to perform "BlockCopyStep" or to fetch, decode and execute an instruction.", and also wherein "Otherwise the processor will fetch, decode and execute an instruction if there is a current process."].

Regarding ***claim 33***, May'948 discloses the system discussed above in claim 32, and further teaches that said means for fetching are configured to fetch said next multiple sequential instructions prior to completion of execution of said multiple sequential instructions [see col. 21, line 33-col. 22, line 2, wherein "The actions may be performed on behalf of the current process are to perform "StartNextProcess", to perform "BlockCopyStep" or to fetch, decode and execute an instruction.", and also wherein "Otherwise the processor will fetch, decode and execute an instruction if there is a current process. Otherwise the processor will wait until there is a channel request."].

Regarding ***claim 34***, May'948 discloses the system discussed above in claim 1, and further teaches that said central processing unit integrated circuit includes an instruction register configured to store said multiple sequential instructions [see Fig. 2; also see col. 7, line 41-col. 8, line 34; also see Fig. 3, whereby IPTR 50 is used for the current instruction and IPTR S 65 is used for a process that is not the current process, see col. 9, lines 59-67],

said central processing unit integrated circuit being configured to access an operand located in a first instruction location of the instruction register in response to an instruction of the multiple sequential instructions in a second instruction location of the instruction register distinct from the first instruction location [see col. 7, lines 40-col. 8, line 62; also see col. 9, lines 59-67, wherein "Location 65 is used when a process is not the current process to hold a pointer (IPTR) to the next instruction to be executed by the process when it becomes the current process."].

Regarding ***claim 35***, May'948 discloses the system discussed above in claim 34, and further teaches that said central processing unit integrated circuit is configured to access the operand in response to an op-code of the instruction in the second instruction location [operand register OREG 57, see col. 8, line 63-col. 9, line 4; also see the Edwards'698 Patent, whereby the various "operation codes" are described in col. 23, lines 2-20, as well as in col. 29, line 28-col. 32, line 24].

Regarding ***claim 36***, May'948 discloses the system discussed above in claim 1, and further teaches of an instruction register configured to store the multiple sequential instructions in corresponding instruction locations including a particular location for storing an instruction to

be executed [col. 7, lines 40-col. 8, line 62; also see col. 9, lines 59-67, wherein "Location 65 is used when a process is not the current process to hold a pointer (IPTR) to the next instruction to be executed by the process when it becomes the current process."], the central processing unit integrated circuit being configured to respond to content of an instruction of the multiple sequential instructions by accessing the particular location of the instruction register [see col. 7, line 56-col. 8, line 34; also see col. 9, lines 59-67].

Regarding ***claim 37***, May'948 discloses the system discussed above in claim 36, and further teaches that the central processing unit integrated circuit is configured to respond to content of the instruction of the multiple sequential instructions by accessing the particular location of the instruction register after the means for fetching fetches next multiple sequential instructions [see col. 7, lines 40-col. 8, line 62; also see col. 9, lines 59-67, wherein "Location 65 is used when a process is not the current process to hold a pointer (IPTR) to the next instruction to be executed by the process when it becomes the current process."].

Regarding ***claim 38***, May'948 discloses the system discussed above in claim 36, and further teaches that the central processing unit integrated circuit is configured to respond to content of the instruction of the multiple sequential instructions by accessing the first-execution location of the instruction register without the fetching means fetching next multiple sequential instructions [see col. 7, lines 40-col. 8, line 62; also see col. 9, lines 59-67, wherein "Location 65 is used when a process is not the current process to hold a pointer (IPTR) to the next instruction to be executed by the process when it becomes the current process."].

Regarding ***claim 39***, May'948 discloses the system discussed above in claim 36, and further teaches that the content is an op-code [see the Edwards '698 Patent, whereby the various "operation codes" are described in col. 23, lines 2-20, as well as in col. 29, line 28-col. 32, line 24].

Regarding ***claim 40***, May'948 discloses the system discussed above in claim 1, and further teaches that the multiple sequential instructions comprise a first plurality of sequential instructions arranged from beginning to ending positions of the first plurality of sequential instructions [see Fig. 3; also see col. 9, lines 25-67, wherein "Location 65 is used when a process is not the current process to hold a pointer (IPTR) to the next instruction to be executed by the process when it becomes the current process."; also see col. 35, lines 12-32, wherein "...an instruction pointer (IPTR) in the IPTR REG 50 indicates the next instruction to be executed from the sequence of instructions in the program relating to that particular process....When a process is scheduled it either becomes the current process or is added to a list or queue of processes waiting execution. Such a list is formed as a linked list with each process on the list having a pointer in the link location 66 of its workspace to the workspace of the next process on that list."],

the central processing unit integrated circuit being configured to respond to content of a first instruction of the first plurality of sequential instructions by accessing a second instruction in a second plurality of sequential instructions arranged from beginning to ending positions of the second plurality of sequential instructions, the second instruction being in the beginning position of the second plurality of sequential instructions [see col. 9, lines 5-67; also see col. 35, lines 12-53, wherein "...an instruction pointer (IPTR) in the IPTR REG 50 indicates the next

instruction to be executed from the sequence of instructions in the program relating to that particular process....When a process is scheduled it either becomes the current process or is added to a list or queue of processes waiting execution. Such a list is formed as a linked list with each process on the list having a pointer in the link location 66 of its workspace to the workspace of the next process on that list.", also wherein "the processor maintains two lists of processes which are waiting to be executed, one for each priority level."; also see Figs. 3 and 4].

Regarding ***claim 41***, May'948 discloses the system discussed above in claim 40, and further teaches that the second plurality of sequential instructions is distinct from the first plurality of sequential instructions [see col. 35, lines 12-53, wherein "...an instruction pointer (IPTR) in the IPTR REG 50 indicates the next instruction to be executed from the sequence of instructions in the program relating to that particular process....When a process is scheduled it either becomes the current process or is added to a list or queue of processes waiting execution. Such a list is formed as a linked list with each process on the list having a pointer in the link location 66 of its workspace to the workspace of the next process on that list.", also wherein "the processor maintains two lists of processes which are waiting to be executed, one for each priority level."].

Regarding ***claim 42***, May'948 discloses the system discussed above in claim 40, and further teaches that the second plurality of sequential instructions is the first plurality of sequential instructions and the first instruction is disposed in a position other than the beginning position of the first plurality of instructions [see Fig. 3; also see col. 35, lines 12-53, wherein

"...an instruction pointer (IPTR) in the IPTR REG 50 indicates the next instruction to be executed from the sequence of instructions in the program relating to that particular process....When a process is scheduled it either becomes the current process or is added to a list or queue of processes waiting execution. Such a list is formed as a linked list with each process on the list having a pointer in the link location 66 of its workspace to the workspace of the next process on that list."].

Regarding ***claim 43***, May'948 discloses the system discussed above in claim 40, and further teaches that the content is an op-code [see the Edwards '698 Patent, whereby the various "operation codes" are described in col. 23, lines 2-20, as well as in col. 29, line 28-col. 32, line 24].

Regarding ***claim 44***, May'948 discloses the system discussed above in claim 1, and further teaches that the central processing unit integrated circuit includes an instruction register having a plurality of instruction locations for storing the multiple sequential instructions according to an order [see col. 7, line 40-col. 8, line 67; also see Fig. 3; also see col. 35, lines 12-53, wherein "...an instruction pointer (IPTR) in the IPTR REG 50 indicates the next instruction to be executed from the sequence of instructions in the program relating to that particular process....When a process is scheduled it either becomes the current process or is added to a list or queue of processes waiting execution. Such a list is formed as a linked list with each process on the list having a pointer in the link location 66 of its workspace to the workspace of the next process on that list."],

the plurality of instruction locations including a first location to be accessed before any other of the plurality of instruction locations [see col. 35, lines 12-53, wherein "...an instruction pointer (IPTR) in the IPTR REG 50 indicates the next instruction to be executed from the sequence of instructions in the program relating to that particular process....When a process is scheduled it either becomes the current process or is added to a list or queue of processes waiting execution. Such a list is formed as a linked list with each process on the list having a pointer in the link location 66 of its workspace to the workspace of the next process on that list."],

the central processing unit integrated circuit further including means for accessing a next instruction out of the order, the next instruction being located at the first location [see col. 35, lines 12-53, wherein "...an instruction pointer (IPTR) in the IPTR REG 50 indicates the next instruction to be executed from the sequence of instructions in the program relating to that particular process....When a process is scheduled it either becomes the current process or is added to a list or queue of processes waiting execution. Such a list is formed as a linked list with each process on the list having a pointer in the link location 66 of its workspace to the workspace of the next process on that list."].

Regarding ***claim 45***, May'948 discloses the system discussed above in claim 1, and further teaches that

the central processing unit integrated circuit includes an instruction register having a plurality of instruction locations for storing the multiple sequential instructions, the plurality of instruction locations including a first location to be accessed before any other of the plurality of instruction locations [see col. 35, lines 12-53, wherein "...an instruction pointer (IPTR) in the

IPTR REG 50 indicates the next instruction to be executed from the sequence of instructions in the program relating to that particular process....When a process is scheduled it either becomes the current process or is added to a list or queue of processes waiting execution. Such a list is formed as a linked list with each process on the list having a pointer in the link location 66 of its workspace to the workspace of the next process on that list.", also wherein "the processor maintains two lists of processes which are waiting to be executed, one for each priority level."; also see the various examples in Figs. 16A-21C],

the central processing unit integrated circuit further including means, responsive to content of an instruction of the multiple sequential instructions in a location other than the first location, for accessing a next instruction at the first location [see col. 35, lines 12-53, wherein "...an instruction pointer (IPTR) in the IPTR REG 50 indicates the next instruction to be executed from the sequence of instructions in the program relating to that particular process....When a process is scheduled it either becomes the current process or is added to a list or queue of processes waiting execution. Such a list is formed as a linked list with each process on the list having a pointer in the link location 66 of its workspace to the workspace of the next process on that list.", also wherein "the processor maintains two lists of processes which are waiting to be executed, one for each priority level."].

Regarding ***claim 46***, May'948 discloses the system discussed above in claim 1, and further teaches that said central processing unit integrated circuit includes a program counter comprising address bits [whereby the "instruction pointer IPTR" is considered as a counter], said fetching means configured to locate the multiple sequential instructions using the address bits from the program counter [see col. 35, line 12-col. 36, line 2].

Regarding ***claim 47***, May'948 discloses the system discussed above in claim 46, and further teaches that the address bits are a most significant bit portion from the program counter [see Fig. 7; also see col. 7, lines 26-40].

Regarding ***claim 48***, May'948 discloses the system discussed above in claim 47, and further teaches that the central processing unit integrated circuit is configured to increment the address bits of the program counter after said means for fetching multiple sequential instructions fetches the multiple sequential instructions [see Fig. 2; also see Edwards'698 Patent in Fig. 3, and also in col. 21, lines 64-68, wherein "At the start of each instruction, the instruction pointer is incremented. Consequently the instruction pointer always points to the next instruction to be executed. As mentioned, the instruction pointer IPTR is stored in register 67."].

Regarding ***claim 49***, May'948 discloses the system discussed above in claim 47, and further teaches that the most significant bit portion is 30 of 32 bits of the program counter [see Figs. 5 and 6; also see col. 6, lines 4-23].

Regarding ***claim 50***, May'948 discloses the system discussed above in claim 47, and further teaches of an instruction register having a plurality of instruction locations for storing the multiple sequential instructions [see Fig. 3; also see col. 35, lines 12-53, wherein "...an instruction pointer (IPTR) in the IPTR REG 50 indicates the next instruction to be executed from the sequence of instructions in the program relating to that particular process....When a process is scheduled it either becomes the current process or is added to a list or queue of processes waiting execution. Such a list is formed as a linked list with each process on the list having a pointer in the link location 66 of its workspace to the workspace of the next process on that list."], and multiplexer means connected to said instruction register for selectively supplying multiple instructions from said instruction register [see col. 7, lines 26-40, wherein "The output of the decoder is fed through a condition multiplexor 36 to a microinstruction register 37..."].

Regarding ***claim 51***, May'948 discloses the system discussed above in claim 47, and further teaches that the multiple sequential instructions comprise a first plurality of sequential instructions, the central processing unit integrated circuit being configured to respond to content of a first instruction of the first plurality of sequential instructions by accessing a second plurality of sequential instructions using an address specified by the address bits [see col. 35, lines 12-53, wherein "...an instruction pointer (IPTR) in the IPTR REG 50 indicates the next instruction to be executed from the sequence of instructions in the program relating to that particular process....When a process is scheduled it either becomes the current process or is added to a list or queue of processes waiting execution. Such a list is formed as a linked list with each process on the list having a pointer in the link location 66 of its workspace to the workspace of the next

process on that list.", also wherein "the processor maintains two lists of processes which are waiting to be executed, one for each priority level."].

Regarding ***claim 52***, May'948 discloses the system discussed above in claim 51, and further teaches that the second plurality of sequential instructions is distinct from the first plurality of sequential instructions [see col. 35, lines 12-53, wherein "...an instruction pointer (IPTR) in the IPTR REG 50 indicates the next instruction to be executed from the sequence of instructions in the program relating to that particular process....When a process is scheduled it either becomes the current process or is added to a list or queue of processes waiting execution. Such a list is formed as a linked list with each process on the list having a pointer in the link location 66 of its workspace to the workspace of the next process on that list.", also wherein "the processor maintains two lists of processes which are waiting to be executed, one for each priority level."].

Regarding ***claim 53***, May'948 discloses the system discussed above in claim 51, and further teaches that the content is an op-code [see the Edwards '698 Patent, whereby the various "operation codes" are described in col. 23, lines 2-20, as well as in col. 29, line 28-col. 32, line 24].

Regarding ***claim 54***, May'948 discloses the system discussed above in claim 47, and further teaches of an instruction register having a plurality of instruction locations ordered from a beginning instruction location to an ending instruction location, wherein the central processing unit integrated circuit is configured to respond to content in an instruction location other than the beginning instruction location by accessing the beginning instruction location [see Figs. 3 and 4; also see col. 35, lines 12-53, wherein "...an instruction pointer (IPTR) in the IPTR REG 50 indicates the next instruction to be executed from the sequence of instructions in the program relating to that particular process....When a process is scheduled it either becomes the current process or is added to a list or queue of processes waiting execution. Such a list is formed as a linked list with each process on the list having a pointer in the link location 66 of its workspace to the workspace of the next process on that list."].

17. **Claims 1-6 and 8** are rejected under 35 U.S.C. 102(b) as being anticipated by "The Motorola MC68020", written by Doug MacGregor *et al.*, IEEE Micro, August 1984, pages 101-118 (hereafter "MacGregor") in view of the reference "MC68020 32-Bit Microprocessor User's Manual", published by Motorola, having a copyright dated of 1984 (hereafter the "MC68020 User's Manual").

18. The examiner notes that MPEP 2131.01 states in part:

> Normally, only one reference should be used in making a rejection under 35 U.S.C. 102. However, a 35 U.S.C. 102 rejection over multiple references has been held to be proper when the extra references are cited to:
>
> (A) Prove the primary reference contains an "enabled disclosure;"
> (B) Explain the meaning of a term used in the primary reference; or
> (C) Show that a characteristic not disclosed in the reference is inherent.

19. In the instant rejection of independent ***claims 1 and 8,*** and the corresponding dependent claims, the secondary reference of the MC68020 User's Manual is being utilized to show the features that are summarized in the MacGregor reference are inherent in the MC68020 microprocessor. The examiner notes that both of these references describe the Motorola MC68020 microprocessor, with the MC68020 User's Manual giving a more thorough description of the microprocessor disclosed in the MacGregor reference. A full discussion follows below.

Regarding ***claim 1***, MacGregor discloses a microprocessor system, comprising

a central processing unit integrated circuit [see Figure 1 on page 108, being a photograph of the MC68020 integrated circuit],

a memory external of said central processing unit integrated circuit [see page 107, wherein "The enable bit controls the MC68020's use of cache...if it is clear, the cache is disabled and the processor always fetches from external memory."],

a bus connecting said central processing unit integrated circuit to said memory [see page 101, wherein "The MC68020 adds full 32-bit data paths (internal and external)..."], and

means connected to said bus for fetching instructions for said central processing unit integrated circuit on said bus from said memory [see page 101, wherein ; also see page 107, wherein "...the processor always fetches from external memory."],

said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle [see page 107, wherein "The cache interface to the processor data paths allows complete overlap of instruction fetches with data operand accesses, and thus provides a significant increase in performance. If simultaneous instruction and data operand requests are generated by the micromachine, a hit in the instruction cache allows concurrent fetches to take place."; also see page 111, wherein "Figure 10 illustrates that data and instruction addresses are calculated in parallel and have separate paths to the address pads. This allows a simultaneous instruction and data access if there is a hit in the cache while a data access is taking place."],

said bus having a width at least equal to a number of bits in each of the instructions times a number of the instructions fetched in parallel [see Table 2 on page 103, whereby the instructions are shown to be up to 32-bits; also see page 111, wherein "...there is appreciable gain from the 32-bit bus for instruction accesses. Although instructions are of word length and are

fetched a word at a time in the MC68000, there is a benefit in fetching two words at a time, because the instruction stream is sequential in nature."],

said central processing unit including an arithmetic logic unit [see page 101, whereby the MC68020 includes "three 32-bit arithmetic units"],

said first push down stack including means for storing a top item [see Figures 1 and 2 on page 104; also see page 106, wherein "An additional primitive allows transfer of operands to/from the top of the active system stack."] connected to a first input of said arithmetic logic unit [see Figure 2 on page 109] to provide the top item to the first input and means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input [see Figures 1 and 2 on page 104],

a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack [being inherent in a push down stack system],

said arithmetic logic unit having an output connected to said means for storing a top item [see Figure 2 on page 109].

Further, the MC68020 User's Manual additionally describes the MC68020 microprocessor comprising

a memory external of said central processing unit integrated circuit [see Figure 9-1 on page 8-3],

a bus connecting said central processing unit integrated circuit to said memory [see Figure 8-1 on page 8-3, whereby the external memory is connected to the MC68020 via the buses to carry A0-A31 and D0-D31], and

means connected to said bus for fetching instructions for said central processing unit integrated circuit on said bus from said memory [see Figure 1-1 on page 1-2; also see Figure 1-5 on page 1-9],

said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle [see page 1-1, wherein "..the internal operations of this microprocessor are designed to operate in parallel, allowing multiple instructions to be executed concurrently."; also see page 1-8, wherein "Instructions are loaded from the on-chip cache or from external memory during instruction prefetch into stage B."; also see Figure 9-1 on page 9-2],

said central processing unit integrated circuit including an arithmetic logic unit [see Figure 1-1 on page 1-2],

said first push down stack including means for storing a top item [see Figures 1-2 and 1-3 on page 1-3; also see the illustrations on pages 2-21 through 2-24] connected to a first input of said arithmetic logic unit [see Figure 1-1 on page 1-2; also see page 1-2, wherein "Registers A0-A6 and the user, interrupt, and master stack pointers are address registers that may be used as software stack pointers or base address registers."] to provide the top item to the first input and means for storing a next item connected to a second input of said arithmetic logic unit to provide

the next item to the second input [see the illustrations on pages 2-21 through 2-24; also see page 2-20, wherein "Each system stack fills from high to low memory."],

a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack [see page 2-21, wherein "Stack growth from high to low memory is implemented with –(An) to push data on the stack, (An)+ to pull data from the stack. After either a push or a pull operation, register An points to the top item on the stack."],

said arithmetic logic unit having an output connected to said means for storing a top item [see Figure 1-1 on page 1-2].

Regarding ***claim 2***, MacGregor discloses the system discussed above in claim 1, and further teaches of

means connected to said means for fetching multiple instructions for determining by decoding the multiple instructions if multiple instructions fetched by said means for fetching multiple instructions require a memory access, said means for fetching multiple instructions fetching additional multiple instructions if decoding the multiple instructions shows that the multiple instructions do not require a memory access [see page 114, wherein "If succeeding instructions have no need to use the external bus – as is the case for register-to-register operation, branching, and other instructions which hit in the instruction cache and have no external data transfers – then these instructions may have their execution times totally absorbed by the previous write cycle."].

Regarding ***claim 3***, MacGregor discloses the system discussed above in claim 2, and further teaches that the decoding determines if the multiple instructions do not require a memory access by a state of a bit of each of the multiple instructions [see the MC68020 User's Manual, page 7-1, wherein "Address bit A1 is used to select the proper word from the cache entry and the cycle ends. If there is no match, or the valid bit is clear, a cache miss occurs and the instruction is fetched from external memory. This new instruction is automatically written into the cache entry..."].

Regarding ***claim 4***, MacGregor discloses the system discussed above in claim 3, and further teaches that the bit is a most significant bit of the multiple instructions [see the MC68020 User's Manual, page 7-1, wherein "Address bit A1 is used to select the proper word from the cache entry and the cycle ends. If there is no match, or the valid bit is clear, a cache miss occurs and the instruction is fetched from external memory. This new instruction is automatically written into the cache entry..."].

Regarding ***claim 5***, MacGregor discloses the system discussed above in claim 1, and further teaches of an instruction register for the multiple instructions connected to said means for fetching instructions [see page 112, wherein "The depth of the instruction pipe on the MC68020 is three words."; also see Fig. 12 on page 114],

means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession [see Figure 1 on page

104, having a "program counter"; also see page 102, wherein "The MC68000 family supports 14 addressing modes including ...program-counter-relative"],

means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions [see page 109, wherein "The decode PLAs (A1 and A5/A6) have microcode sequences which decode all possible instruction words and accumulate the resulting outputs into a signature register that can then be read out and checked.", also wherein "The instruction pipe and other miscellaneous control sections provide the secondary decode of instructions and generate the actual control signals that result in the decoding and interpretation of the control store."; also see Figure 2 on page 109],

said counter being connected to said means for decoding to receive incrementing and reset control signals from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and to supply a control signal to said means for fetching instructions in response to a SKIP instruction in the multiple instructions [see page 104, also see the MC68020 User's Manual, page 8-10, wherein "This allows the main processor to ...skip them to locate the next instruction."; also for instance, see the MC68020 User's Manual, page B-101, showing the "MOVE" instruction, which sets condition codes to be cleared].

Regarding ***claim 6***, MacGregor discloses the system discussed above in claim 5, and further teaches of a loop counter connected to receive a decrement control signal from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and the decrement control signal to said loop counter in response to a

MICROLOOP instruction in the multiple instructions to provide a microloop within the multiple instructions in said instruction register for a number of repetitions controlled by said loop counter [see the MC68020 User's Manual, page B-77, wherein "This instruction is a looping primitive of three parameters: a condition, a counter (data register), and a displacement. The instruction first tests the condition to determine if the termination condition for the loop has been met, and if so, no operation is performed. If the termination condition is not true, the low order 16 bits of the counter data register are decemented by one. If the result is -1, the counter is exhausted and execution continues with the next instruction. If the result is not equal to -1, execution continues at the location indicated by the current value of the PC [program counter plus the sign-extended 16-bit displacement."].

Regarding ***claim 8***, MacGregor discloses a microprocessor system [see Figure 1 on page 108, being the MC68020 microprocessor], comprising

a central processing unit [see Figure 1 on page 108, being a photograph of the MC68020 integrated circuit],

a memory [see page 107, wherein "The enable bit controls the MC68020's use of cache...if it is clear, the cache is disabled and the processor always fetches from external memory."],

a bus connecting said central processing unit to said memory [see page 101, wherein "The MC68020 adds full 32-bit data paths (internal and external)..."], and

means connected to said bus for fetching instructions for said central processing unit on said bus from said memory, said means for fetching instructions being configured and connected

to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit during a single memory cycle [see page 107, wherein "The cache interface to the processor data paths allows complete overlap of instruction fetches with data operand accesses, and thus provides a significant increase in performance. If simultaneous instruction and data operand requests are generated by the micromachine, a hit in the instruction cache allows concurrent fetches to take place."; also see page 111, wherein "Figure 10 illustrates that data and instruction addresses are calculated in parallel and have separate paths to the address pads. This allows a simultaneous instruction and data access if there is a hit in the cache while a data access is taking place."],

said central processing unit including an arithmetic logic unit [see page 101, whereby the MC68020 includes "three 32-bit arithmetic units"] and a first push down stack [see Figures 1 and 2 on page 104; also see page 106, wherein "An additional primitive allows transfer of operands to/from the top of the active system stack."] connected to said arithmetic logic unit [see Figure 2 on page 109],

said first push down stack further including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input, means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input [see Figure 2 on page 104, which shows Interrupt and Master stack pointers, which indicates the presence of separate push down stacks],

said arithmetic logic unit having an output connected to said means for storing a top item [see Figure 2 on page 109],

a second push down stack, said means for storing a top item being connected to provide an input to said second push down stack and a control means connected between said means for storing a top item and said second push down stack for controlling provision of the input to said second push down stack [see Figure 2 on page 104, which shows Interrupt and Master stack pointers, which indicates the presence of separate push down stacks; also see page 104, wherein "...This additional stack (if the M bit is set) is used in the stacking of process-related exceptions."; Additionally see the MC68020 User's Manual, on pages 2-20 through 2-24],

said second push down stack additionally being configured as a register file and said means for storing a top item and said second push down stack additionally configured as the register file being bidirectionally connected [see Figures 1 and 2 on page 104; also seethe MC68020 Reference Manual on page 2-21, wherein "Stack growth from high to low memory is implemented with –(An) to push data on the stack, (An)+ to pull data from the stack. After either a push or a pull operation, register An points to the top item on the stack."].

20. **Claims 1 and 8** are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Number 4,980,821, issued to Koopman *et al.* on December 25, 1990, being filed on March 24, 1987 (hereafter "Koopman'821").

Regarding ***claim 1***, Koopman'821 discloses a microprocessor system [see Figs. 1A and 1B], comprising

a central processing unit integrated circuit [ALU 60, see Fig. 1B],

a memory external of said central processing unit integrated circuit [microprogram memory 78, see Fig. 1B],

a bus connecting said central processing unit integrated circuit to said memory [bidirectional system bus 32, see Fig. 1A], and

means connected to said bus for fetching instructions for said central processing unit integrated circuit on said bus from said memory [host PC bus interface 36],

said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle [see col. 8, lines 11-48, wherein "...a microinstruction pre-fetch is used. This means that the next microinstruction is being read from micromemory at the same time the current instruction is being executed."], said bus having a width at least equal to a number of bits in each of the instructions times a number of the instructions fetched in parallel [see col. 4, lines 20-44],

said central processing unit integrated circuit including an arithmetic logic unit [ALU 60, see Fig. 1B] and a first push down stack connected to said arithmetic logic unit [data high register (DHI) stack 62],

said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input and means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input [see col. 3, lines 52-59; also see col. 6, lines 18-46],

a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack [see col. 5, line 57-col. 6, line 16],

said arithmetic logic unit having an output connected to said means for storing a top item [see Fig. 1B, whereby the output of ALU 60 is connected to the data hi register 62].

Regarding ***claim 8***, Koopman'821 discloses a microprocessor system [see Figs. 1A and 1B], comprising

a central processing unit [see Fig. 1B],

a memory [microprogram memory 78, see Fig. 1B],

a bus connecting said central processing unit to said memory [bidirectional system bus 32, see Fig. 1A], and

means connected to said bus for fetching instructions for said central processing unit on said bus from said memory, said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple

sequential instructions to said central processing unit during a single memory cycle [see col. 8, lines 11-48, wherein "...a microinstruction pre-fetch is used. This means that the next microinstruction is being read from micromemory at the same time the current instruction is being executed."],

said central processing unit including an arithmetic logic unit [ALU 60, see Fig. 1B] and a first push down stack [data high register (DHI) stack 62] connected to said arithmetic logic unit [see Fig. 1B],

said first push down stack further including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input, means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input [see col. 3, lines 52-59; also see col. 6, lines 18-46],

said arithmetic logic unit having an output connected to said means for storing a top item [see Fig. 1B, whereby the output of ALU 60 is connected to the data hi register 62],

a second push down stack [data lo register 68], said means for storing a top item being connected to provide an input to said second push down stack and a control means connected between said means for storing a top item and said second push down stack for controlling provision of the input to said second push down stack [see col. 3, lines 52-59; also see col. 6, lines 18-46],

said second push down stack additionally being configured as a register file and said means for storing a top item and said second push down stack additionally configured as the register file being bidirectionally connected [see Figs. 1A and 1B; also see col. 3, lines 52-59; also see col. 6, lines 18-46].

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. **Claims 10-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over the T414 Data Sheet in view of the May'948 Patent.

Regarding ***claim 10***, the T414 Data Sheet discloses the system discussed above in claim 9, and but does not expressly disclose of a second push down stack, said means for storing a top item being connected to provide an input to said second push down stack and a control means connected between said means for storing a top item and said second push down stack for controlling provision of the input to said second push down stack.

The May'948 Patent discloses a similar Transputer microprocessor [see col. 5, lines 19-21, wherein "The present embodiment provided an improved form of Transputer (Trade Mark of INMOS International plc) microcomputer."], comprising

a central processing unit integrated circuit [CPU 12, see Fig. 1; also see col. 4, lines 42-49],

a memory external of said central processing unit integrated circuit [see col. 4, lines 62-65, wherein "An external memory interface 23 is provided and connected to a plurality of pins 24 for connection to an optional external memory."],

a bus connecting said central processing unit integrated circuit to said memory [see Figs. 1 and 2, bidirectional data bus 31, and bus 16; also see col. 7, lines 15-25], and

means connected to said bus for fetching instructions for said central processing unit integrated circuit on said bus from said memory [memory interface 14, see col. 4, lines 48-56],

said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle [col. 7, lines 26-27, wherein "each instruction consists of 8 bits..."; also see col. 6, lines 10-13, wherein "The processor accesses the memory in words...(in this particular example 16 bits)."; also see col. 7, lines 22-25, wherein "Communications between the CPU and the memory is effected via ...data bus 31."; also see Fig. 2, whereby the bus 31 is split so that instructions are transferred in parallel to another priority register bank;

said bus having a width at least equal to a number of bits in each of the instructions times a number of the instructions fetched in parallel [col. 7, lines 26-27, wherein "each instruction consists of 8 bits..."; also see col. 5, line 64-col. 6, line 13, wherein "...the particular wordlength of the example described is 16 bits but it will be understood that other wordlengths such as 8, 16, 24, 32 or other wordlengths may be used....The processor accesses the memory in words...(in this particular example 16 bits)."; also see col. 7, lines 61-62, where a register supplies data, being at least 16 bits, on data bus 31],

said central processing unit integrated circuit including an arithmetic logic unit and a first push down stack connected to said arithmetic logic unit [ALU 30, see Figs. 1 and 2; also see col. 3, lines 33-38],

said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input and means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input [see col. 8, lines 47-56, wherein "The A, B, and C register stack 54, 55, and 56 are...organised as a stack so that the loading of a value into the A register is preceded by relocating the existing contents of the B register into the C register and from the A register into the B register. Similarly storing a value derived from the A register causes the contents of the B register to be moved into the A register and the contents of the C register into the B register."],

a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack [see col. 8, lines 50-52, wherein "the loading of a value into the A register is preceded by relocating the existing contents of the B register into the C register..."],

said arithmetic logic unit having an output connected to said means for storing a top item [see col. 8, lines 47-49, wherein "The A, B, and C register stack 54, 55, and 56 are the sources and destinations for most arithmetic and logical operations."; also see Fig. 2].

Further, May'948 additionally teaches of a second push down stack, said means for storing a top item being connected to provide an input to said second push down stack and a control means connected between said means for storing a top item and said second push down stack for controlling provision of the input to said second push down stack [being the stack of A, B, and C registers in the priority 0 register bank 39, see Fig. 2].

The T414 Data Sheet and the May'948 Patent are combinable because they are from the same field of endeavor, both being drawn to an Inmos Transputer microprocessor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the

Register bank teachings described in the May'948 Patent within the system described the T414 Data Sheet. The suggestion/motivation for doing so would have been that the system described in the T414 Data Sheet would be easily adapted to incorporate the register bank teachings described in the May'948 Patent, as the components and systems appear to be identical. Therefore, it would have been obvious to combine the teachings of the May'948 Patent with the system of the T414 Data Sheet to obtain the invention as specified in claim 10.

Regarding ***claim 11***, the T414 Data Sheet and the May'948 Patent disclose the system discussed above in claim 10, and the May'948 Patent further teaches that said second push down stack is additionally configured as a register file and said means for storing a top item and said second push down stack additionally configured as the register file are bidirectionally connected [see Fig. 2].

Regarding ***claim 12***, the T414 Data Sheet and the May'948 Patent disclose the system discussed above in claim 11, and the May'948 Patent further teaches of means connected to said means for fetching multiple instructions for determining by decoding the multiple instructions if multiple instructions fetched by said means for fetching multiple instructions require a memory access [see col. 7, lines 26-39, wherein "each instruction consists of 8 bits having the format shown in Fig. 7. 4 bits represent the required function of the instruction and 4 bits are allocated

for data. Each instruction derived from the program sequence for the process is fed into an instruction buffer 34 and the instruction is decoded by the decoder 35."], said means for fetching multiple instructions fetching additional multiple instructions if decoding the multiple instructions shows that the multiple instructions do not require a memory access [see col. 9, lines 7-9 and 31-33].

23. **Claims 9-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over "The Motorola MC68020", written by Doug MacGregor *et al.*, IEEE Micro, August 1984, pages 101-118 (hereafter "MacGregor") in view of the reference "MC68020 32-Bit Microprocessor User's Manual", published by Motorola, having a copyright dated of 1984 (hereafter the "MC68020 User's Manual"), and further in view of U.S. Patent Number 4,985,848, issued to Pfeiffer *et al.* (hereafter "Pfeiffer").

Regarding ***claim 9***, MacGregor discloses a microprocessor system, comprising

a central processing unit [see Figure 1 on page 108, being a photograph of the MC68020 integrated circuit],

an external memory [see page 107, wherein "The enable bit controls the MC68020's use of cache...if it is clear, the cache is disabled and the processor always fetches from external memory."],

a bus connecting said central processing unit to said *external memory* [see page 101, wherein "The MC68020 adds full 32-bit data paths (internal and external)..."; also see Figure 6 on page 110], and

multiplexing means on said bus between said central processing unit and *said external memory* [see page 107, wherein "The key elements used to implement this new concept are the data multiplexer, the SIZE outputs, and the DSACKx inputs."; also see page 109, wherein "the microROM and the nanoROM contents can be multiplexed"; also see Figure 8 on page 112, showing a "multiplexer"],

said multiplexing means being connected and configured to provide multiplexed row addresses, column addresses and data on said bus from said central processing unit to said dynamic random access memory and to provide data from said dynamic random access memory to said central processing unit [see Figure 8 on page 112], and

means connected to said bus for fetching instructions for said central processing unit on said bus from *said external memory*, said means for fetching instructions being configured to fetch multiple sequential instructions from *said external memory* in parallel and supply the multiple instructions to said central processing unit during a single memory cycle [see page 107, wherein "The cache interface to the processor data paths allows complete overlap of instruction fetches with data operand access, and thus provides a significant increase in performance. If simultaneous instruction and data operand requests are generated by the micromachine, a hit in the instruction cache allows concurrent fetches to take place."; also see page 11, wherein "The instruction cache...allows simultaneous instruction and data accesses to occur."; also see page 11, wherein "...there is an appreciable gain from the 32-bit bus for instruction accesses. Although

instructions are of word length and are fetched a word at a time in the MC68000, there is a benefit in fetching two words at a time, because the instruction stream is sequential in nature. The MC68020 stores the second word in a temporary register."],

said central processing unit including an arithmetic logic unit and a first push down stack connected to said arithmetic logic unit [see Figures 1 and 2 on page 104; also see page 106, wherein "An additional primitive allows transfer of operands to/from the top of the active system stack."],

said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input [see Figures 1 and 2 on page 104], and

means for storing a next item connected to a second input of said arithmetic logic unit [see Figure 2 on page 109] to provide the next item to the second input [see Figures 1 and 2 on page 104],

a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack [being inherent in a push down stack system],

said arithmetic logic unit having an output connected to said means for storing a top item [see Figure 2 on page 109].

Further, the MC68020 User's Manual additionally describes the MC68020 microprocessor comprising

a memory external of said central processing unit integrated circuit [see Figure 9-1 on page 8-3],

a bus connecting said central processing unit integrated circuit to said memory [see Figure 8-1 on page 8-3, whereby the external memory is connected to the MC68020 via the buses to carry A0-A31 and D0-D31], and

multiplexing means on said bus between said central processing unit and *said external memory* [see pages 5-3 through 5-5]

means connected to said bus for fetching instructions for said central processing unit integrated circuit on said bus from said memory [see Figure 1-1 on page 1-2; also see Figure 1-5 on page 1-9],

said means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle [see page 1-1, wherein "..the internal operations of this microprocessor are designed to operate in parallel, allowing multiple instructions to be executed concurrently."; also see page 1-8, wherein "Instructions are loaded from the on-chip cache or from external memory during instruction prefetch into stage B."; also see Figure 9-1 on page 9-2],

said central processing unit integrated circuit including an arithmetic logic unit [see Figure 1-1 on page 1-2],

said first push down stack including means for storing a top item [see Figures 1-2 and 1-3 on page 1-3; also see the illustrations on pages 2-21 through 2-24] connected to a first input of said arithmetic logic unit [see Figure 1-1 on page 1-2; also see page 1-2, wherein "Registers A0-A6 and the user, interrupt, and master stack pointers are address registers that may be used as software stack pointers or base address registers."] to provide the top item to the first input and means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input [see the illustrations on pages 2-21 through 2-24; also see page 2-20, wherein "Each system stack fills from high to low memory."],

a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack [see page 2-21, wherein "Stack growth from high to low memory is implemented with –(An) to push data on the stack, (An)+ to pull data from the stack. After either a push or a pull operation, register An points to the top item on the stack."],

said arithmetic logic unit having an output connected to said means for storing a top item [see Figure 1-1 on page 1-2].

However, MacGregor and the MC68020 User's Manual fail to expressly disclose if the *external memory* is dynamic RAM.

Pfeiffer discloses a system that includes the Motorola 68020 having a dynamic RAM [see col. 7, lines 11-46, wherein "The interface 52 may be of the type manufactured by Motorola, and identified as integrated circuit type MC68020....A dynamic random access memory unit 60 and a

programmable read-only memory 62 are under the control of the memory manager 56 for storing information either temporarily, or permanently."; also see Fig. 3].

MacGregor, the MC68020, & Pfeiffer are combinable because they are from the same field of endeavor, each describing features and embodiments of the Motorola MC68020 microprocessor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to utilize the MC68020 processor discussed in MacGregor in the application described by Pfeiffer that utilized a DRAM. The suggestion/motivation for doing so would have been that the MacGregor system would easily be modified to incorporate the teachings of a DRAM, as described in Pfeiffer, as the DRAM is utilized for virtual storage of data, thereby allowing the high use segments to remain in the high speed memory, as recognized by Pfeiffer in col. 7, lines 35-42. Further, in the MC68020 Reference Manual on page 1-7, the MC68020 supports "virtual memory is to provide a limited amount of high-speed physical memory that can be accessed directly by the processor while maintaining an image of a much larger 'virtual' memory on secondary storage devices ..." Therefore, it would have been obvious to combine the teachings of Pfeiffer with the MC68020 teachings of MacGregor and the MC68020 User's Manual to obtain the invention as specified in claim 9.

Regarding ***claim 10***, MacGregor, the MC68020 Reference Manual, and Pfeiffer disclose the system discussed above in claim 9, and MacGregor further teaches of a second push down stack, said means for storing a top item being connected to provide an input to said second push down stack and a control means connected between said means for storing a top item and said

second push down stack for controlling provision of the input to said second push down stack [see Figure 2 on page 104, which shows Interrupt and Master stack pointers, which indicates the presence of separate push down stacks; also see page 104, wherein "...This additional stack (if the M bit is set) is used in the stacking of process-related exceptions."; Additionally see the MC68020 User's Manual, on pages 2-20 through 2-24].

Regarding ***claim 11***, MacGregor, the MC68020 Reference Manual, and Pfeiffer disclose the system discussed above in claim 10, and the MacGregor further teaches that said second push down stack is additionally configured as a register file and said means for storing a top item and said second push down stack additionally configured as the register file are bidirectionally connected [see Figures 1 and 2 on page 104; also seethe MC68020 Reference Manual on page 2-21, wherein "Stack growth from high to low memory is implemented with –(An) to push data on the stack, (An)+ to pull data from the stack. After either a push or a pull operation, register An points to the top item on the stack."].

Regarding ***claim 12***, MacGregor, the MC68020 Reference Manual, and Pfeiffer disclose the system discussed above in claim 11, and the MacGregor further teaches of means connected to said means for fetching multiple instructions for determining by decoding the multiple instructions if multiple instructions fetched by said means for fetching multiple instructions require a memory access, said means for fetching multiple instructions fetching additional multiple instructions if decoding the multiple instructions shows that the multiple instructions do not require a memory access [see page 114, wherein "If succeeding instructions have no need to

use the external bus – as is the case for register-to-register operation, branching, and other instructions which hit in the instruction cache and have no external data transfers – then these instructions may have their execution times totally absorbed by the previous write cycle."].

Regarding ***claim 13***, MacGregor, the MC68020 Reference Manual, and Pfeiffer disclose the system discussed above in claim 12, and MacGregor further teaches of an instruction register for the multiple instructions connected to said means for fetching instructions [see page 112, wherein "The depth of the instruction pipe on the MC68020 is three words."; also see Fig. 12 on page 114],

means connected to said instruction register for supplying the multiple instructions in succession from said instruction register, a counter connected to control said means for supplying the multiple instructions to supply the multiple instructions in succession [see Figure 1 on page 104, having a "program counter"; also see page 102, wherein "The MC68000 family supports 14 addressing modes including ...program-counter-relative"],

means for decoding the multiple instructions connected to receive the multiple instructions in succession from the means for supplying the multiple instructions, said counter being connected to said means for decoding to receive incrementing and reset control signals from said means for decoding [see page 109, wherein "The decode PLAs (A1 and A5/A6) have microcode sequences which decode all possible instruction words and accumulate the resulting outputs into a signature register that can then be read out and checked.", also wherein "The instruction pipe and other miscellaneous control sections provide the secondary decode of

instructions and generate the actual control signals that result in the decoding and interpretation of the control store."; also see Figure 2 on page 109],

said means for decoding being configured to supply the reset control signal to said counter and to supply a control signal to said means for fetching instructions in response to a SKIP instruction in the multiple instructions [see page 104, also see the MC68020 User's Manual, page 8-10, wherein "This allows the main processor to ...skip them to locate the next instruction."; also for instance, see the MC68020 User's Manual, page B-101, showing the "MOVE" instruction, which sets condition codes to be cleared].

Regarding ***claim 14***, MacGregor, the MC68020 Reference Manual, and Pfeiffer disclose the system discussed above in claim 13, and MacGregor further teaches of a loop counter connected to receive a decrement control signal from said means for decoding, said means for decoding being configured to supply the reset control signal to said counter and the decrement control signal to said loop counter in response to a MICROLOOP instruction in the multiple instructions within the multiple instructions in said instruction register for a number of repetitions controlled by said loop counter [see the MC68020 User's Manual, page B-77, wherein "This instruction is a looping primitive of three parameters: a condition, a counter (data register), and a displacement. The instruction first tests the condition to determine if the termination condition for the loop has been met, and if so, no operation is performed. If the termination condition is not true, the low order 16 bits of the counter data register are decemented by one. If the result is -1, the counter is exhausted and execution continues with the

next instruction. If the result is not equal to -1, execution continues at the location indicated by the current value of the PC [program counter plus the sign-extended 16-bit displacement."].

Regarding ***claim 15***, MacGregor, the MC68020 Reference Manual, and Pfeiffer disclose the system discussed above in claim 13, and MacGregor further teaches that said means for decoding is configured to control said counter in response to one of the multiple instructions utilizing a variable width operand stored in said instruction register with the multiple instructions [see page 102, wherein "Variable-byte-length operands are provided to support the coprocessor interface-coprocessors can define operand lengths suitable for the application."; also see page 105, wherein "the main processor can perform an effective address calculation and then either pass the evaluated effective address to the coprocessor or fetch a variable-length operand and pass that to the coprocessor."], said microprocessor system additionally comprising means connected to said counter to select the variable width operand for use with the instruction utilizing the variable width operand in response to a state of said counter resulting from control of said counter by said means for decoding [see Figure 2 on page 109; also see page 112, wherein "The execution unit is divided into three 32-bit sections, each with a 32-bit adder: the instruction address section, in which the instruction addresses are calculated and then pointers are stored; the operand address section, in which the operand addresses are calculated..."].

Regarding ***claim 16***, MacGregor, the MC68020 Reference Manual, and Pfeiffer disclose the system discussed above in claim 12, and MacGregor further teaches that the decoding determines if the multiple instructions do not require a memory access by a state of a bit of each

of the multiple instructions [see the MC68020 User's Manual, page 7-1, wherein "Address bit A1 is used to select the proper word from the cache entry and the cycle ends. If there is no match, or the valid bit is clear, a cache miss occurs and the instruction is fetched from external memory. This new instruction is automatically written into the cache entry..."].

Regarding ***claim 17***, MacGregor, the MC68020 Reference Manual, and Pfeiffer disclose the system discussed above in claim 16, and MacGregor further teaches that the bit is a most significant bit of the multiple instructions [see the MC68020 User's Manual, page 7-1, wherein "Address bit A1 is used to select the proper word from the cache entry and the cycle ends. If there is no match, or the valid bit is clear, a cache miss occurs and the instruction is fetched from external memory. This new instruction is automatically written into the cache entry..."].

STATEMENT OF REASONS FOR PATENTABILITY AND/OR CONFIRMATION

The following is an examiner's statement of reasons for patentability and/or confirmation of the claims found patentable in this reexamination proceeding:

Claims 21-27 are deemed as patentable.

Regarding ***claim 21***, in the examiner's opinion, it would not have been obvious to one of ordinary skill in the art at the time the invention was made to have the system defined in claim 9, further include the features that require said microprocessor system is configured to provide different memory access timing for different storing capacity sizes of said dynamic random access memory by including a sensing circuit and a driver circuit, and an output enable line connected between said dynamic random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level after a memory read operation as a function of different capacitance on said bus as a result of the different storing capacity sizes of said dynamic random access memory, said microprocessor system being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal.

Regarding ***claim 23***, in the examiner's opinion, it would not have been obvious to one of ordinary skill in the art have the system discussed in claim 9 further be configured to operate at variable clock speed, with said microprocessor system additionally comprising a ring counter variable speed system clock connected to said central processing unit, said central processing unit and said ring counter variable speed system clock being provided in a single integrated

circuit, said ring counter variable speed system clock being configured to provide different clock speed to said central processing unit as a result of transistor propagation delays, depending on at least one of temperature of said single integrated circuit, voltage and microprocessor fabrication process for said single integrated circuit.

Regarding ***claim 26***, in the examiner's opinion, it would not have been obvious to one of ordinary skill in the art at the time of the invention to have the system discussed above in claim 9, further include the features that require said first push down stack has a first plurality of stack registers having stack memory elements configured as latches, a second plurality of stack registers having stack memory elements configured as a random access memory, said first and second plurality of stack registers and said central processing unit being provided in a single integrated circuit with a top one of said second plurality of stack registers being connected to said a bottom one of said first plurality of stack registers, and a third plurality of stack registers having stack memory elements configured as a random access memory external to said single integrated circuit, with a top one of said third plurality of stack registers being connected to a bottom one of said second plurality of stack registers, said microprocessor system being configured to operate said first, second and third plurality of stack registers hierarchically as interconnected stacks.

Any comments considered necessary by PATENT OWNER regarding the above statement must be submitted promptly to avoid processing delays. Such submission by the

patent owner should be labeled: "Comments on Statement of Reasons for Patentability and/or Confirmation" and will be placed in the reexamination file.

Conclusion

24. Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that *ex parte* reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extensions of time in *ex parte* reexamination proceedings are provided for in 37 CFR 1.550(c).

25. In order to ensure full consideration of any amendments, affidavits or declarations, or other documents as evidence of patentability, such documents must be submitted in response to this Office action. Submissions after the next Office action, which is intended to be a final action, will be governed by the requirements of 37 CFR 1.116, after final rejection and 37 CFR 41.33 after appeal, which will be strictly enforced.

26. The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent No. 5,440,749 throughout the course of this reexamination proceeding.

27. ALL correspondence relating to this ex parte reexamination proceeding should be directed as follows:

Please mail any communications to:

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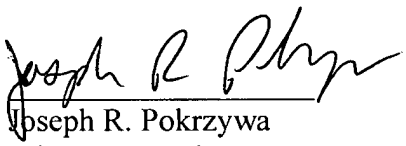

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ESK

Notice of References Cited	Application/Control No. 90/009,034, 90/009,389 & 90/010,520	Applicant(s)/Patent Under Reexamination 5440749	
	Examiner JOSEPH R. POKRZYWA	Art Unit 3992	Page 1 of 1

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*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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PTO/SB/08A&B (02-09)

Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				**Application Number**	90/009,034
				Filing Date	March 31, 2008
				First Named Inventor	---
				Art Unit	3992
(Use as many sheets as necessary)				Examiner Name	Joseph R. Pokrzywa
Sheet	1	of	54	Attorney Docket Number	0081-011X1

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	EP	~~90/009,380 Reexam Ordered 01-08-2008~~	
	EQ	~~90/009,380 Request for Reexamination dated 01-16-2008~~	
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	FB	~~90-008,225 and 90-008,299 Notice of Intent to Issue a Reexam Certificate dated 04-21-09~~	
	FC	~~90-008,225 Notice of Failure to Comply with Ex Parte Reexamination Request Filing Requirements dated~~ 10-16-2006	
	FD	~~90-008,225 Response to Notice of Failure to Comply with Ex Parte Reexamination Request Filing~~ Requirements: Letter Accompany Replacement PTO Form, SB/42, dated 11-15-06	
	FE	~~90-008,227 Examiner Interview Summary Record dated 02-12-08~~	
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				First Named Inventor	---
				Art Unit	3992
(Use as many sheets as necessary)				Examiner Name	Joseph R. Pokrzywa
Sheet	9	of	54	Attorney Docket Number	0081-011X1

NON PATENT LITERATURE DOCUMENTS			
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	FV	~~90-008,237 Notice of Failure to Comply with Ex Parte Reexamination Request Filing Requirements dated~~ 10-19-2006	
	FW	~~90-008,237 Response to Notice of Failure to Comply with Ex Parte Reexamination Request Filing~~ Requirements: Letter Accompanying Replacement PTO Form SB/42 dated 11-17-2006	
	FX	~~90-008,237 Response to Notice of Failure to Comply with Ex Parte Reexamination Request Filing~~ Requirements dated 10-19-2006	
	FY	~~90-008,237 Response to Non-Final Office Action dated 09-02-08~~	
	FZ	~~90-008,297, 90-008,308, 90-008,474 Examiner Interview Summary Record dated 04-29-09~~	
	GA	~~90-008,297, 90-008,308, 90-008,474 Final Office Action dated 03-17-09~~	
	GB	~~90-008,299 Order Granting Reexam dated 12-22-2006~~	
	GC	~~90-008,299 Request for Reexamination dated 10-10-2006~~	
	GD	~~90-008,308 Non-Final Office Action dated 07-02-08~~	
	GE	~~90-008,886 Reexam Ordered 01-16-2007~~	

Examiner Signature	/Joseph Pokrzywa/	Date Considered	11/10/2009

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	~~CF~~	~~90 009,396 Request for Reexamination dated 10-10-06~~	
	~~CG~~	~~90 009,474 Reexam Ordered 01-05-07~~	
	~~CH~~	~~90 009,474 Request for Reexamination dated 01-30-07~~	
	~~CI~~	~~90 009,888 Reexam Ordered 01-09-09~~	
	~~CJ~~	~~90 009,388 Request for Reexam dated 01-16-09~~	
	~~XK~~	~~90 009,457 Request for Reexamination dated 01-21-2009~~	
/J.P./	GK	Acorn Computers, Ltd., Acorn RISC Machine CPU Software Manual, Issue 1.00 October 1985	
/J.P./	GL	Acorn's RISC Leapfrog, Acorn User special issue, June 1987; 59: 149-153	
/J.P./	GM	AGRAWAL et al., "Design Considerations for a Bipolar Implementation of SPARC," Compcon Spring apos;88. Thirty-Third IEEE Computer Society International Conference, Digest of Papers, 29 Feb-3 Mar 1988, pp. 6 - 9	
/J.P./	GN	AGRAWAL, "An 80 MHz Bipolar ECL Implementation of SPARC," Sun Microsystems, Inc., June 25, 1989, 40 pages total.	

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/J.P./	GO	Alliacense Product Report - Preliminary Review, USP 5,440,749; GPS Car Navigation Main Processor	
/J.P./	GP	Alliacense Product Report - Preliminary Review, USP 5,440,749; GPS Navigation System GPS Chipset	
/J.P./	GQ	Alliacense Product Report - Preliminary Review, USP 5,440,749; GPS Navigation System Main Microprocessor	
/J.P./	GR	Alliacense Product Report - Preliminary Review, USP 5,440,749; Kyocera Digital Camera Finecam S3R Image Processor	
/J.P./	GS	Alliacense Product Report - Preliminary Review, USP 5,440,749; PDA/Mobile Navigation, GPS Processor	
/J.P./	GT	Alliacense US Patent 5,784,584 Product Report, NEC Microcomputer, V850E2 32 Bit Microcontroller, pp.1-8 (2006)	
/J.P./	GU	Alliacense US Patent 5,784,584 Product Report, TLCS-900/H1 Series TMP92C820, Toshiba Microcontroller TMP92C820 / TLCS-900/H1 Series 16-bit Microcontroller, pages 1-9 (2006)	
/J.P./	GV	Alliacense US Patent 5,809,336 Product Report, Toshiba Microcontroller TMP93CS44/S45 /TLCS - 900/L Series 16-bit Microcontroller (2006)	
/J.P./	GW	Alliacense US Patent 5,809,336 Product Report, NEC Microcontroller UDP789478, 8 Bit Microcontroller, 38 pages (2006)	
/J.P./	GX	Alliacense US Patent 5,809,336 Product Report, Toshiba Microcontroller TMP92CZ26 / TMP92CW26, 32 bit Microcontroller (2006)	

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/J.P./	GY	Alliacense US Patent 5,809,336 Product Report, Toshiba MPEG-4 Audiovisual LSI TC35273 MPEG-4 Audiovisual Code LSI (2006)	
/J.P./	GZ	ANDERSON, D.W., "The IBM System/360 Model 91: Machine Philosophy and Instruction Handling, IBM Journal, IBM, January 1967, pp. 8 -24.	
/J.P./	HA	ARM Datasheet, Part No. 1 85250 0360 0, Issue No. 1 (March 17, 1987)	
/J.P./	HB	ATMEL SPARC Instruction Set, "Assembly Language Syntax," Rev. 4168C-AERO-08/01, 2002	
/J.P./	HC	BAGULA, "A 5V Self-Adaptive Microcomputer with 16Kb of #2 Program Storage and Security," IEEE International Solid-State Circuit Conference, 1983, pp. 34-5	
/J.P./	HD	BAYKO, "Great Microprocessors of the Past and Present (V 11.7.0), downloaded from: <<http://web.archive.org/web/20010107210400/http://bwrc.eecs.berkeley.edu/CIC/Archive/cup_history.html>>, Feb 2007, 60 pages total.	
/J.P./	HE	BIT SPARC Integer Unit B5000 Datasheet attached to a presentation by Anant Agrawal in 1989, 28 pages	
/J.P./	HF	Books Review: Operating Systems A Systematic View, William S. Davis, Addison-Wesley Publishing Company, Inc., 1987; 26(4):453-454.	
/J.P./	HG	BOSSHART et al., "A 533K-Transistor LISP Processor Chip," IEEE Journal of Solid State Circuits, SC-22(5): 808-819 (October 1987).	
/J.P./	HH	BOURKE, "Character Synchronization During Overrun Conditions," Delphion, IBM Technical Disclosure Bulletin, Dec 1977	

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/J.P./	HI	Burroughs Corporation, "Burroughs B5500 Information Processing System Reference Manual," 1973.	
/J.P./	HJ	CAL RUN FORTRAN Guide, University of California, Computer Center, Berkeley, 292 pages total. (Sep 1974)	
	HK	~~Case no. 09-cv-4083, Sirius XM Radio Inc. vs. Technology Properties, Patriot, and Alliacense Ltd.,~~ Declaratory Judgment filed 04-24-09	
	HL	~~Case no. 2:05-cv-00494 (TJW) Supplemental Declaration of Alvin M. Deepain in Support of Plaintiffs'~~ Reply Claim Construction Brief filed 4/9/07	
	HM	~~Case no. 2:05-cv-00494 (TJW) Daniels deposition of 8/18/07, Exhibit 12. Photo of 68332 with other~~ support chips.	
	HN	~~Case no. 2:05-cv-00494 (TJW) Declaration of Roger L. Cook in Support of Plaintiffs Technology Property~~ Limited's and Patriot Scientific Corporations' Claim Construction Brief filed 3/19/07	
	HO	~~Case no. 2:05-cv-00494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-8 Asam~~ Processor Invalidity Chart	
	HP	~~Case no. 2:05-cv-00494 (TJW) Defendant NEC Electronics America, Inc.'s Preliminary Invalidity~~ Contentions Under Patent Rule 3-3, filed 09/18/06	
	HQ	~~Case no. 2:05-cv-00494 (TJW) Defendants' Brief Regarding Construction of Disputed Claim Terms of the~~ 336 and 148 Patents filed 4/2/07	
	HR	~~Case No. 2:05-cv-00494 (TJW) Defendants' Brief Regarding Construction of Disputed Claim Terms of~~ the 584 Patent filed 4/2/07	

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	HS	~~Case no. 2:05-cv-00494 (TJW) Defendants' Sur-Reply Brief Regarding Construction of Disputed Claim~~ Terms of the 336 Patent filed 4/29/07	
	HT	~~Case no. 2:05-cv-00494 (TJW) Plaintiffs' Claim Construction Reply Brief filed 4/9/07~~	
	HU	~~Case no. 2:05-cv-00494 (TJW) Plaintiffs Technology Property Limited's and Patriot Scientific~~ Corporation's Claim Construction Brief filed 3/19/07	
	HV	~~Case no. 2:05-cv-00494 (TJW) TPL Declaration of Alvin M. Despain in Support of Plaintiffs' Claim~~ Construction Brief filed 3/19/07	
	HW	~~Case no. 2:05-cv-00494 (TJW) TPL Defendants' Unopposed Motion for Leave to File a Sur-Reply Brief~~ Regarding Claim Construction filed 4/19/07	
	HX	~~Case no. 2:05-cv-00494 (TJW) TPL Supplemental Declaration of Roger L. Cook in Support of Plaintiffs'~~ Technology Property Limited's and Patriot Scientific Corporations' Claim Construction Brief filed 4/9/07	
	HY	~~Case no. 2:05-cv-494 (TJW) Daniels Deposition - transcript of 8/10/07~~	
	HZ	~~Case no. 2:05-cv-494 (TJW) Daniels deposition of 8/10/07, Exhibit 5: 10/20/88 Letter to Daniels from~~ Fisher.	
	IA	~~Case no. 2:05-cv-494 (TJW) Daniels deposition of 8/10/07, Exhibit 6: List of Motorola Microcontroller~~ business major goals for 1989.	
	IB	~~Case no. 2:05-cv-494 (TJW) Daniels deposition of 8/10/07, Exhibit 7: Motorola Microcontroller Division,~~ "Customer Management Briefing Summary" Sales Brochure (1988)	

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	IC	~~Case no. 2:05-cv-494 (TJW) Daniels deposition of 8/10/07, Exhibit 8: Motorola's MC68882~~ Microcontroller	
	ID	~~Case no. 2:05-cv-494 (TJW) Daniels deposition of 8/10/07, Exhibit 9: Die photo~~	
	IE	~~Case no. 2:05-cv-494 (TJW) Daniels deposition of 8/10/07, Exhibit 10: DANIELS, "A Participant's~~ Perspective," IEEE Micro, 16(6):21-31 (1996).	
	IF	~~Case no. 2:05-cv-494 (TJW) Daniels deposition of 8/10/07, Exhibit 11: SCHELL, "A legacy of~~ leadership," Mos Talk, 22(9): 4 pages (1997). Article re Gary Daniels, Senior Vice President of MCTG)	
	IG	~~Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-1 ODC 6800~~ Invalidity Chart	
	IH	~~Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-2 MIPS~~ Invalidity Chart	
	II	~~Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-3 SPARC~~ Invalidity Chart	
	IJ	~~Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-4 IBM RT PC~~ ROMP Invalidity Chart	
	IK	~~Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-5 Berkeley~~ RISC I and RISC II Invalidity Chart	
	IL	~~Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-6 Porter~~ Invalidity Chart - USP 3,976,977	

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	IM	~~Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit A-7 CRAY-1~~ Invalidity Chart	
	IN	~~Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions Exhibit B: RIOS~~ References	
	IO	~~Case no. 2:05-cv-494 (TJW) Defendant ARM Preliminary Invalidity Contentions, filed 10/12/06~~	
	IP	~~Case no. 2:05-cv-494 (TJW) Defendant NEC Preliminary Invalidity Contentions filed 9/18/06~~	
	IQ	~~Case no. 2:05-cv-494 (TJW) Defendant Toshiba Preliminary Invalidity Contentions filed 9/18/06~~	
	IR	~~Case no. 2:05-cv-494 (TJW) Defendants MEI, PNA, and JVC Preliminary Invalidity Contentions filed~~ 9/18/06	
	IS	~~Case no. 2:05-cv-494 (TJW) Defendants MEI, PNA, and JVC Preliminary Invalidity Contentions filed~~ 9/18/06 EXHIBIT A - Claim Chart for '148 Patent	
	IT	~~Case no. 2:05-cv-494 (TJW) Defendants MEI, PNA, and JVC Preliminary Invalidity Contentions filed~~ 9/18/06 EXHIBIT B - Claim Chart for '336 Patent	
	IU	~~Case no. 2:05-cv-494 (TJW) Defendants MEI, PNA, and JVC Preliminary Invalidity Contentions filed~~ 9/18/06 EXHIBIT C - Claim Chart for '584 Patent	
	IV	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07, Exhibit 4: Memo of 9/12/92 Fish to Higgins~~ re: ShBoom Patents.	

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	IW	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07, Exhibit 8: Letter of 6/14/92 Higgins to Falk~~ re: patent application for HIGH PERFORMANCE LOW COST MICROPROCESSOR.	
	IX	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07, Exhibit 8: Letter of 6/30/92 Higgins to Falk~~ re: patent application for HIGH PERFORMANCE LOW COST MICROPROCESSOR.	
	IY	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07, Exhibit 10: Letter of 5/12/92, Fish to Higgens~~ re Patent Defense	
	IZ	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07, Exhibit 12: Agreement executed 1/3/89~~ between PTA Inc. and Chuck Moore, dba Computer Cowboys.	
	JA	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07, Exhibit 13: Oki Japan MSH Boom 06000~~ Schematic (7/13/89).	
	JB	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07, Exhibit 14: Assignment of 07/390,334 from~~ Fish to Fish Family Trust.	
	JC	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07, Exhibit 15: Stock Purchase and Technology~~ Transfer Agreement between Fish Family Trust, Helmut Falk, and Nanotronics Corporation (8/16/91).	
	JD	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07, Exhibit 16: fax of 7/16/04 Marshall to~~ Suanders and Heptig w/ attached 7/15/04 memo from Beatie re: Fish and Moore.	
	JE	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07, Exhibit 17: Fax of 7/29/04, Heptig to Marshall~~ with attached executed agreement.	
	JF	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07, Exhibit 18: Plaintiffs' Second Amended~~ Complaint filed 9/22/06 in 3:06-cv-00815.	

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	JG	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 19: Settlement Agreement between~~ Patriot Scientific Corporation, Fish, and the trustee of Fish Family Trust.	
	JH	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 21: Comparisons of RISC Chips~~ (12/11/88).	
	JI	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 22: VL86C010 An Affordable 32-bit~~ RISC Microprocessor System, VLSI Technology, Inc. (various articles)	
	JJ	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 29: "SH-BOOM Patent~~ Documentation," (6/21/89).	
	JK	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 30: "SH-BOOM Licensing Strategy,"~~ (1/19/90).	
	JL	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 31: "Transputer Includes~~ Multiprocessing protocol," 1/2/91.	
	JM	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 32: Article titled "INMOS details next~~ Transputer," (4/18/91).	
	JN	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 33: Articles from Electronic World~~ News.	
	JO	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 36: Comparison of Intel 80960 and~~ SH-BOOM Microprocessors (1989).	
	JP	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 37: Memo of 7/13/89, Fish to Chu w/~~ attached comparison of MIPS 2000 to SH-BOOM.	

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(Use as many sheets as necessary)				Examiner Name	Joseph R. Pokrzywa
Sheet	19	of	54	Attorney Docket Number	0081-011X1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	JQ	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 39: fax of 6/10/92 Fish to Higgins w/~~ attached document titled "State of the Prior Art SHBOOM Microprocessor".	
	JR	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 39: 4/12/89 Time and Responsibility~~ Schedule.	
	JS	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 40: handwritten note.~~	
	JT	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 41: memo of 6/89 to PT Acquisitions,~~ Inc. re: fees due for searches conducted.	
	JU	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 42: memo of 6/28/92 Fish to Higgins~~ re: Dialog Patents re: SHBOOM.	
	JV	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 43: Letter of 8/6/98 Haarr to Turner~~ transmitting documents.	
	JW	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 44: Declaration of Moore re: US~~ patent application 08/484,918.	
	JX	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 45: fax of 11/9/89, Leakrane to Fish~~ with attached draft license agreement between PT Acquisitions and Oki Electric Industries.	
	JY	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 46: Letter of 11/20/89 Fish to Slater~~ re: Japanese "borrowing" Sh-BOOM 50 MHZ RISC CHIP.	
	JZ	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 47: Letter of 12/20/89 Leakrane to~~ Fish re: SHBOOM project.	

Examiner Signature	/Joseph Pokrzywa/	Date Considered	11/10/2009

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PTO/SB/08A&B (02-09)

Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				**Application Number**	90/009,034
				Filing Date	March 31, 2008
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				Art Unit	3992
(Use as many sheets as necessary)				Examiner Name	Joseph R. Pokrzywa
Sheet	20	of	54	Attorney Docket Number	0081-011X1

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	KA	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 48: Letter of 7/16/90 Fish to Leckron~~ re: attorney client relationship and conflict of interest.	
	KB	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 49: Letter of 7/24/90 Leckrone to Fish~~ re: letter of 7/16/90 (EX 48).	
	KC	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 50: Letter of 8/27/90 Moore to Fish re:~~ SHBOOM confidentiality.	
	KD	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 51: PT Acquisitions / Alliance~~ Semiconductor Corp. Manufacturing Agreement (7/20/90).	
	KE	~~Case no. 2:05-cv-494 (TJW) Fish deposition of 6/25-26/07; Exhibit 52: Letter of 2/6/90 to PT Acquisitions~~ from Dun & Bradstreet Receivable Recovery Systems re: final notice for payment of account.	
	KF	~~Case no. 2:05-cv-494 (TJW) Fish Deposition Transcripts volumes 1 (6/25/07) and 2 (6/26/07)~~	
	KG	~~Case no. 2:05-cv-494 (TJW) McDermott deposition of 8/9/07; Exhibit 01: Subpoena of 8/1/07 for Mark~~ McDermott in 2:05-cv-494 (TJW)	
	KH	~~Case no. 2:05-cv-494 (TJW) McDermott deposition of 8/9/07; Exhibit 12: Notes from class taken at~~ University of Texas (September 1987)	
	KI	~~Case no. 2:05-cv-494 (TJW) McDermott deposition of 8/9/07; Exhibit 2: "Motorola's MC68332~~ Microcontroller" layout design	
	KJ	~~Case no. 2:05-cv-494 (TJW) McDermott deposition of 8/9/07; Exhibit 3: Photos of wafers pre-chip I and~~ II and final wafer and die photo of chip	

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	KK	~~Case no. 2:05-cv-494 (TJW) McDermott deposition of 8/9/07, Exhibit 4: Photo of Motorola's CMP X-82~~ bit Microcontroller	
	KL	~~Case no. 2:05-cv-494 (TJW) McDermott deposition of 8/9/07, Exhibit 5: Photo of individual die from pre-~~ chip I, II and the final chip	
	KM	~~Case no. 2:05-cv-494 (TJW) McDermott deposition of 8/9/07, Exhibit 7: Patent Application transmittal~~ letter received by USPTO 8/26/88 for application 237022	
	KN	~~Case no. 2:05-cv-494 (TJW) McDermott deposition of 8/9/07, Exhibit 8: Schematic used to lay out chip~~	
	KO	~~Case no. 2:05-cv-494 (TJW) McDermott deposition of 8/9/07, Exhibit 10: HARWOOD et al., "Testability~~ Features Of the MC68332 Modular Microcontroller," 1989 International Test Conference, paper 28.2, pages 615-623 (1989)	
	KP	~~Case no. 2:05-cv-494 (TJW) McDermott deposition of 8/9/07, Exhibit 23: VY86Gxxx ARM 32-BIT CMOS~~ product literature, EDN (11/21/91).	
	KQ	~~Case No. 2:05-cv-494 (TJW) McDermott Deposition transcript, 8/9/07~~	
	KR	~~Case no. 2:05-cv-494 (TJW) MEI claim charts on MOSTEK 3873 chip, filed 8/8/07~~	
	KS	~~Case no. 2:05-cv-494 (TJW) MEI Invalidity Contentions on '148 and '336 patents filed 8/22/07~~	
	KT	~~Case no. 2:05-cv-494 (TJW) Memorandum Opinion and Order (Markman) filed 6/15/07~~	

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	KU	~~Case no. 2:05-cv-494 (TJW) NEC Defendants' Preliminary Invalidity Contentions filed 9/25/06~~	
	KV	~~Case No. 2:05-cv-494 (TJW); Daniels deposition of 8/10/07; Exhibit 1: Subpoena of 8/1/07 for Cary~~ Daniels	
	KW	~~Case No. 2:05-cv-494 (TJW); Daniels deposition of 8/10/07; Exhibit 2: Motorola Microprocessor~~ Products Group, Milestones for Management Review	
	KX	~~Case No. 2:05-cv-494 (TJW); Daniels deposition of 8/10/07; Exhibit 4: Motorola, "Embedded Control~~ Solutions, Powered by Motorola" product brochure (1988)	
	KY	~~Case no. 5:08-cv-00877 JF, Acer and Gateway vs. TPL, Patriot, and Alliacense, Complaint for~~ Declaratory Judgment filed 2/8/08	
	KZ	~~Case no. 5:08-cv-00877 JF Acer and Gateway vs. TPL, Patriot, and Alliacense, Preliminary Invalidity~~ Contentions (Patent L.R. 3-3)	
	LA	~~Case No. 5:08-cv-00877 JF Acer Declaration of Harold H. Davis in Support of Plaintiff's Motion to Stay~~ All Proceedings Pending Reexamination of the Patents-in-Suit, dated 05-01-09	
	LB	~~Case No. 5:08-cv-00877 JF Acer Inc. and Acer America Corporation Plaintiff's Motion and Motion to Stay~~ All Proceedings Pending Reexamination of the Patents-in-Suit, dated 05-01-09	
	LC	~~Case No. 5:08-cv-00877 JF Acer Inc. and Acer America Corporation's and Gateway First Amended~~ Complaint for Declaratory Judgment dated 02-09-09	
	LD	~~Case No. 5:08-cv-00877 JF Acer Inc. and Acer America Corporation's Responses to Defendant~~ Technology Properties Limited's First Set of Interrogatories, dated 04-03-09	

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	LE	~~Case No. 5:08-cv-00877-JF Gateway, Inc.'s Responses to Defendants Technology Properties Limited's~~ First Set of Interrogatories dated 04-03-09	
	LF	~~Case no. 5:08-cv-00882-JF, HTC vs. TPL, Patriot, and Alliacense, Complaint for Declaratory Judgment~~ filed 2/8/08	
	LG	~~Case no. 5:08-cv-00882-JF, HTC vs. TPL, Patriot, and Alliacense, First Amended Complaint for~~ Declaratory Judgment filed 07-10-08	
	LH	~~Case no. 5:08-cv-00884-JF Acustek and Asus vs. TPL, Patriot, MGM, and Alliacense, First Amended~~ Complaint filed 02-13-08	
	LI	~~Case no. 5:08-cv-00884-JF Acustek and Asus vs. TPL, Patriot, MGM, and Alliacense, Second Amended~~ Complaint filed 09-25-08	
	LJ	~~Case no. 5:08-cv-00884-JF, Acustek vs. TPL, Patriot, and Alliacense, Complaint for Declaratory~~ Judgment filed 2/8/08	
	LK	~~Case no. C08005398 JF, Barco's Patent Local Rule 3-3 Invalidity Contentions dated 04-08-2009~~	
	LL	~~Case no. C08005398, BARCO N.V. v. Technology Properties Ltd., Patriot Scientific Corp., and Alliacense~~ Ltd., Complaint for Declaratory Judgment, Demand for Jury Trial, dated 12-01-08	
/J.P./	LM	CDC 6000 Computer Systems - COBOL INSTANT 6000, Version 3; Control Data Publication No. 60327600A (Apr 1971)	
/J.P./	LN	CDC 6000 Computer Systems, 7600 Computer Systems: FORTRAN Extended Instant 6000 Version 3, 7600 Version 1; Control Publication No. 60305900A (May 1971)	

Examiner Signature	/Joseph Pokrzywa/	Date Considered	11/10/2009

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/J.P./	LO	CDC 6000 Computer Systems/ 7600 Computer Systems: FORTRAN Extended Reference Manual, 6000 Version 3, 7600 Version 1; Control Data Publication No. 60329100, Revision D (1972)	
/J.P./	LP	CDC 6000 Series Computer System, 6642 Distributive Data Path Operation and Programming Reference Manual; Control Data Publication No. 60376300C (Mar 1979)	
/J.P./	LQ	CDC 6000 Series Computer Systems - Chippewa Operating System Documentation, Vol. I, Preliminary Edition (updated May 1966)	
/J.P./	LR	CDC 6000 Series Computer Systems - Chippewa Operating System Documentation, Vol. II, Preliminary Edition, Peripheral Packages and Overlays (Oct 1965)	
/J.P./	LS	CDC 6000 Series Computer Systems - Chippewa Operating System Documentation, Vol. III, Preliminary Edition, DSD - The Systems Display, (Nov 1965)	
/J.P./	LT	CDC 6000 Series Computer Systems ASCENT General Information Manual; Control Data Publication No. 60135400 (Feb 66)	
/J.P./	LU	CDC 6000 Series Computer Systems Chippewa Operating System Reference Manual; Control Data Publication No. 60134400 (Dec 1965)	
/J.P./	LV	CDC 6000 Series Computer Systems Hardware Reference Manual; Control Data Publication No. 60100000 (Aug 1978)	
/J.P./	LW	CDC 6000 Series Computer Systems/ 7600 Computer System: 6000 Compass Version 2, 7600 Versions 1 & 2 Reference Manual; Control Data Publication No. 60279900, Revision D, (1970, 1971, 1972)	
/J.P./	LX	CDC 6000 Series Computer Systems: Chippewa Operating System FORTRAN Reference Manual; Control Data Publication No. 60132700A (May 1966)	

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/J.P./	LY	CDC 6000 Series Computer Systems: Peripheral Equipment Reference Manual; Control Data Publication No. 60156100, Revision J (Mar 1970)	
/J.P./	LZ	CDC 6000 Series Computer Systems: Site Preparation and Installation Manual; Control Data Publication No. 60142400, Revision B (Sep 1965)	
/J.P./	MA	CDC 6000 Series Computer Systems: FORTRAN Extended General Information, Contral Data Publication No. 60176400 (Oct 1966)	
/J.P./	MB	CDC 6000 Series FORTRAN Extended 4.0, Internal Maintenance Specifications, (1971)	
/J.P./	MC	CDC 6000 Series Introduction and Peripheral Processors Training Manual, Second Edition; Control Data Publication No. 60250400 (Nov 1968)	
/J.P./	MD	CDC 6400 Central Processor; Control Data Publication No. 60257200 (Feb 1967)	
/J.P./	ME	CDC 6400/6500/6600 ASCENT-TO-COMPASS TRANSLATOR; Control Data Publication No. 60191000 (Mar 1967)	
/J.P./	MF	CDC 6400/6500/6600 Computer System Input/Output Specification; Control Data Publication No. 60045100 (September 1967)	
/J.P./	MG	CDC 6400/6500/6600 Computer System Instant SMM; Control Data Publication No. 60299500 (Nov 1969)	
/J.P./	MH	CDC 6400/6500/6600 Computer Systems COMPASS Reference Manual; Data 60190900, Revision B (Mar 1969)	

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/J.P./	MI	CDC 6400/6500/6600 Computer Systems Reference Manual; Control Data Publication No. 60100000, Revision K (Aug 1970)	
/J.P./	MJ	CDC 6400/6500/6600 Computer Systems Reference Manual; Control Data Publication No. 60100000D (1965, 1966, 1967)	
/J.P./	MK	CDC 6400/6500/6600 Extended Core Storage Systems Reference Manual; Control Data Publication No. 60225100, (Feb 1968)	
/J.P./	ML	CDC 6400/6500/6600 Jovial General Information Manual; Control Data Publication No. 60252100A (Mar 1969)	
/J.P./	MM	CDC 6400/6600 Computer Systems: ASCENT/ASPER Reference Manual; Control Data Publication No. 60172700 (Jul 1966)	
/J.P./	MN	CDC 6400/6600 FORTAN Conversion Guide; Data Publication No. 60175500 (Aug 1966)	
/J.P./	MO	CDC 6400/6600 Systems Bulletin (10 Oct 1966), 84 pages	
/J.P./	MP	CDC 6400/6600, Export/Import 8231 Reference Manual; Data Publication No. 60189100 (April 1967)	
/J.P./	MQ	CDC 6600 Central Processor Vol. 1; Control & Memory; Data Control Publication No. 020167 (March 1967)	
/J.P./	MR	CDC 6600 Central Processor, Vol. 2, Functional Units; Control Data Publication No. 60239700 (Mar 1967)	

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/J.P./	MS	CDC 6600 CHASSIS TABS; Control Data Publication No. 63016700A (Apr 1965)	
/J.P./	MT	CDC 6600 CHASSIS TABS; Control Data Publication No. 63019800 (Mar 1965)	
/J.P./	MU	CDC 6600 Chippewa Operating System; Control Data Publication No. 60124500, Revision C (April 1965)	
/J.P./	MV	CDC 6600 Computer System 6601 A-J, 6613A/B/C, 6604A/B/C, 6614-A/B/C Central Processor (Including Functional Units) Vol. 1, Diagrams & Circuit Description; Control Data Publication No. 60119300BT(Jan 1968)	
/J.P./	MW	CDC 6600 Computer System 6601 A-J, 6613A/B/C, 6604A/B/C, 6614-A/B/C Peripheral and Control Processor/Central Memory/Clock/Extended Core Storage Coupler (Std Opt 10102 and/or Spec Opt 60080)/ Power Wiring, Vol. 2, Diagrams & Circuit Descriptions; Control Data Publication No. 60119300BT (Jan 1968)	
/J.P./	MX	CDC 6600 Computer System Operating System/Reference Manual, SIPROS66, 1st ed.; Control Data Publication No. 60101800A (1965)	
/J.P./	MY	CDC 6600 Computer System Programming System/Reference Manual, Vol. 1. ASCENT; Control Data Publication No. 60101600B (1965)	
/J.P./	MZ	CDC 6600 Computer System Programming System/Reference Manual, Vol. 2, ASPER; Control Data Publication No. 60101700B (1965)	
/J.P./	NA	CDC 6600 Computer System Programming Vol. 3, FORTRAN 66; Control Data Publication No. 60101500B (1965)	

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/J.P./	NB	CDC 6600 Computer Training Manual Vol. 2, Preliminary Edition, Section 7.2 Shift Functional Units, 164 pages	
/J.P./	NC	CDC 6600 Data Channel Equipment 6602-B/6612-A, 6603-B, 6622-A, 6681-B, 6682-A/6683-A, S.O. 60022, 60028, 60029, Diagrams & Circuit Description' Control Data Publication No. 60125000, Revision G (June 1966)	
/J.P./	ND	CDC 6600 Training Manual; Control Data Publication No. 60147400, Revision A (June 1965)	
/J.P./	NE	CDC 6603 - A/B/C Disk File Controller Reference Manual; Control Data Publication No. 60334000 (1970)	
/J.P./	NF	CDC 6638 Disk File Subsystem Training Supplement; Control Data Publication 602500800A (Oct 1968)	
/J.P./	NG	CDC 6638 Disk File System: Standard Option 10037-A, 6639-A/B File Controller -- Diagrams and Circuit Description/Maintenance/Maintenance Aids/Parts List/ Wire Lists/Chassis Tabs; Control Data No. 60227300, Revision H (Mar 1974)	
/J.P./	NH	CDC 6639 - A/B Disk File Controller Reference Manual; Control Data Publication No. 60334100E (Aug 1973)	
/J.P./	NI	CDC 6639 Disk Controller Training Manual Test Edition (Sep 1967), 28 pages.	
/J.P./	NJ	CDC APL Version 2 Reference Manual, CDC Operating Systems : NOS; Control Data Publication NO. 60454000F (Nov 1980)	
/J.P./	NK	CDC Basic Version 3 Reference Manual: NOS 1 & NOS/BE 1; Control Data Publication No. 19983900G (Oct 1980)	

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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	90/009,034
				Filing Date	March 31, 2008
				First Named Inventor	---
				Art Unit	3992
(Use as many sheets as necessary)				Examiner Name	Joseph R. Pokrzywa
Sheet	29	of	54	Attorney Docket Number	0081-011X1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/J.P./	NL	CDC Chippewa Operating System, Document Class ERS, System No. E012, Version 1.1; External Reference Specifications - Chippewa Operating System, (Jun 1966)	
/J.P./	NM	CDC Chippewa Operating System, Document Class SIR, System No. E012, Version 1.0, (March 3, 1966)	
/J.P./	NN	CDC Chippewa Operating System, Document Class SIR, System No. E012, Version 1.1, (March 3, 1966)	
/J.P./	NO	CDC COBOL Version 4 Instant Manual, Cyber 170 Series, Cyber 70 Models 72, 73, 74, 6000 Series; Control Data Publication No. 60497000A (Feb 1976)	
/J.P./	NP	CDC COBOL Version 5 Instant Manual, Operating Systems: NOS 1/BE 1; Control Data Publication No. 60497300B (Feb 1981)	
/J.P./	NQ	CDC CODES/Control Data 6400/6500/6600 Computer Systems; Control Data Publication No. 60141900, Revision C (6/15/67)	
/J.P./	NR	CDC CODES/Control Data 6400/6500/6600/6700 Computer Systems; Control Data Publication No. 60141900, Revision D (6/10/70)	
/J.P./	NS	CDC CODES/Control Data 6600; Control Data Publication No. 60141900, Revision A (May 1965)	
/J.P./	NT	CDC COMPASS Version3 Instant, Operating Systems: NOS 1, NOS 2, NOS/ BE 1, SCOPE 2; Control Data Publication No. 60492800D (Jun 1982)	
/J.P./	NU	CDC Course No. FH4010-1C, NOS Analysis, Student Handout, Revision C (Apr 1980)	

Examiner Signature	/Joseph Pokrzywa/	Date Considered	11/10/2009

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/J.P./	NV	CDC Course No. FH4010-4C NOS Analysis, Study Dump (Apr 1980)	
/J.P./	NW	CDC Cyber 170 Models 720, 730, 740, 750 and 760 Model 176 (Level B/C) Computer Systems, Codes; Control Data Publication No. 60456920C, (Jun 1981)	
/J.P./	NX	CDC Cyber 70 Computer Systems Models 72, 73, 74, 6000 Computer Systems: FORTRAN Reference Manual Models 72, 73, 74 Version 2.3, 6000 Version 2.3; Control Data Publication No. 19980400, Revision F (July 1972)	
/J.P./	NY	CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems – ALGOL Reference Manual, Cyber 70 Series Version 4, 6000 Series Version 4, 7600 Series Version 4; Control Data Publication No. 60384700A (Aug 1973)	
/J.P./	NZ	CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems: COBOL INSTANT Models 72, 73, 74 Version 4, Model 76 Version 1, 6000 Version 4; Control Data Publication No. 60328400A (Dec 1971)	
/J.P./	OA	CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems: FORTRAN Extended Instant Models 72, 73, 74 Version 4, Model 76 Version 2, 7600 Version 2, 6000 Version 4; Control Data Publication No. 60357900A (Nov 1971)	
/J.P./	OB	CDC Cyber 70 Computer Systems Models 72, 73, 74, 76, 7600 Computer System, 6000 Computer Systems: FORTRAN Extended Reference Manual Models 72, 73, 74 Version 4, Model 76 Version 2, 6000 Version 4; Control Data Publication No. 60305600A (Oct 1971)	
/J.P./	OC	CDC Cyber 70 Series 6000 Series Computer Systems: APL*Cyber Reference Manual; Control Data Publication No. 19980400B (July 1973)	
/J.P./	OD	CDC Cyber 70 Series Computer Systems 72, 73, 74, 6000 Series Computer Systems -- Kornos 2.1 Workshop Reference Manual; Control Data Publication No. 97404700D (1976)	
/J.P./	OE	CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, KRONO 2.1 Operator Guide; Control Data Guide; Control Data Publication 60407700A (Jun 1973)	

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/J.P./	OF	CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, KRONOS 2.1 Installation Handbook; Control Data Publication no. 60407500A (Jun 1973)	
/J.P./	OG	CDC Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems, KRONOS 2.1 Time-Sharing User's Reference Manual; Control Data Publication No. 60407600B (May 1974)	
/J.P./	OH	CDC Cyber 70/ Model 76 Computer System, 7600 Computer System: FORTRAN Run, Version 2 Reference Manual; Control Data 60360700C (May 1974)	
/J.P./	OI	CDC Cyber Interactive Debug Version 1 Guide for Users of FORTRAN Extended Version 4, CDC Operating Systems: NOS 1, NOS/ BE 1, Control Data Publication No. 60482700A (Feb 1979)	
/J.P./	OJ	CDC Cyber Interactive Debug Version 1 Guide for Users of FORTRAN Version 5, Operating Systems: NOS 1, NOS/ BE 1; Control Data Publication No. 60484100C (Sep 1984)	
/J.P./	OK	CDC Cyber Interactive Debug Version 1 Reference Manual, NOS 1, NOS 2, NOS/ BE 1; Data Control Publication NO. 60481400D (Jun 1984)	
/J.P./	OL	CDC Cyber Loader Version 1 Instant, CDC Operating System NOS1, NOS/ BE 1; Control Data Publication No. 60449800C (Aug 1979)	
/J.P./	OM	CDC Disk Storage Subsystem -- Operation and Programming Manual; Control Data Publication No. 60363900, Version T (1972 -1980)	
/J.P./	ON	CDC FORTRAN Extended 2.0, Document Class ERS, System No. C012, (Dec 1966)	
/J.P./	OO	CDC FORTRAN Extended 2.0, Document Class IMS, Internal Maintenance Specifications - 64/65//6600 V FORTRAN Extended Version 2 (Mar 1969)	

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/J.P./	OP	CDC FORTRAN Extended Version 4 Instant Manual, Operating Systems: NOS 1, NOS/BE 1, SCOPE 2; Control Data Publication No. 60497900B (Jun 1981)	
/J.P./	OQ	CDC FORTRAN Extended, Sales Technical Memorandum (May 1967)	
/J.P./	OR	CDC FORTRAN Version 5 Instant, CDC Operating Systems: NOS 1, NOS/ BE 1, SCOPE 2; Control Data Publication No. 60483900A (Jan 1981)	
/J.P./	OS	CDC GED FORTRAN Extended 1.0, Product No. C012, Dept No. 254, Project No. 4P63FTN (Aug 1967)	
/J.P./	OT	CDC INSTANT 6400/3500/6500 SIMULA; Control Data Publication No. 60235100, Revision A (Feb 1969)	
/J.P./	OU	CDC INSTANT 6400/6500/6600 COMPASS; Control Data Publication No. 60191900, Revision A (1968)	
/J.P./	OV	CDC INSTANT FORTRAN 2.3 (6000 Series); Data Publication No. 60189500D (May 1969)	
/J.P./	OW	CDC Internal Maintenance Specification: FORTRAN V5, ; Control Data Publication No. 77987506A	
/J.P./	OX	CDC Internal Maintenance Specification: FORTRAN V5, ; Control Data Publication No. 77987506A	
/J.P./	OY	CDC KRONOS 2.1 Reference Manual Volume 1 of 2; Control Data Cyber 70 Series Models 72/73/74, 6000 Series Computer Systems; Control Data Publication No. 60407000D (Jun 1975)	

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/J.P./	OZ	CDC KRONOS 2.1 Time-Sharing User's Reference Manual, Cyber 70 Series Models 72, 73, 74, 6000 Series Computer Systems; Control Data Publication No. 60407600D (Jun 1975)	
/J.P./	PA	CDC Model dd 60A Computer Control Console/Customer Engineering Manual; Control Data Publication No. 82100010 (Mar 1965)	
/J.P./	PB	CDC Model dd60b Computer Control Console/Customer Engineering Manual; Control Data Publication No. 82103500 (Feb 1967)	
/J.P./	PC	CDC Network Products: Network Access Method Version 1, Network Definition Language Reference Manual; Control Data Publication No. 60480000J (May 1981)	
/J.P./	PD	CDC Network Products: Network Terminal User's Instant -- Operating System NOS 1; Control Data Publication No. 60455270C, (Oct 1980)	
/J.P./	PE	CDC NOS 2 Operations Handbook; Control Data Publication No. 60459310, (Aug 1994)	
/J.P./	PF	CDC NOS Version 1 Applications Programmer's Instant, CDC Computer Systems: Cyber 170 Series, Cyber 70 Models 71, 72, 73 74, 6000 Series; Control Data Publication No. 60436000H (Jan 1980)	
/J.P./	PG	CDC NOS Version 1 Internal Maintenance Specification Volume 1 of 3; Control Data Publication No. 60454300B (Aug 1979)	
/J.P./	PH	CDC NOS Version 1 Internal Maintenance Specification Volume 2 of 3; Control Data Publication No. 60454300B (Aug 1979)	
/J.P./	PI	CDC NOS Version 1 Internal Maintenance Specification Volume 3 of 3; Control Data Publication No. 60454300B (Aug 1979)	

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/J.P./	PJ	CDC NOS Version 1 Operator's Guide, CDC Computer Systems: Cyber 170 Series, Cyber 70 Model 71, 72, 73 74, 6000 Series (Dec 1980)	
/J.P./	PK	CDC NOS Version 1 Reference Manual Volume 1 of 2, CDC Computer Systems: Cyber 170 Series, Cyber 70 Models 71, 72, 73, 74, 6000 Series; Control Data Publication No. 60435400J (1979)	
/J.P./	PL	CDC NOS Version 1 Reference Manual Volume 2 of 2, CDC Computer Systems: Cyber 170 Series, Cyber 70 Models 71, 72, 73, 74, 6000 Series; Control Data Publication No. 60445300E (1977)	
/J.P./	PM	CDC NOS Version 1 System Maintenance Reference Manual; Control Data Publication No. 60455380H (Apr 1981)	
/J.P./	PN	CDC NOS Version 2 Analysis Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60459300D (Oct 84)	
/J.P./	PO	CDC NOS Version 2 Analysis Handbook; Control Data Publication No. 60459300U (Jul 1994)	
/J.P./	PP	CDC NOS Version 2 Installation Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60459320E_ (Mar 1985)	
/J.P./	PQ	CDC NOS Version 2 Operation/Analysis Handbook, Cyber 170, Cyber 70 Models 71, 72, 73, 74 6000, Control Data Publication No. 60459310C (Oct 1983)	
/J.P./	PR	CDC NOS Version 2 System Maintenance Reference Manual, Cyber 170, Cyber 70 Models 71 , 72, 73 74, 6000; Control Data Publication No. 60459300C (Oct 1983)	
/J.P./	PS	CDC NOS/BE Version 1 Diagnostic Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60494400-V (1986)	

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/J.P./	PT	CDC NOS/BE Version 1 Installation Handbook, Cyber 180, Cyber 170, Cyber 70 Models 71, 72, 73, 74, 6000; Control Data Publication No. 60494300AB (Dec 1986)	
/J.P./	PU	CDC NOS/BE Version 1 Reference Manual, Cyber 170 Series, Cyber 70 Models 71, 72, 73, 74, 6000 Series; Control Data Publication No. 60493800M 1981	
/J.P./	PV	CDC Outline of Reports on "Feasibility Study of 64/6600 FORTRAN Ver 3.0 and Conversational FORTRAN, FORTRAN Study Project, Product No. X010, Dept No. 254, Project No. 4P63, (Jun 1966)	
/J.P./	PW	CDC Pascal Version 1 Reference Manual, Operating Systems: NOS 2; Control Data Publication No. 60497700 (Sep 1983)	
/J.P./	PX	CDC Pascal Version 1 Reference Manual, Operating Systems: NOS 2; Control Data Publication No. 60497700A (Dec 1982)	
/J.P./	PY	CDC PL/1 Version 1 Instant, CDC Operating Systems: NOS 1, NOS/ BE 1; Control Data Publication No. 60483700A (Nov 1979)	
/J.P./	PZ	CDC SIMSCRIPT 11.5 Instant; Control Data Publication No. 84000450B (Sep 1978)	
/J.P./	QA	CDC Sort/Merge Version 4 and 1 Instant, Operating Systems: NOS 1, NOS/BE 1, SCOPE 2; Control Data Publication No. 60497600C (Jan 1981)	
/J.P./	QB	CDC Sort/Merge Version 5 Reference Manual, Operating Systems: NOS 2, NOS/ BE 1; Control Data Publication No. 60484800C (Feb 1984)	
/J.P./	QC	CDC SYMPL Version 1 Instant, NOS 1, NOS/BE 1, SCOPE 2; Control Data Publication NO. 60482600A (May 1978)	

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/J.P./	QD	CDC SYMPL Version 1 Users Guide, Operating Systems: NOS 1, NOS/BE 1, SCOPE 2; Control Data Publication No. 60499800B (Apr 1978)	
/J.P./	QE	CDC Update Instant, Cyber 170 Series, Cyber 70 Series, 6000 Series, 7600 Computer Systems; Control Data Publication No. 60450000A (Nov 75)	
/J.P./	QF	CDC Update Reference Manual Operating Systems: SCOPE 3.4, KRONOS 2.1; Control Data Publication No. 60342500, Revision H (1971 - 1976)	
/J.P./	QG	CDC XEDIT Version 3 Reference Manual, Operating System: NOS 1; Control Data Publication No. 60455730B (Aug 1979)	
/J.P./	QH	Chippewa Laboratories FORTRAN Compiler Run, Preliminary Edition, CDC 6000 Series Computer Systems, (Apr 1966)	
/J.P./	QI	CHO et al., WAM 3.6: A 40K Cache Memory and Memory Management Unit," ISSCC '86, Feb 19, 1986.	
/J.P./	QJ	CHO et al., "The Memory Architecture and the Cache and Memory Management Unit for the Fairchild CLIPPER Processor," Report No. UCB/CSD 86/289, Computer Science Division (EECS), University of California (April 1986)	
/J.P./	QK	CLIPPER™ 32-Bit Microprocessor, Introduction to the CLIPPER Architecture, published by Fairchild in 1986.	
/J.P./	QL	CORDELL, II et al., "Advanced Interactive Executive Program Development Environment," IBM Systems Journal, 1987; 26(4):361-382	
/J.P./	QM	CRAWFORD, "The i486 Executing Instructions in One Clock Cycle," IEEE Micro, pp. 28 - 36 (Feb 1990)	

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/J.P./	QN	Cray-1 Computer System Hardware Reference Manual, Publication No. 2240004, Rev C, November 4, 1977	
/J.P./	QO	Disk Routines and Overlays, Chippewa Operating System, CDC Development Division - Applications, (Nov 1965)	
/J.P./	QP	DITZEL et al., "The Hardware Architecture of the CRISP Microprocessor," AT & T Information Systems, ACM, pages 309-319 and table of contents (1987).	
/J.P./	QQ	DOWSING et al., "Computer Architecture: A First Course, Chapter 6: Architecture and the Designer," Van Nostrand Reinhold (UK) Co. Ltd., pp. 126-139.	
/J.P./	QR	DS5000 Soft Microcontroller User's Guide Preliminary V 1.0, Dallas Semiconductor	
/J.P./	QS	DUELL, C. H., "Everything that can be invented has been invented," 2 pages downloaded from http://www.tplgroup.net/patents/index.php	
/J.P./	QT	EVANS et al., "An Experimental 512-bit Nonvolatile Memory with Ferroelectric Storage Cell," IEEE Journal of Solid-Sate Circuits, 23(5):1171-1175.	
/J.P./	QU	Excerpt from A Seymour Cray Perspective http//research.microsoft.com/users/gbell/craytalk/sld029.htm (Slide 29)	
/J.P./	QV	Excerpt from A Seymour Cray Perspective http://research. Microsoft.com/users/gbell/craytalk/sld/001.htm (Slide 1)	
/J.P./	QW	Fairchild Microcomputers, F8/3870, F6800, BIT Slice, IC Master 1980, pages 1, 2016-2040 (1980).	

Examiner Signature	/Joseph Pokrzywa/	Date Considered	11/10/2009

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/J.P./	QX	FIASCONARO, J., "Microarchitecture of the HP9000 Series 500 CPU," Microarchitecture of VLSI Computers, NATO ASI Series No. 96, Antognetti, eds., pages 55-81	
/J.P./	QY	Field Maintenance Print Set, KA780-01-01 Rev. A,	
	~~QZ~~	~~File History of '449 Patent: Office Action of January 31, 2000~~	
	~~RA~~	~~File History of '226 Patent: Amendment of April 11, 1996~~	
	~~RB~~	~~File History of '998 Patent: Amendment of January 8, 1997~~	
	~~RC~~	~~File History of '226 Patent: Amendment of July 3, 1997~~	
	~~RD~~	~~File History of '594 Patent: Amendment of June 12, 1997~~	
/J.P./	RE	FISHER et al., "Very Long Instruction Word Architectures and the ELI-512," ACM pp. 140-150 (1983)	
/J.P./	RF	FUKUI et al., "High Speed CMOS 4-bit Microcomputer SM550 Series," pp. 107 -109 published 1982, 1983. (Document in Japanese)	
/J.P./	RG	FURBER, VSLI RISC Architecture and Organization, Chapter 3: Commercial VLSI RISC, pp. 124 - 129, Marcel Dekker, Inc., 1989	

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NON PATENT LITERATURE DOCUMENTS			
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/J.P./	RH	GB Patent Application 8233733, INMOS, Ltd. Microcomputer, filed 11-26-1982	
/J.P./	RI	GE 600 Series, publication	
/J.P./	RJ	GE-625 / 635 Programming Reference Manual, revised January 1996	
/J.P./	RK	GERSHON, Preface, IBM Systems Journal 26(4):324-325	
/J.P./	RL	GREEN et al., "A Perspective on Advanced Peer-to-Peer Networking," IBM Systems Journal, 1987; 26(4):414-428.	
/J.P./	RM	GRIMES et al., "64 bit Processor, The Intel i860 64-Bit Processor: A General-Purpose CPU with 3D Graphics Capabilities", published by Intel, p. 85 (July 1989)	
/J.P./	RN	GRISHMAN, R., "Assembly Language Programming for the Control Data 6000 and Cyber Series Algorithmics"	
/J.P./	RO	GRONDALSKI et al., "Microprocessors-Special Purpose - THPM 16.3: A VLSI Chip Set for a Massively Parallel Architecture," 1987 IEEE International Solid-State Circuits Conference, February 26, 1987, pp. 1998- 198.	
/J.P./	RP	GROSS et al., "Measurement and evaluation of MIPS architecture and processor," ACM Trans. Computer Systems, pp.229-257 August 1988.	
/J.P./	RQ	GUTTAG, "The TMS34010: An Embedded Microprocessor", IEEE Micro, vol. 8, no. 3, May 1988, pp. 39-52	

Examiner Signature	/Joseph Pokrzywa/	Date Considered	11/10/2009

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/J.P./	RR	HANSEN, "A RISC Microprocessor with Integral MMU and Cache Interface," ICCD '86, pp. 145 - 148, 1986	
/J.P./	RS	HENNESSY et al., "Hardware/software tradeoff for increased performance," Proceedings of the Symposium on Architectural Support for Programming Languages and Operating Systems,, pages 2-11. ACM, April 1982	
/J.P./	RT	HENNESSY et al., "Hardware/software Tradeoff for Increased Performance," Technical Report No. 22.8, Computer Systems Laboratory, Feb 1983, 24 pages	
/J.P./	RU	HENNESSY et al., "MIPS: A Microprocessor Architecture," IEEE, pages 17-22 (1982).	
/J.P./	RV	HENNESSY et al., "MIPS: A VLSI Processor Architecture" VLSI Systems and Computer, Kung eds. , Carnegi-Mellon University, pp. 337 - 346 (1981)	
/J.P./	RW	HENNESSY et al., "The MIPS Machine", COMPCON, IEEE, Spring 1982, pp. 2-7.	
/J.P./	RX	HENNESSY, "Performance Issues in VLSI Processor Design," IEEE on VLSI in Computers, , pp. 153 - 156. (1983)	
/J.P./	RY	HINTON, "80960 -- Next Generation, "COMPCON Spring 89, IEEE, 13-16 (1989)	
/J.P./	RZ	Hitachi America Ltd., "8-Bit Single-Chip Microprocessor Data Book", July 1985, Table of Contents and pp. 251-279.	
/J.P./	SA	HOLLINGSWORTH et al., "The Fairchild Clipper: Instruction Set Architecture and Processor Implementation," Report No. UCB/CSD 87/329, Computer Science Division (EECS), University of California Berkeley, California, (February 11, 1987)	

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/J.P./	SB	HOROWITZ et al., "A 20- MIPS Peak, 32-bit Microprocessor with On-Chip Cache," IEEE Journal of Solid State Circuits, SC-22(5):790-799 (October 1987).	
/J.P./	SC	HP 9000 Instrument Controllers, Technical Specifications Guide, October, 1989.pdf	
/J.P./	SD	HP 9000 Series Computer Systems, HP-UX Reference 09000-090004, Preliminary November, 1982	
/J.P./	SE	HP Sacajawea External Reference Specification Preliminary Version 1.1 (1/14/87).	
/J.P./	SF	HUGHES, "Off-Chip Module Clock Controller," Delphion, IBM Technical Disclosure Bulletin, Sep 1989	
/J.P./	SG	HUNTER, "Introduction to the Clipper Architecture," IEEE Micro, pp. 6-26 (August 1987)	
/J.P./	SH	IBM RT PC, BYTE 1986 Extra Edition, Inside The IBM PCs, pp. 60-78	
/J.P./	SI	IBM Systems Reference Library, IBM System/360 Model 67 Functional Characteristics, File No. S360-01, Form A27-2719-0, published by IBM (1967).	
/J.P./	SJ	IEEE Std 796-1983, Microcomputer System Bus, pp. 9-46	
/J.P./	SK	Index of/pdf/cdc/6x00, downloaded from http://www.bitsavers.org/pdf/cdc/6x00/	

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/J.P./	SL	INMOS Engineering Data, IMS T414M Transputer, Extended Temperature," (August 1987).	
/J.P./	SM	INMOS IMS T212 Engineering Data Preliminary Data Sheet (August 1987)	
/J.P./	SN	INMOS IMS T414 Data Sheet, (June 1987)	
/J.P./	SO	INMOS IMS T414 Transputer, Engineering Data, pp. 107-163.	
/J.P./	SP	INMOS IMS T414 Transputer, Preliminary Data	
/J.P./	SQ	INMOS IMS T800 Transputer Preliminary Data Sheet April 1987	
/J.P./	SR	INMOS Limited, IMS T424 Transputer Reference Manual, 1984	
/J.P./	SS	INMOS Limited, Transputer Reference Manual, Prentice Hall, 368 pages (1988), relevant pages 1-4, 73 and 96	
/J.P./	ST	INMOS M212 Disk Processor Product Overview October 1987 , 12 pages total.	
/J.P./	SU	Intel 386TM DX Microprocessor 32-Bit CHMOS Microprocessor With Integrated Memory Management (1995)	

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/J.P./	SV	Intel 4004 Data Sheet Single Chip 4-Bit 9-Channel Microprocessor, pages 8-15 to 8-23	
/J.P./	SW	Intel 8008 8-Bit Parallel Central Processor Unit, published by Intel (November 1972), Users Manual	
/J.P./	SX	Intel 80386 Programmer's Reference Manual, published by Intel (1986)	
/J.P./	SY	Intel 80960CA User's Manual published by Intel (1989)	
/J.P./	SZ	Intel Architecture Optimization Manual, Order Number 242816-003, published by Intel (1997)	
/J.P./	TA	Intel Architecture Software Developer's Manual, Volume 1: Basic Architecture, published by Intel (1997)	
/J.P./	TB	INTEL i860 64-Bit Microprocessor, Intel Corporation February 1989.	
/J.P./	TC	Intel MCS-4 Micro Computer Set, Integrated Circuit Engineering Collection (November 1971)	
/J.P./	TD	Intel, iAPX 386 High Performance 32-Bit Microprocessor Product Review (April 1984)	
/J.P./	TE	Intel 8080A/8080A-1/8080A-2, 8-Bit N-Channel Microprocessor, Order Number: 231453-001, Its Respective Manufacturer (Nov 1986)	

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/J.P./	TF	JGUPPI et al., "A 20 MIPS Sustained 32b CMOS with 64b Data Bus," IEEE Int'l Solid State Circuits Conf., pages 84-86 (1989).	
/J.P./	TG	JOHNSON et al., "A Variable Delay Line PLL for CPU-Coprocessor Synchronization," IEEE Journal of Solid-State Circuits, 23(5): 1218-1223, October 1988	
/J.P./	TH	KATEVENIS et al., "Reduced Instruction Set Computer Architecture for VLSI," Doctoral Dissertation, Oct 1983	
/J.P./	TI	KATEVENIS et al., "The RISC II Micro-Architecture," Journal of VLSI and Computer Systems, 1(2):138-152 (1984)	
/J.P./	TJ	KIPP, "Micron Technology Inc. Reports Financial Results," Business Wire, New York, Sep 26, 1988	
/J.P./	TK	KOHN et al., "Introducing INTEL i860 64-Bit Microprocessor," Intel Corporation, IEEE Micro (August 1989)	
/J.P./	TL	KOOPMAN, "RTX 4000," Proceedings of 1989 Rochester Forth Conference, pp. 84-86.	
/J.P./	TM	KOOPMAN, "The WISC Concept: A proposal for a writable instruction set computer," BYTE, pp. 187-193. (April 1987)	
/J.P./	TN	KOOPMAN, Jr. et al. "MVP Microcoded CPU/16 Architecture," Proceedings of 1986 Rochester Forth Conference, pp. 277-280.	
/J.P./	TO	KOOPMAN, Jr. et al., "WISC Technologies, Inc., Writable Instruction Set, Stack Oriented Computers: The WISC Concept," 1987 Rochester Forth Conference, Journal of Forth Application and Research, 5(1):49-71.	

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/J.P./	TP	KOOPMAN, Jr., Stack Computers: the new wave, 1989	
/J.P./	TQ	LOUCKS et al., "Advanced Interactive Executive (AIX) Operating System Overview," IBM Systems Journal, 1987; 26(4):326-345	
/J.P./	TR	LSI Logic Corporation MIPS Architecture RISC Technology Backgrounder, "Introduction to RISC Technology," LSI Logic Corporation (April 1988).	
/J.P./	TS	MATICK, "Self-Clocked Cache," Delphion, IBM Technical Disclosure Bulletin, Apr 1985	
/J.P./	TT	Matsushita Electric, 8 bit Dual 1-chip Microcomputer MN1890 Series User's Manual, translation of original Japanese language document, by Matsushita Electric Industrial Co., Ltd. Semiconductor Sales Division	
/J.P./	TU	Matsushita Electronics Corporation, MN1880 (MN18882) Instruction Manual, (document in Japanese) 1988	
/J.P./	TV	Matsushita Electronics Corporation, MN188166 User's Manual, Japanese language document	
/J.P./	TW	Matsushita Electronics Corporation, MN18882 LSI User's Manual, Japanese language document, 1987	
/J.P./	TX	Matsushita Electronics Corporation, Specification Sheet, MN18882 (Book1) translation of the Japanese language original, Code No. MIG0175, Matsushita Electronics Industry Corporation, Microcomputer Products Division, 10/2/90.	
/J.P./	TY	MATTHYS R. J., Crystal Oscillator Circuits, John Wiley & Sons, pages 25-64 (1983).	

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/J.P./	TZ	MAY, "The Transputer and Occam," International Conference on the Impact of Digital Microelectronics and Microprocessors on Particle Physics, held 3/28-30/88, published by World Scientific in 1988, Budnich, eds. pages 205-211.	
/J.P./	UA	MAY, D., "The Influence of VLSI Technology on Computer Architecture," INMOS Ltd, pages 247-256 (1988).	
/J.P./	UB	McFarlane letter via e-mail from to Hoge, Agarwal, & Spears re: "Attorney Eyes Only" status of depositions of Daniels and McDermott, dated 1/17/08	
/J.P./	UC	MEAD et al., eds., Introduction to VLSI Systems, Addison Wesley Publishers, (1980), 144 pages.	
/J.P./	UD	MILLER, "Frequency Modulated Ring Oscillator for a Mode Regulated Substrate Bias Generator, Delphion, IBM Technical Disclosure Bulletin, Sep 1989	
/J.P./	UE	MILLS et al., "Box Structured Information Systems, " IBM Systems Journal, 1987; 26(4):395-413	
/J.P./	UF	MINYARD, Using a TMS320C30 Serial Port as an Asynchronous RS-232 Port, Application Brief: SPRA240, Texas Instruments (May 1994)	
/J.P./	UG	MMP Portfolio, News Release: Roland Becomes 50th Licensee, Setting a Major Milestone in Moore Microprocessor Patent Licensing Program," 3 pages (May 1, 2009)	
/J.P./	UH	MOELANDS, A. P. M., "Serial I/O with the MAB8400 series microcomputers," Electronic Components and Applications, 3(1):38-46 (1980).	
/J.P./	UI	MOORE, P., "INMOS Technical Note 15: IMS B005 Design of a Disk Controller board with drives," December 3, 1986	

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/J.P./	UJ	Mostek Corp., "Mostek 1981 3870/F8 Microcomputer Data Book", February 1981, pp. III-76 through III-77, III-100 through III-129, and VI-1 through VI-11	
/J.P./	UK	Mostek Corp., Advertisement, EDN, November 20, 1976.	
/J.P./	UL	Motorola Inc., MC 68332 32-Bit Microcontroller System Integration User's Manual Preliminary Edition, Revision 0.8, (1989)	
/J.P./	UM	Motorola MC146805H2, Advance Information, pages 1-12	
/J.P./	UN	Motorola MC68HC11A8 HCMOS Single-Chip Microcomputer, table of contents and introduction (1985).	
/J.P./	UO	Motorola Semiconductors MC146805H2, Product Brochure.	
/J.P./	UP	Motorola, "How to Take Control" product brochure by Motorola (1988)	
/J.P./	UQ	MOTOROLA, MC68300 Family MC68332 User's Manual, (1995).	
/J.P./	UR	MOTOROLA, MC88100 RISC Microprocessor User's Manual (1989).	
/J.P./	US	MOUSSOURIS et al., "A CMOS RISC Processor Integrated System Functions," Proceedings of 31st IEEE Computer Society International Conference, Cathedral Hill Hotel, San Francisco, CA March 3-6, 1986, pp. 126 - 131, 1986.	

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/J.P./	UT	National Semiconductor HPC16400/HPC36400/HPC46400 High-Performance MicroControllers with HDLC Controller product literature	
/J.P./	UU	NEC Data Sheet MOS Integrated Circuit uPD75008, 4 bit Single-Chip Microcomputer (1989).	
/J.P./	UV	NEC Electronics Inc. High-End, 8-Bit, Single-Chip CMOS Microcomputers product literature	
/J.P./	UW	NEC Electronics Inc. Microcomputer Products Microprocessors, Peripherals, & DSP Products Data Book Vol. 2 of 2 cover page	
/J.P./	UX	NEC Electronics Inc. Microcomputer Products Single-Chip Products Data Book Vol. 1 of 2 cover page	
/J.P./	UY	NEC Electronics Inc. MOS Integrated Circuit uPD70208H, 70216H Data Sheet, V40HL, V50HL 16/8, 16-Bit Microprocessor (1995)	
/J.P./	UZ	NEC Electronics Inc. MOS Integrated Circuit uPD7225 Programmable LCD Controller/Driver (1986, 1999)	
/J.P./	VA	NEC Electronics Inc. uPD78C10/C11/C14 8-Bit, Single-Chip CMOS Microcomputers with A/D Converter product literature	
/J.P./	VB	OLSON, "Semiconductor Die with Wiring Skirt (Packaging Structure), Delphion, IBM Technical Disclosure Bulletin, July 1978.	
/J.P./	VC	O'Neil, "Pipeline Memory System for Drams", Delphion, IBM Technical Disclosure Bulletin, May 1989.	

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/J.P./	VD	PAKER, Y., Multi-Processor Systems, Academic Press, pages 1-23 (1983)	
/J.P./	VE	Parent Continuity Data for 07/389,334 downloaded from PAIR	
/J.P./	VF	PATTERSON et al., "Architecture of a VLSI Instruction Cache for A RISC," ACM, pages 108-116 (1983).	
/J.P./	VG	PATTERSON et al., "RISC I: A Reduced Instruction Set VLSI Computer," Proceedings of the 8th annual symposium on Computer Architecture on Computer Architecture, Minneapolis, Minnesota, pp. 443 - 457 (May 1981)	
/J.P./	VH	PATTERSON, "RISC Watch", ACM, Vol. 12 (1):11-19 (March 1984).	
/J.P./	VI	PATTERSON, D. A., "Reduced Instruction Set Computers" Communication of the ACM, , 28(1):.8-21, January 1985	
/J.P./	VJ	POUNTAIN, "The Archimedea A310," BYTE, 1987	
/J.P./	VK	PRZYBYISKI et al., "Organization and VLSI Implementation of MIPS," Technical Report: CSL-TR-84-259, Apr1984	
/J.P./	VL	PRZYBYISKI, "The Design Verification and Testing of MIPS", 1984 Conference on Advanced Research in VLSI, pp. 100 - 109.	
/J.P./	VM	Rangel (PTI) letter by fax to McFarlane, Hoge, Agarawal & Spears re: non-confidential status of deposition transcripts of Daniels and McDermott, dated 1/15/08	

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Receipt date: 07/17/2009

PTO/SB/08A&B (02-09)

Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				**Application Number**	90/009,034
				Filing Date	March 31, 2008
				First Named Inventor	---
				Art Unit	3992
(Use as many sheets as necessary)				Examiner Name	Joseph R. Pokrzywa
Sheet	50	of	54	Attorney Docket Number	0081-011X1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/J.P./	VN	RAU et al., "The Cydra 5 Departmental Supercomputer, Design Philosophies, Decisions, and Trade-offs," IEEE, pages 12-36 (1989).	
/J.P./	VO	REEKIE, Realtime DSP: The TMS320C30 Course, Revision 3 (Feb 20 1994r)	
/J.P./	VP	RISC Roots: CDC 6000 (1965) www.//bwrc.eecs.berkley.edu/CIC/archive/cpu_history.html, downloaded 10/27/2006	
/J.P./	VQ	ROCHE et al., "Method of Assuring a Two-Cycle Start, Zero Cycle Stop, Non-Chopping on Chip Clock Control Throughout a VLSI Clock System," Delphion, IBM Technical Disclosure Bulletin, Sep 1989	
/J.P./	VR	ROWEN et al., "A Pipelined 32b NMOS Microprocessors and Microcontrollers," IEEE International Solida-State Circuits Conference, pp. 180 -181, 1984.	
/J.P./	VS	RUBINFELD et al., "The CVAX CPU, A CMOS VAX Microprocessor Chip", International Conference on Computer Design, October, 1987.	
/J.P./	VT	RYAN, D.P., "Intel's 80960: An Architecture Optimized for Embedded Control," IEEE Micro, published in June 1988.	
/J.P./	VU	SANAMRAD et al., "A Hardware Syntactic Analysis Processor," IEEE, August 1987, pp. 73-80	
/J.P./	VV	SEQUIN et al., "Design and Implementation of RISC I," pages 276-298 from VLSI Architecture, B. Randell and P.C. Treleaven, editors, Prentice Hall, 1983.	
/J.P./	VW	SHEPHERD et al., "Current and Future Transputers," INMOS Presentation given at June 15, 1988 Workshop on Computer Architecture	

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/J.P./	VX	SHERBURNE, R. W., "Processor Design Tradeoffs in VLSI," U.C. Berkeley, May, 1984. PhD Dissertation.	
/J.P./	VY	SHIH, "Microprogramming Heritage of RISC Design," Proceedings of the 23rd annual workshop and symposium on Microprogramming and microarchitecture, pp. 275-280. (1990)	
/J.P./	WA	SHYAM, "Hardware External Reference Specification for Enhanced Champion/Paladin," Revision of 11/11/86.	
/J.P./	WB	SIBIGTROTH, J. M., "Motorola's MC68HC11: Definition and Design of a VLSI Microprocessor," IEEE Micro, 4(1):54-65 (1984).	
/J.P./	WC	Signetics Microprocessor Data manual cover page	
/J.P./	WD	Signetics Microprocessor Products Data manual, 8X330 Floppy Disk Formatter/Controller product specification	
/J.P./	WE	Signetics Microprocessor Products Data manual, SC96AH Series Single-Chip 16-Bit Microcontrollers preliminary specification	
/J.P./	WF	SIMPSON et al., "The IBM RT PC ROMP Processor and Memory Management Unit Architecture," IBM systems Journal, December 1987; 26(4):346-360.	
/J.P./	WG	SIMPSON, R.O., " The IBM RT Personal Computer," BYTE 11(11):43-78 (October 1986).	
/J.P./	WH	SKRUHAK et al., "Modular Design of a High Performance 32-bit Microcontroller," IEEE 1989 Custom Integrated Circuits Conference, pages 23.8.1-23.8.4 (1989).	

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/J.P./	WI	STANLEY, R. C., "Microprocessors in brief," IBM J. Res. Develop., 29(2):110-118 (March 1985).	
/J.P./	WJ	Submicron Systems Architecture Project, Caltech Computer Science Technical Report, November 1, 1991	
/J.P./	WK	SULTAN et al., "Implementing System-36 Advanced Peer-to-Peer Networking," IBM Systems Journal, 1987; 26(4):429-452.	
/J.P./	WL	Texas Instrument, "TMS 370 Microcontroller Family User's Guide," (1996), 873 pages	
/J.P./	WM	Texas Instruments TMS320C30 Digital Signal Processor product literature, SPRS032A (April 1996, Revised June 1997)	
/J.P./	WN	Texas Instruments TMS34010 Graphics System Processor product literature	
/J.P./	WO	The Ring Oscillator VCO Schematic, 1 page.	
/J.P./	WP	THORNTON, J. E., "Considerations in Computer Design Leading Up To the Control Data 6600," Control Data Chippewa Laboratory (1970).	
/J.P./	WQ	THORNTON, J. E., "Design of a Computer, The Control Data 6600," published by Advanced Design Laboratory (1970).	
/J.P./	WR	Toshiba TLCS-42, 47, 470 User's Manual Published in April 1986	

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/J.P./	WS	UNGAR et al., "Architecture of SOAR: Smalltalk on a RISC," Proceedings of the 11th Annual International Symposium on Computer Architecture ISCA '84. ACM Press, New York, NY, pages 188-197 (1984).	
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/J.P./	WU	VAX 8800 System Technical Description Vol. 2, EK-KA88I-TD-PRE, Section 6, Instruction Box (IBOX), Preliminary Edition (July 1986)	
/J.P./	WV	VAX Maintenance Handbook: VAX-11/780, EK-VAXV2-HB-002, 1983 Edition	
/J.P./	WW	VL86C010 RISC Family Data Manual , Application Specific Logic Product Division, 1987	
/J.P./	WX	WATERS et al., "AIX Usability Enhancements and Human Factors," IBM Systems Journal, 1987; 26(4):383-394.	
/J.P./	WY	Whitby-Strevens, The transputer, Proceedings of the 12th annual international symposium on Computer architecture, p.292-300, June 17-19, 1985, Boston, Massachusetts, United States	
/J.P./	WZ	WHITEBY-Streven, "Transputer Technical Notes from INMOS," Google Groups; comp.sys.transputer, dated September 7, 1988.	
/J.P./	XA	WILLIAMS, "Chip Set Tackles Laptop Design Issues, Offers Flat-Panel VGA Control," Computer Design, October 15, 1988; 27(19):21-22	
/J.P./	XL	AGRAWAL, "Bipolar ECL Implementation," The SPARC Technical Papers, Catanzaro, eds., Springer-Verlag, NY, pp. 201-211. (1991)	

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/J.P./	XM	GILL et al. Summary of MIPS Instruction. CSL Technical Note No. 237, Computer Systems Laboratory, Stanford University, November 1983. 50 pages total.	
/J.P./	XN	HENNESSY et al., "Design of a High Performance VSL Processor, " Third Caltech Conference on Very Large Scale Integration," Bryant eds., California Institute of Technology, Computer Science Press, pp. 33-54. (1983)	
/J.P./	XO	HOROWITZ et al., "A 32b Microprocessor with On-Chip 2Kbyte Instruction Cache," IEEE International Solid State Circuits Conference, pp. 30, 31 and 328 (1987)	
/J.P./	XP	KNAPP, "Frequency Stability Analysis of Transistorized Crystal Oscillator," IEEE Transactions on Instrumentation and Measurement, Vol. 12, No. 1, pp. 2-5. (June 1963)	
/J.P./	XQ	NICOUD et al., "The Transputer Instruction Set," IEEE Micro, Vol. 9, No. 3, pp. 60-75 (May 1989)	
/J.P./	XR	PARASURAMAN, "High Performance Microprocessor Architectures," Proceedings of the IEEE, Vol. 64, No. 6, pp. 851-859. (June 1976)	
/J.P./	XS	PROEBSTING et al., "A TTL Compatible 4096-Bit N-Channel RAM," IEEE International Solid State Circuits Conference, Volume: XVI, pp. 28-29 (February 1973)	
/J.P./	XT	SCHOEFFLER, "Microprocessor Architecture," IEEE Transactions on Industrial Electronics and Control Instrumentation, Volume IECI-22, Issue 3, pp. 256-272. (August 1975)	
/J.P./	XU	WALLS et al., "A Frequency-Lock System for Improved Quartz Crystal Oscillator Performance," IEEE Transactions on Instrumentation and Measurement, Vol. IM-27, No. 3, pp. 249-252 (September 1978)	

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Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
90/009,034, 90/009,389, 90/010,520	5440749
Examiner	**Art Unit**
JOSEPH R. POKRZYWA	3992

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date
Final	Original	11/13/09
	(1)	✓
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	3	✓
	4	✓
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	(8)	✓
	(9)	✓
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Claim		Date
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Search Notes

Application/Control No.	Applicant(s)/Patent under Reexamination	
90/009,034, 90/009,389, 90/010,526	5440749	
Examiner	**Art Unit**	
JOSEPH R. POKRZYWA	3992	

SEARCHED			
Class	Subclass	Date	Examiner

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
reviewed prosecution history	11/2/2009	J.P.