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EXAMINER	
ART UNIT	PAPER NUMBER

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Please find below and/or attached an Office communication concerning this application or proceeding.

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CENTRAL REEXAMINATION UNIT

EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/009,388*.

PATENT NO. *5530890*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Office Action in Ex Parte Reexamination	Control No. 90/009,388	Patent Under Reexamination 5530890	
	Examiner JOSEPH R. POKRZYWA	Art Unit 3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

a☒ Responsive to the communication(s) filed on *05 January 2010*. b☒ This action is made FINAL.
c☐ A statement under 37 CFR 1.530 has not been received from the patent owner.

A shortened statutory period for response to this action is set to expire *2* month(s) from the mailing date of this letter. Failure to respond within the period for response will result in termination of the proceeding and issuance of an *ex parte* reexamination certificate in accordance with this action. 37 CFR 1.550(d). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).** If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☐ Information Disclosure Statement, PTO/SB/08.
3. ☐ Interview Summary, PTO-474.
4. ☐ _____.

Part II SUMMARY OF ACTION

1a. ☒ Claims *1-10* are subject to reexamination.
1b. ☐ Claims _____ are not subject to reexamination.
2. ☐ Claims _____ have been canceled in the present reexamination proceeding.
3. ☐ Claims *9 and 10* are patentable and/or confirmed.
4. ☐ Claims *1-8* are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ The drawings, filed on _____ are acceptable.
7. ☐ The proposed drawing correction, filed on _____ has been (7a)☐ approved (7b)☐ disapproved.
8. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
   a)☐ All b)☐ Some* c)☐ None of the certified copies have
   1☐ been received.
   2☐ not been received.
   3☐ been filed in Application No. _____.
   4☐ been filed in reexamination Control No. _____.
   5☐ been received by the International Bureau in PCT application No. _____.
   * See the attached detailed Office action for a list of the certified copies not received.
9. ☐ Since the proceeding appears to be in condition for issuance of an *ex parte* reexamination certificate except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte* Quayle, 1935 C.D. 11, 453 O.G. 213.
10. ☐ Other: _____

cc: Requester (if third party requester)

DETAILED ACTION

Response to Request for Reconsideration

1. The Patent Owner's response was received on 1/5/2010, and has been entered and made of record. Currently, claims 1-10 of U.S. Patent Number 5,530,890 (hereafter "the '890 Patent") are pending.

2. Original claims 1-10 issued in the '890 Patent on Jun. 25, 1996. On 1/16/2009, the Third Party requested *ex parte* reexamination of claims 1-10 of the '890 Patent, whereby an order for reexamination of claims 1-10 was mailed on 4/8/2009. The Patent Owner's current response dated 1/5/2010 was received in response to the first non-final Office action dated 11/5/2009. In the Office action dated 11/5/2009, claims 1-8 of the '890 Patent were rejected, and claims 9 and 10 of the '890 Patent were indicated as being patentable, whereby the examiner notes that claim 1 is the only independent claim of the '890 Patent.

Claim Rejections - 35 USC § 102

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. **Claims 1-6** are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Number 4,989,113, issued to Hull, Jr. *et al.* (hereafter "Hull, Jr.").

Regarding ***claim 1***, Hull Jr. discloses a microprocessor [see Abstract], which comprises

a main central processing unit [CPU 12 and controller 14] and a separate direct memory access central processing unit [DMA control 22] in a single integrated circuit comprising said microprocessor [see Fig. 1],

said main central processing unit [CPU 12 and controller 14] having an arithmetic logic unit [see Fig. 2, ALU 48],

a first push down stack [data registers 50a through 50h, collectively referred to as registers 50] with a top item register [data register 50a] and a next item register [data register 50b], connected to provide inputs to said arithmetic logic unit [see Fig. 2; also see col. 8, lines 51-55],

an output of said arithmetic logic unit being connected to said top item register [see Fig. 2],

said top item register also being connected to provide inputs to an internal data bus [see col. 8, lines 51-55],

said internal data bus being bidirectionally connected to a loop counter [see col. 9, lines 54-67],

said loop counter being connected to a decrementer [see col. 9, lines 54-67, whereby "CPU 12 interprets the absence of a displacement signal as an increment or decrement the contents of register 54 used in repetitive operation."],

said internal data bus being bidirectionally connected to a stack pointer [see col. 16, lines 23-55, whereby the system utilizes a "pipelining" of the instruction codes], return stack pointer [see col. 9,lines 36-67], mode register [index registers 68a and 68b, se col. 10, lines 33-55] and instruction register [auxiliary register 54, see col. 9, lines 4-61],

said internal data bus being connected to a memory controller [controller 14, see Figs. 1 and 4],

to a Y register of a return push down stack [registers 68, see col. 10, line 33-col. 11, line 14],

an X register [register 205] and a program counter [program counter 92, see col. 16, line 22-col. 18, line 9],

said Y register, X register and program counter providing outputs to an internal address bus [see Figs. 1, 2, and 4],

said internal address bus providing inputs to said memory controller and to an incrementer [see col. 17, line 60-col. 18, line 9],

said incrementer being connected to said internal data bus [see col. 16, lines 38-55],

said direct memory access central processing unit [DMA control 22] providing inputs to said memory controller [controller 14, see Figs. 1 and 4, also see col. 18, lines 10-53],

said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory [see Fig. 1, RAMs 16 and 18].

Regarding ***claim 2***, Hull, Jr. discloses the microprocessor discussed above in claim 1, and further teaches that said memory controller includes a multiplexing means [interface ports 24 and 26] between said central processing unit and said address/data bus [see Figs. 1 and 3], said multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus [see col. 13, line 38-col. 14, line 46].

Regarding ***claim 3***, Hull, Jr. discloses the microprocessor discussed above in claim 1, and further teaches that said memory controller includes means for fetching instructions for said central processing unit on said address/data bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle [see col. 13, lines 26-37].

Regarding ***claim 4***, Hull, Jr. discloses the microprocessor discussed above in claim 3, and further teaches of means connected to said means for fetching instructions for determining if multiple instructions fetched by said means for fetching instructions require a memory access [see col. 13, lines 26-37], said means for fetching instructions fetching additional multiple instructions if the multiple instructions do not require a memory access [see col. 13, lines 26-37].

Regarding ***claim 5***, Hull, Jr. discloses the microprocessor discussed above in claim 3, and further teaches that said microprocessor and a dynamic random access memory are contained in a single integrated circuit [see Fig. 1] and said means for fetching instructions includes a column latch for receiving the multiple instructions [instruction cache 36, see Fig. 1; also see col. 5, line 41-col. 6, line 12].

Regarding ***claim 6***, Hull, Jr. discloses the microprocessor discussed above in claim 1, and further teaches that said microprocessor includes a sensing circuit and a driver circuit [interrupt logic 250], and an output enable line for connection between the random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level [see col. 18, lines 10-53], said microprocessor being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal [see col. 18, lines 10-53].

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. **Claims 1-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Number 4,758,948, issued to May *et al.* (hereafter "May'948"), which incorporates by reference the reference of U.S. Patent Number 4,680,698, issued to Edwards *et al.* (hereafter Edwards'698 Patent"), further in view of the "Transputer Reference Manual", published by Inmos Ltd., 1988 (hereafter the "Transputer Manual").

Regarding ***claim 1***, May'948 discloses a microprocessor [see Fig. 1], which comprises

a main central processing unit [CPU 12, see Figs. 1 and 2] and *a separate memory access processing unit* [external memory interface 23, seen in Fig. 1] in a single integrated circuit comprising said microprocessor [see Fig. 1],

said main central processing unit [CPU 12, see Figs. 1 and 2] having an arithmetic logic unit [see Fig. 2, ALU 30, also see col. 4, lines 52 and 53, wherein "The CPU 12 incorporates an arithmetic logic unit (ALU)..."],

a first push down stack [see Fig. 2, whereby the A, B and C registers 54, 55, and 56, respectively, within the Priority 1 register bank operate as a first push down stack] with a top item register [A register 54] and a next item register [B register 55], connected to provide inputs to said arithmetic logic unit [see col. 8, lines 47-56, wherein "The A, B, and C register stack 54, 55, and 56 are the sources and destinations for most arithmetic and logical operations. They are

organised as a stack so that the loading of a value into the A register is preceded by relocating the existing contents of the B register into the C register and from the A register into the B register. Similarly storing a value derived from the A register causes the contents of the B register to be moved into the A register and the contents of the C register into the B register."],

an output of said arithmetic logic unit being connected to said top item register [see Fig. 2, whereby the Z bus includes an output from the ALU 30 and an input to the A register 54],

said top item register also being connected to provide inputs to an internal data bus [see Fig. 2, whereby the data bus 31 is connected to the A register 54],

said internal data bus [data bus 31] being bidirectionally connected to a loop counter [being interpreted as the workspace pointer WPTR REG register 51 and the O REG register 57, seen in Fig. 3, whereby the Edwards'698 Patent states on cols. 15 and 16 within the procedure "load from workspace and increment (function code 3)", the purpose of the function includes "to facilitate the use of workspace locations as loop counters, incrementing towards zero", and includes the definition "WPTR + OREG := AREG + 1"],

said loop counter being connected to a decrementer [the Edwards'698 Patent states on cols. 15 and 16 within the procedure "load from workspace and increment (function code 3)", the purpose of the function includes "to facilitate the use of workspace locations as loop counters, incrementing towards zero", thereby effectively acting as a decrementer],

said internal data bus [data bus 31] being bidirectionally connected to a stack pointer [see Fig. 3 IPTR S 65, also see col. 9, lines 59-68, wherein "Location 65 is used

when a process is not the current process to hold a pointer (IPTR) to the next instruction to be executed by the process when it becomes the current process."], return stack pointer [see Fig. 3, LINK S 66, also see col. 9, lines 59-68, wherein "Location 66 is used to store a workspace pointer of a next process on a link list or queue of processes awaiting execution."], mode register [see Fig. 3, STATE S 67, also see col. 9, lines 59-68, wherein "Location 67 is normally used to contain an indication of the state of a process performing an alternative input operation or as a pointer for copying of a block of data."; additionally see col. 7, line 69-col. 8, line 7, wherein "PRI FLAG" is a "1 bit register or flag 47 for indicating the priority 0 or 1 of the currently executing process."] and instruction register [IB Reg 34, also see col. 7, lines 29-31, wherein "Each instruction derived from the program sequence for the process is fed to an instruction buffer 34."],

said internal data bus being connected to a memory controller [memory interface 14],

to a Y register of a return push down stack [BPTR REG 52, see Figs. 2 and 4],

an X register [FPTR REG 53, see Figs. 2 and 4] and a program counter [byte counter 111, see Fig. 12],

said Y register, X register and program counter providing outputs to an internal address bus [Z bus 81, see Figs. 2, 12, and 13],

said internal address bus providing inputs to said memory controller and to an incrementer [see col. 12, lines 35-54, wherein "the pointer register 122 incorporates an incrementor so that as each byte is received the pointer increments to the memory destination address for the next byte of the input message."; also see Fig. 13],

said incrementer being connected to said internal data bus [see Fig. 13],

s*aid memory access processing unit* [external memory interface 23, seen in Fig. 1] providing inputs to said memory controller [see Fig. 1 and 2, whereby external memory interface 23 provides inputs to the memory interface 14],

said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory [see Fig. 10, whereby memory interface 14 has an address/data bus 33 and 31, and also a plurality if control lines providing input to RAM, see Fig. 1].

However, the May'948 Patent does not expressly state if the *separate memory access processing unit* is a separate direct memory access central processing unit being in a single IC with the main central processing unit, and subsequently, if said direct memory access central processing unit provides inputs to said memory controller.

The Transputer Manual discloses a microprocessor [see Figure 1.1 on page 108], which comprises

a main central processing unit [32 bit Processor, see Figure 1.1 on page 108] and a separate direct memory access central processing unit [see page 150, wherein "DMA may also inhibit an internally running program from accessing external memory....DMA allows a bootstrap program to be loaded into external RAM ready for execution after reset."; also see pages 132-151, which shows various configurations of the EMI] in a single integrated circuit

comprising said microprocessor [see page 150, whereby the External Memory Interface allows for the programmed control of direct memory access; see Figure 1.1 on page 108],

said main central processing unit having a first push down stack [the A, B, and C registers, seen in Figs. 3.1 and 3.3; also see page 11, wherein "The A, B and C registers which form an evaluation stack."] with a top item register [Register A] and a next item register [B register], connected to provide inputs to said arithmetic logic unit [see page 111, wherein A, B, and C are sources and destinations for most arithmetic and logical operations. Loading a value into the stack pushes B into C, and A into B, before loading A."],

an internal data bus being bidirectionally connected to a loop counter [see page 115, wherein "This uses a workspace locator as a counter of the parallel construct components which have still to terminate. The counter is initialized to the number of components before the process is started. Each component ends with an end process instruction which decrements and tests the counter. For all but the last component, the counter is non-zero and the component is descheduled. For the last component, the counter is zero, and the main process continues."],

said loop counter being connected to a decrementer [see page 115],

said direct memory access central processing unit [being the External Memory Interface, seen in Fig. 1.1 on page 108] providing inputs to said memory controller [see page 108, whereby the External Memory Interface provides an input to the 32-bit Processor],

said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory [see Fig. 1.1 on page 108].

The May'948 Patent & the Transputer Manual are combinable because they are from the same field of endeavor, both being drawn to an Inmos Transputer microprocessor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the DMA teachings described in the Transputer Manual within the system described the May'948 Patent. The suggestion/motivation for doing so would have been that the system described in the May'948 Patent would be easily adapted to incorporate the direct memory access controller teachings described in the Transputer Manual, as the components and systems appear to be identical. Therefore, it would have been obvious to combine the teachings of the Transputer Manual with the system of the May'948 Patent to obtain the invention as specified in claim 1.

Regarding ***claim 2***, the May'948 Patent and the Transputer Manual disclose the microprocessor discussed above in claim 1, and the May'948 Patent further teaches that said memory controller includes a multiplexing means [condition multiplexor 36, seen in Fig. 2] between said central processing unit and said address/data bus [see Fig. 2], said multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus [see col. 7, lines 32-35]. Additionally, the Transputer Manual further teaches of including a multiplexing means [see Fig. 7.8 on page 140, Row/Column address multiplexer], with said multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus [see Fig. 7.8 on page 140, Row/Column address multiplexer].

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the multiplexer teachings described in the Transputer Manual within the system described the May'948 Patent. The suggestion/motivation for doing so would have been that the system described in the May'948 Patent would be easily adapted to incorporate the further teachings described in the Transputer Manual, as the components and systems appear to be identical. Therefore, it would have been obvious to combine the further teachings of the Transputer Manual with the system of the May'948 Patent to obtain the invention as specified in claim 2.

Regarding ***claim 3***, the May'948 Patent and the Transputer Manual disclose the microprocessor discussed above in claim 1, and the May'948 Patent further teaches that said memory controller includes means for fetching instructions for said central processing unit on said address/data bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle [see col. 6, lines 4-24; also see col. 7, lines 15-39].

Regarding ***claim 4***, the May'948 Patent and the Transputer Manual disclose the microprocessor discussed above in claim 3, and the May'948 Patent further teaches of means connected to said means for fetching instructions for determining if multiple instructions fetched by said means for fetching instructions require a memory access [see col. 6, lines 4-24; also see col. 7, lines 15-39], said means for fetching instructions fetching additional multiple instructions

if the multiple instructions do not require a memory access [see col. 6, lines 4-24; also see col. 7, lines 15-39].

7. **Claims 7 and 8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hull, Jr. in view of Kato *et al.* (U.S. Patent Number 4,766,567, hereafter "Kato").

Regarding ***claim 7***, Hull, Jr. discloses the microprocessor discussed above in claim 1, and further teaches of **a system clock** to said main central processing unit, said main central processing unit and **said system clock** being provided in a single integrated circuit [see Figs. 1 and 4, being clock generator 200, seen in Fig. 4, and read in col. 15, lines 7-27].

However, Hull, Jr. does not expressly describe the system clock as being a ring oscillator variable speed system clock connected to said main central processing unit, with the main central processing unit and the ring oscillator variable speed system clock being provided in a single integrated circuit.

Kato discloses a microprocessor having a ring oscillator variable speed system clock connected to said main central processing unit, said main central processing unit and said ring oscillator variable speed system clock being provided in a single integrated circuit [clock generator 4, see Figs. 1 and 4; also see col. 10, line 51-col. 11, line 7].

Hull, Jr. & Kato are combinable because they are from the same field of endeavor, being semiconductor systems having two distinct clock generators. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the ring oscillator teachings of Kato in the system taught by Hull, Jr. The suggestion/motivation for doing so would have been that the clock generator of Hull, Jr. would become more efficient, as using a ring oscillator would lower output frequency in proportion to the speed of the data processing circuit which is also lowered due to the drop of power supply voltage, being a characteristic of using a ring oscillator recognized by Kato on col. 11, lines 2-7. Therefore, it would have been obvious to combine the ring oscillator teachings of Kato with the system of Hull, Jr. to obtain the invention as specified in claim 7.

Regarding ***claim 8***, Hull, Jr. and Kato disclose the microprocessor discussed above in claim 7, and Hull, Jr. further teaches that said memory controller includes an input/output interface connected to exchange coupling control signals, addresses and data with said main central processing unit [see Fig. 1], said microprocessor additionally including a second clock independent [timer 40] of said ring oscillator variable speed system clock connected to said input/output interface [whereby timer 40 is independent of clock generator 200, seen in Figs. 1 and 4].

Response to Arguments

8. Patent Owner's arguments filed 1/5/2010 have been fully considered but they are not persuasive.

9. In response to the Patent Owner's argument regarding the rejection of claims 1-6 under 35 U.S.C. 102(e) as being anticipated by the Hull, Jr. reference, the Patent Owner argues on page 2 that the Hull reference fails to expressly disclose "a first push down stack...to provide inputs to said arithmetic logic unit". The examiner notes that claim 1, being the only independent claim, currently requires that "said main processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus..." Thus, independent claim 1 requires the various connections of the various components, as the claim defines a structure of the components.

10. With this, as seen in Fig. 2, Hull shows a stack of registers 50. Continuing, in col. 7, lines 55-66, Hull states "data registers 50a through 50h (collectively referred to as data registers 50)..." Further, on col. 8, lines 47-55, Hull states "The primary function of data registers 50 is an accumulator function, so that the plurality of data registers 50 in effect provides CPU 12 with multiple accumulators." Therefore, the stack of registers 50, having a top item register 50a, and a next item register 50b, can be reasonably and broadly interpreted as "a first push down stack".

11. In this regard, MPEP 2111 [R-5], states, in part:

> During patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification." >The Federal Circuit's en banc decision in *Phillips v. AWH Corp.*, 415 F.3d 1303, 75 USPQ2d 1321 (Fed. Cir. 2005) expressly recognized that the USPTO employs the "broadest reasonable interpretation" standard:
>
> > The Patent and Trademark Office ("PTO") determines the scope of claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." In re Am. Acad. of Sci. Tech. Ctr., 367 F.3d 1359, 1364[, 70 USPQ2d 1827] (Fed. Cir. 2004). Indeed, the rules of the PTO require that application claims must "conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description." 37 CFR 1.75(d)(1).

12. With this, in the reference of Hull, the stack of registers 50, seen in Fig. 2, having a top item register 50a, and a next item register 50b, as discussed on col. 7, lines 55-66, can be broadly, and reasonably interpreted as "a first push down stack", being an interpretation that is consistent with the specification of the '890 Patent, as in the specification of the '890 Patent, particularly seen in Fig. 2, a top of stack register 76 and a next item register 78, being referred to as a "push down stack", are connected to an ALU 80.

13. Further, on page 3, the Patent Owner states that "Hull provides no indication that registers 50 operate as top and next item registers (as required by Claim 1) associated with stack elements located in memory as described, for example, in US'890's Fig. 21". However, the

examiner notes that claim 1 does not require any specific "operation" of the "top item register" and "next item register", nor of the "push down stack". Particularly, the current claim language requires a structure, and does not specify any function of the "first push down stack", the "top item register", or the "next item register", whereby claim 1 requires "said main processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, ...an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus..." There is no requirement of any operation performed by the "top item register" and the "next item register". Because the structure of Hull's stack of registers appears to be equivalent, and consistent to the stack of registers in Fig. 2 of the '890 Patent, as noted above, the limitation is seen to be reasonably interpreted by Hull. Therefore, Hull is seen as teaching of "said main processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus..."

14. Continuing, on page 3, the Patent Owner argues that the Hull reference fails to teach of a "stack pointer", as the Patent Owner argues that the program counter 92 of Hull, "is not a stack pointer". Claim 1 currently states "...said internal data bus being bidirectionally connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register,..." With this, the examiner notes that the current claim language does not require any specific operations or functionality of "a stack

pointer", and only requires that an internal data bus be bidirectionally connected to a stack pointer. There is no specific requirement that a "stack pointer" is associated with the "first push down stack", or if the "stack pointer" points "to a top of a data stack", as argued by the Patent Owner. If the Patent Owner wishes that these features be considered in interpreting the current claim language, then the claim must be amended accordingly.

15. Further, Hull states on col. 18, lines 46-53, "As is well known in the art for such an operation, controller 14 will cause the prior contents of program counter 92 to be stored in a predetermined memory location (generally called a "stack"), so that the location of the instruction code which would have been fetched next will be reloaded after the interrupt has been serviced." Additionally, as read in col. 10, lines 8-32, Hull states "instruction codes...including those listed in Table 1... "add" specifies the memory location to be addressed, "Arn" specifies the contents of one of registers 54, and "disp" the value of displacement code generated by controller 14. The updated value of the contents of one of auxiliary registers 54 is denoted by "ARn'" in Table 1." Thus, with this, the instruction codes appear to point to contents in a register stack. Further, as seen in Figs. 4 and 1 of Hull, the lines leading to the internal bus 34a from the program counter 92 are seen to be bidirectional. Therefore, Hull is seen to teach of "said internal data bus being bidirectionally connected to a stack pointer", as currently required in claim 1.

16. Therefore, the rejection of claims 1-6, as cited in the Office action dated 11/5/2009, under 35 U.S.C. 102(e) as being anticipated by Hull, is maintained and repeated in this Office action.

17. Continuing, with respect to the rejection of claims 1-4 under 35 USC 103(a) as being unpatentable over May'948, which incorporates by reference Edwards '698, and further in view of the Transputer Manual, whereby on page 5, the Patent Owner argues that "none of the Transputer references, from May'948 to the Transputer Manuals, disclose a stack pointer associated with registers A, B and C, which the office action has identified as the 'first push down stack.'". Further, the Patent Owner argues that because of the internal connection of the A, B, and C register stack, the A, B, C register stack would not need a stack pointer.

18. However, the examiner notes that currently claim 1 requires "...said internal data bus being bidirectionally connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register,..." With this, there is no requirement that the "stack pointer" be associated with the push down stack, as argued by the Patent Owner, only that an internal data bus is "bidirectionally connected to a stack pointer". If the Patent Owner desires that feature that the stack pointer expressly points to the first push down stack to be considered in interpreting the current claim language, then the claim must be amended accordingly.

19. Further, the examiner notes that MPEP 2111, as noted above, requires that "During patent examination, the pending claims must be 'given their broadest reasonable interpretation consistent with the specification.'" With this, in reviewing the reference of May '948, as stated in col. 35, lines 12-32, May '948 states "The instruction pointer (IPTR) of any process in the list is stored in the IPTR location 65 of its workspace as shown in FIG. 3." Continuing, in viewing

Fig. 2, May '948 illustrates the IPTR 50 is shown as being bidirectionally connected to the stack registers A, B, and C. With this, the instruction pointer IPTR of May '948 can be seen as pointing to the stack of the A, B, and C registers. This is also described in May '948 on col. 27, lines 36-42.

20. Continuing, on page 6, the Patent Owner argues that the IPTR 65 "contains the address of an instruction, not the address of the top of a data stack." With this the examiner notes that nowhere does the current claim language expressly require that the stack pointer includes "the address of the top of a data stack". If the Patent Owner wishes that this feature be considered in interpreting the current claim language, then the claim must be amended accordingly.
With this, the May '948 reference discloses the IPTR S 65 as a pointer to a register stack, therein being considered as a "stack pointer", whereby in col. 9, lines 59-68 "Location 65 is used when a process is not the current process to fold a pointer (IPTR) to the next instruction to be executed by the process when it becomes the current process".

21. Therefore, the rejection of claims 1-4, as cited in the Office action dated 11/5/2009, under 35 U.S.C. 103(a) as being unpatentable over May '948, expressly incorporating Edwards ''698 Patent, further in view of the Transputer Manual, is maintained and repeated in this Office action.

STATEMENT OF REASONS FOR PATENTABILITY AND/OR CONFIRMATION

The following is an examiner's statement of reasons for patentability and/or confirmation of the claims found patentable in this reexamination proceeding:

Claims 9 and 10 are confirmed as patentable.

Regarding dependent ***claim 9***, the examiner does believe that the prior art of record expressly discloses the invention as claimed, particularly including the feature requiring the first push down stack has a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit. The prior art of Hull, Jr. teaches of stack elements, as seen in Fig. 2. However, Hull, Jr. fails to expressly teach of a third stack element configured as a RAM external to the single integrated circuit. Further, the reference of Muller (U.S. Patent 4,969,091), noted in the Request for Reexamination, teaches of implementing a push down stack. But, Muller fails to expressly teach the architecture that is required by the claim language, which requires a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit. Thus,

the prior art of record is not seen to expressly disclose this architecture. Therefore, in the examiner's opinion, the claim is deemed patentable.

Any comments considered necessary by PATENT OWNER regarding the above statement must be submitted promptly to avoid processing delays. Such submission by the patent owner should be labeled: "Comments on Statement of Reasons for Patentability and/or Confirmation" and will be placed in the reexamination file.

Conclusion

22. The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent No. 5,530,890 throughout the course of this reexamination proceeding.

23. **THIS ACTION IS MADE FINAL.**

A shortened statutory period for response to this action is set to expire TWO MONTHS from the mailing date of this action.

Extensions of time under 37 CFR 1.136(a) do not apply in reexamination proceedings. The provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Further, in 35 U.S.C. 305 and in 37 CFR 1.550(a), it is required that reexamination proceedings "will be conducted with special dispatch within the Office."

Extensions of time in reexamination proceedings are provided for in 37 CFR 1.550(c). A request for extension of time must be filed on or before the day on which a response to this action is due, and it must be accompanied by the petition fee set forth in 37 CFR 1.17(g). The mere filing of a request will not effect any extension of time. An extension of time will be granted only for sufficient cause, and for a reasonable time specified.

The filing of a timely first response to this final rejection will be construed as including a request to extend the shortened statutory period for an additional month, which will be granted even if previous extensions have been granted. In no event however, will the statutory period for response expire later than SIX MONTHS from the mailing date of the final action. See MPEP § 2265.

24. ALL correspondence relating to this ex parte reexamination proceeding should be directed as follows:

Please mail any communications to:

Attn: Mail Stop "Ex Parte Reexam"
Central Reexamination Unit
Commissioner for Patents
P. O. Box 1450
Alexandria VA 22313-1450

Please FAX any communications to:

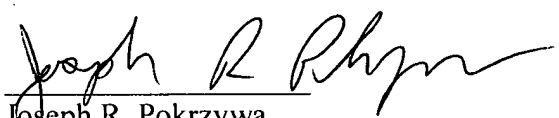
(571) 273-9900
Central Reexamination Unit

Please hand-deliver any communications to:

Customer Service Window
Attn: Central Reexamination Unit
Randolph Building, Lobby Level
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

Signed:



Joseph R. Pokrzywa
Primary Examiner
Central Reexamination Unit 3992
(571) 272-7410

Conferees: /r.g.f./
ESK

Index of Claims

Application/Control No.	Applicant(s)/Patent under Reexamination
90/009,388	5530890
Examiner	**Art Unit**
JOSEPH R. POKRZYWA	3992

√	Rejected	–	(Through numeral) Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

Claim		Date									
Final	Original	10/5/09	4/21/10								
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	2	✓	✓								
	3	✓	✓								
	4	✓	✓								
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	6	✓	✓								
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