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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/009,388	01/16/2009	5530890	0081-011D1X1	7136

40972 7590 11/03/2010

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EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 11/03/2010

Please find below and/or attached an Office communication concerning this application or proceeding.

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CENTRAL REEXAMINATION UNIT

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EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/009,388*.

PATENT NO. *5530890*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Notice of Intent to Issue Ex Parte Reexamination Certificate	Control No.	Patent Under Reexamination	
	90/009,388	5530890	
	Examiner	Art Unit	
	JOSEPH R. POKRZYWA	3992	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ Prosecution on the merits is (or remains) closed in this *ex parte* reexamination proceeding. This proceeding is subject to reopening at the initiative of the Office or upon petition. *Cf.* 37 CFR 1.313(a). A Certificate will be issued in view of
   - (a) ☐ Patent owner's communication(s) filed: _____.
   - (b) ☐ Patent owner's late response filed: _____.
   - (c) ☐ Patent owner's failure to file an appropriate response to the Office action mailed: _____.
   - (d) ☐ Patent owner's failure to timely file an Appeal Brief (37 CFR 41.31).
   - (e) ☒ Other: *Telephone Interview dated 9/22/2010*.

   Status of *Ex Parte* Reexamination:
   - (f) Change in the Specification: ☐ Yes ☒ No
   - (g) Change in the Drawing(s): ☐ Yes ☒ No
   - (h) Status of the Claim(s):
     - (1) Patent claim(s) confirmed: *5-10*.
     - (2) Patent claim(s) amended (including dependent on amended claim(s)): _____
     - (3) Patent claim(s) canceled: *1-4*.
     - (4) Newly presented claim(s) patentable: 11-20.
     - (5) Newly presented canceled claims: _____.
     - (6) Patent claim(s) ☐ previously ☐ currently disclaimed: _____
     - (7) Patent claim(s) not subject to reexamination: _____.

2. ☒ Note the attached statement of reasons for patentability and/or confirmation. Any comments considered necessary by patent owner regarding reasons for patentability and/or confirmation must be submitted promptly to avoid processing delays. Such submission(s) should be labeled: "Comments On Statement of Reasons for Patentability and/or Confirmation."

3. ☐ Note attached NOTICE OF REFERENCES CITED (PTO-892).

4. ☒ Note attached LIST OF REFERENCES CITED (PTO/SB/08 or PTO/SB/08 substitute).

5. ☐ The drawing correction request filed on _____ is: ☐ approved ☐ disapproved.

6. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
   a)☐ All b)☐ Some* c)☐ None of the certified copies have
   - ☐ been received.
   - ☐ not been received.
   - ☐ been filed in Application No. _____.
   - ☐ been filed in reexamination Control No. _____.
   - ☐ been received by the International Bureau in PCT Application No. _____.

   * Certified copies not received: _____.

7. ☒ Note attached Examiner's Amendment.

8. ☐ Note attached Interview Summary (PTO-474).

9. ☐ Other: _____.

cc: Requester (if third party requester)

DETAILED ACTION

Response to Telephone Interview

1. The Patent Owner authorized an Examiner's Amendment, appearing below, which cancels claims 1-4, being the current claims that stand rejected in the Final Office action dated 4/29/2010, and discussed in the Advisory Action dated 8/12/2010.

Summary of Issues

2. Briefly, original claims 1-10 of U.S. Patent Number 5,530,890 (hereafter "the '890 Patent") issued on June 25, 1996. In the after-final amendment dated 6/29/2010, which has been entered, and made of record, the Patent Owner added claims 11-20, whereby new independent claim 11 adds the limitation of "said stack pointer pointing into said first push down stack" to the text of what appears in original claim 1, and new dependent claims 12-20 directly correspond to original dependent claims 2-10. Thus, presently, the current pending claims of the '890 Patent are claims 1-20.

Examiner's Amendment

3. An examiner's amendment to the record appears below. The changes made by this examiner's amendment will be reflected in the reexamination certificate to issue in due course.

Claims 1-4 are cancelled.

STATEMENT OF REASONS FOR PATENTABILITY AND/OR CONFIRMATION

The following is an examiner's statement of reasons for patentability and/or confirmation of the claims found patentable in this reexamination proceeding:

Claims 5-10 are confirmed as patentable.

Claims 11-20 are deemed as patentable.

Regarding dependent ***claim 5***, in the examiner's opinion, it would not have been obvious to have the claimed microprocessor include the features of "the microprocessor and a dynamic random access memory contained in a single integrated circuit and said means for fetching instructions includes a column latch for receiving the multiple instructions", combined with the features of "a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register,..." The closest prior art, being the references of Hull, Jr. and May'948 are not seen to expressly describe these features. Particularly, May'948 fails to expressly disclose "the microprocessor and a dynamic random access memory contained in a single integrated circuit and said means for fetching instructions includes a column latch for receiving the multiple instructions". Further, as previously described in the Advisory Office action dated 8/12/2010, the Hull, Jr. reference is unclear of teaching of a "first push down stack with a top item and a next item register". With this, while the Hull, Jr. reference does describe a dynamic random access memory, the examiner is unclear of any motivation to utilize the various teachings in the Hull, Jr. system in the combination of May'948, Edwards'698 and the

Transputer Reference Manual. With this, there appears to be no clear teaching of the combination of these features in the prior art of record. Therefore, claim 5 is rendered patentable.

Regarding ***claim 6***, in the examiner's opinion, it would not have been obvious at the time of the invention to have the claimed microprocessor include "a sensing circuit and a driver circuit and an output enable line for connection between the random access memory, said sensing circuit, and said driver, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level", combined with the features of "a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register,..." The closest prior art, being the references of Hull, Jr. and May'948 are not seen to expressly describe these features. Particularly, May'948 fails to expressly disclose "a sensing circuit and a driver circuit and an output enable line for connection between the random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level". Further, as previously described in the Advisory Office action dated 8/12/2010, the Hull, Jr. reference is unclear of teaching of a "first push down stack with a top item and a next item register". With this, while the Hull, Jr. reference does describe a sensing circuit, the examiner is unclear of any motivation to utilize the various teachings in the Hull, Jr. system in the combination of May'948, Edwards'698 and the Transputer Reference

Manual. With this, there appears to be no clear teaching of the combination of these features in the prior art of record. Therefore, claim 6 is rendered patentable.

Regarding ***claim 7***, in the examiner's opinion, it would not have been obvious to one of ordinary skill in the art to have the microprocessor additionally comprising the features of "a ring oscillator variable speed system clock connected to said main central processing unit, said main central processing unit and said ring oscillator variable speed system clock being provided in a single integrated circuit", combined with the features of "a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register,..." The closest prior art, being the references of Hull, Jr. and May'948 are not seen to expressly describe any ring oscillator variable speed system clock. The reference of Kato is seen to describe using a ring oscillator, but the examiner is unclear of any motivation to utilize the various teachings in the Kato reference in the combination of May'948, Edwards'698 and the Transputer Reference Manual. With this, there appears to be no clear teaching of the combination of these features in the prior art of record. Therefore, claim 7 is rendered patentable.

Regarding ***claim 9***, the examiner does believe that the prior art of record expressly discloses the invention as claimed, particularly including the feature requiring the first push down stack has a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit. The prior art of Hull, Jr. teaches of stack elements, as seen in Fig. 2. However, Hull, Jr. fails to expressly teach of a third stack element configured as a RAM external to the single integrated circuit. Further, the reference of Muller (U.S. Patent 4,969,091), noted in the Request for Reexamination, teaches of implementing a push down stack. But, Muller fails to expressly teach the architecture that is required by the claim language, which requires a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit. Thus, the prior art of record is not seen to expressly disclose this architecture. Therefore, in the examiner's opinion, claim 9 is deemed patentable.

Regarding ***claim 11***, in the examiner's opinion, it would not have been obvious to one of ordinary skill in the art to have the microprocessor additionally comprising the features of "a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit,...said internal bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register, said stack pointer pointing into said first push down stack,..." The closest prior art of record, being the May'948 reference does teach of using a push down stack. However, the May'948 reference does not expressly describe a stack pointer that points "into said first push down stack". With this feature, which was added in the Patent Owner's amendment dated 6/29/2010, claim 11 is deemed patentable.

Any comments considered necessary by PATENT OWNER regarding the above statement must be submitted promptly to avoid processing delays. Such submission by the patent owner should be labeled: "Comments on Statement of Reasons for Patentability and/or Confirmation" and will be placed in the reexamination file.

Conclusion

4. **All** correspondence relating to this ex parte reexamination proceeding should be directed:

By Mail to: Mail Stop *Ex Parte* Reexam
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

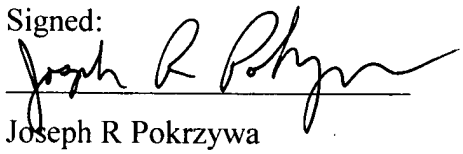
By FAX to: (571) 273-9900
Central Reexamination Unit

By hand: Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Registered users of EFS-Web may alternatively submit such correspondence via the electronic filing system EFS-Web, at https://sportal.uspto.gov/authenticate/authenticateuserlocalepf.html. EFS-Web offers the benefit of quick submission to the particular area of the Office that needs to act on the correspondence. Also, EFS-Web submissions are "soft scanned" (i.e., electronically uploaded) directly into the official file for the reexamination proceeding, which offers parties the opportunity to review the content of their submissions after the "soft scanning" process is complete.

Any inquiry concerning this communication should be directed to Joseph R. Pokrzywa at telephone number 571-272-7410.

Signed:



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Conferees: /r.g.f./
ESK