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| 90/009,388 | 01/16/2009 | 5530890 | 0081-011D1X1 | 7136 |

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| EXAMINER | |
|---|---|
| ART UNIT | PAPER NUMBER |

DATE MAILED: 11/05/2009

Please find below and/or attached an Office communication concerning this application or proceeding.

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CENTRAL REEXAMINATION UNIT

# *EX PARTE* REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/009,388*.

PATENT NO. *5530890*.

ART UNIT *3992*.

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

| Office Action in Ex Parte Reexamination | Control No. 90/009,388 | Patent Under Reexamination 5530890 | |
|---|---|---|---|
| | Examiner JOSEPH R. POKRZYWA | Art Unit 3992 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

a☐ Responsive to the communication(s) filed on _____ . b☐ This action is made FINAL.
c☐ A statement under 37 CFR 1.530 has not been received from the patent owner.

A shortened statutory period for response to this action is set to expire 2 month(s) from the mailing date of this letter. Failure to respond within the period for response will result in termination of the proceeding and issuance of an *ex parte* reexamination certificate in accordance with this action. 37 CFR 1.550(d). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).** If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☐ Information Disclosure Statement, PTO/SB/08.
3. ☐ Interview Summary, PTO-474.
4. ☐ _____.

Part II SUMMARY OF ACTION

1a. ☒ Claims 1-10 are subject to reexamination.
1b. ☐ Claims _____ are not subject to reexamination.
2. ☐ Claims _____ have been canceled in the present reexamination proceeding.
3. ☒ Claims 9 and 10 are patentable and/or confirmed.
4. ☒ Claims 1-8 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ The drawings, filed on _____ are acceptable.
7. ☐ The proposed drawing correction, filed on _____ has been (7a)☐ approved (7b)☐ disapproved.
8. ☐ Acknowledgment is made of the priority claim under 35 U.S.C. § 119(a)-(d) or (f).
   a)☐ All b)☐ Some* c)☐ None of the certified copies have
   1☐ been received.
   2☐ not been received.
   3☐ been filed in Application No. _____ .
   4☐ been filed in reexamination Control No. _____.
   5☐ been received by the International Bureau in PCT application No. _____.
   * See the attached detailed Office action for a list of the certified copies not received.
9. ☐ Since the proceeding appears to be in condition for issuance of an *ex parte* reexamination certificate except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte* Quayle, 1935 C.D. 11, 453 O.G. 213.
10. ☐ Other: _____

cc: Requester (if third party requester)

## DETAILED ACTION

### *Brief Summary of Proceedings*

1. Claims 1-10 originally issued in U.S. Patent 5,530,890 (hereafter "the '890 Patent") on Jun. 25, 1996. On 1/16/2009, the Third Party requested *ex parte* reexamination of claims 1-10 of the '890 Patent. On 4/8/2009, an order for reexamination of claims 1-10 was mailed. The examiner notes that claim 1 is the only independent claim of the '890 Patent.

### *Discussion of Prior Art of Record*

2. The examiner notes that the Third Party Requester cites in the Request for Reexamination dated 1/16/2009 two main primary references, with the first being the article "The Motorola MC68020", authored by MacGregor *et al.*, and published in August 1984 (noted as "MacGregor"), and the second being U.S. Patent Number 4,758,948, issued to May *et al.* (noted herein as the "May'948 Patent"). However, both of these references are seen to fall short of teaching each of the limitations of the specific claimed architecture of independent claim 1 of the '890 Patent.

3. For instance, there is no specific disclosure in the MacGregor reference of a push down stack that "is connected to provide inputs to said arithmetic logic unit, an output of the ALU being connected to the top item register in the push down stack, with the top item register also

being connected to provide inputs to an internal data bus". The disclosure of MacGregor is unclear of teaching of the specific connections required in the current claim language. Thus, the reference by itself falls short of anticipating the claim language. Further, both the MacGregor reference and the May reference are unclear if the microprocessor comprises a main CPU and a separate DMA CPU in a single integrated circuit.

4. The specification of the '890 Patent describes this feature as being "another unusual aspect to the high performance microprocessor 50", and describes the on-chip RAM gives a performance equal to that obtained with the use of static RAMs, at a quarter of the cost. Thus, the examiner notes that this is believed to be a key feature in the invention claimed in the '890 Patent. The reference of MacGregor states on page 107 that "The reduced bus utilization by the MC68020 also increases system performance by providing more bus bandwidth for other masters such as DMA devices." However, with this statement, MacGregor does not specify and is not clear that a DMU CPU is included in a single integrated circuit as the main CPU within a microprocessor. Similarly, the reference of the May'948 Patent does not disclose of a DMA CPU being on the same integrated circuit as a main CPU. The Third Party Requester stated in the Request that "Onc skilled in the art would have understood that he May transputer system had a MEM REQUEST pin that was specifically configured to be coupled to a DMA controller." However, with this, there is still no specific disclosure within the May'948 Patent itself that expressly states of a DMA controller being on the same integrated circuit as a main CPU.

5. However, upon review of the references submitted in the Request for Reexamination, the examiner notes that the reference of the "Transputer Reference Manual", published by Inmos Ltd., 1988 (hereafter the "Transputer Manual"), is seen to describe an on-chip DMA controller. Thus, a rejection of independent claim 1 follows that utilizes the May'948 Patent, which incorporates by reference the reference of U.S. Patent Number 4,680,698, issued to Edwards *et al.* (hereafter the "Edwards'698 Patent"), and further in view of the "Transputer Reference Manual", published by Inmos Ltd., 1988 (hereafter the "Transputer Manual").

6. Further, also upon review of the references cited in the Request for Reexamination on page 11 (as well as pages 26 and 27) that teach of on-chip DMA controllers, the examiner notes that the reference of U.S. Patent 4,989,113, issued to Hull, Jr. *et al.* can be interpreted as teaching the other features that are required by the current claim language. Thus an additional rejection follows which utilizes this reference, and is discussed more fully below.

***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. **Claims 1-6** are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Number 4,989,113, issued to Hull, Jr. *et al.* (hereafter "Hull").

Regarding ***claim 1***, Hull Jr. discloses a microprocessor [see Abstract], which comprises

a main central processing unit [CPU 12 and controller 14] and a separate direct memory access central processing unit [DMA control 22] in a single integrated circuit comprising said microprocessor [see Fig. 1],

said main central processing unit [CPU 12 and controller 14] having an arithmetic logic unit [see Fig. 2, ALU 48],

a first push down stack [data registers 50a through 50h, collectively referred to as registers 50] with a top item register [data register 50a] and a next item register [data register 50b], connected to provide inputs to said arithmetic logic unit [see Fig. 2; also see col. 8, lines 51-55],

an output of said arithmetic logic unit being connected to said top item register [see Fig. 2],

said top item register also being connected to provide inputs to an internal data bus [see col. 8, lines 51-55],

said internal data bus being bidirectionally connected to a loop counter [see col. 9, lines 54-67],

said loop counter being connected to a decrementer [see col. 9, lines 54-67, whereby "CPU 12 interprets the absence of a displacement signal as an increment or decrement the contents of register 54 used in repetitive operation."],

said internal data bus being bidirectionally connected to a stack pointer [see col. 16, lines 23-55, whereby the system utilizes a "pipelining" of the instruction codes], return stack pointer [see col. 9,lines 36-67], mode register [index registers 68a and 68b, se col. 10, lines 33-55] and instruction register [auxiliary register 54, see col. 9, lines 4-61],

said internal data bus being connected to a memory controller [controller 14, see Figs. 1 and 4],

to a Y register of a return push down stack [registers 68, see col. 10, line 33-col. 11, line 14],

an X register [register 205] and a program counter [program counter 92, see col. 16, line 22-col. 18, line 9],

said Y register, X register and program counter providing outputs to an internal address bus [see Figs. 1, 2, and 4],

said internal address bus providing inputs to said memory controller and to an incrementer [see col. 17, line 60-col. 18, line 9],

said incrementer being connected to said internal data bus [see col. 16, lines 38-55],

said direct memory access central processing unit [DMA control 22] providing inputs to said memory controller [controller 14, see Figs. 1 and 4, also see col. 18, lines 10-53],

said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory [see Fig. 1, RAMs 16 and 18].

Regarding ***claim 2***, Hull, Jr. discloses the microprocessor discussed above in claim 1, and further teaches that said memory controller includes a multiplexing means [interface ports 24 and 26] between said central processing unit and said address/data bus [see Figs. 1 and 3], said multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus [see col. 13, line 38-col. 14, line 46].

Regarding ***claim 3***, Hull, Jr. discloses the microprocessor discussed above in claim 1, and further teaches that said memory controller includes means for fetching instructions for said central processing unit on said address/data bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle [see col. 13, lines 26-37].

Regarding ***claim 4***, Hull, Jr. discloses the microprocessor discussed above in claim 3, and further teaches of means connected to said means for fetching instructions for determining if multiple instructions fetched by said means for fetching instructions require a memory access [see col. 13, lines 26-37], said means for fetching instructions fetching additional multiple instructions if the multiple instructions do not require a memory access [see col. 13, lines 26-37].

Regarding ***claim 5***, Hull, Jr. discloses the microprocessor discussed above in claim 3, and further teaches that said microprocessor and a dynamic random access memory are contained in a single integrated circuit [see Fig. 1] and said means for fetching instructions includes a column latch for receiving the multiple instructions [instruction cache 36, see Fig. 1; also see col. 5, line 41-col. 6, line 12].

Regarding ***claim 6***, Hull, Jr. discloses the microprocessor discussed above in claim 1, and further teaches that said microprocessor includes a sensing circuit and a driver circuit [interrupt logic 250], and an output enable line for connection between the random access memory, said sensing circuit and said driver circuit, said sensing circuit being configured to provide a ready signal when said output enable line reaches a predetermined electrical level [see col. 18, lines 10-53], said microprocessor being configured so that said driver circuit provides an enabling signal on said output enable line responsive to the ready signal [see col. 18, lines 10-53].

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claims 1-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Number 4,758,948, issued to May *et al.* (hereafter "May'948"), which incorporates by reference the reference of U.S. Patent Number 4,680,698, issued to Edwards *et al.* (hereafter Edwards'698 Patent"), further in view of the "Transputer Reference Manual", published by Inmos Ltd., 1988 (hereafter the "Transputer Manual").

Regarding ***claim 1***, May'948 discloses a microprocessor [see Fig. 1], which comprises

a main central processing unit [CPU 12, see Figs. 1 and 2] and *a separate memory access processing unit* [external memory interface 23, seen in Fig. 1] in a single integrated circuit comprising said microprocessor [see Fig. 1],

said main central processing unit [CPU 12, see Figs. 1 and 2] having an arithmetic logic unit [see Fig. 2, ALU 30, also see col. 4, lines 52 and 53, wherein "The CPU 12 incorporates an arithmetic logic unit (ALU)..."],

a first push down stack [see Fig. 2, whereby the A, B and C registers 54, 55, and 56, respectively, within the Priority 1 register bank operate as a first push down stack] with a top item register [A register 54] and a next item register [B register 55], connected to provide inputs to said arithmetic logic unit [see col. 8, lines 47-56, wherein "The A, B, and C register stack 54,

55, and 56 are the sources and destinations for most arithmetic and logical operations. They are organised as a stack so that the loading of a value into the A register is preceded by relocating the existing contents of the B register into the C register and from the A register into the B register. Similarly storing a value derived from the A register causes the contents of the B register to be moved into the A register and the contents of the C register into the B register."],

an output of said arithmetic logic unit being connected to said top item register [see Fig. 2, whereby the Z bus includes an output from the ALU 30 and an input to the A register 54],

said top item register also being connected to provide inputs to an internal data bus [see Fig. 2, whereby the data bus 31 is connected to the A register 54],

said internal data bus [data bus 31] being bidirectionally connected to a loop counter [being interpreted as the workspace pointer WPTR REG register 51 and the O REG register 57, seen in Fig. 3, whereby the Edwards'698 Patent states on cols. 15 and 16 within the procedure "load from workspace and increment (function code 3)", the purpose of the function includes "to facilitate the use of workspace locations as loop counters, incrementing towards zero", and includes the definition "WPTR + OREG := AREG + 1"],

said loop counter being connected to a decrementer [the Edwards'698 Patent states on cols. 15 and 16 within the procedure "load from workspace and increment (function code 3)", the purpose of the function includes "to facilitate the use of workspace locations as loop counters, incrementing towards zero", thereby effectively acting as a decrementer],

said internal data bus [data bus 31] being bidirectionally connected to a stack pointer [see Fig. 3 IPTR S 65, also see col. 9, lines 59-68, wherein "Location 65 is used when a process is not the current process to hold a pointer (IPTR) to the next instruction to be executed by the process when it becomes the current process."], return stack pointer [see Fig. 3, LINK S 66, also see col. 9, lines 59-68, wherein "Location 66 is used to store a workspace pointer of a next process on a link list or queue of processes awaiting execution."], mode register [see Fig. 3, STATE S 67, also see col. 9, lines 59-68, wherein "Location 67 is normally used to contain an indication of the state of a process performing an alternative input operation or as a pointer for copying of a block of data."; additionally see col. 7, line 69-col. 8, line 7, wherein "PRI FLAG" is a "1 bit register or flag 47 for indicating the priority 0 or 1 of the currently executing process."] and instruction register [IB Reg 34, also see col. 7, lines 29-31, wherein "Each instruction derived from the program sequence for the process is fed to an instruction buffer 34."],

said internal data bus being connected to a memory controller [memory interface 14],

to a Y register of a return push down stack [BPTR REG 52, see Figs. 2 and 4],

an X register [FPTR REG 53, see Figs. 2 and 4] and a program counter [byte counter 111, see Fig. 12],

said Y register, X register and program counter providing outputs to an internal address bus [Z bus 81, see Figs. 2, 12, and 13],

said internal address bus providing inputs to said memory controller and to an incrementer [see col. 12, lines 35-54, wherein "the pointer register 122 incorporates an

incrementor so that as each byte is received the pointer increments to the memory destination address for the next byte of the input message."; also see Fig. 13],

said incrementer being connected to said internal data bus [see Fig. 13],

s*aid memory access processing unit* [external memory interface 23, seen in Fig. 1] providing inputs to said memory controller [see Fig. 1 and 2, whereby external memory interface 23 provides inputs to the memory interface 14 ],

said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory [see Fig. 10, whereby memory interface 14 has an address/data bus 33 and 31, and also a plurality if control lines providing input to RAM, see Fig. 1].

However, the May'948 Patent does not expressly state if th*e separate memory access processing unit* is a separate direct memory access central processing unit being in a single IC with the main central processing unit, and subsequently, if said direct memory access central processing unit provides inputs to said memory controller.

The Transputer Manual discloses a microprocessor [see Figure 1.1 on page 108], which comprises

a main central processing unit [32 bit Processor, see Figure 1.1 on page 108] and a separate direct memory access central processing unit [see page 150, wherein "DMA may also inhibit an internally running program from accessing external memory....DMA allows a bootstrap program to be loaded into external RAM ready for execution after reset."; also see pages 132-151, which shows various configurations of the EMI] in a single integrated circuit

comprising said microprocessor [see page 150, whereby the External Memory Interface allows for the programmed control of direct memory access; see Figure 1.1 on page 108],

said main central processing unit having a first push down stack [the A, B, and C registers, seen in Figs. 3.1 and 3.3; also see page 11, wherein "The A, B and C registers which form an evaluation stack."] with a top item register [Register A] and a next item register [B register], connected to provide inputs to said arithmetic logic unit [see page 111, wherein A, B, and C are sources and destinations for most arithmetic and logical operations. Loading a value into the stack pushes B into C, and A into B, before loading A."],

an internal data bus being bidirectionally connected to a loop counter [see page 115, wherein "This uses a workspace locator as a counter of the parallel construct components which have still to terminate. The counter is initialized to the number of components before the process is started. Each component ends with an end process instruction which decrements and tests the counter. For all but the last component, the counter is non-zero and the component is descheduled. For the last component, the counter is zero, and the main process continues."],

said loop counter being connected to a decrementer [see page 115],

said direct memory access central processing unit [being the External Memory Interface, seen in Fig. 1.1 on page 108] providing inputs to said memory controller [see page 108, whereby the External Memory Interface provides an input to the 32-bit Processor],

said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory [see Fig. 1.1 on page 108].

The May'948 Patent & the Transputer Manual are combinable because they are from the same field of endeavor, both being drawn to an Inmos Transputer microprocessor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the DMA teachings described in the Transputer Manual within the system described the May'948 Patent. The suggestion/motivation for doing so would have been that the system described in the May'948 Patent would be easily adapted to incorporate the direct memory access controller teachings described in the Transputer Manual, as the components and systems appear to be identical. Therefore, it would have been obvious to combine the teachings of the Transputer Manual with the system of the May'948 Patent to obtain the invention as specified in claim 1.

Regarding ***claim 2***, the May'948 Patent and the Transputer Manual disclose the microprocessor discussed above in claim 1, and the May'948 Patent further teaches that said memory controller includes a multiplexing means [condition multiplexor 36, seen in Fig. 2] between said central processing unit and said address/data bus [see Fig. 2], said multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus [see col. 7, lines 32-35]. Additionally, the Transputer Manual further teaches of including a multiplexing means [see Fig. 7.8 on page 140, Row/Column address multiplexer], with said multiplexing means being connected and configured to provide row addresses, column addresses and data on said address/data bus [see Fig. 7.8 on page 140, Row/Column address multiplexer].

Therefore, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the multiplexer teachings described in the Transputer Manual within the system described the May'948 Patent. The suggestion/motivation for doing so would have been that the system described in the May'948 Patent would be easily adapted to incorporate the further teachings described in the Transputer Manual, as the components and systems appear to be identical. Therefore, it would have been obvious to combine the further teachings of the Transputer Manual with the system of the May'948 Patent to obtain the invention as specified in claim 2.

Regarding ***claim 3***, the May'948 Patent and the Transputer Manual disclose the microprocessor discussed above in claim 1, and the May'948 Patent further teaches that said memory controller includes means for fetching instructions for said central processing unit on said address/data bus, said means for fetching instructions being configured to fetch multiple sequential instructions in a single memory cycle [see col. 6, lines 4-24; also see col. 7, lines 15-39].

Regarding ***claim 4***, the May'948 Patent and the Transputer Manual disclose the microprocessor discussed above in claim 3, and the May'948 Patent further teaches of means connected to said means for fetching instructions for determining if multiple instructions fetched by said means for fetching instructions require a memory access [see col. 6, lines 4-24; also see col. 7, lines 15-39], said means for fetching instructions fetching additional multiple instructions

if the multiple instructions do not require a memory access [see col. 6, lines 4-24; also see col. 7, lines 15-39].

11. **Claims 7 and 8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hull, Jr. in view of Kato *et al.* (U.S. Patent Number 4,766,567).

Regarding ***claim 7***, Hull, Jr. discloses the microprocessor discussed above in claim 1, and further teaches of **a system clock** to said main central processing unit, said main central processing unit and **said system clock** being provided in a single integrated circuit [see Figs. 1 and 4, being clock generator 200, seen in Fig. 4, and read in col. 15, lines 7-27].

However, Hull, Jr. does not expressly describe the system clock as being a ring oscillator variable speed system clock connected to said main central processing unit, with the main central processing unit and the ring oscillator variable speed system clock being provided in a single integrated circuit.

Kato discloses a microprocessor having a ring oscillator variable speed system clock connected to said main central processing unit, said main central processing unit and said ring oscillator variable speed system clock being provided in a single integrated circuit [clock generator 4, see Figs. 1 and 4; also see col. 10, line 51-col. 11, line 7].

Hull, Jr. & Kato are combinable because they are from the same field of endeavor, being semiconductor systems having two distinct clock generators. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to include the ring oscillator teachings of Kato in the system taught by Hull, Jr. The suggestion/motivation for doing so would have been that the clock generator of Hull, Jr. would become more efficient, as using a ring oscillator would lower output frequency in proportion to the speed of the data processing circuit which is also lowered due to the drop of power supply voltage, being a characteristic of using a ring oscillator recognized by Kato on col. 11, lines 2-7. Therefore, it would have been obvious to combine the ring oscillator teachings of Kato with the system of Hull, Jr. to obtain the invention as specified in claim 7.

Regarding ***claim 8***, Hull, Jr. and Kato disclose the microprocessor discussed above in claim 7, and Hull, Jr. further teaches that said memory controller includes an input/output interface connected to exchange coupling control signals, addresses and data with said main central processing unit [see Fig. 1], said microprocessor additionally including a second clock independent [timer 40] of said ring oscillator variable speed system clock connected to said input/output interface [whereby timer 40 is independent of clock generator 200, seen in Figs. 1 and 4].

**STATEMENT OF REASONS FOR PATENTABILITY AND/OR CONFIRMATION**

The following is an examiner's statement of reasons for patentability and/or confirmation of the claims found patentable in this reexamination proceeding:

**Claims 9 and 10** are confirmed as patentable.

Regarding dependent ***claim 9***, the examiner does believe that the prior art of record expressly discloses the invention as claimed, particularly including the feature requiring the first push down stack has a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit. The prior art of Hull, Jr. teaches of stack elements, as seen in Fig. 2. However, Hull, Jr. fails to expressly teach of a third stack element configured as a RAM external to the single integrated circuit. Further, the reference of Muller (U.S. Patent 4,969,091), noted in the Request for Reexamination, teaches of implementing a push down stack. But, Muller fails to expressly teach the architecture that is required by the claim language, which requires a first plurality of stack elements configured as latches, a second plurality of stack elements configured as a random access memory, said first and second plurality of stack elements and said central processing unit being provided in a single integrated circuit, and a third plurality of stack elements configured as a random access memory external to said single integrated circuit. Thus,

the prior art of record is not seen to expressly disclose this architecture. Therefore, in the examiner's opinion, the claim is deemed patentable.

Any comments considered necessary by PATENT OWNER regarding the above statement must be submitted promptly to avoid processing delays. Such submission by the patent owner should be labeled: "Comments on Statement of Reasons for Patentability and/or Confirmation" and will be placed in the reexamination file.

***Conclusion***

12. Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that *ex parte* reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extensions of time in *ex parte* reexamination proceedings are provided for in 37 CFR 1.550(c).

13. In order to ensure full consideration of any amendments, affidavits or declarations, or other documents as evidence of patentability, such documents must be submitted in response to this Office action. Submissions after the next Office action, which is intended to be a final action, will be governed by the requirements of 37 CFR 1.116, after final rejection and 37 CFR 41.33 after appeal, which will be strictly enforced.

14. The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving Patent No. 5,530,890 throughout the course of this reexamination proceeding.

15. ALL correspondence relating to this ex parte reexamination proceeding should be directed as follows:

**Please mail any communications to:**

Attn: Mail Stop "Ex Parte Reexam"
Central Reexamination Unit
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Any inquiry concerning this communication should be directed to Joseph R. Pokrzywa at telephone number 571-272-7410.

Signed:

Joseph R. Pokrzywa
Primary Examiner
Central Reexamination Unit 3992
(571) 272-7410

Conferees:

/r.g.f./ OPQA

| Notice of References Cited | Application/Control No. 90/009,388 | Applicant(s)/Patent Under Reexamination 5530890 | |
|---|---|---|---|
| | Examiner JOSEPH R. POKRZYWA | Art Unit 3992 | Page 1 of 1 |

**U.S. PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Name | Classification |
|---|---|---|---|---|---|
| * | A | US-4,989,113 | 01-1991 | Hull, Jr. et al. | 710/22 |
| | B | US- | | | |
| | C | US- | | | |
| | D | US- | | | |
| | E | US- | | | |
| | F | US- | | | |
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**FOREIGN PATENT DOCUMENTS**

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**NON-PATENT DOCUMENTS**

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

# Index of Claims

| Application/Control No. | Applicant(s)/Patent under Reexamination |
|---|---|
| 90/009,388 | 5530890 |
| **Examiner** | **Art Unit** |
| JOSEPH R. POKRZYWA | 3992 |

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| Claim | | Date |
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| Final | Original | 10/5/09 |
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